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2020-02-11

FMX Data Flow Training

03-Dec-2019

Connected Home Division



PON HGU Datapath (Single Box) – LAN <--> PON

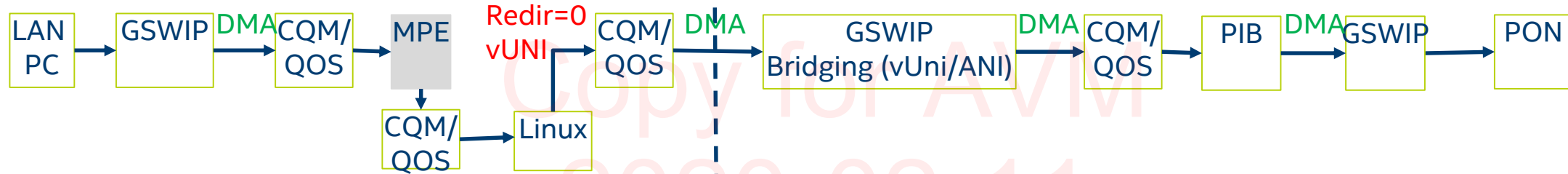
Upstream

FLM UNI->ANI Routing Data Flow with MPE Acceleration:

Share existing DMA as configured for PMAC0/1



FLM UNI->ANI Routing Data Flow with Linux Slow Path

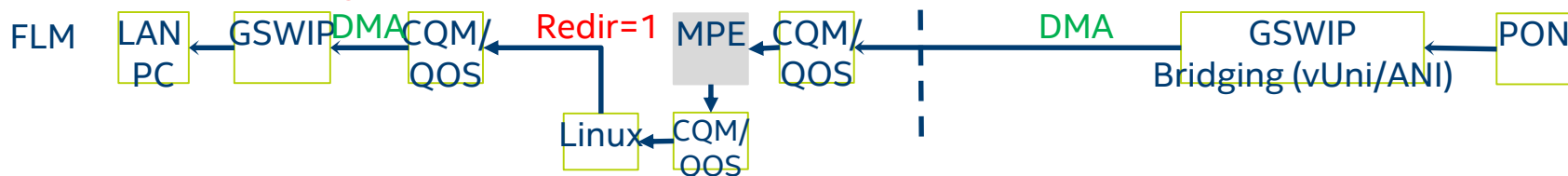


FLM ANI->UNI Routing Data Flow with MPE Acceleration:

5 proto tuple, don't care vUNI or vANI



FLM ANI->UNI Routing Data Flow with Linux Slow Path:



Downstream

- Port 0 - Mpe / CPU
- Port 2 - PON IP
- Port 3 & 4 - LAN
- Port 5/6 - vAni

HGU Model as per BBF TR-156

- Models HGU as if like it is a 2-box model (Ethernet Router + PON Modem).
- PON Modem and Ethernet RG – 2 separate virtual entities within a HGU.
- [BBF TR-156i4](#)

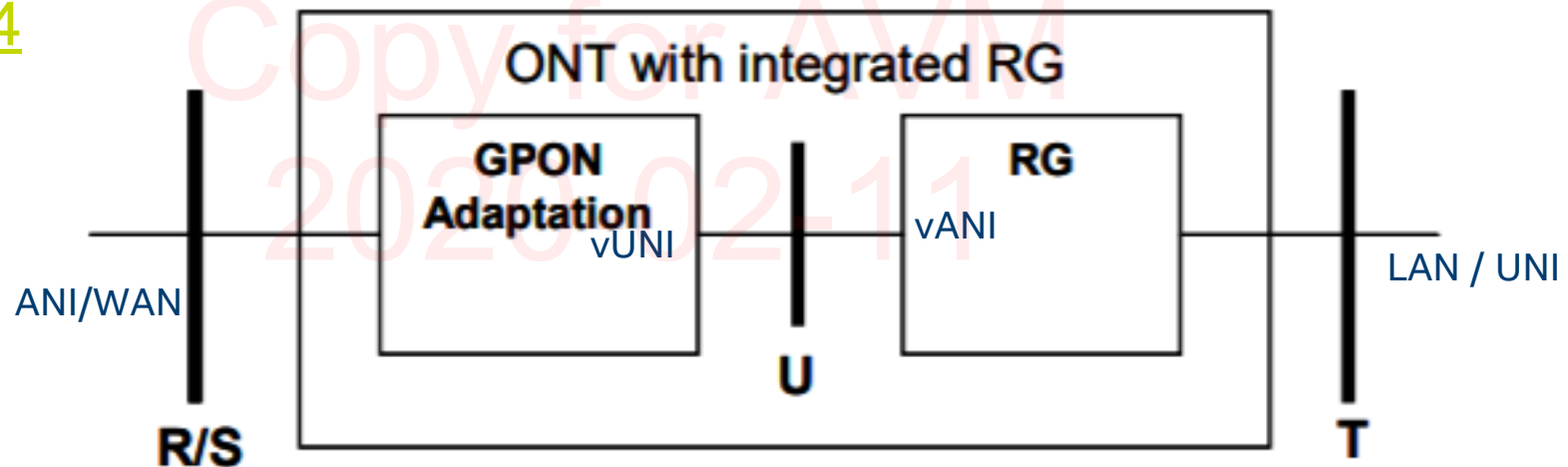


Figure 3 – ONT and RG as a single entity

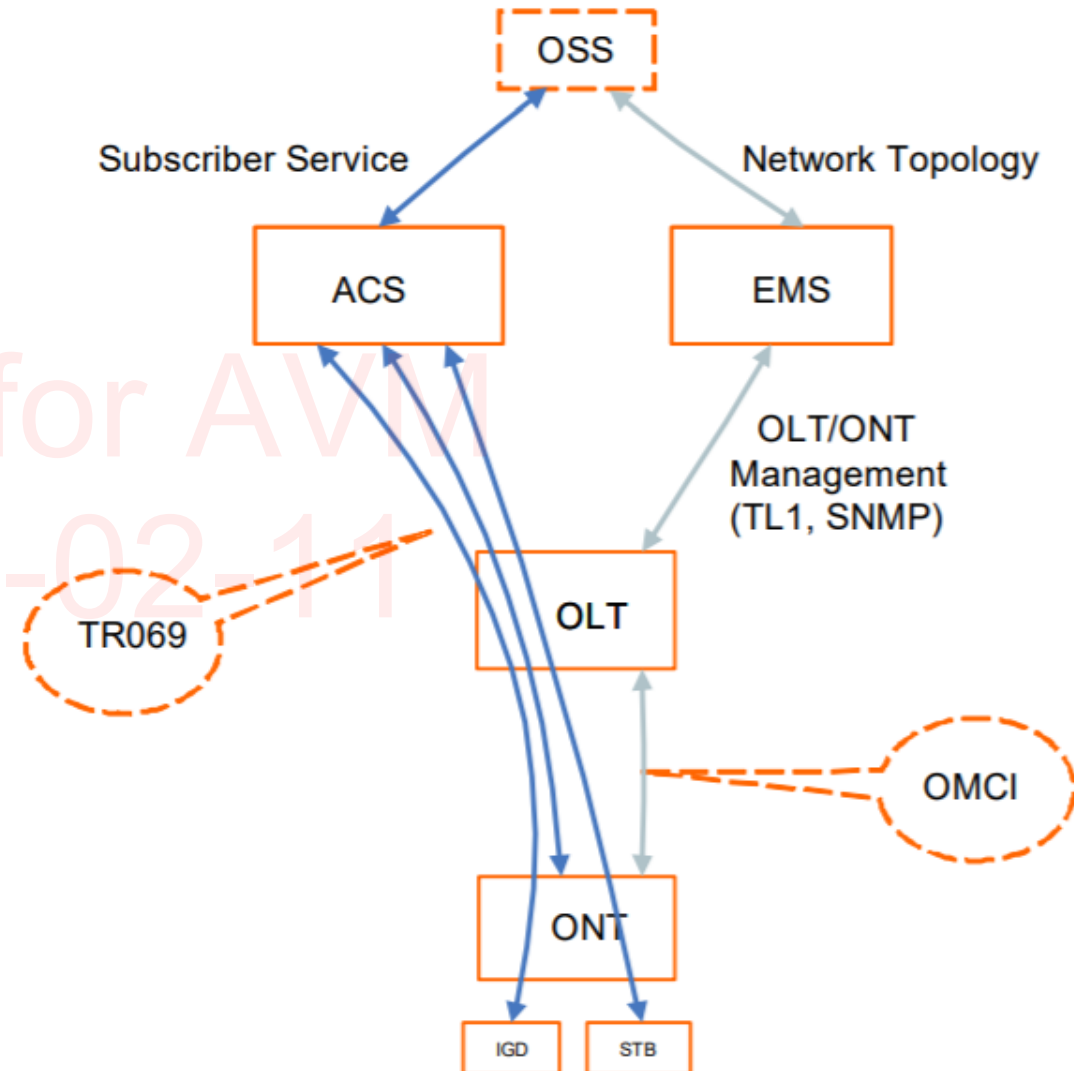
PON-CPE management model as per BBF TR-142

BBF TR-142:

Dual Management :

OMCI/SIEPON & TR-069 based

config & mgmt from OSS/BSS.



TR-069 and OMCI

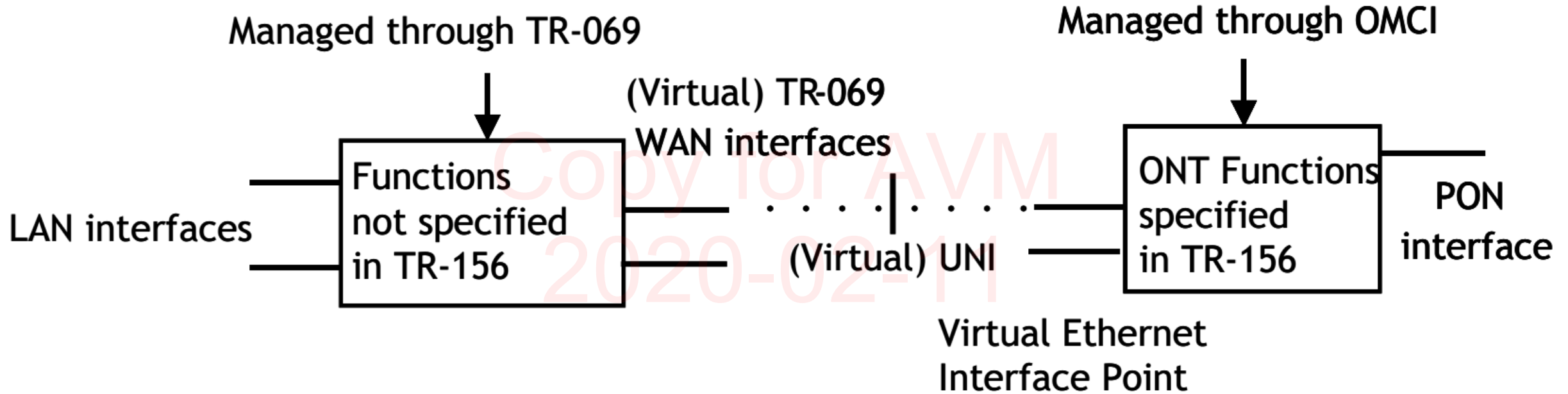


Figure 4: Concept of a Virtual UNI for OMCI and TR-069 domains of responsibilities

TR-069 and OMCI

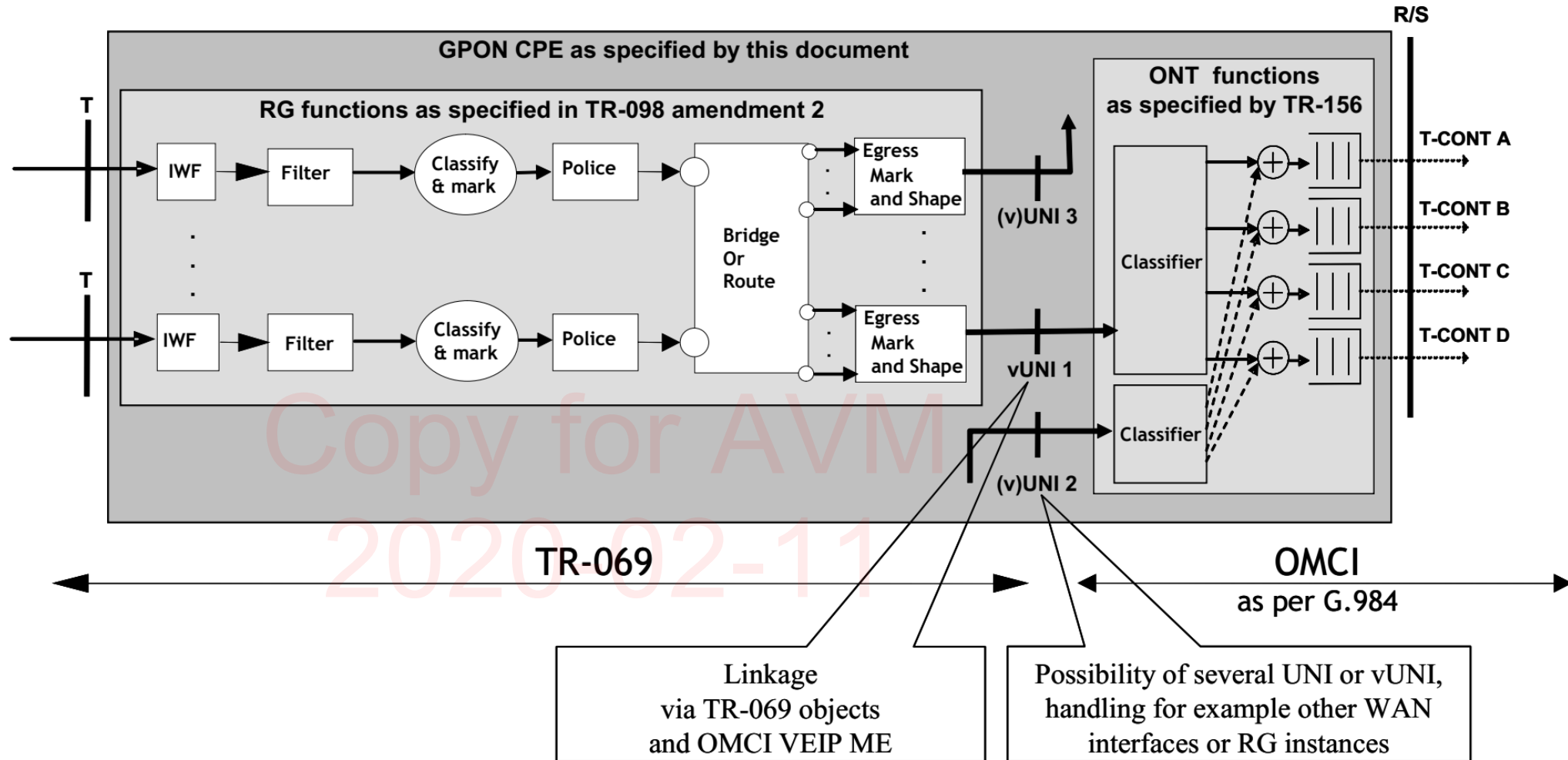


Figure 5: Representation of the upstream traffic; OMCI and TR-069 management of a multi-port single-subscriber GPON CPE

GSWIP Roadmap

Incremental feature support

GSWIP2.2

xRX300v2,
F25G/F25S/F24S

- + Per port backpressure
- + Buffer reservation
- + Double VLAN editing
- + Port trunking
- + 1588/PTP

GSWIP3.0

GRX350/550 GSWIP_L,
PAE

- + Central QoS path support
- + 5-tuple routing IPv4/IPv6/routing/NAT/6RD/Dslite
- + 4k (RTL parameter) routing entries
- + Tunnel decapsulation: L2TP/CAPWAP/GRE
- + L2NAT

GSWIP3.1

F-MX GSWIP-O

- No routing/tunnel
- No L2NAT
- + 10Gbps MAC
- + G.INT support
- + Bridging and counting at **interface level** (WLAN VAP, GPON GEM, VLAN)
- + Upto 68Gbps@666Mhz bandwidth
- + 31.7Mpps@666Mhz classification packet rate
- + OMCI bridging and VLAN function support
- + OAM delay and loss measurement
- + Enhanced 1588/PTP

GSWIP3.2

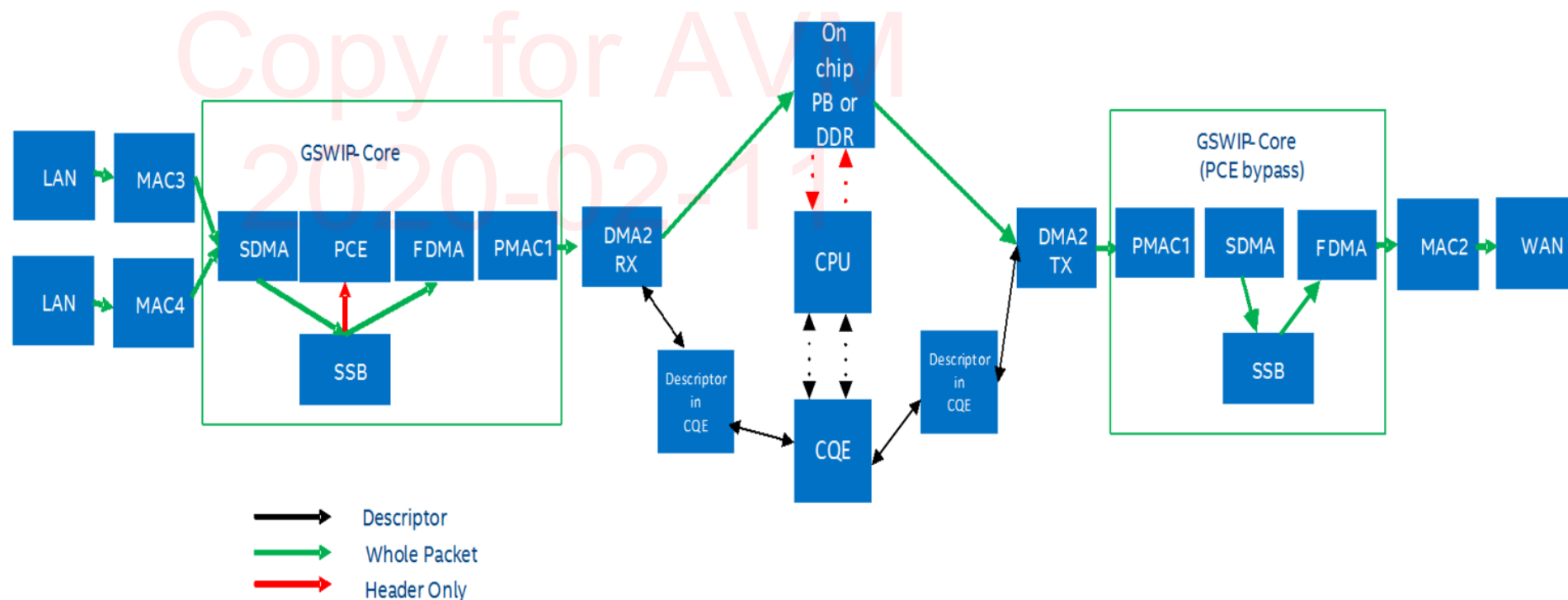
LGM GSWIP-O

- + Upto 81Gbps@800Mhz bandwidth
- + 38Mpps@800Mhz classification packet rate
- + Header-only mode support
- + MAC-in-MAC mode
- + Pre-parser priority classification
- + TCP/UDP/IP checksum verification/generation
- + Mirror of PCE bypass path
- + Pre-L2 header with configurable size
- + 802.11 traffic flow classification
- + PMAC Egress CRC insertion

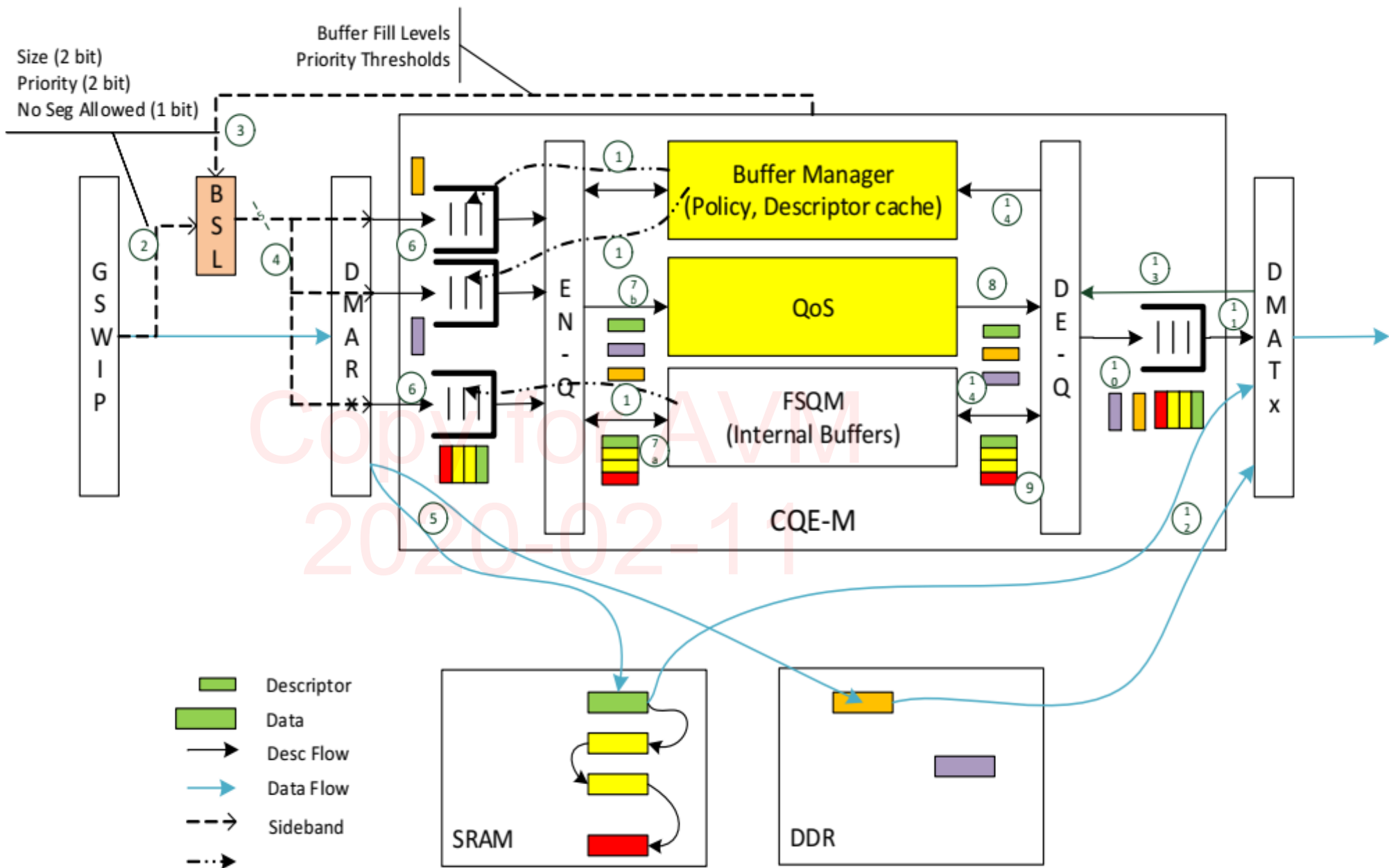
Data Flows: Upstream CQEM Mode

DMA/CQE determines to store packets either on chip PB or DDR based on traffic class and buffer usage

In PON mode, CQEM is always needed in upstream because of its TDM nature



QoS



CPU Cluster


GRX350
GRX550

Trusted
Core
Controls CPU
Access




- Control of CPU Access
- Secure platform (secure boot, secure storage,...)
- Control of Security zones
- Scrambled DDR access

CPU 1
Linux




HW ID

CPU 2
VoIP




HW ID

CPU 3
MPE
(add-on packet
handling)



HW ID


CPU 4
Linux OS
(Apps running on
core or Container)



HW ID

Crossbar with Hardware Gates
(only programmable by Trusted Core)


WAN




USB



Sec. Core DDR Zone



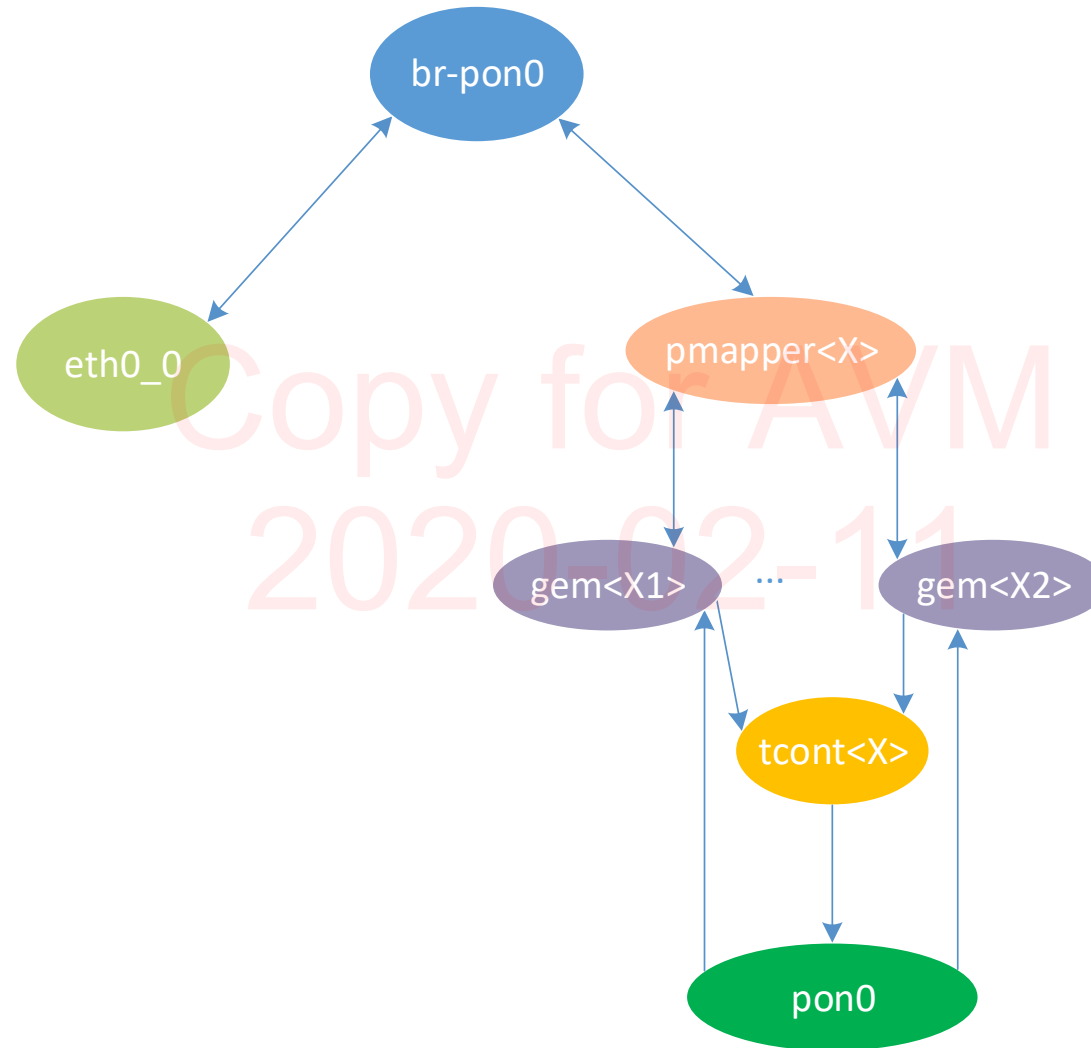
Linux DDR Zone



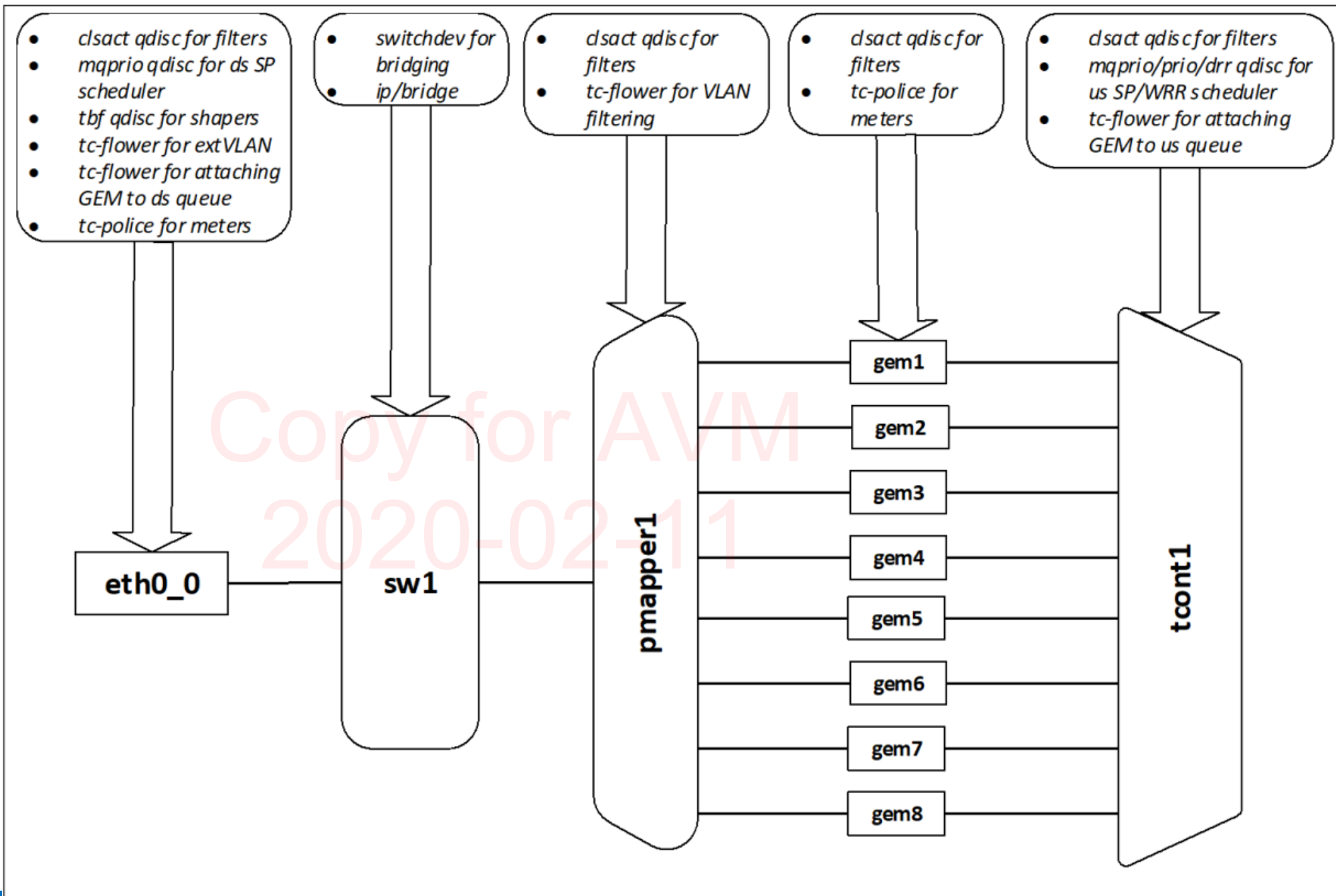
App DDR Zone

DDR Memory Regions
(HW enforced)

SFU/SFP PON Bridge – Linux config example

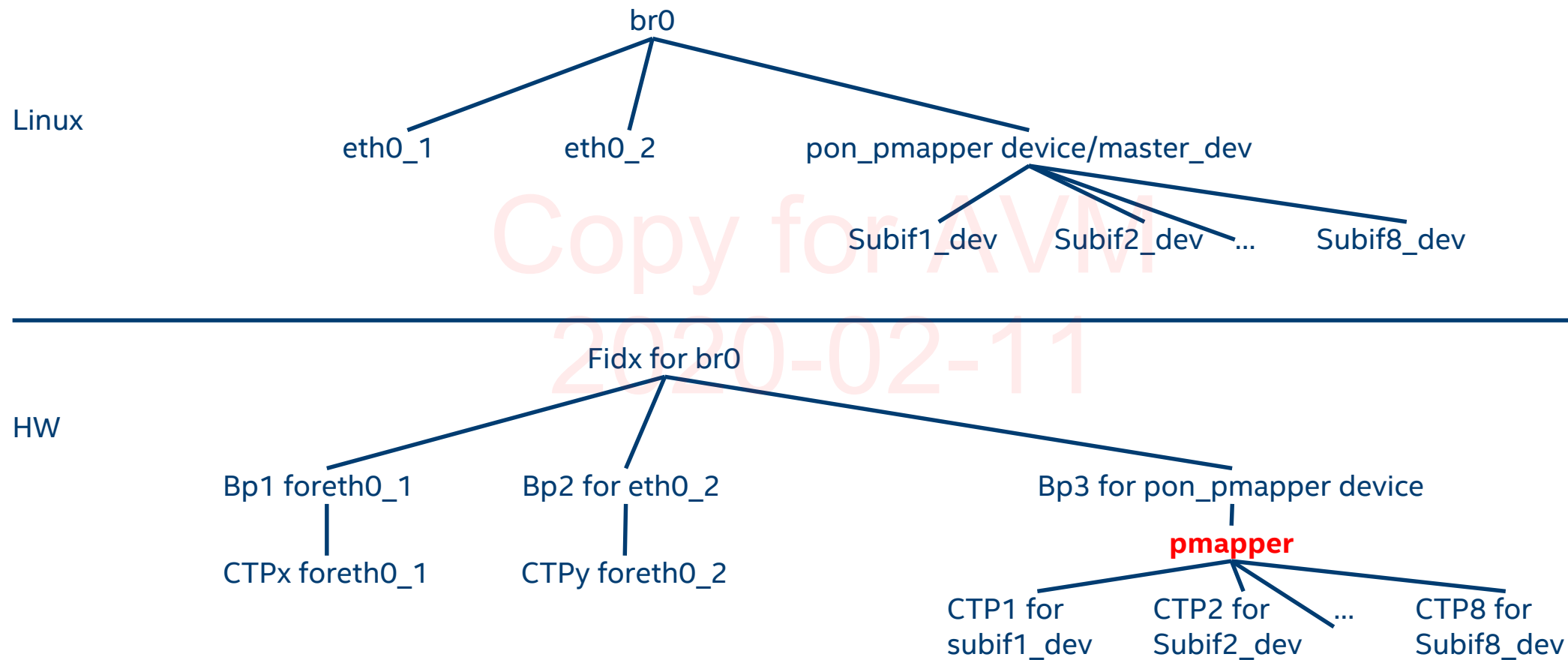


SW pmapper Config

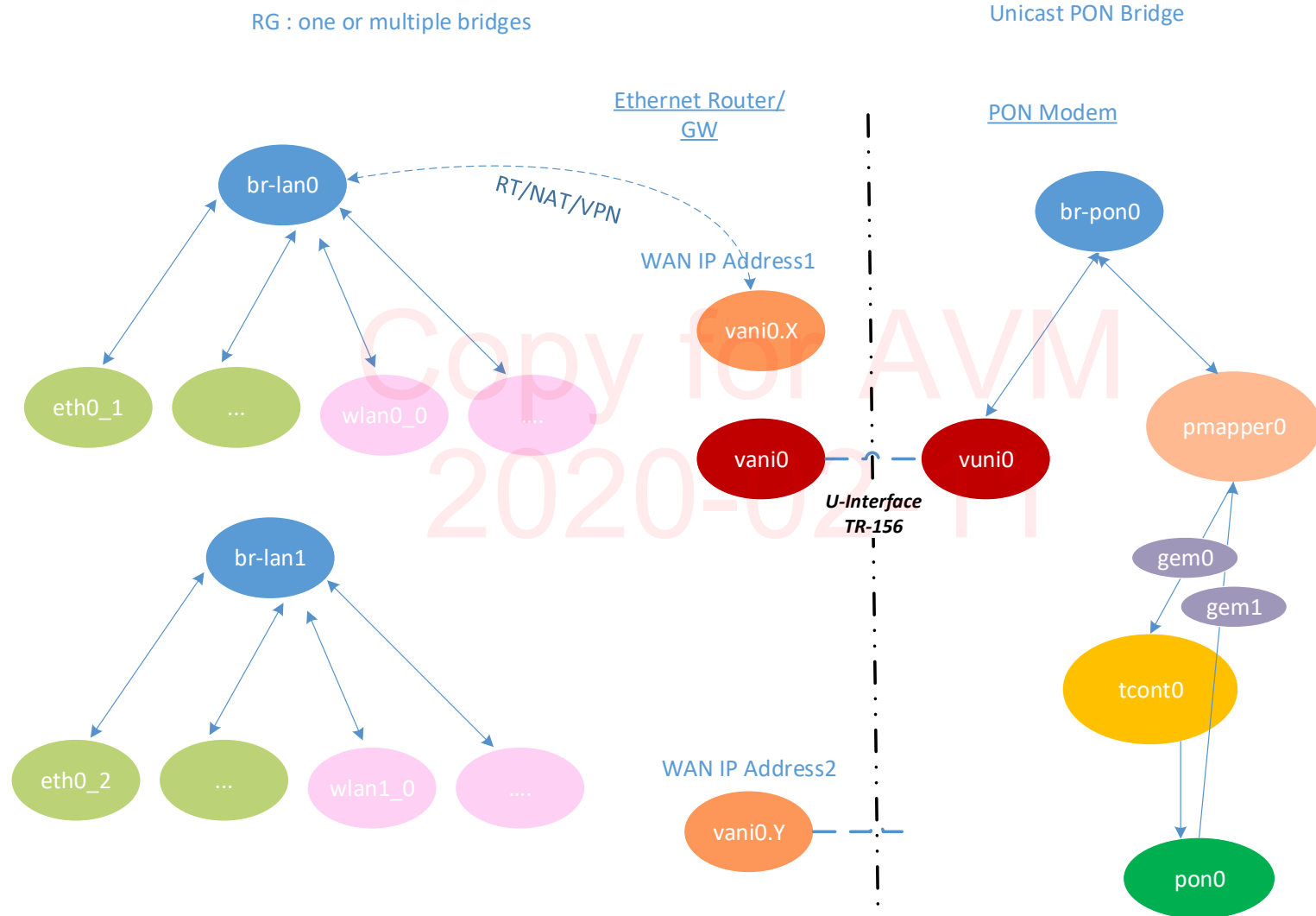


Connected Home Figure 15 OMCI Data Path and QoS Flow Mapped to Linux* Network Devices

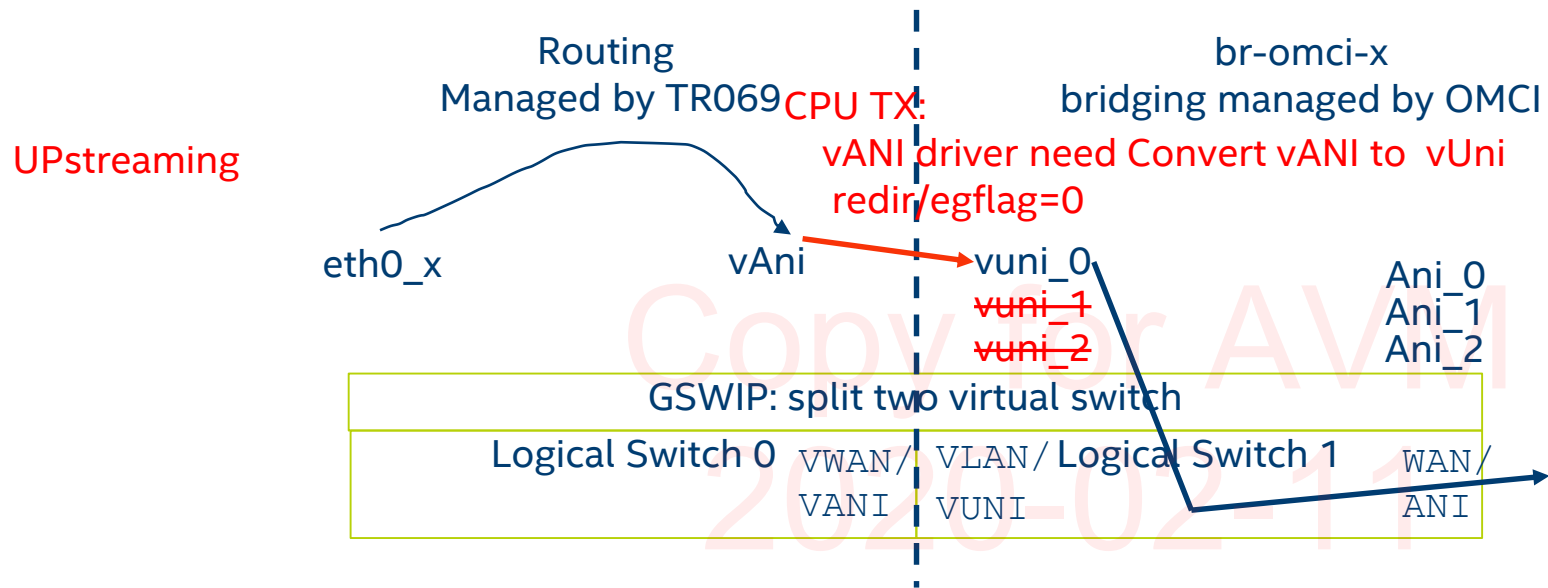
Datapath bridge port mapping via pmapper



HGU Linux Config example



PON HGU Datapath (Single Box)–vANI TX /Upstream



vANI driver need convert vANI to vUNI's device and subif

vAni driver's xmit/TX API:

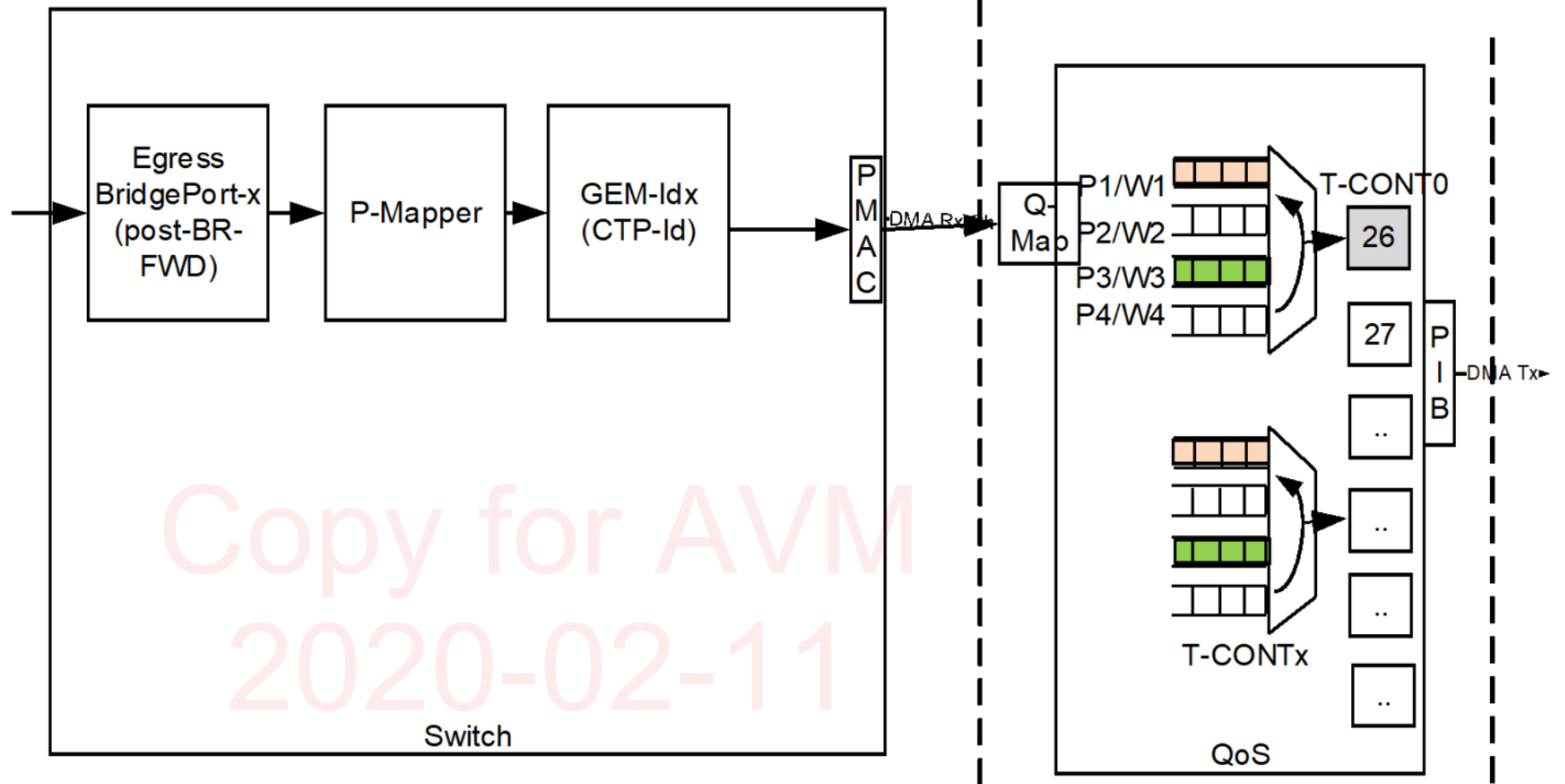
- convert vANI to vUNI_0 (skb->dev) and vUNI's dp_subif_t
- call dp_xmit

vAni no need rx API

dp_xmit

- redir/egflag must set to 0
- set up 1 BP and 1 CTP for vANI and VUNI respectively

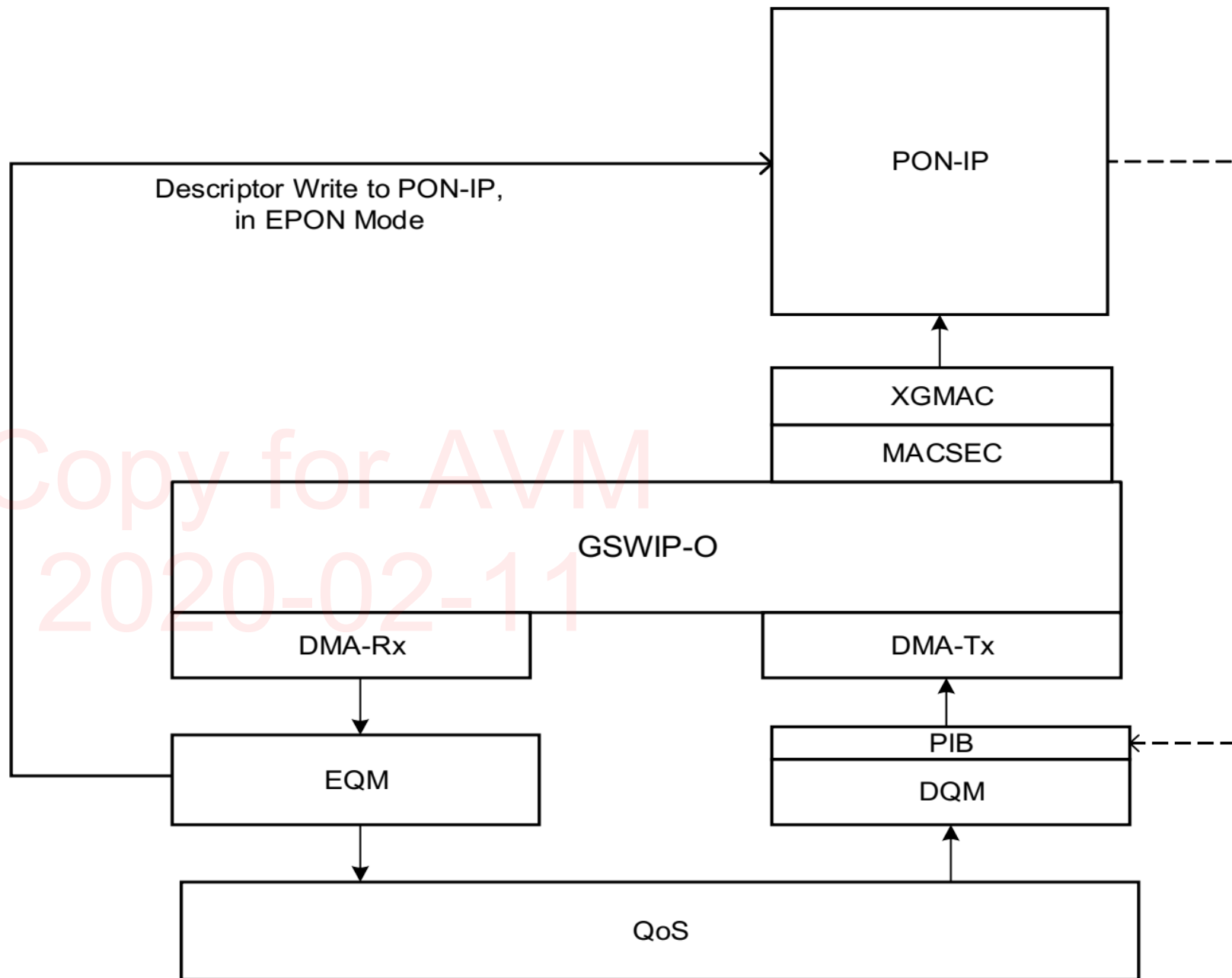
US PON-IP



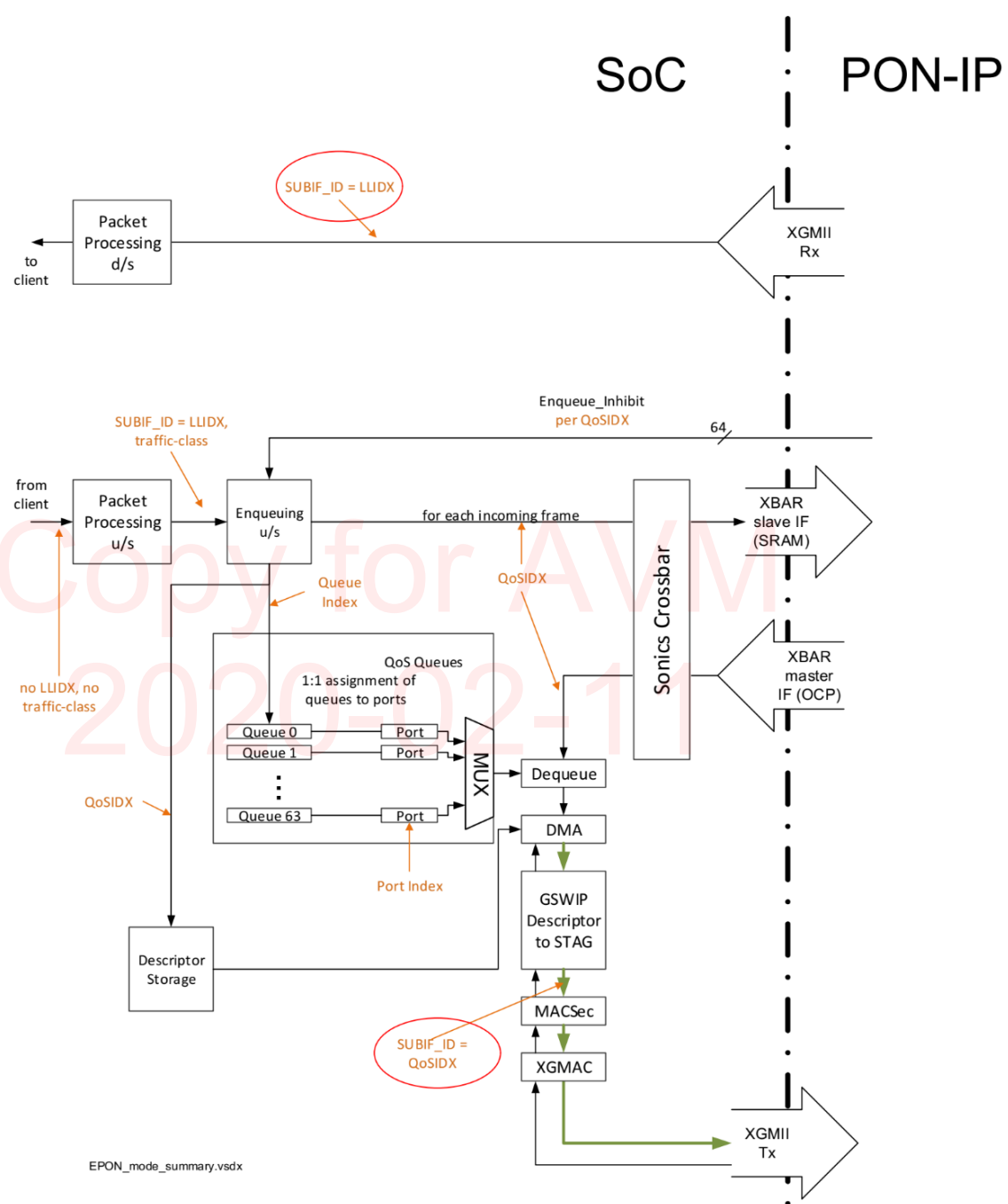
US_GPON_QOS

Upstream GPON QoS Flow

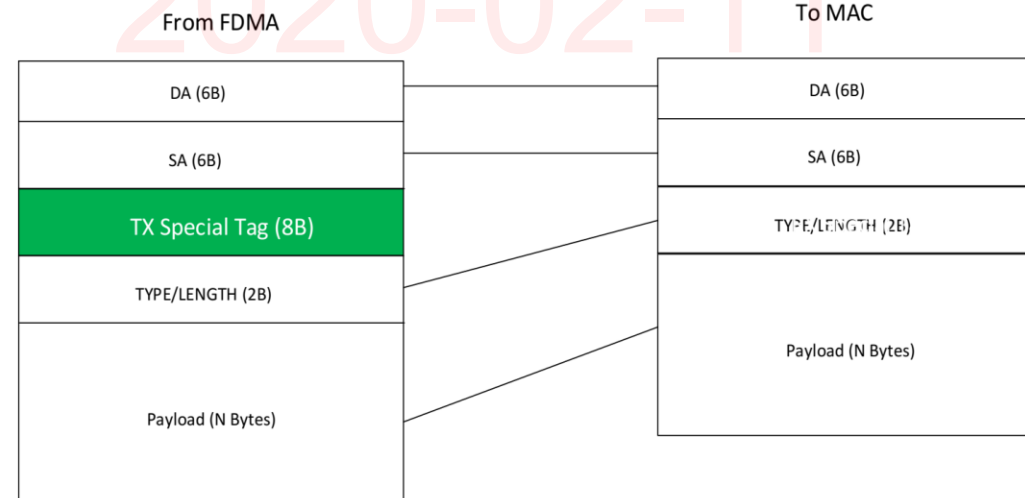
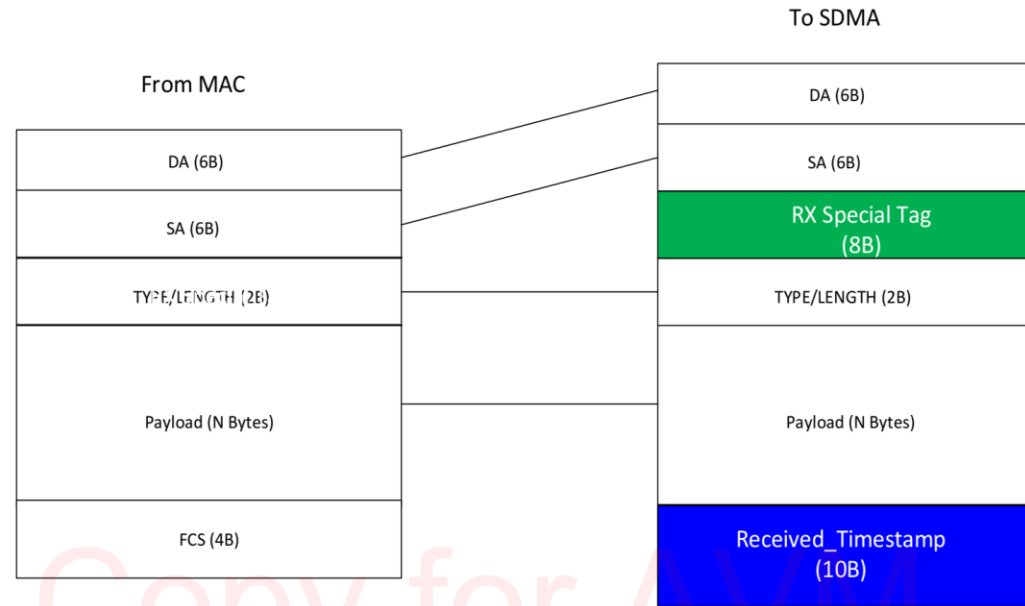
PON-IP Flow



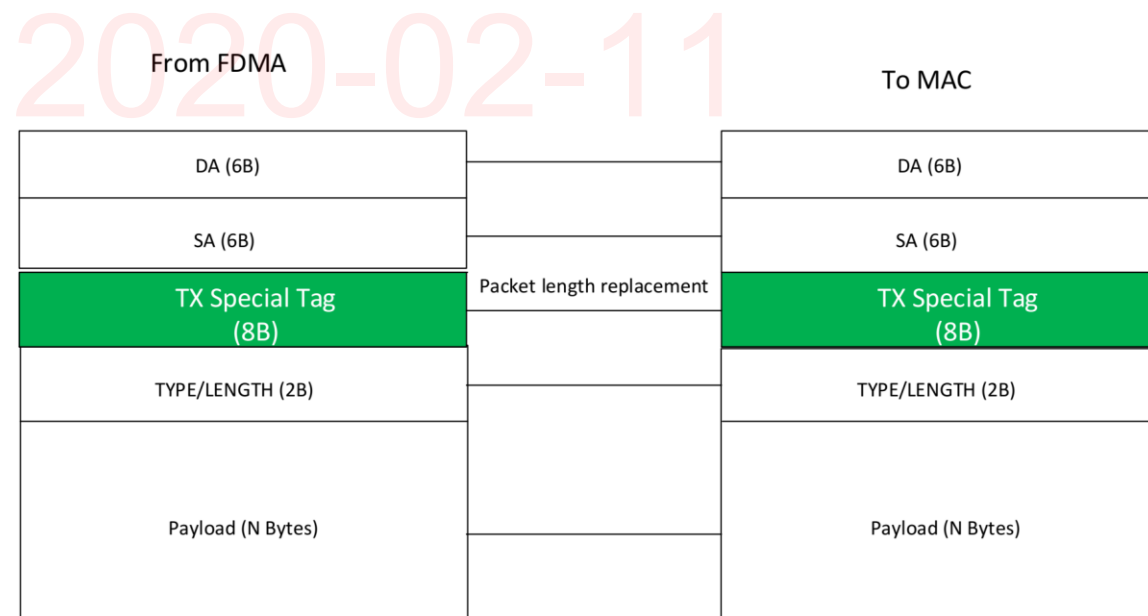
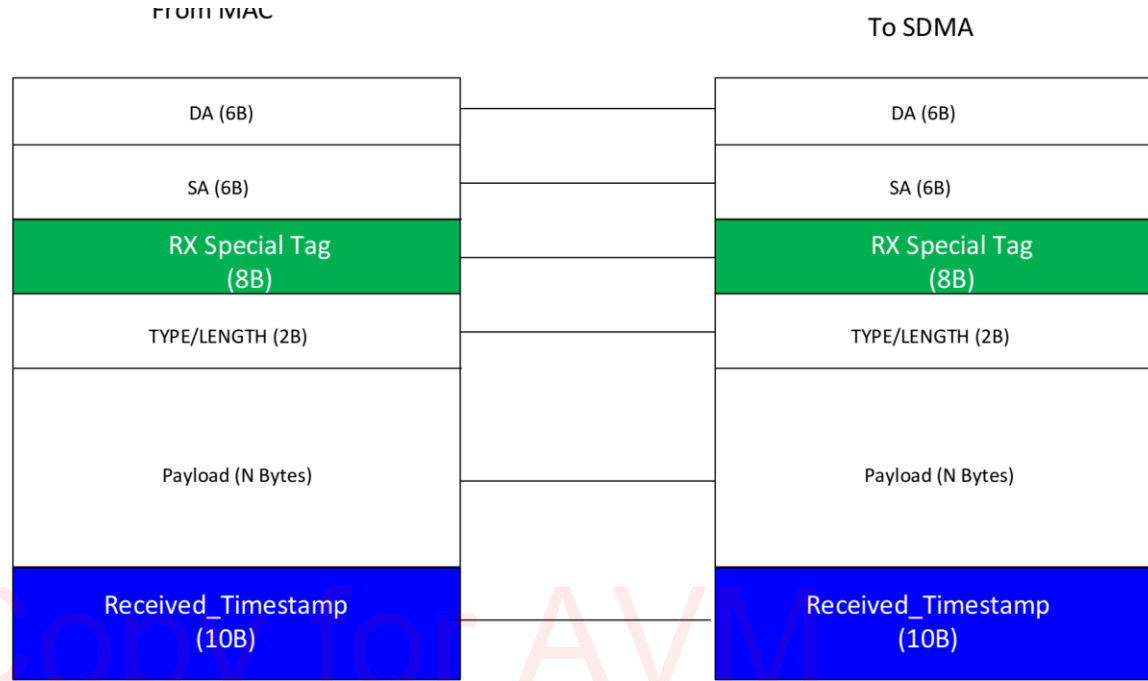
PON-IP US Flow



Special Tag Eth WAN



Special Tag PON WAN



Parser Results to CPU

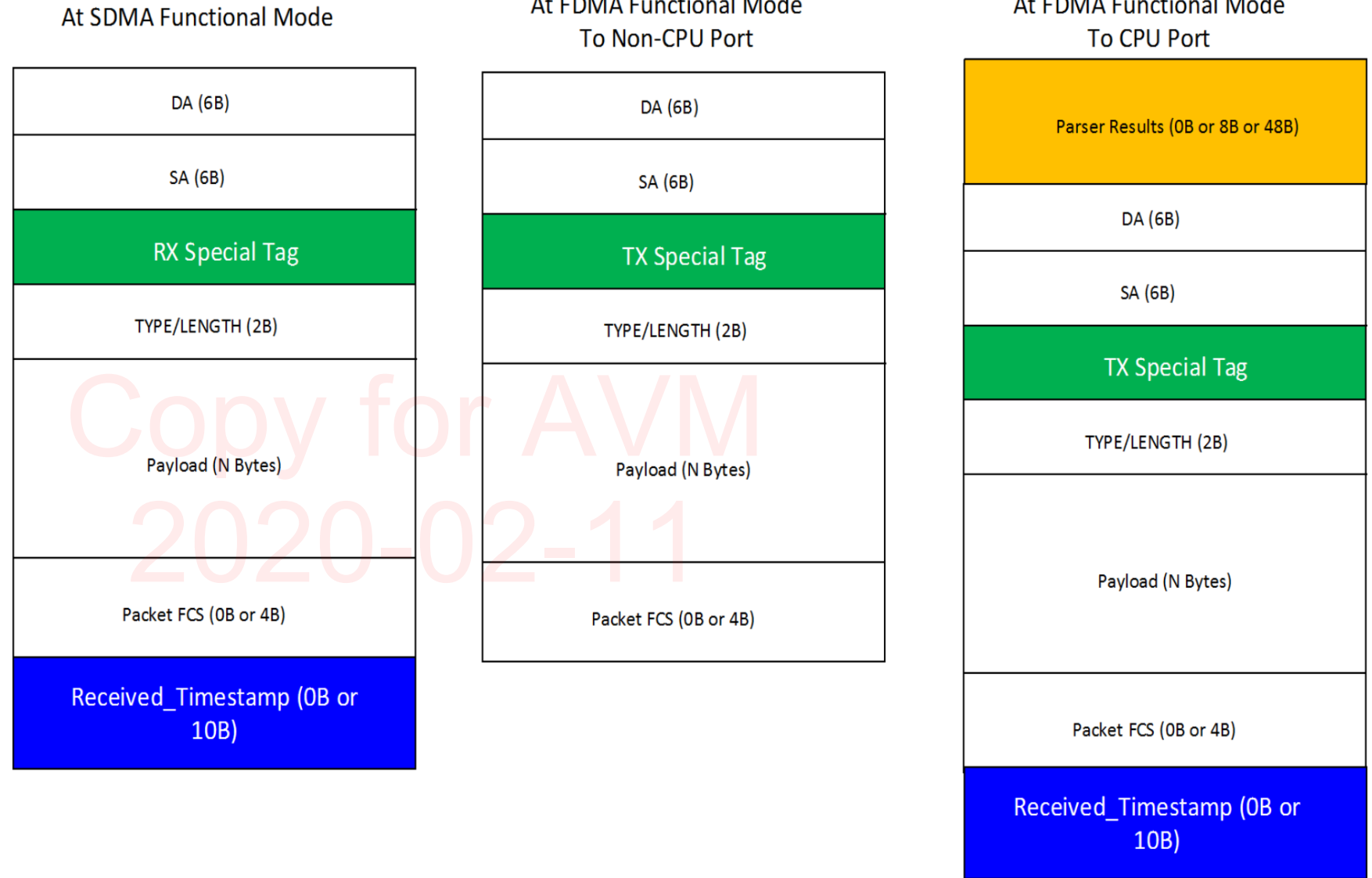
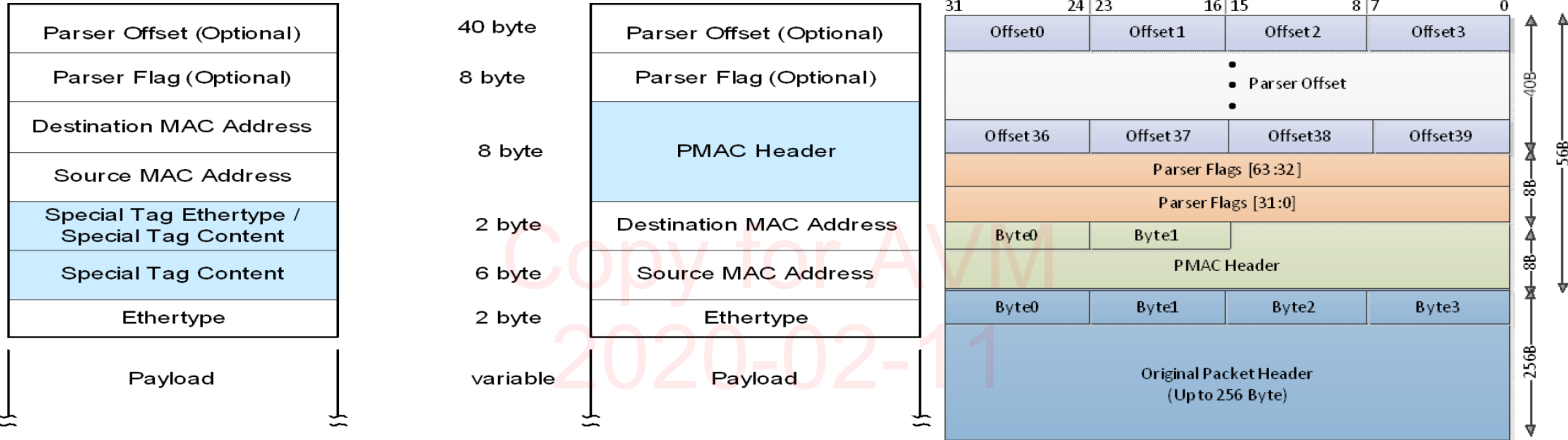


Figure 19 Packet Format At SDMA/FDMA Interface: Functional Mode

Parser Results + PMAC Header to CPU



Parser Flags (Microcode Output Flags)																															
Bit-31	Bit-30	Bit-29	Bit-28	Bit-27	Bit-26	Bit-25	Bit-24	Bit-23	Bit-22	Bit-21	Bit-20	Bit-19	Bit-18	Bit-17	Bit-16	Bit-15	Bit-14	Bit-13	Bit-12	Bit-11	Bit-10	Bit-9	Bit-8	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
LRO Exception Flag	L2TP Data Flag	UDP Hdr after 2nd IP Hdr	Inner IPv6 with Extension Header	EAPO L Flag	IP Fragment Flag	TCP Ack Flag	Outer IPv6 with Extension Header	IPv4 with Option Flag	IGMP Flag	UDP Hdr after 1st IP Hdr	TCP Flag	RT Exception Flag (CPU handled)	Inner IPv6 Flag	Inner IPv4 Flag	Outer IPv6 Flag	Outer IPv4 Flag	PPPoE Session Flag	SNAP encapsulated Flag	4th VLAN Tag Flag	3rd VLAN Tag Flag	2nd VLAN Tag Flag	1st VLAN Tag Flag	Special Tag Flag	Reserved (Future Use)	Reserved (Future Use)	Reserved (Future Use)	Length Encapsulated Flag	GRE Flag	CAP WAP Flag	Parser Error Flag	WoL Flag

Figure 7 Parser Bit Flags

Special Tag Format

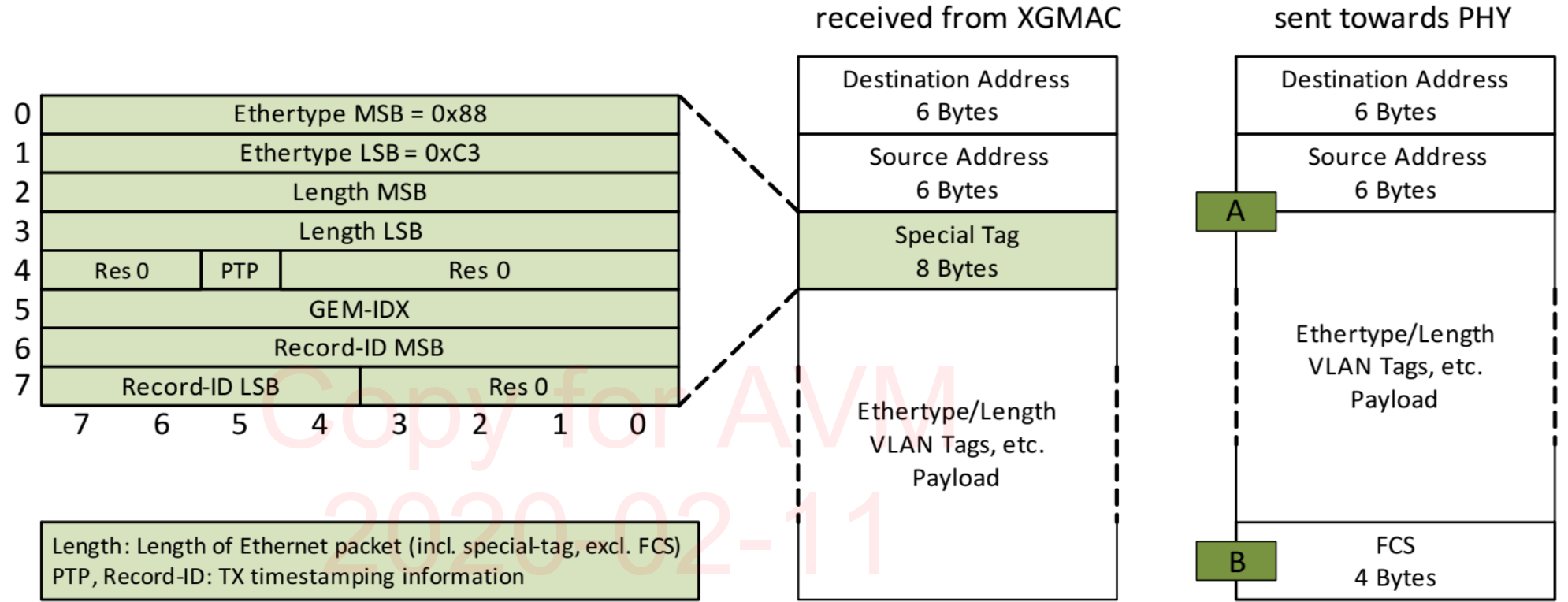
- Record_ID = PTP Sequence_ID
- EtherType = 0x88C3



Figure 215 Special Tag Handed by MAC Adaption Layer

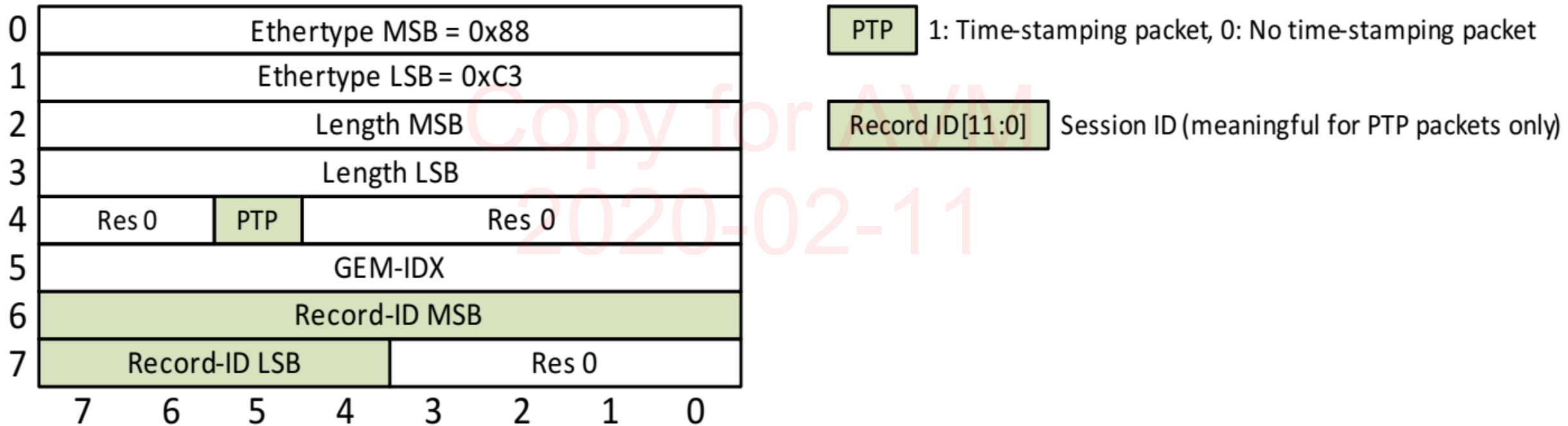
Special Tag PON US

TX packet processing (upstream)



Special Tag PON US

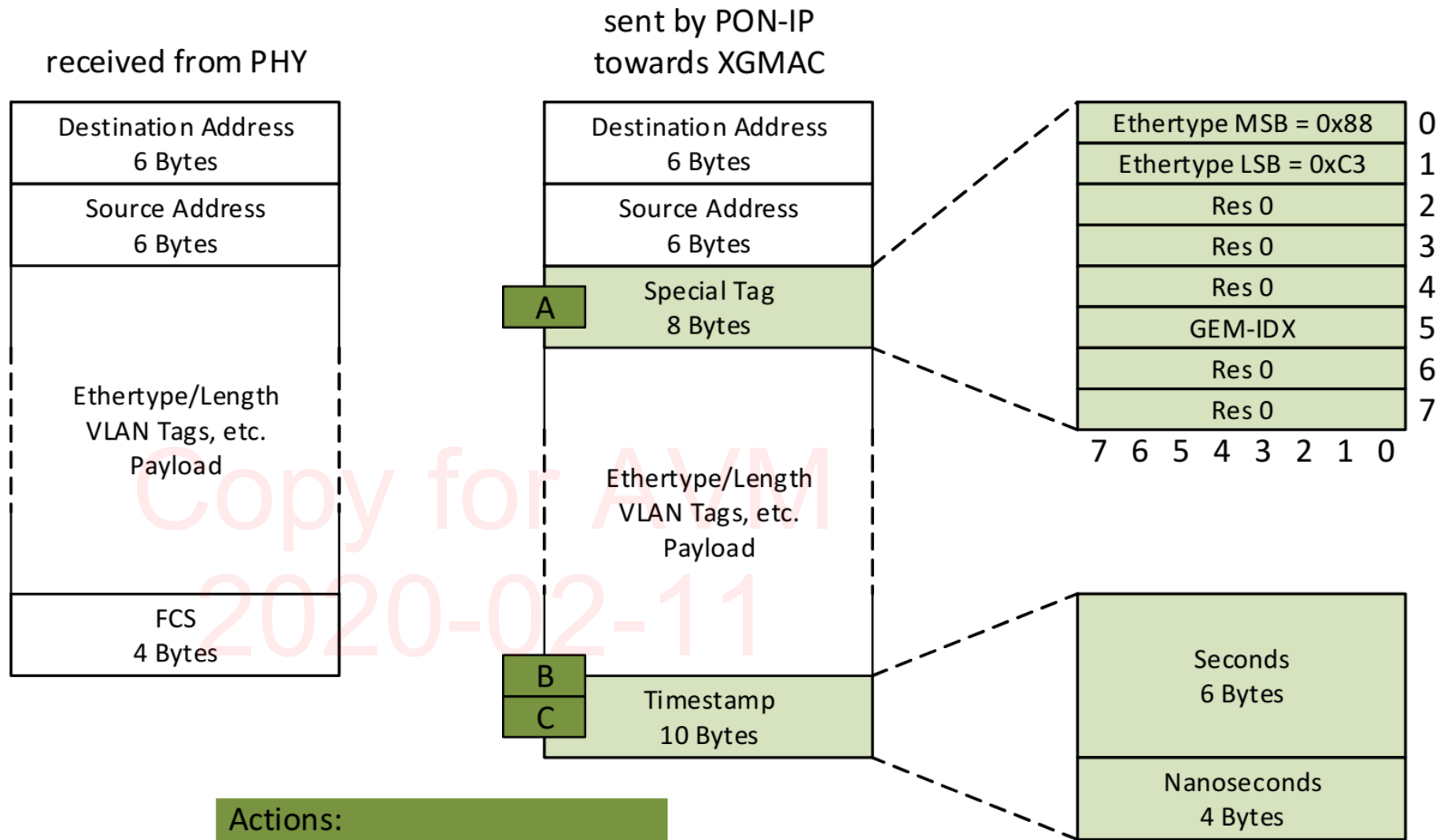
Timestamping information contained in TX special tag



PON_IP_XGMII_protocol.vsd, Page: TX timestamp, September 5, 2017

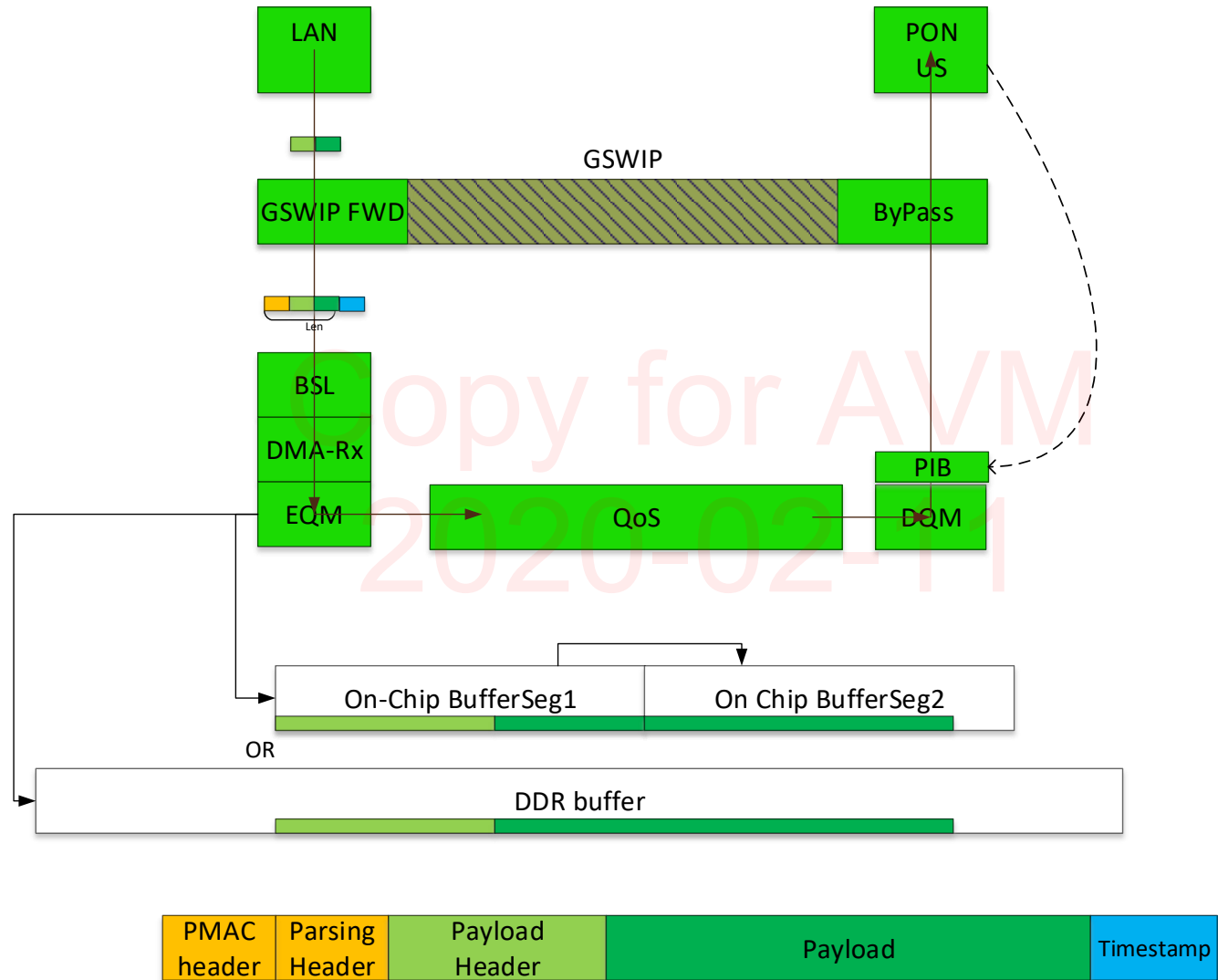
TX Time-stamping Information

Special Tag PON DS

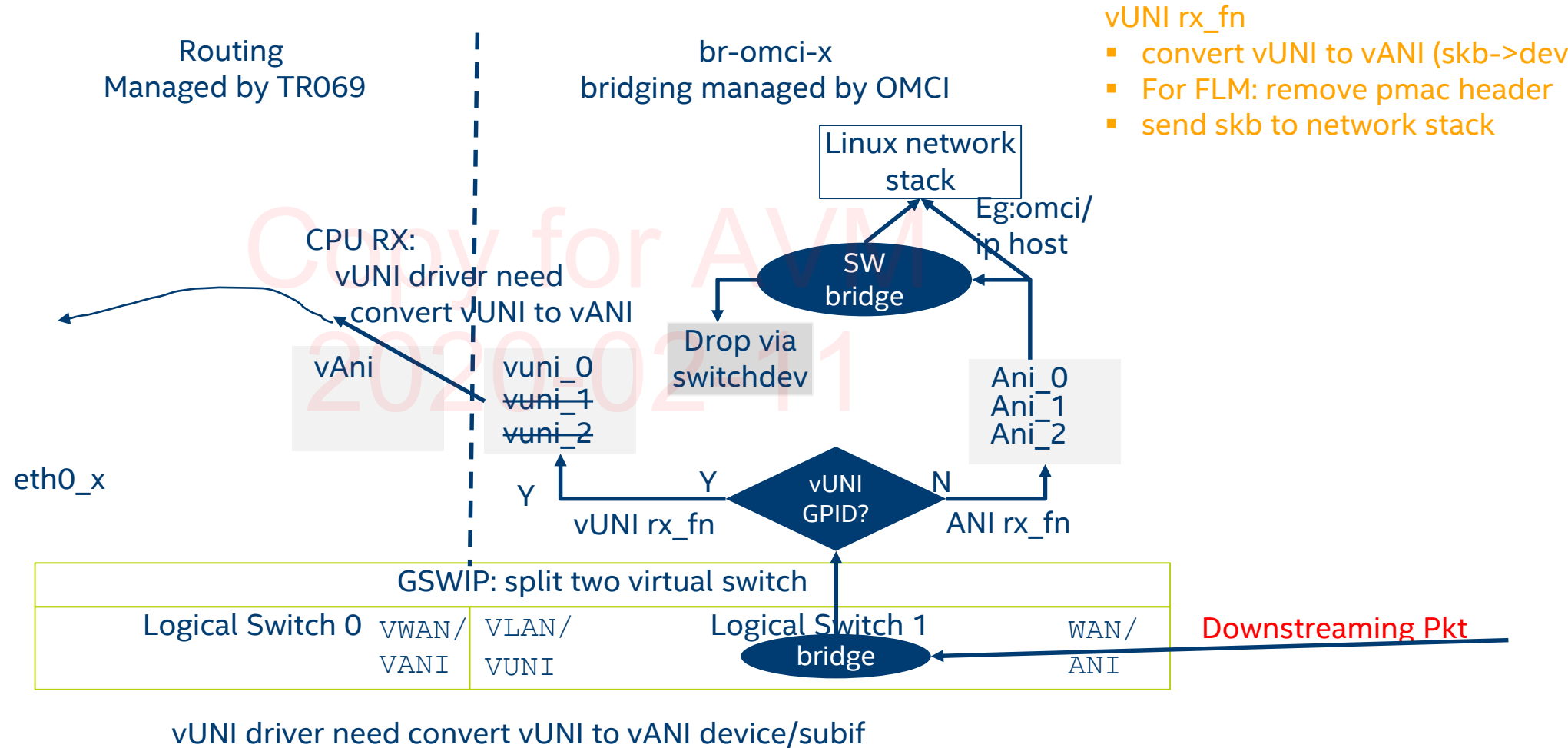


Actions:
 A: insert special tag
 B: check and remove FCS
 C: append timestamp

PON-US flow in 10G PON



PON HGU Datapath (Single Box)–vUNI RX/Downstream

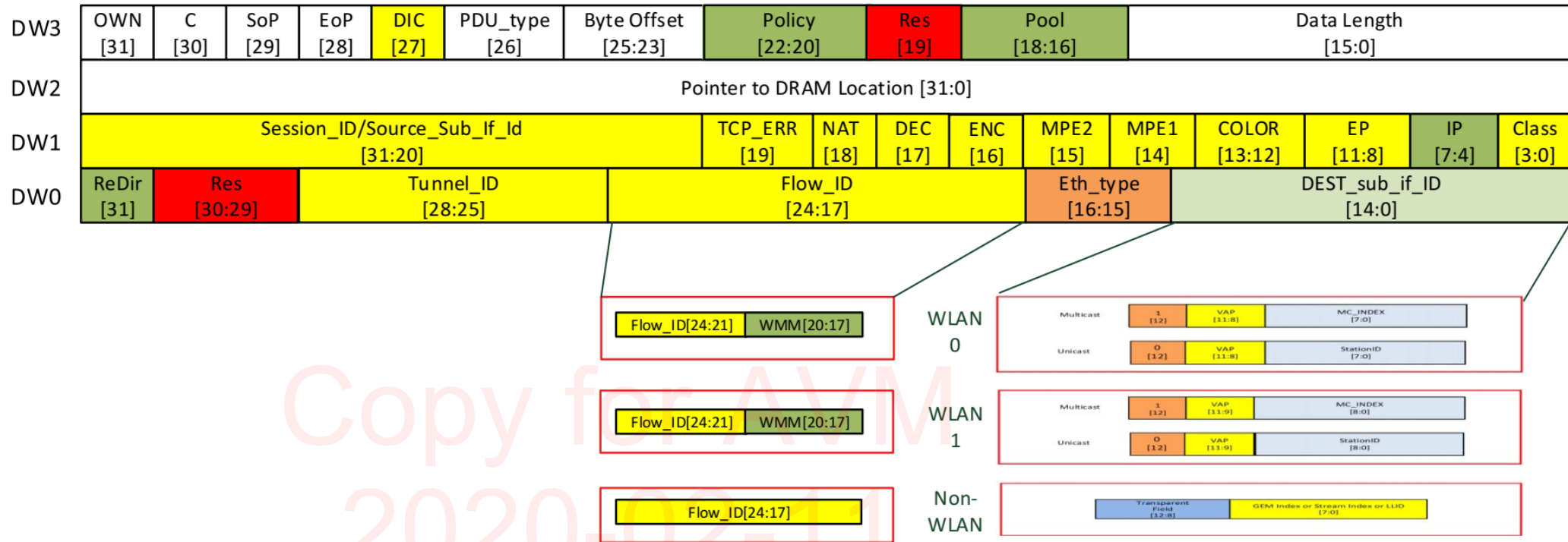


vUNI rx_fn

- convert vUNI to vANI (skb->dev)
- For FLM: remove pmac header
- send skb to network stack

Desc

DMA Descriptor Format



CPU/ACA Buffer Return Format

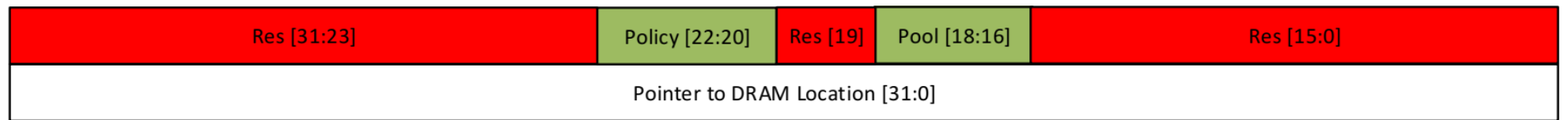


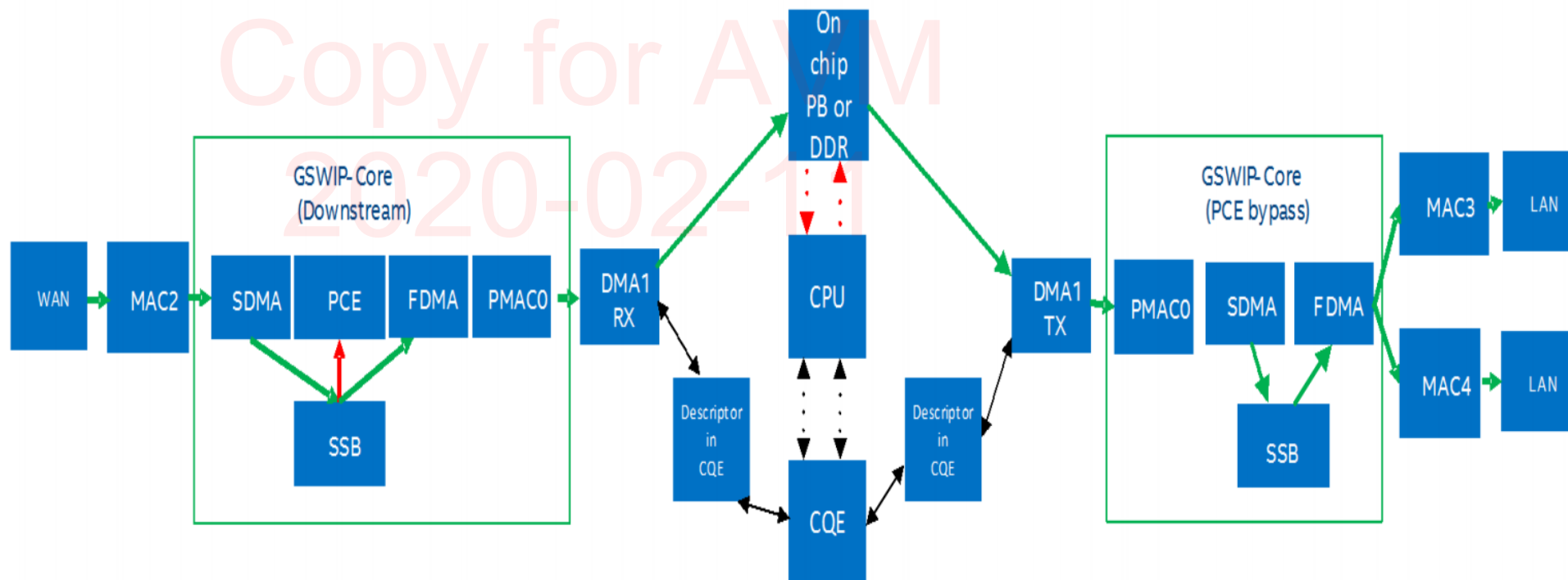
Figure 118 DMA Descriptor and Buffer Return Command

Data Flows: Downstream CQEM Mode

DMA/CQE determines to store packets either on chip PB or DDR based on traffic class and buffer usage

-  Descriptor
-  Whole Packet
-  Header Only

Enables queueing and QoS if LAN interface is slow or temporarily unavailable



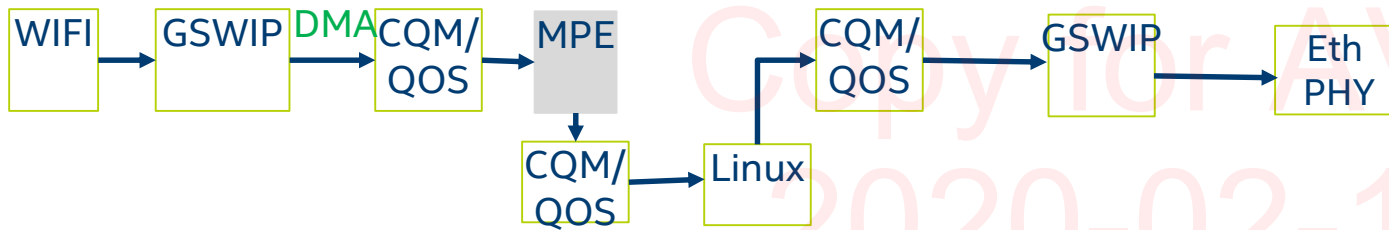
PON HGU Datapath (Single Box Routed) – WiFi <--> Eth WAN

Upstream

FLM WIFI->ANI Routing Data Flow with MPE Acceleration:



FLM WIFI->ANI Routing Data Flow with Linux Slow Path



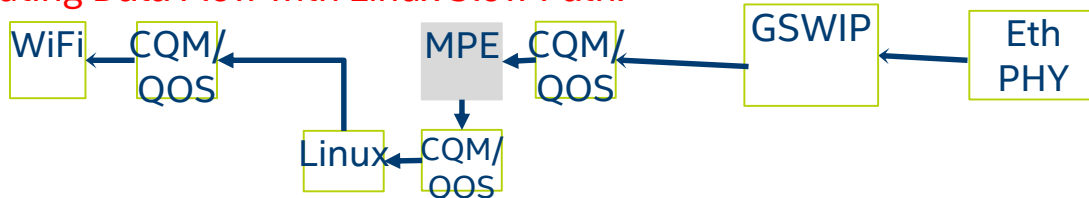
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Downstream

FLM ANI->UNI Routing Data Flow with MPE Acceleration:



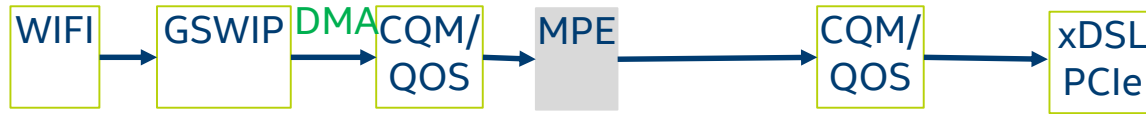
FLM ANI->UNI Routing Data Flow with Linux Slow Path:



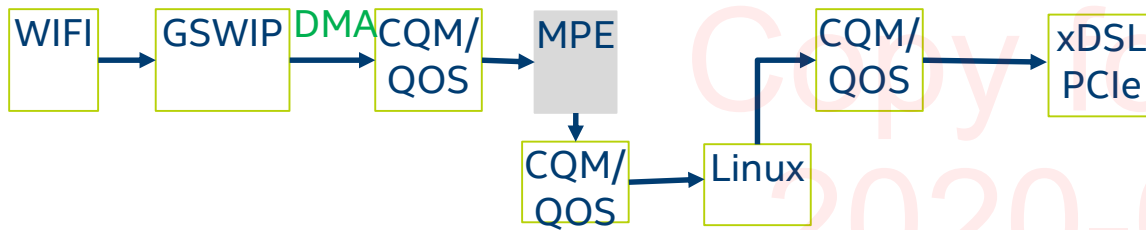
PON HGU Datapath (Single Box Routed) – WiFi <--> xDSL

Upstream

FLM WIFI->ANI Routing Data Flow with MPE Acceleration:



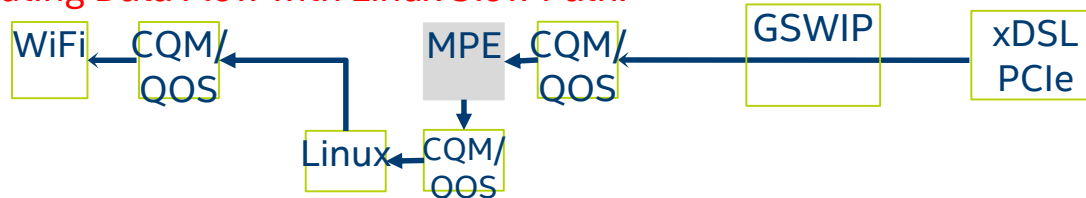
FLM WIFI->ANI Routing Data Flow with Linux Slow Path



FLM ANI->UNI Routing Data Flow with MPE Acceleration:



FLM ANI->UNI Routing Data Flow with Linux Slow Path:



Downstream

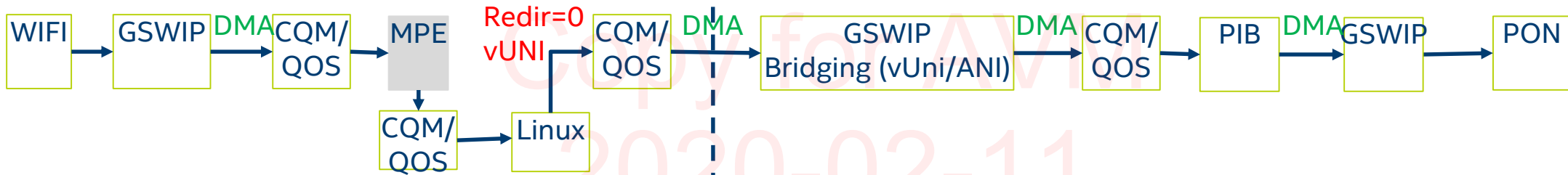
PON HGU Datapath (Single Box Routing) – WiFi <--> PON

Upstream

FLM WIFI->ANI Routing Data Flow with MPE Acceleration:



FLM WIFI->ANI Routing Data Flow with Linux Slow Path



FLM ANI->UNI Routing Data Flow with MPE Acceleration:



FLM ANI->UNI Routing Data Flow with Linux Slow Path:

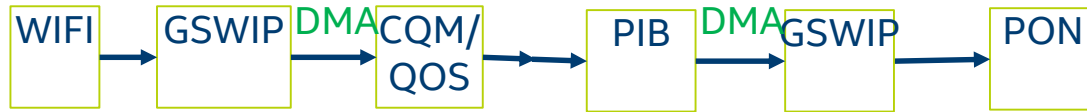


Downstream

PON HGU Datapath (Single Box Bridging) – WiFi <--> PON

Upstream

FLM WIFI->ANI Bridging



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Downstream

FLM ANI->UNI Bridging



PON HGU Datapath (Single Box Bridging) – WiFi <--> xDSL

Upstream

WiFi to DSL Bridging



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Downstream

DSL to WiFi Bridging



PON HGU Datapath (Single Box)-Bridging

Default LAN to LAN



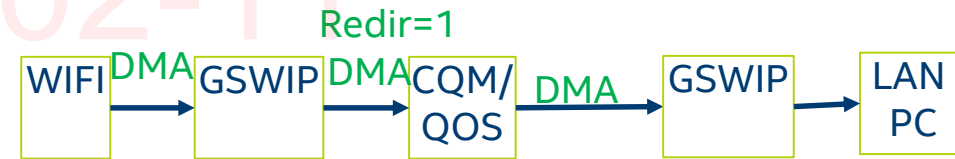
LAN to LAN using QoS (non-default)



Default Wifi to LAN



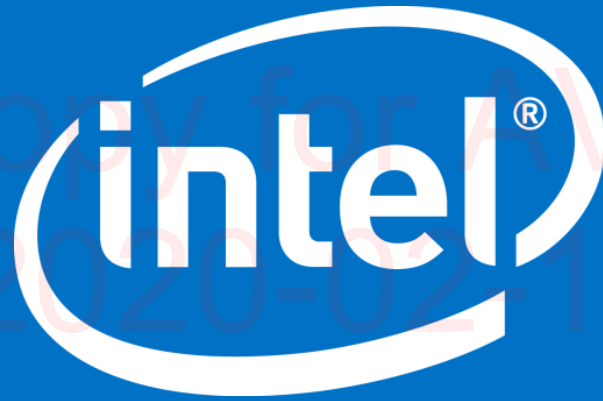
Wifi to LAN using QoS (Non-default)



LAN to Wifi using QoS (Non-default)



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Queue ID Computation

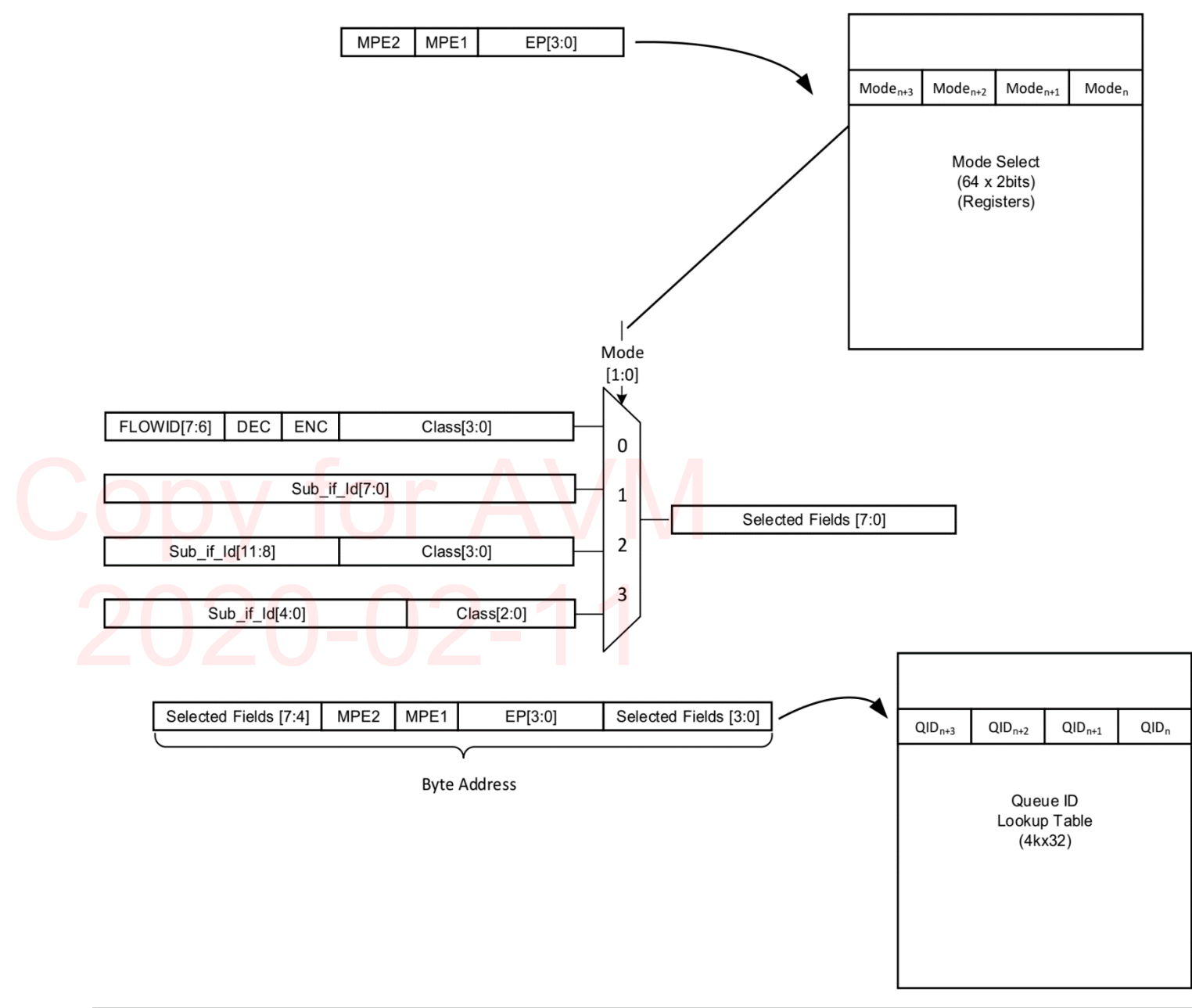


Figure 121 Queue ID Computation