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TECHNICAL REPORT

colour inside

Flexible printed circuit boards (FPCBs) – Method of compensation of impedance variations

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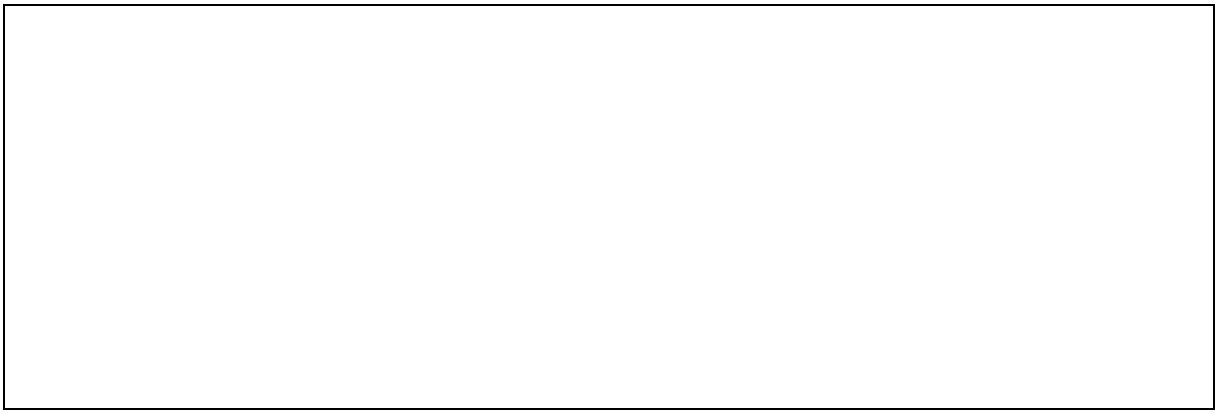
International Electrotechnical Commission



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Flexible printed circuit boards (FPCBs) – Method of compensation of impedance variations

INTERNATIONAL
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FLEXIBLE PRINTED CIRCUIT BOARDS (FPCBs) – METHOD OF COMPENSATION OF IMPEDANCE VARIATIONS

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IEC TR 63017, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
91/1283/DTR	91/1308/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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- withdrawn,
- replaced by a revised edition, or
- amended.

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FLEXIBLE PRINTED CIRCUIT BOARDS (FPCBs) – METHOD OF COMPENSATION OF IMPEDANCE VARIATIONS

1 Scope

This Technical Report specifies a compensation method of Cu linewidth according to impeadance reduction by using noise suppression materials (hereafter referred to as NSMs) for FPCBs.

This Technical Report presents an optimum result for maintaining a designated performance of FPCBs by using NSMs. It also indicates a measuring method for an impedance variation of FPCBs using NSMs with the prevailing TDR (time domain reflectometry) method. This method is resticted to measuring only the variation of an impedance value in accordance with the variation of the Cu linewidth by using NSMs for FPCBs. This report, however, neither determines nor indicates the structure or material of FPCBs.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IPC 2141A *Design Guide for High-Speed Controlled Impedance Circuits Boards*
http://www.ipc.org/

3 Apparatus

3.1 Time domain reflectometry

Time domain reflectometry (hereafter referred to as TDR) is utilized to identify the impedance data at the specific frequency range of FPCBs.

3.2 Block diagram for impedance measuring

Figure 1 gives one example of a TDR setup.

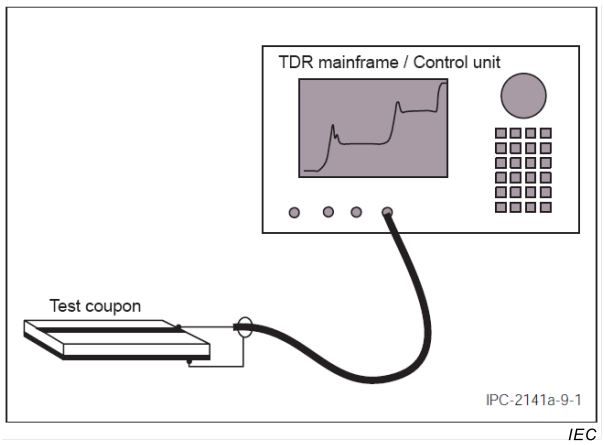

Figure 1 – TDR test system

NOTE A guideline for TDR is provided in Annex A.

4 Test specimen

4.1 General

FPCBs using NSMs should reduce the effect of electro-magnetic interference. However, without appropriate application of NSMs, it may cause poor signal quality on the FPCB due to the impedance variation of Cu circuit lines.

A major factor of impedance variation using NSMs is due to the structure variation of FPCBs, as shown in Figure 2.

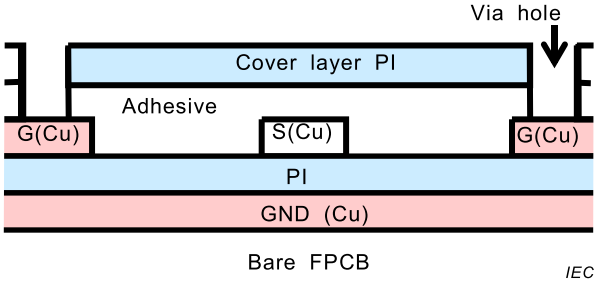

Figure 2a – <Micro strip line structure without NSMs>

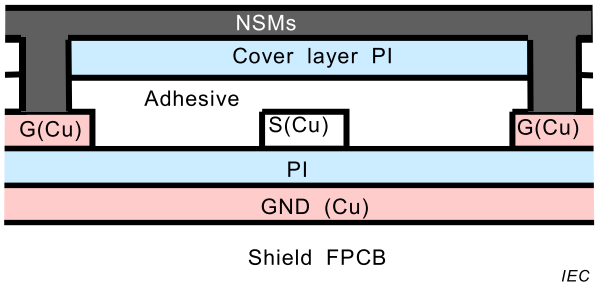

Figure 2b – <Strip line structure with NSMs>

NOTE A guideline for the theoretical background of impedance variation is provided in Annex B.

Figure 2 – Two types of impedance structure of FPCB

4.2 Structure

Test specimens shall be designed by two structures, i.e. with and without using NSMs in one FPCB board. Test specimens shall be divided into two halves with one board (consisting of the two parts of one bare FPCB and one shield FPCB) for equitable estimation. This structure has the merit of uniformly measuring at once a bare and a shield FPCB under the same condition. One FPCB without using NSMs has a structure of a micro-strip line. This type is called bare FPCB. Another FPCB using NSMs has a structure of a strip line. This type is called shield FPCB (see Figure 3).

A Cu line is formed with a linear distance direction, because the variation of the shield effect is very weak for a curved line.

Generally, the number of Cu patterns of the test specimen can be over the 5 (for example LW1 ~ LW5) for verification of the characteristic impedance (Z_0). But the number and width of the Cu line shall vary in accordance with the supplier's activity.

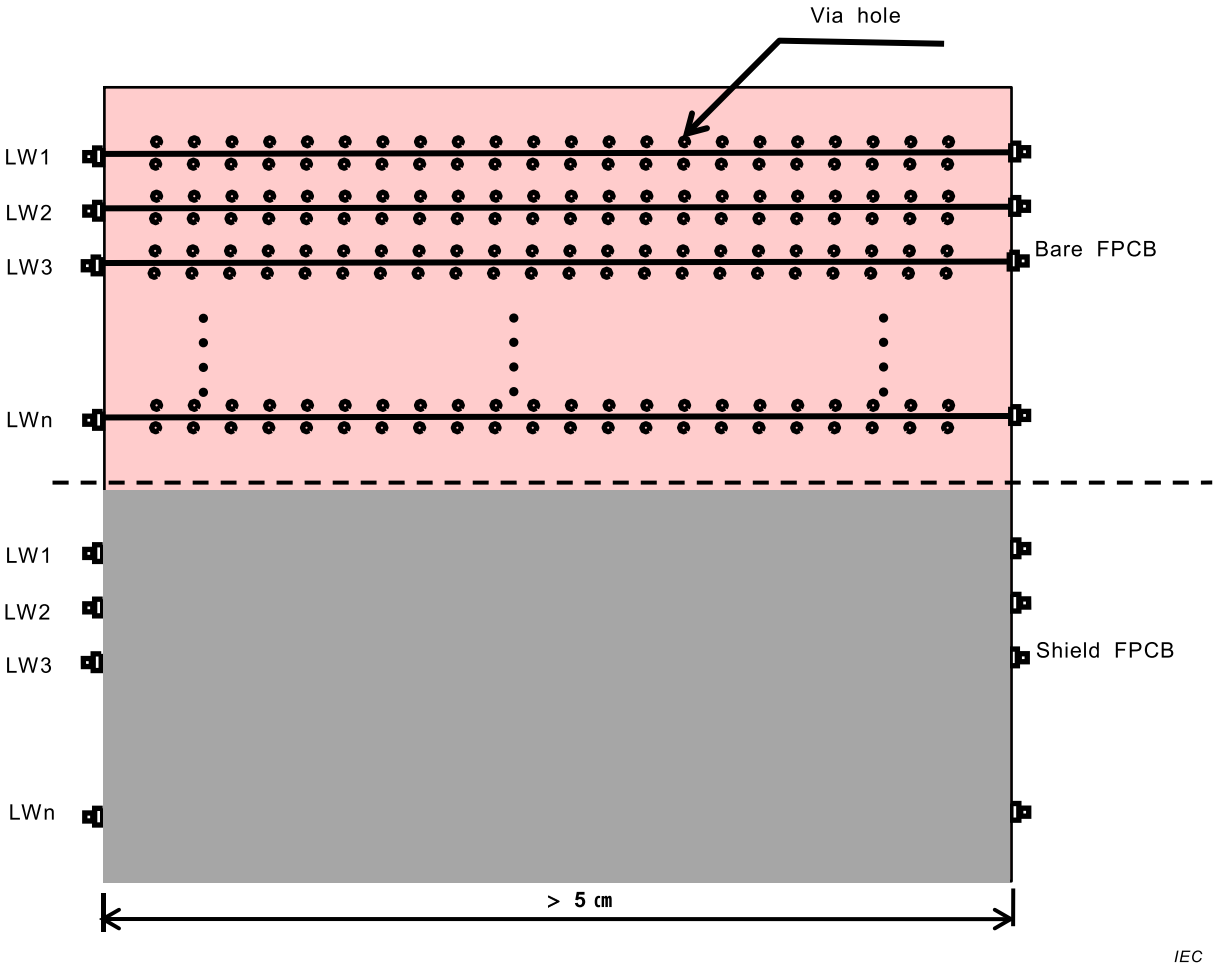

Figure 3 – Schematic diagram of a test specimen

Size, spacing and number of via holes for test specimens shall not be limited, but sufficiently represented. Especially, via holes offer an important role to contact the NSMs with the ground plan of shield FPCB. The number of via holes shall be as agreed between user and supplier (hereafter referred to as AABUS).

The length of the test specimen shall be over 5 cm in order to obtain stable values from the measuring equipment. Each end of the test specimen should consist of SMA (subminiature A) connectors. For discernment of a Cu line-width, write each – number to the bare – end of the test specimen near the SMA connector.

The decision of width and thickness of a test specimen shall depend on to the pitch or the number of the Cu line or according to the requirements of the user. However, generally the structure of the test coupon shall be AABUS.

An impedance value for FPCBs shall be changed with respect to the Cu pattern width, layer structure, thickness and materials. The structure and materials of the test specimens is required depending on the user's sample specifications. But the variation of these test specimens is not important, because the user of FPCBs shall check only the impedance variation effect by using NSMs for the user's sample specification.

4.3 Test method

In order to measure the proper impedance value for the test specimen, the following procedures shall be empoyed.

a) Impedance values of the test specimen shall be measured by employing TDR, test specimen and coaxial cable according to IPC 2141A.

b) Measurement conditions shall be set by means of the TDR, such as dielectric constant, measurement point, rising time, pulse width, etc.

c) The impedance value of the test specimen shall be measured according to the Cu line width for bare FPCB.

d) The measurement of the above process according to Cu line width shall be repeated for the shield FPCB (see Figure 4).

NOTE The guideline of the test method is provided in Annex C.

e) The measuring value of the two types FPCBs (bare and shield) shall be presented in form of a diagram (line chart using excel).

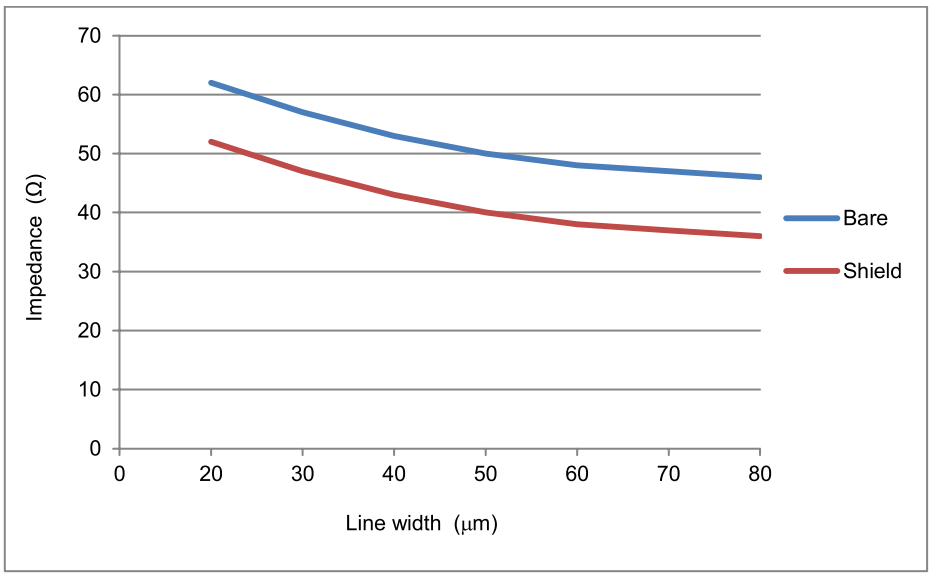

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Figure 4 – Impedance value of two type FPCB (bare and shield)

f) In order to obtain the correct data, a direct hand contact to the specimen should be avoided as the electrostatic capacity varies.

NOTE The effect of hand contact with the test specimen is provided in Annex D.

4.4 Calculation

The following applies to the calculation of the compensation values.

a) Generally, a demand of the characteristic impedance value (Z_0) is 50 Ω for a single Cu line, 100 Ω for a differential Cu line.

b) In the case of a single Cu line, draw a straight base line corresponding to a characteristic impedance value (50 Ω) on a excel chart (see Figure 5).

c) Find a cross point of the Cu line width for a characteristic impedance value (50 Ω) with each curve of bare and shield FPCB.

d) Especially, check the Cu line width in the point to meet the 50 Ω impedance value from the shield FPCB curve.

e) Calculate a difference (ΔL) of the Cu line width between two points.

f) Reduce ΔL by degrees to the Cu line width of the bare FPCB.

g) Show this value in a new design of a Cu line width for the bare FPCB.

NOTE A detailed test result is provided in Annex E.

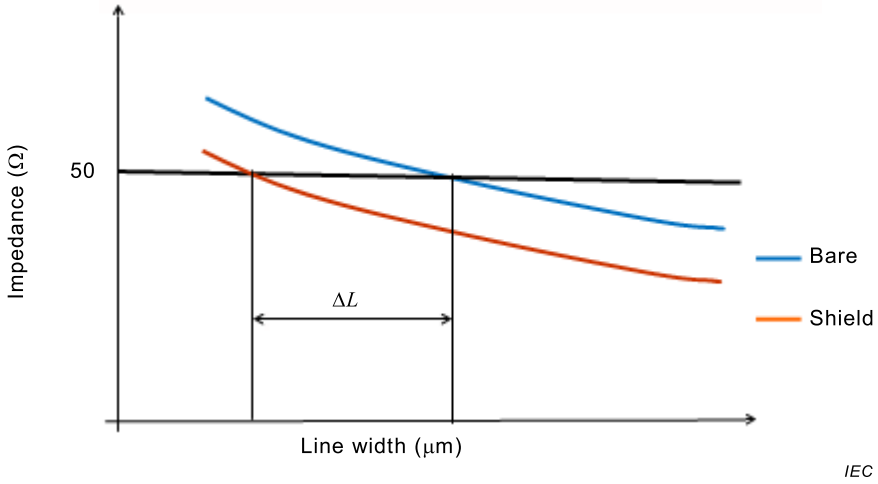

Figure 5 – Compensation value (ΔL) of the Cu line width for the shield FPCB

5 Report

In case that the specification of the measurement is contained in the report, it shall be provided with the details as specified below.

a) Type of TDR equipment.
b) Type of shied materials (structure, thickness, maker).
c) Type of base materials (structure, maker).
d) The range of Cu line width.
e) The range of impedance (Z) variation according to the Cu line width of the test specimen.
f) Impedance value data according to the Cu line width.

Annex A
(normative)

Block diagram for impedance measuring with TDR

Time Domain Reflectometry (TDR) shall be used for impedance measurements according to IPC 2141A.

The TDR setup (IPC 2141A) is presented in Figure A.1.

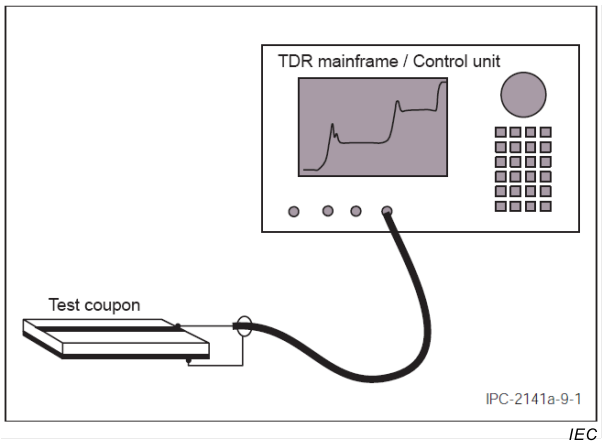

Figure A.1 – TDR test system according to IPC 2141a-9-1

Test setup by Agilent TDR 54754A[1] is presented in Figure A.2.

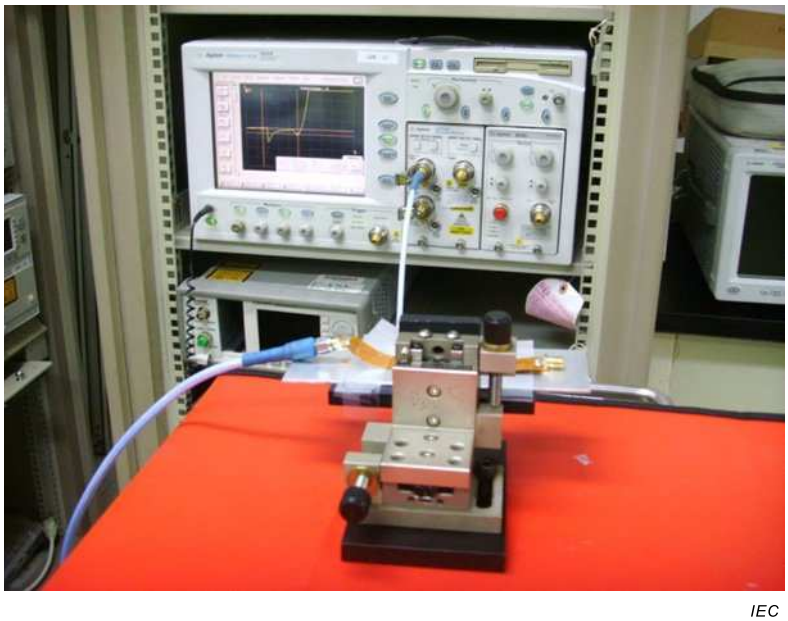

Figure A.2 – TDR test system according to Agilent TDR 54754A

1 Agilent TDR 54754A is the trade name of a product supplied by Agilent Technologies.

This information is given for the convenience of users of this document and does not constitute an endorsement by IEC of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Annex B
(informative)

Theoretical background

The application of shield FPCB (with using NSMs) in electronic devices (or equipment) shall be able to reduce the effect of electro-magnetic interference, but it will eventually result in bad signal quality of FPCBs, because of the impedance variation of Cu circuit lines.

The purpose of this Technical Report is to settle the problem that FPCBs using NSMs suffer from, i.e. to eliminate an impedance mismatch by means of impedance compensation.

A major factor causing the impedance variation by using NSMs is due to the structure variation of FPCBs as shown in Figure B.1.

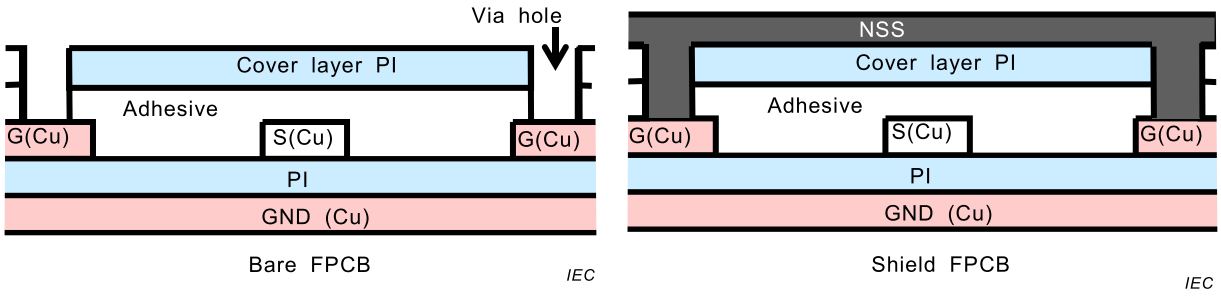

Figure B.1 a – <Micro strip line structure> **Figure B.1 b – <Strip line structure>**

Figure B.1 – Two types of impedance structure of FPCBs

The impedance value of the strip line structure for FPCBs is lower than that of the micro-strip line structure, as shown in Figure B.2. NSMs shall play a role with respect of the metal layer, because they are composed of a metal component. Accordingly, the micro-strip line structure for bare FPCBs shall be changed to the strip line structure after application of NSMs for bare FPCB.

The impedance value decreases, as the Cu line width increases.

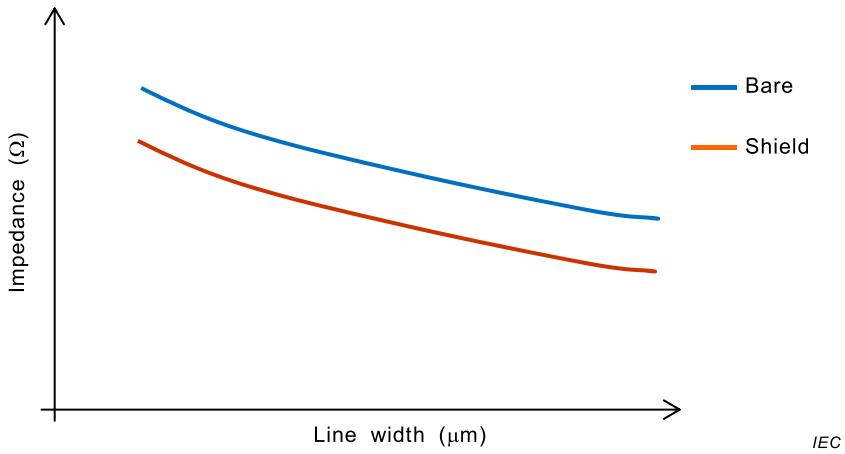

Figure B.2 – Comparison of the impedance value of a bare FPCB versus a shield FPCB

FPCB suppliers have to produce a new reduction design of Cu line width for new impedance matching (Z_0, 50 Ω).

Annex C
(informative)

Example of an impedance measurement with TDR

The test specimen shows two different impedance values according to the structure variation between a bare FPCB and a shield FPCB, as depicted in Figure C.1.

Example: test specimen: 8 cm (bare) +8 cm (shield), 100 μm Cu line width, with the following values:

- impedance value with bare FPCB: 50,9 Ω;
- impedance value with shield FPCB: 31,3 Ω;
- the impedance difference between two types: ΔZ (19,6 Ω).

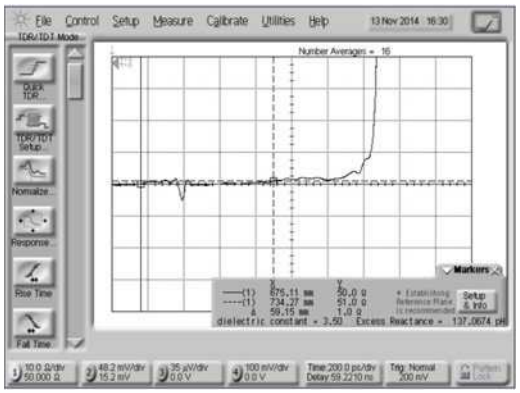

Figure C.1 a – <Bare FPCB>

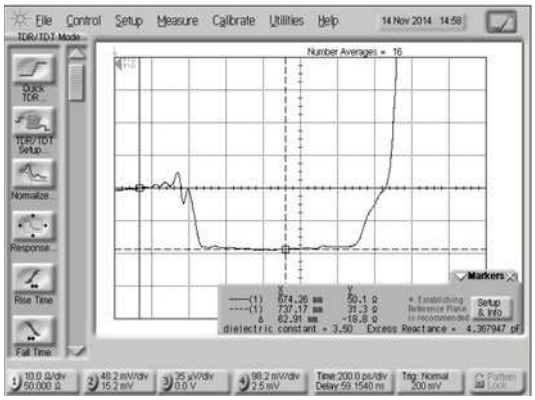

Figure C.1 b – <Shield FPCB>

Figure C.1 – Photographic view of the impedance measurement with TDR

Annex D
(informative)

Hand contact effect

The impedance value for a shield FPCB is not influenced by hand contact. But the impedance value for a bare FPCB is able to vary due to hand contact, as shown in Figure D.1. Especially, the effect of hand contact is more increased by a small line width.

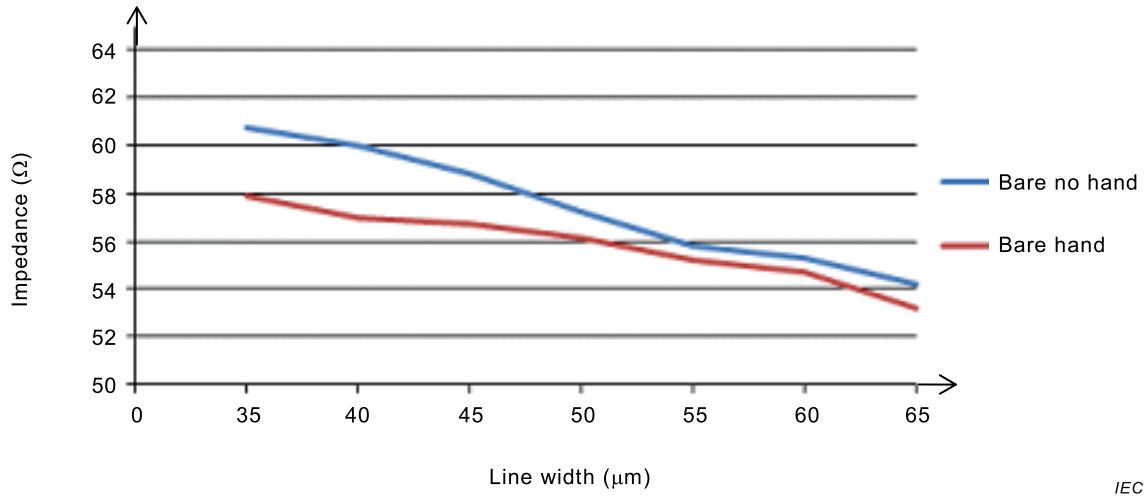

Figure D.1 – Effect of impedance variation by hand contact for bare FPCB

Annex E
(informative)

Test result

E.1 Shield 1 FPCB

Figure E.1 shows the result of a test specimen that uses an 8 cm length shield (8 cm (bare) +8 cm (shield 1)).

To satisfy the 50 Ω condition for shield 1 FPCB, the Cu line width shall be near 40 μm.

The range of impedance (Z) reduction with NSMs: 16 Ω ~ 30 Ω (within the range of 30 μm ~ 150 μm Cu line width).

- Need of a reduction of the line width for new impedance matching (Z_0, 50 Ω).
- (example) Bare FPCB (100 μm) ⇒ Shield 1 FPCB (40 μm): 60 μm wide difference (ΔL).

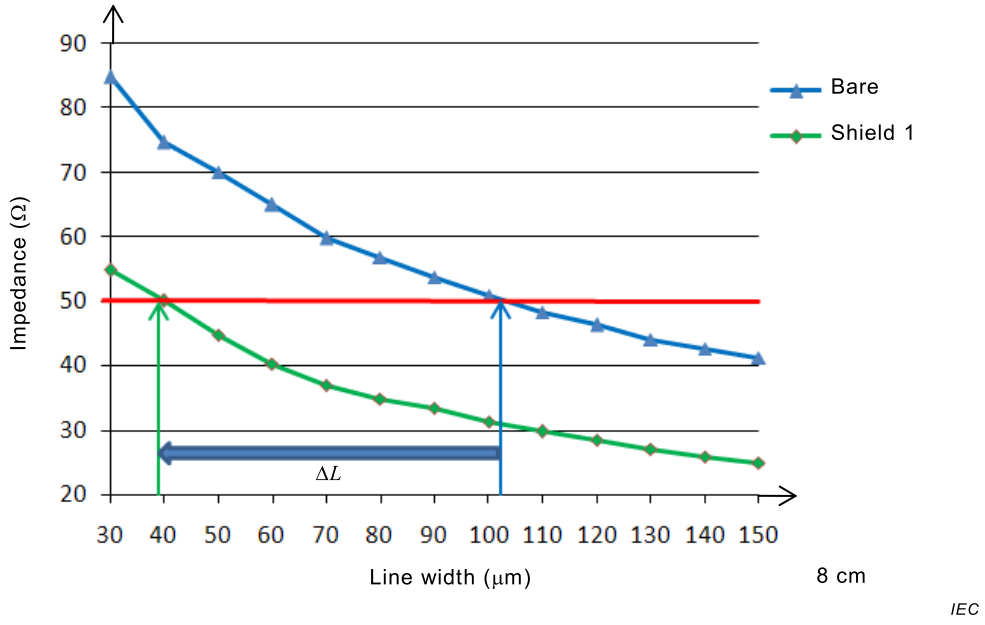

Figure E.1 – Measurement result of the test specimen for shield 1 FPCB

A cross-section of a test specimen using shield 1 FPCB is as shown in Table E.1. Where, a Cu thickness of NSMs for shield 1 FPCB is 2 μm.

Table E.1 – Cross-section of test specimen with using shield 1 FPCB

FPCB	**FCCL** (Flexible Copper Clad Laminate)	PI 50 μm, Cu 12 μm
	Cu thickness	24 μm (Cu plating 12 μm)
	C/L	PI 12 μm, Adhesive 25 μm
	Pattern space	200 μm
NSMs	**Material**	Cu
	Thickness	2 μm

E.2 Shield 2 FPCB

Figure E.2 shows the result of test specimen with using 8 cm length (8 cm (bare) +8 cm (shield 2)).

To satisfy the 50 Ω condition for shield 2 FPCB, Cu line width shall be nearby 50 μm.

The range of impedance (Z) reduction with NSMs: 13 Ω ~ 24 Ω (within the range of 30 μm ~ 150 μm Cu line width).

- Need of a reduction of the line width for new impedance matching (Z_0, 50 Ω).
- (example) Bare FPCB (100 μm) ⇒ Shield 2 FPCB (50 μm): 50 μm wide difference (ΔL).

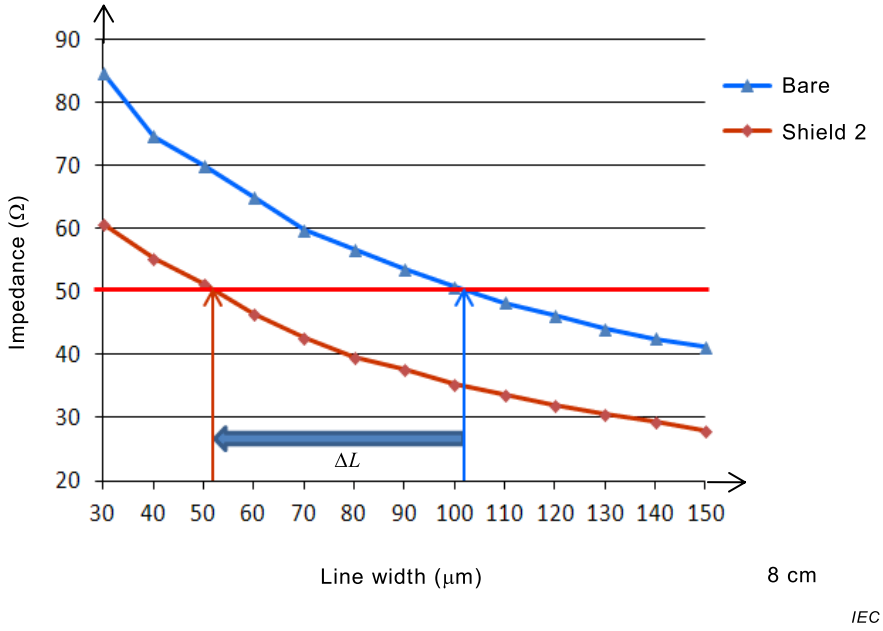

Figure E.2 – Measurement result of the test specimen for shield 2 FPCB

A cross-section of a test specimen with using shield 2 FPCB is as indicated in Table E.2. Where, a Cu (or Ag) thickness of NSMs for shield 2 FPCB is 0,1 μm.

Table E.2 – Cross-section of test specimen with using shield 2 FPCB

FPCB	**FCCL**	PI 50 μm, Cu 12 μm
	Cu thickness	24 μm (Cu plating 12 μm)
	C/L	PI 12 μm, adhesive 25 μm
	Pattern space	200 μm
NSMs	**material**	Cu (or Ag)
	thickness	0,1 μm

Bibliography

IEC 62333-1:2006, *Noise suppression sheet for digital devices and equipment – Part 1: Definitions and general properties*

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