IEC PAS 62878-2-5

Edition 1.0 2015-08

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD

colour inside

Device embedded substrate – Guidelines – Data format

IEC PAS 62878-2-5:2015-08(en)

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

IEC Catalogue - webstore.iec.ch/catalogue

The stand-alone application for consulting the entire bibliographical information on IEC International Standards, Technical Specifications, Technical Reports and other documents. Available for PC, Mac OS, Android Tablets and iPad.

IEC publications search - www.iec.ch/searchpub

The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,…). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished

Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and also once a month by email.

Electropedia - www.electropedia.org

The world's leading online dictionary of electronic and electrical terms containing more than 30 000 terms and definitions in English and French, with equivalent terms in 15 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

IEC Glossary - std.iec.ch/glossary

More than 60 000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.

IEC Customer Service Centre - webstore.iec.ch/csc

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: csc@iec.ch.

IEC PAS 62878-2-5

Edition 1.0 2015-08

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD

colour inside

Device embedded substrate – Guidelines – Data format

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.180; 31.190

ISBN 978-2-8322-2808-1

Warning! Make sure that you obtained this publication from an authorized distributor.

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

DEVICE EMBEDDED SUBSTRATE – GUIDELINES – DATA FORMAT

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as “IEC Publication(s)”). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public.

IEC PAS 62878-2-5 was submitted by the JPCA (Japan Electronics Packaging and Circuits Association) and has been processed by IEC technical committee 91: Electronics assembly technology.

It is based on JPCA-EB02 (2011). It is published as a double-logo IEC / JPCA PAS.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document

Draft PAS	Report on voting
91/1257/PAS	91/1264/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single period up to a maximum of 3 years, at the end of which it shall be published as another type of normative document, or shall be withdrawn.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

DEVICE EMBEDDED SUBSTRATE – GUIDELINES – DATA FORMAT

1 Scope

This part of IEC 62878 defines the data format for active and passive devices embedded inside an organic board whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material. The basic structures, the terminology, reliability tests and a design guide are described in the “Standard of device embedded substrate", JPCA EB01, fourth edition.

A device embedded substrate contains device(s) in the board and is connected in a 3D way. Conventional 2D design technology using GERBER format cannot describe all the connection information in a device embedded substrate. We have several proposals to express 3D data formats but they cannot describe the structures given in EB01. The JPCA Committee for standardization of device embedded substrates has studied various formats and developed a format, FUJIKO V-1.0, which can express substrate design data in CAM data used in actual production. This Publicly Available Specification (PAS) described the FUJIKO data format.

Figure 1.1 shows the design flow of a device embedded substrate. The design data can be directly sent to a board manufacturing system using the FUJIKO format, or can be converted to CAM data and then be used in production. The data contain 3D information of coordinates and shapes of devices used. It is possible to check the status of device embedding in a board, and also make it a common knowledge in production know-how of a production line.

This PAS describes the expression of 3D data information, the concept of layers, the structure of board data, and definitions of information repeatedly used in design.

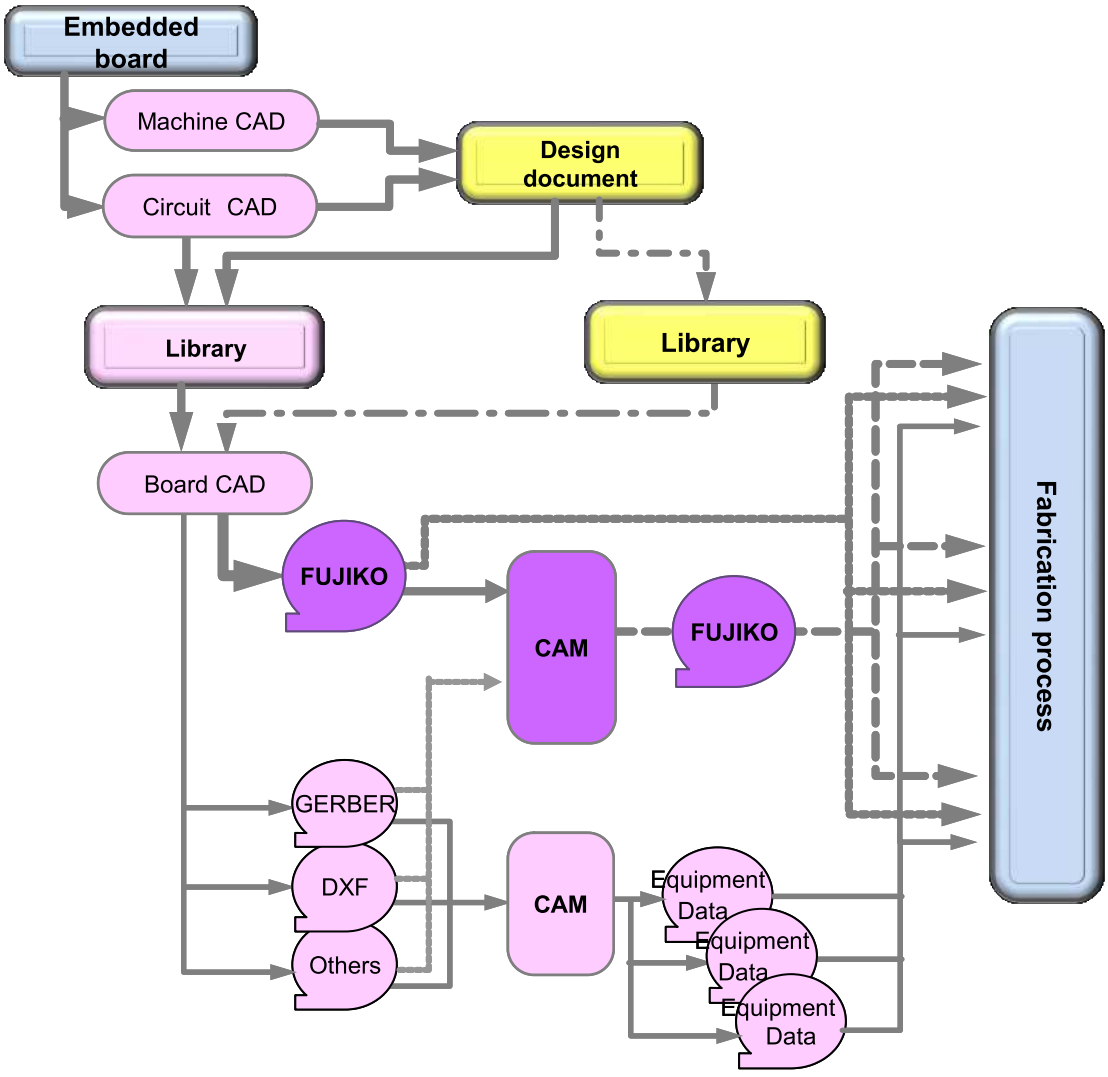


Figure 1.1 – Flow chart of design of device embedded substrate

1.1 Purpose

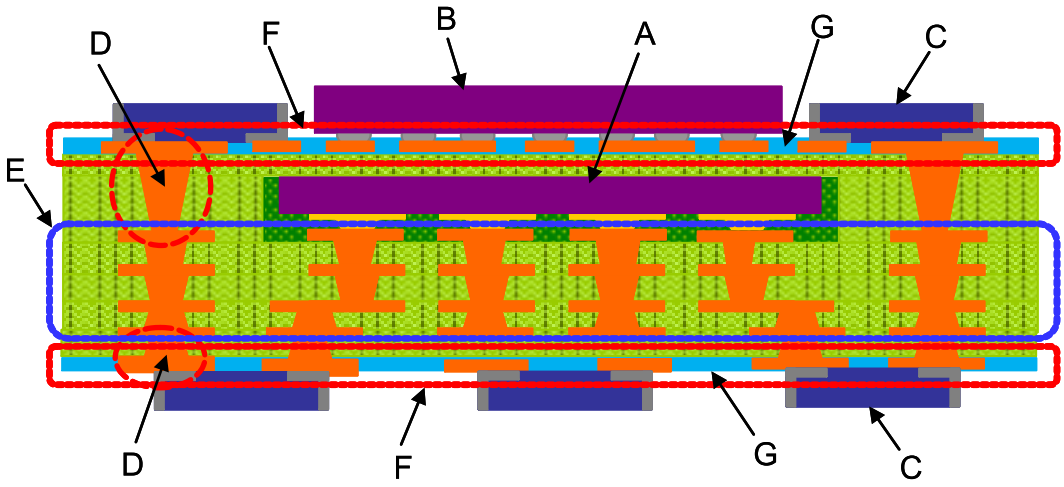
This file format describes the detailed 3D information of the following electronic circuit boards including device embedded substrate and SiP (system in package), and makes it possible to use necessary information from the stage of design to fabrication of products.

1.2 Applicable range

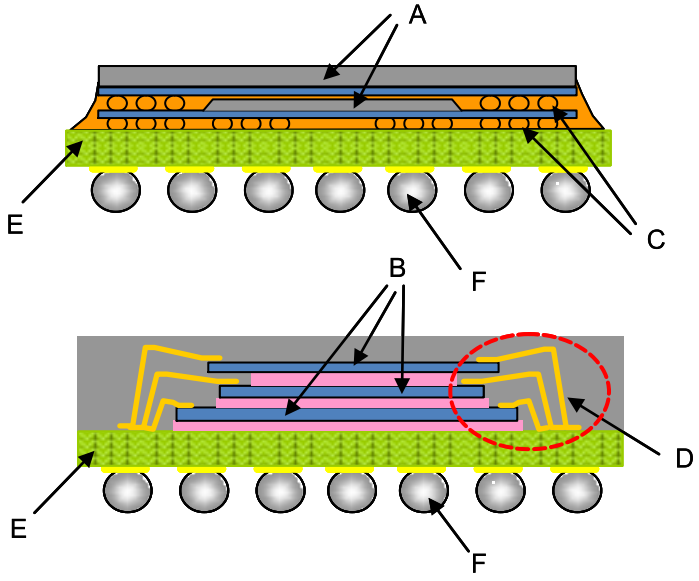
1.2.1 Product

It is possible to maintain the following design information of device embedded substrate as shown in Figure 1.2.

1) Information of inside device embedded substrate and surface mounting.
2) Assembly information of SiP (System in Package).



A	Embedded active device	E	Inner pattern
B	Surface mounted active device	F	Surface pattern
C	Surface mounted passive device	G	Solder resist
D	Layer connecting via		



A	CSP	D	Wire bonding
B	Bare die semiconductor device	E	Interposer
C	Solder ball	F	Solder ball

Figure 1.2 – General concept of product

1.2.2 Process

The format describes maintained and available information of each stage in production as described in Figure 1.1

1) Design
2) Simulation
3) Substrate fabrication
4) Device embedding
5) Test.

Table 1.1 – Information required in production

Process	Holding data of	Data available for
Design	Circuit Components Shape of the board Board structure Design/Production rule (for check)	Limited condition Net list
Simulation	Circuit Characteristics of components Board properties (materials) Board structure Art work	Electrical properties Thermal properties Mechanical properties Electronic properties Additional information in production
Substrate fabrication	Art work Drilling Symbol marks Panel format	Equipment Additional information in production
Device embedding	Component shape Embedding position Interconnection terminals Symbol marks	Equipment Relative positions of component Component list
Test	Art work Component shape Component position Terminal information Marks	Electrical test equipment Video image inspection

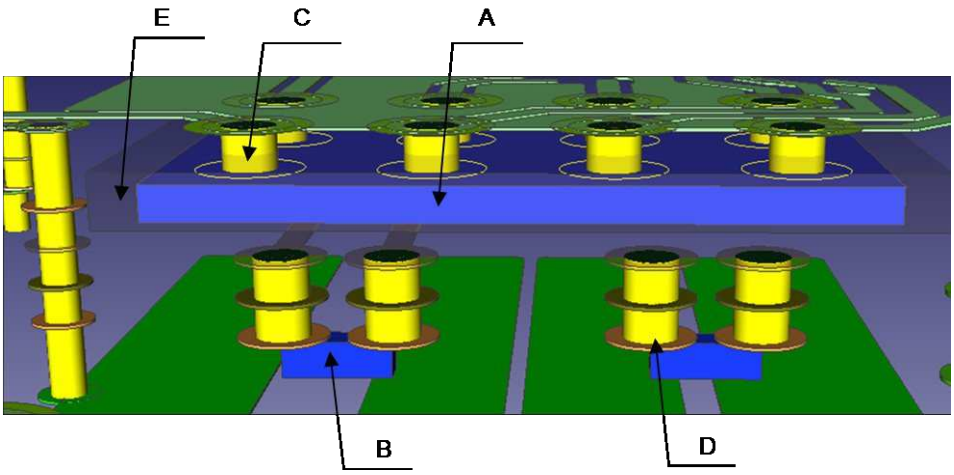
1.3 Features

Data format has the following characteristics:

1) can contain the structure of the device embedding substrate specified inEB01;
2) can contain information of SiP in general (chip stack, PoP TSV, wire bonding, flip-chip, interposer, etc.);
3) design data of terminal positions of embedding device in a virtual layer specified in EB01;
4) information of internal structure of devices such as SiP which cannot be described as a structure of a device embedded substrate and of a terminal structure as 3D design data;
5) seamless keeping of design data of devices having different level such as SiP and of embedding substrate.

1.3.1 Maintenance of the device embedded substrate structure

It is possible to keep and illustrate the 3D structure of device embedded substrate as shown in Figure 1.3. It is also possible to check its 3D structure.

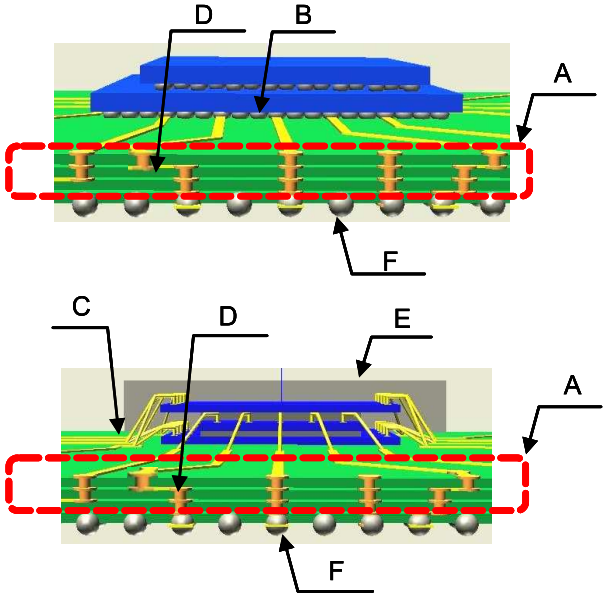


A	Embedded active device	D	Pad connection
B	Embedded passive device	E	Space without board material
C	Via connection		

Figure 1.3 – Example of a structure of a device embedded substrate

1.3.2 Maintenance of SiP interposer structure

It is possible to keep and illustrate the 3D structure of SiP substrate as shown in Figure 1.4. It is also possible to check structures of flip-chip and wire bonding mounting.

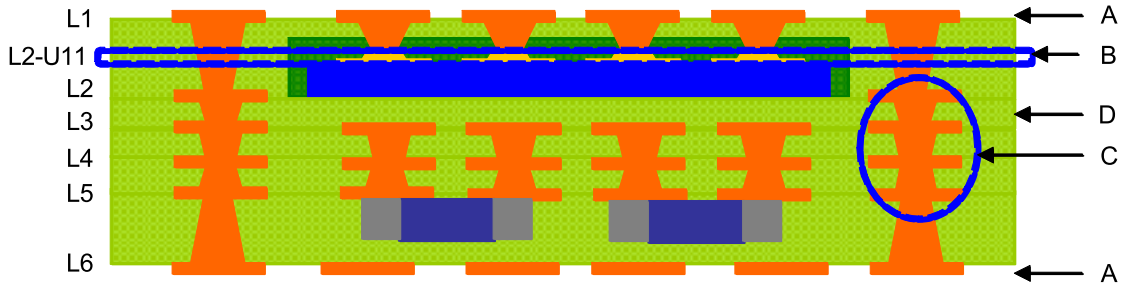


A	Interposer	D	Interposer
B	Flip-chip connection	E	Package
C	Wire bonding connection	F	Solder ball

Figure 1.4 – Examples of a structure of a SiP interposer

1.3.3 Maintenance of design data with a virtual layer of terminal positions of embedded device(s)

It is possible to keep the design data defined in EB01 of the terminal position of a via connection not on a conductor layer, but as in a virtual layer. It can be maintained in the structure shown in Figure 1.5.

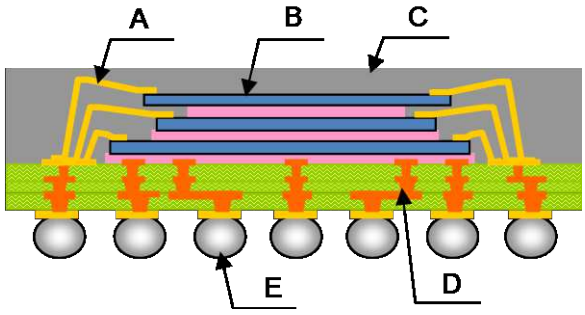


A	Surface conductor layer	C	Inner conductor
B	Virtual layer (connection position)	D	Insulation layer

Figure 1.5 – Example of a laying terminal position of an embedded device in a virtual layer

1.3.4 Maintenance of terminal structure and embedded device structure including SiP

It is possible to keep the design data of the terminal position of such as SiP as shown in Figure 1.6.

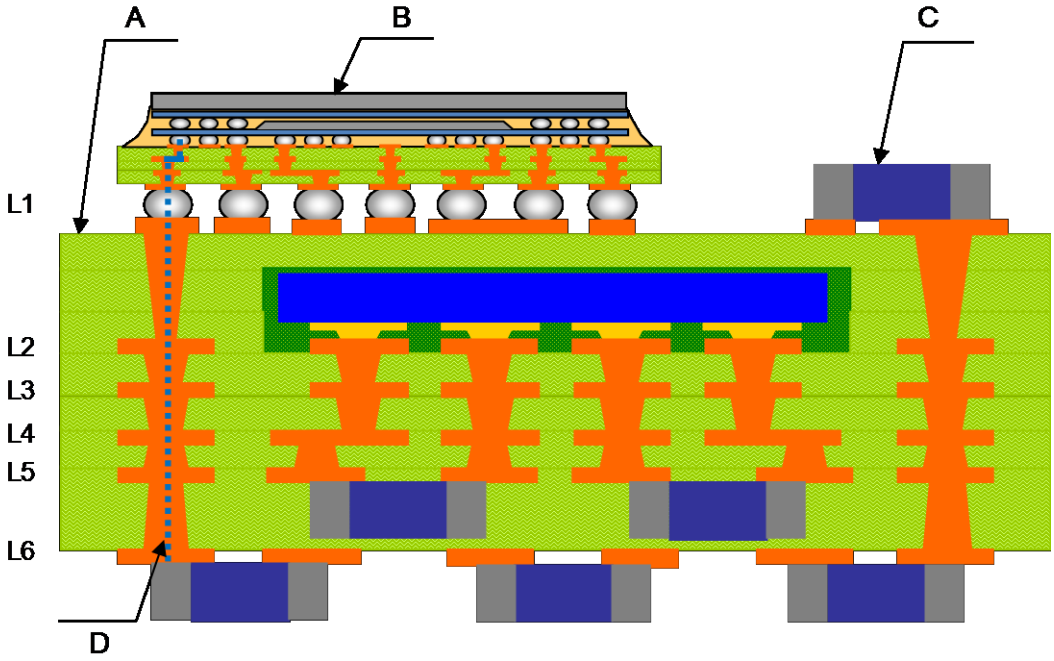


A	Bonding wire	D	Interposer
B	Chip stack	E	Solder ball
C	Package shape		

Figure 1.6 – Example of showing structures of device embedding and terminals

1.3.5 Seamless ownership of design data

It is possible to keep the design data of SiP and the device embedding substrate being made on different layers as shown in Figure 1.7.



A	Substrate (Printed wiring board)	C	Surface mounted passive device
B	SiP	D	The same net

Figure 1.7 – Example of showing structures of SiP and of a device embedding substrate

2 File description

2.1 File description summary

2.1.1 Types of data and their structure

1) Types of data

There are three types of data of substrate, definition and user defined data. Details of these data are shown in Table 2.1.

Table 2.1 – List of data

Type		Details	
Type name	**Content**	**Name**	**Content**
Board data	Basic structure elements of board data	Board information	Total data of board including embedding devices
		Layer map information	Layer combination information ofembedding devices and layers
		Device arrangement information	Position of devices and embedding layers
		Basic figure information	Available figure elements in board data There are ten (10) types of figures 1 Point 2 Area 3 Line 4 Text 5 Bonding wire 6 Semi-sphere 7 Rectangular prismoid 8 Via 9 Device 10 Group
		Net information	Device pin construction and wiring patterns
		Artwork information	Figure pattern other than wiring pattern
		Package information	Package figure information
		External terminal information	Figures and names of external terminals
		Internal terminal information	Figures and names of internal terminals
		User expandable information	Arbitrarily expandable data of the format user “Definition” = “Value” can be arbitrarily defined
Definition data	Definition of information which can be repeatedly used. It may be referred to from board data.	Layer definition	Shapes of layer construction, conductor layer(s) and insulation layer(s) – including scooped partsuch as a cavity
		Land definition	Shape of land (pad)
		Via definition	Diameter of via (pad stack) and landshape in each layer
		Device definition	Pin and package shape of embedding device
		Basic pattern information	Usable pattern elements in the defined data Types of figures are the same as in board data
		User expandable information	Arbitrarily expandable data of the format user “Definition” = “Value” can be arbitrarily defined

2) Data structure

The data structure of FUJIKO is based on the board data shown in Figure 2.1. Repeatedly used data information is formalized and is possible to identify definition data. The data expandable by users can be added to the board data and definition data.

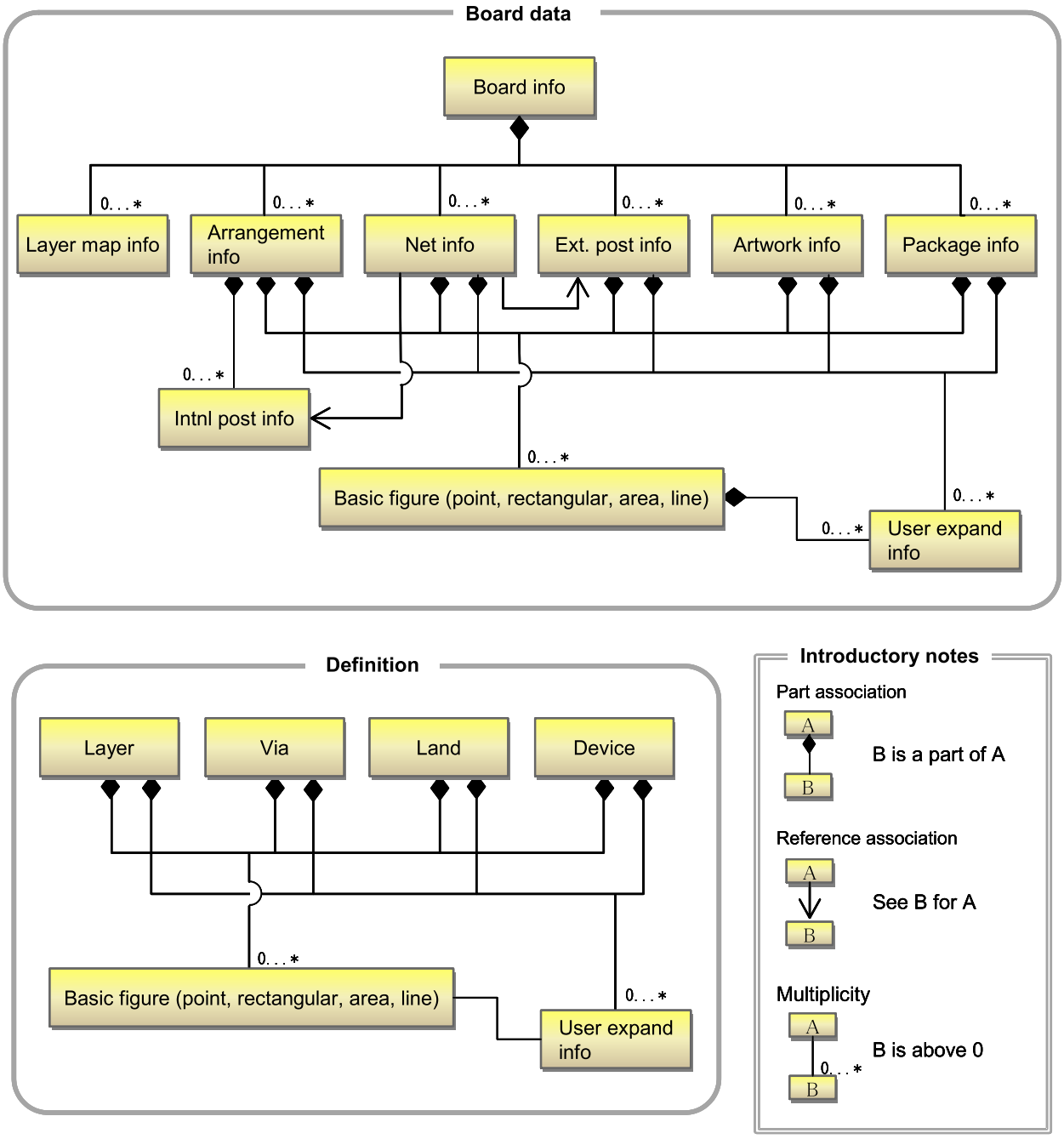


Figure 2.1 – Data structure

2.1.2 File structure

File structure is either of the following two methods.

1) Each definition data and board data are stored in one file as shown Figure 2.2 (recommended).
2) Definition data are stored in a separate file as shown in Figure 2.3.

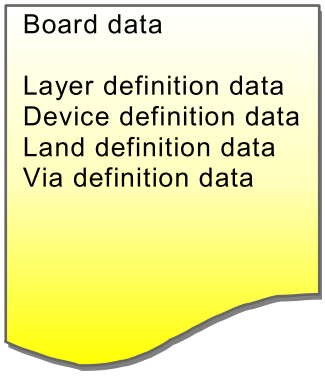


Figure 2.2 – One file structure (recommended)

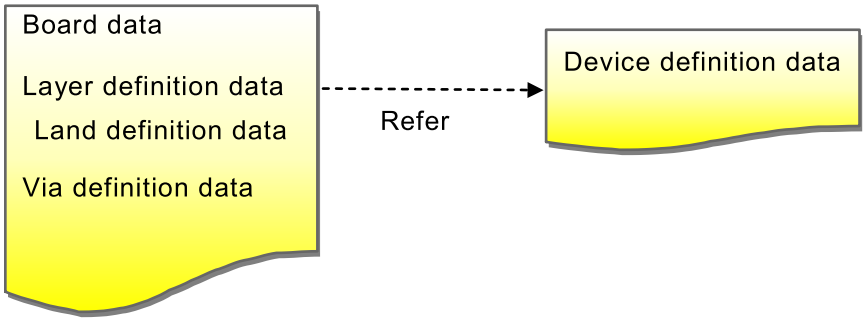


Figure 2.3 – Two-File structure

2.2 3D expression

FUJIKO format is expressed in 3D coordinates. 3D coordinate expression is a space expressed by three diagonal axes, X, Y and Z.

2.2.1 Coordinates

The coordinates of this format are shown in Figure 2.4 and have the following definitions.

1) Rotation of an axis is anti-clockwise.
2) Selection of unit length may be selected from mm, μm and nm.
3) Directions of axes are horizontal direction for x-axis, side direction for y-axis and vertical (height/thickness) direction for z-axis.

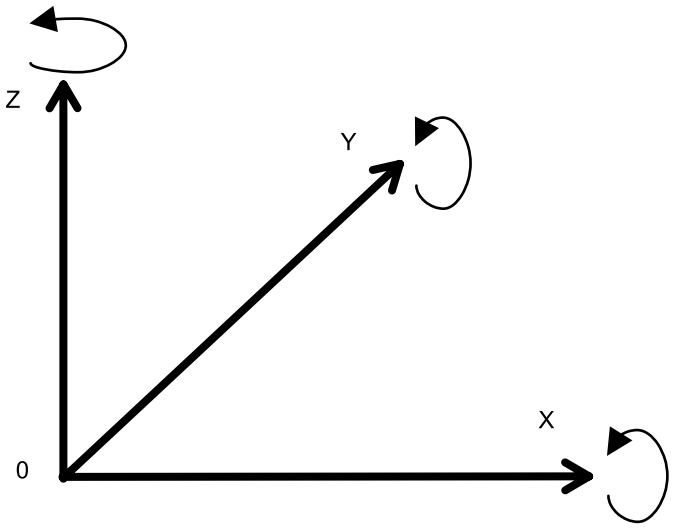


Figure 2.4 – Definition of coordinates

2.2.2 Position description

Specification of a 3D position is available as shown in Figure 2.5 to indicate layer structure and 3D coordination. Directions of axes can be expressed in horizontal direction for x-axis, side direction for y-axis and height direction for z-axis.

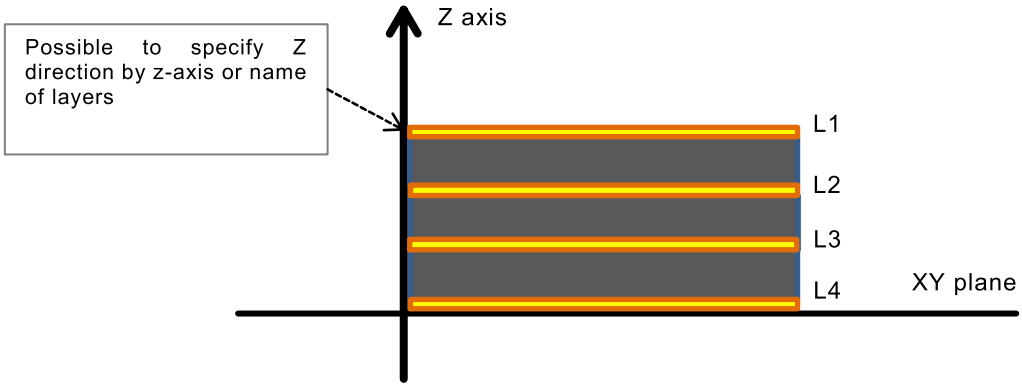


Figure 2.5 – Position definition

2.2.3 Relation between coordinate origin and board position

There is no specified relation between coordinates origin [(x, y, x) = (0, 0, 0)] and the board position as shown in Figure 2.6.

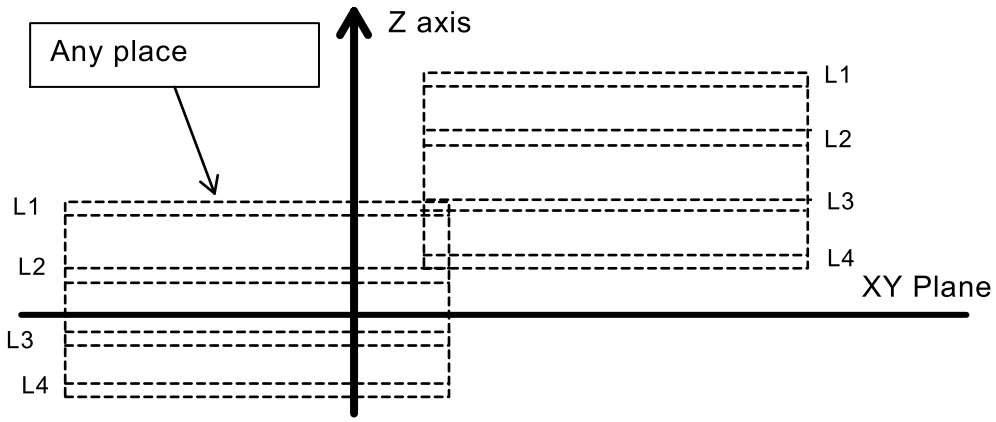


Figure 2.6 – Relation between coordinates and board position

2.3 Layer concept

There are two types of layers, conductor layer and virtual layer as illustrated in Figure 2.7. Characteristics of layers are explained below. The conductor layer is the layer coinciding with the terminals of an embedding component and a conducting layer. The conductor layer with internal posts that can be connected to the embedded device is the embedding layer. This concept is not applicable to embedding of a device which is not connected to a conductor layer, such as vias. A virtual layer is considered as a virtual conductor layer at interconnection points of an embedding component. This format can maintain coordinate data and design data in both of layer base and the 3D Z axis base design. It is recommended, however, that the data maintenance in the layer base in the case board structure is described within the description made in EB01. Use of 3D Z coordinate base can be used for describing design data such as for SiP which may not be an appropriate use of the above structure. The 3D Z coordinate base may not be appropriate to describe information necessary in the production process. Additional information transfer other than defined the present format data may be necessary between processes (among designs and design to production) and efficiency may be lowered in design and production.

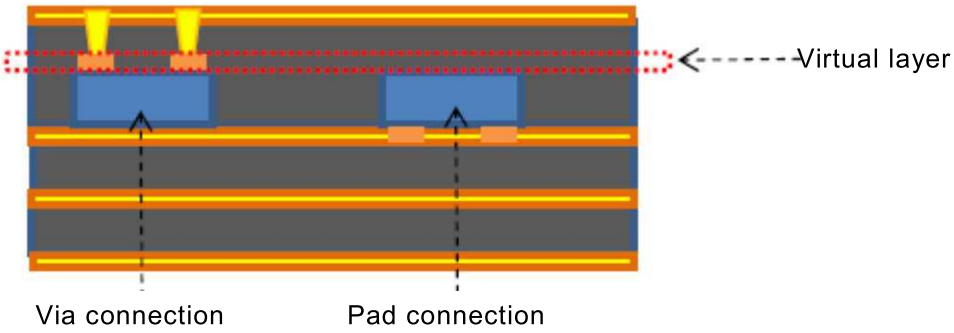


Figure 2.7 – Layer concept

2.4 Substrate data

Board data are to keep information of the basic elements of a device embedding substrate. There are the following nine types of information. Each type of the information is illustrated in the board data of Figure 2.1. Package information is held in case there is no internal connection information of embedded components.

1) Layer map information
2) Device arrangement information
3) Basic forms

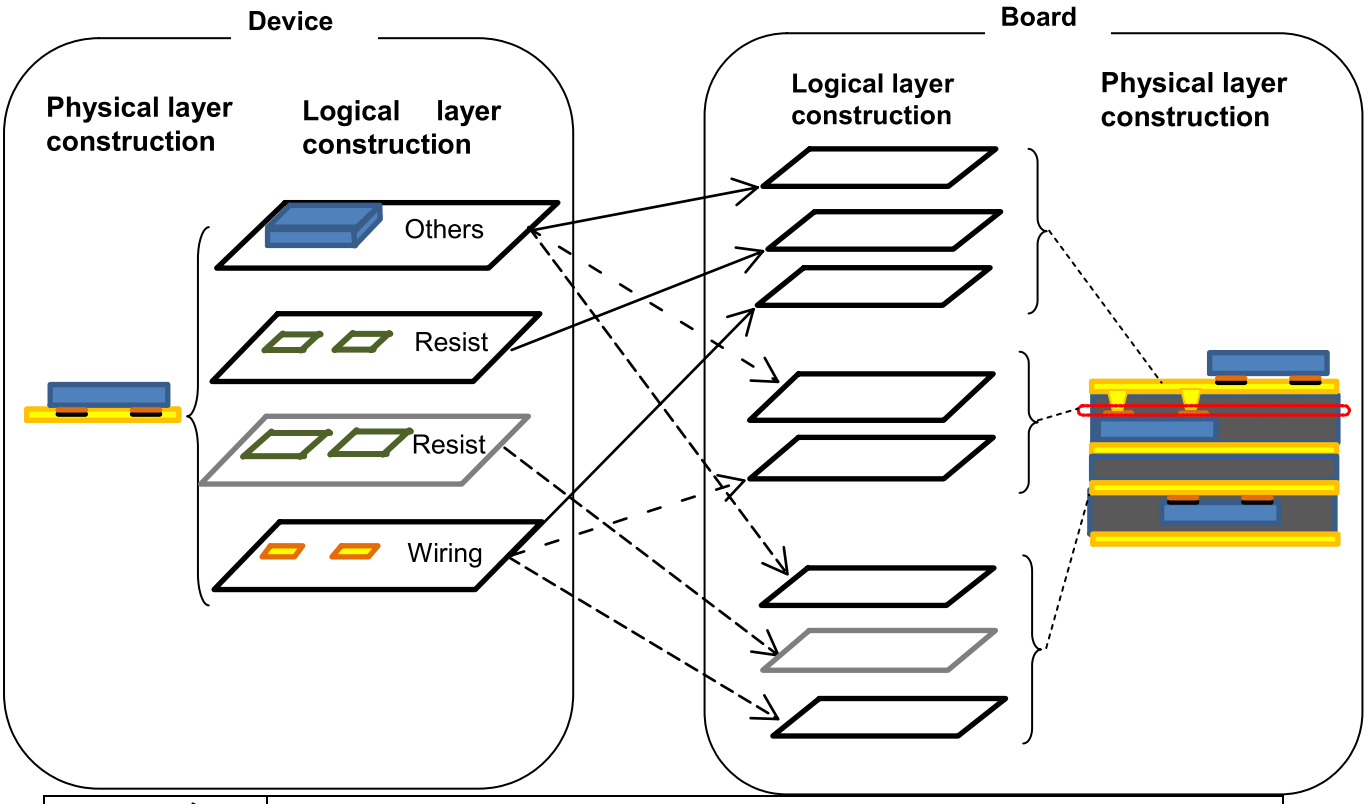
4) Net information
5) Artwork information
6) Package information
7) External port information
8) Inside port information
9) User data expansion information

2.4.1 Layer map information

This information maintains the relation between inner and outer layers as devices are mounted and embedded, as shown in Figure 2.8 and Figure 2.9.

1) Information of mounting layers

The information shows connections in each mounting layer and mounting direction.



——→	Device is embedded in layer = L1 (conductor layer), and connected in L1
– – – – – →	Device is embedded in layer = L3 (conductor layer), and connected in L3
– – – – →	Device is embedded in layer = L2 (conductor layer), and connected in L2-U11 (virtual layer)

Figure 2.8 – Construction of mounting layers

2) Omission of mounting layers

Logic layers for embedding devices and for boards are combined in case the layer map information is omitted. It is possible only in the case where there is only one logic layer of the same type in one physical layer.

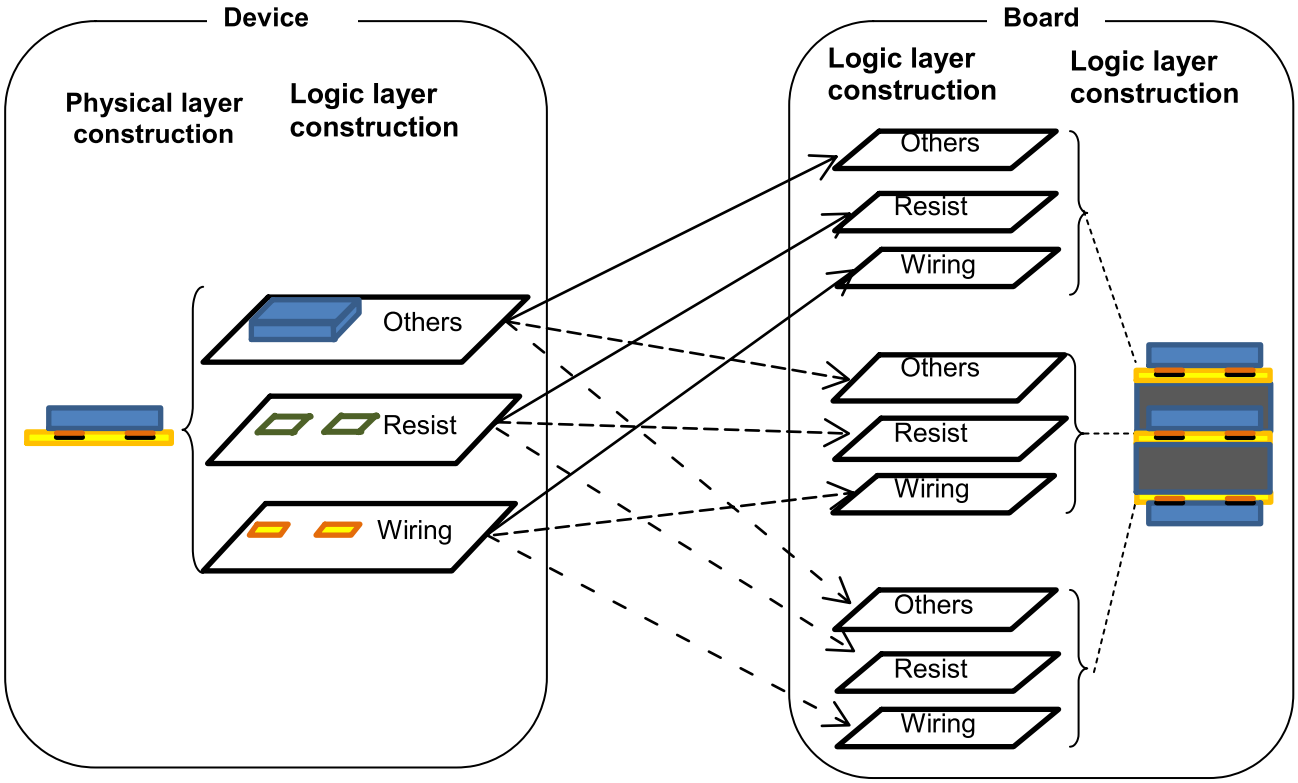


Figure 2.9 – Construction in the case of omission of mounting layers

2.4.2 Device arrangement information

The information has the position, figure and attribute of a device on a board. The external posts of a device become automatically internal posts (terminals) of a board.

1) Device attributes

   Name of a device on a board is the reference name of the device.

2) Device position attributes

   It is possible to specify the position in the following two ways (layer base design/3D coordinate design)

   a) XY coordinates/Z axis rotation/embedding layer/embedding direction/off-set/Connection terminal position in layer

   b) XYZ coordinates/XYZ axes rotation

3) Figure attributes

   Specified name of a device

2.4.2.1 Attribute of device position and arrangement

1) Layer definition

There are two ways of describing the vertical position of an embedded device for layer and Z axis. Details are shown in Figure 2.10 and Figure 2.11.

a) Pad connection

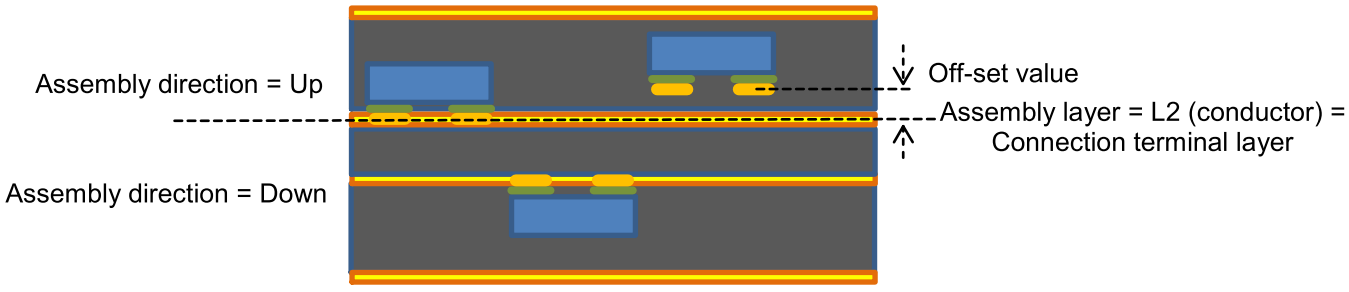


Figure 2.10 – Layer definition in pad connection

b) Via connection

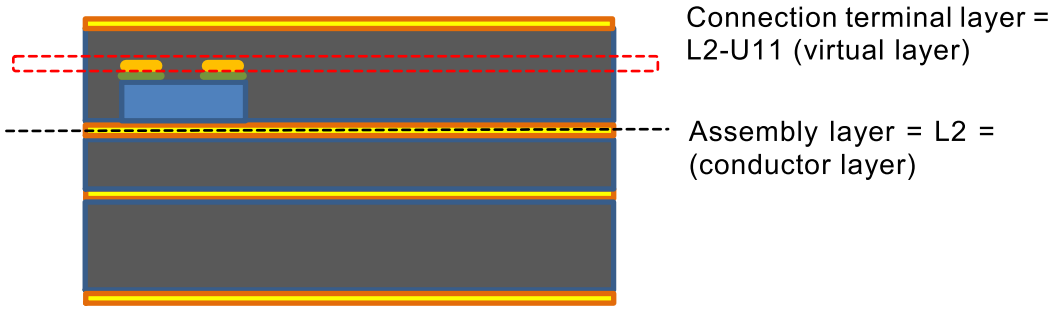


Figure 2.11 – Layer definition in via connection

2) Z coordinate definition

It is possible to use XYZ coordinates and XYZ axes rotation as the position specifying parameters.

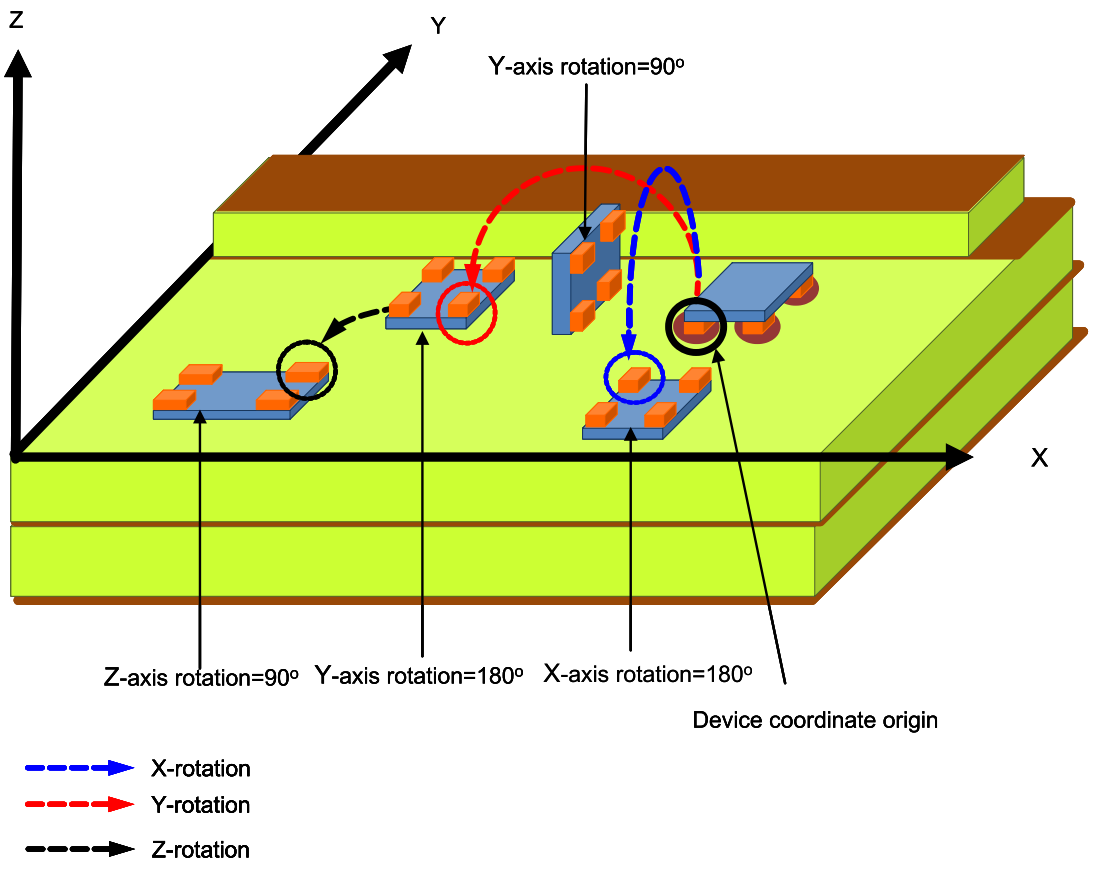


Figure 2.12 – XYZ axes rotation direction

2.4.3 Basic figures

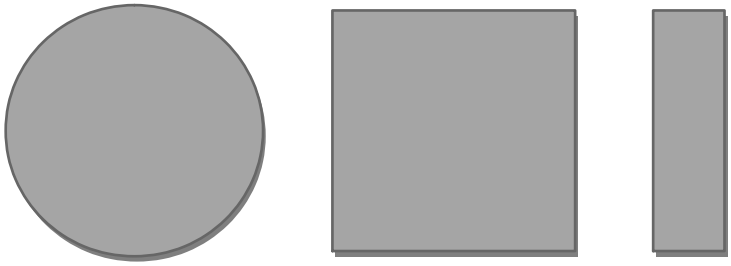
Figures of the following ten (10) types are available as figures in a board.

1) Point
2) Area
3) Line
4) Text
5) Bonding wire
6) Semi-sphere
7) Rectangular prismoid
8) Via
9) Device
10) Group

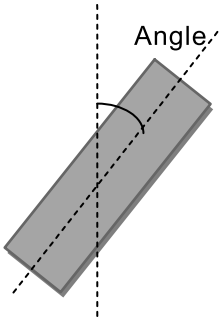
2.4.3.1 Point

It is possible to specify round, angle and rectangular shapes as shown in Figure 2.13.

1) Shapes of round, square and rectangular



2) Rotation angle



3) Thickness

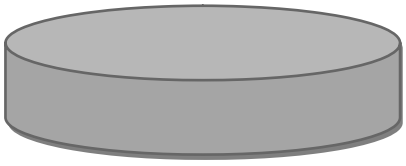
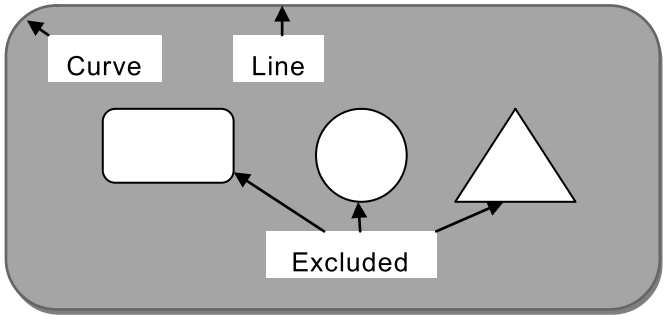


Figure 2.13 – Point

2.4.3.2 Area

Area can be specified as indicated in Figure 2.14.

1) It is a closed shape with many components and can specify line/curve as composing elements and excluded parts



2) Thickness

Figure 2.14 – Area shapes

2.4.3.3 Line

Line can be specified as indicated in Figure 2.15.

1) Can specify a continuous line having line and curve as composing g elements.

2) Can specify an extruded shape (round/angle).

3) Can specify types of cross sections (round or rectangular shape) and thickness

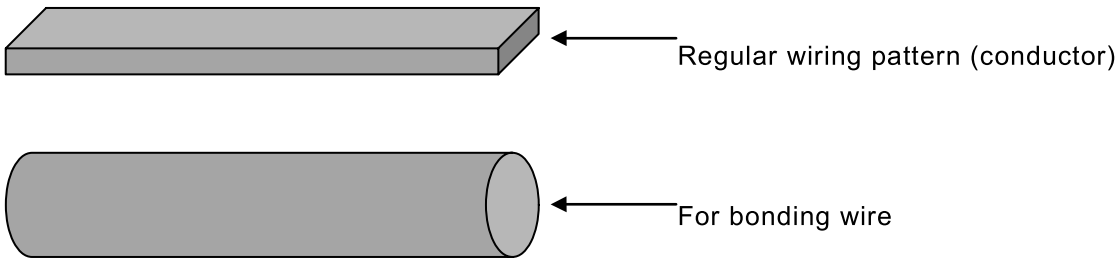
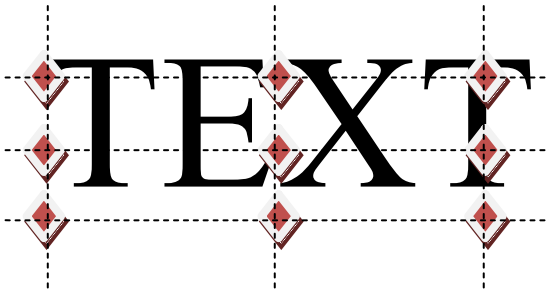


Figure 2.15 – Area shapes

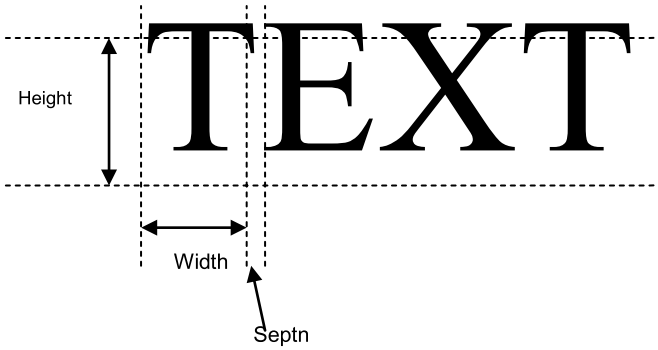
2.4.3.4 Text

Text is able to specify as indicated in Figure 2.16 with the origin of a letter, its height, with and separation and inclination.

1) Original points of letters



2) Letter height/width/separation



3) Letter angle

Figure 2.16 – Letter data

4) Possible to maintain expanded patterns of vector font of text

Figure 2.17 – Text shape

2.4.3.5 Bonding wire

Bonding wire is able to specify as indicated in Figure 2.18 for figure types 1 to 4.

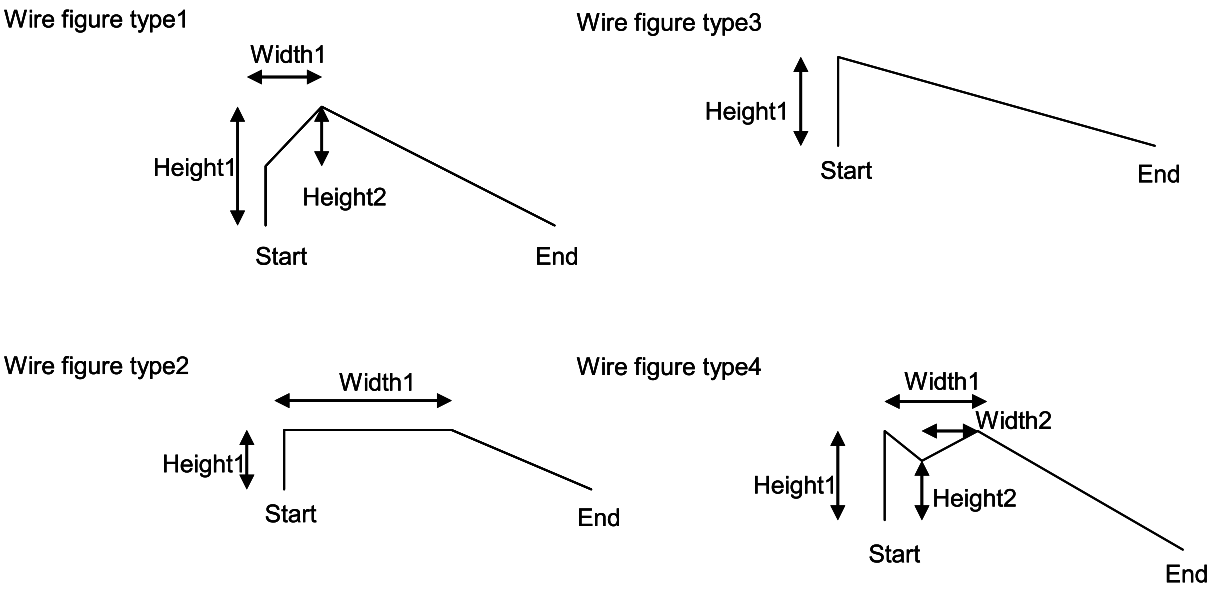


Figure 2.18 – Bonding wire information

2.4.3.6 Semi-sphere

Half ball is able to specify as indicated in Figure 2.19.

1) Radius
2) Rotation angle

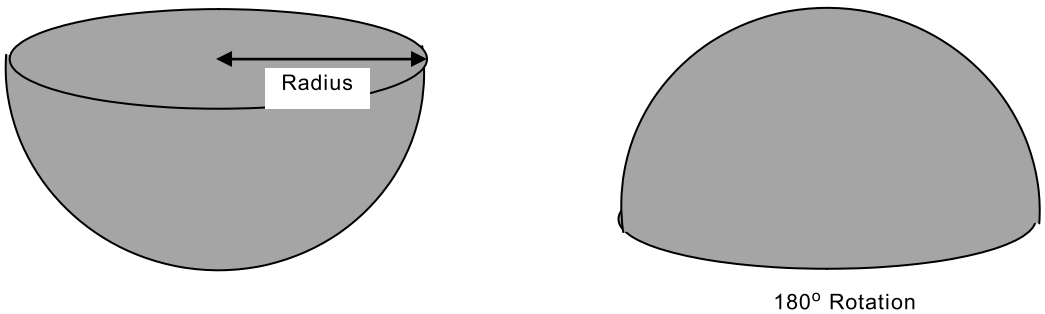


Figure 2.19 – Wire bonding shape

2.4.3.7 Rectangular prismoid

Rectangular cone is able to specify as indicated in Figure 2.20.

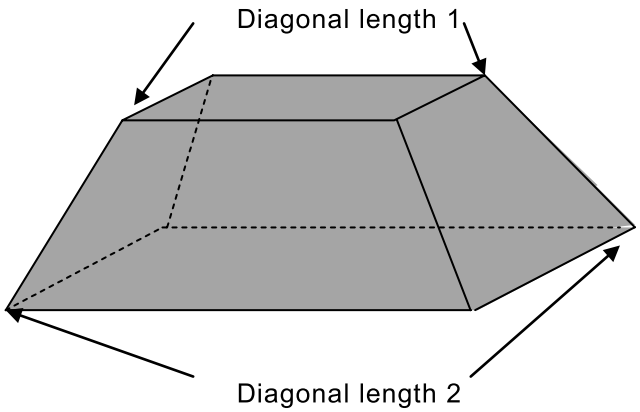


Figure 2.20 – Rectangular prismoid

2.4.3.8 Via

It is possible to specify the following three types of via as shown in Figure 2.21

1) Can specify via definition and refer to hole information and land information.
2) Can specify attributes of connection and un-connection for each layer.
3) Can specify grid positions of device mounting for numbers and separation of devices.

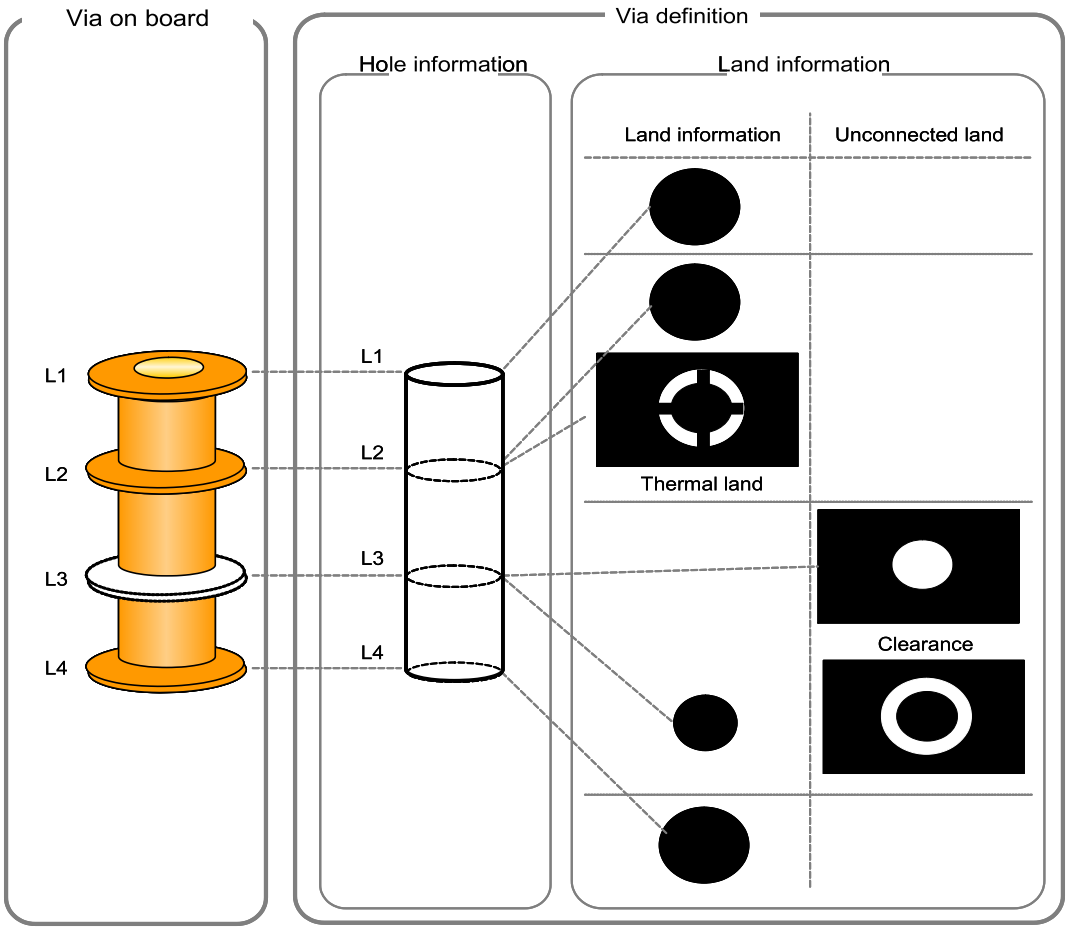


Figure 2.21 – Examples of via specification

2.4.3.9 Device

It is possible to specify the following three types. Figure 2.22 shows examples.

1) Can specify names of device structure as attribute of the device.
2) Device figures can be arranged on a board as specified by device structure.
3) Can specify grid positions of device mounting for numbers and separation of devices..

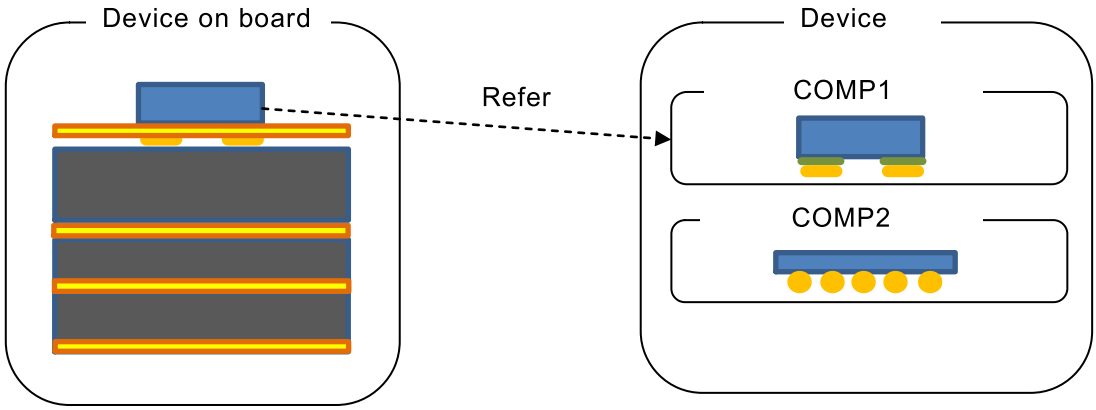


Figure 2.22 – Device definition

2.4.3.10 Group

Group is a combination of basic figures such as dimension lines as shown in Figure 2.23. It can be handled as one figure.

Figure 2.23 – Example of group such as dimension lines

2.4.4 Net information

The net information maintains the connection terminal and wiring pattern information shown in Figure 2.24. Connection terminal information is the information giving interconnection between internal pads of a device or the connection of internal pads and external pads.

1) Connection pad information
   a) Names of internal pads
   b) Names of external pads
2) Wiring figures
   a) Point
   b) Area
   c) Line
   d) Bonding wire
   e) Semi-sphere
   f) Via

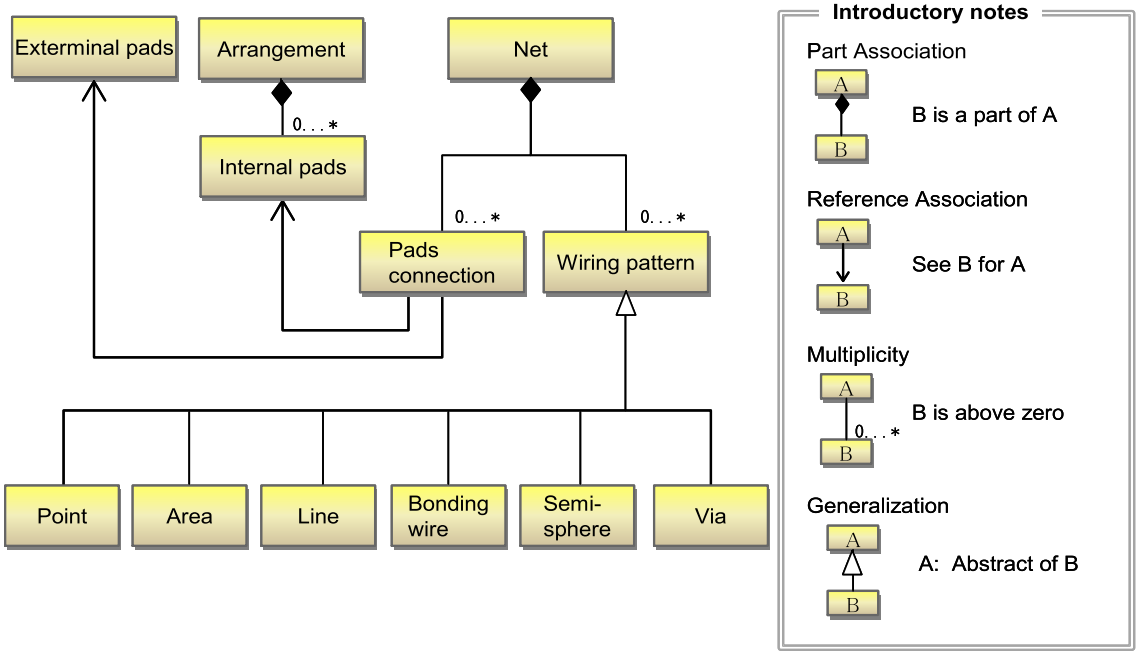


Figure 2.24 – Data structure of net information

2.4.5 Artwork information

Artwork information maintains artwork figure data on a board which are not included in the net information. Artwork figures include the following basic figures. Symbol mark, mold, spacer and remarks are also included in the information.

1) Point
2) Area
3) Line
4) Text
5) Bonding wire
6) Semi-sphere
7) Rectangular prismoid
8) Via
9) Device

2.4.6 Package information

The package information maintains the figures when the main structure has the package figure. Device package figure can use the following basic figures.

1) Point
2) Area
3) Line
4) Text
5) Semi-sphere
6) Rectangular prismoid

2.4.7 External port information

External points are the terminals of signals to supply electronic information from embedded devices and board to outside of the board. The point information maintains the shape and names of the external points the board structure has. The following shapes can be used for the information.

1) Point
2) Area
3) Line
4) Semi-sphere
5) Via

2.4.8 Internal port information

Internal ports are the terminals when a device is embedded to supply data to external ports. They connect the inside net of the board to outside world and have the same structure as the external ports.

2.4.9 User expansion information

The user expansion information illustrated in Figure 2.1 is possible to expand of definition data and board data. Property is expandable data by the user of the format. It is possible to apply this property to a part of definition data and board data. It is possible to select any combination of “definition name” = “data”.

2.5 Defined data

Defined data are the definition of repeatedly used information. The definition data illustrated in Figure 2-1 contain the following four definitions.

1) Layer definition
2) Land definition
3) Via definition
4) Device definition

2.5.1 Layer definition

Layer definition includes the two types of information, physical information which gives physical figures and construction, and logical information which can be specified arbitrary necessary in design. The virtual layer is included in the physical information. It is also possible to link physical layer and logical layer.

(1)Physical information
- a) It maintains physical layer structure and its order
- b) It maintains attribute of each physical layer such as size, shape and material of both conductor and insulator layers
- c) It maintains types of conductor and virtual layers

(2)Logical layer information
- a) Layout of figures (conductor, solder resist, symbol marks, etc.)
- b) Polarity of a figure (positive or negative)
- c) Link information to physical layer
- d) Position relation with physical layer

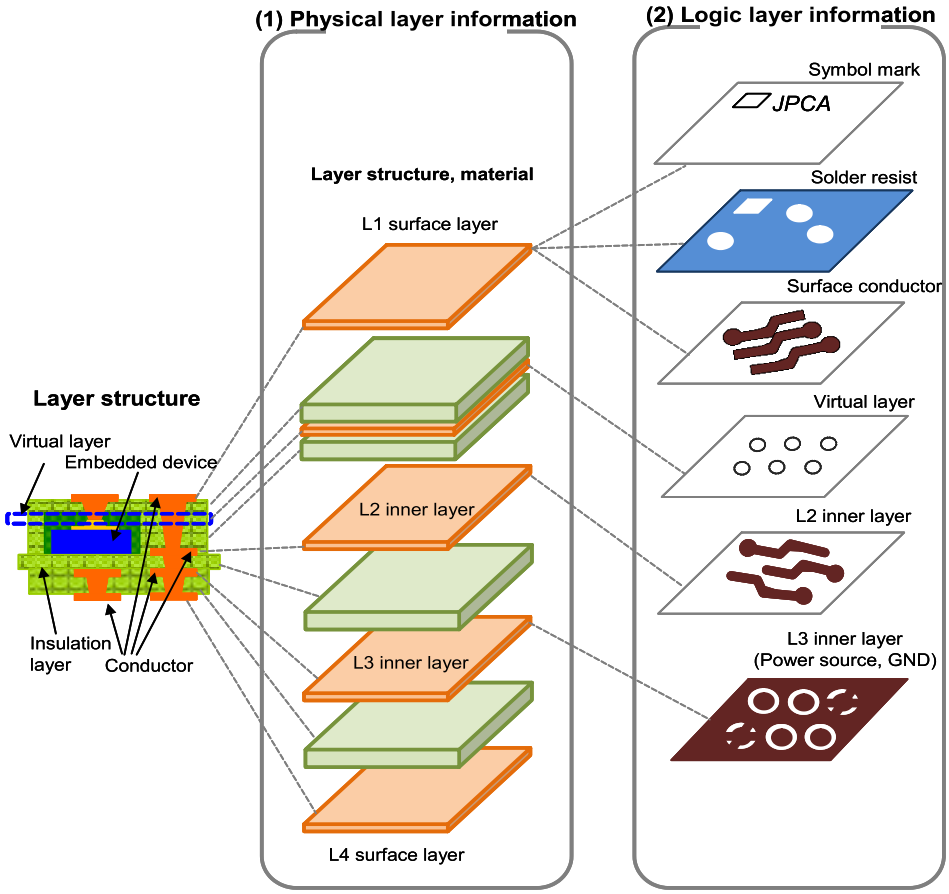


Figure 2.25 – Relation of layer definition data

2.5.2 Land definition

It defines the land information used in device embedded substrate as shown in Figure 2.26.

1) It contains a land having more than one basic figure
2) It contains a land combined with positive and negative figures
3) It contains all the lands except a conductor land having resist

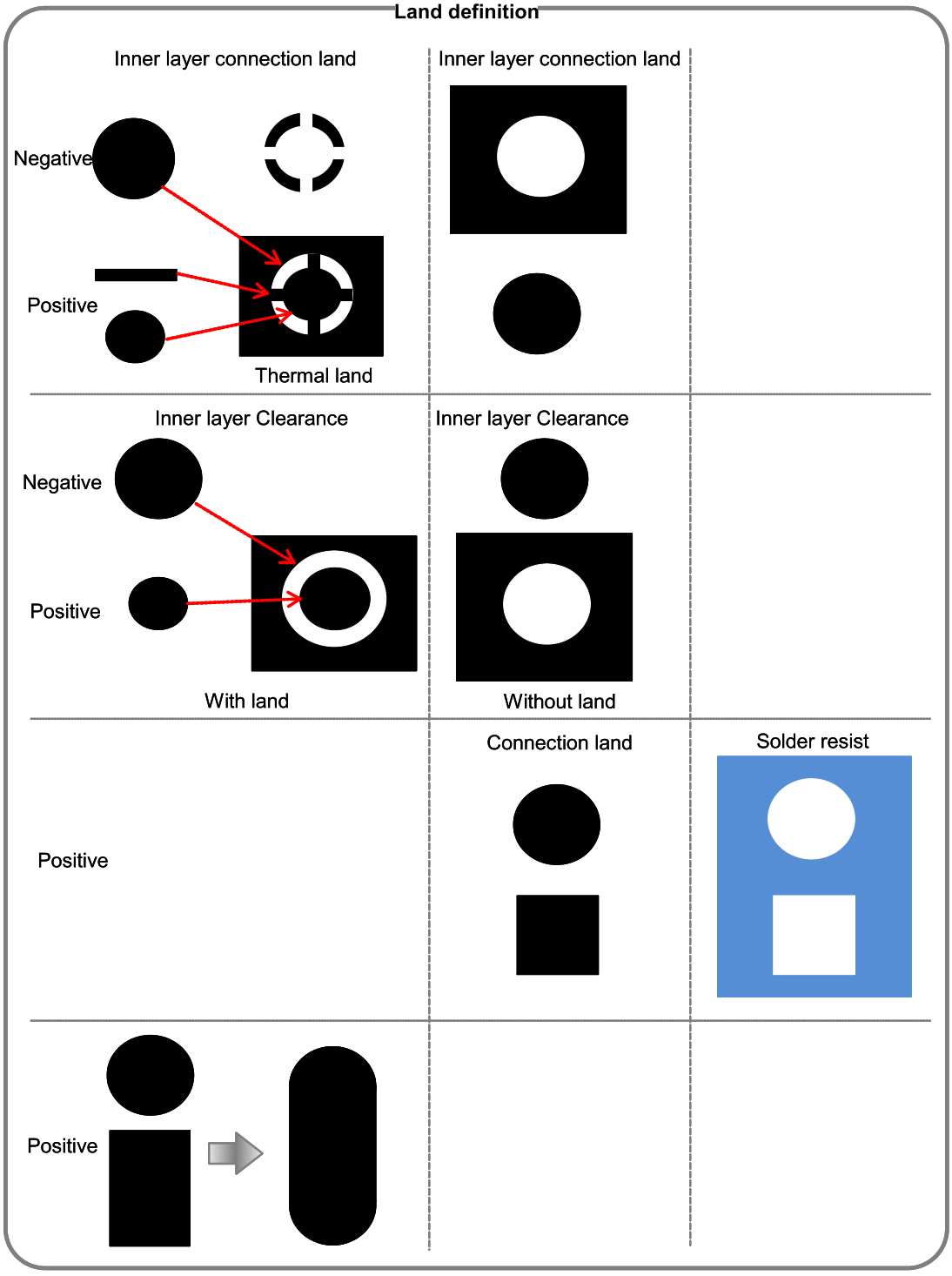


Figure 2.26 – Land definitions

2.5.3 Via definition

Via definition is the information of holes and lands used in a device embedded substrate as illustrated in Figure 2.27.

(1) Hole information

a) Shape of a hole is round or rectangular
b) It shows the area a through-hole exists
c) It shows the area for an existing build-up hole

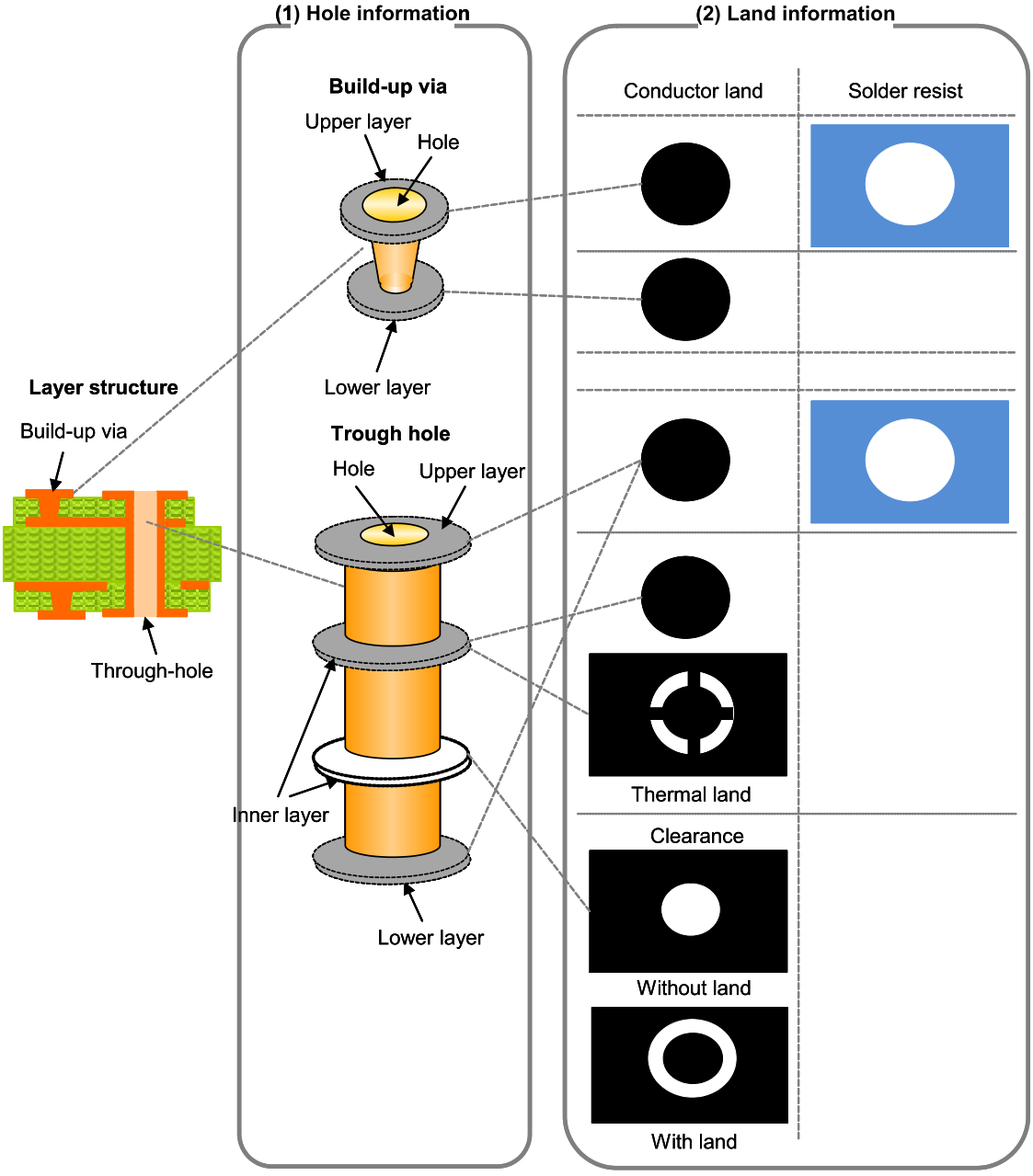


Figure 2.27 – Relation between hole information and land information

2.5.4 Device definition

Information of the component arrangement on a board is kept in the library.

Two patterns of information arrangement can be held as illustrated in for SiP, modules and MEMS for complete component which holds wiring drawing completely as shown in the figure, and the one connection information and wiring drawing are simplified into black boxes as shown in Figure 2.29 for packages and modules.

1) Embedded device with information of internal connections (the same construction as the board information to be described later).

a) Layer information within component	Layer construction, shape
b) Component arrangement information	Position information of component
c) Net information	Wiring shape, internal and external
d) terminal connection information	
e) Artwork information	Shapes other than 1) to 3)
f) Package information	Package and module shapes
g) External terminal information	External terminal shape, name

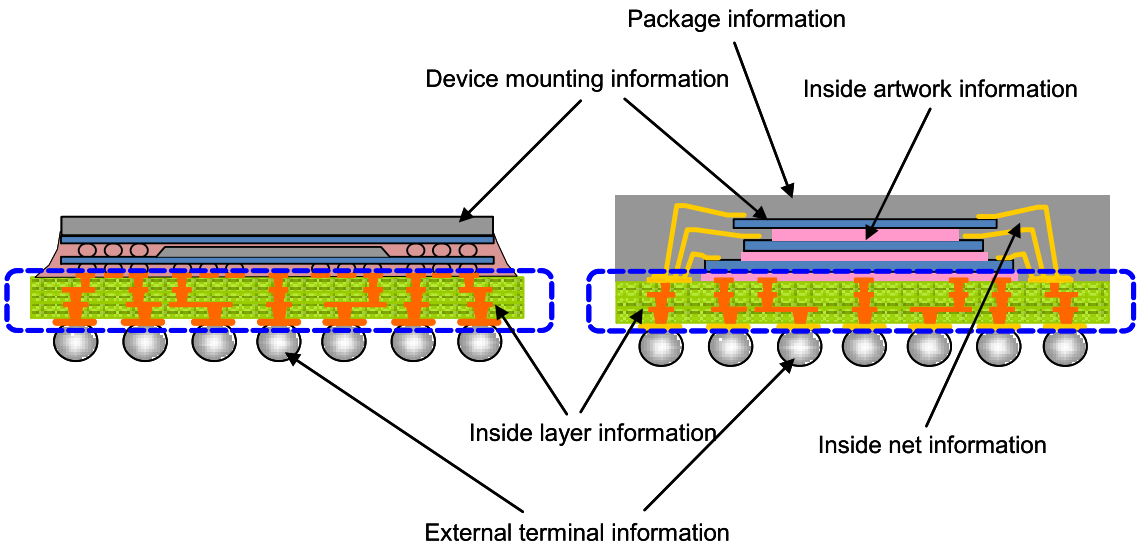


Figure 2.28 – Definitions of SiP, module and MEMS

2) Package and mold components

a) Package information	shape of the package
b) External terminal information	shape and name of external terminal

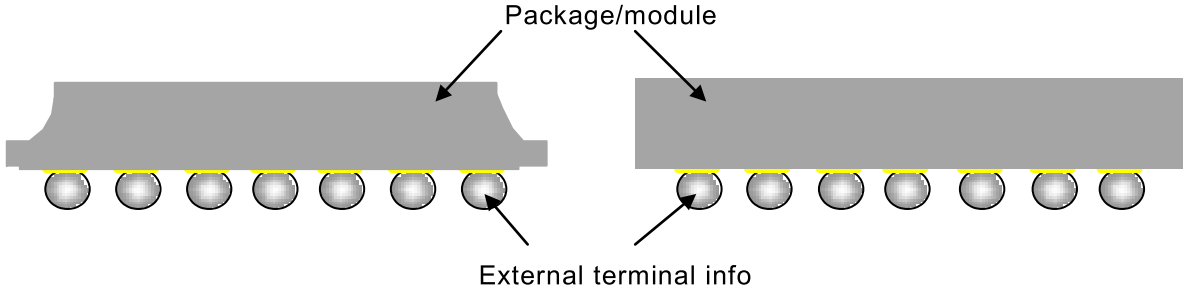


Figure 2.29 – Definitions of package and mold components

2.5.5 User expansion definition

The user expansion definition makes it possible to enlarge a part of definition data and board data as shown in Figure 2.1. Property is the data which a format user can freely expand to his/her usage. It is possible to apply to definition data and a part of board data. It is possible to give combinations of “definition” = “value” as a user likes.

3 Terminology

Term	Abbreviation	Meaning
Artwork information		Artwork information in this document shows SiP not included in Net and figure data in board (symbol mark, inside of Sip, mold, spacer, remarks, etc.).
Board information		Total information of device embedded substrate including embedded devices.
Bottom hole diameter		The diameter of the exit side of a hole made in a substrate.
Bottom layer		The term “bottom layer” is used differently from the names of layers here to indicate the bottom side when a substrate is processed.
Chip stack		A package of semiconductor chips stacked vertically.
Clearance		The area around a through-hole where there is no conductor to prevent electrical connection between a large conductor area such as for power supply or ground and a plated through-hole.
Computer aided manufacturing	CAM	The interactive use of computer systems, programs, and procedures in various phases of a manufacturing process wherein, the decision-making activity rests with the human operator and a computer provides the data manipulation functions.
Computer aided design	CAD	The interactive use of computer systems, programs, and procedures in the design process wherein, the decision-making activity rests with the human operator and a computer provides the data manipulation function.
DXF	DXF	Data format for AutoCAD. It generally means a type of data format to draw figures using board CAD data.
Design document		Design document in this document is the documentation of information necessary in circuit board design.
Device arrangement information		Information includes position, shape and attributes of embedding device included in the net information in this PAS.
Device embedded substrate		A substrate in which active device(s) (semiconductor device) and/or passive device(s) (e.g., resistor or capacitor) is formed using thick film technology or embedding them within the substrate.
Electronic circuit simulation		Composing elements forming devices and circuit are expressed in mathematical and logical models and confirm their total operation by means of a computer.
Electronic design automation	EDA	A generic term covering soft-ware, hard-ware and technique to use them in automatic design of electronic equipment and semiconductor devices.
Flip chip	FC	A leadless monolithic circuit element structure that electrically and mechanically interconnects to a printed board by conductive bumps.
GERBER		A type of data format that consists of aperture selection and operation commands and dimensions in X- and Y-coordinates. (The data is generally used to direct a photo-plotter in generating photo-plotted artwork.)
Interposer		A material placed between two surfaces giving electrical insulation, redistribution of electrical connections, mechanical strength and/or controlled mechanical and thermal separation between the two surfaces. NOTE An interposer may be used as a means for redistributing electrical connections and/or allowing for different thermal expansions between adjacent surfaces.

Term	Abbreviation	Meaning
Land		A portion of a conductive pattern usually used for the connection and/or attachment of components.
Land definition		A definition in this PAS to maintain a shape of specific land, pad, solder resist and others.
Layer definition		Combination of physical information of shape and construction and logic information giving design and production units in this PAS.
Layer map		A map showing relation between devices and board as devices are arranged on a board.
Library		Data base of design information based on design document as to be used in board CAD.
Logical layer		A layer which can be arbitrarily formed in case it is difficult to physically express a layer in design. It is possible to relate it to a physical layer. It is different from the layers in a multi-layer substrate.
Micro-electro-mechanical system	MEMS	A system integrating micro-machine, mechanical elements, sensor, actuator, and electronic circuit into one module.
Net information		Device pin construction and wiring pattern in this PAS.
Package information		Shapes of board and devices when they have package shape patterns in this document.
Package on package	PoP	A single or multiple package(s) are mounted on a package of a single chip or multiple chips as single package.
Pad		See “land”.
Physical layer		A layer consisting of a physical layer construction and structure.
Port information		Information of figures and names of external terminals of a device or a substrate with terminals.
Structure		The total structure of a device embedded substrate and/or surface device mounted to the substrate are called “structure” in this PAS.
System in a package	SiP	A multi-chip package (MCP) that performs a system function.
Thermal land		Heat energy may leak to outside of a land/Through-hole when a device is soldered on a large pattern such as power supply or ground. A cut is often made around such a soldering point to prevent thermal dissipation.
Through silicon via	TSV	A hole is made in a silicon chip and filled with metal to electrically connect upper and lower side of the chip for 3D stacking package.
Top layer		The term “top layer” is used differently from the names of layers here to indicate the top side when a substrate is processed.
Top hole diameter		The diameter of the entrance side of a hole made in a substrate.
Via definition		A plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material.
Virtual layer		Name of the layer connecting conductor layers when a device is embedded. It corresponds to the connection point of a device terminal specified in EB01.
Wire bonding	WB	Micro-bonding between a die and base material, lead frame, etc.

4 Commentary – Additional information

The statement here is to state additional information to this document and not a part of the PAS.

I. Process of preparation of this document

Printed wiring board has been used in various equipment including electronic circuits and wide ranges of equipment requiring electronic circuitry. It is expected to expand its applications to wider ranges of applications. However, unification of design, production and tests is not available yet in each step of the process and effective realization of design, effective production process reduction are not realized yet. Effective use of design information of boards necessary in production of boards is now an urgent requirement by means of automation and rationalization of processes. The committee of developing data format of printed wiring boards in JPCA was formed in July 1992. The data format committee has been working to develop a format applicable to different CAD systems, highly requested by various applications. They developed “JPCA data format specification” in August 1993. The CAD technology then was not widely used yet and communication among printed wiring board manufacturers was not sufficient enough. In 2008, production of device embedded substrates started and 3D CAD to describe the status of device embedding was required in the design stage of the device. Design information of hole formation, appearance test, electric test were necessary to evaluate performance of products. A committee of data format standardization was formed in the committee of device embedded substrate technology in JPCA in July 2011. The new committee is to develop data format for device embedded substrate standard for circuit board, electric test equipment, image test equipment, and assembly equipment together with experts from related manufacturers. The present document, EB02, was developed to supply the required information to the industry and we are also preparing an international standard by proposing this document to IEC (International Electrotechnical Commission).

The main issues of this document are the following two.

1) Data of board CAD and of FUJIKO and both necessary data of production facility and of test equipment producers are compiled to make it possible to unify the necessary information in production as shown in Table 1.1.
2) Data format is formed to enable simulation of design, production and characteristics of device embedded substrate. Know-how of realizing total assembly technology is necessary for printed wiring board production technology based on characteristics of device embedded substrate.

II. Additional explanations (numbers are from the section numbers of this document)

1 Scope

1.1 Purpose

This section is prepared to make it simple to have 3D data and data of each production and test equipment based on complex electronic circuitry based on board CAD data for device embedded substrate design as shown in Figure 1.1.

1.2 Application range

1.2.1 Product

The present document covers device embedded substrate and SiP (system in package). The contents of this document can also be applicable to conventional electronic circuit board (printed wiring board).

1.2.2 Process

The process statement covers necessary data maintenance from design to production of device embedded substrate, and state necessary data in each process.

1.3 Features

This chapter states the features of data format in this document.

2 File description

Detailed description is made for structure of each data format (2.1 to 2.6).

_____

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

3, rue de Varembé
PO Box 131
CH-1211 Geneva 20
Switzerland

Tel: + 41 22 919 02 11
Fax: + 41 22 919 03 00
info@iec.ch
www.iec.ch