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Test methods for the characterization of organic transistors and materials

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TEST METHODS FOR THE CHARACTERIZATION OF ORGANIC TRANSISTORS AND MATERIALS

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1620™-2008	113/184/FDIS	113/194/RVD

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IEEE Standard for Test Methods for the Characterization of Organic Transistors and Materials

Sponsor
Microprocessor Standards Committee
of the
IEEE Computer Society

Approved 26 September 2008
IEEE-SA Standards Board

Abstract: Recommended methods and standardized reporting practices for electrical characterization of printed and organic transistors are covered. Due to the nature of printed and organic electronics, significant measurement errors can be introduced if the electrical characterization design-of-experiment is not properly addressed. This standard describes the most common sources of measurement error, particularly for high-impedance electrical measurements commonly required for printed and organic transistors. This standard also gives recommended practices in order to minimize and/or characterize the effect of measurement artifacts and other sources of error encountered while measuring printed and organic transistors.
Keywords: electrical characterization, FET, flexible electronics, high impedance, nanocomposite, nanotechnology, OFET, organic electronics, organic transistor, printed electronics, printing, transistor

IEEE Introduction

This introduction is not part of IEEE Std 1620-2008, IEEE Standard for Test Methods for the Characterization of Organic Transistors and Materials.

This standard covers recommended methods and standardized reporting practices for electrical characterization of organic transistors. Due to the nature of organic transistors, significant measurement errors can be introduced if not properly addressed. This standard describes the most common sources of measurement error and gives recommended practices in order to minimize and/or characterize the effect of each.

Standard reporting practices are included in order to minimize confusion in analyzing reported data. Disclosure of environmental conditions and sample size are included so that results can be appropriately assessed by the research community. These reporting practices also support repeatability of results so that new discoveries may be confirmed more efficiently.

The practices in this standard were compiled from research and industry organizations developing organic transistor devices, materials, and manufacturing techniques. These practices were based on standard operating procedures utilized in laboratories worldwide.

This standard was initiated in 2002 to facilitate the evolution of organic transistors from the laboratory into a sustainable industry. Standardized characterization methods and reporting practices create a means of effective comparison of information and a foundation for manufacturing readiness.

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Test Methods for the Characterization of Organic Transistors and Materials

1. Overview

1.1 Scope

This standard describes a method for characterizing organic electronic devices, including measurement techniques, methods of reporting data, and the testing conditions during characterization.

1.2 Purpose

The purpose of this standard is to provide a method for systematically characterizing organic transistors. These standards are intended to maximize reproducibility of published results by providing a framework for testing organic devices, whose unique properties cause measurement issues not typically encountered with inorganic devices. This standard stresses disclosure of the procedures used to measure data and extract parameters so that data quality may be easily assessed. This standard also sets guidelines for reporting data, so that information is clear and consistent throughout the research community and industry.

1.3 Electrical characterization overview

1.3.1 Testing apparatus

Testing is performed using an electronic device test system with measurement sensitivity sufficient to give an accuracy of at least ±0.1% (minimum sensitivity at or better than three orders of magnitude below expected signal level). For example, the smallest current through an organic transistor is often the gate leakage current. If gate leakage is approximately 1 pA (10^{-12} A), the instrument shall have a resolution of 1 fA (10^{-15} A) or smaller. Additionally, due to the large (>1 GΩ) impedances encountered in organic devices, the input impedance of all elements of the test system shall be at least three orders of magnitude greater than the highest impedance in the device. Commercial semiconductor systems with the capability to characterize organic devices typically have input impedance values of 10^{16} Ω, which is a recommended minimum value.

This test method requires that the instrumentation be calibrated against a known and appropriate set of standards (e.g., National Institute of Standards and Technology, NIST). These calibrations may be performed by the equipment user or as a service by the equipment vendor. Calibration is not performed against a known organic field-effect transistor (OFET) or other FET-type device; the basic instrument operations (e.g., voltage, current, and resistance) are calibrated against some method traceable to a NIST (or similar internationally recognized standards organization) physical standard. Re-calibration is required according to the instrument manufacturer's recommendations or when the instrument is moved or when the testing conditions change significantly (e.g., temperature change greater than 10 °C, relative humidity change greater than 30%).

1.3.2 Measurement techniques

1.3.2.1 Required measurements

Characterization of the organic transistor requires at minimum the following two primary sets of measurements:

— The transfer (I_{DS} vs. V_{GS}) curves, which allow for preliminary determination of field-effect mobility, μ, and threshold voltage, V_T.

— The I versus V output (I_{DS} vs. V_{DS}) curves that provide saturation and general electrical performance information. This curve is used to determine whether the device exhibits FET-like behavior.

— The gate leakage (I_{GS} vs. V_{GS}) curves that characterize the gate dielectric quality and quantify leakage current from the gate to the channel. Leakage measurements are carried out prior to transfer or I versus V measurements to ensure gate dielectric integrity before subsequent measurements are performed. Gate leakage characterization is necessary to ensure that its magnitude is negligible to the magnitude of the drain current, so that reliable and useful device characteristics may be measured and key parameters extracted.

1.3.2.2 Recommended measurements

The following additional measurement is strongly recommended:

— The stray capacitance values C_{GD} and C_{GS}. Stray capacitance values have a negative effect on device switching speed and may affect device electrical characterization.

1.3.3 Repeatability and reporting sample size

Sample performance between different devices may vary due to variations in the fabrication process. Additionally, it is critical to determine how repeatable the reported results are. Therefore, sample size is to be reported thus:

— If no sample size is reported, it is assumed that the data represents a sample size of a single device (i.e., may not represent repeatable results).

— For sample sizes larger than one, the sample size is reported with the method of sampling (whether all devices were characterized, a randomly-chosen fraction of the total sample set, etc.).

A description of what the reported data demonstrates (average values, worst-case, etc.) is also required.

1.3.4 Application of low-noise techniques

Generally, lower absolute gate bias voltages cause smaller stress effects, such as shifts in the threshold voltage, than higher absolute gate biases. Depending on the device structure, this shifting may be reduced by ensuring that the device under test is properly grounded. This issue may be further improved if this grounding is through a low-impedance path to system ground.

In order for comparability between different device structures and eventual compatibility to nanoelectronics, voltages should be referenced to the corresponding film thickness (V_{GS}) and channel length (V_{DS}). Sufficient information is to be given so that electrical fields (V/cm) may be determined. Preferably, electrical field values are specified.

Due to optical sensitivity of some organic semiconducting materials, all measurements should be conducted inside a light-insulating enclosure that is preferably earth (safety) grounded. Optical isolation is recommended if exposure to ambient light causes a change of more than 1% from values obtained in the dark.

Due to the high impedances and extremely low current values being measured, proximity of personnel, heavy machinery, or other potential electromagnetic/radiofrequency interference (EMI/RFI) sources should be maintained as far away from the measurement system while in operation. This is of particular concern when measured voltages are below 1 mV or when current values are less than 1 μA.

2. Definitions, acronyms, and abbreviations

2.1 Definitions

For the purposes of this standard, the following terms and definitions apply. *The Authoritative Dictionary of IEEE Standards Terms* [B1][1] should be referenced for terms not defined in this clause.

2.1.1 bottom-contact device: A field-effect transistor structure for which the source and drain electrodes are located closer to the substrate than the semiconductor. Typically in a bottom-contact device, the source and drain will be located sandwiched between the gate dielectric and the semiconductor material.

[1] The numbers in brackets correspond to those of the bibliography in Annex A.

2.1.2 bottom-gate device: A field-effect transistor structure for which the gate electrode is closer (or adjacent) to the substrate than the channel. Devices that utilize a doped substrate (e.g., doped silicon wafer) as the gate electrode are generally bottom-gate devices.

2.1.3 bulk: Electrical connection to the substrate, and the corresponding voltage applied. Typically, this bias is applied only during device test through a ground chuck. Current flow is usually negligible through the substrate; therefore, in most circumstances no voltage will be applied to the bulk during device operation. However, negligible current flow must be verified during individual device tests. Since most OFETs reside on an insulating substrate, the electrical properties of the bulk are typically ignored.

2.1.4 characteristic: I_{DS} vs. V_{DS} for a fixed V_{GS}. *See also:* **output curve**.

2.1.5 C_{GD}: Capacitance measured between the gate electrode and the drain electrode.

2.1.6 C_{GS}: Capacitance measured between the gate electrode and the source electrode.

2.1.7 conductance (g_s): The slope of the output curve, expressed as

$$g_s = \frac{\partial I_d}{\partial V_d}$$

2.1.8 drain: Device electrode whose current flow is controlled by the conductivity of the semiconducting channel. Typically, the drain electrode is identical physically to the source electrode. The sign of the voltage at which the drain electrode is biased relative to the source electrode depends on the nature of the majority carriers. The bias is more positive for electrons and more negative for holes.

2.1.9 dwell time: Duration starting at the point in time when the measurement voltage is applied to the time when the measurement is recorded. Used to minimize measurement errors due to transient noise. Alternatively, sweep speed can be adjusted.

2.1.10 earth ground: Safety grounding directly to earth ground connection or instrument frame, typically separate of system/signal ground. Intended for shielding operator from high voltages and provides additional noise shielding.

2.1.11 EMI/RFI: Electromagnetic and radio-frequency interference, potential contributor to noise in measurements.

2.1.12 environmental condition: Real or artificial atmospheric conditions immediately surrounding the device under test. These values are to be measured as close to the device under test as possible, and performed in a manner which introduces minimal effect on the test environment.

2.1.13 field-effect mobility: In units of $cm^2/V{\cdot}s$, majority carrier mobility of semiconductor material derived through transfer curve measurement of fabricated device. The field effect mobility is usually derived from either saturation or linear approximations.

2.1.14 force voltage: Voltage source that is supplied by the instrument in order to bias a particular electrode.

2.1.15 gate: Device electrode to which a voltage is applied in order to control the current flow through the semiconducting channel between the source and drain.

2.1.16 gate leakage: Undesirable current flow from the gate electrode through the gate dielectric and organic semiconductor to the source and drain electrodes.

2.1.17 ground chuck: Conductive platform on which the device under test is placed. The ground chuck is electrically referenced to system ground.

2.1.18 I_{DS}: The current flow measured through the drain electrode.

2.1.19 I_{GS}: The current flow measured through the gate electrode. *See also:* **leakage current**.

2.1.20 leakage current: Current flow through the gate dielectric; synonymous with I_{GS}. *See also*: $\boldsymbol{I_{GS}}$.

2.1.21 on/off ratio: The maximum ("on") I_{DS} value divided by the minimum ("off") I_{DS} value, obtained from a transfer (I_{DS} vs. V_{GS}) measurement. This ratio characterizes the ability of the device to switch a signal "on" and "off."

2.1.22 output curve: I_{DS} vs. V_{DS} for a fixed V_{GS}. *See also:* **characteristic**.

2.1.23 semiconductor channel: Space between the source and drain electrodes through the semiconductor material. The electrical conductivity of the channel is controlled by changing the voltage applied to the gate electrode.

2.1.24 source: Device electrode whose current flow is controlled by the conductivity of the semiconducting channel. All voltages within the device are typically referenced to the voltage at the source electrode.

2.1.25 stray capacitance: Any undesirable interlayer or interfacial capacitance within the device. These typically impede device performance and are a likely source of measurement errors.

2.1.26 subthreshold swing: The maximum slope of the log(I_D) vs. V_{GS} curve in the subthreshold regime.

2.1.27 system ground: Zero voltage reference or "LO" connection to instrument. Typically isolated from earth ground.

2.1.28 threshold voltage: Minimum gate voltage required to induce the channel. This value is obtained from a transfer (I_{DS} vs. V_{GS}) measurement.

2.1.29 top-contact device: A field-effect transistor structure where the source and drain electrodes are located further from the substrate than the semiconductor.

2.1.30 top-gate device: A field-effect transistor structure where the semiconducting channel is closer (or adjacent) to the substrate than the gate electrode. Typically, the gate electrode is the last device element deposited when fabricating a top-gate device structure.

2.1.31 transconductance (g_m): The slope of the transfer curve, expressed as

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$$

2.1.32 transfer curve: Measurement for which the drain current is measured as the gate voltage is swept from a start voltage to a stop voltage in increments of a step voltage. *See also:* **transconductance**.

2.1.33 transport property: Physical property of a material or device that governs the behavior of an electrical charge passing through it.

2.1.34 turn-on voltage: The voltage at which strong accumulation occurs for normally "off" devices or strong inversion occurs for normally "on" devices. As all known organic transistors do not operate in the inversion regime, this term should *not* be used when describing organic transistor behavior.

2.1.35 V_{DS}: The voltage measured between the drain electrode and the source electrode.

2.1.36 V_{GS}: The voltage measured between the gate electrode and the source electrode.

2.1.37 V_{SS}: The voltage at the source electrode referenced to system ground.

2.2 Acronyms and abbreviations

EMI	electromagnetic interference
FET	field effect transistor
IEEE	Institute of Electrical and Electronics Engineers
NIST	National Institute of Standards and Technology
OET	organic electronic technology
OFET	organic field-effect transistor
OST	organic semiconductor technology
PFET	polymer field-effect transistor
RFI	radiofrequency interference
RH	relative humidity
UV	ultraviolet

3. Standard OFET characterization procedures

3.1 Device structures

The device structure used for characterization is to be reported, including general device geometry, electrode placement, etc. At a minimum, the following geometrical information is to be reported:

- Relation of gate electrode to substrate (e.g., bottom-gate or top-gate)
- Relation of source and drain electrode to semiconductor and dielectric (e.g., top-contact or bottom-contact)
- Channel length and channel width (in μm or mm)
- Dielectric thickness (in Å, nm, or μm)

The following information for device fabrication is to be reported:

- Substrate composition
- Deposition process of organic semiconductor (e.g., vacuum deposition, spin-coating, jetting)
- Deposition process of dielectric

— Deposition process of electrodes

Any surface treatment between deposition steps, including chemical, interfacial agents to promote ordering (such as octadecyltrichlorosilane between dielectric and semiconductor), mechanical (e.g., brushing to promote ordering), or any other enhancements used.

3.2 Guidelines for the OFET characterization process

Table 1, Table 2, and Table 3 show examples of electrical settings used for electrical characterization of OFET devices. Note that these values are shown as a general guideline, and may vary significantly due to variations in device properties. Settings are to be chosen so that:

— Step size is small enough to give a minimum of 10 data points per curve. Twenty-five or more points are recommended. Increased number of data points results in more accurate curve fitting and greater noise/outlier tolerance, and therefore more accurate parameter extraction. The number of points used for each measurement is reported in some clear fashion (e.g., start, stop, and step values; number of points measured).

— Gate voltage values for V_{DS} vs. I_{DS} measurements are chosen to give a minimum of three curves. Five or more curves are recommended. Values for gate voltage are to reflect the full expected operating range and/or demonstrate full device operating range.

— Minimum dwell time is 10 ms, but 100 ms or more is strongly recommended for each data point. Required dwell time is dependent on factors such as device and instrument impedance values, field-effect mobility, etc., and is selected sufficiently long so that transient effects do not affect measurement significantly (<5% of steady-state minimum, <1% recommended).

— Range of chosen values accurately represents full device operating range. These values are chosen so that device behavior is shown for the full expected operating range.

One probe is used per electrode (gate, source, and drain), plus one shielded ground chuck connection that is in electrical contact with the substrate (“bulk”). If the measured resistance for any channel is less than 1 kΩ, two probes per electrode (one “force” electrode for current application, one “sense” electrode for voltage measurement) are used to minimize electrode and interfacial impedance errors.

Note that OFET response may not be stable over time. See 3.3.2 for more information on device instability.

Table 1—Example measurement settings, p-channel devices (all values in volts)

Measurement type	V_{DS} start	V_{DS} stop	V_{DS} step	V_{DS} bias	V_{GS} start	V_{GS} stop	V_{GS} step	V_{SS} bias	Bulk
I_{GS} vs. V_{GS}	—	—	—	0	+20	–80	–1	0	0
I_{DS} vs. V_{DS}, #1	+20	–80	–1	—	–60	+20	+5	0	0
I_{DS} vs. V_{DS}, #2	–80	+20	+1	—	+20	–60	–5	0	0
I_{DS} vs. V_{DS}, #1	—	—	—	–1	+20	–80	–1	0	0
I_{DS} vs. V_{DS}, #2	—	—	—	–1	–80	+20	+1	0	0
I_{DS} vs. V_{DS}, #3	—	—	—	–40	+20	–80	–1	0	0
I_{DS} vs. V_{DS}, #4	—	—	—	–40	–80	+20	+1	0	0
I_{DS} vs. V_{DS}, #5	—	—	—	–60	+20	–80	–1	0	0
I_{DS} vs. V_{DS}, #6	—	—	—	–60	–80	+20	+1	0	0

Table 2— Example measurement settings, n-channel devices (all values in volts)

Measurement type	V_{DS} start	V_{DS} stop	V_{DS} step	V_{DS} bias	V_{GS} start	V_{GS} stop	V_{GS} step	V_{SS} bias	Bulk
I_{GS} vs. V_{GS}	—	—	—	0	–20	+80	+1	0	0
I_{DS} vs. V_{DS}, #1	–20	+80	+1	—	+60	–20	–5	0	0
I_{DS} vs. V_{DS}, #2	+80	–20	–1	—	–20	+60	+5	0	0
I_{DS} vs. V_{DS}, #1	—	—	—	+1	–20	+80	+1	0	0
I_{DS} vs. V_{DS}, #2	—	—	—	+1	+80	–20	–1	0	0
I_{DS} vs. V_{DS}, #3	—	—	—	+40	–20	+80	+1	0	0
I_{DS} vs. V_{DS}, #4	—	—	—	+40	+80	–20	–1	0	0
I_{DS} vs. V_{DS}, #5	—	—	—	+60	–20	+80	+1	0	0
I_{DS} vs. V_{DS}, #6	—	—	—	+60	+80	–20	–1	0	0

Table 3—Stray capacitance settings, all devices

Measurement type	V_{Bias}	f_{Bias1} (primary)	f_{Bias2}	f_{Bias3}	f_{Bias4}	f_{Bias5}	f_{Bias6}	f_{Bias7}
C_{GD}	1V	1 kHz	100 Hz	2 kHz	5 kHz	10 kHz	50 kHz	100 kHz
C_{GS}	1V	1 kHz	100 Hz	2 kHz	5 kHz	10 kHz	50 kHz	100 kHz

3.3 Electrical standards

3.3.1 Reasons for and results from each measurement type

3.3.1.1 Transfer measurements

Transfer (I_{DS} vs. V_{GS}) measurements are necessary for the characterization of field-effect mobility, threshold voltage, and on/off ratio. These data are typically necessary for characterization of the semiconductor transport properties. Transconductance is also derived from this measurement. Circuit models also generally require at least one transfer curve in addition to the *I* versus *V* output data for parameter extraction.

3.3.1.2 *I* vs *V* output measurement

I versus *V* output (I_{DS} vs. V_{DS}) curves provide the most data on device performance from a single measurement. While not generally of direct use for characterization of the semiconductor transport properties, it is necessary for the development of device models for circuit simulation and design.

3.3.1.3 Gate leakage measurement and its effect on drain current

Gate leakage (I_{GS} vs. V_{GS}) measurements are necessary to ensure sufficient electrical isolation required between the gate electrode and semiconductor channel for useful device operation. This measurement provides data on leakage currents that might interfere with transistor performance. This measurement requires that both the drain and source electrodes are grounded ($V_{DS} = V_{SS} = 0$V). V_{GS} is then swept while I_{GS} is measured. Ideally, zero current flow should be measured from the gate to the channel, but in practical devices, I_{GS} should be sufficiently lower than I_{DS} while the device is in operation, i.e., $I_{GS} < 0.001 I_{DS}$.

To ensure that leakage current does not significantly offset the measured drain current value, the following shall be performed:

— The gate leakage shall be measured over the full range of gate voltages expected in operation and used for transfer curve and *I* versus *V* output measurements.

— The magnitude of gate leakage current shall be at minimum two orders of magnitude less than the magnitude of the drain current through the entire range of device operation, except in the range of gate voltages where the device is considered in the “off” state.

— For significant leakage current (gate leakage exceeding 1% of drain current), transfer and *I* vs. *V* output measurements and any parameters extracted will have significant error, and may continue to accurately fit device models for parameter extraction. If data is to be reported with significant leakage, electrical measurement data may be reported as long as complete gate leakage data are also included. However, extracted parameters that are dependent on the magnitude of drain current (such as device mobility) shall not be reported.

— In the case of parameter extraction, such as curve fitting of transfer data for the extraction of device mobility and threshold voltage, the allowable number of significant figures that may be reported is bounded by how many orders of magnitude the gate leakage is below the magnitude of the drain current.

NOTE 1—Significant gate leakage can result in artificially large values for device mobility without significantly noticeable error in curve fitting or parameter extraction. Although significant gate leakage may manifest itself in reduction of on/off ratio, situations are known to exist where the measured on/off ratio will not be noticeably affected, such as nonlinear gate leakage resulting in stray Schottky contacts or other nonlinear effects.

NOTE 2—The guideline on determination of allowable significant figures is only an upper bound on the total allowable number of significant figures used for reporting, and may be further reduced by other factors, such as measurement noise, quality of curve fit, etc.

3.3.2 Bias stress effects and other directionally-dependent phenomena

Due to stray capacitance effects, potential bias stress phenomena, mobile ionic impurities, or other mechanisms, the direction of voltage bias stepping (i.e., towards more positive values versus more negative values) has been shown to give slightly different electrical data. The results of these phenomena can range from simple shifts of the threshold voltage to severe deviations from ideal transistor behavior, such as an apparent gate voltage-dependent mobility or a lack of a saturation region in an output curve. The determination of parameters that are derived from current-voltage curves, such as the field-effect mobility and threshold voltage, can be strongly affected by these phenomena. In order to determine the severity of hysteresis resulting from the above effects, it is recommended to:

— Perform each measurement twice, first from “off” (the voltage range at which the device is most likely off) to “on.” A second measurement is performed from the “on” state to the “off” state.

— Devices are to sit idle, unbiased (preferably with all three terminals grounded through a low-impedance path to system ground) for a recommended minimum of 10 min before any measurement. This is to minimize both long-lifetime electro-optical effects when the device is

inserted into the measurement system, and stray capacitance-charging effects from previous measurements.

— Characterize the stray capacitance values using at least one frequency using a force voltage of 1 Vrms. If only one frequency is to be used, stray capacitance is characterized at 1 kHz. Other recommended frequency values are listed in Table 3.

3.3.3 Problems with slow polarization of dielectrics

Dielectrics can be polarizable or for other reasons have large dispersion over the frequency range of interest. It is possible that slow polarization of the gate dielectric can affect the accuracy of charge mobility measurements in organic transistors. This polarization can lead to an increase of the charge induced in the semiconductor and therefore an overestimate of the mobility. In many circumstances this extra charge is not accounted for in the determination of the gate capacitance per unit area (C_i) because measurements of the dielectric constant or capacitance are obtained using frequencies of 50 Hz to 1 kHz. The measurement of the current output of the device, from which the mobility is calculated, can take several minutes to obtain, hence the capacitance and mobility are measured in two very different regimes.

Generally, the capacitance will be calculated by measuring the dielectric thickness and using a quoted value of the dielectric constant (which is determined at a chosen frequency, typically 1 kHz) or by directly measuring the capacitance (typically using frequencies of 50 Hz or above). However, transistor characterization is often performed over a period of ~100 s and hence in a very different frequency regime. Slow polarization effects may be present on these larger timescales but not at 50 Hz. Therefore, some idea of the frequency dependence of the dielectric constant is useful to avoid incorrect mobility measurements.

— One method of performing these measurements is to use an impedance analyzer to investigate the low frequency impedance of these types of polymers. However, care must be taken to replicate the composition of layers found in the transistor so as to account for any potential interface effects (e.g., injection barriers, doping of layers) that may have an effect upon the movement of charge within these layers.

— An alternative to ac impedance analysis is to scan the gate voltage at a much faster rate while performing a transfer measurement and then see whether the mobility has changed at all compared to when the measurement is performed at a longer time scale (e.g., ~100 s). Reducing the scan time can be achieved by altering the integration time and/or using fewer points. While this impairs the accuracy of the measurement, it is possible to tell whether, qualitatively, there are any polarization effects present.

To evaluate the effect of dielectric polarization on the semiconductor it is recommended that one or both of the following tests are used:

— The scan rate of the voltage on the gate of the transistor is set such that measurements of the mobility are made where the total scan time covers a range, e.g., 100 s, 10 s, 1 s. Any strong polarization effects will be seen in the transfer characteristics. In general, the calculated mobility will be higher at the slow scan rate than at the fast scan rate and may cover a smaller gate voltage range, i.e., a sharper peak in the mobility when plotted in the linear regime from the transconductance. Note that this method will only *qualitatively* determine whether there are *strong* polarization effects. The decrease in accuracy of the current measurements for the fast scan will make the mobility measurement less accurate than for the slow one, hence it will not be correct to quantify the effect by this method.

— If dielectric polarization is suspected in the device, then it is possible to quantify this effect using impedance spectroscopy. A sandwich structure is fabricated consisting of the same material layers that are present in the transistor in the same order, and this is connected to a frequency analyzer. A small sinusoidal signal (~0.1V p-p amplitude) is applied across the device and the corresponding

current flow recorded for frequencies that cover a range from the timescale of the slow scan in the transconductance plot to the frequency at which the capacitance per unit area is measured (or the dielectric constant of the material is measured). A comparison can then be made between the dielectric response at these two frequencies and as to whether the effective capacitance may change, resulting in an erroneous mobility measurement.

3.4 Reporting data

3.4.1 Minimum reporting standards

The *minimum* information that is reported with all electrical characterization data is shown in Table 4. Table 5 shows the acceptable variations for reporting dielectric properties. The combinations are such that the other two parameters may be determined by calculation. Reporting these parameters shall follow the terminology, symbol use, and units as shown in Table 4 and Table 5. Environmental test and storage conditions (discussed in 3.5) are also to be reported.

The number of data points used for any curve fitting for parameter extraction shall be disclosed. Additionally, if available, information on the quality of the curve fit shall also be reported (e.g., reliability factor *R*).

Table 4—List of parameters to be reported with all electrical data

Characteristic	Standard symbol	Units
Channel width	W	μm (< 1 mm) mm (≥ 1 mm)
Channel length	L	μm
Dielectric information	*(See Table 5)*	(*See Table 5*)
Device temperature	T	°C or K
Environmental relative humidity	RH	%
Field-effect mobility[a]	μ	$cm^2/V \cdot s$
Threshold voltage[a]	V_T	V
On/off ratio[a]	I_{on}/I_{off}	unitless

*Techniques used to calculate marked parameters are to be reported (*see* 3.4.2, 3.4.3, 3.4.4).

Table 5—Acceptable dielectric information combinations

Option number	Capacitance per unit area (C_i, F/cm^2)	Dielectric thickness (d, μm, or nm)	Relative dielectric constant (unitless, at specified frequency)	Frequency of measurement (Hz)
1	✓	✓	✓	✓
2	✓	✓	—	✓
3	✓	—	✓	✓
4	—	✓	✓	✓

3.4.2 Determination and reporting of device mobility

In order to maximize repeatability, the technique used to extract field-effect mobility values from characterization data shall be reported. The mobility value is reported in units of $cm^2/V \cdot s$, with the majority carrier mobility of semiconductor material derived through transfer curve measurement of a fabricated

device. The field effect mobility is usually derived from either saturation or linear approximations. In the case of saturation, this follows the approximation

$$\left[I_{DS} \approx \frac{W}{2L} C_i \mu (V_{GS} - V_T)^2 \right] \tag{3}$$

typically by finding the slope of $I_{DS}^{1/2}$ vs. V_{GS} (transfer in saturation) and solving for the mobility. In the case of the linear approximation

$$\left[I_{DS} \approx \frac{W}{L} C_i \mu (V_{GS} - V_T) V_{DS} \right] \tag{4}$$

where V_{DS} must be << $(V_{GS}$-$V_T)$, the derivative of the approximation can be equated to the slope of the transfer (taken at a V_{DS} in the linear regime).

In the linear regime, the mobility can be calculated by using the slope of the transfer curve and the differential of Equation (4) [see Equation (5)]. When quoting the field-effect mobility, the value must be taken in the regime where V_{DS} is << $(V_{GS}$–$V_T)$ (for a *p*-type device). If the transistor displays a substantial dependence (greater than 10%) of the mobility upon applied gate voltage then this must be indicated by inclusion of the transfer plot showing the mobility plotted on a secondary axis to the drain current.

$$\mu = \frac{\partial I_{DS}}{\partial V_G} \frac{L}{W C_i V_{DS}} \tag{5}$$

3.4.3 Determination and reporting of on/off ratio

In order to maximize repeatability, the technique used to determine on/off ratio values from characterization data shall be reported. This ratio is generally reported as the ratio of the maximum to the minimum drain current (I_{DS}) values obtained during a transfer measurement. Note that this ratio may be different for different values of V_{DS} used for the transfer measurement. In the literature, the maximum observed on/off ratio is generally reported. The V_{DS} and the device dimensions used to obtain the reported on/off ratio should be disclosed.

3.4.4 Determination and reporting of dielectric constant

The technique used to measure the dielectric constant of the gate insulator can have a significant impact on the value obtained. Consequently, variations in dielectric constant will affect extracted values for device mobility and threshold voltage. Dielectric measurements are typically performed using a parallel-plate capacitance measurement method, where the complex impedance is measured at a specified frequency. The dielectric constant may also be determined as a function of frequency, especially if the dielectric constant value varies significantly with frequency (see 3.3.3 for a more detailed discussion).

At a minimum, the dielectric constant is to be reported along with the frequency at which the value was obtained. Typically, this is 1 kHz. Alternatively, a frequency may be chosen that is sensible for the application of interest. However, since most applications of organic electronics operate at or below 100 Hz, the variation of dielectric constant versus frequency should be reported if the value deviates more than 10% from the reported (i.e., 1 kHz) value. It is highly recommended that a curve of dielectric constant versus frequency be supplied when reporting data.

3.4.5 Reporting of environmental conditions

The environmental conditions present during device storage and characterization shall be reported with all electrical characterization data. Guidelines for environmental monitoring are detailed in 3.5.

3.4.6 Other reportable parameters

Table 6 lists other parameters that can be extracted and reported with electrical data. Reporting these parameters shall follow the terminology, symbol use, and units as shown in Table 6.

Table 6—Other parameters that can be reported with electrical data

Characteristic	Standard symbol	Units
Subthreshold swing	S	V/decade
Transconductance	g_m	S
Loss tangent of gate dielectric	δ	radians or degrees

3.5 Environmental control and standards

Device storage conditions from time of device fabrication to time of measurement are to be reported. Environmental conditions during device storage have been shown to significantly affect device performance. Changes in the storage and characterization environment will result in potentially significant variation in device performance. Therefore, diligent reporting of device storage and characterization environments is necessary for comparing or verifying data.

The environmental conditions driving the measurement should be monitored and recorded for every measurement. Conditions are at a minimum to be recorded at the beginning and at the end of each experiment. However, real-time recording of the environmental conditions repeatedly and recorded with each data point is recommended.

The following environmental conditions must be monitored and recorded:

— Measurement atmosphere (e.g., ambient air, nitrogen environment, vacuum).

— Light illumination conditions and light exposure time (e.g., dark, UV protection). Also include change in lighting conditions, such as length of time sample was placed in dark after light exposure and before electrical measurement.

— Device temperature (measured to a resolution of at least 1 °C or 1 K, 0.1 °C or 0.1 K recommended).

— Relative humidity (RH) (to a resolution of 5% minimum, 1% recommended).

— Measurement duration, time of measurement (in order to assist in evaluating measurement artifacts due to very long-lifetime effects).

Annex A
(informative)
Bibliography

[B1] IEEE 100, *The Authoritative Dictionary of IEEE Standards Terms*, Seventh Edition, New York, Institute of Electrical and Electronics Engineers, Inc.

Annex B
(informative)
IEEE List of Participants

At the time this standard was submitted to the IEEE-SA Standards Board, the Working Group for Electronic and Molecular Electronics had the following membership:

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Paul Brazis, Jr., *Vice Chair*

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