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Nanomanufacturing – Large scale manufacturing for nanoelectronics

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CONTENTS

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NANOMANUFACTURING – LARGE SCALE MANUFACTURING FOR NANOELECTRONICS

FOREWORD

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The text of this standard is based on the following documents:

FDIS	Report on voting
113/271/FDIS	113/280/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The IEC Technical Committee and IEEE Technical Committee have decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

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- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

[1] A list of IEEE participants can be found at the following URL: http://standards.ieee.org/downloads/62659/62659-2015/62659-2015_wg-participants.pdf

INTRODUCTION

In order to fully benefit from the cost, performance, and flexibility of new electronics products manufactured on a large-scale, industries accustomed to the purchase, use, and engineering of continuum materials need to grow to embrace appropriate new practices at the nanoscale. The purpose of this International Standard is to enable the quick, low-risk adoption of nanomaterials into large-scale electronics manufacturing. In addition a best set of common practices for use by semiconductor fabricators will be delineated.

The description of nanomaterials to be incorporated into the electronics process can be described in terms of: composition (material), density, purity, size/dimensions, properties such as electrical characteristics (conductive, non-conductive, and semiconductive), associated media (delivery medium), fabrication, surface functionalization, particle size distribution, surface area, shape, and degree of aggregation and agglomeration, etc.

These standards for the characterization of nanomaterials also provide an opportunity to help ensure consistency in metrics and measurement methods when specifying or producing nanomaterials for electronics applications. This is important when multiple vendors or technology partners are involved.

NANOMANUFACTURING – LARGE SCALE MANUFACTURING FOR NANOELECTRONICS

1 Scope

This International Standard provides a framework for introducing nanoelectronics into large scale, high volume production in semiconductor manufacturing facilities through the incorporation of nanomaterials (e.g. carbon nanotubes, graphene, quantum dots, etc.). Since semiconductor manufacturing facilities need to incorporate practices that maintain high yields, there are very strict requirements for how manufacturing is performed. Nanomaterials represent a potential contaminant in semiconductor manufacturing facilities and need to be introduced in a structured and methodical way.

This International Standard provides steps employed to facilitate the introduction of nanomaterials into the semiconductor manufacturing facilities. This sequence is described below under the areas of raw materials acquisition, materials processing, design, IC fabrication, testing, and end-use. These activities represent the major stages of the supply chain in semiconductor manufacturing facilities.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

None.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
nanoscale
size range from approximately 1 nm to 100 nm

Note 1 to entry: Properties that are not extrapolations from a larger size will typically, but not exclusively, be exhibited in this size range. For such properties the size limits are considered approximate.

Note 2 to entry: The lower limit in this definition (approximately 1 nm) is introduced to avoid single and small groups of atoms from being designated as nano-objects or elements of nanostructures, which might be implied by the absence of a lower limit.

[SOURCE: ISO/TS 80004-1:2010, 2.1]

3.2
nanotechnology
application of scientific knowledge to manipulate and control matter in the **nanoscale** (3.1) in order to make use of size- and structure-dependent properties and phenomena, as distinct from those associated with individual atoms or molecules or with bulk materials

Note 1 to entry: Manipulation and control includes material synthesis.

[SOURCE: ISO/TS 80004-1:2010, 2.3]

3.3
nanoelectronics
electronic devices that incorporate **nanoscale** (3.1) materials, processes and properties

3.4
nanomanufacturing
intentional synthesis, generation or control of **nanomaterials** (3.6), or fabrication steps in the **nanoscale** (3.1), for commercial purposes

[SOURCE: ISO/TS 80004-1:2010, 2.11]

3.4.1
bottom-up nanomanufacturing
processes that use small fundamental units to create larger functionally rich structures or assemblies

3.4.2
hybrid nanomanufacturing
combination of additive and subtractive controlled processing to create an intentional nanoscaled structure

3.4.3
top-down nanomanufacturing
processes that create structures at the nanoscale from macroscopic designs

3.5
nanomanufacturing process
ensemble of activities to intentionally synthesize, generate or control **nanomaterials** (3.6), or fabrication steps in the **nanoscale** (3.1)

[SOURCE: ISO/TS 80004-1:2010, 2.12]

3.6
nanomaterial
material with any external dimension in the nanoscale or having internal or surface structure in the **nanoscale** (3.1)

Note 1 to entry: This generic term is inclusive of nano-objec**t** and nanostructured material.

[SOURCE: ISO/TS 80004-1:2010, 2.4]

3.7
nano-object
material with one, two or three external dimensions in the **nanoscale** (3.1)

Note 1 to entry: Generic term for all discrete nanoscale objects.

[SOURCE: ISO/TS 80004-1:2010, 2.5]

3.8
nanostructure
composition of inter-related constituent parts, in which one or more of those parts is a **nanoscale** (3.1) region

Note 1 to entry: A region is defined by a boundary representing a discontinuity in properties.

[SOURCE: ISO/TS 80004-1:2010, 2.6]

3.9
nanofibre
nano-object (3.7) with two similar external dimensions in the **nanoscale** (3.1) and the third dimension significantly larger

Note 1 to entry: A nanofibre can be flexible or rigid.

Note 2 to entry: The two similar external dimensions are considered to differ in size by less than three times and the significantly larger external dimension is considered to differ from the other two by more than three times.

Note 3 to entry: The largest external dimension is not necessarily in the nanoscale.

[SOURCE: ISO/TS 27687:2008, 4.3]

3.10
nanoparticle
nano-object (3.7) with all three external dimensions in the **nanoscale** (3.1)

Note 1 to entry: If the lengths of the longest to the shortest axes of the nano-object differ significantly (typically by more than three times), the terms nanofibre or nanoplate are intended to be used instead of the term nanoparticle.

[SOURCE: ISO/TS 27687:2008, 4.1]

3.11
nanowire
electrically conducting or semi-conducting **nanofibre** (3.9)

[SOURCE: ISO/TS 27687:2008, 4.6]

3.12
nanosheet
freestanding nanofilm

3.13
graphene
single layer of carbon atoms with each atom bound to three neighbours in a honeycomb structure

Note 1 to entry: It is an important building block of many carbon nano-objects.

[SOURCE: ISO/TS 80004-3:2010, 2.11]

3.14
nanotube
hollow **nanofibre** (3.9)

[SOURCE: ISO/TS 27687-2008, 4.4]

3.15
nanorod
solid **nanofibre** (3.9)

[SOURCE: ISO/TS 27687-2008, 4.5]

4 Abbreviations

The following abbreviations are used in this standard:

CNT – Carbon nanotube

HDL – Hardware description language

ATE – Automatic test equipment

5 Nanomaterials incorporation into electronics fabrication

5.1 General

Nanomanufacturing processes follow three general methods of production: bottom-up nanomanufacturing, top-down manufacturing and a hybrid version of these two methods, each based on the location of the initiating material. See Figure 1.

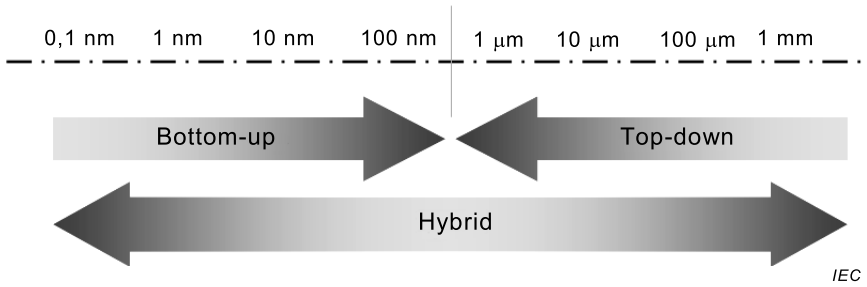

Figure 1 – Relationship between bottom-up, top-down and hybrid device fabrication processes for nanoelectronics over length scales

Tables 1 and 2 describe representative workflows for the creation of nanoelectronics within the two most common manufacturing processes. Incorporation of nanomaterials into electronics fabrication may utilize a hybrid process in which creation of nanoelectronics employs a combination of elements of both of these workflows.

Table 1 – Bottom-up process for nanoelectronics

Workflow	Processing
Desired pattern defined using lithographic technique	Desired pattern developed in seed planting software tool to produce the seed positions
Functionalized surface	Seed layer is produced on substrate layer
Functional surface generation and growth	The desired pattern described by functional surface allows seeds to grow and assemble. Additive raw material grown from functionalized surface
Completed pattern	Finished device

Table 2 – Top-down process for nanoelectronics

Workflow	Activity
Raw material coating of substrate	Material added to substrate
Desired pattern defined using lithographic technique	Desired pattern developed
Pattern etched	The desired pattern described by lithographic process and excess material selectively removed; patterning and etching repeated as necessary
Completed pattern	Finished device

A workflow for nanomaterials incorporation into electronics fabrication is highlighted in Table 3, comparing a CNT electronics workflow to that of a CMOS workflow.

Table 3 – Comparison of CMOS processes with exemplary CNT electronics process

Workflow	CNT electronics	Si CMOS electronics
Raw materials acquisition	CNT in grams	Wolframite/Sheelite (Tungsten ore) in metric tonnes
Materials processing	CNT in 1 L or 4 L aqueous solutions	150 mm, 200 mm or 300 mm W targets for sputter deposition
Design	Full custom layout;	Multi-core microprocessor synthesized from HDL;
IC fabrication	0,15 µm CMOS line	45 nm, 200 mm wafer Si CMOS foundry
Testing	Semi-automatic wafer probe stations	High throughput ATE
End-use	Solid-state data recorder module	Mainboard with chipset for notebook computers

The primary areas for elucidation to move from start to product include: raw materials, processed materials, IC fabrication processes, design and test and end-user systems. Each area has specific requirements and function which has dependencies based upon the end-user system requirements. This document will provide a framework for the elucidation of generic approaches to describe these systems with the goal to coalesce with other standards activities wherever a common thread or shared methodology can be exploited.

5.2 Raw materials acquisition

Raw materials use for nanoelectronics at the large scale falls into four primary categories: nanoparticles, nanowires, nanotubes and nanosheets, which may include zero-dimensional nanomaterials, one-dimensional nanomaterials, two-dimensional nanomaterials or three-dimensional nanomaterials, either separately or in combination or as a mixture. Nanotubes are distinct from nanowires because of the hollow nature of a tubular structural motif versus the solid form of a wire. Several IEC and IEEE efforts, for example IEC 62624/IEEE Std 1650 and IEC PAS 62565-2-1, have focused on delineation of various aspects of nanotube generation and description. Those efforts will be incorporated as references for this effort.

Some of the key features of raw carbon nanotube materials examination include sourcing, growth conditions including gas control, temperature control, substrate choice and control, diameter (and chirality) control, length control, surface functionalization, contamination measurement from catalysts in the case of nanotubes and additional carbon contamination as well. These are detailed in IEC PAS 62565-2-1.

In the case of nanoparticles the synthesis methodologies are quite diverse and the focus will be on monodispersity, composition control, surface functionalization and contamination.

In the case of nanowires, the synthesis will focus on methods which specify gas concentrations, temperature control, substrate choices, diameter control, length control, surface functionalization and contamination. All of these raw materials generation methodologies require close examination of safety conditions during growth, harvesting safety and waste stream handling and monitoring. IEC PAS 62565-1 shall be the model for the future nanowire blank detail specification.

In the case of nanosheets, the synthesis will focus on providing monatomically layered carbon atoms with a specified stacking of one or more layers. Controlled growth will focus on methods which specify gas concentrations, temperature control, substrate choices, and contamination.

5.3 Materials processing

The concept of processing nanomaterials for use in CMOS is relatively new. Indeed nanomaterials can be grown or self-assembled directly on substrates without significant purification. In the case that direct growth is not preferable, solutions of nanomaterials are necessary and must be prepared in a proper manner for use in CMOS. Density/distribution of nanotubes in solution is a factor relating to metrics, purity and performance. Particular attention must be paid to the areas of removal of contaminants especially metals such as iron, nickel and cobalt. Type sourcing of nanomaterials, either by diameter in the case of nanotubes or nanowires or via monodispersity in the case of nanoparticles, is likely a necessary condition for work to proceed in a fabrication environment. Specific issues to be addressed regarding waste streams including waste from purifications, solvents and cleaning protocols are important. Processes shall comply with applicable environmental regulations.

5.4 Design

Standard design such as those for integrated circuits is appropriate whenever possible using nanomaterials. Design of nanoscale devices that exploit quantum effects is still being developed as theoretical and empirical advances generate more detailed understanding of these properties.

5.5 Fabrication

Fabrication processes using nanomaterials are evolving. In order to fabricate devices even with purified or processed nanomaterials, care must be taken to comply with standard guidelines, protocols and procedures common to the semiconductor industry. Special attention to cleanliness, waste disposal and subsequent processing and compliance with established industry standards and practices, including those described in the ISO 14644 and ISO 14698 series of cleanroom standards, are critical.

For example, handling of wafers with modern robotics is a necessity and can only be accomplished by ensuring that substrates are cleaned to the degree necessary not to contaminate modern robotics handlers. Other fabrication processes such as deposition, patterning, and etching need to conform to standard processes. Care must be taken to guarantee that the nanomaterials are neither destroyed nor act as contaminants.

5.6 Test

Test methods such as those for integrated circuits are appropriate whenever possible using nanomaterials. In many cases function-based testing of devices and nanostructures is achievable using existing techniques. Test of nanoscale devices that exploit quantum effects are still being developed as theoretical and empirical advances generate more detailed understanding of these properties. Nanoscale metrology capabilities are currently being developed along with nanoscale lithography, and in many cases these will be appropriate for other nanostructures.

5.7 End-use

It is necessary for inputs and outputs from nanoelectronics to conform to standard ranges typical in the electronics industry. Various protocols and standards are already in place which should be utilized in their entirety. Waste streams and end of life practices should be adhered to as is the case for standard integrated circuits.

6 Safety and environmental issues

Safety and safe handling of nanomaterials certainly pertains to this emerging technology, just as safe handling and processing/disposal of hazardous materials are considerations in the current semiconductor process. Standards and regulations are currently evolving and in some cases may not yet be identified. Precautionary safety practices should always be the guide until specific standards can be developed.

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