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Edition 1.0 2014-02

TECHNICAL SPECIFICATION

colour inside

Process management for avionics – Aerospace and defence electronic systems containing lead-free solder –
Part 3: Performance testing for systems containing lead-free solder and finishes

IEC TS 62647-3:2014-02(en)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE AND DEFENCE ELECTRONIC SYSTEMS CONTAINING LEAD-FREE SOLDER –

Part 3: Performance testing for systems containing lead-free solder and finishes

FOREWORD

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- the required support cannot be obtained for the publication of an International Standard, despite repeated efforts, or
- the subject is still under technical development or where, for any other reason, there is the future but no immediate possibility of an agreement on an International Standard.

Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC/TS 62647-3, which is a technical specification, has been prepared by IEC technical committee 107: Process management for avionics.

The text of this technical specification is based on the following documents: IEC/PAS 62647-3 and GEIA-STD-0005-3.

This technical specification cancels and replaces IEC/PAS 62647-3, published in 2011. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) Terms and definition subclause changed in Clause 3.
b) Coherence with IEC/TS 62647-1, IEC/TS 62647-21 and IEC/TS 62647-22 definitions.
c) Introduction of “g-force” definition.
d) Reference to IEC 62647 documents when already published.
e) Harmonization of preconditioning data at Table B.1 level with regard to 5.3.3.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
107/213/DTS	107/233/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62647 series, published under the general title *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

The implementation of lead-free (Pb-free) interconnection technology into electronics has resulted in a variety of reactions by designers, manufacturers, and users. While the prime motivation for lead-free (Pb-free) technology was to address the social concern of improving the environment by limiting the amount of toxic and dangerous substances used in products, the ramifications of this initiative have provided a state of uncertainty regarding the performance – in this context, defined as operation and reliability, i.e. the expected life cycle of a product – of aerospace and defence systems. For over fifty years, tin-lead solder was the benchmark for electronics assembly and generations of research baselined its performance under a variety of operating conditions including the harsh settings of aerospace and defence equipment. However, with the integration of lead-free (Pb-free) technology, aerospace and defence companies are faced with questions as to whether these new materials will provide, as a minimum, the same degree of confidence during the life cycle of critical systems and products.

In evaluating performance, two approaches are used: analysis/modelling and test. This document addresses the latter, providing guidance and direction in the development and execution of performance tests for lead-free (Pb-free) electronic interconnections. The user of this document needs to be aware of the following: This document does not give answers as to how to perform a specific test. Products and systems applications vary immensely, so designers need to understand use conditions and the entire life cycle. Once this is understood, then this document can be used to give designers an understanding of how to develop a suitable test, e.g., ascertain the type of platform in which a product will be used, comprehending all the environmental effects on the platform, and learning why material characterization is key to deciding upon test parameters, etc.

Sound engineering knowledge and judgment will be required for the successful use of this document.

The global transition to lead-free (Pb-free) electronics has a significant impact on the electronics industry; it is especially disruptive to aerospace, defence and other industries that produce electronic equipment for high performance applications. These applications, hereinafter described as ADHP (Aerospace, Defence and High Performance), are characterized by severe or harsh operating environments, long service lifetimes, and high consequences of failure. In many cases, ADHP electronics need to be repairable at the soldered assembly level. Typically, ADHP industry production volumes may be low and, due to low market share, may not be able to resist the change to lead-free (Pb-free). Furthermore, the reliability tests conducted by suppliers of solder materials, components, and sub-assemblies cannot be assumed to assure reliability in ADHP applications. This document provides guidance (and in some cases direction) to designers, manufacturers, and maintainers of ADHP electronics in assessing performance of lead-free (Pb-free) interconnections.

Over the past several decades, electronics manufacturers have developed methods to conduct and interpret results from reliability tests for lead-bearing solder alloys. Since these alloys have been used almost universally in all segments of the electronics industry, and since a large body of data, knowledge, and experience has been assembled, the reliability tests for Pb-bearing solder alloys are well-understood and widely accepted.

When it became apparent that the use of Pb-bearing alloys would decline rapidly, programs were implemented to evaluate the reliability of the lead-free (Pb-free) replacement alloys. Those programs have generated a considerable database. To date, however, there is no reliability test method that is widely accepted in the ADHP industries. Reasons for this include:

a) No single lead-free (Pb-free) solder alloy has emerged as a replacement for lead-bearing alloys; instead, a number of alloys are being used in various segments of the electronics industry.

b) The physical, chemical, and metallurgical properties of the various lead-free (Pb-free) replacement alloys vary significantly.

c) Due to the many sources of solder alloys used in electronic component termination materials or finishes, assembly processes, and repair processes, the potential number of combinations of alloy compositions is nearly unlimited. It is an enormous task to collect data for all these combinations.

d) The test methods developed by other segments: the IPC-9701A and IPC/JEDEC-9703 are directed toward shorter service lives and more benign environments. Also, there is still a question of suitable dwell times and acceleration factors. However, the intent of this document is to provide a means of coordinating the information from the IPC-9701A and IPC/JEDEC-9703 into a basic approach for ADHP suppliers.

e) The data from reliability tests that have been conducted are subject to a variety of interpretations.

In view of the above facts, it would be desirable for high-reliability users of lead-free (Pb-free) solder alloys to wait until a larger body of data has been collected, and methods for conducting reliability tests and interpreting the results have gained wide acceptance for high-reliability products. In the long run, this will indeed occur. However, the transition to lead-free (Pb-free) solder is well under way and there is an urgent need for a reliability test method, or set of methods, based on industry consensus. While acknowledging the uncertainties mentioned above, this document provides necessary information for designing and conducting performance tests for aerospace products. In addition, when developing test approaches, the material in question needs to be suitably characterized. Such material properties as ultimate tensile strength, yield strength, Poisson's ratio, creep rate, and stress relaxation have been shown to be key attributes in evaluating fatigue characteristics of lead-free (Pb-free) solders.

Because of the dynamic nature of the transition to lead-free (Pb-free) electronics, this and other similar documents are based on the best information and expertise available; its update will be considered as future knowledge and data are obtained.

PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE AND DEFENCE ELECTRONIC SYSTEMS CONTAINING LEAD-FREE SOLDER –

Part 3: Performance testing for systems containing lead-free solder and finishes

1 Scope

This part of the IEC 62647 series defines for circuit card assemblies (CCA):

– a default method for those companies that require a pre-defined approach, and

– a protocol for those companies that wish to develop their own test methods.

The intent of this document is not to prescribe a certain method, but to aid avionics/defence suppliers in satisfying the reliability and/or performance requirements of IEC/TS 62647-1 as well as support the expectations in IEC/TS 62647-21.

The default method (see Clause 5) is intended for use by electronic equipment manufacturers, repair facilities, or programs that, for a variety of reasons, may be unable to develop methods specific to their own products and applications. It should be used when little or no other information is available to define, conduct, and interpret results from reliability, qualification, or other tests for electronic equipment containing lead-free (Pb-free) solder. The default method is intended to be conservative, i.e., it is biased toward minimizing the risk to users of ADHP electronic equipment.

The protocol (see Clause 6) is intended for use by manufacturers or repair facilities that have the necessary resources to design and conduct reliability, qualification, or process development tests that are specific to their products, their operating conditions, and their applications. Users of the protocol will have the necessary knowledge, experience, and data to customize their own methods for designing, conducting, and interpreting results from the data. Key to developing a protocol is a firm understanding of all material properties for the lead-free (Pb-free) material in question as well as knowledge of package- and board-level attributes as described in 5.3.2. As an example, research has shown that the mechanisms for creep can be different between tin-lead and tin-silver-copper (SAC) solders. Understanding these mechanisms is key to determining critical test parameters such as dwell time for thermal cycling. The protocol portion of this document provides guidance on performing sufficient characterization of new materials in order to accurately define test parameters.

Use of the protocol is encouraged, since it is likely to yield more accurate results, and to be less expensive than the default method. The IEC/TS 62647-22 provides a comprehensive overview of those technical considerations necessary in implementing a test protocol.

This specification addresses the evaluation of failure mechanisms, through performance testing, expected in electronic products containing lead-free (Pb-free) solder. One failure mode, fatigue-failure through the solder-joint, is considered a primary failure mode in ADHP electronics and can be understood in terms of physics of failure and life-projections. Understanding all of the potential failure modes caused by lead-free (Pb-free) solder of ADHP electronics is a critical element in defining early field-failures/reliability issues. Grouping of different failure modes may result in incorrect and/or misleading test conclusions. Failure analysis efforts should be conducted to insure that individual failure modes are identified, thus enabling the correct application of reliability assessments and life-projection efforts.

When properly used, the methods or protocol defined in this specification can be used along with the processes documented in compliance to the IPC-SM-785, to satisfy, at least in part, the reliability requirements of the IPC-SM-785 and JESD22-B110A.

Any portion of this document can be used to develop a lead-free (Pb-free) assembly test program, i.e., this document is tailorable and provides room for flexibility. For those situations in which results are used for reliability, verification, or qualification, stakeholder concurrence needs to be sought and documented so that expectations are understood and addressed.

This specification may be used for products in all stages of the transition to lead-free (Pb-free) solder, including:

- products that have been designed and qualified with traditional tin-lead electronic components, materials, and assembly processes, and are being re-qualified with use of lead-free (Pb-free) components;
- products with tin-lead designs transitioning to lead-free (Pb-free) solder; and
- products newly-designed with lead-free (Pb-free) solder.

For programs that were designed with tin-lead solder, and are currently not using any lead-free (Pb-free) solder, the traditional methods may be used. It is important, however, for those programs to have processes in place to maintain the tin-lead configuration including those outsourced or manufactured by subcontractors.

With respect to products as mentioned above, the methods presented in this document are intended to be applied at the level of assembly at which soldering occurs, i.e., circuit card assembly (CCA) level.

This document may be used by other high-performance and high-reliability industries, at their discretion.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC/TS 62647-22:2013, *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 22: Technical guidelines*

IPC-9701A:2006, *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*

IPC-SM-785, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*

JESD22-B110A, *Subassembly Mechanical Shock*

MIL-STD-810G:2008, *Environmental Engineering Considerations and Laboratory Tests*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1.1
coupon
test sample representing a scaled-down or proportional version of an actual product or higher level test vehicle

3.1.2
CTE
coefficient of thermal expansion
degree of expansion of a material divided by the change in temperature

Note 1 to entry: PCB/PWB CTE (X-Y-axis) is measured in the direction in the plane of the piece part mounting surface and is used to quantify the stresses in the solder joint arising from the differences in CTE between the piece parts and the PCB/PWB during thermal cycling. CTE (Z-axis) is measured in the "thickness" direction and is typically used to quantify plated through hole stress.

[SOURCE: IEC/TS 62647-22:2013, 3.1.8]

3.1.3
g-force
force per unit mass that can be measured with an accelerometer and perceived as weight (with "g" from "gravitational")

Note 1 to entry: Since such a force is perceived as a weight, any g-force can be described as a "weight per unit mass". g-forces, when multiplied by a mass upon which they act, are associated with a certain type of mechanical force in the correct sense of the term force, and this force produces compressive stress and tensile stress.

3.1.4
lead-free
Pb-free
less than 0,1 % by weight of lead (Pb) in accordance with reduction of hazardous substances(RoHS) guidelines

[SOURCE: IEC/TS 62647-1:2012, 3.8]

3.1.5
PCB
printed circuit board
PWB
printed wiring board
substrate using conductive pathways, tracks or signal traces etched from copper sheets laminated, and allowing to connect electrically un set of electronic components to realize a circuit card.

[SOURCE: IEC/TS 62647-21:2013, 3.1.10]

3.1.6
tin-lead
solder bearing the elements tin and lead, and corresponding to 63% by weight of tin and 37% by weight of lead unless otherwise specified

3.1.7
vehicle
test sample such as a populated circuit card assembly (CCA)

3.2 Abbreviations

ADHP	Aerospace, Defence and High Performance NOTE This refers to a generalized level of equipment used in harsh and stringent operating conditions.

CCA	Circuit card assembly
JCAA	Joint Council of Aging Aircraft (organization within the US Department of Defence that has performed extensive lead-free solder reliability testing)
JG-PP or JGPP	Joint Group on Pollution Prevention (NASA group that began the lead-free solder testing)[1]
PSD	Power spectral density NOTE It describes how the power of a signal or time series is distributed with frequency.
RoHS	Restriction of Hazardous Substances NOTE The RoHS directive is a European directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment

4 Assumption

For the purposes of this document, if the element “lead” is implied, it will be stated either as Pb, as lead (Pb), or as tin-lead.

If a piece part terminal or termination “lead” is referred to, such as in a flat pack or a dual-inline package, the nomenclature lead/terminal or lead-terminal will be used.

5 Default test methods

5.1 General

Use of the default method shall be limited to CCAs. Test coupons may also be used provided the concerns listed in 5.3.2 are considered.

5.2 Test vehicles

5.2.1 Test vehicle type

Test vehicles used in testing of electronic systems containing lead-free solder shall consist of soldered assemblies that are representative of the materials and processes used in the assembly and/or repair procedures used by the ADHP electronics manufacturer or repair facility. Characterization and documentation of the test vehicle attributes (both design and manufacturing) is recommended. Test vehicle attribute documentation shall include, at a minimum, the following data:

- board type, material, size, finish, thickness, copper content
- piece-part material, package size, package type, termination finish
- assembly solder alloy
- assembly processes including fluxes and cleaners
- thermal management materials
- underfill and staking materials
- other mechanically attached structures

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1 JGPP Pb-free solder testing was completed with the support of JCAA.

- environmental coatings
- repair history/process (including solder alloys)

The utilization of electrically functional assemblies/units or representative test vehicles is permitted provided full characterization of the electronic assembly materials, test vehicle configuration, and assembly processes are documented. IPC-9701A:2006, 4.2, contains additional guidance on the characterization and documentation for test vehicles.

Test coupons may be used but the user is cautioned that various attributes of concern can be different at coupon level, i.e., cool down rates, metallurgy, pitch, others. If the use of coupons is desired, the user shall perform an analysis to determine if such attribute differences exist. If differences are determined, the user shall mitigate associated risks. Be aware that results are based upon the processes used and that complete documentation of the processes is necessary if this document is being used to evaluate the processes.

5.2.2 Sample size

The number of test vehicles shall be based on a statistically based sample size and analysis plan. Accordingly, several options are available. IPC-9701A specifies a minimum number of 33 test samples. However, sample sizes can be smaller or larger depending upon usage conditions. Annex A provides additional insight into sample size selection.

5.3 Pre-conditioning by thermal aging method

5.3.1 General

Lead-free solder properties tend to change over time even under typical storage conditions. So test programs shall include some preconditioning exposure before the primary environments (e.g., temperature cycling, vibration, mechanical shock) to replicate these changes for the lifetime; IPC-9701A contains some guidance. Isothermal elevated temperature aging can accelerate these changes, such as grain growth, intermetallic compound growth, diffusion-driven voids, segregation, and oxidation. Such preconditioning can also help gain consistency among test articles by driving the grain structures to similar characteristics. The isothermal aging method may not cause changes representative of all particular application environments and processing conditions (curing bake, burn-in, environmental stress screening, field use and storage, etc.), so the test protocol and test result interpretation should account for this effect, and different time/temperature combinations may be required for different programs. In addition, the test protocol may need to include other preconditioning environments to assess all the effects pertinent to a particular application.

5.3.2 Thermal aging acceleration model

The default acceleration model which allows the tailoring of the basic isothermal aging preconditioning exposure follows the Arrhenius formulation:

$$AF = \exp\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\frac{E_a}{k} \quad (1)$$

where

AF is the acceleration factor (dimensionless),

T_1 is the test temperature in K (in the default case, 100 °C, or 373,15 K),

T_2 is the application temperature,

E_a is the activation energy (eV), and

k is Boltzmann's constant ($8{,}620 \times 10^{-5}$) eV/K.

For most metallics, E_a typically is 0,9 to 1,0. However, use of measured results, i.e., actual test data, is encouraged when available.

NOTE E_a is based on specific material properties.

Each mechanism, i.e., grain growth, intermetallic compound growth, etc., may have its own E_a and a summation of E_a should be used by either test or analysis.

Isothermal aging may be used as a preconditioning process prior to mechanical vibration and shock qualification testing. Specific details are beyond the scope of this document.

Other models may be used as appropriate.

5.3.3 Default test parameters

The isothermal aging of assembled test vehicles should consist of 100 °C for 24 hours. These isothermal aging parameters will not represent all applications, so the preconditioning exposure should be tailored as necessary to meet the goals of a particular test program.

5.4 Default temperature cycle test method

5.4.1 Test parameters

The temperature cycle test parameters, test temperature ranges, and thermal cycle test duration shall be in accordance with IPC-9701A:2006, 3.4.3, 5.1 and 5.2. Test monitoring requirements shall be in accordance with IPC-9701A:2006, Table 4-4. The default test temperatures shall be –55 °C to 125 °C and the duration shall be minimum 1 000 cycles. The ramp shall be less than 20 °C/minute and the dwell time shall be 15 minutes minimum. The CCA shall reach the temperature for the dwell time duration as defined in IPC-9701A. Ramp rates, other than those specified here may be used but only if material characterization or data supports a change. Refer to 6.4 of this specification.

NOTE The –55 °C lower limit is selected based on defence requirements (e.g., performance, storage, etc.). However, if the user is interested in determining the acceleration factor at this temperature, he can consider the behavioural factors. Refer to the second paragraph of 6.3.1. Accordingly, the use of –55 °C readily accommodates a “go/no-go” type test, i.e., straight performance test.

5.4.2 Test duration

The number of temperature cycles (or duration) shall be sufficient enough to evaluate the expected performance of the samples in the required applications. Continuing the test to complete failure, or to $>$ 75 % failure of all samples is recommended in order to obtain proper statistical metrics.

In most cases, 1 000 cycles may be sufficient. A 1 000 cycles is considered a standard duration for many companies/organizations. However, Table 4-1 of IPC-9701A:2006 provides additional guidance for duration values.

NOTE Subclause 5.4.4 of this document, provides further information about the number of temperature cycles and their interpretation with respect to service life.

5.4.3 Failure determination and analysis

Failure determination can be performed by either of two methods.

One method is to define and monitor failure per the daisy-chain monitoring method as described in IPC-9701A:2006, 4.3.3. Implementation of this method requires the manufacture of special-purpose assemblies constructed from special-purpose test components and test boards. This method is therefore not generally applicable to standard functional hardware.

The second method is to monitor electrical performance of functioning CCAs continuously during the test.

For each of these two methods, the test monitoring and failure criteria shall be fully documented.

Traditionally, for tin-lead solder, a third method has occasionally been used, i.e., failure analysis via optical criteria. For lead-free solders, this method is not recommended. The failure modes of most lead-free solders, as known at this time, would render the optical approach useless since the cracks tend to be extremely small and cannot be reliably discerned against the naturally frosty and fissured surface of lead-free solder.

Failure analysis shall be performed in accordance with the test plan, on a minimum of three components per test board type. Typical candidates for failure analysis include: early failures and failures that fall near the statistical fit, and failures that deviate from the statistical fit.

Techniques for failure analysis may include methods such as "dye and pry" or cross-sectioning, as appropriate for the components in question. Failure modes shall be documented. The most important information to be obtained from the failure analysis is whether or not the failure is associated with the solder interconnection, or whether it relates to the package or board, or some other non-solder related failure. Beyond this, failure analysis should also provide information on where solder joint failures occur (within the bulk solder or at the intermetallic layer or interface). Results may also distinguish between fracture modes within the solder. Grouping of different failure modes may result in incorrect and/or misleading test conclusions. Failure analysis efforts should be conducted to insure that individual failure modes are identified and characterized to avoid the confounding of statistical analyses.

Statistical analysis of the test sample failure data shall be completed in accordance with the test sample and analysis plan. The completed statistical analysis shall be included in the test documentation. The A 2-parameter Weibull plot is preferred but only if this can provide a good fit to the experimental data.

5.4.4 Acceleration model

While this document is not meant for use exclusively for reliability testing, 5.4.4 is presented for information.

The default general form of the acceleration model for temperature cycle testing is:

$$AF = \left(\frac{\Delta T_1}{\Delta T_2} \right)^c \tag{2}$$

where;

AF is the acceleration factor,

ΔT_1 is the temperature cycle range in test (in the default case, 165 °C, other values have to be agreed),

ΔT_2 is the application temperature range,

c is the exponent (fatigue ductility exponent) and is material and package dependent; it includes dependency leaded versus leadless configurations.

Additional possible dependencies are discussed in the Note.

For many lead-free materials, many parameters have not yet been characterized. Many references are available which discuss the fatigue ductility exponent. It is the responsibility of the user to choose the applicable value. Examples for presently documented values for the

fatigue ductility are in Annex B. It provides a short subset of such references. Annex B also provides properties (e.g., acceleration test parameters, fatigue ductility exponents, etc.) for presently known materials but the user should be aware that "c" is not yet known for many lead-free materials.

This basic model assumes that there are no significant differences between the test vehicle and the in-use application except for the temperature differential or that differences between test conditions and in-use conditions do not have a significant effect on the acceleration factor.

If there are significant differences other than temperature differentials, additional correction factors to Equation (2) may be required depending on the solder material being used. Factors that have been identified as modifying the basic acceleration factor equation or the value of c, for some solder materials, include but are not limited to:

- dwell times at temperature,
- component packages including die dimensional characteristics,
- PCB / PWB attachment designs (pad dimensions),
- solder thickness,
- PCB / PWB thermo-mechanical characteristics (CTE, stiffness, thickness, etc.),
- thermal ramp rates,
- coating material,
- coating application methods.

An AF model supported by the literature for the specific material being used should be selected and applied within literature supported limits to predict the application performance of a material from known performance under known conditions. Annex B includes an example of test-to-application and product characteristics for SAC 305 that modifies the basic acceleration factor equation.

NOTE The following is an example of application of the basic AF equation.

i) Determine a value of c for the material being used from the literature. In this example, a value of 3,0 will be assumed.

ii) Determine the temperature range of the application. In this case a temperature cycle from 25 °C (room temperature) to 95 °C will be assumed. The differential is 70 °C.

iii) Confirm that there are no other modifying characteristics that are significant. In this case the test vehicle is identical to the unit to enter service and is comprised of one package type of integrated circuit. The ramp rates and dwell times are identical between test and application. For this example, it is assumed that there are no significant differences between the test conditions and the application conditions.

iv) Using the test temperature differential, assume 165 °C in this case, compute the AF. In this case the AF is $(165/70)^3$=13,1.

v) Determine the number of thermal cycles in-use for the desired design life. In this case assume one cycle per day.

vi) Compute the equivalent life demonstrated by test. In this case where one cycle per day is assumed, survival for 1 000 test cycles is equivalent to 1 000 × 13,1 = 13 100 cycles, or 13 100 days of use. This is equivalent to 13 100/365 = 35,9 years of use.

As there are many research projects still running investigations of the acceleration model and the material specific parameters, Annex B will be updated at each release of the document. The user of this document is recommended to observe this trend.

5.5 Vibration test

In deciding upon a vibration test, the designer will need to determine the purpose of the test and how the test data will be utilized. If accelerated testing is of interest, IPC-SM-785 shall be used. For a wider range of stress levels (e.g., design verification), MIL-STD-810G shall be used. If there is a conflict between any of the cited standards requirements and those of the

specific product or system requirements, the user shall conduct an analysis to determine which of the two is most beneficial (conservative) and proceed accordingly.

In all cases, samples shall be pre-conditioned in accordance with 5.3.

5.6 Mechanical shock

In deciding upon a mechanical shock test, the designer will need to determine the purpose of the test and how the test data will be utilized. If accelerated testing is of interest, IPC-SM-785 shall be used. For moderate levels of shock, JESD22-B110A shall be used. For a wider range of stress levels (e.g. design verification), MIL-STD-810G shall be used. If there is a conflict between any of the cited standards requirements and those of the specific product or system requirements, the user shall conduct an analysis to determine which of the two is most beneficial (conservative) and proceed accordingly. In addition, IPC/JEDEC-9703, as an informational reference, provides further insight into tailoring a shock test.

In all cases, samples shall be pre-conditioned in accordance with 5.3.

5.7 Combined environments

Since combined environmental testing is a relatively new concept in performance testing, no default approach exists at the present time. Subclause 6.6 provides information and possible approaches as part of a protocol effort in characterizing new materials. The user may refer to 6.6 for insight on such testing.

6 Protocol to design and conduct performance tests

6.1 General

In order to conservatively assess the as-designed equipment performance, one would need to know the failure rate of a soldered joint at the end of equipment life and for a typical accumulated environmental experience. This is for each ‘specific solder - board passivation - piece part terminal finishing’ combination being used within that equipment and takes into account the different component package types/styles and silicon (die) to package ratio (package size such as chip scale). Subsequently, Clause 6 contains information on accelerated aging of lead-free interconnections that facilitates confirmation that the performance of any equipment under test is representative of that equipment at the end of its design lifetime.

NOTE Aerospace and military applications can result in conditions of

- cyclic high rates of change of temperature, long dwell times, and high vibration, or
- continuous medium temperatures (for several years at a time) with a requirement to withstand occasional high mechanical shock.

An important function of this protocol is to make the user aware that different dwell times and ramp rates, influenced by solder type, material mix, substrate characteristic, and component type, will produce different results. In other words, solder (or other interconnection materials) will require sufficient characterization (material properties) prior to executing performance tests. For example, SAC 305 solder has been characterized in the industry and the data shows different stress relaxation/creep response times than that for eutectic tin-lead solder. Thus, for newer, unknown materials, robust testing of materials properties should be conducted to acquire relevant properties to address specific concerns, e.g., reliability models of interest.

Users should be cautioned that use of bulk test samples may not be representative of material behaviour in an interconnection configuration. When at all possible, actual soldered test vehicles should be considered for accurate results.

6.2 Test vehicles

The requirements shall be the same as those in 5.2.1.

6.3 Temperature cycle test protocol

6.3.1 General

This test protocol is based on the following assumptions:

- the acceleration model is a form of the inverse power law;
- temperature cycling is the appropriate stress method;
- high-temperature and low-temperature dwell times (t_{hd}) are critical parameters of the time-temperature cycle [13][2];
- sufficient low temperature limit is –40 °C or –55 °C depending upon contract requirement; the user should note that this limit can be different especially for new materials if characterization indicates that stress relaxation changes significantly at a lower temperature;
- the ramp rate shall be less than 20 °C/minute. A slower ramp rate can be used if characterization data indicates that stress relaxation is not affected. The user is also directed to IPC-9701A for further implications in using a slower ramp rate;
- the dwell time t_{hd} should exceed the recovery time (t_r) for a given alloy, or combination of alloys. A shorter t_{hd} may be used if the user provides documentation relative to the effect of shorter t_{hd} on cyclic damage, and hence, on the acceleration factor.

One issue with using –55 °C for the low temperature limit is that less creep occurs at low temperature, so the assessment of the acceleration factor with most models now in use treats a 15 °C delta at low temperature the same as a 15 °C delta at high temperature. The effect is that one could assume a greater acceleration factor for the majority of the application environment (centered at approximately 25 °C) than should be taken. On the other hand, colder temperatures can induce greater stress in the solder joint that may initiate a crack. Current industry experience suggests that the basic guidance used on Sn-Pb solder probably applies here: Accelerate most of the fatigue through temperature ranges most likely to be encountered in use; address the cold temperature limits (below approximately –20 °C for Sn-Pb) with additional cycles to the cold limit of the application. In some cases, a compromise approach may be taken and –40 °C can be selected as the lower temperature limit (even if the –55 °C limit applies) for accelerated durability testing. To address ultimate strength issues, typical systems tests (i.e., MIL-STD-810G) can be used since contractors and program offices usually prefer a simple test protocol (i.e., one temperature cycle profile).

Users of this specification may develop temperature cycle tests based on modifications of the above assumptions, provided those modifications are based on credible, documented, and conclusive data related to their own products.

The steps described in 6.3.2 through 6.3.7 shall be followed in developing lead-free solder performance tests.

6.3.2 Measure the recovery time

During thermal cycling, elastic strain energy is converted to and dissipated as creep work by the creep process, thus increasing the cyclic damage [14]. The timeframe during which this occurs is usually known as “recovery time” but it is best described as “stress relaxation time” or “creep process time.” Hereon, this time will be called “stress relaxation time”.

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2 Numbers in square brackets refer to the Bibliography.

The stress relaxation times, t_r, for all alloys, and combinations thereof, that are used in the manufacturer or repair facility's products shall be determined over a range of temperatures that include the high temperature limits of the temperature cycle test. See Figure 1.

The specific methods, parameters, and results of these measurements shall be documented for all solder alloys, and combinations thereof.

Figure 1 shows a notional method for accomplishing this requirement. If the method illustrated in Figure 1 cannot be verified, then the applicable methods used shall be defined and documented.

NOTE The purpose of this test is to ensure that the high-temperature dwell time is long enough for mechanical stresses to be relieved in the alloys being tested.

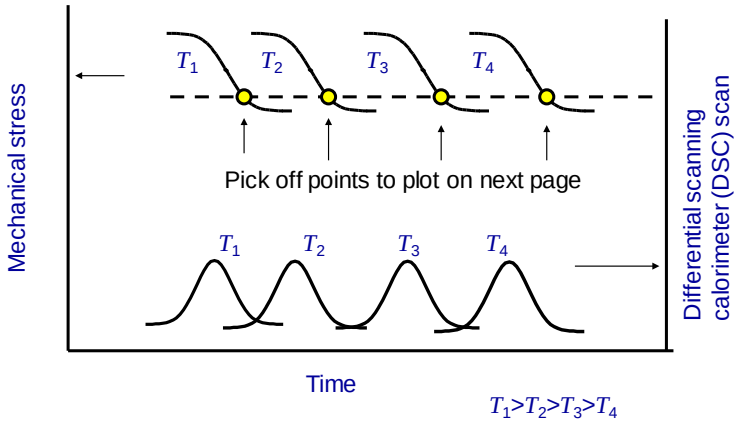


Figure 1 – Notional method for determining the recovery time for a given solder alloy, or combination of alloys

The steps in this method are:

1) Select samples representative of the alloys and combinations to be tested. The samples do not necessarily have to be elements of electronic components.
2) Apply stresses to produce defined amounts of strain in the selected samples.
3) Measure t_r, which is the time required for the samples to recover to a defined minimum stress level, e.g., 90 % of the stresses are relieved, over a range of temperatures. Various methods of measuring t_r may be used; illustrated above are mechanical and thermal measurements.

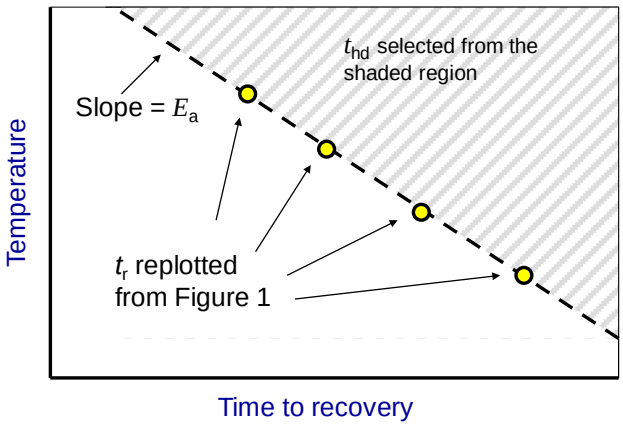
It is expected that the specific methods and parameters will be selected for each given application.

6.3.3 Determine the high-temperature dwell times and temperatures

The high temperature dwell times, t_{hd}, for all alloys and combinations thereof, for the given high temperature limit of the temperature cycle test shall be determined for each upper temperature limit, on the basis of the data collected from 6.3.2.

The specific methods, parameters, and results of these determinations shall be documented for all solder alloys, and combinations thereof.

Figure 2 shows a notional method for accomplishing this requirement. The relationship illustrated in Figure 2 should be verified for all alloys, and combinations thereof. If it cannot be verified, the applicable relationship shall be verified and used.



NOTE This example assumes an idealized system but the slope can differ depending on material, temperature range, and dwell time.

Figure 2 – Notional method for determining the relationship between high temperature dwell time, t_{hd}, and recovery time, t_r

The above example is based on the assumption that this relationship is governed by an Arrhenius relationship of the form:

$$t_r = \mathrm{A}\ \exp(-E_a/kT) \tag{3}$$

where t_r is recovery time, A is the proportionality constant, T is the temperature, E_a is the activation energy, and k is Boltzmann's constant.

6.3.4 Select other test parameters as appropriate for the application

Other temperature cycle test parameters shall be selected and documented for all pertinent solder alloys and combinations thereof.

Since t_{hd} is considered to be the critical parameter for this type of test, the default values in 5.4.1 may be used for the lower temperature limit and dwell time, and temperature ramp rate. Alternately, other parameters may be used, provided that they are documented.

6.3.5 Conduct tests

Temperature cycle tests shall be conducted, using the parameters determined in 6.3. The observed failures shall be analysed to verify that they are due to temperature cycling stresses.

6.3.6 Determine the temperature versus cycles-to-failure relationship

The relationship between the cycles-to-failure and the temperature cycling range shall be determined and documented for all alloys, and combinations thereof.

Figure 3 shows a notional method to accomplish this requirement. It illustrates an S-N curve based on the inverse power law, which is used to determine the exponent of Equation (4). If this relationship cannot be verified, the applicable relationship shall be determined and documented.

NOTE The S of S-N curve stands for "stress"; that means repetitive load. N stands for "number of cycles-to-failure".

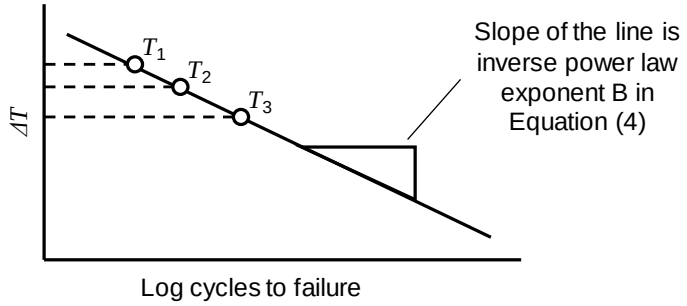


Figure 3 – Cycles-to-failure – Notional method for determining the relationship between cycles-to-failure

The notional method shown in Figure 3 is based on the following equation:

$$N_{\text{ff}} = N_{\text{ft}}\left(\frac{\Delta T_{\text{t}}}{\Delta T_{\text{u}}}\right)^{B} \tag{4}$$

where

N_{ff} is the cycles-to-failure in actual use (field) conditions,

N_{ft} is the cycles-to-failure for test,

T_{t} is the temperature at test, and

T_{u} is the temperature during actual use.

6.3.7 Estimate the cycles-to-failure

The relationship determined in 6.3.2 through 6.3.6 above shall be used to estimate the cycles-to-failure of the given solder alloys, and combinations thereof, for the given applications.

6.4 Vibration test

6.4.1 General

For vibration test methods, the user can refer to 5.5. However, prior to selecting a method, the user shall review the information provided in the three paragraphs below for additional insight on method selection.

Typical operational environments can take sustained time to accrue high cycle fatigue failure. Excessive vibration levels at the CCA level can introduce secondary failure modes that would not be encountered during normal life. If, after reviewing the suggested methods in 5.5, the user feels this is the case, then further analysis may be necessary. For example a finite element analysis of the board can be performed to establish expected limits or determine use of a step stress test approach. Should the results show excessive component termination stress or if board level deflection exceeds prudent design limits, then test design should be exercised with caution, especially if accelerated life testing is intended.

Regarding fatigue, equivalent damage and less test time can be realized by raising test levels. This relationship is a nonlinear factor. A simplified fatigue relationship to determine time at test levels versus operational limits should be used. This is equivalent to the vibration fatigue life limit or service life. It is recommended that the lowest vibration level that will meet test duration time be used and that the test duration may need to be adjusted when defining the test level.

MIL-STD-810G:2008, Method 514.6, Annex A, paragraph 2.2, has been used to determine test level and test time to satisfy fatigue life requirements. Equation (5) provides the relationship using the inverse power law:

$$(W_0/W_1) = (T_1/T_0)^{1/m} \quad (5)$$

where

W is the vibration level (PSD),

T is the time to achieve high cycle fatigue failure,

$1/m$ is the material constant (slope of the log/log S-N curve),

and W_0 and T_0 are established by material characterization.

Supplier data frequently provides this information.

6.5 Mechanical shock

For mechanical shock test methods, the user is referred to 5.6. However, prior to selecting a method, the user shall review the information provided in the paragraph below for additional insight on method selection.

With all solder alloys, the formation of intermetallic compounds (IMCs) due to recombination during the solder processes and solid state diffusion will occur. With lead-free solder, many of these compounds demonstrate a much more brittle characteristic, forming a ductile/brittle interface. The majority of failures of a lead-free solder joint due to shock has been along this IMC interface. A simplified relationship between the two interface materials is used to determine the acceleration of crack propagation along the IMC interface. The impact of multiple shocks has not been provided since it is not considered a dominant environment and it is recommended that operational profiles should be considered when considering the frequency or number of impulses.

Equation (6) provides a shock relationship using again the inverse power law:

$$AF = (\varepsilon_s/\varepsilon_a)^{1/2} \quad (6)$$

where

AF is the acceleration factor,

ε_a is Young's modulus for the intermetallics,

ε_s is Young's modulus for the solder alloy.

6.6 Combined environments test protocol

6.6.1 General

The term combined environments test has been coined to indicate a concern that a product will experience more than one environmental condition during its life cycle. Some popular approaches have been to combine thermal cycling with vibration. However, one needs to understand the complete life cycle of a product in terms of what kinds of environments it will see during its operating life as well as during storage or other down-time situations. Once all conditions are identified, then the designer needs to determine which of those conditions would exert a stress, the magnitude of the stress, and the percentage of time that the stress is present (e.g. duty cycle) on the product. Since thermal cycle, vibration, and mechanical shock are three sources that influence crack propagation, the scope of this document will be limited to these three environments.

If one looks at environmental effects, a prediction of damage can then be evaluated using openly available models such as Miner's Cumulative Damage Law [6, 7, 8] as expressed in Equation (7):

$$D = \sum_{i=1}^{k} (n_i / N_i) \quad (7)$$

where

i is the number of environmental conditions (effects),

n_i is the number of cycles at the i^{th} effect;

N_i is the total number of all effects cycles (lifetime) for the product.

The quantity D is the total damage (sum of all effects) and is experimentally found to be between 0,7 and 2,2 although usually, for design purposes, D is assumed to be 1.

With Miner's Law, the approach would be to add the effects (damage) of each stress (environmental condition) over the life cycle of the product.

$$D = n_{\text{thermal cycle}}/N_{\text{thermal cycle}} + n_{\text{vibration}}/N_{\text{vibration}} + n_{\text{mech shock}}/N_{\text{mech shock}} + \ldots\ldots + n_i/N_i \quad (8)$$

Where each term represents that component of damage attributable to the stress condition cited and "i" is the i^{th} stress or environmental condition.

Combined environmental testing provides the closest approximation of what performance capability a solder joint of a given alloy can achieve.

The total damage accuracy can be improved by considering weighting factors for each stress effect notionally expressed by Equation (9):

$$D = \sum_{i=1}^{k} [W(n_i / N_i)]D \quad (9)$$

where

W is the weighting factor (not to be confused with the vibration level variables shown in 6.4).

Since it is critical that the environmental profile match that of the design or system application, the weighting factor can be used to tailor the test. Because the thermal cycle temperature limits and dwell time are fixed, the test duration, vibration environment, and shock environment should be tailored.

Classically, shock environmental testing has used 20 g_{rms}. Pulse duration has varied from 9 ms to 20 ms depending on operational application. This environment should be adjusted if a greater g-level is seen in the actual use environment (such as missile launch, which can be as high as 100 g_{rms}) or if shock is a greater driving factor in the low cycle fatigue failure (such as a ground vehicle in off-road applications). The frequency and number of total shock pulses should be a factor tailored as part of the overall environmental profile. The vibration environment remains to be defined. Test time duration and the g-force for a given solder alloy should be evaluated. The combination of these three environments (thermal cycle, vibration, and shock) should be tailored such that the total destructive force is great enough to result in failure of the test article starting in the second half of the test and preferably 100 % of all test articles fail at the end of the duration of the test. As a minimum, 63 % of the population should fail during the testing if properly designed. This will allow standard chi square statistical methods to be used to predict the solder joint failure rate and the AF of the test environment.

The total damage of the combination of all environments can be greater than the sum of the individual environments as indicated in Miner's Law. However, at this time this factor is assumed to be 1 until further testing can be performed to demonstrate this relationship with some degree of confidence.

6.6.2 Combined environment relation

Recalling Equations (2), (5), and (6), Miner's Law can be expressed to determine the cumulative damage based on contributions from each environment that contributes to the failure. Each of the environment's acceleration factor (AF) is weighted by the percentage each environment contributes to the total destructive force. By weighting the acceleration factors with an operational profile, a close approximation of the combined test environment is established.

Reminder of Equations (2), (5) and (6):

$$(\Delta T_t/\Delta T_u)^C = (AF)_1 \tag{10}$$

$$(W_0/W_1) = (T_1/T_0)^{1/m} = (AF)_2 \tag{11}$$

$$AF = (\varepsilon_s/\varepsilon_a)^{1/2} = (AF)_3 \tag{12}$$

Equation (13) expresses the estimated acceleration factor for the combined test environment:

$$AF_{(\text{combined environment})} = (A \times (AF)_1) + (B \times (AF)_2) + (C \times (AF)_3) \tag{13}$$

where

A is the weighted factor (as a %) of what the temperature cycles contributes to the destructive force;

B is the weighted factor (as a %) of what the vibration contributes to the destructive force;

C is the weighted factor (as a %) of what the shock contributes to the destructive force.

The board resonant frequency (f_n) or the first mode is used to calculate the time required to accumulate the number of cycles for high cycle fatigue (T_0). Using the operating weighting factor (B), multiply the vibration high cycle fatigue to calculate the number of cycles required for the accelerated life test. Calculate the time required to accumulate the weighted number of cycles (T_1). Insert the time into Equation (11) and calculate for the g-force needed to accumulate the equivalent destructive force necessary for the combined environment.

Vibration should be evenly distributed over the entire test duration. Total time to perform this test is reduced.

6.6.3 Additional insight: NASA-DoD lead-free project

The objectives of combined environment tests can vary. As an example, the NASA-DoD lead-free project [5, 10], initiated in 2007, was deployed to augment lead-free performance data from the preceding effort, the Joint Council on Aging Aircraft (JCAA) JG-PP lead-free (Pb-free) project [9]. In the NASA-DoD effort, the objectives are:

- Determine the reliability of reworked solder joints in high-reliability defence and aerospace electronics assemblies.
- Assess the process parameters for reworking high-reliability lead-free defence and aerospace electronics assemblies.
- Develop baseline recommendations for process guideline and risk assessment for assembling high-reliability lead-free defence and aerospace electronics assemblies.

This project includes thermal cycle, vibration, mechanical shock, and a combined environment test that is comprised of thermal cycle and vibration in separate actions, not truly combined. Annex C contains information from this test effort. The designers are encouraged to review Annex C and use its information at their discretion.

The user has to keep the following in mind: The NASA-DoD project is provided as an example only. The project was designed to exceed the normal anticipated environments to provide failure data as quickly as possible. Each program should evaluate the protocols and determine if the profiles presented can be used to predict failures in their environments.

6.6.4 Additional insight: concept of life cycle in accordance with MIL-STD-810G

Earlier in 6.6.1, the concept of life cycle was discussed as an approach to identifying those environmental conditions that contribute to the overall stress or effects experienced by a product. MIL-STD-810G introduces the crucial necessity of tailoring the test requirements to the application requirements (i.e., life cycle environmental profile). This then allows one to specify a MIL-STD-810G test method and appropriate application specific criteria to define the proper test. The user should be aware that one weakness in the vibration method is that it identifies the fatigue exponent as a constant value, when in reality it varies with material and structure properties. Thus analysis and/or testing is required to determine the value of the exponent.

The user is encouraged to review Section 4 and Annex C of MIL-STD-810G:2008 for additional information on typical use histories for various military/aerospace platforms as well as climatic conditions.

6.7 Failure determination and analysis

Regarding any failure analysis activity following a protocol study, refer to the direction and information provided in 5.4.3.

7 Final remarks

This specification was developed with an overall focus of providing value to the user. It was generated thanks to the inputs of a global team involved in the aerospace/defence industry and sensitive to the performance challenges in maintaining customer confidence. Lead-free technology poses many challenges and potential risks and, since testing is a key approach to answering these concerns, a dedicated effort has produced this resource document to provide information, guidance, and some requirements to facilitate an appropriate test program. As lead-free research continues, the knowledge base of materials and interactions will increase leading to subsequent revision of this specification. For this release, the specification has focused on the importance of material characterization with emphasis on effects in thermal cycling. However, suitable information has been related on vibration, mechanical shock and combined environments.

The key to effective use of this document is the flexibility to allow tailoring to address specific product and program conditions. Again, when employing the tailoring option, the only requirement is that there shall be concurrence among all stakeholders and that the concurrence shall be documented.

The value of this document will be realized by the effective planning and execution of the user.

Annex A
(informative)

Test sample size

In this discussion, "F_{xx}" numbers refer to the percentage of the sample size, or, in an application, the number of the population of parts that have failed; i.e., F_{50} refers to the point in life where 50 % of the individuals in the sample or population have failed. F_{01} refers to the point where 0,01 % of the sample or population has failed, etc. Obviously, with a small sample size like 10, the F_{01} point for a population cannot be measured directly, since the first failure in this sample size would be at the F_{10} point, but should be estimated by statistical analysis. The F_{63} point (63 % of population or sample has failed) is commonly used as a standard metric in wear-out discussions because this point is directly calculated by Weibull distribution estimation software programs. Weibull estimation is a factor that mathematically determines properties of the Weibull distribution function[3].

Also, in this discussion, sample size refers to the number of components, not the number of solder joints. The first failure of any solder joint of a component is defined as the life of that sample item. The number of solder joints is absolutely not a sample size definition. N = 20 means 20 nominally identical components soldered identically, with identical solder, on identical printed circuit boards (PCBs)/printed wiring boards (PWBs), e.g., the 20 components could all be on the same PCB/PWB, as long as the location (local CTE and side/side warp, for instance) effects are known/incorporated.

A sample size of 33 is often used as a default standard but is not an “absolute” requirement. Smaller samples sizes (N = 20 and even N = 10) can provide useful metrics, to suit the objective, and the resulting precision can be determined up-front, in test planning. Larger sample sizes, N = 50, for instance, will produce more precision in the resultant metrics, especially in early-distribution reliability for products such as heart-implant electronics, and more opportunity for test suspension and/or during-test sample withdrawals, without hampering precision significantly. If $\pm$ 5 % is needed, use N = 50. If $\pm$ 20 % is appropriate, use N = 10. The expected precision of results based on sample size can be calculated up-front by using appropriate statistical techniques. For the proposed test program, N = 20 is recommended as a good balance between precision (typically $\pm <$ 15 % for estimation of the F_{63} point), versus the cost due to the larger required sample size of the experimental program to obtain higher precision of the statistical estimates.

If the objective is to compare A versus B, it is recommended that a central metric (i.e., central to the failure distribution of the population between no failures and 100 % failures) be used, such as the F_{63} or F_{50} failure percentage points. If the objective is to estimate early failure points in the life distribution, such as the $F_{,01}$ or $F_{,001}$ points, use a larger sample size.

It is desirable to allow the test to run until all samples fail. This provides higher confidence levels and precision of the statistical estimates. But suspension (i.e., terminating the test) when 60 % of the parts have failed, to approximately cut the test time in half, will yield metrics with reasonable confidence levels within 5 % to 10 %. If the objective is specification compliance data (i.e., greater than a pre-determined number), recognize that sample size is critical: the greater the sample size, the more likely to encounter failing samples. Again, that can be estimated up-front. For any set of failure data, commonly available Weibull estimating software programs can provide a "most likely" estimate of population life over time and confidence intervals for this estimate.

Without testing to failure, characterizing reliability (or cumulative failure, F_x) requires assuming a failure distribution shape for reliability levels of practical interest in most

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3 Please refer to statistical texts for further discussion of the Weibull distribution.

applications, such as F_{01} and lower. In addition, without data varying stress levels, there should also be an assumption for the test acceleration factor, AF. If reasonable data exists to estimate the acceleration factor, testing of N samples can only estimate reliability levels around $F_{100/N}$, so typical test times to address an application requirement with lifetime T_{life} should exceed $AF \times T_{\text{life}}$. The amount that the test time should exceed this time depends on the failure distribution.

Annex B
(informative)

Material properties of lead-free solder materials

Annex B provides data and information regarding those material properties and test parameters unique to specific lead-free interconnection materials.

For SAC 305:

Given the amount of work already performed in characterizing the SAC 305 (i.e., Sn-3,0Ag-0,5Cu) alloy, Table B.1 below provides test and acceleration model parameters for SAC 305.

Table B.1 – Test and acceleration model parameters

Allowable test temp (°C)	**Allowable test temp** (°C)	**Allowable temp in service** (°C)	**Allowable temp in service** (°C)	**Test dwell time**	***AF* exponential factor**	***AF* exponential factor**	***AF* correct factor for 1 hour plus in service**	**Allowable surface finishes**	**Substrate stabilization points to start dwell periods**	**Pre-conditioning**	***AF***
Maximum	Minimum	Maximum	Minimum	Minutes	Area array devices and leaded devices	SMT 2512 and larger chip devices	As required by application	RoHS compliant only	95 % of temperature delta set points	24 hours at 100 °C	AF + test [temperature delta / in-service temperature delta] x exponential factor
125 °C	–55 °C	125 °C	–40 °C	10,00	2,70	1,50	0,50	X	X	X	Testing below –20 °C may cause premature failure due to non-creep related failure mechanisms

Supplement to Table B.1:

1) Temperature test ranges are limited to –55 °C to +125 °C minimum and maximum.

   The user should be aware that testing below –20 °C can cause premature failure due to non-creep related failure mechanisms. See IPC-SM-785.

2) Dwell times at temperature are 10 minutes after the substrate reaches 95 % of the difference between chamber set points. That is, if the temperature set points are –40 °C and +120 °C, the difference is 160 °C. 5 % of this difference is 8 °C. The substrate should reach 112 °C and –32 °C before the dwell times commence.

3) The acceleration equation power factor is 2,7 for all area array devices and leaded devices and 1,5 for chip resistors or capacitors with form factors of 2 512 or larger. See IPC-9701A:2006.

4) An in-service dwell time factor of 0,5 will be applied for units that experience high temperature in-service dwell periods greater than 1 hour per cycle. See IPC-9701A:2006.

5) A preconditioning period of 24 hours at 100 °C will be applied to the test samples before the test is initiated. [19]

6) This model does not apply for in-service applications above 125 °C or below –40 °C. See IPC-TM-785.

7) RoHS compliant component termination finishes are required for test and in the application. This requirement is imposed to prevent degradation of solder fatigue life due to interaction of SAC and tin lead solders. See JESD22-B110A.

8) Additional worked-out examples are available from workshop proceedings presented by DfR Solutions. Contact DfR Solutions at URL: http://www.dfrsolutions.com.

References for Table B.1:

1) Epidemiological Study on Sn-Ag-Cu Solder: Benchmarking Results from Accelerated Life Testing

Craig Hillman, Nathan Blattau, Ed Dodd, and Joelle Arnold SMTA 2006 Chicago

2) Osterman, Michael, “Strain Range Approximation for Estimating Fatigue Life of Lead-Free Solder Interconnects Under Temperature Cycle Loading”, IPC/JEDEC Global Conference on Lead Free Reliability & Reliability Testing for RoHS Lead Free Electronics, Boston, MA, April 10-11, 2007. (Note: IPC 9701A:2006, 4.3.1 is recommending 24 hours at 100 °C.)

3) Osterman, Michael, “Effect of Temperature Cycle on the Durability Lead-free (Pb-free) Interconnects

(Sn96.5Ag3.0Cu0.5 and SnCuNi)”, University of Maryland Center for Advanced Life-Cycle

Engineering Project C06-06, 2006.

4) Dasgupta, A., “Risk Assessment & Accelerated Qualification of Lead-free (Pb-free) Electronics,” University of Maryland Center for Advanced Life-Cycle Engineering Project C03-05, 2003

References regarding the fatigue ductility exponent:

5) Engelmaier, Werner, *Solder Joints in Electronics: Design for Reliability*, Engelmaier Associates, L.C., Ormand Beach, FL, www.tms.org/Meetings/ Annual-97/Program/Sessions/MA332.html

6) Salmela, Olli, “*Comments on the IPC Surface Mount Attachment Reliability Guidelines*”, quality and Reliability Engineering International, *Qual. Reliab. Engng. Int.* 2005; 21:345–354, published online 10 March 2005 in Wiley InterScience (www.interscience.wiley.com). DOI: 10.1002/qre.667

7) Osterman, M. et. al., “*Effect of Temperature Cycle on the Durability Lead-free (Pb-free) Interconnects (Sn96.5Ag3.0Cu0.5 and SN100C)*”, Report of Project C06-06, CALCE EPSC Fall 2006 Technical Review, University of Maryland Center for Advanced Life-Cycle Engineering, October 17, 2006.

EXAMPLE

Temperature	**Test**	**In-service**	**Test/use**
Low	–40 °C	10 °C	
High	125 °C	80 °C	
Delta	165 °C	70 °C	2,36
Temp ratio test/use	2,36	2,36	
	Area array exponent	**2 512 exponent**	
	2,70	1,50	
AF at 10-minute dwell	10,13	3,62	
AF factor for 1+ hour in-service dwells	0,50	0,50	
AF for 1+ hour in-service dwells	5,06	1,81	
Assume 1 thermal cycle per day at 12-hour dwells (typical commercial aircraft)			
Required 1 % failure in-service cycles	360,00	360,00	1 year in-service at 12-hour dwells
Required 1 % failure test cycles	71,1	198,95	1 year in-service at 12-hour dwells
Required 1 % failure test cycles	1 422,07	3 979,09	20 years in-service at 12-hour dwells

Annex C
(informative)

NASA-DoD lead-free electronics project test information[4]

C.1 General

NOTE At the date of publication, information in Annex C was found at the JG-PP web site.

This NASA-DoD project is provided as an example only. The project was designed to exceed the normal anticipated environments to provide failure data as quickly as possible. Each program should evaluate the protocols and determine whether the profiles presented can be used to predict failures in their environments. The information provided in Annex C is presented as information for use at the user's discretion. The Joint Test Protocol can be found at http://teerm.nasa.gov/nasa_dodleadfreeelectronics_proj2.htm

C.2 Vibration test

C.2.1 General

The following protocol was developed for the 2007 NASA-DoD lead-free electronics project, which was conducted to test the effects that lead-free (Pb-free) finishes on electronics components and various lead-free solders had on the repair and rework processes used by various original equipment manufacturers and DoD repair depots.

C.2.2 Vibration test description

This test was designed to satisfy the general requirements of MIL-STD-810G:2008, Method 514.6 (vibration), and was performed using the following procedure:

- Confirm the electrical continuity of each test channel prior to testing. One channel will be used per component.
- Place the CCAs into a test fixture in random order and mount the test fixture onto an electro-dynamic shaker.
- Conduct a step stress test in the Z-axis only (i.e., perpendicular to the plane of the circuit board). Most failures will occur with displacements applied in the Z-axis as that will result in maximum board bending for each of the major modes.
- Run the test using the stress steps shown in Table C.3. Subject the test vehicles to 8,0 g_{rms} for one hour. Then increase the Z-axis vibration level in 2,0 g_{rms} increments, shaking for one hour per step until the 20,0 g_{rms} level is completed. Then subject the test vehicles to a final one hour of vibration at 28,0 g_{rms}.
- Continuously monitor the electrical continuity of the solder joints during the test using event detectors with shielded cables. All wires used for monitoring will be soldered directly to the test vehicles and then glued to the test vehicles (with stress relief) to minimize wire fatigue during the test.
- If feasible, a complete modal analysis should be conducted on one test vehicle using a laser vibrometer system in order to determine the resonant frequencies and the actual deflection shapes for each mode.

The stakeholders agreed that a stress step test representing increasingly severe vibration environments was appropriate for this test. A step stress test was required since a test

4 Taken from the NASA-DoD lead-free (Pb-free) project's Joint Test Protocol, 19 September 2007.

conducted at a constant 8,0 g_{rms} level would take thousands of hours to fail the same number of components as a step stress test. This is because some locations on a circuit assembly experience very low stresses and severe vibration is required in order to fail components at these locations. The shape of the PSD (power spectral density) curve for each step stress level was designed so that all of the major resonances of the test vehicles would be excited by the random vibration input. The PSD curves (Figure C.1) presented in MIL-STD-810G were used as guides for the creation of this step stress test but were not directly duplicated.

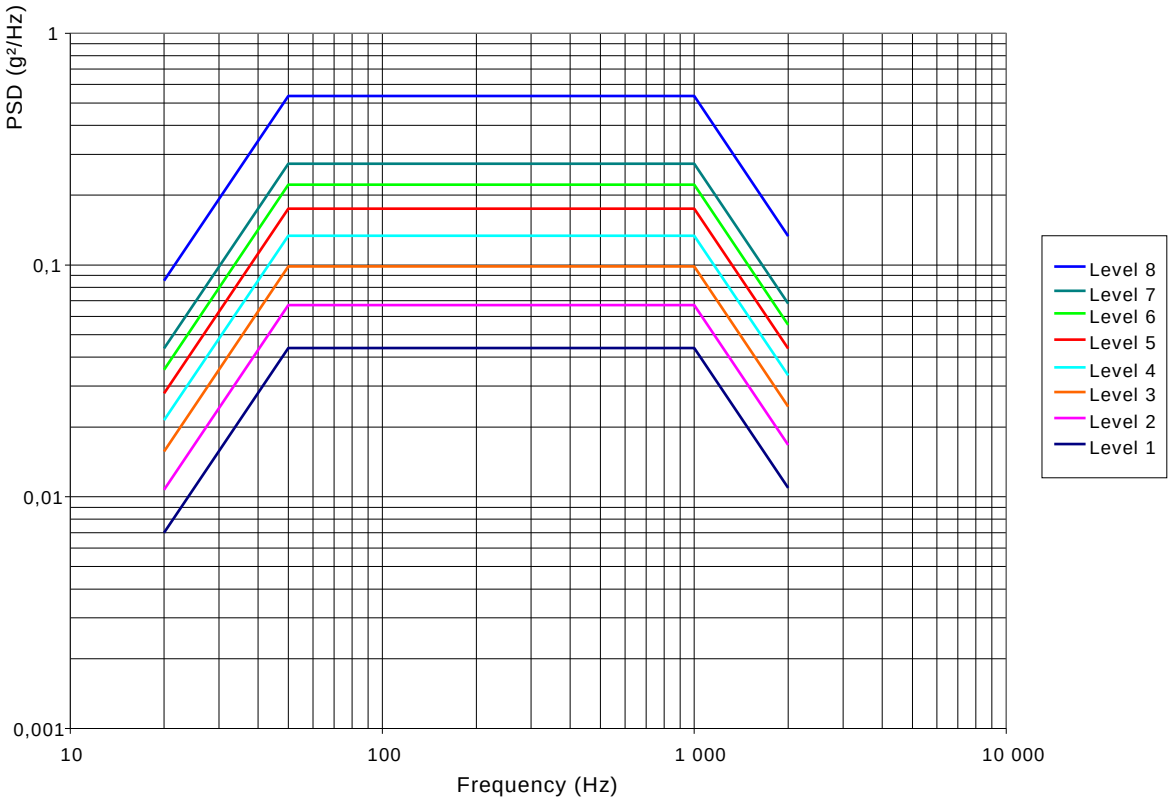

Figure C.1 – Vibration spectrum

Table C.1 describes the different levels' profiles.

Table C.1 – Vibration profile

Level 1	**Level 2**	**Level 3**
20 Hz at 0,00698 g^2/Hz	20 Hz at 0,0107 g^2/Hz	20 Hz at 0,0157 g^2/Hz
20 Hz to 50 Hz at +6,0 dB/octave	20 Hz to 50 Hz at +6,0 dB/octave	20 Hz to 50 Hz at +6,0 dB/octave
50 Hz to 1 000 Hz at 0,0438 g^2/Hz	50 Hz to 1 000 Hz at 0,067 g^2/Hz	50 Hz to 1 000 Hz at 0,0984 g^2/Hz
1 000 Hz to 2 000 Hz at –6,0 dB/octave	1 000 Hz to 2 000 Hz at –6,0 dB/octave	1 000 Hz to 2 000 Hz at –6,0 dB/octave
2 000 Hz at 0,0109 g^2/Hz	2 000 Hz at 0,0167 g^2/Hz	2 000 Hz at 0,0245 g^2/Hz
Composite = 8,0 g_{rms}	**Composite = 9,9 g_{rms}**	**Composite = 12,0 g_{rms}**

Level 4	**Level 5**	**Level 6**
20 Hz at 0,0214 g^2/Hz	20 Hz at 0,0279 g^2/Hz	20 Hz at 0,0354 g^2/Hz
20 Hz to 50 Hz at +6,0 dB/octave	20 Hz to 50 Hz at +6,0 dB/octave	20 Hz to 50 Hz at +6,0 dB/octave

50 Hz to 1 000 Hz at 0,134 g^2/Hz	50 Hz to 1 000 Hz at 0,175 g^2/Hz	50 Hz to 1 000 Hz at 0,2215 g^2/Hz
1 000 Hz to 2 000 Hz at –6,0 dB/octave	1 000 Hz to 2 000 Hz at –6,0 dB/octave	1 000 Hz to 2 000 Hz at –6,0 dB/octave
2 000 Hz at 0,0334 g^2/Hz	2 000 Hz at 0,0436 g^2/Hz	2 000 Hz at 0,0552 g^2/Hz
Composite = 14,0 g_{rms}	**Composite = 16,0 g_{rms}**	**Composite = 18,0 g_{rms}**

Level 7	**Level 8**
20 Hz at 0,0437 g^2/Hz	20 Hz at 0,0855 g^2/Hz
20 Hz to 50 Hz at +6,0 dB/octave	20 Hz to 50 Hz at +6,0 dB/octave
50 Hz to 1 000 Hz at 0,2734 g^2/Hz	50 Hz to 1 000 Hz at 0,5360 g^2/Hz
1 000 Hz to 2 000 Hz at –6,0 dB/octave	1 000 Hz to 2 000 Hz at –6,0 dB/octave
2 000 Hz at 0,0682 g^2/Hz	2 000 Hz at 0,1330 g^2/Hz
Composite = 20,0 g_{rms}	**Composite = 28,0 g_{rms}**

C.2.3 Vibration test rationale

The general requirements of MIL-STD-810G:2008, Method 514.6 (vibration), are appropriate for determining how lead-free solder alloys perform under severe vibration. The vibration test was run using the stress steps shown in Figure C.1 and Table C.1 developed specifically for the NASA-DoD lead-free electronics project by the Electronic, Electrical and Electromechanical (EEE) Parts and Packaging Group of NASA Marshall Space Flight Center and Boeing. Project stakeholders agreed that a step stress vibration test was required in order to maximize the number of components that would fail during the test. A test conducted at a constant 8,0 g_{rms} level would have required thousands of hours to fail the same number of components as the step stress test.

Table C.2 presents the vibration test methodology. The “Manufactured” test vehicles represent PCB/PWB and electronic components assemblies newly manufactured. The “Reworked” test vehicles represent PCB/PWB and electronic components assemblies manufactured and reworked prior to being tested. Most of the test vehicles had an immersion silver PCB/PWB finishing except for one lead-free “Manufactured” test vehicle that had an ENIG PCB/PWB finishing and one Sn-Pb “Reworked” test vehicle that had also an ENIG PCB/PWB finishing.

Table C.2 – Vibration test methodology

Parameters	Start at 8,0 g_{rms} then step up in 2 g_{rms} increments in the axis perpendicular to the plane of the test vehicles until the 20,0 g_{rms} level is completed. Vibrate for 1 hour at each test level. Finish with 1 hour at 28,0 g_{rms}.						
Number of test vehicles required							
Manufactured				Reworked			
Manufac-tured; reflow solder alloy: Sn-Pb.	Manufac-tured; reflow solder alloy: lead-free SAC305.	Manufac-tured; reflow solder alloy: lead-free SAC305. (ENIG PCB/PWB finishing)	Manufac-tured; reflow solder alloy: lead-free SN100C.	Reworked; reflow solder alloy: Sn-Pb.	Reworked; reflow solder alloy: Sn-Pb. (ENIG PCB/PWB finishing)	Reworked; reflow solder alloy: lead-free SAC305.
5	5	1	5	5	1	5
Trials per specimen						
1	1	1	1	1	1	1

C.2.4 Vibration of major or unique equipment

Specific equipment included:

– electro-dynamic shaker (Figures C.2 and C.3),
– event detector,
– fixture.

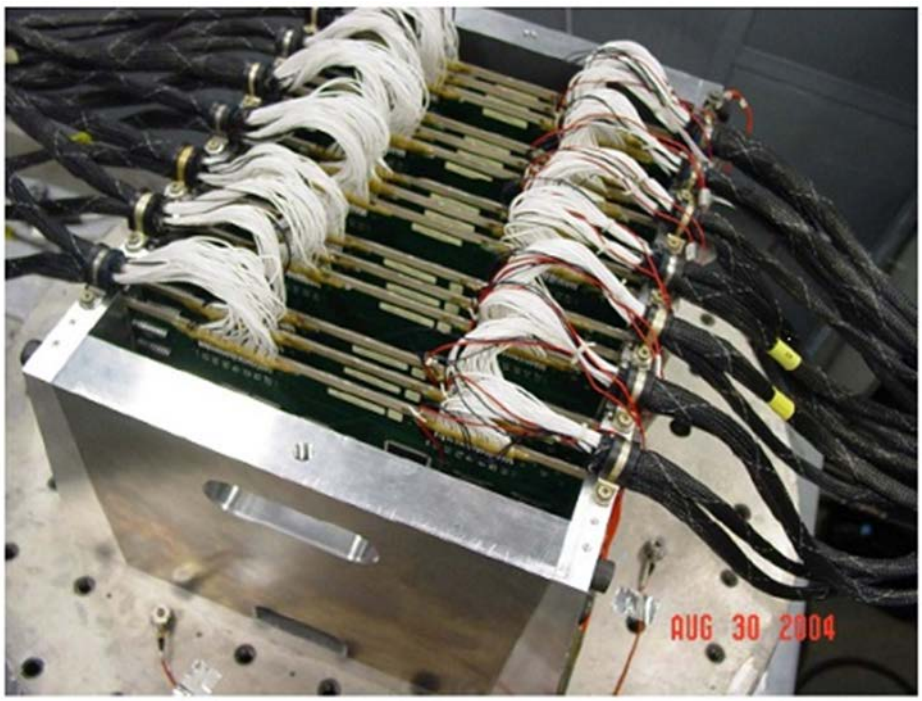

Figure C.2 – Vibration test fixture[5]

5 From the JCAA/JG-PP lead-free (Pb-free) solder project team, which is a predecessor team to the NASA-DoD lead-free (Pb-free) project team.

Figure C.3 – Vibration table showing Y-axis[6]

C.2.5 Vibration data recording and calculations

Record data and comparison to acceptance criteria were performed as specified in the test protocol.

C.3 Mechanical shock

C.3.1 Mechanical shock description

The purpose of this test was to determine the resistance of solders to the stresses associated with high-intensity shocks. Testing was performed in accordance with the requirements specified in MIL-STD-810G. A step stress shock test was performed to maximize the number of failures generated which allowed comparisons of solder reliability to be made.

The CCAs were mounted in a fixture on an electro-dynamic shaker. The required shock response spectrum (SRS) was programmed into the digital shock controller which in turn generated the required transient shock time history.

Testing followed MIL-STD-810G:2008, Method 516.6, with the following modifications:

1) 100 shocks were applied per test level (rather than 3) and all of the shocks were applied in the Z-axis, and
2) the shock transients that were applied at the levels specified in MIL-STD-810G:2008, Method 516.6 (Functional Test for Flight Equipment, Functional Test for Ground Equipment, and Crash Hazard Test for Ground Equipment), followed the modified parameters given in Table C.3.

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6 From the JCAA/JG-PP lead-free (Pb-free) solder project team, which is a predecessor team to the NASA-DoD lead-free (Pb-free) project team.

An additional step stress test was then being conducted (in accordance with Table C.3 and Figure C.4) with the shocks having been applied in the Z-axis only. Testing continued until a majority (approximately 63 %) of components failed. Shock levels, pulse durations and/or frequencies were modified, as necessary, during testing based on the actual capabilities of the electro-dynamic shaker used.

Requirements were as follows: the test SRS shall be within +3 dB and –1,5 dB of the nominal requirement over a minimum of 90 % of the frequency band when using a 1/12-octave analysis bandwidth. The remaining 10 % of the frequency band shall be within +6 dB and –3 dB of the nominal requirement.

The electrical continuity of the solder joints was continuously monitored during the test. All test results were recorded.

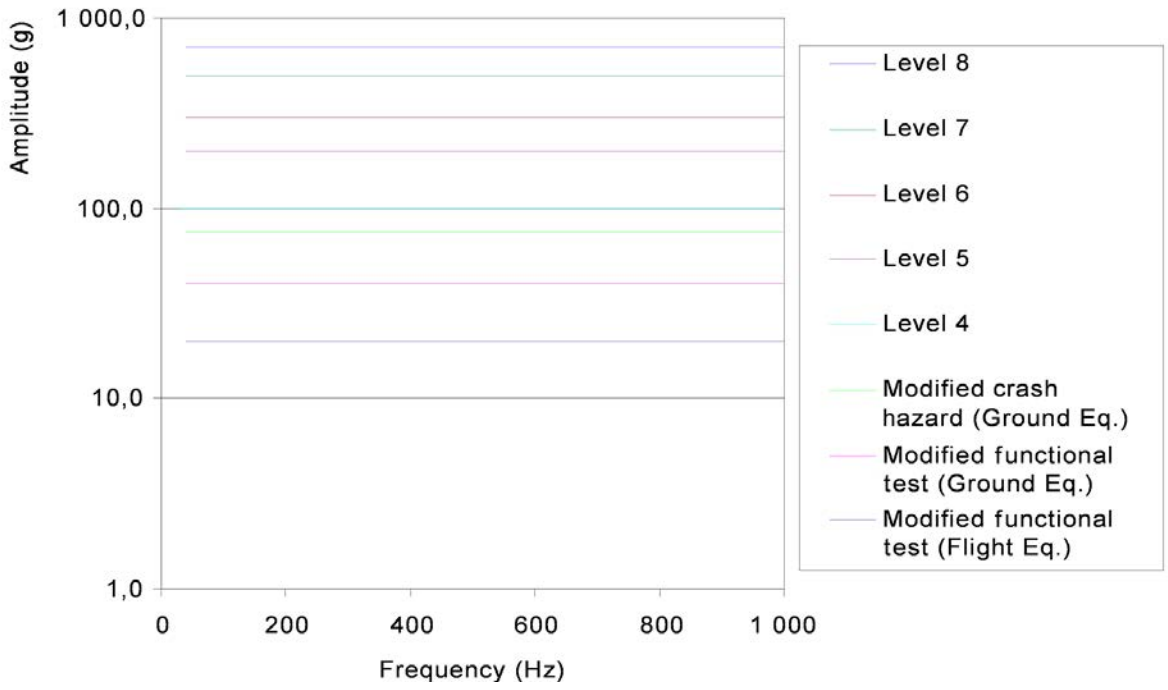

Figure C.4 – Mechanical shock response spectrum

C.3.2 Mechanical shock rationale

The project stakeholders felt that MIL-STD-810G:2008, Method 516.6, Procedure I (Functional Shock), was appropriate for determining how lead-free solder alloys performed under severe mechanical shock.

The stakeholders agreed that a stress step test representing different shock scenarios was necessary. The first three levels address the requirements of MIL-STD-810G. MIL-STD-810G:2008, Method 516.6, Procedure I (Functional Shock), was intended to test material (including mechanical, electrical, hydraulic, and electronic) in its functional mode and to assess the physical integrity, continuity, and functionality of the material to shock. In general, the material was required to function during the shock and to survive without damage to shocks representative of those that may have been encountered during operational service. The project representatives agreed that all three MIL-STD-810G shock levels (Functional Test for Flight Equipment, Functional Test for Ground Equipment, and Crash Hazard Test for Ground Equipment) were to be used (with modification as per Table C.3) as they were representative of different field environments. The project representatives felt that only testing in the Z-axis was required as this was the only axis which allows significant board bending

and subsequent solder joint failures. The representatives also felt that the number of shocks per test should be increased from 3 to 100 in order to increase the probability of failure at any one test level.

Additional step stress shock testing was then being performed to obtain as many failures as possible (levels 4 through 8). One hundred shocks were applied per level and the shocks were again applied in the Z-axis only. These additional step stress levels were derived by NASA Jet Propulsion Laboratory and Boeing representatives.

Table C.3 – Mechanical shock test methodology – Test procedure

<table>
<tr><td rowspan="10">Parameters</td><td colspan="5">The shock transients will be applied perpendicular to the plane of the board and will be increased after every 100 shocks (i.e., a step stress test)</td></tr>
<tr><td colspan="2">Test shock response spectra</td><td>Amplitude (g)</td><td>Time (ms)</td><td>Number of shocks per level</td></tr>
<tr><td colspan="2">Modified functional test for flight equipment (Level 1)</td><td>20</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="2">Modified functional test for ground equipment (Level 2)</td><td>40</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="2">Modified crash hazard test for ground equipment (Level 3)</td><td>75</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="2">Level 4</td><td>100</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="2">Level 5</td><td>200</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="2">Level 6</td><td>300</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="2">Level 7</td><td>500</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="2">Level 8</td><td>700</td><td>< 30</td><td>100</td></tr>
<tr><td colspan="6">Number of test vehicles required</td></tr>
<tr><td colspan="2">Manufactured</td><td colspan="3">Reworked</td></tr>
<tr><td>Manufactured; reflow solder alloy: Sn-Pb.</td><td>Manufactured; reflow solder alloy: lead-free SAC305.</td><td>Reworked; reflow solder alloy: Sn-Pb.</td><td>Reworked; reflow solder alloy: Sn-Pb.

(ENIG PCB/PWB finishing)</td><td>Reworked; reflow solder alloy: lead-free SAC305.</td></tr>
<tr><td>5</td><td>5</td><td>5</td><td>1</td><td>5</td></tr>
<tr><td colspan="5">Trials per specimen</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>

NOTE The test vehicles had similar characteristics than those in C.2.3.

C.3.3 Mechanical shock of major or unique equipment

Figure C.5 shows a mechanical shock test set-up:

– shock table (Figure C.3),
– event detector,
– fixture.

Figure C.5 – Mechanical shock test set-up[7]

Connectors are not to be used (hard wiring and adhesive staking is the accepted practice).

C.3.4 Data recording and calculations

Record data and comparison to acceptance criteria were performed as specified in the test protocol.

C.4 Combined environment test

C.4.1 General

The following protocol was developed for the NASA-DoD 2007 lead-free electronics project, which was conducted to test the effects that lead-free finishes on electronics components and various lead-free solders had on the repair and rework processes used by various original equipment manufacturers and DoD repair depots.

NOTE The intent of this combined environment protocol was to test until at least 63 % was reached to establish the break point of each solder tested. Comparison of this data provided an indication of reliability and operation relative to the base line solder chosen.

Requirements were as follows:

– The combined environments test (CET) protocol is based on MIL-STD-810G:2008, Method 516.6, Procedure I (section 4.6.2.3, Functional Shock).
– Data capture shall be via an event detector monitoring electrical continuity.
– The controlling acceptance criteria for the CET was “better than or equal to Sn-Pb controls at 10 % Weibull cumulative failures.”
– Failure of a test board in a specific test does not necessarily disqualify a lead-free solder alloy for use in an application for which that test does not apply.
– Electrical performance requirements for a particular circuit apply only to parts containing that circuit.
– A 10 % noncompliance of minimal Weibull distribution data for combined environments testing is selected because it was a compromise between the 63,2 % failures, which is taken as normal life, and 1 % failures (or first failure), which is most important in high reliability systems.

7 From JCAA/JG-PP lead-free (Pb-free) solder project team.

C.4.2 Combined environment test description

The objective of this test was to determine the operational and endurance limits of the test vehicles and solder alloys.

The CET was based on a modified highly accelerated life test (HALT), a process in which products are subjected to accelerated environments to find weak links in the design and/or manufacturing process.

The CET process can identify design and process related problems in a much shorter time frame than other development tests. CET was used to determine the operation and endurance limits of the solder alloys by subjecting the test vehicles to accelerated environments. The limits identified in CET were used to compare performance differences in the lead-free test alloys versus the baseline standard tin-lead (Sn-37Pb) alloy. The primary accelerated environments were temperature extremes (both limits and rate of change) and vibration (pseudo-random six degrees of freedom) used in combination. The electrical continuity of the solder joints were continuously monitored during the test. All test results were recorded.

The test was performed as per the following procedure requirements:

– Use a temperature range of –55 °C to +125 °C with 20 °C/min ramps.
– The dwell times at each temperature extreme are the times required to stabilize the test sample plus a 15-min soak.
– A 10 g_{rms} pseudo-random vibration is applied for the duration of the thermal cycle.
– Testing is continued until sufficient data is generated to obtain statistically significant Weibull plots indicating relative solder joint endurance (cycles-to-failure) rates.
– If significant failure rates are not evidenced after 50 cycles, the vibration levels are incremented by 5 g_{rms} and cycling continued for an additional 50 cycles.
– This process is repeated until all parts have failed or 55 g_{rms} is reached.

C.4.3 Combined environment test rationale

Combined environments testing provides a method to identify comparative potential reliability differences in the test alloys versus the tin-lead baseline in a short period of time.

Table C.4 – Combined environments test methodology

Parameters	• –55 °C to +125 °C • Number of cycles ≥ 500 • 20 °C/min ramp • 15-min soak • Vibration last 10 min of soak period • 10 g_{rms}, initial • Increase 5 g_{rms} after every 50 cycles • 55 g_{rms}, maximum
Major or unique equipment	• HALT chamber • Event detector (from Anatech Electronics Inc.[8] or other provider) • Fixture

[8] This information is given for the convenience of users of this specification and does not constitute an endorsement by IEC. Other provider may be considered if their product can lead to the same results.

C.4.4 Data recording and calculations

Record data and comparison to acceptance criteria were performed as specified in the test protocol.

Bibliography

[1] GEIA-STD-0005-1, *Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free (Pb-free) Solder*

[2] GEIA-STD-0005-2, *Standard for Mitigating the Effects of Tin whiskers in Aerospace and High Performance Electronic Systems*

[3] GEIA-HB-0005-1, *Program Management / Systems Engineering Guidelines For Managing The Transition To Lead-free (Pb-free) Electronics*

[4] GEIA-HB-0005-2, *Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Lead-free (Pb-free) Solder and Finishes*

[5] NASA-DoD LFE Test Protocol, 19 September 2007

[6] Shigley, Joseph Edward, Mechanical Engineering Design, THIRD EDITION, McGraw-Hill Book Company, New York, NY, 1977, pp. 185-188.

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http://teerm.nasa.gov/nasa_dodleadfreeelectronics_proj2.htm

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[13] Communication with W. Engelmaier, January 7, 2006

[14] Communication with W. Engelmaier, January 7, 2006 and Follow-up communication with A. Dasgupta on September 28, 2007

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[16] IEC/TS 62647-1:2012, *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 1: Preparation for a lead-free control plan*

[17] IEC/TS 62647-2, *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 2: Mitigation of deleterious effects of tin*

[18] IEC/TS 62647-21, *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 21: Program management – Systems engineering guidelines for managing the transition to lead-free electronics*

[19] IPC/JEDEC-9703, Testing Methodologies for Solder Joint Reliability in Shock Conditions, *Mechanical Shock Test for Solder Joint Reliability*

[20] IEC 62137-1 Series, *Surface mounting technology – Environmental and endurance test methods for surface mount solder joint*

[21] IEC 62137-3, *Electronics assembly technology – Part 3: Selection guidance of environmental and endurance test methods for solder joints*

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