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TECHNICAL REPORT

Nanoscale electrical contacts and interconnects

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NANOSCALE ELECTRICAL CONTACTS AND INTERCONNECTS

FOREWORD

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IEC 62632, which is a technical report, has been prepared by IEC technical committee 113: Nanotechnology standardization for electrical and electronic products and systems.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
113/135/DTR	113/167/RVC

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

The purpose of this technical report is to assess the current status of nanoscale contacts and interconnects, and to provide a basis for establishing international standards with the goal of accelerating innovation in nano-electrotechnology.

Nanoscale contacts and interconnects are expected to constitute challenges for many applications of nano-electrotechnology. The commercial success of many nanoscale electrotechnical subassemblies for electrical, optical, and magnetic products and systems will require contacts or connections to micro- and macroscale devices and systems. Present instrumentation used to characterize and view nanoscale contacts in three dimensions is not adequate for accelerating innovation and therefore commercialization. The standards and measurement methods associated with such instrumentation, and the theories used to interpret measurement results make it difficult to assess performance, reliability, and durability of subassemblies with enhanced functionalities based on nano-electrotechnology.

Nano-electrotechnology stakeholders tend to prefer those standards for nanoscale contacts that are technology- and material-neutral. Promoting standards that are too nano-electromaterial- and process-specific may impede creativity and innovation. Those developing nano-electrotechnology standards will face challenges to achieve balances among standards for nanoscale contacts that are applicable to many applications (DC, AC, and RF) and that are applicable to only a few specific materials with limited applications (e.g. digital).

Nano-electrotechnology is part of nanotechnology. They are often cross-sectional technologies with the potential for many cross-disciplinary applications. From the perspective of the International Electrotechnical Commission (IEC), nano-electrotechnologies include the following areas at the nanoscale: nanostructured sensors; nano-electronics, nano-materials, and nano-devices; optoelectronics; optical materials and devices; organic (opto)-electronics; magnetic materials and devices; radio frequency devices, components and systems; electrodes with nanostructured surfaces; electrotechnical properties of nanotubes/nanowires; analytical equipment and techniques for measurement of electrotechnical properties; patterning equipment and techniques; masks and lithography; performance, durability, and reliability assessment for nanoelectronics; fuel cells; and bio-electronic applications.

The economic significance of nanoscale contacts and interconnects is considerable. Introducing integrated circuits (IC) with higher density increases computing speed and reduces the cost of components for computing and a wide range of applications. If the rate of technology innovation were to slow dramatically due perhaps to the performance, reliability, and durability of nanoscale contacts, there could be a slowing in the introduction of new computing and consumer electronics. This could in turn reduce growth in the semiconductor sector and could have a negative ripple effect in other sectors that depend on semiconductors. Such a decline could have considerable productivity implications for all global economic sectors that rely on semiconductors. Furthermore, if the nanoscale contact processes have unacceptable variations, the yield for circuits may become too low for traditional business models. This would dramatically increase the cost of products, make the new technology more costly, and reverse the 4-decade-old deflationary trend in the semiconductor industry – namely, the substantial decrease in cost per function with each new technology generation.

The development of standards for nano-scale contacts and interconnects will often occur in the context of one or more of the following business models for nano-technologies:

a) Traditional business model

   Research and development supported in part by grants lead to new technologies for prototype product development followed by building manufacturing capacity, deployment, and commercialization. This model may not be appropriate for nano-electrotechnologies because it is very capital intensive and takes too long for commercialization with investors, who often want financial success (positive returns on their investments) quickly.

b) Solution-looking-for-a-problem-or-market business model

Research and development leads to new technology that may have phenomenal commercial success or more likely may remain as an interesting technology sitting on a shelf. Commercialization challenges include, in part, the following:

1) it usually takes a very long time to integrate a specific nano-electromaterial into large-scale industrial processes that customers appreciate and want;
2) markets for specific nano-electromaterials are limited even though the market for the application of the related technology may be large; and
3) costs associated with scaling from the R&D prototype volumes to commercial manufacturing volumes are considerable.

In the context of standards developers, this may not be an optimum model for nano-electrotechnology stakeholders.

c) Penetrate existing markets model:

Based on what the customer wants or on increased functionality for the given application:

1) use core competencies in nano-electrotechnologies to penetrate existing markets and develop nano-electrotechnical subassemblies directed at increasing functionality with lower cost-per-function for specific applications;
2) build a large nano-electrotechnical subassembly portfolio for a positive revenue stream;
3) invest a reasonable portion of profits to develop unique processing capabilities that will maintain a diverse portfolio, while manufacturing some high-volume nano-electrotechnical subassemblies;
4) establish joint ventures and partnerships from the start with organizations that are financially sound and already have access to large markets; and
5) combine efficiently for all stages of subassembly development and commercialization the forces of market pull and technology push, with an emphasis on market pull.

A detailed analysis of the broad implementation of nanomaterials in applications has identified a number of products expected to reach the market in the near future. Some of these products have already emerged from research and are on the market. Because there are so many products being developed that might incorporate nanomaterials, the focus of this report had to be intentionally restricted.

Nanoscale contacts can be formed in many ways, and could have applicability in a variety of products and applications. In particular, contacts may be useful in electrical, optical, magnetic, chemical, and mechanical applications. To limit the scope of this technical report, products and applications have intentionally been restricted to electrical and optical contacts or devices. For the most part, nanoscale contacts covered in this report are restricted to a macroscopic conductor making some contact either directly to a nanoscale contact and then to a nano-object, or making connection to a bulk material that then makes a nanoscale contact to a nano-object.

An analysis of the use of nanomaterials in components and products was conducted. In the analysis, publicly available roadmaps on nanotechnology were reviewed in detail and mind maps were developed that showed the likely use of nanomaterials in nanocomponents, that ultimately nano-enable a product. Through a thorough review of the roadmaps, and through a thorough review of marketing projections, a small number of product applications were highlighted as the focus for this technical report. The product areas of focus include:

– semiconductor devices and integrated circuits: nanoscale contacts and interconnects to the devices on the wafer surface (including the use of graphene);
– OLED lighting and displays (polymer to nano-object contacts, nano-composite materials);

- products that used metal-to-nanowire contacts (including graphene sheets to nanowire via interconnects);
- photovoltaic products (use of nano-objects in PV products to conduct current or to enhance solar efficiency);
- printable electronics, flexible electronics, and flexible displays;
- batteries (lithium-ion and ultra-capacitor products); and
- solid-state lighting (using quantum dots for improved efficiency).

Although many other products and applications exist today that are using a variety of nanoscale contacts and interconnects, it is believed that the above categories highlight some of the most likely candidates that are either on the market today or may be soon. This technical report will restrict itself to this scope, with the expectation of expanding to other products and applications in the future.

It was also difficult in many cases to find published research results concerning any nano-contacts and nano-interconnects related to the various product areas listed above. In particular, the published literature primarily included coverage of CNTs (carbon nanotubes), CNFs (carbon nanofibres), nanowire-to-metal interconnects and graphene interconnects. There was very limited coverage of nano-contacts and interconnects in organic materials to III-V semiconductors such as GaAs, and in magnetic structures. All of these technologies are discussed in this technical report. Due to a lack of published literature related to PV products, printable electronics, batteries and solid-state lighting, those technologies are not discussed in great detail in this report, but may be added in the near future as research reports are published.

Another part of the scope of this technical report relates to measurement techniques used with nano-contacts and interconnects. Throughout the review and analysis, measurement techniques were identified that might benefit from IEC TC113 standards development. This TR provides a summary of potential standards development activities that would enable the nanotechnology to move forward toward greater market penetration.

Two types of nanoscale contacts and nano-interconnects emerged as the most important components to the nanotechnology industry: nanotube interconnects and graphene. These two types of electronic contacts have become critically important to the semiconductor industry in recent years. As the scaling of semiconductor devices continues toward smaller and smaller sizes, circuits have run into limits on the conductivity of copper interconnects and their contacts. The semiconductor industry has started to invest a great deal of money and time into research on graphene and nanotube interconnects in hopes of finding a technology that will help extend Moore's law for a number of additional generations or "technology nodes." Graphene has showed promise in this regard, and appears as the major technology that might extend Moore's law for semiconductor interconnects. Due to this increased interest, many researchers have been studying this material and contacts to graphene. A major part of this TR is therefore devoted to graphene technology, and a good part devoted to nanotubes. Vertical nanotubes may be used to connect horizontal graphene sheets in the vertical direction on an integrated circuit or printed circuit board.

NANOSCALE ELECTRICAL CONTACTS AND INTERCONNECTS

1 Scope

This technical report describes a variety of nanoscale contacts and nano-interconnects used in research and development and in present-day products.

The intent of this technical report is to identify nanoscale contacts and nano-interconnects that will be common in products, to describe the state-of-the-art and to describe some key features and issues related to these contacts. In particular, the following are discussed in each of the nanoscale contacts or nano-interconnects discussed in Clause 5:

– type and configuration of the nanoscale contacts and interconnects formed;
– requirements of the nanoscale contacts and interconnects in products;
– fabrication technologies, processes, and process controls used to make the nanoscale contacts and interconnects;
– characterization techniques used to quantify nanoscale contacts and nano-interconnects;
– functionality and performance of nanoscale contacts and interconnects;
– reliability of the nanoscale contacts and interconnects in products; and
– expectations of when the product and the associated nanoscale contacts will reach the market.

This technical report points out the positive and negative characteristics of the nanoscale contacts and interconnects in each technology or nanomaterial discussed. This information may be helpful to product designers and researchers in their efforts to bring other nano-enabled products to the market. Recommendations for the formation and use of nanoscale contacts and interconnects are also indicated.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/TS 27687:2008, *Nanotechnologies – Terminology and definitions for nano-objects – Nanoparticle, nanofibre and nanoplate*

ISO/IEC 80004 (all parts), *Nanotechnologies – Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/TS 27687:2008 and ISO/IEC 80004, as well as the following apply.

3.1
nanoscale contact
interface between a conductor or conductive bulk material and a nano-object that can pass energy in the form of either current or light

3.2
nanoscale interconnect
a series of conductors or conductive bulk materials connected together by nanoscale contacts that can pass energy in the form of either current or light

4 Framework of the technical report:

This clause addresses the identification of product applications and technical experts, and creation of questions addressed with respect to the various nanoscale contacts and nanoscale interconnects discussed in this technical report.

A process was followed to identify technical experts in the field of nanoscale contacts and nano-interconnects. Initially, a large group of attendees who had participated in a Materials Research Society (MRS) workshop (in 2010, San Francisco) on nanoscale contacts and interconnects were approached. Through personal email contact, nearly a dozen of these individuals agreed to discuss issues related to contacts and interconnects with the author of this technical report (TR). Additionally, these individuals recommended or provided many documents to be used in this TR. A bibliography is included at the end of the TR and is referenced throughout this report.

From the discussions with technical experts, the following list of concerns and questions related to nanoscale contacts and nano-interconnects was formulated. These questions informed the general discussions that took place and focused the attention of the TR on these issues. Throughout the TR, many of these questions are addressed in general, and sometimes specifically.

– What are the types and configurations of the nanoscale contacts formed?
– What types of nanomaterials are used in the product?
– How are these nanomaterials contacted?
– What is the conductor or conductive bulk material used?
– Between which materials (two or more) is the nanoscale contact formed?
– Are there multiple nanoscale contacts in the overall configuration?
– What are the requirements of the nanoscale contacts in products?
– What is the purpose of the nanoscale contact in the product?
– Is the contact meant to pass current? How much?
– Is there an expectation that light will be generated from the nanoscale configuration?
– What are the electrical specifications for the device and in particular the nanoscale contacts?
– Are there other specifications that relate to temperature, environment, voltage, current, frequency, geometry of contact, number of contacts formed, transparency, mechanical and chemical stability or other critical parameters?

• Fabrication technologies, processes, and process controls used to make the nanoscale contacts

– How are nano-scale contacts fabricated or manufactured?
– What process steps are used to fabricate contacts or interconnects?
– What incoming requirements are there related to the nanomaterials used?
– What control processes exist to repeat the process successfully every time the product is manufactured or fabricated?
– Are there special treatments of the nanomaterials used prior to incorporation into the device?

- Are there special post fabrication processes to insure quality nanoscale contacts, such as annealing, light activation, sintering, etc.?
- Are these devices or products being mass produced today, or are the efforts restricted to an R&D environment?

• Characterization techniques used to quantify a nanoscale contact:

- How are the nanoscale configurations characterized?
- Is there an effort to fully characterize the nanoscale contacts formed?
- What are the critical parameters being measured in the nanoscale contacts?
  - I-V characteristics?
  - Ohmic behavior?
  - Schottky behavior?
  - Frequency behavior?
  - Transparency required?
  - Mechanical robustness?
  - Chemical stability?
  - Other characteristics measured?
- What type of diagnostic analysis is employed to deeply understand the type and quality of the nanoscale contacts formed?
- What types of standards activities might be needed to help the industry with the manufacturing and characterization of nanoscale contacts and nano-interconnects?

• Functionality and performance of the nanoscale contacts

- Is the expected functionality from the nanoscale contacts observed?
- Do the nanoscale contacts meet all the requirements for the product?
- What efforts are being or have been made to improve the characteristics of the contacts?

• Reliability of the nanoscale contacts in the product

- Are reliability requirements established for the nanoscale contacts?
- How is reliability measured or characterized?
- Is accelerated life testing used in characterization? What are the results observed?
- Has any long-term aging been employed with the nanoscale contacts? What are the results observed?

• Expectations of when the product and the associated nanoscale contacts will reach the market

- Is the nano-enabled technology/product presently on the market?
- When is the nano-enabled technology/product expected to be on the market?
- What improvements need to be made to the nanoscale contacts and/or nanomaterials to make the technology/product successful?
- What are the plans for next-generation technology/products?

The framework above provides a comprehensive set of questions to be asked that aid in understanding nanoscale contacts and nano-interconnects. The technologies that were explored for this TR are summarized in Clause 5. Note that many of the above questions are not asked by the researchers in every technology effort presented below. Some research focuses primarily on fabrication and performance, while other types might look into reliability. No one paper discusses comprehensively all the areas listed above, but the literature as a whole does give us a good perspective of the pros and cons of the various technologies.

There were some areas that could not be covered with any degree of detail. The area where this was most apparent was the discussion on “expectations of when the product and the associated nanoscale contacts will reach the market.” None of the more than 70 papers that were studied for this TR discussed this topic. The message this sends is that the time for nanoscale contacts and nano-interconnects is not yet imminent. There is still much research to be done before such products will be considered mainstream.

The second least covered area in research publications is “reliability of the nanoscale contacts in the product.” Although there is some reliability coverage, generally the research focuses much more on advanced devices and alternate state variables other than charge and light and much less on improvements in processing for reproducible, high-quality contacts and interconnects. Many of the concerns that follow below in 5.1 to 5.3 relate to bringing nano-contacts and nano-interconnects to a level of maturity allowing selection of the most promising of these as candidates for high-volume manufacturing.

5 Analysis of state-of-the-art nanoscale contacts and nano-interconnect technologies

5.1 Nanotubes and nanowires

5.1.1 Type and configuration of the nanoscale contacts formed

The technologies for nanoscale contacts and nano-interconnects discussed in this clause include the following:

– SWCNTs (single-wall carbon nanotubes);;
– MWCNTs (multi-wall carbon nanotubes);
– SnO_2 nanowires (tin-oxide nanowires);
– Si nanowires (silicon nanowires);
– CNFs (carbon nanofibres) to gold electrodes;
– PECVD (plasma-enhanced chemical vapour deposition)-grown CNTs and CNFs on metal under-layers; and
– Ni-silicide to n-Si (n-type silicon) nanowires.

5.1.2 Requirements of the nanoscale contacts in products

Typical nanoscale contacts should theoretically be either a pure Schottky barrier (ideality factor of 1.0, follows thermionic emissions theory of transport, barrier height defined by work functions of the materials), or ohmic (linear I-V characteristic, with a contact resistance that is a relatively small fraction of the overall resistance of the nanowire device).

Humpston [10][1] suggests that low electrical resistance has been reported for CNTs at values about 10^{-4} Ω-cm, and having current densities of 10^{12} A/cm^2.

Univeristy Course [36] reports additional properties of CNTs having mean free paths for electrons at a room temperature of 1 000 nm, as compared to copper at 40 nm. This explains why CNTs are expected to have low resistance values, and be able to conduct large current densities. However, these theoretical values are somewhat diminished by the great difficulty in forming a low-resistance nanoscale contact to an isolated CNT. It is noted that it is very difficult to make a quality contact to a 1 nm-sized nanostructure.

[1] Numbers in square brackets refer to the Bibliography.

5.1.3 Fabrication technologies, processes, and process controls used to make the nanoscale contacts

Univeristy Course [36] suggests that forming bundles or ropes of CNTs might be a better solution for interconnects on integrated circuits (IC). These bundles or ropes might also address the issue that CNT growth typically results in both metallic and semiconducting nanotubes, and one cannot deterministically get one or the other with the present technology maturity. This is a significant issue to be overcome before CNT interconnect will ever make its way into the mainstream. As an interconnect, if the CNTs were semiconducting, they would not contribute to the current conduction compared to metallic CNTs. Alternatively, if the CNTs were metallic, they would cause a short, if the intention was to have semiconducting CNTs instead.

Additionally, small diameter (<10 nm), multi-wall CNTs (MWCNTs) are metallic in nature, and have a mean free path of just a few nanometres, compared to micrometres for SWCNTs. This makes MWCNTs essentially unusable in a semiconductor device environment where traces must traverse micrometre distances. It should be pointed out that Li [15] claimed mean free paths in MWCNTs, but they had diameters of 100 nm. This size of MWCNT essentially defeats the goal of reducing the conductor size below 20 nm as a replacement for Cu in future technology nodes. These characteristics of SWCNTs and MWCNTs make the fabrication of useful devices in large volume a non-trivial challenge.

PECVD-grown CNTs and CNFs on metal under-layers were studied (Sun [34]). The nanoscale contacts formed were studied individually with nano-manipulators in an SEM. It was shown that under-layer metals must not interact with the catalysts (Ni, Co, or Fe) to form alloys when growing CNTs/CNFs. A poisoning of the catalyst could result. Additionally the under-layer metal must form a low contact resistance and provide excellent adhesion to the catalysts and to the underlying silicon substrate. Sun [34] chose Ti, Cr, and Al as underlying metals to study. Unfortunately, Al as an under-layer metal led to alumina (an insulator) being formed in growth. Therefore, these contacts had essentially infinite resistance and were not useful. Al appears to be unsuitable as an under-layer metal for via interconnect applications.

Mohney [20] discussed how they made contacts with Ti/Au metalization to semiconductor nanowires. They stated that “negligible current is transported through the nanowires before the native oxide is stripped and the top Ti/Au contact is deposited.” This clearly indicates that a Si nanowire, or other semiconducting nanowire, would form a native oxide on its surface. Also, before any metalization could make direct contact to the nanowire, the oxide would need to be sputtered or etched away in some fashion. This is a concern for any mass production of semiconductor nanowires used in integrated circuits. Solutions that address use of nanoscale devices, such as nanowire resistive elements, must be addressed before these structures will become main stream.

Dellas [6] performed important research on the fabrication of $NiSi_2$ (nickel silicide) to silicon nanowires. $NiSi_2$ has recently been used to make MOS (metal oxide semiconductor) field-effect transistors on integrated circuits with excellent ohmic contact characteristics. Since these ohmic contacts have become mainstream in Si chips, it was decided to try to make similar ohmic contacts and to characterize them when contacting Si nanowires. It was determined that on planar Si MOS devices, $NiSi_2$ contacts could be easily formed on most typical orientations in Si, including (111), (011), and (001). This was found to be the case because no matter what orientation the initial $NiSi_2$ began, it quickly propagated along planes of formation that led to quality ohmic contacts being formed. This, however, was not found to be the case in Si nanowire $NiSi_2$ formation. The only orientation of Si nanowires that would form good $NiSi_2$ ohmic contacts was (111). Propagation and phase transformations generally present in planar, and micrometre-sized structures, were not present in nanowires, and therefore quality ohmic contacts could not easily be formed.

This research once again points to the issue of extrapolating common techniques used in Si manufacturing for use in nanoscale contacts formation. Much research will need to be done to develop proper manufacturing techniques to be used at the nanoscale. It can't be assumed that every Si nanowire that will be contacted by $NiSi_2$ ohmic contacts will have the (111)

orientation. Therefore, the $NiSi_2$ ohmic contact technology might not be portable to nanoscale contacts.

Vogler [39] reported on the effects of different dielectric layers on the surface of CNTs. It was shown that Al_2O_3-coated CNTs have three times the conductivity of SiO_2 coated CNTs. This likely has something to do with surface effects caused by the dielectric in direct contact with the surface of the CNT. It also points out the many unknowns that might exist as one tries to make CNT interconnect. Almost every effect that can happen at the surface of a semiconductor will have more impact as one scales to the nanometre size. This is one reason why predicting the performance of micro-sized devices is easier and fabricating them is more forgiving.

5.1.4 Characterization techniques used to quantify a nanoscale contact

In general, the research groups that study CNTs and nanowires use both 2- and 4-probe electrical resistivity measurements on individual nanowires. These are simple, and traditionally accepted approaches to characterization. There was no mention of any particular issue in the characterization of these resistive-like devices. However, a proper choice of contact probe and procedures is important to obtain reproducible results.

SnO_2 nanowires (Hernandez-Ramirez, et al [9]) have high contact resistance values and nonlinear I-V characteristics when measured with 2 probes. This is explained by the existence of back-to-back Schottky barriers arising from the platinum-nanowire contacts used. Platinum was the probe metal. Hernandez-Ramirez, et al. noted that “although one-dimensional materials (nanowires, CNTs) are believed to have new and improved electrical properties, accessing them individually to perform full electrical characterization remains a challenge.” And it should be pointed out that this research was only meant to be on individual nanowires, and scaling many contacts to many nanowires will be orders of magnitude more difficult. The research concluded that only 4-probe measurements should be used to assess the resistivity and resistance characteristics of nanowires.

NOTE The methods for interpreting and extracting resistances from 4-probe measurements have not been validated when any of the dimensions are at the nanoscale. The theory and modelling is based on 3D continuum concepts. The experimental arrangement of the 4-probes results in a 4-terminal device. Thus, correctly extracting a resistance requires improved devices models and computer simulations. The history of EBIC measurements across junctions in the 1980s provides lessons to be learned for nanotechnologies.

Sun [34] used nano-manipulator tips with a 20-nm diameter under SEM (scanning electron microscopy) imaging to contact the CNTs/CNFs. Clearly, this type of technique does not lend itself to characterization in a manufacturing environment.

Madriz, Y. S. [17] measured CNFs that were connected to metal electrodes. The circuit models used were RC circuits, and the experimental data demonstrate that CNFs are purely resistive up to frequencies of 50 GHz. However, a comment made by the authors in the conclusion was troubling: “The difference between the model and experiment comes primarily from process variation.” This again speaks directly to the lack of process control when trying to form nanoscale contacts to CNFs. Two parameters that are particularly difficult to control are the CNF bulk resistance, and the contact resistance between CNF and electrodes. This paper published in 2010 continues to suggest that there is simply too much variation in contact resistance to nanostructures to be able to predict performance of the finished devices.

5.1.5 Functionality and performance of the nanoscale contacts

An investigation of tunnelling between carbon nanofibres and gold electrodes was carried out by Yamada [42]. The major investigation was that of placing carbon nanofibres directly on top of gold electrodes, and characterizing them. It was found that the initial resistance is typically measured in the megaohm range. The researchers then passed current through the electrodes-nanoscale contacts-CNFs in the range of 10^5 A/cm^2 to 10^6 A/cm^2 for a few minutes. They observed that the resistance would decrease by 2-3 orders of magnitude. The researchers called this phenomena “current stressing.” Through experimentation, it was also

noted that the change in resistance was in the nanoscale contacts, and not in the bulk of the CNF.

The conclusions of Yamada et. al. were that current stressing reduced the tunnelling gap in the contacts between the CNF and gold electrodes. This occurred through a change in the interfacial nanostructure morphology and impurity reduction as a result of joule heating. It is believed that the current stressing through heating is a common method in the semiconductor field of turning a poor ohmic contact into a reasonable one. In a research environment, this current stressing method is very common, but a manufacturing process requires that any expected ohmic contacts will be ohmic upon deposition of the final contact metal. Process development must take place that eliminates the possibilities of interfacial contamination before such processes can be released to manufacturing

Sun [34] showed that there are significant effects on nanoscale contacts resistance that depend upon average tube diameter, diameter distribution, density, growth rates, choice of under-layer metal, and choice of catalyst in PECVD-grown CNTs and CNFs. Sun cited in the introduction, that even in 2009, the optimized conditions for growth to achieve a low-resistance contact remained a challenge.

Sun also noted that the growth of CNTs/CNFs on under-layer metals always led to nanoscale contacts with metal oxides between the CNT/CNF and the under-layer metal. Oxides of Ti and Cr were measured with XPS. This then led to high contact resistance. The observed contact resistances were between ~4 kΩ – 5 kΩ for average CNT diameters of ~60 nm – 120 nm. Sun suggested that “metal oxide formation between CNT and under-layer metal is one of the major causes of large contact resistance” in the structures studied.

Madriz J. K [16] investigated CNFs that were bridged across two gold electrodes. Their study measured the resistances and capacitances of the electrode-CNF-electrode structures. The test method used to characterize the CNFs included measuring the test structure without a CNF, then measuring the CNF in the structure, and finally subtracting the S-parameters from the two cases to deduce the characteristics of the CNF itself. This is a common method used to characterize a device, while eliminating any test structure-based parameters in the measurement. The troubling results of this research lie in the lack of correlation of resistance and capacitance to diameter and length of the CNF devices. One would expect that for the same CNF diameter, a correlation would exist if the length of the CNF were doubled. However, the results observed were the following:

– length of the CNF did not correlate with resistance measured for the device, even when taking the contact resistance into account;
– devices of similar diameter and length had variations of greater than 50 % in resistance, pointing to the lack of consistency of device formation; and
– capacitance showed no correlation in the measurements made.

These results indicate that the method used to build test structures has significant issues of consistency and represents a critical challenge for standards development. There is not enough control of the interface between a CNF and the electrode in this research work, and it likely is the cause of variability seen in the electrical characterization performed.

An alternative view of the research work by Madriz might suggest that much of the inconsistency and correlation issues come from the characterization method used. A high frequency interconnect with acceptable propagation characteristics should show a small value of S11 < -20 dB (small reflection coefficient), and high value of S21 close to 0 dB (i.e. transmission coefficient close to 1). This is difficult to achieve with nanoscale interconnects due to inherently large impedance mismatch between nanoscale fibre and the standard interconnect impedance of 50 Ω. A 50 Ω nanoscale interconnect or impedance transformers are needed in order to interface and transmit high-frequency signals efficiently between nano-structured electronics and the characterization electronics. It is recommended that extreme care be taken when trying to make high-frequency impedance measurements of nanoscale devices.

Sarpatwari et. al. [30] performed extensive research on Schottky barriers formed between nanowires and metals. They looked at the effects of both geometry and surfaces that can significantly alter conduction through nanowire contacts. It had previously been reported that "barrier-width thinning" might occur in nanoscale contacts, and this could result in increased tunnel currents. Additionally, Fermi-level pinning at the interface between the metal and semiconductor nanowire might be reduced in nanoscale contacts compared with bulk Schottky contacts. These were explored by the researchers. Until this group conducted this research, no other systematic investigation had been reported on the metal/nanowire Schottky diode I-V characteristics, and how one might extract the true Schottky barrier height from the I-V characteristics.

This research group built a device that was a Ni-Silicide nanowire Schottky contact to an n- Si nanowire to an n+ Si nanowire to an ohmic contact. This nanowire device was completely surrounded by Si oxide and a surround-gate metal. Techniques such as gate-bias I-V characterization were employed to study the Schottky-nanowire contacts. The research team then investigated effects on the Schottky barrier from gate bias, temperature, doping densities in the nanowire and ohmic region, interface trapping, gate structure overlap, and image-force-lowering effects. This group was able to plot the effective Schottky-barrier height as a function of the ideality factor of the diode, and from that curve, extrapolate to an ideality of 1,0 to deduce a barrier height of 0,557 meV for the Ni silicide/n-Si nanowire Schottky diodes. This research work was probably most significant for its thorough method of measurement of the Schottky diodes, and for its explanation that the diodes deviate from the thermionic emission models for a diode because of enhanced tunnelling effects at the interface.

It is important to once again point out the "single-device nature" of this characterization effort. Methods such as that described in this work are useful in the measurement of a few devices or nanowires, but would not be useful in the characterization of large numbers of devices. To bring this research work to the production and characterization of millions of nanowires would take quite a change in approach and method.

Mohney [20] did extensive research on ohmic contacts to semiconductor nanowires. They measured "specific contact resistances" about $(5 \times 10^{-4})\ \Omega cm^2$ for Ti/Au contacts to boron-doped, $10^{19}\ cm^{-3}$, p-type Si nanowires with diameters of about 80 nm – 100 nm. Contact resistance is then given by the "specific contact resistance" divided by A (area of the contact, assuming a uniform current through the entire contact area). This assumption of uniform current is typically a bad assumption due to edge current effects, and is particularly bad for very small nanoscale contacts. This research team did an extensive investigation of ohmic contacts to characterize them properly.

The nanowires used in the research by Mohney [20] were very heavily doped, so that edge depletion and surface effects on the nanowires could be neglected. This assumption would of course become worse as the doping in the nanowire was reduced. A second big assumption in the measurement work by Mohney was that the nanowires have a uniform resistivity and identical radii. In 2005, and possibly still today, this assumption of uniformity was not normally met because fabrication methods:

– produce nanowires of different radii;

– produce nanowires with different crystallographic orientations; and

– produce only a fraction of nanowires that are considered bicrystals or semiconducting.

Mohney used both 4-point probing and varying lengths of nanowires between contacts in the characterization of the nanowires and nanoscale contacts. The 4-point probing technique was the best choice for accurate measurement of contact resistances. The work clearly established "specific contact resistances" about $(5 \times 10^{-4})\ \Omega cm^2$ for Ti/Au contacts to p-type Si nanowires with diameters of about 80 nm – 100 nm. Future research work could be compared to this benchmark measurement. It should also be noted that the concentration of dopant in the p-type nanowires was estimated in the range of $10^{19}/cm^3$. This was measured using secondary ion mass spectrometry (SIMS), but this technique is not highly accurate as it

is very difficult to use this technique on nano-sized wires. Nonetheless, the assumption of highly-doped nanowires was likely reasonable.

5.1.6 Reliability of the nanoscale contacts in the product

The papers cited in this clause do not address reliability to any significant degree, and therefore nothing appears under this topic.

5.1.7 Expectations of when the product and the associated nanoscale contacts will reach the market

No mention of any expectation of technology reaching the market is discussed in papers cited in this clause, and therefore nothing appears under this topic.

5.2 Via interconnects using CNTs and CNFs

5.2.1 Type and configuration of the nanoscale interconnects formed

One of the goals related to CNT and CNF usage is to provide local-interconnects for integrated circuits. These via interconnects would need to be better than the copper vias that are presently used in the industry. Moreover, copper vias are presently beginning to have issues with electromigration, resistance increases with shrinking size, and limited current density. CNTs and CNFs exhibit robust thermal and mechanical properties that should make them ideal for on-chip interconnect.

CNTs are also envisioned for use as “bumps” on printed circuit boards to replace the present solder bump. Solder bumps are made of eutectic metals of Sn and have stress, flexibility, and conductivity issues, especially due to warping of printed circuit boards. A CNT via potentially has higher thermal conductivity, and excellent mechanical strength and flexibility.

Kreupl [12] cites a current density in CNTs that exceeds copper by a factor of 1 000. This is a significant driving force for consideration of CNTs for via interconnects as they should resolve some of the electromigration and reliability issues of Cu vias as current densities increase with decreasing via size. Kreupl suggests current density in CNTs between 0,54 and $1{,}8 \times 10^{10}$ A/cm^2. This research also compares “arrays of SWCNTs” to “varying-diameter MWCNTs” to “copper wires.” It was found that arrays of SWCNTs would provide the lowest resistance in an interconnect, outperforming Cu by 10 to 100 times for wires in the range of 30 nm diameter. Exactly how one might fabricate such arrays and also ensure that the SWCNTs are all metallic is not discussed in this paper. They do suggest that the bottom of the via should have a metal oxide in the bottom of the via of either Ta, Al, Ti, Cu, or Cr. The researchers suggest using CVD growth techniques for the SWCNTs at 450 °C – 800 °C.

MWCNTs appear to outperform Cu up to diameters of about 15 nm. This is important as it is much easier to grow MWCNTs that are metallic than it is to grow arrays of all-metallic SWCNTs. In fact, the latter has never been reported to the collective knowledge of the members of IEC/TC 113.

5.2.2 Requirements of the nanoscale interconnects in products

Low contact resistance is one requirement for vias formed using nanostructures.

5.2.3 Fabrication technologies, processes, and process controls used to make the nanoscale interconnects

Kreupl [12] discusses two approaches to growing SWCNTs in vias. One method is called the “bottom-up approach” which starts with a catalyst, then the SWCNTs are grown and covered with SiO_2, which is finally planarized. Metal is then connected to the top of the exposed SWCNTs. The second method suggested is called the “buried catalyst approach.” In this process, the catalyst is deposited across the metal under-layer electrode and is then coated

with SiO_2. A via is etched in the SiO_2, in which the SWCNT arrays are grown, and finally coated with a top-metal electrode.

Kreupl reports experimental results that show current densities of only 5×10^8 A/cm^2, and a resistance for a 20 nm wide MWCNT of 7,8 kΩ. These experimental results are not good compared to the theoretical estimates. The current density is nearly two orders of magnitude lower than predicted, and the resistance of the wire is also nearly 2 orders of magnitude higher than what would be the resistance in an equivalently sized Cu wire. Additionally, there was a "required" annealing step of 900 °C to reach this resistance value experimentally. This is because the "nanoscale contact" is not metal-to-MWCNT exactly, but also includes interfacial issues with dielectrics which lead to tunnelling or thermionic emission currents rather than ohmic contacts.

Kreupl also brings up the issue of contacting the many "shells" of the MWCNT. It is believed that the process did not make ohmic contact to all the concentric CNTs in the MWCNT, and this poses great complexity in the manufacturing process. It will be a grand challenge to planarize and contact all the shells of a MWCNT in mass production.

5.2.4 Characterization techniques used to quantify a nanoscale interconnect

No specific discussion of unique methods or issues related to characterization of CNT or CNF via interconnects were discussed in the papers used in this clause. Therefore no additional comments are made here.

5.2.5 Functionality and performance of the nanoscale interconnects

Wu W. [40] studied CNT- and CNF-based interconnects. They concluded that there was an existence of a thin and poorly conducting layer between the CNFs and the metal electrodes that they were grown on. This oxide-based layer produces nano-interconnects that are not purely ohmic, but behave like a tunnel diode. The authors concluded that vias fabricated from grown CNFs would have their resistance dominated by the contact resistance of the CNF to the underlying metal electrode.

In conclusion, Wu states "the contact resistance at the metal-carbon interface dominates the electrical characteristics of carbon nanostructures in via interconnects." This is again an alarm signal for the potential use of carbon nanostructures in integrated circuit applications. There must be a solution to overcome any interfacial issues related to oxides or contamination before these types of contacts will be useful on integrated circuits.

Ngo [24] performed research and characterization on CNFs as they might be used in via applications in ICs. Their main interest was to explore the possibility of substituting CNFs for Cu vias that would be susceptible to electromigration reliability issues. The CNFs in this research were formed by a plasma-enhanced chemical vapour deposition (PECVD) process. This process produced CNFs with stacked-cone morphology. The lowest resistance value measured in this research was 5,8 kΩ for a single 21-nm diameter, 4-μm long Pd-catalyzed CNF, which corresponds to a resistivity of 50 μΩ-cm.

Ngo concludes that if one compares this resistance/resistivity result to a scaled down copper interconnect technology, the CNF result will NOT achieve the predicted 312 Ω for the 21-nm diameter 4-μm-tall copper via. Indeed the 5.8 kΩ result is nearly 20 times bigger than 312 Ω. Now it must be cautioned that the model for a scaled down Cu via doesn't consider some negative effects such as electromigration, additional resistance from grain-boundary scattering, sidewall roughness scattering, or voids. However, even with these real possibilities, there is no indication at this time that CNFs will be a viable via replacement for Cu. The one positive characteristic of CNFs that is a true advantage over Cu is the lack of a failure mode due to electromigration.

5.2.6 Reliability of the nanoscale interconnects in the product

The papers cited in this clause did not address reliability to any significant degree, and therefore nothing appears under this topic.

5.2.7 Expectations of when the product and the associated nanoscale contacts will reach the market

No mention of any expectation of technology reaching the market was discussed in papers cited in this clause, and therefore nothing appears under this topic.

5.3 Surface (lateral) interconnects using CNTs and CNFs

5.3.1 Type and configuration of the nanoscale interconnects formed

It is pointed out here that CNTs have been studied not only as surface-interconnect in ICs, but also as active gates on FETs (field effect transistors). Sinha [31] studied the performance of such CNT FETs, and projected that these unique transistors might outperform their traditional counterpart FETs by as much as 8 times higher. This research effort does state in its conclusion that “CNTs possess the capacity speeds to surpass CMOS transistors, assuming that high-level integration and process-related challenges are met.” In addition to the integration and process challenges cited, the research team made some assumptions in their models that are likely not realizable. They used CNT to metal Schottky barrier heights of 0 V. Additionally, they had to assume dielectric constants and thicknesses of gate oxide that are unrealizable. These assumptions lead to large over-predictions of performance. No research group in the world has proposed a solution to making millions of transistors on an IC (integrated circuit) that have perpendicular current flow, excellent contact resistance, and reliability of 100 %, which is a requirement of every transistor in an integrated circuit to have general functionality.

The rest of this clause addresses the use of CNTs and CNFs in lateral interconnect, and not as components in FET devices.

CNTs and CNFs have been envisioned for potential use in local, lateral interconnects on ICs. There have been many discussions related to this topic over the past 10-15 years, but there continue to be huge challenges to face. These challenges include:

– alignment of multiple nanotubes in orthogonal direction on ICs;
– making excellent ohmic contacts to those nanotubes;
– producing only metallic nanotubes when building interconnects;
– having a mass-production process for putting nanotubes on an IC;
– making connections to vias on ICs; and
– blending all new process technology into the fabrication process for ICs.

If we consider the first issue listed above relating to orthogonal nanotubes on an IC, we can see the magnitude of the issue for interconnects. One could imagine two independent nanotubes contacting each other to form a junction. This junction might be ohmic in nature if two metallic nanotubes came into contact, or might be a Schottky barrier if two semiconducting nanotubes came into contact. To be successful as an interconnect, we must assume that the contact formed is between two metallic nanotubes. One can envision the difficulties of the formation of such a contact, and how they maintain a contact to each other, and not just because they happen to contact each other at an intersection. How would one position the nanotubes? How would one insure that they are perpendicular to each other? How would one maintain the close contact? These are all contact issues which are fundamentally difficult to surmount.

Menon [19] did research on forming continuous crystal T-junctions with carbon nanotubes. The study looked at formation of T-junctions between two different metallic CNTs. The final

conclusion of a physically realizable T-junction is one that transitions from metallic to semiconducting to metallic. Thus a tunnelling junction is formed, and not the desired metallic to metallic connection that is highly desired and required for a quality on-chip interconnect. The work by Menon demonstrates the real difficulty in forming just a single metal-to-metal CNT contact on an IC. This problem is greatly compounded when one thinks of the challenge to form these same types of interconnects by the millions across the surface of a wafer as is regularly done with Cu and Al in ICs today. Menon makes no suggestion that it would be possible to form a metal-to-metal CNT T-junction, thus exposing a significant barrier to successful implementation of local interconnects with CNTs.

5.3.2 Requirements of nanoscale interconnects in products

As mentioned above, the CNTs must be metallic, conductive, highly-integrated, orthogonal, and with extremely low contact resistances where two or more CNTs meet.

5.3.3 Fabrication technologies, processes, and process controls used to make the nanoscale interconnects

Massoud [18] performed research on both SWCNT and MWCNT and compared performance to Cu interconnects. Most significantly, Massoud made significant contributions to CNT technology by speaking directly to issues that exist with CNT fabrication.

One observation made was that the controls on MWCNTs, at least in the year 2008, were not good enough to maintain resistance and diameter control. Therefore, with the wide variation in MWCNT resistance, there was simply no hope for such devices in interconnect technology unless major control enhancements were made. Similarly, there were comments related to the area of the surface that would need to be covered by CNTs to be useful as an interconnect in ICs. Again, in 2008, there was simply no growth technique that would produce the 30 % – 40 % density on the surface for either SWCNTs or MWCNTs in vertical (via) or horizontal (interconnect) applications.

Thus, even though Massoud suggested that SWCNTs and MWCNTs might produce up to 2 times lower delay in a circuit, he pointed out at the same time that there was no realizable manufacturing method available to fabricate the ideal CNT bundles needed to reach this level of performance. Much fabrication development remains to be done.

5.3.4 Characterization techniques used to quantify a nanoscale interconnects

No specific discussion of unique methods or issues related to characterization of CNT or CNF lateral interconnects was contained in papers used in this clause. Therefore no additional comments are made here.

5.3.5 Functionality and performance of the nanoscale interconnects

Raychowdhury [27] published an excellent journal article that addressed assertions of many experts that CNTs would be a solution for interconnects as Cu was challenged at smaller dimensions. In the research conducted, a direct comparison of individual CNTs to Cu interconnect, then multiple, tightly-packed, planar CNTs to Cu interconnect, and finally arrays of tightly-packed CNTs to Cu interconnect was performed. The results of the research dispel much of the hype about the imminent replacement of Cu interconnect with CNTs.

The issues with Cu were cited by Raychowdhury as:

– susceptibility to electromigration at high current densities ($> 10^6$ A/cm^2);
– lower reliability as interconnect dimensions are scaled; and
– higher resistivity of Cu as dimensions decrease, due to electron-surface and grain-boundary scatterings.

As part of the research, the resistance of CNTs was modelled and measured. Two significant observations were made:

– the resistance of CNTs begins to rise after the CNT gets close to the mean-free-path for electrons at about 1 μm; and

– the resistance of CNTs is bias dependent with low bias voltages (< 0,1 V) producing resistance values of 5 kΩ – 10 kΩ, whereas higher bias voltages (> 0,5 V) produce resistance values of 50 kΩ – 500 kΩ.

These types of resistance changes can be seen in I-V characteristics of CNTs of all different lengths from 2 μm to 50 μm in length. These resistance values are significantly higher than what might have been predicted theoretically, and are also large when compared to Cu interconnect.

What was more remarkable in the research by Raychowdhury [27] was the focus on "signal delay" in the interconnects. The ITRS (International Technology Roadmap for Semiconductors) has a prediction that the delay needs to be about 5×10^{-12} sec for an interconnect length of 1 mm. Unfortunately, a single CNT is likely to produce more than 2 orders of magnitude more delay than the ITRS roadmap suggests is required. Raychowdhury concludes "a single CNT would be insufficient to act as a high-speed interconnect for the future technology. However, for very short or local interconnects, where a very low current drive is required, CNTs may be useful." This conclusion, if verified independently by others, suggests that single CNTs are not likely candidates for high speed interconnects in ICs.

Next the research team looked into a parallel group of CNTs to route the same signal. This planar 2-d array of CNTs would have at least 1 000 times more current capacity than a Cu interconnect of the same geometry. However, the effect of being able to handle more current reliably does not translate into improved circuit performance or reduced delay. The reasons for this are that:

– CMOS circuits are voltage driven and not current driven;

– therefore the resistance and not its current density limits are important in predicting performance (resistance combined with capacitance adds delay in a circuit);

– Cu interconnect can be made very tall even as the width of the line is reduced through the use of damascene processes, which substantially reduces the resistance of Cu wires; and

– since the cross-sectional area of 2-d CNT arrays is small compared to Cu, the quantum resistances and scattering effects cause delays in signal propagation.

As a result, even with higher current density, the switching delay of a 2-d CNT array of interconnects far exceeds that of Cu. The results show a difference of about 3-4 orders of magnitude more delay in SWCNTs than in Cu with an equivalent width of 80 nm.

The major conclusion from this clause is that "for a voltage-driven circuit, the interconnect resistance, and not the current density, determines the switching speed." And for SWCNTs, the clear winner is Cu.

Lastly, Raychowdhury [27] looked at 3-d arrays of CNTs that were 20 CNTs wide with each CNT having a 4 nm diameter, and with N CNT layers or rows extending vertically from the surface of the device (Z-direction). This CNT array was compared directly to Cu interconnects that are 80 nm wide, and 625 nm high. This 1:8 width-to-height ratio is common in damascene processes today in ICs. The results were again not encouraging for CMOS (complementary metal-oxide semiconductor) circuits. If the value of N = 5, then the delay is 4 orders of magnitude larger than for Cu. As N increases, this difference in delay decreases, but never approaches the performance of Cu. In fact, even if N = 200, the delay is still 1-2 orders of magnitude longer in CNTs than in Cu for interconnect lengths $< 10^{-6}$ m. Even for interconnect lengths $> 10^{-6}$ m, the delay for the 200 stacked CNT arrays is no better than that for Cu.

Moreover, the notion of actually fabricating a 200 tall stack of closely packed CNTs that are all purely metallic and all contribute to the current flow and interconnect path is highly unlikely to be achieved. This is a major issue for CNT interconnect as even with simple theoretical calculations, there really appears to be no justification for looking more deeply into interconnects of CNTs.

In conclusion, Raychowdhury states that “although CNTs have high current densities and greater reliability, the intrinsic quantum resistance limits their performance in voltage-driven circuits. The charging and discharging times of CNTs are large and they severely limit high-frequency operation.”

Li Y. M [15] has published what appears to be a contrary conclusion to that of Raychowdhury above. They report that MWCNTs can produce signal delays that are as low as 15 % of the delay in equivalent Cu interconnect. Their theoretical calculations were for interconnects of 1 000 μm (1 mm) length. If the length of interconnect drops to 200 μm, the improvement in delay for MWCNTs is between 30 % and 50 %. Nevertheless it seems that the work was not fairly represented as they used “driver” circuits in their simulation that were sized to be 100 times bigger than the minimum size required. When they made this assumption, they essentially introduced the ability to charge up capacitance much better than in a real life application where circuits are design much closer to the minimum size needed to reach the speeds desired in a circuit.

It was also shown that the signal delay for local interconnect with MWCNTs was actually worse than that of Cu, even when assuming the driver was oversized by 100 times. Local interconnect was defined as lengths less than 1 400 nm or 1,4 μm.

For the present technical report, this research does at least suggest that long interconnect with MWCNTs might be useful and constitute a possible replacement for Cu. However, all of the actual implementation issues at hand that have been mentioned many times throughout this report continue to exist and must be overcome before the use of MWCNTs is realized. Moreover, the effort to achieve a desired six-fold improvement over Cu interconnect delay may be so large that it will not be justified.

5.3.6 Reliability of the nanoscale interconnects in the product

The papers cited in this clause did not address reliability to any significant degree, and therefore nothing appears under this topic.

5.3.7 Expectations of when the product and the associated nanoscale contacts will reach the market

No mention of any expectation of technology reaching the market was discussed in papers cited in this clause, and therefore nothing appears under this topic.

5.4 Graphene

5.4.1 General

Graphene is a single-layer of carbon atoms, discovered in 2004, and arranged in honeycomb shaped lattices. These layers exhibit some excellent characteristics, including:

– extreme strength;
– tensile modulus of 32 GPa (Anusha [2]); 100 GPa (Nayak [23]);
– breaking strength 200 times greater than steel (Anusha [2]);
– Young's modulus of 0,5 TPa (Anusha [2]);
– spring constant of 1-5 N/m (Anusha [2]);
– mean free path of ~1 μm (Nayak [23]);

- optical transparence and conductivity;
- high conductivity (both thermally and electrically);
- thermal conductivity of about (5×10^3) $Wm^{-1}K^{-1}$ (Anusha [2]);
- high room-temperature electron mobility of 10^5 $cm^2/V\text{-}s$ (Nayak [23]);
- current-carrying capacity of CNTs and GNRs of 10^{10} A/cm^2 (Nayak [23]);
- demonstration of the quantum Hall effect at much higher temperatures than silicon (Now [25])

Mullaney [21] discussed the benefits of graphene and how its properties could be “tuned” by growing it on different surfaces. When graphene is deposited on a surface treated with oxygen, graphene exhibits semiconducting properties. When graphene is deposited on a surface treated with hydrogen, it exhibits metallic properties.

Graphene at room temperature allows electrons to move essentially like photons or massless particles of light and with very little resistance. This should mean that graphene interconnects will remain cooler than a copper interconnect (less resistance, fewer obstacles, fewer electron collisions, cooler) of the same size. Cooler interconnects should improve a computer's speed and performance.

Graphene has been suggested to offer 1 million-to-1 ratios of on-to-off states in a device, which could result in a memory with 5 orders-of-magnitude more storage capacity than present day flash memories provide (Humpstonm [10]).

Graphene is a two-dimensional material, and therefore might be usable and a better alternative to 3-dimensional semiconductor devices that are being used today.

Graphene also has an extremely high surface area to mass ratio, and therefore the use of graphene in ultracapacitors is possible. Graphene ultracapacitors have been estimated to reach higher energy-storage densities than is currently available in any other known technology.

Broad market areas that will likely make use of graphene in the near future include the aerospace, automotive, electronics, energy storage, solar, oil service, and lubricant sectors. The characteristics listed above have been suggested to be excellent for applications such as micro-chips (integrated circuits), touch-screen technologies, LCD (liquid crystal display) screens, organic photovoltaic cells, organic light-emitting diodes, and solar cells. Although use in electronics is on the horizon, the near-term demand will be for composites and electrodes for applications in the automotive, plastics, metals, aerospace and energy markets (Future Markets [7]).

5.4.2 Type and configuration of the nanoscale contacts formed:

Graphene sheets will not be the normal interconnect on integrated circuits. These large sheets will need to be formed into graphene nanoribbons (GNRs). GNRs have already been shown to have similar characteristics to CNTs. Lithographic patterning of graphene can avoid CNT issues related to chirality control and alignment. In particular, the GNRs will need to have controlled edges that are typically characterized as either zigzag or armchair. These descriptors refer to the shape of the sides of the GNRs in the direction of current flow. A zigzag edge is as it sounds (using just 2 segments of the hexagon of graphene), and the armchair edge is one where the edge has 3 sides of the hexagon of graphene in it, forming what looks like an armchair.

One other type of contact on graphene that might be of interest is a doped ohmic contact. Graphene is altered when metals are attached to it. Giovanneti [8] studied the impact from many different metal contacts to graphene including Al, Co, Ni, Cu, Pd, Ag, Pt, and Au. The results showed that Co, Ni, and Pd altered graphene through chemisorption, and Al, Cu, Ag, Au, and Pt altered graphene by weak adsorption. The chemisorption process made the

contact a graphene-metal like material, with strongly perturbed energy bands. Al, Ag, and Cu shift the Fermi levels slightly making the material n-type in the vicinity of the contact. Au and Pt caused the graphene to shift to p-type material. These changes are important for making ohmic contacts, but also might be useful in trying to make p-n junctions or more complex transistors of either p-n-p or n-p-n junctions.

Although these types of doping techniques have been in the literature since 2008, there has not yet been any demonstration of diodes or transistors made with doping approaches with metals near the junctions that are formed. This implies that either the right articles have been elusive, or the technique does not port well to devices such as diodes or transistors. Much work is still left to be done to establish reliable procedure(s) for opening well defined bandgaps in graphene.

5.4.3 Requirements of the nanoscale contacts in the products:

Graphene is considered to be a potential heir to copper and silicon as the fundamental building block of nanoelectronics. To meet these high expectations, the resistance, current-carrying capability, reliability, and ability to blend the technology into mainstream IC manufacturing will all need to be achieved.

In particular, if graphene were to be used as a flexible transparent conductor in touch screens, the graphene sheets would need to be produced in very wide continuous format that could be adhered to the substrate of the screen material. Graphene would be a tremendous improvement over the present indium-tin-oxide transparent electrode that is brittle (cannot be used on a flexible substrate), and expensive (needs to be deposited in a plasma chamber in the fabrication facility over very large areas). Subbaraman [33] reported that sheets of 63 cm width of graphene on a polyester substrate (sheet) were fabricated by Samsung and Sungkyunkwan University in Korea. This is another demonstration of graphene meeting a requirement for use in real products such as touch screens.

Theoretical research work (Naeemi [22]) showed just how well graphene can perform as a GNR compared to Cu interconnect. This work looked at GNRs that were assumed to have smooth edges, which is known not to be the case. GNRs are either categorized as zigzag or armchair, as already mentioned. The conclusion of the theoretical modelling suggests that GNRs with smooth edges can have smaller resistances compared to copper wires with unity aspect ratios for widths below 8 nm. Additionally, stacks of non-interacting GNRs can have substantially smaller resistivity compared to Cu wires. Above 8 nm, Cu has lower resistance. This tends to imply that graphene interconnect might only be of value in local and short distance interconnect, and Cu would be the conductor of choice in larger and longer distance interconnect. There may be a combination of GNRs and Cu on integrated circuits in the future.

5.4.4 Fabrication technologies, processes, and process controls used to make the nanoscale contacts:

Ohmic contacts to graphene are certainly a requirement, and they must achieve low specific contact resistance. Robinson [29] reported a fabrication method that treated the graphene surface prior to deposition of electrodes of Ti/Au, Al/Au, Ni/Au, Cu/Au, Pd/Au and Pt/Au. All of these contacts produced similar specific contact resistance values of $< 10^{-7}\ \Omega cm^2$. This is a clear demonstration that high quality ohmic contacts are possible between metals and graphene.

Peterson [26] explained that adapting IC (integrated circuit) processes to graphene has been challenging. Patterning or lithography is one issue because of the very small dimensions, and because the patterning process may leave charge on the surface or edges of the patterned graphene, thus affecting its properties. Similarly, the dielectric used above or below graphene sheets has an effect on the properties, as do the metal contacts. Also, the dielectrics used might need functionalization in order to stick to the graphene.

Graphene has been explored with ICs using formation techniques such as exfoliation, decomposition of SiC, CVD (chemical vapour deposition), and reduction of graphene oxide, to

name a few. Some methods of graphene formation also require transfer of the final graphene sheet to the surface of the IC. All of these methods of formation of graphene can impact the properties due to differences in layer morphology, background doping, film stress and defectivity levels.

Peterson concludes that it may be possible for graphene to scale below present copper interconnects in terms of both resistance and reliability in CMOS circuits. However, there are still many processing challenges ahead. Since this article was given in a conference, and because it was presented by Intel, a company at the leading edge of process technology development for ICs, it is reasonable that their estimate of much work to be done is realistic.

Stan [32] discussed the fabrication of GNRs from graphene sheets. If one starts with a graphene sheet, one could pattern this using standard lithography and etching approaches found in the semiconductor industry. This would be an improvement compared to the issues common with the orientation and placement of individual CNTs in a circuit. Additionally, the width and length of a GNR could be controlled with lithographic techniques. The width of a GNR is crucial, since it will determine to a great extent the metallic character of the interconnect. These characteristics of patterned GNRs will be a step forward compared to CNTs where chirality is predetermined statistically during the manufacturing process and nearly impossible to control.

However, it should be pointed out that GNRs will not provide a cure-all solution. The width of the GNR will determine its metallic character, and a GNR can change from metallic to semiconducting just by slight changes in its width. For instance, an 11-atom wide armchair GNR would be semi-metallic, whereas a 7-atom wide armchair GNR would be semiconducting. Although these “characteristics” are cited by Stan [32] as a feature of GNRs, to control an armchair structure to be exactly 7 atoms wide, versus 11 atoms wide, is an enormous challenge. We are talking about controls in the range of 4 atoms length, a challenge for any lithography system in the semiconductor industry at present.

Moreover, it is also critical to have the GNR structures either perpendicular to or parallel to the current flow on the chips or integrated circuits. This is not trivial, unless the graphene sheets can naturally be formed with orientation automatically defined by features on the surface of the integrated circuit during fabrication. This is not addressed by Stan nor by any other paper encountered for this technical report.

Teweldebrhan [37] reports, as do many articles, that there are impacts on graphene sheets from various exposures. In Teweldebrhan, the information relates to irradiating graphene with low-energy electron beams. This transforms the graphene crystal to a nano-crystalline form and finally into an amorphous material. In this transformation, graphene changes from being a good conductor of electricity and heat to being an insulator. This change is reported here to point out that many different exposures of graphene to different conditions will lead to different results. Since the nanostructured devices are more susceptible to variations due to surface changes, it will be a long time before the manufacturing community will know exactly what to do and what not to do to keep a fabrication process under complete control. In the past, this was simpler to control, when dealing with devices larger than the nanoscale. This will be another of the many fabrication challenges in the graphene-nanotechnology arena in the future.

Brooks [3] reports on fabrication and measurement of graphene nanoribbons. In their research, graphene sheets were patterned by electron-beam lithography, followed by plasma etching to make 30 nm wide ribbons that were connected to palladium for electrical contact. They reported no measurable Schottky barrier at the contact, which likely means the ohmic contacts were of high quality. They further indicated that the resistivity of the single-layer graphene was higher than that of Cu and was higher than what was expected from a 30 nm line width of graphene.

In particular, the average interconnect resistivity measured was 71 μΩ-cm. This is compared to the bulk resistivity of Cu at 1,72 μΩ-cm, and resistivity of narrow Cu wires of 5,0 μΩ-cm.

We can see from this data that the resistivity is between 14 to 41 times more in graphene than Cu. It should be pointed out that resistivity values in the literature have reported ranges from 0,6 μΩ-cm to 200 μΩ-cm. These results do not necessarily destroy the notion of using graphene interconnect, but does show that achieving the low theoretical resistivity values will be challenging, and will take additional research. It still does appear that some demonstrations of resistivity in graphene have outperformed Cu by as much as 10 times less resistivity. This research did not dive into an explanation of the discrepancy between their experiment and theoretical predictions.

Xu [41] published studies not only into the interconnect delay expected from GNRs but how they compare to CNTs and Cu. The first items discussed in the research addressed some major issues related to using GNRs as interconnect, and many of these dealt with real, practical fabrication problems, including the following.

– GNRs have edge scattering due to their zigzag or armchair nature, and these are not considered smooth or specular edges. Scattering results in a reduction of mean-free-path and also leads to higher resistance than pure theory predicts. It is the researcher's expectation that real GNRs will not come close to theoretical predictions. CNTs on the other hand have no such scattering issues.

– Although monolayer graphene has a very large mean free path and conductivity, multi-layer graphene has a much lower conductivity per layer due to inter-sheet electron hopping. Therefore, an assumption that stacking up layers will lead to great improvement in resistivity may not necessarily be realized.

– It is known that GNRs can have either zigzag or armchair edges, and it is assumed by many researchers that one can specify the metallic or semiconducting nature of a GNR from the exact atomic width of the GNR. However, this implies that the number, N, of hexagonal carbon rings across the width of the GNR is fixed everywhere along the length (N = 3p-1 for metallic; or $N = 3p$, $3p+1$ (semiconducting); where p is an integer). This implies that for the entire length of a GNR, the edge is exactly the same atomic width and is considered smooth or very specular. However, nano-patterning to the accuracy of 1 atom is not a practical goal and simply cannot be achieved with technology available today or in the near future. Moreover, since single graphene layers will not achieve the resistivity needs for interconnect, the final interconnect will be required to have multiple layers. The specularity and edge-width control for multi-layer GNRs will be even more difficult than single-layer graphene. At this time, control of the width at the accuracy needed for use is simply not feasible. This leaves one to question the practical implementation of graphene as an interconnect in ICs.

Xu [41] summarizes his team's research in a table presenting three of the interconnects that were studied: mono-layer GNRs, neutral multi-layer GNRs and rough-edged non-specular AsF_5-doped multi-layer GNRs. All of these GNR variations produced interconnect delay at the 11 nm node that was worse than that of Copper. The researchers did conclude that both SWCNTs and smooth-edged specular AsF_5-doped multi-layer GNRs had better delay than that of Copper theoretically. This was true for both global and local interconnects. However, upon closer inspection of the improvement factor leading to the conclusion of "better delay performance," it is clear that the improvement achieved might only be a factor of 2 at best. Considering that to achieve this factor of 2 improvement will require substantial fabrication technology and that these were only theoretical calculations, it is not very encouraging that either of these interconnect schemes will lead to successful replacement of Cu at the 11-nm node. We have already cited the many issues for SWCNT interconnect. It is also important to note that achieving perfectly smooth edges in multi-layered GNRs may simply be impossible.

Standards development efforts on nano-electrotechnologies will often occur in the context of one or more of the following nano-electrotechnical business models, as described in the introduction:

– traditional;

– solution-looking-for-a-problem-or-market business model;

– penetrate existing markets.

In support of the conclusions of Xu [41], Li, Xu, Srivastava and Banerjee [14] stated that “in order to make GNR interconnects comparable with Cu or CNT interconnects, both intercalation doping and high edge-specularity must be achieved.” This means that doping of each layer of the GNR must take place with little electron interaction between adjacent graphene layers, and the edges must be very smooth. Both of these conditions, as discussed above, appear to be nearly impossible to achieve any time in the near future.

Li, Xu, Srivastava and Banerjee suggest that they felt SWCNTs and MWCNTs could provide better performance than Cu as an interconnect. However, we again point out that no researcher has presented a process of integration of such conductors into large-scale integration schemes, nor have they addressed many of the other fabrication issues that come with the use of CNTs as either a local or global interconnect.

5.4.5 Characterization techniques used to quantify a nanoscale contact

Chen [5] reports on research to characterize both CNT and graphene interconnects used to make ring oscillators. Aligned CNTs were used as local interconnect on some circuits, and 80 μm-long graphene local interconnects were also used to fabricate a 5-stage ring oscillator. These circuits both performed well in tests at frequencies similar to reference circuits made with Al interconnect. There was, however, no definitive proof that these circuits would outperform the reference circuits. The ITRS (International Technology Roadmap for Semiconductors) roadmap suggests that a carbon nanotube FET will outperform the ITRS target for the 11-nm technology node by 2-3 times. This research does not prove or disprove such a projection at this time, but does demonstrate that it will be very difficult to jump to high-density integrated circuits made with either CNTs or graphene. It is always a very large step to move from simple ring oscillators to high-density ICs with millions of transistors and interconnects over multi-layered circuits.

5.4.6 Functionality and performance of the nanoscale contacts

Sizes of sheets reported:

– 50 mm^2 (Now [25]);

– 63 cm-wide sheets of graphene on polyester sheets (Subbaraman [33]).

It has been reported that transparent conductive films from 3M have sheet resistance orders of magnitude lower than current ITO (indium tin oxide) implementations on flexible polyester substrates (3M [1]) These films include the use of graphene sheets. The reported sheet resistance of 18 Ω/square is significantly better than the ITO value of 300 Ω/square. Additionally, the transmission for the films was reported as 89,4 % for the graphene transparent film, and 87 % for the ITO film. One of the most important characteristics is the fact that the graphene material can be flexed, whereas ITO cannot. These excellent results make the graphene-based conductive films ideal for touch screens and EMI shielding applications.

Although few details have been provided by 3M on the nanoscale contacts, it appears that by screen printing 0,25 mm metal traces over the graphene material provides excellent conductivity between the macroscopic electrodes and the nano-sized graphene.

It appears that graphene is well suited for this application, and that little development of the technology will be needed to utilize this technology today.

5.4.7 Reliability of the nanoscale contacts in the product

Yu [43] performed reliability studies on graphene. There were very few researchers that have put reliability studies on their priority lists. It is believed that this is the case because researchers are still trying to validate that graphene might be a suitable replacement for scaled Cu interconnects. Yu looked at bilayer graphene and interconnects to Cu. The ultimate conclusion was that current-induced breakdown does occur at the bilayer graphene (BLG)/Cu contact. BLG was found to carry 100 times more current than Cu, and DC current-induced

thermal annealing helped to significantly reduce the contact resistance between the BLG and Cu. This again hints at the likelihood that the contact is not pristine, but is likely contaminated by at least a native oxide that inhibits current flow, but can be overcome with a reasonable amount of current. This is not a good practice to rely upon in a manufacturing environment, nor will it yield circuits with optimum performance, if any performance at all. BLG to Cu contacts must be ohmic immediately after deposition, or they will be essentially useless in an IC with high density.

Yu [43] found that two different breakdown mechanisms were active in the BLG/Cu interconnect. The breakdown mechanisms were invoked at different stressing current densities. Linear dependence of breakdown current on graphene geometry aspect ratios implies that Joule heating may be the primary breakdown mechanism in graphene. This observation contradicts the notion that electrons can flow in CNTs or graphene without collision, and therefore as “cool” carriers. Yu found that the carriers are not as “cool” as anticipated, and joule heating is a major breakdown factor.

Yu showed that before annealing, the BLG-to-Cu contact resistance was nearly infinite. Then the contacts were exposed to currents from low-voltage sweeps to 1 V for several cycles. The measured resistance was still in the G Ω range. Once the voltage sweep was raised to 3 V, the contacts exhibited nearly linear or ohmic I-V characteristics. The resistance values were in the k Ω range, indicating a drastically improved contact quality. This is however an annealing process that is not feasible for application in an IC. It is only a process that can be used with strings of BLG-Cu contacts, and only in a research exercise.

The two kinds of breakdown mechanisms observed were:

– graphene breakdown and
– graphene/Cu contact damage.

These were observed depending on the current-stressing conditions. The BLG was observed to “open” with a visible crack in the graphene layers at current densities of about 3×10^8 A/cm^2. This current density is similar to the expected breakdown observed in both CNTs and GNRs. At breakdown, the current drops to zero as the interconnect “opens.”

The second breakdown mechanism occurs at the graphene/Cu contact, and occurs at about 2×10^6 A/cm^2. This value is comparable to the electromigration limits in Cu, generally quoted at about 1×10^6 A/cm^2. It is therefore believed that the breakdown mechanism at the contact is probably related to electromigration. This second breakdown mechanism is a serious drawback, and potentially limits the graphene/Cu interconnect to a performance current that is only about what can be achieved in Cu-only interconnect.

5.4.8 Expectations of when the product and the associated nanoscale contacts will reach the market

Nayak [23] reports on many theoretical and experimental barriers that continue to exist before GNRs will become mainstream in ICs. These include:

– how resistance changes from isolated GNRs to deposited-on-dielectric GNRs;
– how different dielectrics affect GNR electrical characteristics;
– what bonding and stability exists with underlying substrates on which GNRs are put;
– which types of nano-conductors (CNTs, GNRs, or atomic wires) have the best performance on dielectric substrate materials;
– what power requirements are needed for high-performance carbon-based interconnect; and
– how packaging and thermal constraints affect GNR interconnects.

These and many other technology questions will need to be answered before CNTs, GNR, or other carbon-based interconnects become mainstream technology for ICs.

5.5 Organic devices

Burroughes et. al. [4] stated that “one of the challenges with all organic thin film transistors is to ensure a good ohmic contact between the source and drain electrodes and the organic semiconductor.” The inventor goes on to demonstrate that a silver (Ag) contact performs the worst when measuring the mobility of carriers in the transistor, and Ag contacts with TCNQ organic material doping provides higher mobility by about 1 order of magnitude, but that Ag contacts with F4TCNQ-doped organic materials provides another 2 orders of magnitude increase in mobility (cm^2/V-sec). The results depend heavily on the organic materials being used, and the doping optimization must take place with every different organic material being used in the transistor channel.

By no means was there a claim that the mobility had been optimized. This speaks to the great difficulty of making contacts to such organic materials, even when using macroscopic-sized contact areas.

It was noted that “electron transport through metal-molecule contacts greatly affects the operation and performance of electronic devices based on organic semiconductors.” (Vitali, Levita, Ohmann, Comisso, De Vita, & Kern [38]). Further it was noted that despite experimental and theoretical efforts, a clear understanding of the contact barrier at the single-molecule level is missing. This is a recognition that even in 2010, understanding of contacts in organic devices was not fully developed.

5.6 Nanoscale contacts to GaAs – Functionality and performance

Even as GaAs devices have scaled to the nanometer scale, the contacts to such devices remain in the 1 μm range. To gain true advantage, nanometer-range contacts to GaAs are needed. These contacts must have low contact resistance and must be spatially uniform at the nanometer-length scale. Research has demonstrated contacts with specific contact resistance as low as 1×10^{-6} ohm-cm^2. Lee, et al., [13] note however that these contacts are still a factor of 2-10 times higher in contact resistance compared to the best ohmic contacts to GaAs (gallium arsenide) semiconductors. Additionally, to make contacts of the quality reported, the process had to use low-temperature growth of GaAs at ~250-300 °C, which essentially dopes the GaAs surface with about $10^{20}/cm^3$ arsenic atoms. Additionally, the contacts needed to use an organic monolayer of xylyl dithiol to place a nanometer-size Au cluster on the surface. These techniques, although useful for demonstration purposes, are not suitable for large-scale manufacturing. Moreover, the electrical characteristics of the contact were investigated with an electrode tip inside a UHV STM (scanning tunnelling microscope).

To summarize the status of nanoscale contacts to GaAs from Lee's research, it can be said that the contacts performed reasonably well (although not linear as ohmic contacts should be), but they had to be processed and characterized in unique ways that do not lend themselves well to semiconductor manufacturing. It may not be possible to scale up this research technique.

5.7 Magnetic nanoscale contacts

5.7.1 Type and configuration of the nanoscale contacts formed

Researchers (Tsymbal [35]) have shown that magnetic nanoscale contacts can be formed when contact dimensions constrain the geometries and have an effect on spin transport. Magnetic domain walls are formed in some contacts. From this property, ballistic anisotropic magnetoresistance (BAMR) originates from the effect of spin-orbit interaction on ballistic conductance.

Chopra and Hua at SUNY (Johnson [11]) have demonstrated in experiments something called “ballistic magnetoresistance (BMR).” Giant magnetoresistance (GMR) read heads have

enabled hard drives to approach the theoretical limit of 20 GBits/square inch. BMR could enable much smaller domains leading to terabits/square inch. The researchers have observed a 3 000 % change in resistance in the domains.

The notion of BMR revolves around the characteristic that the electron mean free path is comparable to the length of the nanotube or nanoscale contacts formed, thus leading to ballistic motion. As noted by the researchers, “the width of a domain wall in a normal bulk conductor is about 100 nm to 200 nm, but the domain wall of a nano-contact must fit inside the nano-conductor itself. Therefore, the length of the nano-conductor is essentially the width of the domain wall – only about 1 nm.” Since a spin down must switch to a spin up condition in just 1 nm, the resistance should approach infinity, but of course is limited by non-ideal conditions and is seen as a very high resistance instead.

Tsymbal points to the many unanswered questions with this technology, citing various unknown factors:

a) nature of very small domain walls;

b) dynamics of the domain walls;

c) speed of the domain switching possible; and

d) control of morphology of nanoscale contacts as they are used over time.

It will likely be some time before the physical mechanisms of BMR are fully understood and characterized.

5.7.2 Fabrication technologies, processes, and process controls used to make the nanoscale contacts

The unique properties mentioned by Tsymbal [35] have been observed, but sufficient understanding of them and fabrication and characterization techniques will still need much development. Then useful devices based on these properties need to be realized. This area of nanoscale contacts is very immature at the present time.

6 Standardization needs to support commercialisation

Based on the analysis of the state-of-the-art in nanoscale contacts discussed in Clause 5, various key technology and standardization issues need to be addressed. There are specific areas of technology development and standardization that can support commercialization of the identified nano-enabled products cited in this TR. In general, standardization efforts should be directed, in part, at the following major topic areas:

a) Nanomaterial specifications
   - Standards need to be established to define the nanomaterials being used in a nanoscale contacts or nanoscale interconnect, and to specify the control parameters crucial to successful formation of the nanoscale contacts or nanoscale interconnects.

b) Volume manufacturing techniques
   - A standard approach to making nanoscale contacts to organic materials is needed.
   - A mass production approach for making contact to semiconducting nanowires that typically form a native oxide during any growth condition, or on exposure to oxygen atmospheres is needed.
   - Formation of $NiSi_2$ ohmic contacts to more than the (111) orientations in CNTs will need further development as formation of ohmic silicides was unsuccessful as of 2009 by Dellas [6].
   - A deterministic method of manufacturing either just metallic nanowires or just semiconducting nanowires is needed. This problem applies to both SWCNTs and MWCNTs.

- A deep understanding of all surface effects will need to be achieved before consistent manufacturing of nano-sized devices can take place. Nano-sized devices differ significantly from slightly larger devices that are not as much affected by surface conditions.

  Control of the exact width of a GNR device using lithography techniques available in a semiconducting manufacturing facility will need to be developed. This would need to be done at the atomic scale as GNR width determines metallic or semiconductor character specifically.

- Orientation of graphene sheets on the surface of a chip needs to be aligned with the patterns on the wafer. The zigzag or armchair sides of a GNR must be parallel or perpendicular to the current flow directions on the chip.
- If MWCNTs are used in vias, a method of insuring contacts to the many shells of the MWCNT both at the bottom and top of the via will need to be developed.
- If MWCNTs will be used for interconnect, the control of the diameter of the MWCNTs will need to be improved greatly, and the area coverage with MWCNTs will need to reach nearly 40 %, which is not achievable today.

c) Characterization of materials and devices

- Scanning tunnelling microscopy for studying metal-organic nanoscale contacts may need to be developed.
- Four-probe measurements for extracting resistance values for conductive nanomaterials (nanowires, nanosheets, etc.) needs to be standardized for all research and manufacturing efforts.
- Methods to extract Schottky-barrier heights on devices in a manufacturing environment, and not just for individual nanowires, needs to be developed and standardized.
- TEM (transmission electron microscopy) use for understanding the orientation and number of layers in graphene sheets must be standardized.
- Some measurement technique to accurately measure the number of graphene sheets in a structure on the surface of a semiconductor needs development and standardization.
- Some measurement technique to accurately measure the atomic width and length of a GNR needs development and standardization.

d) Methods to optimize contact resistance

- There is a need to define “current stressing,” or annealing, and to establish standards for performing this technique.

7 Summary

This technical report primarily covers CNTs and graphene used in local and global silicon interconnect schemes. There is a minor amount of coverage of other semiconductors such as GaAs and magnetic devices. The technical report will be circulated to experts to gather critical commentary. It is hoped that some of these technical experts who review the TR will also suggest additional technical experts and technical publications that could enhance the present report. There are plenty of lacunae in the TR today, and it is the intent of TC 113 to embellish this report continually with the latest information from the research and manufacturing environments. Some specific next steps are mentioned below.

Questions that arise with respect to the performance, reliability, and durability of future nanoscale devices, which depend critically on gaining atom- and molecular-level and nanoscale-level understanding of contact formation and functionality in terms of carrier transport and electrical, optical, magnetic, chemical, and mechanical properties must be addressed in the near future to accelerate adoption of nanotechnology into electrotechnical products.

The performance, reliability, and durability of future nanoscale devices depend critically on gaining atom- and molecular-level and nanoscale-level understanding of contact formation and functionality in terms of carrier transport and electrical, optical, magnetic, chemical, and mechanical properties. Many questions arise. These include:

a) How are electronic, optical, magnetic, chemical, and mechanical properties of the nano-electro-material affected by contacts?

b) How do molecules and nano-electro-materials respond when contacts are established?

c) What roles are played by the contact metal and alloys?

d) Are our theoretical understanding, computer simulations and visualization methods such that we can predict the carrier transport and electrical (DC, AC, RF, analog, digital, and mixed-signal), optical, magnetic, chemical and mechanical properties of nanoscale systems?

e) How will we separate electronic, optical, magnetic, chemical and mechanical effects and record and measure detailed changes in such effects during the formation and lifetimes of contacts?

f) How will we answer these various types of questions?

The instruments that will be used to answer these questions are expensive. Interpreting and extracting meaningful results from the large sets of data that they produce requires considerable time and expertise from many disciplines. In principle, many instruments and techniques that could provide significant insights for research, development, deployment, and high volume manufacturing of nanoscale contacts do not deliver because often the results that they give lead to inadequate correlations among properties and dynamic behaviour of contacts during formation and during their useful lifetime before failure. Standards and their associated measurements will play critical roles in enabling such validated correlations to advance innovation.

IEC/TC 113 believes that there are significant challenges ahead for the manufacture of nano-contacts and nano-interconnects. It is also believed that without a firm understanding of the science, methods and manufacturing techniques related to nanoscale contacts, useful electronic devices employing nanomaterials and nanoscale devices may be difficult to achieve. In particular, the researchers in the graphene area really need to combine their research efforts in a coordinated manner to bring the technology forward quickly, if there will be any chance to replace Cu interconnect in ICs.

- **Next steps**

1) It has been pointed out in the TR that virtually no information on nanoscale contacts and nanoscale interconnects was published related to PV products, printable electronics, batteries, and solid-state lighting. This TR needs to be enhanced by information related to products being produced in these industries. There needs to be an effort to draw out information from those companies and technical experts making such products. Also, yearly reviews of the technical literature need to be done to search for nanoscale contacts and nanoscale interconnect data related to these product areas.

2) There needs to be an increased effort by IEC/TC 113 and ISO/TC 229 to define terminology to be used consistently with nanoscale contacts and interconnects.

3) The IEC TC113 needs to define a roadmap for standardization related to characterization of nanoscale contacts and interconnects. The results of these standards would be to standardize the methods for people around the globe.

4) Technical readers of this TR should help the members of IEC/TC 113 to improve and enhance the present report for researchers globally.

5) The TR needs to be made globally available to researchers and manufacturers as soon as possible to inform the community. An attempt will be made to present the findings in this TR in a nanotechnology conference in 2013.

6) In future versions of the TR, it would be good to include comments about contacts and interconnects that are smaller than the macroscopic and microscopic contacts and interconnects primarily covered in the present TR.

7) Use the collective wisdom of several IEC National Committees and other invited international technical experts to develop a consensus on how best to begin answering the above questions a) to f).

8) Develop a systematic approach to classify the design, experimental realization and characterization of nanoscale electronic contacts for top down and bottom up nanoelectronics:

   a) integrated contacts in bulk materials (key words: top down fabrication, planar technology);

   b) molecular building blocks assembled to electrical contacts (key words: reproducible fabrication of the molecular building blocks, cleaning, separation of metallic and semi-conducting CNTs, assembling, self-assembling).

9) Develop guidelines for best practices, measurement methods, instrumentation and standards so that reproducible comparisons of the performance, reliability and durability concerning nanoscale contacts become quantitatively possible at all stages of the economic model and of the nano-electrotechnical cycle. The following two sets of stages form the context in which nano-electrotechnology stakeholders work, and have considerable overlap and many synergisms with each other.

   a) Economic model stages: The stages of the economic model that involve buyer-seller interfaces at each stage are research, development, initial deployment, commercialization (large-scale, high-volume manufacturing), end use by the customers and consumers, and end-of-life (disposing and recycling).

   b) Nano-electrotechnical cycle stages: The stages of the nano-electrotechnical cycle are raw and/or recycled materials, process, subassembly, system integration, product, end use, end-of-life (disposing and recycling).

10) Convene a workshop with breakout sessions to begin building an international agreement on action plans for addressing the kinds of questions summarized in items a) to f) above, and have the attendees determine which among the many instrumentation and theoretical approaches for eventual high-volume manufacturing of nanoscale contacts have the highest priorities for the available limited resources.

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