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INTERNATIONAL STANDARD

EMC IC modelling – Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE)





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INTERNATIONAL ELECTROTECHNICAL COMMISSION



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EMC IC MODELLING -

Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE)

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International Standard IEC 62433-2 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47A/794/FDIS	47A/799/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62433 series, under the general title *EMC IC modelling*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

EMC IC MODELLING -

Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE)

1 Scope

This part of IEC 62433 specifies macro-models for ICs to simulate conducted electromagnetic emissions on a printed circuit board. The model is commonly called Integrated Circuit Emission Model - Conducted Emission (ICEM-CE).

The ICEM-CE model can also be used for modelling an IC-die, a functional block and an Intellectual Property block (IP).

The ICEM-CE model can be used to model both digital and analogue ICs.

Basically, conducted emissions have two origins:

- conducted emissions through power supply terminals and ground reference structures;
- conducted emissions through input/output (I/O) terminals.

The ICEM-CE model addresses those two types of origins in a single approach.

This standard defines structures and components of the macro-model for EMI simulation taking into account the IC's internal activities.

This standard gives general data, which can be implemented in different formats or languages such as IBIS, IMIC, SPICE, VHDL-AMS and Verilog. SPICE is however chosen as default simulation environment to cover all the conducted emissions.

This standard also specifies requirements for information that shall be incorporated in each ICEM-CE model or component part of the model for model circulation, but description syntax is not within the scope of this standard.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967 (all parts), Integrated Circuits – Measurement of electromagnetic emissions, 150 KHz to 1 GHz

IEC 61967-4, Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω /150 Ω direct coupling method

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1

external terminal

terminal of an IC macro-model, which interfaces the model to the external environment of the IC, such as power supply pins and I/O pins

NOTE In this document, the name of each external terminal starts with "ET".

3.2

internal terminal

terminal of an IC macro-model's component, which interfaces the component to other components of the IC macro-model

NOTE In this document, the name of each internal terminal starts with "IT".

4 Philosophy

4.1 General

Integrated circuits will have more and more gates on silicon and technical progress will develop faster. To predict the electromagnetic behaviour of equipment, it is required to model the switching of the input and output interface and the internal activities of an integrated circuit effectively.

Figure 1 depicts an example of decomposition of an IC to enable conducted emissions analysis. The internal digital activity (culprit) is a source of electromagnetic noise that originates in switching of active devices. The coupling path propagates the emissions to the IC's external terminals: pins/pads. The coupling path is the power distribution network or I/O lines inside the IC.



Figure 1 – Decomposition example of a digital IC for conducted emissions analysis

4.2 Conducted emission from core activity (digital culprit)

The current transients are created in the core area on the IC-die. Due to the characteristics of the digital coupling paths, the passive distribution network on printed circuit board (PCB) and the availability of on-chip decoupling, a portion of these current transients will occur at the power supply pins of the IC.

NOTE These off-chip power supply currents can be measured according to the IEC 61967 series.

4.3 Conducted emission from I/O activity

I/Os activities may create voltage fluctuations of power and ground levels, and conducted emissions appear at power and ground pins through the I/Os' coupling path. And the output signals at output pins themselves are sources of conducted emissions to the printed circuit boards.

NOTE The measurement set-up is done according to the IEC 61967 series.

5 Basic components

5.1 General

The basic components are component parts of the IC macro-model or block component or sub-model component. The following subclauses define the basic components.

NOTE The block component and the sub-model component are defined in Subclause 6.3.1 and 6.4.1 respectively.

5.2 Internal Activity (IA)

The Internal Activity (IA) component is the electromagnetic noise source that originates in switching of active devices in the IC or in a portion of the IC. This component is applicable for both analogue and digital circuitry.

The IA is described using an independent current source or an independent voltage source with two internal terminals as shown in Figure 2.



Figure 2 – IA component

The characteristics of IA component are typically described in the time domain, and the characteristics can also be described in the frequency domain.

The description of an IA component shall contain the following information.

- Name of the IA component
- Names of its internal terminals
- Operational mode or test vector
- Domain (time or frequency)
- Definition of origin of time, and cycle-time for the operational mode (for time domain)
- Definition of origin of phase (for frequency domain)
- Operational conditions and applicable ranges
 - a) Power supply voltage ranges
 - b) Temperature range

- c) Frequency range
- Characteristics of the IA
 - a) Current or voltage waveform over the whole cycle-time (for time domain)
 - b) Current or voltage amplitude and phase, versus frequency over the whole frequency range (for frequency domain)

EXAMPLE 1

Figure 3 shows an example of characteristics of IA in the time domain. The waveform depends on the specific operational mode of function. A simple waveform such as a triangular waveform can be used for the component description.



Figure 3 – Example of IA characteristics in the time domain

EXAMPLE 2

Figure 4 shows an example of characteristics of IA in the frequency domain.





5.3 Passive Distribution Network (PDN)

The Passive Distribution Network component (PDN) presents the characteristics of propagation path of electromagnetic noises such as power distribution network (part of the PDN). The PDN can be linear or non-linear.

The PDN consists of passive elements, and is equipped with internal terminals. And the PDN can have external terminals.

The PDN can be described using a netlist. In the case the PDN can be assumed to be linear, some matrix formats such as the S-parameter can also present the PDN characteristics.

The description of a PDN component shall contain the following information.

- Name of the PDN component
- Names of its internal terminals and external terminals
- Applicable ranges
 - a) Power supply voltage range
 - b) Temperature range
 - c) Applicable load conditions if the PDN is for output
 - d) Applicable frequency range
- Characteristics of the PDN

EXAMPLE 1

Figure 5 shows an example of a four-terminal PDN using lumped elements. The ETVdd and ETVss are two external terminals of the PDN. The IT[1] and the IT[0] are two internal terminals.



Figure 5 – Example of a four-terminal PDN using lumped elements

EXAMPLE 2

Figure 6 depicts the seven-terminal PDN structure using distributed elements such as transmission lines. The ETVxx are the four external terminals, the ITVxx are two internal terminals and the ETGnd is the common ground of the four transmission lines, connected to the PCB ground.



Figure 6 – Example of a seven-terminal PDN using distributed elements

EXAMPLE 3

Figure 7 shows an example of a twelve-terminal PDN using scattering parameters in a matrix format (black box). The ET[x] are external terminals. The IT[1] to IT[6] are internal terminals. A ground plane below the modelled IC is taken as an ideal reference ground for these terminals.



Figure 7 – Example of a twelve-terminal PDN using matrix representation

6 IC macro-models

6.1 General

An IC is modelled as an IC macro-model. Three types of IC macro-models, general model, block-based model and sub-model-based model, are possible. These IC macro-models are defined in this subclause.

The description of an IC macro-model shall contain the following information for model circulation.

- Name of the IC macro-model
- Type of the model, general model or block-based model or sub-model-based model
- Names of components that are included in the IC macro-model
- Names of its external terminals
- Connections of the internal terminals of its components

6.2 General IC macro-model

The general model consists of a single PDN and one or more IAs as shown in Figure 8. The PDN shall include both the whole PDN on the IC die(s) and the whole PDN of the package. An on-chip decoupling capacitor shall also be included in the PDN if it exists.

NOTE This structure is suitable for the model circulation to IC users because of the least disclosure of proprietary information of the IC vendor.



ET[5]

IA

⊢ET[1]

ET[0]

IC model

ET[9]

ET[8]



ET[4]

Figure 8 – General IC macro-model

6.3 Block-based IC macro-model

6.3.1 **Block component**

The block component represents EMC properties of a specific functional block of IC such as embedded memory.

The block component consists of a single PDN and one or more IAs. The PDN includes PDN of the specific functional block, a portion of global power/ground network and a portion of package PDN, which are directly involved into the block's functionality. The on-chip decoupling capacitor is a part of the PDN. The component is equipped with external terminals and internal terminals.

The description of a block component shall include the following information.

- Name of the block component
- Names of the basic components that make up the block component
- Connections of the internal terminals of its basic components •

EXAMPLE 1

Figure 9 shows an example of block component. The block consists of an IA and a PDN. The internal terminals of the IA are connected to the internal terminals of the PDN.



Figure 9 – Example of block component

EXAMPLE 2

Figure 10 depicts a three I/Os model. The I/OPDN component describes how I/Os are powered and the I/OPDNA describes noise transfer characteristics among terminals. The I/OIA components describe the current activity. They are built up using two IA components; one to specify the high state behaviour and the other one to specify the low state. Figure 10 shows the two types of I/O PDN components of the complete I/O model. The IBIS model could be an implementation example.



IEC 1653/08

Figure 10 – Example of block components for I/Os

6.3.2 Inter-Block Coupling component (IBC)

The Inter-Block Coupling (IBC) is a network of passive elements that presents a coupling effect between blocks. The IBC is equipped with two or more internal terminals.

The description of an IBC component shall contain the following information.

- Name of the IBC
- Names of its internal terminals
- Applicable ranges
 - a) Power supply voltage ranges
 - b) Temperature range
 - c) Applicable frequency range
- Characteristics of the IBC

EXAMPLE

Figure 11 shows an example of IBC. The relationship between the block and the IBC is shown in Figure 12.



IEC 1654/08





Figure 12 – Relationship between blocks and IBC

6.3.3 Block-based IC macro-model structure

The block-based structure is shown in Figure 13. The model consists of block components and IBC components. The PDN of global wiring on die and the PDN on package are incorporated into the PDNs of blocks.

- NOTE 1 This structure is suitable for modelling from measurements.
- NOTE 2 By combining PDNs of block and IBCs, this structure can be converted into general structure.



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IEC 1656/08

Figure 13 – Block-based IC macro-model

EXAMPLE

Figure 14 depicts an example of block-based IC macro-model. Each block has two external terminals and three internal terminals. Three IBC blocks interconnect the internal terminals, IT2, IT3, IT4, IT5 and IT6. In this example, IBCs are used to model the substrate coupling caused by the sheet resistance between the three internal ground terminals.





Figure 14 – Example of block-based IC macro-model

6.4 Sub-model-based IC macro-model

6.4.1 Sub-model component

The sub-model in Figure 16 represents the electromagnetic behaviour of specific functional circuits of IC. An intellectual property (IP) shall be modelled as a sub-model, and some specific functional circuits such as embedded memory and CPU core can be modelled using the sub-model. The sub-model can be repeatedly used in the IC and/or other ICs.

The sub-model consists of a single PDN and one or more IAs. This PDN is a PDN of the specific functional circuits. The sub-model is equipped with internal terminals but does not have any external terminals.

The sub-model description shall contain the following information.

- Name of the sub-model
- Names of its internal terminals
- Names of the basic components that are included in the sub-model
- Connections of the internal terminals of basic components

EXAMPLE

Figure 15 shows a simple sub-model example.



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Figure 15 – Example of simple sub-model

6.4.2 Sub-model-based IC macro-model structure

The sub-model-based structure is shown in Figure 16. It consists of one or more sub-models, a PDN of die, and a PDN of package. The PDN of die includes the global power/ground network of IC die and the on-chip decoupling capacitor if it exists, but does not include PDNs that belong to sub-models. Some IAs such as IAs for standard cell circuits can be directly connected to the PDN of die (not shown in the figure).

NOTE 1 This structure is suitable for modelling using IC design information.

NOTE 2 By combining PDNs of the whole IC macro-model, a sub-model-based IC macro-model can be converted into a general IC macro-model.



Figure 16 – Sub-model-based IC macro-model

7 Requirements for parameter extraction

7.1 General

ICEM-CE model parameters can be extracted from either design information or measurements. Detailed methodology for model parameter extractions are not the purpose of this standard. This clause gives basic requirements for model parameter extractions from measurements.

NOTE Annex A gives examples of parameter extractions from design information and from measurements.

7.2 Environmental extraction constraints

The ICEM macro-model parameter extractions have to be performed under normal room temperature conditions: 23 °C \pm 5 °C. There are no additional requirements on air pressure and humidity.

When open silicon is used, the lights shall be dimmed or switched off in order not to generate photonic effects.

NOTE Some substrate materials are hydroscopic which might affect the permittivity of the material and its loss tangent.

7.3 IA parameter extraction

IA can be derived by design data or by calculating by measurements under the following conditions:

- Nominal power supply voltages and typical loadings shall be applied to the device under test.
- Input signals such as specific test vector which correspond to the specific operational mode shall be applied.

7.4 PDN parameter extraction

The PDN parameters shall be derived by analyzing impedances between the terminals under the nominal power supplies.

The derived parameters are only suited and re-useable for conducted emission simulations when the PVT (process, voltage and temperature) conditions are the same.

NOTE 1 PDN is static, but due to the N-well and gate-oxide capacitances that are involved, the power supply voltage will affect it.

NOTE 2 Most of the impedance parameters can be derived from measurements using an impedance analyzer of S-parameter VNA (Vector Network Analyser)

7.5 IBC parameter extraction

The IBC impedance can be derived from the Vdd to Vss impedance by subtracting the impedance part that belongs to the PDN. A detailed method should be elaborated in future.

Annex A

(informative)

Model parameter generation

A.1 Introduction

The purpose of this annex is to explain the methodologies used to extract the components. Three different ways are possible:

- Default parameters can be used when no other data is available.
- Parameters derived from parasitic element extractor tools, which can be used at the design phase of the IC and/or 3D electromagnetic field simulator.
- Parameters derived from measurements when the IC is already available.

A.2 Default structure and values

A.2.1 General

The PDN and IA components can be obtained using technological data coming from the IC and the packaging suppliers. The accuracy of default values is relatively low compared to values obtained by measurements or design information.

A.2.2 IA parameters

The IA structure is shown in Figure 2. It is possible to quickly determine the IA component using the technological data, which can be obtained from IC suppliers. Table A.1 shows typical values of the parameters.

As an example, for 0,5 μ m ASIC technology, cell density is around 7000. The probable number of cells in 3×3 mm² area is approximately 7,000 × 9 = 63 k gates. Considering that in average 10 % of cells are switching simultaneously, the probable CPU current at each clock edge is 63 k gates × 10 % × 0,75 mA = 4725 mA.

Technology	Year	Power	Cell density	Clock frequency	Peak gate current	Rise/Fall
CINOS		V	/mm²	MHz	mA/gate	ns
1,2µm	1985	5	1500	4 to 50	1,1	0,7
0,8µm	1990	5	4000	4 to 90	0,9	0,5
0,5µm	1993	5	7000	8 to 120	0,75	0,3
0,35µm	1995	5 to 3,3	13000	16 to 300	0,6	0,2
0,25µm	1997	5 to 2,5	18000	40 to 450	0,4	0,12
0,18µm	1999	3,3 to 2,0	22000	100 to 900	0,3	0,1
0,12µm	2001	2,5 to 1,2	28500	150 to 1200	0,2	0,07

 Table A.1 – Typical parameters for CMOS logic technologies

Table A.2 gives the default number of logic gates for typical microcontrollers.

As an example, a 16-bit RISC microcontroller is fabricated in 0,25 μ m technology. The microcontroller has approximately 15000 gates. The probable CPU current at each clock edge is 15000 × 10 % × 0,4 mA = 600 mA. The rise and fall time of the peak current is 0,12 ns.

CPU technology	Total number of logic cells	Synchronous switching on clock edge
8 bits CISC	3000 to 5000	300 to 500
8 bits RISC	3000 to 5000	300 to 500
16 bits CISC	15000 to 20000	1500 to 2000
16 bits RISC	12000 to 18000	1200 to 1800
32 bits CISC	40000 to 60000	4000 to 6000
32 bits RISC	40000 to 60000	4000 to 6000

Table A.2 – Typical number of logic gates vs. CPU technology

A.2.3 PDN parameters

The default structure of PDN is given in Figure 5.

The technological data given by the package suppliers enable to build quickly a PDN component. The typical values of the R, L and C are summarized in Table A.3. These values are used for the frequency range from DC to approximately 1 GHz.

Packag	Pin count	R	L	С	
N TYTTT	Dual in Line (DIL)	64 pins	0,025 Ω to 0,075 Ω	2 nH to 15 nH	1 pF to 10 pF
TUTTOTTOTTOTTOTTOTTOTTOTTOTT	Shrink dual in line (SDIL)	64 pins	0,025 Ω to 0,1 Ω	1 nH to 10 nH	1 pF to 10 pF
Contract Contract	Small Outline Package (SOP)	64 pins	0,025 Ω to 0,05 Ω	1 nH to 7 nH	1 pF to 7 pF
Annual Lannun	Quad Flat Pack (QFP)	400 pins	0,035 Ω to 0,55 Ω	3 nH to 7 nH	2 pF to 5 pF
	Ball Grid Array (BGA)	800 pins	0,05 Ω to 0,15 Ω	0,5 nH to 10 nH	1 pF to 10 pF
	Fine Pitch Ball Grid Array (FBGA)	1500 pins	0,05 Ω to 0,2 Ω	0,5 nH to 10 nH	1 pF to 20 pF
	Mould Chip Scale Package (MCSP)	1500 pins	0,025 Ω to 0,1 Ω	0,5 nH to 5 nH	1 pF to 15 pF

Table A.3 – R, L and C parameters for various package types

A.3 Model parameter generation from design information

A.3.1 General

ICs suppliers can extract parameters from their design information using IC design tools.

A.3.2 IA parameters

The current source is the main component in the ICEM-CE model: it summarizes the contribution of all the logic gates on the current flowing through the power supply pins of the component. The behavioural simulation is a statistical approach that could be done at the early stage of the design flow (no need of the layout for example), and could take into account a very important numbers of gates. The way to build the current source is based on a statistical evaluation of the core elements: choice of the more representative gate (the most frequently-used gate in the design), choice of the typical load of the gate. From this information, a simulation can be done at the circuit level to extract the consumption current of the typical gate. For example, in a particular 16-bit micro-controller, the most popular gate is an inverter. Figure A.1 illustrates the test schematic to define the typical current waveform.



Figure A.1 – Typical characterization current gate schematic

This example shows the description of the PDN, local and distributed on-chip decoupling networks, and the description of the IA. As the inverter has a non-symmetric structure, the current peak is not the same for the switching-on and the switching-off: the average between these two current waveforms is therefore required in the approach given in Figure A.2.



Figure A.2 – Current peak during switching transition

The second part of the methodology consists in multiplying this elementary current waveform by the number of gates that are switching at the same time. Figure A.3 illustrates this step. The aim is to obtain the number of logical nodes that change state in function of time for a given software implemented in the micro-controller. The feasibility of this operation is possible thanks to the Verilog source code, which models the micro-controller. Different types of analysis can be done, such as Best Case Simulation (BCS), Worst Case Simulation (WCS) and simulations at some corner cases of the technology.



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Figure A.3 – Example of IA extraction procedure from design

The comparison of the activity between these two cases is given in Figure A.4. The worst case peak is in fact determined to have the minimum delay in the signal propagation, and it is the opposite for the best case peak. The impact is in fact that the worst case peak presents a better synchronization of the signal and more gates are switching at the same time. The current peak is therefore sharper and the maximum value is higher than for the best case peak. The best case peak has therefore been chosen for the end of this study. In Figure A.4 the "RTL peak" item means Register Transfer Level.



Figure A.4 – Technology Influence

The final waveform corresponding to a specific internal code embedded in the microcontroller is given in Figure A.5.



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Figure A.5 – Final current waveform for a program period

The validation of this methodology has been done using the IEC 61967-4 measurement (conducted emission) on the power supply. The current has been measured through the 1 Ω resistance inserted on the ground path of the IC. The passive part of the ICEM-CE model has been obtained by the parameters by default described in Annex C. Indeed, the Test PCB has also been modelled by an RLC block using the classical formula for identifying the RLC parameters.



Figure A.6 – Comparison between measurement and simulation

It can be observed in Figure A.6 that we are able to predict the harmonic current peak up to 100 MHz. More measurements with other 16-bit micro-controllers have been done and the same results were obtained. It can therefore be considered that the simulation methodology is correct but needs improvement to extend the frequency range of validity. As far as this methodology is concerned, many approximations are performed and especially for the modelling of the interconnections, package and PCB. The need to go higher in frequency will force to use RF methods for the passive, bonding and package extraction, like presented in the previous paragraph.

A.3.3 PDN parameters

Package and Bonding wire modelling can be determined by using a 3D EM solver. From this simulation, the S-parameter file of the whole path is obtained and then is reduced to a lumped element model depending of the accuracy needed for the simulation. Another solution is to use the mathematical approach, using solvers, in order to calculate the parameters of the lumped element model directly linked to the geometry of the package. The structure of the model is given in Figure A.7 and could be reduced by one of the order reduction methods depending on the accuracy needed for the simulation.



Figure A.7 – Lumped element model of a package

The information needed to extract package and bonding parameters is listed below:

- Package mechanical drawing
- Die size and cavity size
- Bonding diagram
- Type of bonding (diameter, material)
- Distance to the ground plane

An example of a package netlist is given below.

subckt package ET0 ET1 ET2 ETn IT0 IT1 IT2 ITn gnd.				
#Definition of the	leadframe part	L		-
L1	ET0	n00	1,820e-09	
R1	n01	n02	2,408e-01	
C1	n00	gnd	1e-12	
L2	ET1	n10	1,828e-09	
R2	n11	n12	2,434e-01	
C2	n10	gnd	1e-12	
L3	ET2	n20	1,820e-09	
R3	n21	n22	2,408e-01	
C3	n20	gnd	1e-12	

K01 K12 K02	0,2597 0,1089 0,0612			
 C01 C12 C02	n00 n10 n00		n10 n20 n20	0,5e-12 0,5e-12 0,2e-12
 # Definition of wire	e bonding part			
L1wb	ET1	IT10	1.820	e-09
R1wb	IT10	IT1	2,408	e-01
L2wb	ET2	IT20	1.828	e-09
R2wb	IT20	IT2	2,434	e-01
K01wb	0,2597			
K12wb	0,1089			
K02wb	0,0612			
.ends package				

Figure A.8 illustrates the previous netlist and shows how the different elements of the package have been modelled. Some other architecture could also be taken into account, especially for the new packaging solutions.



Figure A.8 – Circuit structure of the netlist

A.4 Model parameter generation from measurements

A.4.1 IA parameters

The IA component is described by a parameter called i_A . Most of the time, this parameter is not accessible directly. The transfer function PDN (f) has already been extracted and the current flowing externally, $i_{Ext}(t)$, has been measured. Depending on which analysis is needed, i_A can be described either in the time or in the frequency domain. It also depends on whether i_{Ext} is measured in the time or the frequency domain.

• Frequency domain

 $i_{Ext}(f)$ is described in frequency and $i_A(f)$ is modelled directly by using the formula expressed in Figure A.9. In this figure it is assumed that the power-supply is equivalently shorted in the frequency band of interest.



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Figure A.9 – Principle of the IA computation

In case of multiple IAs, a matrix form can be used as shown in the following expression:

$$\begin{bmatrix} \mathbf{i}_{A[n]} \\ \mathbf{.} \\ \mathbf{i}_{A[1]} \end{bmatrix} = \begin{bmatrix} \mathsf{PDN} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{i}_{\mathsf{Ext}[n]} \\ \mathbf{.} \\ \mathbf{i}_{\mathsf{Ext}[1]} \end{bmatrix}$$
(A.1)

where PDN is the transfer function between $i_{A[n]}$ and $i_{Ext[n]}$.

• Time domain

 $i_{Ext}(t)$ is measured in the time domain and $i_A(t)$ has to be described in the time domain as well. In that case, the convolution of the discrete Fourier transform is used.

Figure A.10 shows the DFT or FFT process used to generate the IA component.



Figure A.10 – Process involved to model $i_A(t)$

First, $i_{Ext}(t)$ is measured using either the IEC 61967-4 proposal or other techniques (magnetic probe, ferrite probe ...). Figure A.11 presents an example in the time domain.





Figure A.11 – i_{Ext}(t) measured using IEC 61967-4

Secondly, a DFT of FFT is applied to convert $i_{Ext}(t)$ in the frequency domain. Thirdly, the previous expression shown above is used to compute i_A in the frequency domain. Lastly, the inverse discrete Fourier transform is applied to express $i_A(f)$ in the time domain plots $i_A(t)$ and $i_{Ext}(t)$ descriptions, see Figure A.12. It should be noted that some precautions have to be taken when a Fourier Transform or convolution process is used, to avoid altering the model with unwanted information due to the Fourier transform algorithm such as spectral leakage. The observation window has to be chosen in order to have a periodic signal. The sampling period of the oscilloscope should be adjusted to give sufficient accuracy to the Fourier Transform, depending on what is to be observed.



Figure A.12 – $i_A(t)$ and $i_{Ext}(t)$ profiles

In the case of multiple pairs of pins, the measurement can be performed separately on each pair and then added to obtain the total current. The methodology described above can be applied. The format of i_A depends on the simulation tools. A common format used by most of the tools is the ASCII format describing i_A by the frequency and its amplitude or by the time and its level.

A.4.2 PDN parameters

A.4.2.1 Overview

A vector network analyzer (VNA) and a test board are used to extract by measurement the parameters of the PDN component. The test board has to be modelled first in order to deembed the measurement and to obtain the parameters of the device. In general the impedance range of these parameters lies in the range 0,05 Ω to 500 Ω and the S11 analysis is used.

$$Z_{x} = -25 \cdot \frac{1 + S_{11}}{S_{11}} \tag{A.2}$$

Unfortunately when the S11 analysis is performed, 10 % of accuracy is obtained when the impedance range is from 5 Ω to 500 Ω , which does not match the previous requirements.

A technique [1]¹ derived from the S21 measurement is proposed in order to better match this range. Based on the knowledge of the S21 measurement, the unknown impedance can be determined using the following expression:

$$Z_{x} = 25 \cdot \frac{S_{21}}{1 - S_{21}} \tag{A.3}$$

With this technique 10 % of accuracy is reached when the impedance is in the range of 0,5 Ω to 500 Ω . If a higher accuracy is needed, a RF impedance bridge should be used.

A.4.2.2 Bias conditions

Several configurations are required to extract all the PDN parameters and it is necessary to connect the power pins to ground or to the power supply rail. To achieve that, all the PDN parameters are extracted while the power supply is maintained off. The internal decoupling capacitors (digital, analogue, I/Os...) are the sum of all parasitic capacitors of CMOS transistors and the value depends on the power supply voltage. So only these PDN parameters are extracted while the power supply is on. In general when a VNA is used, a bias tee is incorporated and the VNA supplies the power to the chip under measurement. If another measurement equipment is used, an external bias tee has to be inserted between the power supply and the device.

A.4.2.3 Measurement technique and de-embedding process

A.4.2.3.1 General

Before extracting the PDN parameters and because a hardware measurement set-up is used, a de-embedding process removes all the parasitic elements of this set-up. The hardware setup consists of measurement equipment such as a VNA, a RF impedance bridge, a measurement probe and the device as illustrated in Figure A.13.

¹ Figures in brackets refer to the Bibliography.



IEC 1672/08



A.4.2.3.2 Measurement probe, Z-Probe

The measurement probe is based on two miniature coaxial connectors as shown in Figures A.14 and A.15. A small PCB track connects both connectors to the device.



IEC 1673/08

Figure A.14 – Miniature 50 Ω coaxial connectors



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Figure A.15 – Impedance probe using two miniature coaxial connectors

The probe is calibrated using open- and short-circuit compensations as shown in Figure A.16.



Figure A.16 – Open and short terminations

Based on these two measurements the parasitic elements of this probe can be determined and finally the probe model is defined. An example is shown in Figure A.17.



Figure A.17 – Measurement probe model

A.4.2.3.3 The measurement Board, Zc

The measurement board can be modelled generally by a parasitic capacitor, which can be measured before mounting the device. Figure A.18 depicts the de-embedding principle and gives an example. The measurement in the upper left corner of Figure A.18 shows the measurement performed before the de-embedding process. The measurement in the upper right corner of the same figure shows the impedance profile after the probe measurement impedance has been removed exhibiting pure RLC impedance.



Figure A.18 – De-embedding principle

A.4.2.4 PDN parameters extraction process

A.4.2.4.1 General

The general process to build the PDN component is explained hereafter.

A.4.2.4.2 Choose the structure of the PDN

Based on the number of pairs of power pins, a predefined structure is chosen and the number of unknown parameters is determined (example: RVcc, RGnd, RAgnd, RAvcc, LGnd...). An example of predefined structure is given in Figure A.19 for a device having one pair of digital pins and one pair of analogue pins.



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Figure A.19 – Example of a predefined PDN structure

The structure of the PDN depends on the number of power pins, the technology, the size of the circuit...). The correlation between the measurement and the PDN component allows validation of the predefined structure. If the number of parameters is insufficient to correctly describe the PDN, extra elements can be added to the model.

A.4.2.4.3 Definition of the number of impedance measurements to be performed

The number of measurements to be performed is at least equal to the number of unknown parameters. Table A.4 below shows the measurement configurations used to extract the R parameters.

Measurement Configurations	VNA (S11)
ZVccGnd_0v	C=1,45 nF, L=3,25 nH, RVccGnd=1,256
ZAvccAgnd	C=687pF, L=2,8 nH, RAgndAvcc=1,63
ZAvssGnd	L=5,66 nH, RSubAVccGnd=1,12
ZAgndVcc_0v	C=1,54 nF, L=5,2 nH, RVccSubAgnd=1,66
ZAvccGnd_0v	C=689 pF, L=4,91 nH, R=2,19

 Table A.4 – Measurement configurations and extracted RLC parameters

For example:

- **ZVccGnd_0v**: ZVcc is connected to the excitation port of the Vector Network Analyzer and the Gnd is connected to the ground.
- **ZAgndGnd**: ZAgnd is connected to the excitation port and the Gnd to the ground. This configuration allows extracting the model of the IBC component.

A.4.2.4.4 Basic measurement configurations

Three basic configurations can be met during the measurement phase. The first one is depicted in Figure A.20 and is for a series inductance and resistance. At low frequencies, the resistance is dominant and gives the R parameter. At high frequencies, the inductance dominates and the L parameter can be determined using the following equation:

$$X_L = j\omega L \Rightarrow L = \frac{X_L}{j\omega}$$
(A.4)



Figure A.20 – RL configuration

Figure A.21 depicts a second configuration seen when a ground and a VCC pin are located on opposite sides and when there is no magnetic coupling between the two pins. The C parameter is determined in the low frequency range by using the following formula:

$$X_C = \frac{1}{j\omega C} \Rightarrow C = \frac{1}{X_C \cdot j\omega}$$
(A.5)

The L parameter is determined in the high frequency range by using the following equation:

$$F_R = \frac{1}{2\pi\sqrt{L \cdot C}} \Longrightarrow L = \frac{1}{(2\pi F_R)^2 \cdot C}$$
(A.6)

The R parameter is determined at the anti-resonance frequency (F_R) .



Figure A.21 – RLC configuration

The third configuration, depicted in Figure A.22, is nearly the same as the previous one except that the Vcc and Gnd pins are closer together and magnetically coupled.



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Figure A.22 – RLC with magnetic coupling configuration

The R, L and C parameters are extracted by using the same method described in the second configuration. The mutual inductance and the magnetic coupling can be determined with the following equations, assuming i1 and i2 (Figure A.23) have the same magnitude but opposite phase (true for the digital part of the IC).



Figure A.23 – Impedance seen from Vcc and Gnd

The input impedance seen across the Vcc and Gnd pins can be determined with the following equation:

$$Z1 = j(L1 + L2) \cdot \omega - j2M \cdot \omega = jLeq \cdot \omega \tag{A.7}$$

In such condition, the equivalent inductance is equal to

$$Leq = L1 + L2 - 2M \tag{A.8}$$

The mutual inductance and the magnetic coupling factor can be determined using the following formulae:

$$M = \frac{L1 + L2 - Leq}{2} \tag{A.9}$$

$$k = \frac{M}{\sqrt{L1 \cdot L2}} \tag{A.10}$$

A.4.2.4.5 Solve the equation

A mathematical solver is used to solve the equation at n=5 unknowns as it shown below.



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A.4.2.4.6 Build the PDN component

The same process is applied to extract the inductance parameters. The complete PDN component can be built (Figure A.24).



Figure A.24 – Complete PDN component

A.4.2.4.7 Choose a correlation configuration

A correlation configuration is determined to check the accuracy of the PDN component. This configuration shall be completely different from those used to extract the RLC parameters. Figure A.25 depicts an example where all the Gnd pins are connected together on a small ground plane and all the Vcc pins are connected together on a small land plane. The device is supplied with an external power supply through the VNA. The analogue power supply is performed by an independent external power supply in order to simplify the correlation process.



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Figure A.25 – Set-up for correlation (left), measurement and prediction (right)

The measurement is performed between the Vcc and the Ground plans and compared to the prediction of the PDN component. Figure A.25 shows quite a good correlation between the PDN component and the measurement.

A.4.2.4.8 Extraction of the Internal decoupling capacitors

Because these parameters vary with the power supply, the device has to be supplied to extract the internal decoupling capacitors. The device shall be supplied with the nominal power supply voltage. Figure A.26 uses the previous set-up to measure the decoupling capacitor of the digital part except that the power is maintained on. The capacitance is now doubled. Figure A.26 plots the impedances of the measurement and of the PDN simulation.



IEC 1685/08

Figure A.26 – Set-up used to measure the internal decoupling capacitor

Annex B

(informative)

Decoupling capacitors optimization

This annex presents a case study in order to show how the ICEM-CE can help to design and to optimize the decoupling network during the design phase of a complete electronic system. The value and the number of decoupling capacitors can be evaluated and determined.

Figure B.1 shows the complete electronic system builds around a power supply (Zps), a PCB (Zpcb), the ICEM-CE model of the device to decouple (Zlcemlev2) and the decoupling capacitor network (Zdec1, Zdec2 and Zdec3). Each part of this system is represented with its impedance model.



IEC 1686/08

Figure B.1 – Equivalent schematic of the complete electronic system

There are several ways to define the number and the values of the decoupling capacitors. The approach presented in this annex used the ICEM-CE model. The process recommended to define the decoupling capacitors is commented hereafter.

The frequency bandwidth of the integrated circuit has to be determined. If there is no specific requirement, a good practice is to limit the bandwidth to the tenth harmonics of the clock frequency (example: fosc = 16 MHz, bandwidth = 160 MHz) or defined by the general formula:

$$BW = \frac{0.35}{t_{rise}} \tag{B.1}$$

Maximum impedance measured at the Vdd/Vss pins of the IC has to be defined to guarantee a minimum noise level. This last parameter depends on the application and is based on the knowledge of the electronic system manufacturer. If there is no specific requirement, a good practice is to choose an impedance less than 1 Ω in the full bandwidth frequency.

The next step consists of calculating decoupling capacitors on the fundamental frequency and on the first harmonics. For example, if the clock frequency is 16 MHz and the parasitic inductance is 1 nH, the decoupling capacitor (in Farad) is determined with the following formula:

$$C = \frac{1}{(6.28 \times 16 \times 10^6)^2 \times 10^{-9}} = 10^{-7}$$
(B.2)

The values and the number are tuned based on the simulation of the model of the complete electronic system shown in Figure B.1. Without the ICEM-CE model and the other models, it is very difficult to define the decoupling network because a capacitor is not only a capacitor but an inductance and a resistance as well. Above the resonance frequency the capacitor is inductive and can cause a new resonance if there is another capacitor around. Also putting several capacitors needs to master the combination of all these resonances.

Figure B.2 shows the impedances before and after the decoupling optimization.

- ZPDN is the ICEM-CE model impedance of the device alone.
- ZVccVss is the profile impedance of the complete system before the decoupling optimization.
- ZVccVssDecMod is the total impedance of ZVccVss added to the decoupling network predicted by simulation.
- ZVccVssDecMeas is the total impedance of ZVccVss added to the decoupling network measured with the network analyzer.



Figure B.2 – Impedance prediction and measurements

Figure B.2 shows a good correlation between ZVccVssDecMod and ZVccVssDecMeas. The remaining impedance differences come from the model of C3. The parasitic inductance is more complex to model due to the geometry and technology used. This result is however far enough for this application.

Annex C (informative)

Conducted emission prediction

This annex uses the ICEM-CE model to predict the emission level according to the IEC 61967-4 proposal. Figure C.1 shows the standard test set-up used for this measurement and how the ICEM-CE of the 16-bit microcontroller is inserted in this set-up.



IEC 1688/08

Figure C.1 – IEC 61967-4 test set-up standard

The simulated spectrum is obtained according to Figure C.1 where the ICEM-CE model of the microcontroller and the IEC 61967-4 test set-up are simulated using a Spice simulator. The spectrums in Figure C.2 show the measured and simulated emissions. Thanks to the ICEM-CE model the agreement is very good up to 200 MHz. Above 200 MHz, to increase the accuracy additional information has to be added.



Figure C.2 – Comparison between prediction and measurement

Annex D

(informative)

Conducted emission prediction at PCB level

In this application, the ICEM-CE model is used to predict the level of the conducted emission measured on the Vddc at the PCB level.

Figure D.1 shows the complete description of a typical microcontroller application used to evaluate the conducted emissions. The figure illustrates the ICEM model of the microcontroller (ZIcem), the PCB model (Zpcb) and the power supply model (Zps). And the ICEM model consists of the PDN and IA components of the core and the I/Os.



Figure D.1 – Prediction of Vddc noise level at PCB level

Figure D.2 plots the measured and the predicted level of the conducted emissions. Thanks to ICEM-CE, there is a good agreement on the noise envelope. The high frequency has not been modelled due to the limitation of the measurement equipment (500 MHz); this is why the model has filtered the high frequency noise.



Figure D.2 – Good agreements on the noise envelope

Bibliography

[1] "Probes and set-up for measuring power-plane impedances with vector network analyser", DesignCon99, Istvan Novak (SUN Microsystems engineer)

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