



**JPCA**

**IEC/PAS 62326-14**

Edition 1.0 2010-09

# **PUBLICLY AVAILABLE SPECIFICATION**

## **PRE-STANDARD**



**Printed boards –**

**Part 14: Device embedded substrate – Terminology / reliability / design guide**



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INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

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## PRINTED BOARDS – Part 14: Device embedded substrate – Terminology / reliability / design guide

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| Draft PAS  | Report on voting |
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## PRINTED BOARDS – Part 14: Device embedded substrate – Terminology / reliability / design guide

### 1 Scope

This PAS is applicable to device embedded substrates fabricated by embedding discrete active and passive electronic devices into an inner layer of a substrate with electric connections by vias, conductor plating, conductive paste, and printing. The device embedded substrate may be used as a substrate to mount SMDs to form electronic circuits, as conductor and insulator layers may be formed after embedding electronic devices.

The purpose of this PAS is to obtain common understanding in design, fabrication and use of device embedded substrates in the industry.

This PAS describes the substrate embedding devices including but not limited to module, integrated passive device (IPD), microelectrochemical systems (MEMS), discrete component formed in the fabrication process of the electronic wiring board, and sheet form component. Figure 1 shows examples of device embedding in the fabrication process of the device embedded substrate. Active and passive devices are connected to each other by interlayer vias and/or conductor patterns. Insulating layers are formed using insulating materials with vias for the connection of inside conductor patterns to the conductor patterns formed on the surface(s) of the substrate. Figure 2 shows the substrate with connections using pads, and Figure 3 shows the board using via connections.

The insulating layer includes rigid and flexible insulating resins such as phenol resin, epoxy resin, polyimide resin and modified polyimide resin, which are reinforced with glass cloth, aramid cloth or paper; and resins without reinforcement. Interconnections to the input and output terminals to the embedded device and the surface conductor pattern include conventional interconnection of the terminals of the embedded device to an interconnecting land for SMD, and formation of terminals on the surface of an embedded device by copper plating or vias using conductive paste.

This PAS does not specify the fabrication process of device embedded substrates, via diameter/via land diameter, conductor width/conductor spacing nor conductor line density.

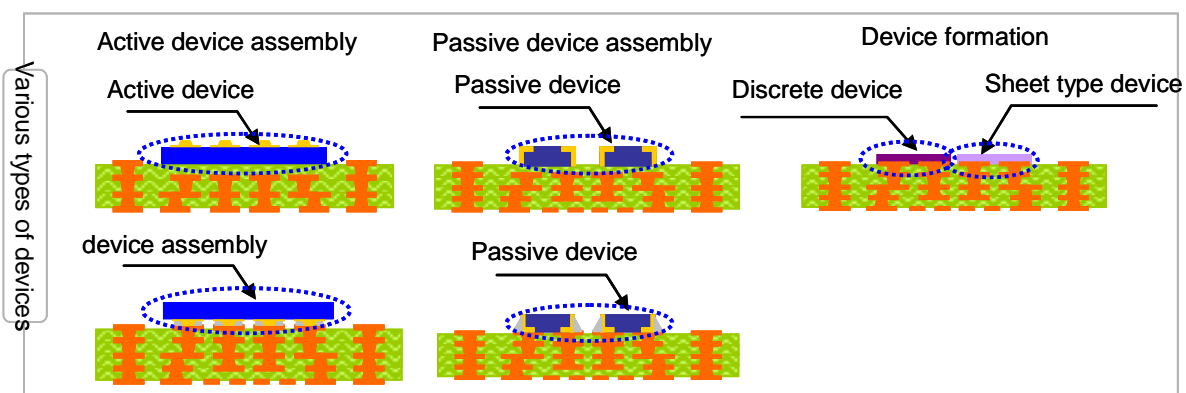


Figure 1 – Examples of device embedded substrate

### 2 Normative references

Void

### 3 General definitions

#### 3.1 Technology of the device embedded substrate

There are two types of device embedded substrates: one type consists in embedding an active and/or passive discrete device on a base substrate and covering it with organic resin and the other consists in forming a device on a substrate and then covering it with organic resin. The device embedded substrate also includes composite type substrates which consist of mass produced inorganic ceramic including LTCC (low temperature co-fired ceramics) substrates (hereafter they are called just ceramics) on which passive devices are embedded as shown in Figure 4, and the other type as shown in Figure 5 where the ceramic substrate is used as a base on which active and passive devices are mounted and the entire body is covered by organic resin; details of inorganic ceramics are not specified in this document. Such a ceramic is treated just handled as a base of a device embedded module.

Classification of device embedding is given in Table 1. Active devices include bare die, wafer-level package (WLP), BGA, LGA, and QFN. Passive devices include chip component, complex chip component like an array and integrated passive device (IPD). Module and MEMS are embedded onto the substrate after packaging and moulding into module and MEMS. The component formed during substrate formation is not covered in this document but also included in Table 1. There are two types of formed passive component embedding, one is to form passive components using thick film or thick film technology on the base of a silicon or compound semiconductor and/or on the stacked chip at the wafer level or on package-on-package (PoP), and the other is to use a sheet-type passive device on an organic substrate first and then to embed the other devices.

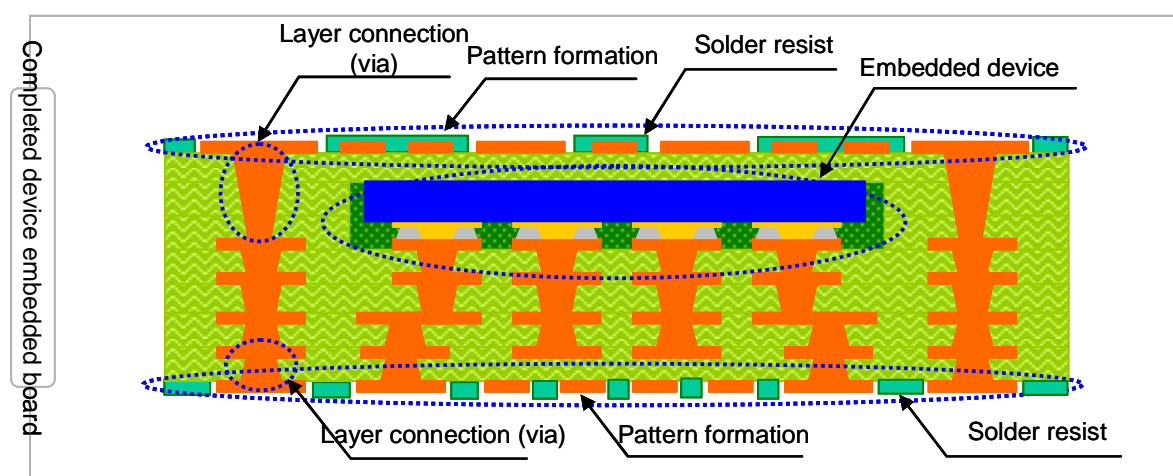


Figure 2 – Completed device embedded substrate (pad connection)

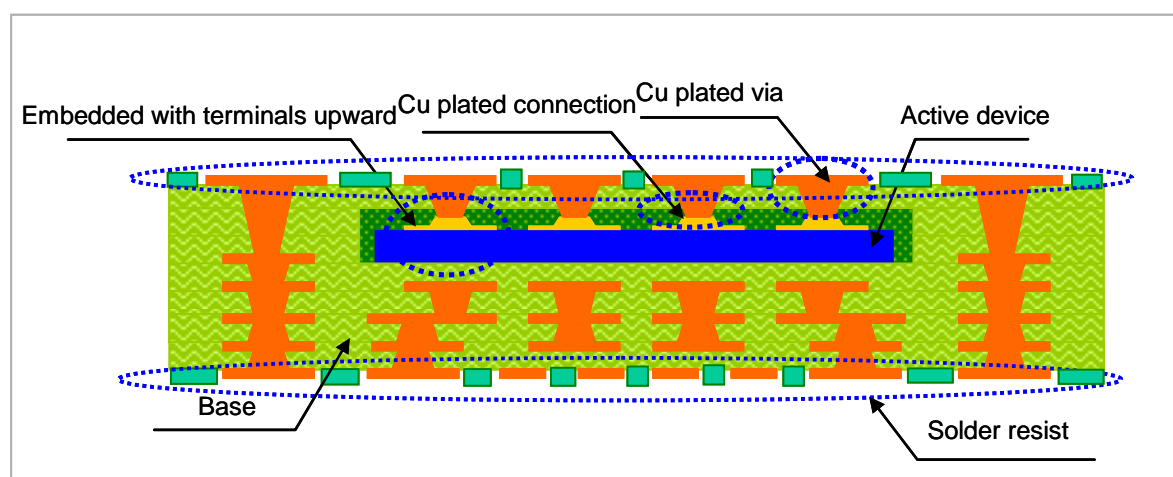
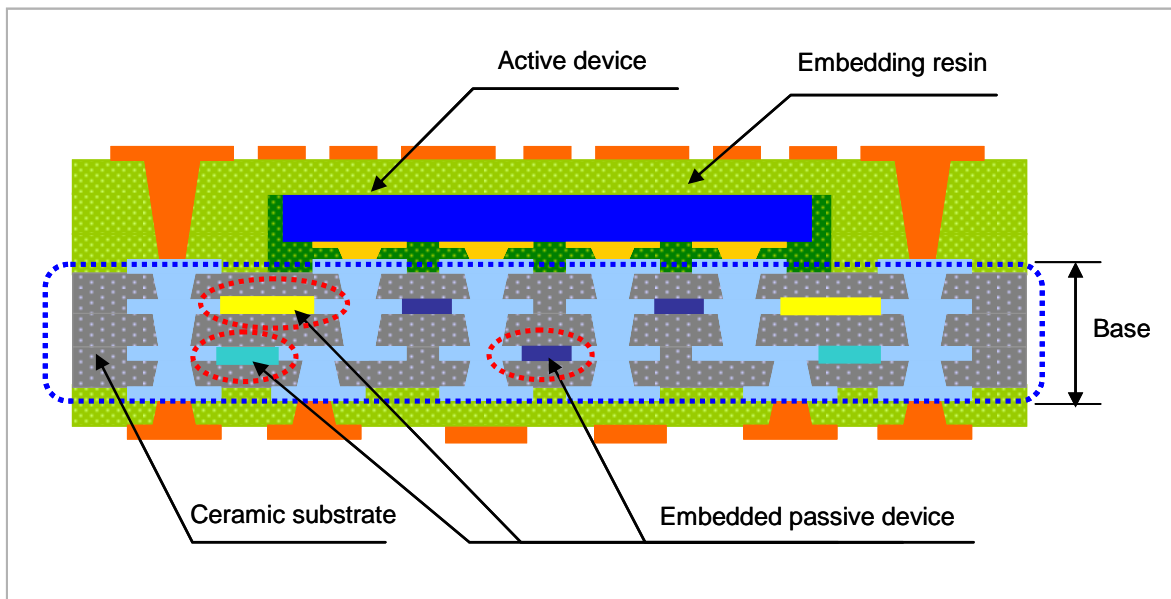
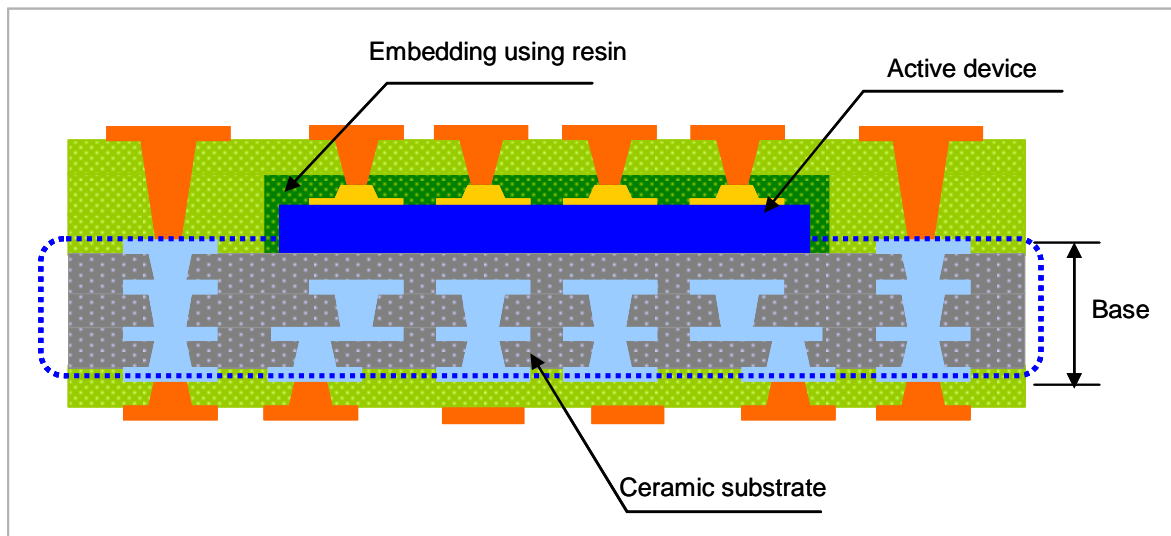


Figure 3 – Completed device embedded substrate (via connection)








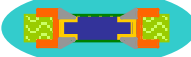












**Figure 4 – Structure of a device embedded substrate using a passive device embedded substrate as a base and then a active and/or a passive device is mounted and then covered by resin (Pad connection type)**







**Figure 5 – Structure of a device embedded substrate using a ceramic board as the base (via connection type)**

**Table 1 – Classification of device embedding**

| Classification | Item                      | Embedding         | Device terminals                  | Bonding                         | Schematics  |
|----------------|---------------------------|-------------------|-----------------------------------|---------------------------------|---|
| Active device  | Bare die                  | Die bonding       | Peripheral                        | Wire bonding                    |    |
|                |                           | Flip chip bonding | Peripheral area array             | Flip chip bonding               |    |
|                |                           | Die bonding       | Peripheral area array             | Via connection (plating, paste) |    |
|                | Wafer level package       | Mounting          | Peripheral area array             | Soldering conductive paste      |    |
|                |                           | Die bonding       | Peripheral area array             | Via connection (plating, paste) |    |
|                | Package                   | Mounting          | BGA, LGA, QFN                     | Soldering conductive paste      |    |
|                |                           | Mounting          | BGA, LGA, QFN                     | Via connection (plating, paste) |    |
| Passive device | Chip component            | Mounting          | Rectangular chip<br>Rod type chip | Through hole                    |    |
|                |                           | Mounting          | Rectangular chip<br>Rod type chip | Soldering conductive paste      |   |
|                |                           | Mounting          | Rectangular chip                  | Via connection (plating, paste) |  |
|                | Module chip component     | Mounting          | Rectangular chip                  | Soldering conductive paste      |  |
|                |                           | Mounting          | Rectangular chip                  | Via connection (plating, paste) |  |
|                | Integrated passive device | Mounting          | IPD                               | Soldering conductive paste      |  |
|                |                           | Mounting          | IPD                               | Via connection (plating, paste) |  |
| Module         | Packaging and moulding    | Mounting          | Arbitrary                         | Soldering conductive paste      |  |
|                |                           | Mounting          | Arbitrary                         | Via connection (plating, paste) |  |
| MEMS           | Packaging and moulding    | Mounting          | Arbitrary                         | Soldering conductive paste      |  |
|                |                           | Mounting          | Arbitrary                         | Via connection (plating, paste) |  |

**Table 1 – Classification of device embedding** *(continued)*

| Classification | Item   | Embedding                     | Device terminals          | Bonding                            | Schematics  |
|----------------|--------|-------------------------------|---------------------------|------------------------------------|---|
| Active device  | Formed | Thin film<br>Sputtering       | Silicon                   | Via connection<br>(plating, paste) |  |
|                |        | Thick film<br>Screen printing | Semiconducting<br>polymer | Via connection<br>(plating, paste) |  |
| Passive device | Formed | Double through<br>hole        | Copper plating            | Via connection<br>(plating, paste) |  |
|                |        | Etching                       | Laminate<br>material      | Via connection<br>(plating, paste) |  |
|                |        | Etching                       | Film                      | Via connection<br>(plating, paste) |   |
|                |        | Screen printing               | Polymer                   | Via connection<br>(plating, paste) |   |
|                |        | Transfer                      | Ferromagnetic<br>Ceramics | Via connection<br>(plating, paste) |   |
|                |        | Lamination                    | Seeding                   | Via connection<br>(plating, paste) |   |
|                |        | Spin coating                  | Polymer                   | Via connection<br>(plating, paste) |   |

### 3.2 Substrate

Structures and fabrication processes of device embedded substrates are illustrated in Table 2. A base substrate is necessary for the device embedded substrate to embed active and passive devices. Most of the base substrates are multilayer substrates and build-up substrates, but an insulating resin board, insulating sheet, metal sheet or film carrier can certainly also be used. Table 2 shows the method to embed the active or passive device and then connect the device to the surface conductor by vias made of copper plating and conductive paste and checking items during the fabrication process.

This document, however, does not cover active devices formed on a silicon interposer, a compound semiconductor substrate or a printed wiring board and passive device (resistor, capacitor or inductor) but it does cover inductors formed together with a conductor pattern and capacitor in its structure.

**Table 2 – Embedded device structure and fabrication process**



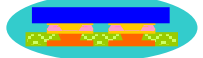











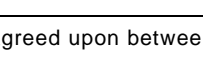



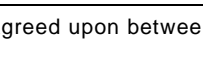
| Process | Item                                  | Structure   |                | To check  |
|---------|---------------------------------------|-------------|----------------|---|
|         |                                       | Pad bonding | Via connection |   |
| 1       | Base                                  |             |                | Opening, short  |
| 2       | Mounting                              |             |                | Position accuracy   |
| 3       | Pad bonding                           |             | —              | Connection, conduction  |
| 4       | Embedding                             |             |                | Microvoid<br>Board thickness<br>Flatness                      |
| 5       | Via hole                              |             |                | Hole position<br>Terminal position<br>Resistance to chemicals |
| 6       | Via hole                              | —           |                | Thicknesses of Cu plating & conductive paste<br>Micro void    |
| 7       | Pattern formation (multi-layer)       |             |                | Open, short   |
| 8       | Surface treatment (solder mask, etc.) |             |                | Observation   |

### 3.3 Jisso mounting and interconnection

There are two types of terminal connections; one is to connect terminals of an embedded device to connecting pads formed on the base, and the other is to form connecting vias on the device after embedding. The device is connected to the pads on the base using conventional semiconductor and SMD mounting techniques and then the device is embedded. The device is connected to the conductor pattern in the second case after embedding by copper plating or conductive paste.

Both of the device mountings can be classified into die-bonding and mounting methods as shown in Table 3.

**Table 3 – Jisso mounting and interconnection of the device embedded substrate**

| Jisso mounting   |                  | Device                    | Interconnection             |                                     | Structure   |  |
|--|------------------|---------------------------|-----------------------------|-------------------------------------|---|--|
|  |                  |                           | Process                     | Interconnection                     |   |  |
| Pad bonding  | Die bonding      | Chip                      | Wire bonding                | Wire melt-connection                |    |  |
|  |                  |                           | Flip-chip bonding           | Metal bonding<br>Contact connection | Metal bonding<br><br>Contact<br>          |  |
|  |                  | Mounting                  | Wafer level packaging (WLP) | Reflow<br>Polymer bonding           | Soldering<br>Conductive paste   | Soldering<br><br>Conductive paste<br>          |
|  | Package          |                           | Reflow<br>Polymer bonding   | Soldering<br>Conductive paste       | <br>Conductive paste<br>                 |  |
|  | Rectangular chip |                           | Reflow<br>Polymer bonding   | Soldering<br>Conductive paste       | Soldering<br><br>Conductive paste<br> |  |
|  | Rod-type chip    |                           | Reflow<br>Polymer bonding   | Soldering<br>Conductive paste       | <br>Conductive paste<br>              |  |
|  | Module           |                           | Reflow<br>Polymer bonding   | Soldering<br>Conductive paste       | Soldering<br><br>Conductive paste<br> |  |
|  | MEMS             |                           | Reflow<br>Polymer bonding   | Soldering<br>Conductive paste       | <br>Conductive paste<br>              |  |
|  | Via bonding      |                           | Die bonding                 | Chip                                | Via connection  | Copper plating<br>Conductive paste   |
|  |                  | Wafer level package (WLP) |                             | Via connection                      | Copper plating<br>Conductive paste  | <br>Conductive paste<br>                   |
|  |                  | Mounting                  | Package                     | Via connection                      | Copper plating<br>Conductive paste  | Copper plating<br><br>Conductive paste<br> |
|  |                  |                           | Rectangular chip            | Via connection                      | Copper plating<br>Conductive paste  | Copper plating<br><br>Conductive paste<br> |
|  |                  |                           | Rod-type chip               | Via connection                      | Copper plating<br>Conductive paste  | <br>Conductive paste<br>                   |
|  |                  |                           | Module                      | Via connection                      | Copper plating<br>Conductive paste  | <br>Conductive paste<br>                   |
|  |                  |                           | MEMS                        | Via connection                      | Copper plating<br>Conductive paste  | <br>Conductive paste<br>                   |
| NOTE The shape and surface treatment of the terminals of the embedding device should be agreed upon between the user and the supplier of the device. |                  |                           |                             |                                     |   |  |



### 3.4 Structure and terminology

#### 3.4.1 General

Figure 6 shows each section of the device embedded substrate and its name. See JPCA-TD01-2008, Terms and definitions in electronic circuits, and JIS C 5603, Terms and definitions in printed wiring boards. The number of layers is counted after completion of the device embedding as L1, L2 ~ L6 (in case of 6 layers) from the top layer.

The structure of the device embedded substrate is illustrated by means of the structure of the build-up substrate. See JPCA-BU01-2007, Build-up wiring board (Terms and test methods). Figure 7 shows the typical structure of the base and Figure 8 the cavity structure. Other structures are shown in Figure 9 with the insulating base, in Figure 10 for the base using a conductive carrier or a metal sheet. Figure 11 shows the structure of the device embedded ceramics and Figure 12 shows the standard ceramic board as the wiring board base.

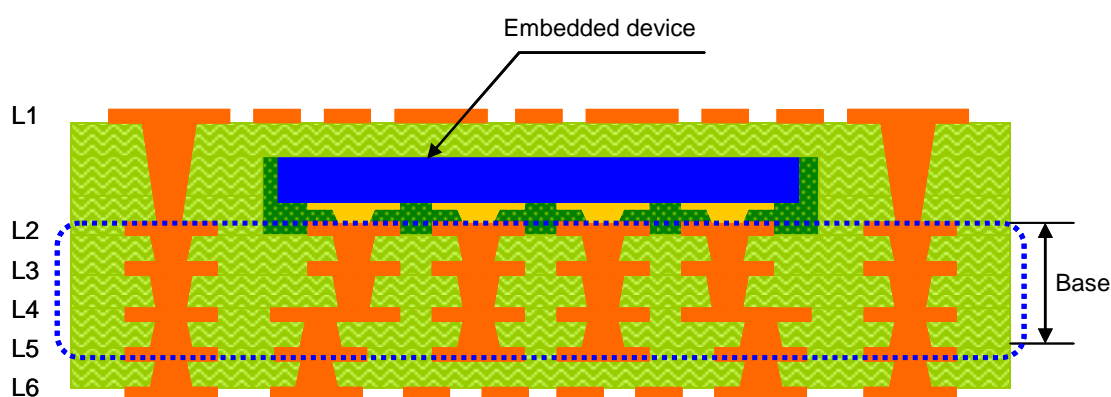


Figure 6 – Entire structure of device embedded substrate

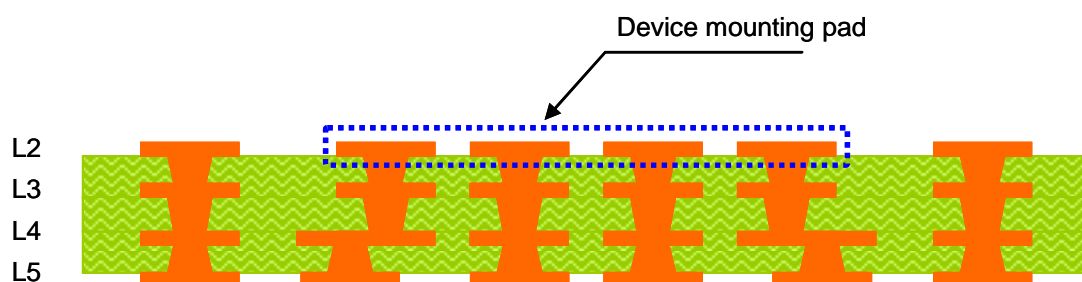


Figure 7 – Base (typical structure)

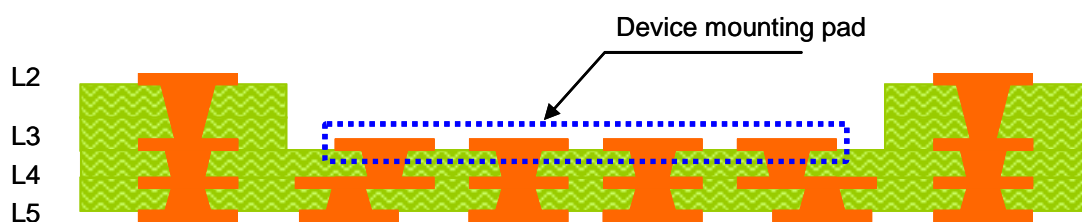
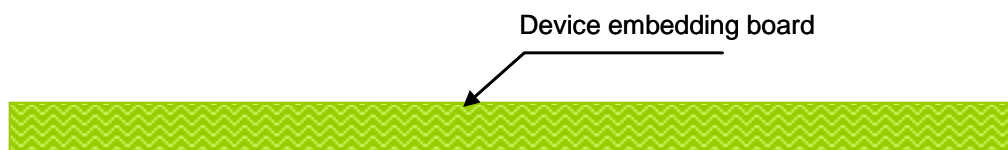


Figure 8 – Base (Cavity structure)

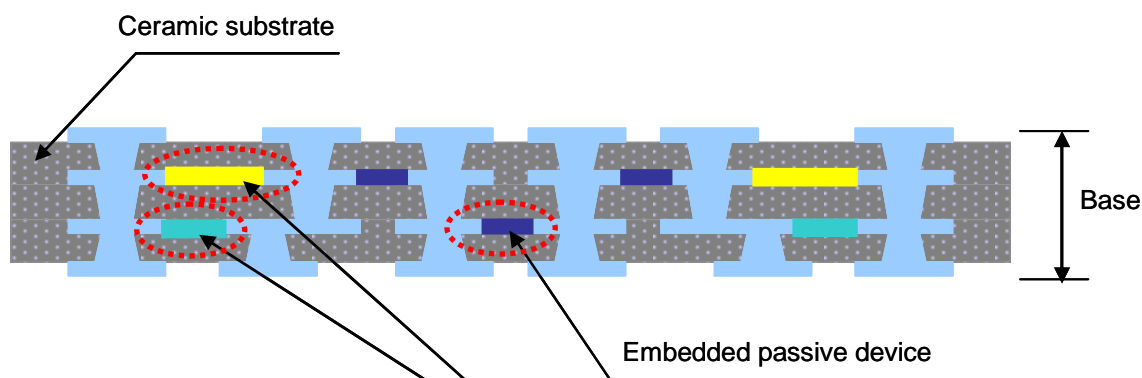


\* Used for terminal connection in electronic circuit board

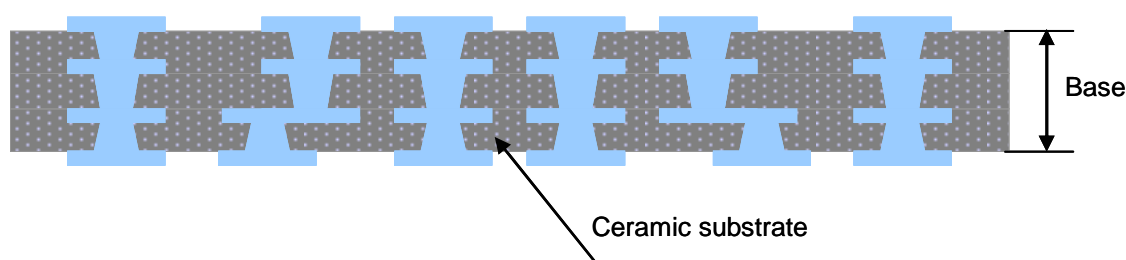
**Figure 9 – Base (insulator)**



**Figure 10 – Base (conductive carrier – metal plate)**



**Figure 11 – Passive device embedded ceramic substrate used as a base**



**Figure 12 – Ceramic board used as base**

Figure 13 to Figure 19 show various cases of device embedding in conventional mounting technique, electric connection after embedding various types of devices, embedding device over more than one layer, device embedding with resin base, and use of conductor layer and metal sheet/copper foil.

### 3.4.2 Device embedding by conventional process

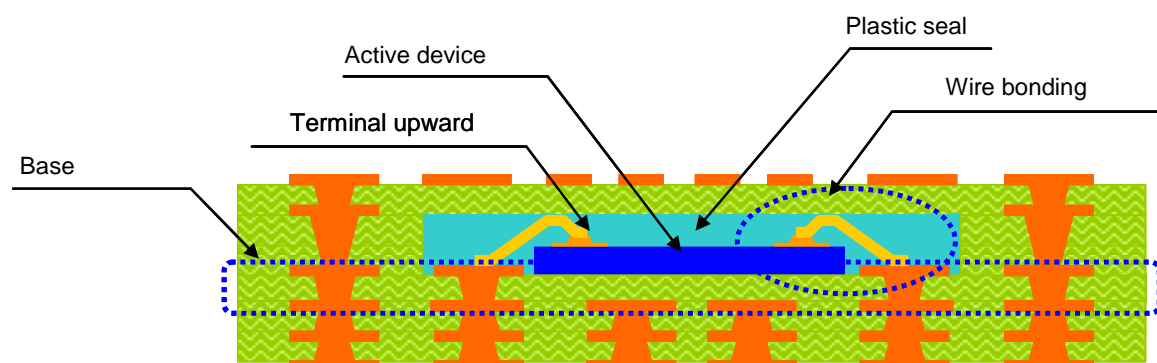


Figure 13a – Wire bonding connection and embedding of active device bear chip

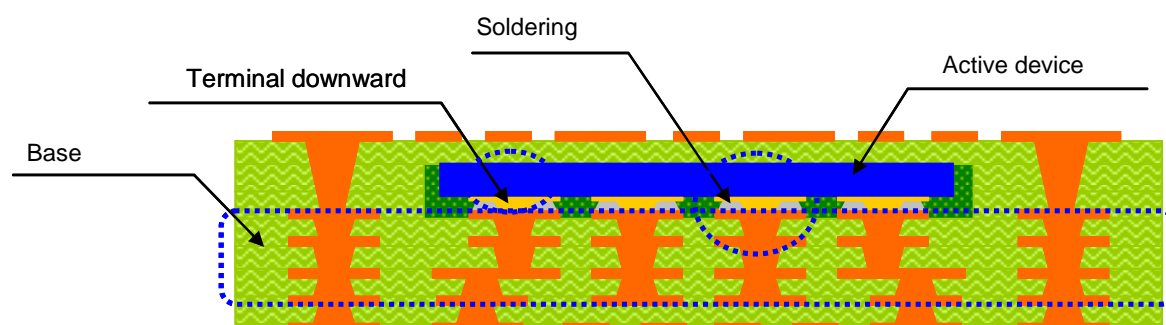


Figure 13b – Soldering connection and embedding of active device

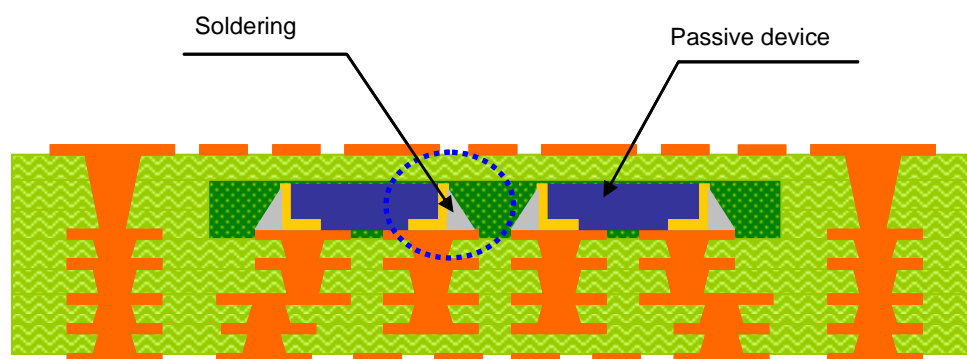


Figure 13c – Soldering connection of square type passive device

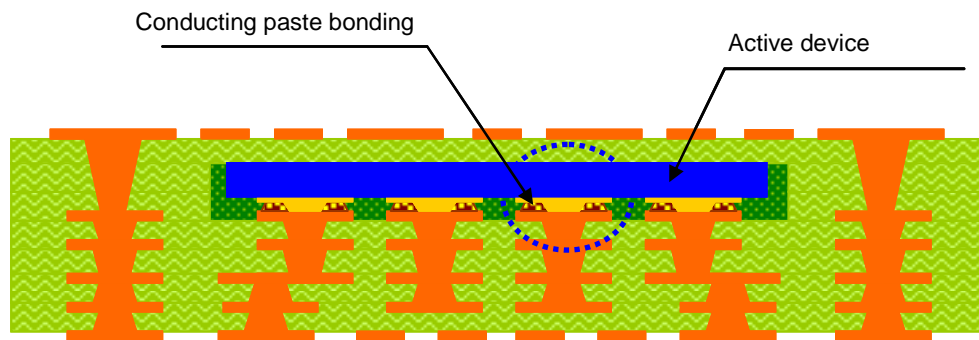


Figure 13d – Conductive resin connection and embedding of active device

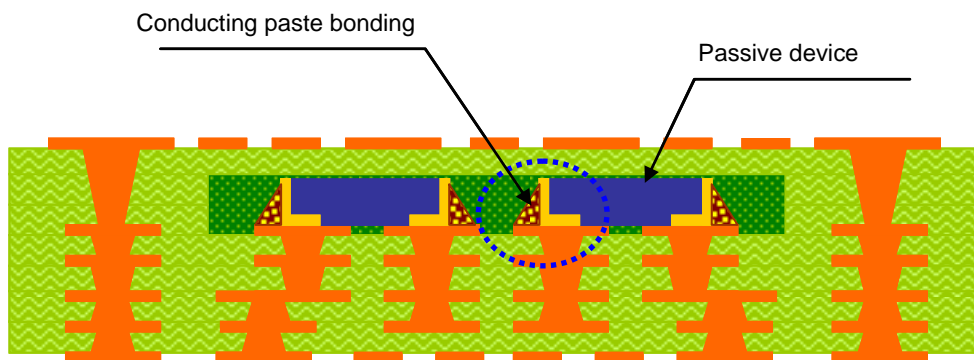


Figure 13e – Conductive resin connection and embedding of square type passive device

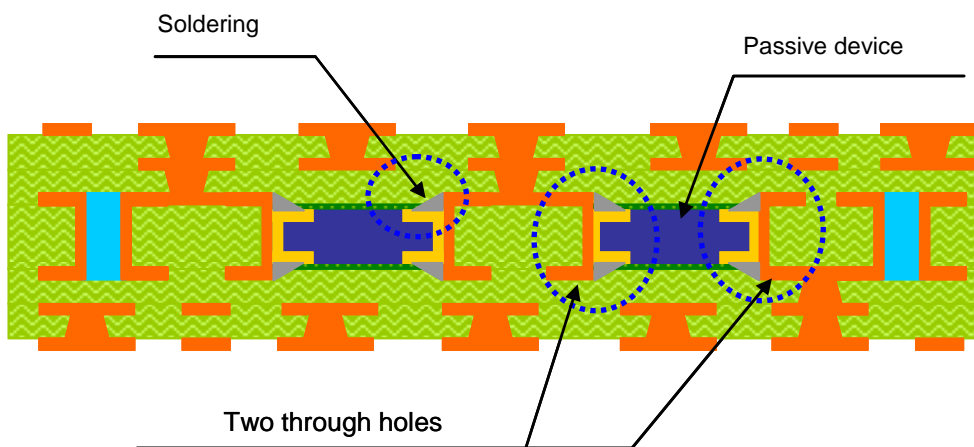


Figure 13f – Soldering connection into through hole and embedding of passive device

Figure 13 – Embedding of device by conventional methods

### 3.4.3 Electrical connection by vias after device embedding

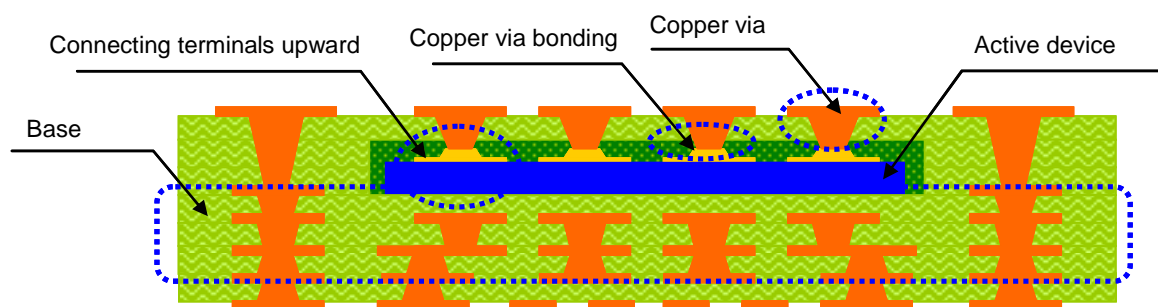


Figure 14a – Connection by Cu plating after embedding of active device



Figure 14b – Connection by Cu plating after embedding of square type passive device

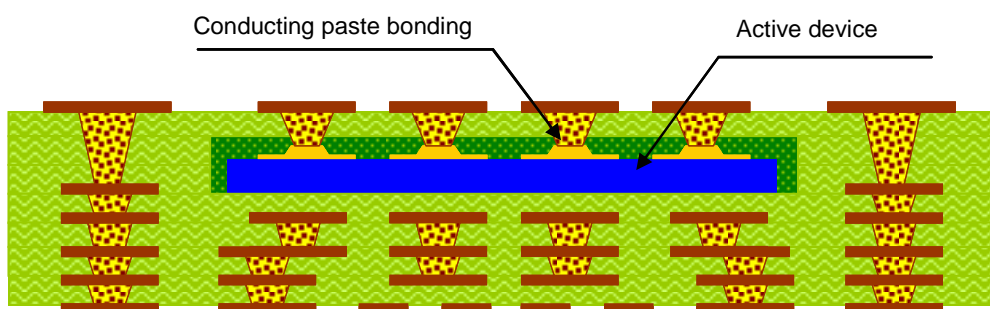


Figure 14c – Conductive paste connection after embedding of active device package

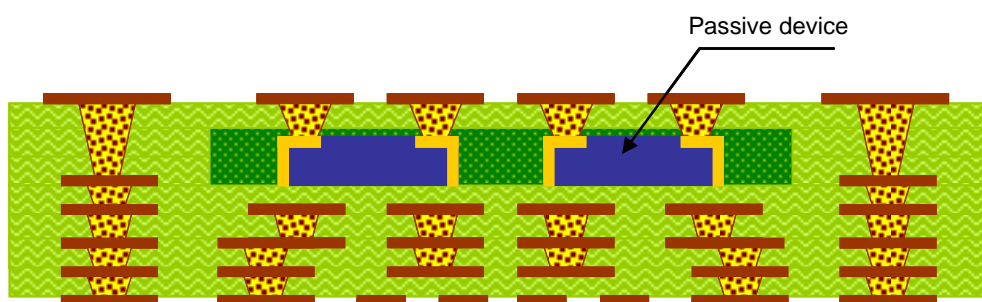


Figure 14d – Conductive paste connection after embedding of square type passive device chip

Figure 14 – Via connection after embedding

### 3.4.4 Embedding of various devices over multiple layers

#### 3.4.4.1 Device embedded substrate of device embedding in multi-layers

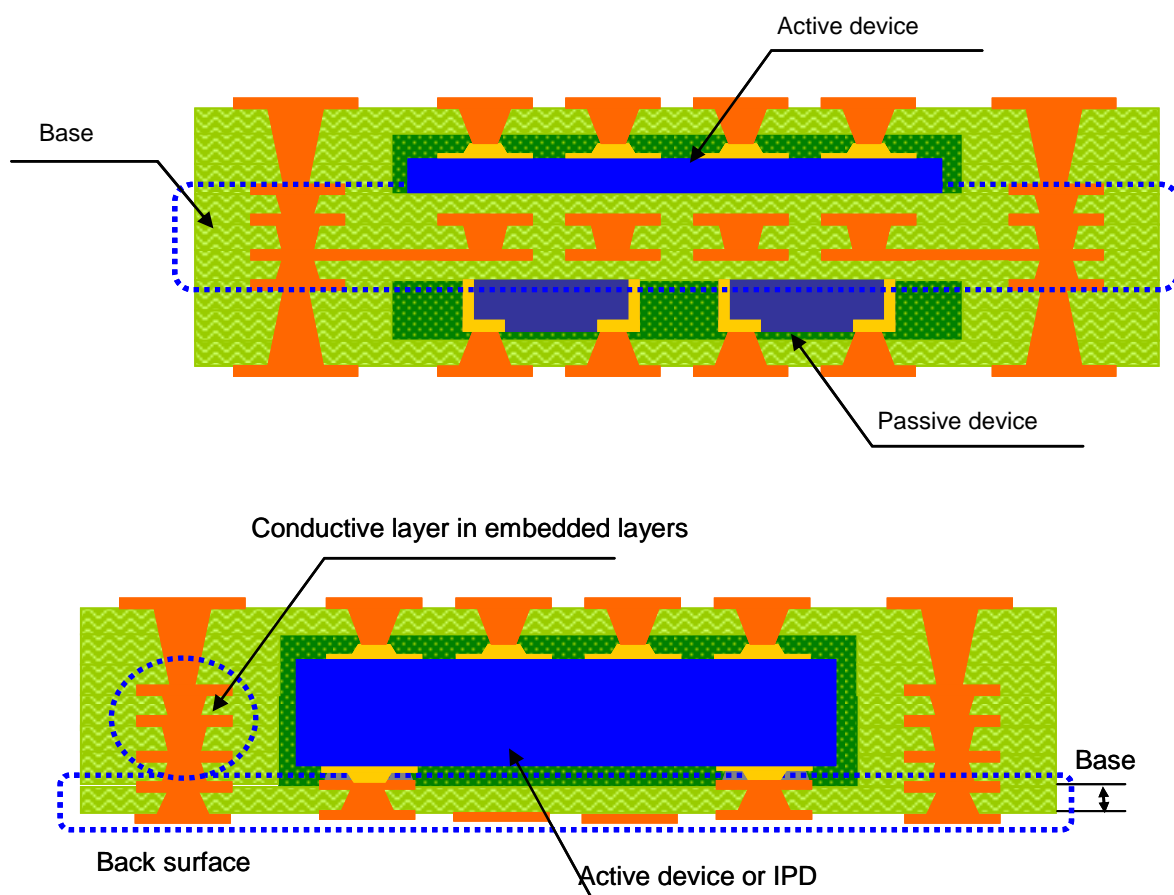


Figure 15 – Embedding of devices over multiple layers

#### 3.4.4.2 Embedding of various devices onto resin base substrate

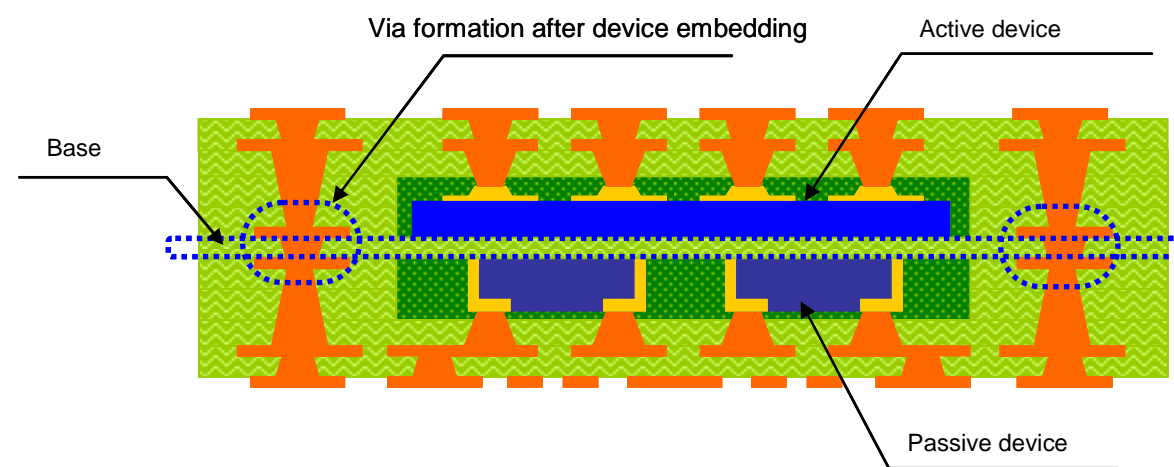


Figure 16 – Resin base substrate

### 3.4.4.3 Device embedding using conductor and metal sheet/copper foil base substrate

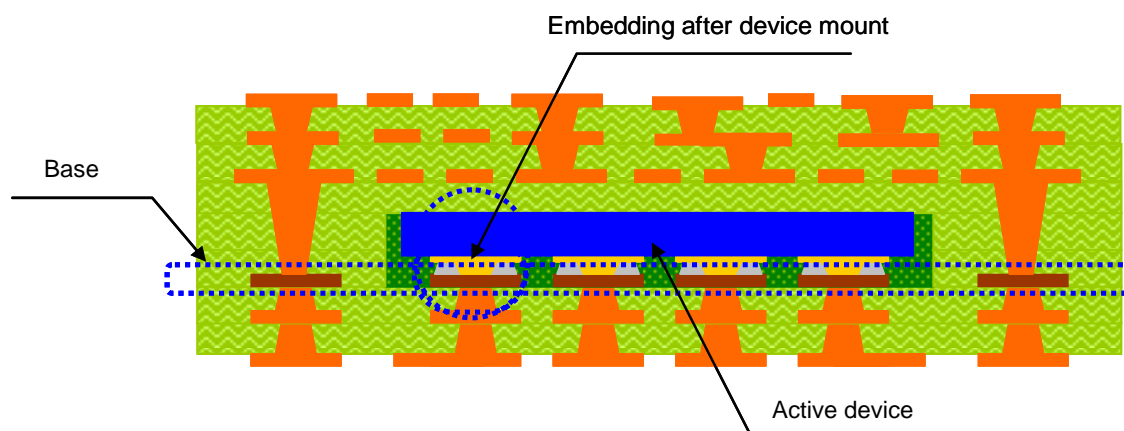


Figure 17 – Conductor and metal sheet/copper foil as the base substrate

### 3.4.4.4 Ceramic and resin composite device embedded substrate using passive device embedded ceramic substrates as the base

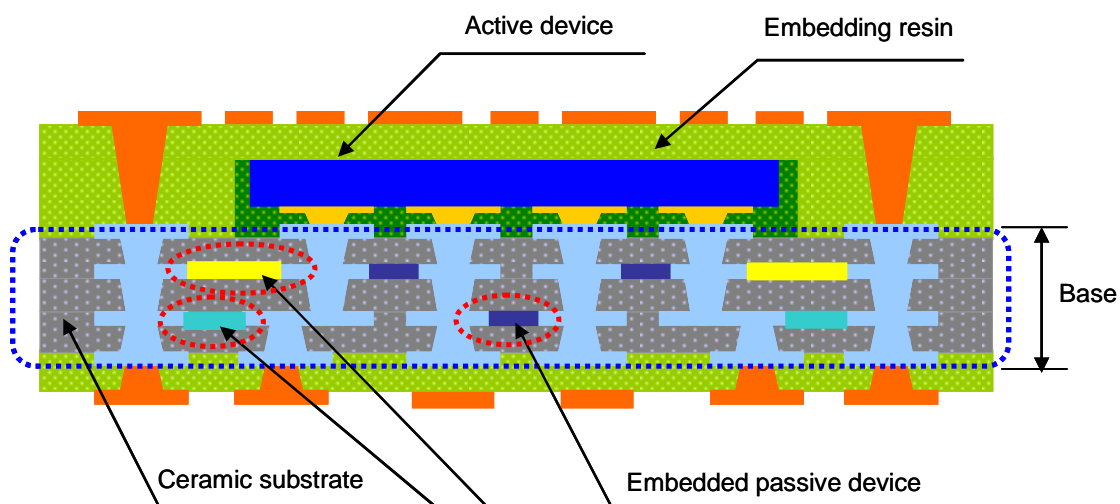


Figure 18 – Device embedded substrate using passive device embedded ceramic substrates as the base

### 3.4.4.5 Device embedded substrate using ceramic and LTCC substrates as the base (including ceramic and LTCC substrates which do not embed passive devices)

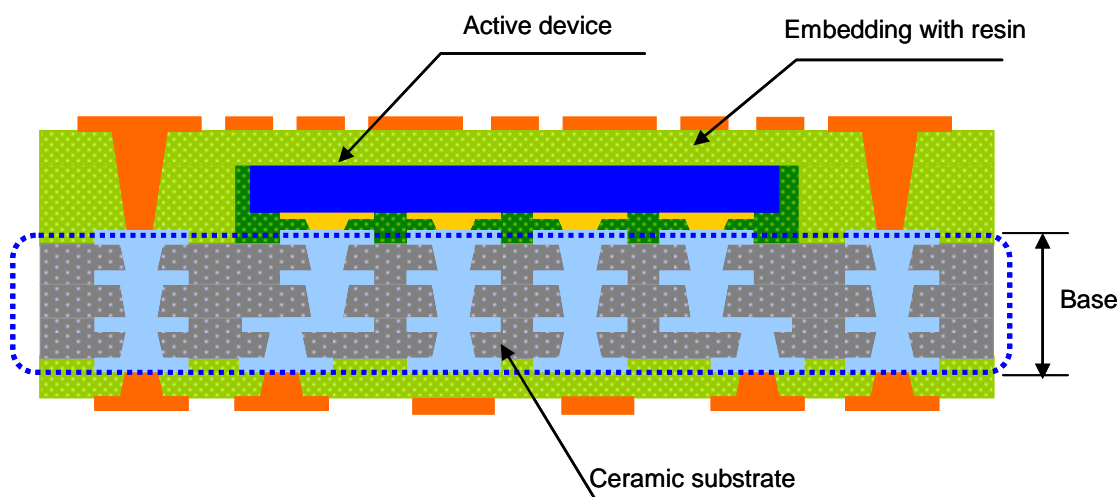


Figure 19 – Device embedded substrate using passive device embedded ceramic substrates as the base – second type

## 4 Test methods

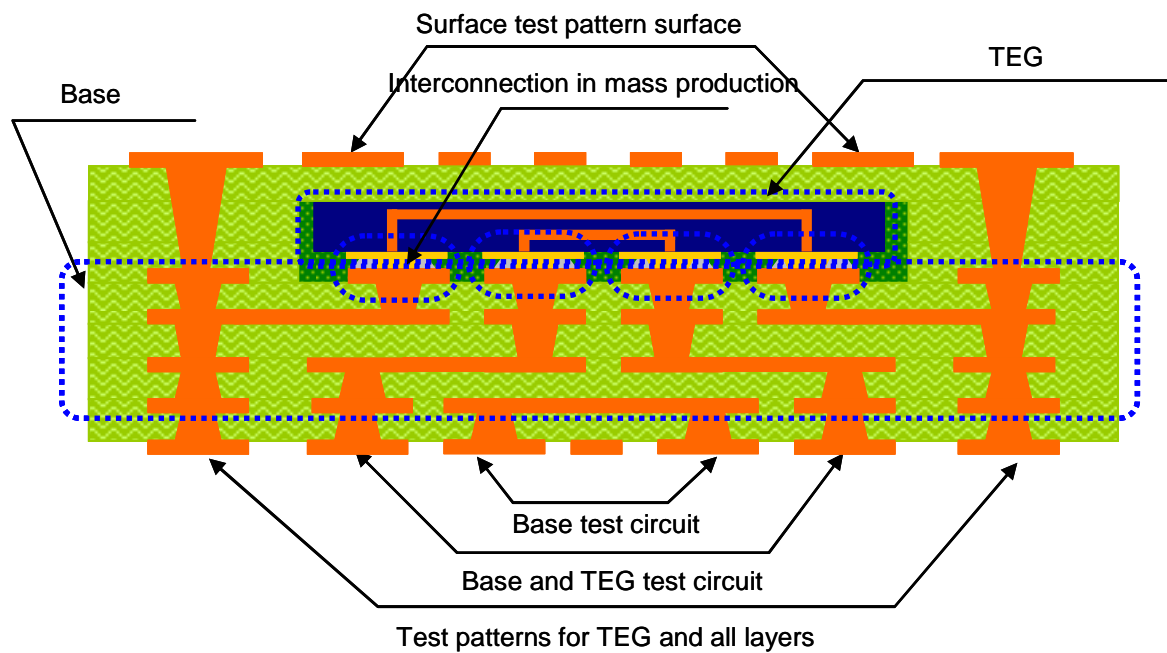
### 4.1 General

The test methods for the un-embedded board are those for the board itself. The specifications and test methods for the embedded board are for the embedded board only and not for the embedded device. It is recommended to evaluate a TEG mounted board (test element group) to obtain assembly condition and library data for design. The TEG is less expensive than actual embedding semiconductor devices and can provide necessary technical data easily. Guarantee of reliability of a product shall be agreed between user and supplier. Embedding of device into board shall also be agreed upon between user and supplier basically based on the statement given in this document.

### 4.2 Structure of TEG (Test Equipment Group – Test vehicle)

A schematic diagram of TEG is shown in Figure 20 for the evaluation of the conductor pattern on the base of a board, the interconnection between the base and the test specimen and the conductor pattern on the board surface. The characteristics of the device embedded board and test equipment shall also be agreed between user and supplier.





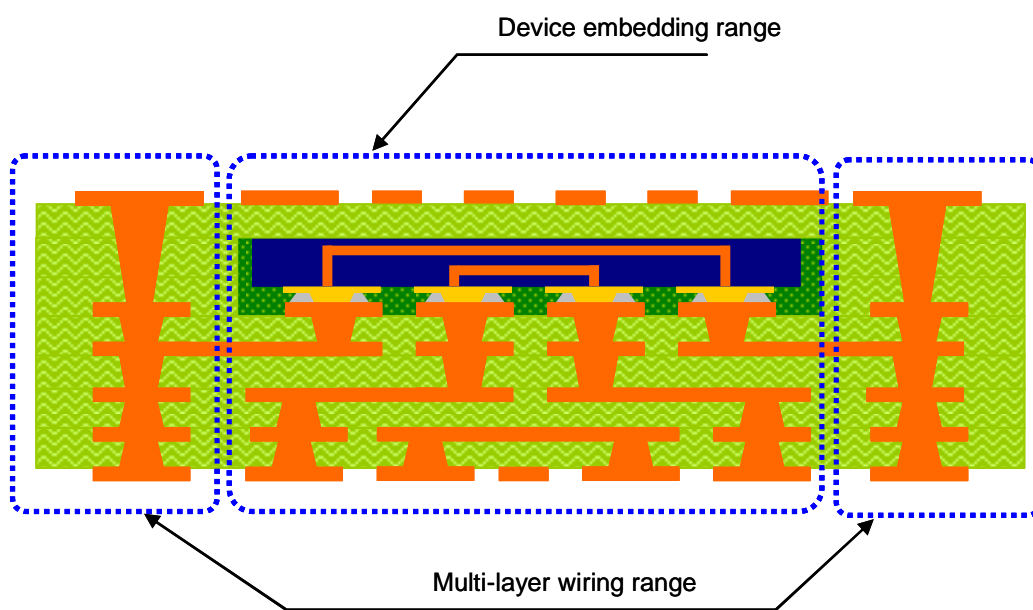
**Figure 20 – Schematic diagram of test circuit**

NOTE Test items, test methods, and test equipment are still under consideration in the standardization committee and there is a possibility that the description made in this document may be changed if necessary.

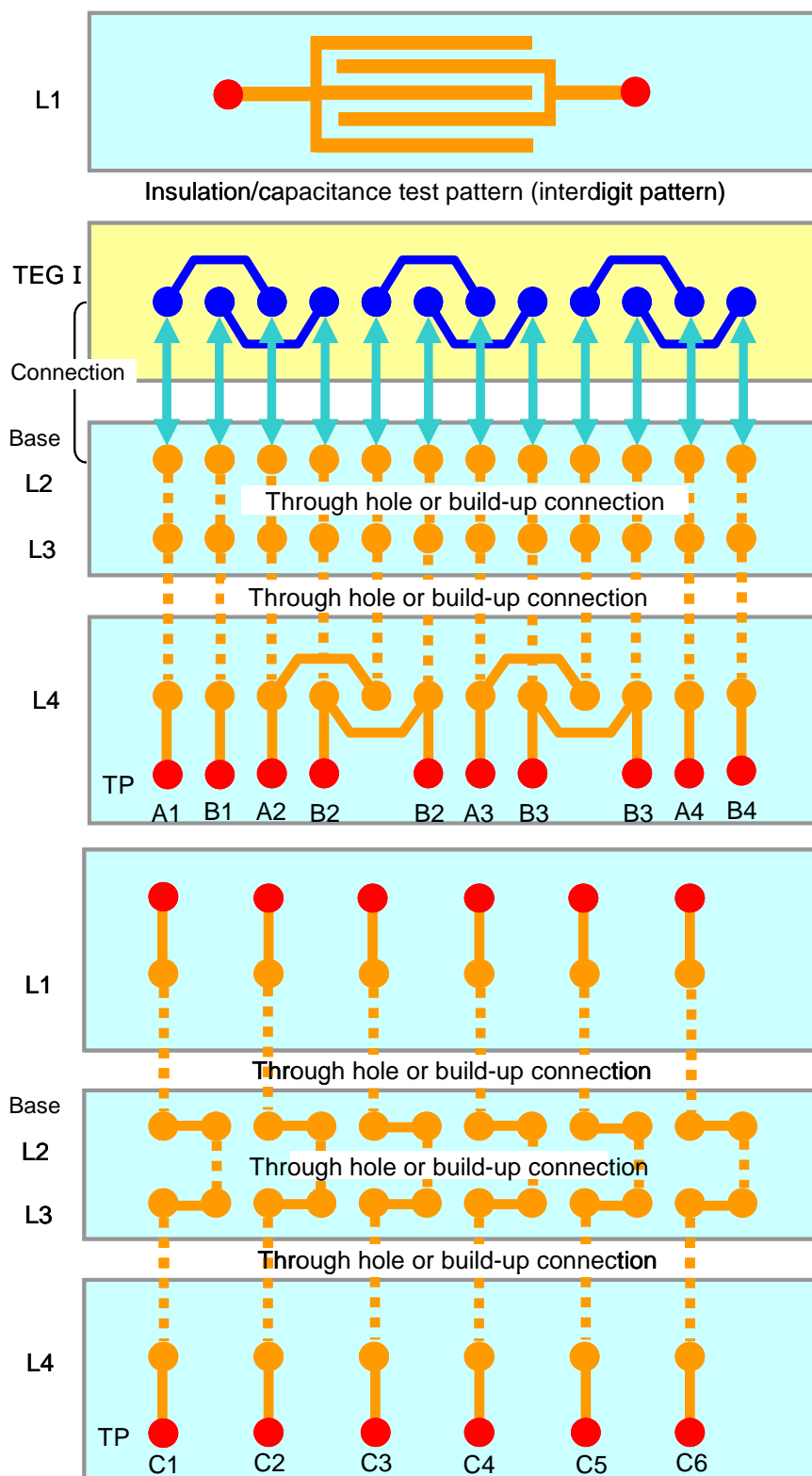
### 4.3 Test circuit

TEG, a dummy specimen of an embedding device, is embedded into board using the actual embedding condition; it is tested for the multilayer wiring patterns shown in Figure 21 similarly to the test of multilayer wiring board for interconnections between conductor pattern by means of through holes and/or vias using the Daisy chain pattern. It is recommended to use the circuit patterns made within the range of device embedding for the tests of inter-digital type capacitor, impedance, insulation and impurity migration as illustrated in Figure 22.

Size of test board, wiring specification of TEG and size as a replacement of embedding device, and wiring specification of the device embedding board shall be agreed between user and supplier.



**Figure 21 – Multilayer wiring patterns**



**Figure 22 – Conceptual structure of test circuit, comb-type capacitor, detection pattern of impedance, insulation and migration**

#### 4.4 Test specimen (TEG) and example of test substrate

Figure 23 shows an example of specimen. It has a Daisy chain pattern in peripheral sections and interdigital capacitor, an impedance detection pattern and a bend detection pattern. Its die size is 10 mm x 10 mm and thickness is 0,15 mm. Electrode number is 316 with a pitch of 120  $\mu\text{m}$ . Electrode size is 110  $\mu\text{m}$  with an opening of 90  $\mu\text{m}$  x 90  $\mu\text{m}$ . Gold bump is used for connection. Figure 24 shows a test board. The conductor resistance (connection evaluation) test is made by the Daisy chain shown in the figure. Insulation resistance test is made using the pattern for evaluation of conductor resistance between conductors and the interdigital pattern shown in Figure 25.

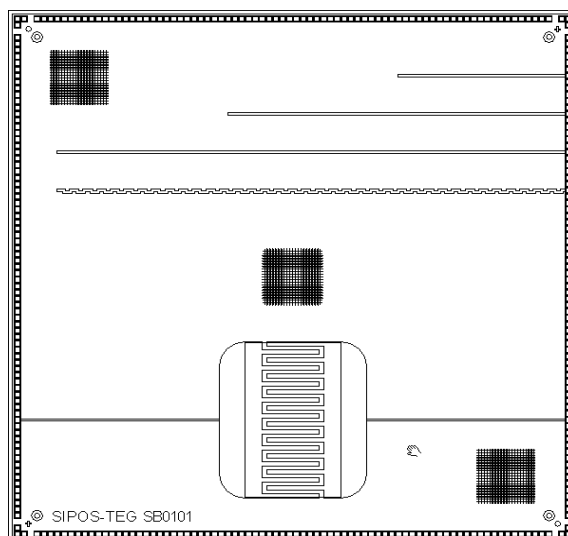


Figure 23 – Example of TEG

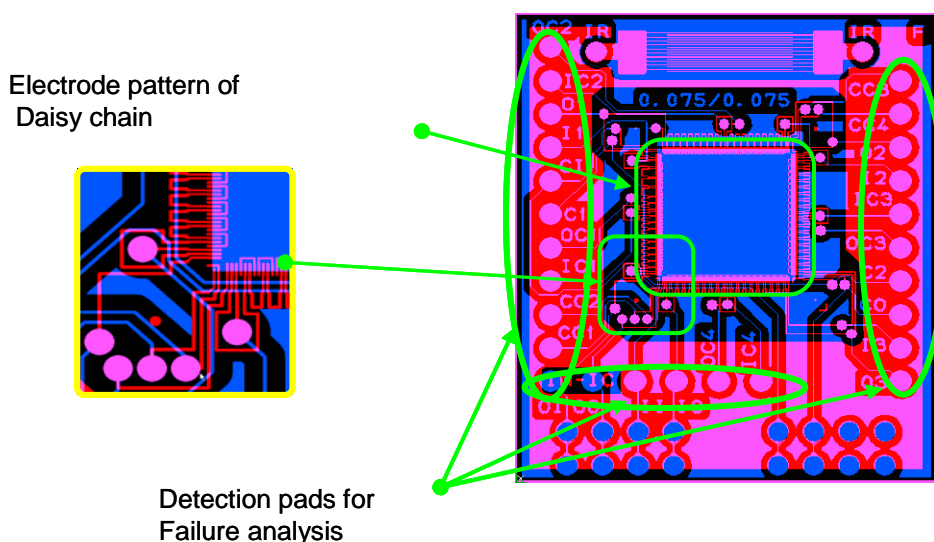
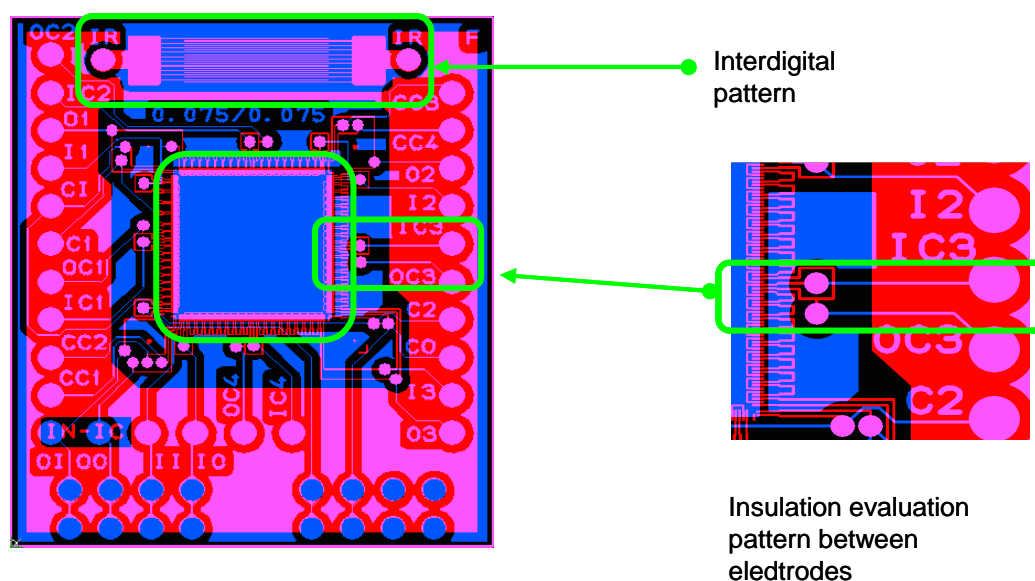


Figure 24 – Example of test circuit for connection evaluation



**Figure 25 – Example of test circuit for insulation evaluation**

## 5 Test items and test equipment

## 5.1 General

Evaluation of device embedded board is basically the same to that of electronic circuit board (printed wiring board and module substrate) but there are some new mechanical and electric test items.

Each test is performed using a specimen embedding the TEG as in actual device embedding using a Daisy chain pattern connection of the TEG and the substrate conductor pattern. It is recommended to use pads independently arranged at corners where the risk of failure is considered relatively high. Evaluation items and test methods are listed in Table 4.

5.2 Test for resistance of conductor

The test method for conduction is shown in Table 4.

Table 4 – Conduction test

| Item                                 |   | Specification  | Test method (JIS C 5012)  |
|--------------------------------------|---|--|---|
| Conduction (conductivity evaluation) | Inner conductor   | To be agreed between user and supplier.<br><br>Relations between resistance and conductor width, conductor thickness and conductor temperature is shown in Figure 26 for reference.<br><br>Conductivity of Cu is taken as $\rho=1,8 \times 10^{-6} \Omega \cdot \text{cm}$ . | As per 7.11 (conductor).<br><br>Shape and dimension of specimen should be agreed between user and supplier.<br><br>1. Test method<br><ul style="list-style-type: none"><li>• Daisy chain or resistance between specified two points.</li></ul><br>2. Equipment<br><ul style="list-style-type: none"><li>• 4 terminal low resistance measurement equipment</li><li>• High/low temperature bath</li></ul> |
|                                      | Outer conductor   |  | As per 7.13 (inner layer connection)  |
|                                      | Plated through hole and via hole (copper plating or conductive paste) |  | Ad per 7.12 (plated through hole)   |
|                                      | Connection to embedded device   | To be agreed between user and supplier   | Use TEG for embedding device test.<br><br>Test for the connection to embedded device is under consideration.  |

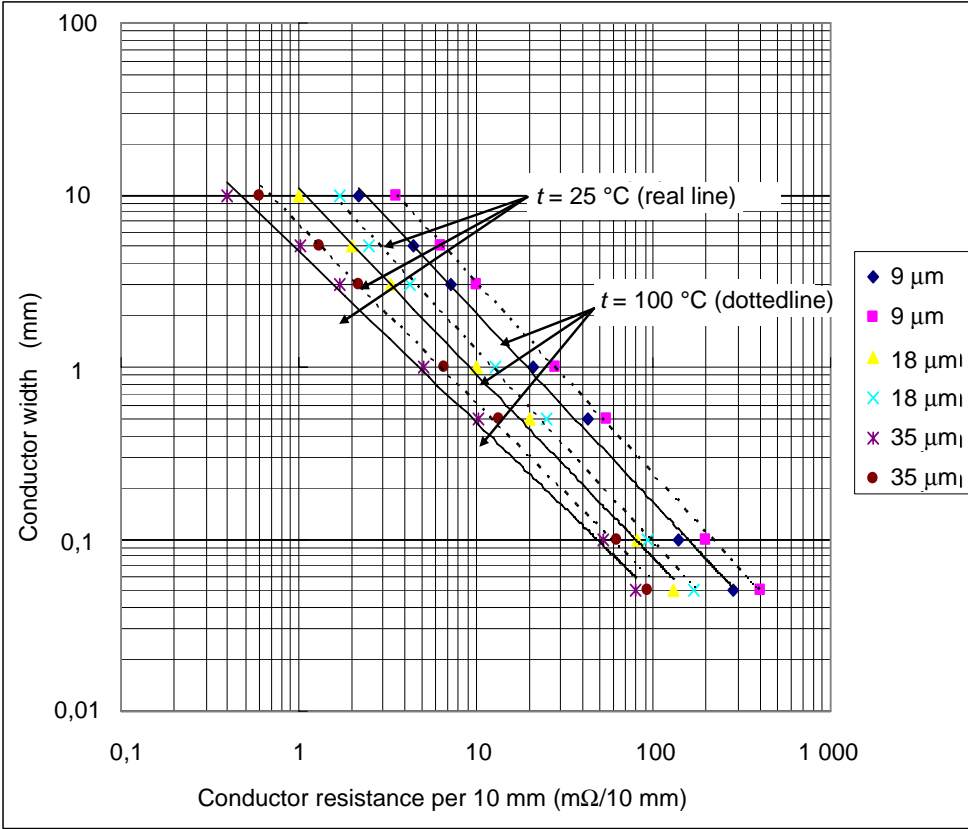


Figure 26 – Resistance per unit length of conductor pattern in relation with conductor width

5.3 Resistance to over current

The test method for resistance over current is shown in Table 5.

Table 5 – Resistance to over current and its test method

| Item                      |                               | Specification  | Test method (JIS C 5012)  |
|---------------------------|-------------------------------|--|---|
| Resistance to overcurrent | Conductor                     | To be agreed between user and supplier   | As per 7.2 (resistance to overcurrent of conductor)   |
|                           | Plated through hole           |  | As per 7.3 (resistance to overcurrent of plated through hole)   |
|                           | Connection to embedded device | To be agreed between user and supplier<br><br>The relation of conductor width, conductor thickness and temperature rise with current are shown in Figure 27. | Under consideration<br><br>Use TEG in place of embedded device.<br><br>The test for the embedded device is under consideration. |

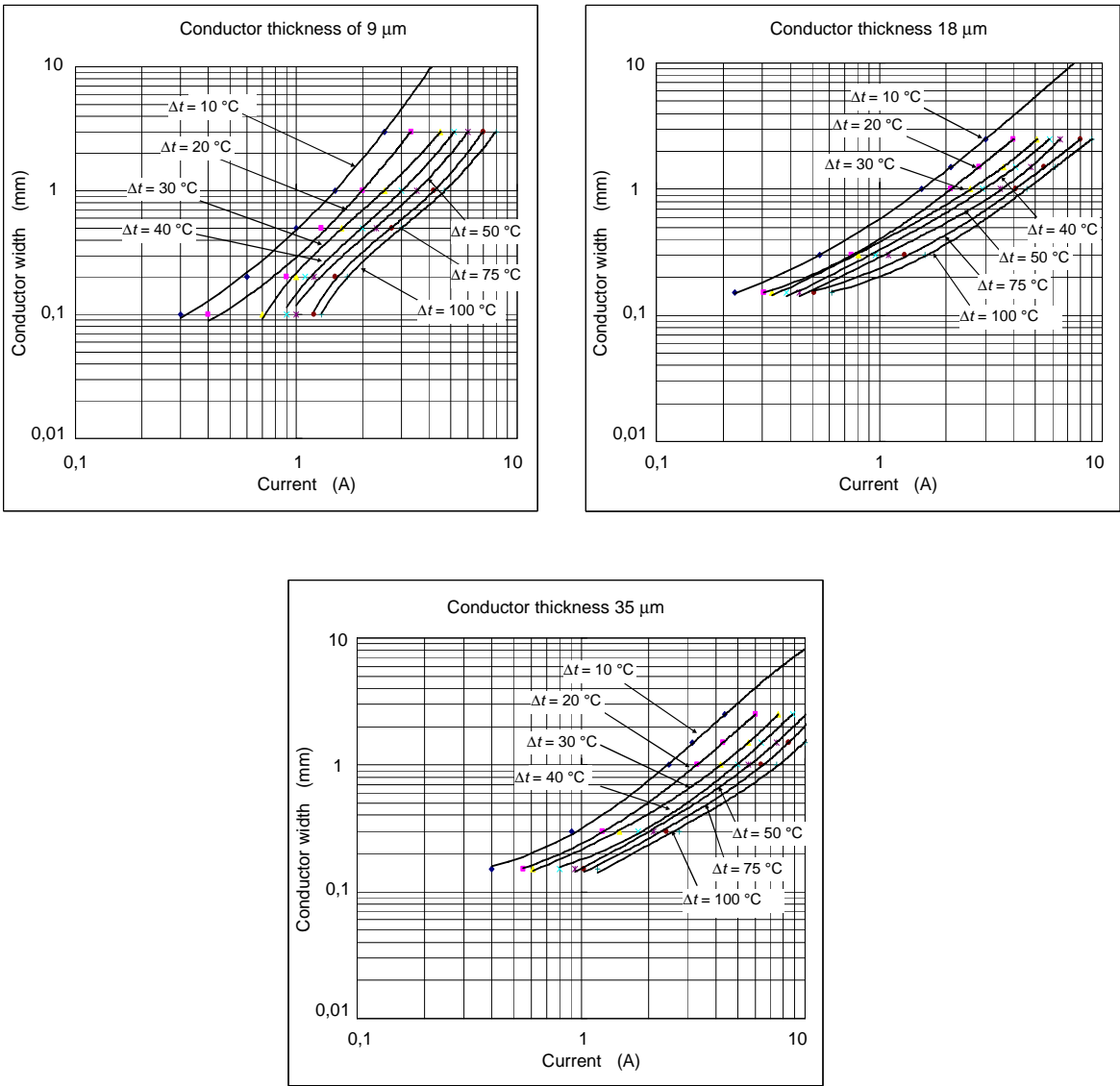


Figure 27 – The relation of conductor width, conductor thickness and temperature rise with current

## 5.4 Withstand voltage

The test method is shown in Table 6.

**Table 6 – Withstand voltage and test method**

| Item   |  | Specification  | Test method (JIS C 5012)  |                             |                   |               |               |               |        |               |     |               |     |        |     |
|--|--|--|---|-----------------------------|-------------------|---------------|---------------|---------------|--------|---------------|-----|---------------|-----|--------|-----|
| Withstand voltage                                | The same plane   | There should be no mechanical damages, flush over, nor insulation damages.   | As per 7.4 (surface withstand voltage)<br><br>The test voltage is chosen from the following table for both outer (with/without solder resist) and inner layers  |                             |                   |               |               |               |        |               |     |               |     |        |     |
|  |  |  | <table><tr><th>Minimum conductor gap<br/>mm</th><th>Test voltage<br/>V</th></tr><tr><td>0,05 ≤ &lt; 0,10</td><td>50</td></tr><tr><td>0,10 ≤ &lt; 0,13</td><td>100</td></tr><tr><td>0.13 ≤ &lt; 0,25</td><td>200</td></tr><tr><td>0,25 ≤ &lt; 0,40</td><td>350</td></tr><tr><td>0,40 ≤</td><td>500</td></tr></table> | Minimum conductor gap<br>mm | Test voltage<br>V | 0,05 ≤ < 0,10 | 50            | 0,10 ≤ < 0,13 | 100    | 0.13 ≤ < 0,25 | 200 | 0,25 ≤ < 0,40 | 350 | 0,40 ≤ | 500 |
|  |  |  | Minimum conductor gap<br>mm   | Test voltage<br>V           |                   |               |               |               |        |               |     |               |     |        |     |
|  |  |  | 0,05 ≤ < 0,10   | 50                          |                   |               |               |               |        |               |     |               |     |        |     |
|  |  |  | 0,10 ≤ < 0,13   | 100                         |                   |               |               |               |        |               |     |               |     |        |     |
|  |  |  | 0.13 ≤ < 0,25   | 200                         |                   |               |               |               |        |               |     |               |     |        |     |
|  |  |  | 0,25 ≤ < 0,40   | 350                         |                   |               |               |               |        |               |     |               |     |        |     |
|  |  |  | 0,40 ≤  | 500                         |                   |               |               |               |        |               |     |               |     |        |     |
| NOTE Solder resist is not considered as coating. |  |  |   |                             |                   |               |               |               |        |               |     |               |     |        |     |
| Interlayer                                       | There should be no mechanical damages, flush over, nor insulation damages. | As per 7.5 (Interlayer withstand voltage)<br><br>The test voltage is chosen from the following table.  |   |                             |                   |               |               |               |        |               |     |               |     |        |     |
|  |  | <table><tr><th>Interlayer distance<br/>mm</th><th>Test voltage<br/>V</th></tr><tr><td>0,05 ≤ &lt; 0,08</td><td>250</td></tr><tr><td>0,08 ≤ &lt; 0,20</td><td>500</td></tr><tr><td>0,02 ≤</td><td>1 000</td></tr></table> | Interlayer distance<br>mm   | Test voltage<br>V           | 0,05 ≤ < 0,08     | 250           | 0,08 ≤ < 0,20 | 500           | 0,02 ≤ | 1 000         |     |               |     |        |     |
|  |  | Interlayer distance<br>mm  | Test voltage<br>V   |                             |                   |               |               |               |        |               |     |               |     |        |     |
|  |  | 0,05 ≤ < 0,08  | 250   |                             |                   |               |               |               |        |               |     |               |     |        |     |
| 0,08 ≤ < 0,20                                    | 500  |  |   |                             |                   |               |               |               |        |               |     |               |     |        |     |
| 0,02 ≤   | 1 000  |  |   |                             |                   |               |               |               |        |               |     |               |     |        |     |
| Connection to embedded device                    | To be agreed between user and supplier                                     | Use TEG for embedding device test.<br><br>Test for the connection to embedded device is under consideration.   |   |                             |                   |               |               |               |        |               |     |               |     |        |     |

## 5.5 Insulation resistance

Test of the insulation resistance is made by using the electrode evaluation pattern made by combination of base and embedding board as in the case of the conductor resistance test. Test items are shown in Table 7.



**Table 7 – Test methods of insulation resistance**

| Item                         |                                       |  | Specification  | Test method (JIS C 5012)  |                            |
|------------------------------|---------------------------------------|--|--|---|----------------------------|
| Insulation resistance        | The same plane                        | Normal   | Insulation resistance should be more than the value shown below.   | See Annex A of this specification.<br>See Annex B of this specification.  |                            |
|                              |                                       |  | Minimum conductor gap<br>mm  |   | Insulation resistance<br>Ω |
|                              |                                       |  | 0,05≤ < 0,13   |   | 1 ×10 <sup>8</sup>         |
|                              |                                       |  | 0,13≤  |   | 5 ×10 <sup>8</sup>         |
|                              |                                       |  |  |   |                            |
|                              |                                       | Resistance to humidity (temperature-humidity cycle)              | Insulation resistance should be more than the value shown below.   | Test should be made as in the case of normal condition.   |                            |
|                              |                                       | Resistance to humidity (steady state)                            | Minimum insulation thickness<br>mm   |   | Insulation resistance<br>Ω |
|                              |                                       |  | 0,05≤ < 0,20   |   | 1 ×10 <sup>8</sup>         |
|                              |                                       |  | 0,20≤  |   | 5 ×10 <sup>8</sup>         |
|                              |                                       |  |  |   |                            |
| Inter-layer                  | Normal                                | Insulation resistance should be more than the value shown below. | See Annex C of this specification. The test voltage is given below.  |   |                            |
|                              |                                       | Minimum insulation thickness<br>mm                               |  | Insulation resistance<br>Ω  |                            |
|                              |                                       | 0,05≤ < 0,20   |  | 1 ×10 <sup>10</sup>   |                            |
|                              |                                       | 0,20≤  |  | 5 ×10 <sup>10</sup>   |                            |
|                              |                                       |  |  |   |                            |
|                              |                                       | Humidity (temperature-humidity cycle)                            | Insulation resistance should be more than the value shown below.   | Test condition is the same as in the case of steady state condition.<br><br>Test should be made after leaving the specimen at room temperature for 1 h. |                            |
|                              |                                       | Humidity (steady state)  | Minimum insulation thickness<br>mm   |   | Insulation resistance<br>Ω |
|                              |                                       |  | 0,05≤ < 0,13   |   | 1 ×10 <sup>10</sup>        |
|                              |                                       |  | 0,13≤  |   | 5 ×10 <sup>10</sup>        |
|                              |                                       |  |  |   |                            |
| Terminals of embedded device | Normal                                | To be agreed between user and supplier.                          | Use TEG for embedded device.<br><br>Test for the interconnection of terminals of embedded device is under consideration. |   |                            |
|                              | Humidity (temperature-humidity cycle) |  |  |   |                            |
|                              | Humidity (steady state)               |  |  |   |                            |

## 5.6 Peeling strength of conductor

Test method and requirement for the peeling strength of conductor are shown in Table 8.

**Table 8 – Peeling strength of conductor and test method**

| Item                          | Specification  | Test method (JIS C 5012)   |
|-------------------------------|--|--|
| Peeling strength of conductor | Peeling strength of conductor should be agreed between use and supplier. | Test method should be agreed between user and supplier based on 8.1 (Peeling strength of conductor). |
|                               | Unit: kN/m   |  |
|                               | Item   |  |
|                               | Specification  |  |
|                               | Glass cloth epoxy resin CCL (FR-4)<br>(Cu foil thickness: 18 µm)         |  |
|                               | 0,98 (for reference)   |  |

## 5.7 Pull-off strength of plated through hole

Test method and requirement for the pull-off strength of plated through hole are shown in Table 9.

**Table 9 – Pull-off strength of plated through hole and test method**

| Item                           | Specification   | Test method (JIS C 5012)                    |
|--------------------------------|---|---|
| Pull-off strength of footprint | Pull-off strength of footprint should be agreed between user and supplier.<br><br>NOTE Pull-off strength of Glass cloth epoxy resin CCL multilayer board should be larger than 39,2N/2mm. | As per 8.4 (pull-off strength of footprint) |

## 5.8 Adhesivity of plated film

Adhesivity of plated film and test method are shown in Table 10.

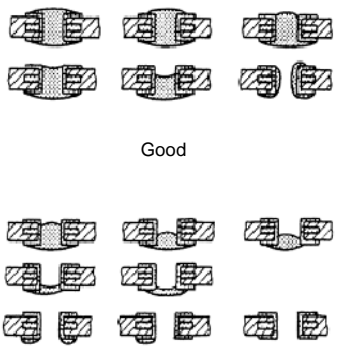

**Table 10 – Adhesivity of plated film and test method**

| Item                      | Characteristics  | Test method (JIS C 5012)               |
|---------------------------|--|--|
| Adhesivity of plated film | There should not be any residue plated film on the tape beside plating overhang. | As per 8.5 (adhesivity of plated film) |

5.9 Solderability

Solderability and its test method are shown in Table 11.

Table 11 – Solderability and test method

| Item          |                              | Specification   | Test method (JIS C 5012)  |
|---------------|------------------------------|---|---|
| Solderability | Footprint                    | There should be no solder sputter on all the footprint.   | As per 10.3 (Solderability test).   |
|               | Through hole                 | <p>Solderability of device assembly holes should be clearly soldered as illustrated in the following illustration (1).</p> <p>There is not specification for the soldered connection of the inner layer conductor and the holes for power supply and/or ground layers which require a wide soldered area.</p> <p>Observable blow-holes (blow of gas contained in solder as illustrated in assembly hole (illustration 2) and the blow holes observable by microsectioning (illustration 3) should be less than 1 % of all the holes. Soldering of vias should be agreed between user and supplier.</p> <p>(1) Soldered shape</p>  <p>Good</p> <p>Not good</p> <p>(2) Surface blow hole      (3) Cross section blow hole</p>  | <p>The maximum soldering temperature is 260 °C and soldering time is 3 s max. for flow soldering, or use the temperature profile given in Annex Figure 6 for "Temperature change in reflow furnace (for reference). Use JIS C 5012, 6.2, Microsectioning when soldered junction is observed by microsectioning.</p> |
|               | Soldering of embedded device | To be agreed between user and supplier.   | Soldering test of embedded device is under consideration.   |

## 5.10 Thermal shock (vapour phase cold heat cycle)

Specification and test method for thermal shock (vapour phase cold heat cycle) are shown in Table 12.

**Table 12 – Characteristics and test method for thermal shock**

| Item   |   | Specification  | Test method (JIS C 5012)  |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
|--|---|--|---|---------------|---------------|---|---------|-------------------|--|--------------|--|-----------------------|------------------|---------------|-----|-----------|--|
| Thermal shock (vapour phase cold heat cycle) | Plated through hole connection<br><br>Plated via connection | <p>Change of connection resistance after test of plated through hole, via connection, or conduction resistance of inner layer should be less than 20 % of the initial value.</p> <p>No floating or peeling of conductor, through hole land or assembly pad should be observed.</p> <p>There should be no delamination.</p> <p>Measling and crazing should satisfy specification in 5.7.3 (defects in lamination).</p> <p>Observation of specimen by microsectioning after test should satisfy specification of 6.1.2 (observation after thermal shock test).</p> <p>Solder resist and marking should satisfy the values given below.</p> <table><thead><tr><th>Item</th><th>Specification</th></tr></thead><tbody><tr><td>Solder resist</td><td>No colour change, no floating, and no blister</td></tr><tr><td>Marking</td><td>Should be legible</td></tr></tbody></table> | Item  | Specification | Solder resist | No colour change, no floating, and no blister | Marking | Should be legible | <p>As per 9.2 (thermal shock – low and high temperature)</p> <p>Specimen is a daisy chain connection of a minimum of 100 holes formed at a specified section of PWB, test coupon, or combined pattern similar to the combined test pattern (D pattern given in Annex Figure 21 or 22).</p> <p>Use condition 2 in Table 4 for test temperature cycle and the number of cycles given below as the specimen thickness may affect the test result.</p> <table><thead><tr><th colspan="2">Cycle number</th></tr><tr><th>Specimen thickness mm</th><th>Number of cycles</th></tr></thead><tbody><tr><td>Less than 1,6</td><td>100</td></tr><tr><td>Above 1,6</td><td>To be agreed between user and supplier</td></tr></tbody></table> <p>Resistance change <math>\Delta R/R</math> (%) is obtained from the following equation:</p> $\Delta R/R \text{ (\%)} = (W_2 - W_1) / W_1 \times 100$ <p>where</p> <p><math>W_1</math> = initial resistance</p> <p><math>W_2</math> = resistance after the test</p> | Cycle number |  | Specimen thickness mm | Number of cycles | Less than 1,6 | 100 | Above 1,6 | To be agreed between user and supplier |
|  | Item  | Specification  |   |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
| Solder resist                                | No colour change, no floating, and no blister               |  |   |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
| Marking                                      | Should be legible   |  |   |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
| Cycle number                                 |   |  |   |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
| Specimen thickness mm                        | Number of cycles  |  |   |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
| Less than 1,6                                | 100   |  |   |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
| Above 1,6                                    | To be agreed between user and supplier                      |  |   |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |
|  | Connection to embedded device                               | To be agreed between user and supplier   | <p>Use TEG for embedding device test.</p> <p>Test for the connection to embedded device is under consideration.</p> |               |               |   |         |                   |  |              |  |                       |                  |               |     |           |  |

### 5.11 Thermal shock (high temperature)

Specification and test method for thermal shock are shown in Table 13.

**Table 13 – Specification and test method for thermal shock**

| Item                             |  | Specification  | Test method (JIS C 5012)  |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
|----------------------------------|--|--|---|--|---------------|--|---------------|---|--|---------|-------------------|---|------------------|--|--------------------------|------------------|-----|----|-------------|---|-------|--|
| Thermal shock (high temperature) | Plate through hole connection<br><br>Plated via connection | <p>Change of connection resistance after test of plated through hole, via connection, or conduction resistance of inner layer should be less than 20 % of the initial value.</p> <p>No floating or peeling of conductor, through hole land or assembly pad should be observed.</p> <p>There should be no delamination.</p> <p>Measling and crazing should satisfy specification in 5.7.3 (defects in lamination).</p> <p>Observation of specimen by microsectioning after test should satisfy specification of 6.1.2 (observation after thermal shock test).</p> <p>Solder resist and marking should satisfy the values given below.</p> <table><tr><th colspan="2">Item</th><th>Specification</th></tr><tr><td></td><td>Solder resist</td><td>No colour change, no floating, and no blister</td></tr><tr><td></td><td>Marking</td><td>Should be legible</td></tr></table> | Item  |  | Specification |  | Solder resist | No colour change, no floating, and no blister |  | Marking | Should be legible | <p>As per 9.3 (thermal shock – high temperature).</p> <p>Specimen is formed at a specified section of PWB, test coupon, or combined pattern similar to the combined test pattern (D pattern given in Annex Figure 21 or 22).</p> <p>Use test temperature cycle and the number of cycles given below as the specimen thickness may affect the test result.</p> <table><tr><th colspan="2">Number of cycles</th></tr><tr><th>Specimen thickness<br/>mm</th><th>Number of cycles</th></tr><tr><td>1,6</td><td>10</td></tr><tr><td>1,6 ≤ &lt; 2,4</td><td>5</td></tr><tr><td>2,4 ≤</td><td>To be agreed between user and supplier</td></tr></table> | Number of cycles |  | Specimen thickness<br>mm | Number of cycles | 1,6 | 10 | 1,6 ≤ < 2,4 | 5 | 2,4 ≤ | To be agreed between user and supplier |
|                                  | Item   |  | Specification   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
|                                  | Solder resist  | No colour change, no floating, and no blister  |   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
|                                  | Marking  | Should be legible  |   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
| Number of cycles                 |  |  |   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
| Specimen thickness<br>mm         | Number of cycles   |  |   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
| 1,6                              | 10   |  |   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
| 1,6 ≤ < 2,4                      | 5  |  |   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
| 2,4 ≤                            | To be agreed between user and supplier                     |  |   |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |
|                                  | Connection to embedded device                              | To be agreed between user and supplier   | <p>Use TEG for embedding device test.</p> <p>Test for the connection to embedded device is under consideration.</p> |  |               |  |               |   |  |         |                   |   |                  |  |                          |                  |     |    |             |   |       |  |

## 5.12 Flammability

Flammability specification and test method are shown in Table 14.

**Table 14 – Flammability specification and test method**

| Item         |  | Specification  | Test method (JIS C 5012) |
|--------------|--|--|--------------------------|
| Flammability | Insulation layer<br>Solder resist<br>Marking | Flammability should conform the requirement of flammability grade.         | In conformity to UL 94.  |
|              | Embedded device                              | Flammability of embedding device should conform that of the device itself. |                          |

## 5.13 Bow and twist

Specification and test method for bow and twist are shown in Table 15.

**Table 15 – Specification and test method for bow and twist**

| Item          |  | Specification  | Test method (JIS C 5012)   |        |                             |  |        |          |  |
|---------------|--|--|--|--------|-----------------------------|--|--------|----------|--|
| Bow and twist | Completed device embedded board (applicable to board thickness of over 0,8 mm) | Bow and twist should satisfy the following values.   | As per 6.3.9 (flatness)  |        |                             |  |        |          |  |
|               |  | For board thickness of less than 0,8 mm, bow and twist should be agreed between user and supplier.   |  |        |                             |  |        |          |  |
|               |  | <table><tr><th rowspan="2">Item</th><th colspan="2">Length of longer side ( L )</th></tr><tr><th>100 mm</th><th>100 mm ≤</th></tr></table> |  | Item   | Length of longer side ( L ) |  | 100 mm | 100 mm ≤ |  |
|               |  | Item   |  |        | Length of longer side ( L ) |  |        |          |  |
|               |  |  |  | 100 mm | 100 mm ≤                    |  |        |          |  |
| Bend          | 0,8 mm   | For length exceeding 100 mm, bend should be less than the value given below<br><br>0,8 mm +<br>$(L - 100) \times 0,007$                    |  |        |                             |  |        |          |  |
| Twist         | 1,0 mm   | For length exceeding 100 mm, twist should be less than the value given below<br><br>1,0 mm +<br>$(L - 100) \times 0,01$                    |  |        |                             |  |        |          |  |
|               | Connection to embedded device  | To be agreed between user and supplier   | Use TEG for embedding device test.<br><br>Test for the connection to embedded device is under consideration. |        |                             |  |        |          |  |

## 5.14 Migration

Specification and test method for migration are given in Table 16.

**Table 16 – Specification and test method for migration**

| Item      |   | Specification  | Test method (JIS C 5012)  |               |           |                             |  |
|-----------|---|--|---|---------------|-----------|-----------------------------|--|
| Migration | Between conductor pattern                               | <div>Migration should satisfy the resistance given below</div> <table><tr><th>Item</th><th>Specification</th></tr><tr><td>Migration</td><td><math>1 \times 10^8 \Omega \leq</math></td></tr></table> <div>Measurement should be made after leaving the specimen for 1 h at room temperature.</div> | Item  | Specification | Migration | $1 \times 10^8 \Omega \leq$ | <div>Standard test condition is given here for reference.</div> <div>Specimen</div> <div>Comb pattern made on board with the minimum conductor gap on the board used.</div> <div>Temperature/relative humidity</div> <div>40°C/90%, 60°C/90% or 85°C/85%</div> <div>Standard applied voltage</div> <div>D C 5 V, 10 V, 15 V, 25 V</div> <div>Time: 250 h, 500 h, 1 000 h</div> |
|           | Item  | Specification  |   |               |           |                             |  |
| Migration | $1 \times 10^8 \Omega \leq$                             |  |   |               |           |                             |  |
|           | Between embedded device terminals and conductor pattern | To be agreed between user and supplier   | <div>Use TEG for embedding device test.</div> <div>Test for the connection to embedded device is under consideration.</div> |               |           |                             |  |

The other tests for mechanical stress given below are under consideration:

- a) vibration (steady state, shock)
- b) vibration at high temperature (steady state, shock)
- c) drop test
- d) bend
- e) torsion
- f) Tg (as is, in operation)
- g) Tg (vibration, resonance, shock)

## 6 Indication, packaging and storage

**6.1** Indication relative to the product should be agreed between user and supplier; however, the following subjects should be included.

- a) Product name or product number
- b) Name of manufacturer or its mark
- c) Date of production

**6.2** Packaging of the product should be agreed between user and supplier; however, the following subjects should be included.

- a) Product name or product number
- b) Number of product in a package
- c) Date of production
- d) Name of manufacturer or its mark

## **6.3 Package and storage**

6.3.1 Packaging: The packaging should be made not to damage product and to avoid the effect of moisture.

6.3.2 Storage: The product should be stored where the effect of moisture can be avoided.

## **7 Design guide**

### **7.1 General**

The design guide of device embedded substrate is essentially the same as the design guide of various electronics circuit boards. The design guide stated here for device embedded substrate is basically the thorough understanding of circuit design, structure design, board design, board manufacturing, jisso (assembly processes) and tests of products. In this design guide are specified the names of constructions and structures of device embedded substrates, structures and restrictions imposed to device embedded bases, conditions of device embedding, and fabrication conditions of electronics circuit boards using device embedded substrates. Details of manufacturing conditions and reliability assurance of products are to be agreed between supplier and user.

### **7.2 Structure of device embedded substrate**

#### **7.2.1 General**

The name of each part of a device embedded substrate is specified in this section to assist the engineers in avoiding technical misunderstanding in relevant sectors of the industry.

#### **7.2.2 Specification of the front and back surfaces of a device embedded substrate**

The definition of the front and back surfaces of a device embedded substrate basically depends on the number of devices mounted on the surface of the substrate as shown in Figure 28. The surface with more components mounted on one face than on the other is defined as the front surface. In the case of mounting a substrate on a printed wiring board (mother board), the surface connection of the substrate to the wiring board is defined as the back surface even in a case with a larger number of input/output terminals (pads) (see Figure 29). In this case the front and back surfaces are agreed between user and supplier, the agreement is the surface definition of priority different from the definition stated here.



## a) Complete device embedded substrate structure

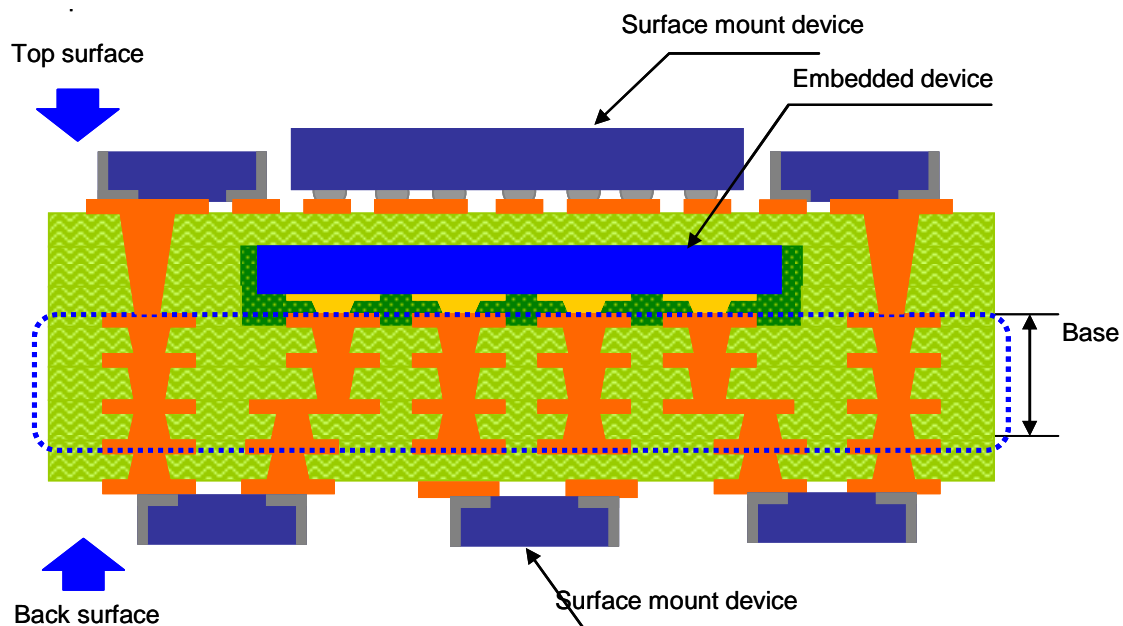


Figure 28 – Definition of front and back surfaces of a device embedded substrate

## b) Device embedded substrate mounted on PWB (mother board)

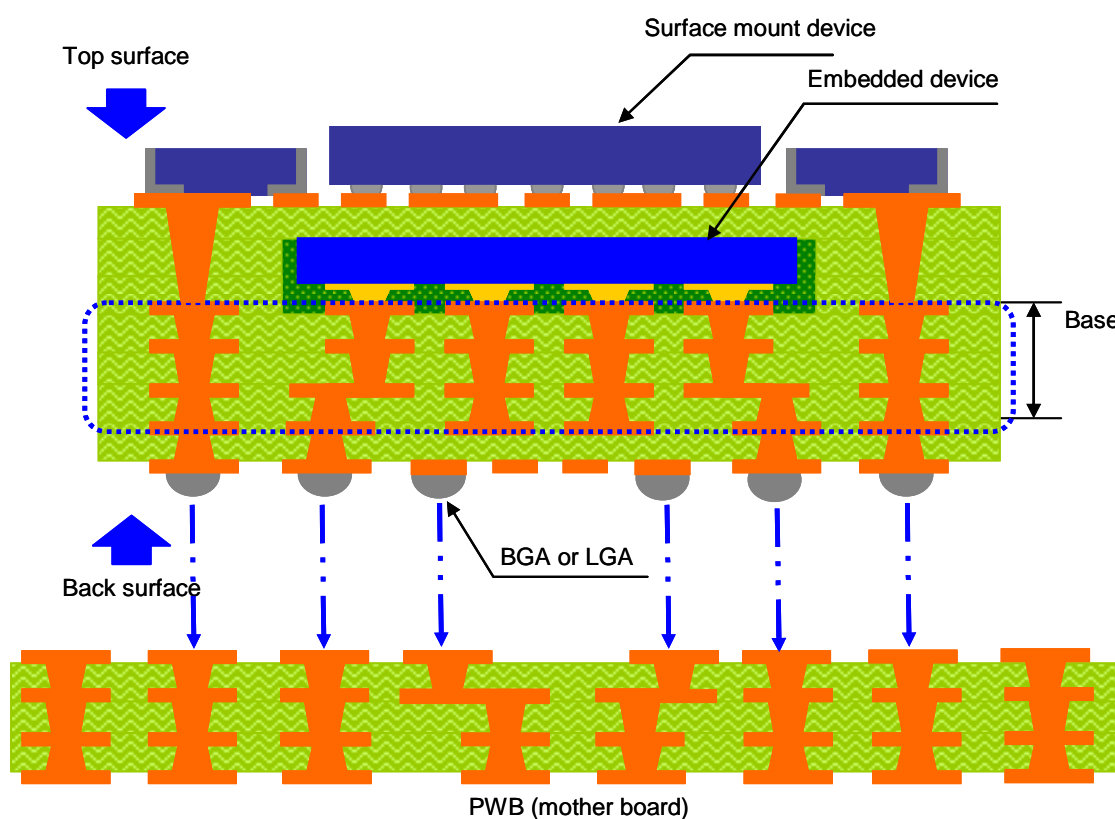


Figure 29 – Definition of front and back surfaces of a device embedded substrate – substrate mounted on a mother board

### 7.2.3 Definition of layers of a device embedded substrate

Layers of a multi-layer device embedded substrate is defined as the layer containing a conductive layer as one layer and defined as L1, L2, ~ L5, L6 (in the case of 6 layers) from the front surface of the substrate (see Figure 30).

In the case where the number of layers of the terminals of the embedded devices and the number of conductor layers are not the same as is the case in the via connection structure, virtual layers are specified to clarify the structure of a device embedded substrate, conductor pattern design, and the positions of embedded devices in substrate manufacturing and assembly processes.

Supplementary names for layers are added in the virtual layers to the layers as an exception to which to die bond or to mount the device to the layer. The front layer faces upward. The surface is upward (U) when terminals face upward and, downward when terminals face downward (D). Two orders of numbers are assigned to express the cases where multiple devices and/or connection terminals exist on the same single layer. The left side number expresses the connecting layer and the right side number expresses the layer number of the embedded devices. In the case of multiple layers, the number is assigned as 1 and 2 from the upper side and 1 and 2 from bottom for down side supplementary layers (see Figures 32 and 33).

EXAMPLES : Die bonding or mounting layer=L2  
 Direction of connection terminals (L1 is upward)=U  
 Connection layer (left side)=1  
 Number of devices in a layer=2  
 Number of embedded devices (first layer of the same position) =1 (may be omitted for only 1)  
 (second layer of the same position)=2 (may be omitted for only 1)  
 EXAMPLES: x x x x L2-U11 (upper side), x x x x L2-U12 (Lower side)  
 NOTE x x x x is the device number or the device mark.

#### a) Names of layers in pad connection

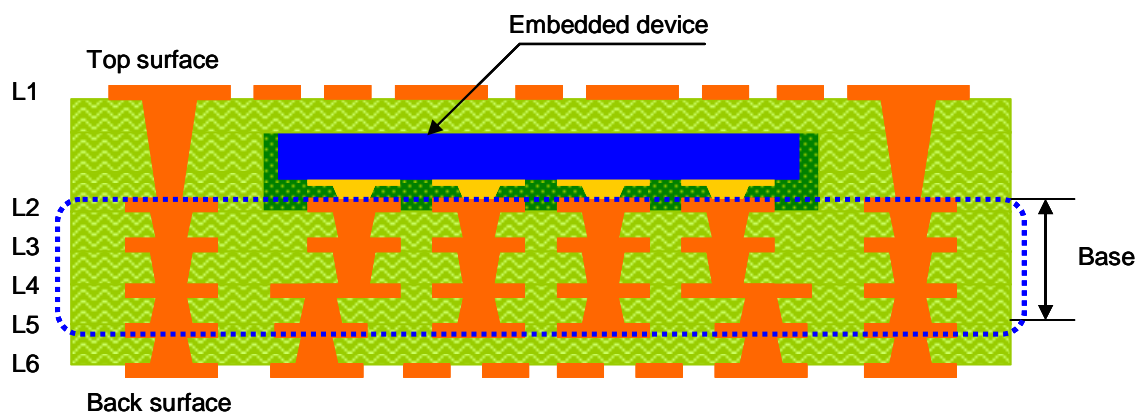


Figure 30 – Definition of layers of a pad-connection substrate

## b) Remarks on positioning of terminals

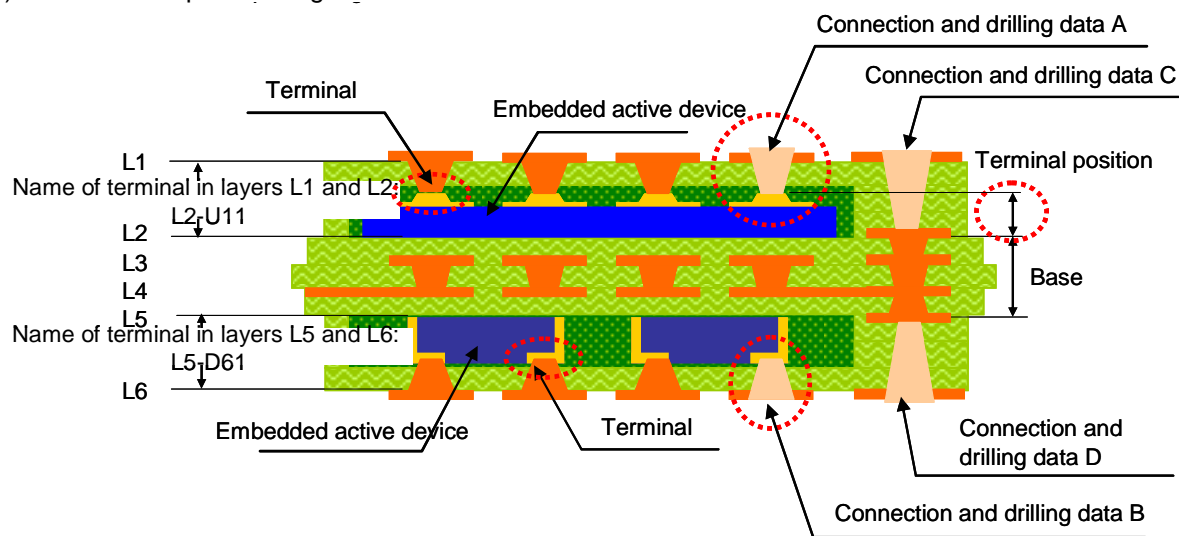


Figure 31 – Illustration of virtual layers

Note added in proof

The virtual layers are necessary to identify the interconnection layers (position) in substrate design for the case the position(s) of interconnection terminals of embedded devices is different from the position of a conductor layer when the position of a conductor layer is used as the reference of positions in an embedded substrate. In a production process, there may be no conductor layer at the terminal position(s). Basic number of layers may be 6 but virtual layer(s) may be required to identify the terminal positions. A virtual layer may be handled as a virtual conductor layer in pattern design and specify the interconnection position. Interconnection data and hole drilling data, A and B, are specified for the terminal connections of an embedded device and interconnection data and hole drilling data, C and D, are specified to the connections to L2 and L5 layers (in the case of this example). The virtual layer may be omitted when the position of terminals of an embedding device and that of a conductor layer is the same as in the case of via connection.

## c) Names of layers in via connections (terminals in between layers)

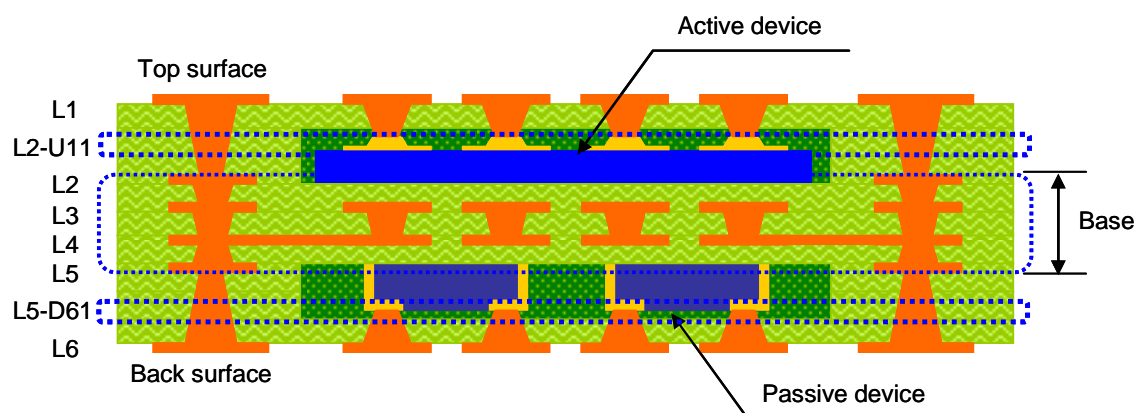
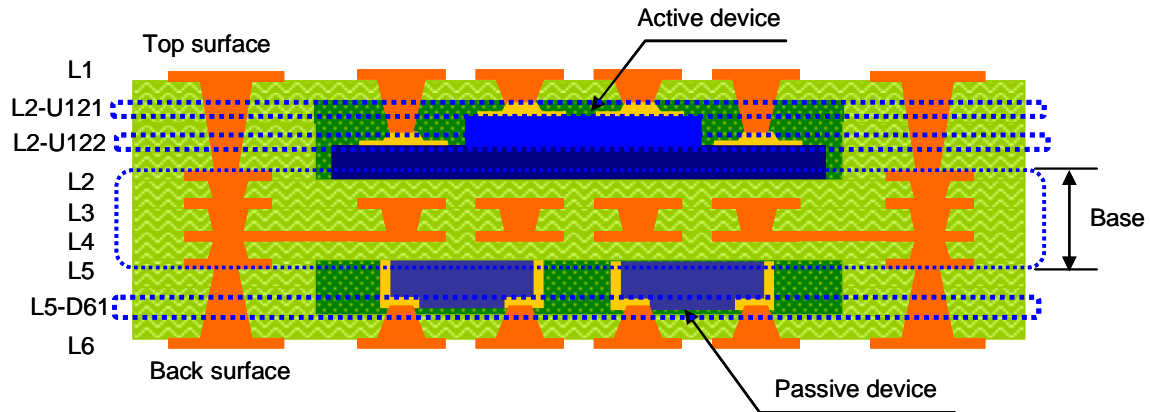


Figure 32 – Layer names in the via interconnection (I)

x x x x - L2-U11 L2: Device is embedded in L2 (2<sup>nd</sup> layer).

U: Terminals are connected upward.  
 11: Connections of single embedded device at L1  
 L5: Device is embedded in L5 (5<sup>th</sup> layer).  
 D: Terminals are connected downward.  
 61: Connection of single embedded device at L6

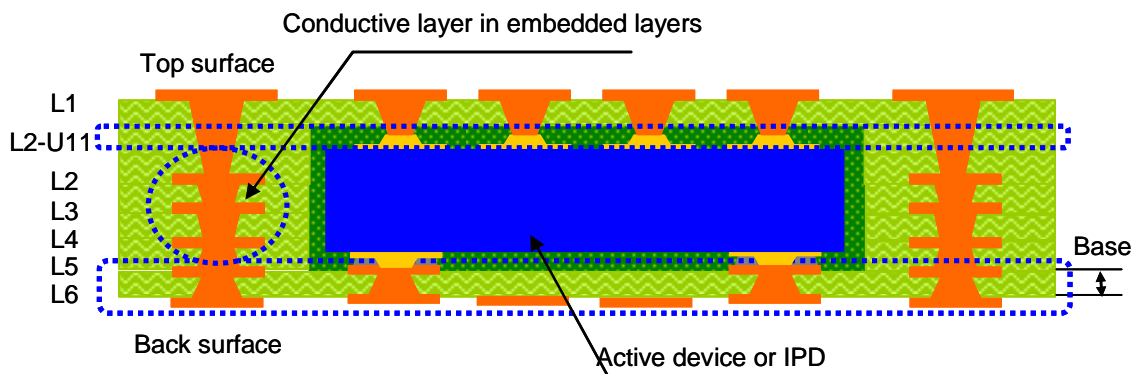
d) Names of layers in via connection (devices are stacked in 2 or more layers)



**Figure 33 – Layer names in the via interconnection (II)**

x x x x - L2-U121 L2: Device is embedded in L2 (2<sup>nd</sup> layer)  
 U: Terminals are connected upward.  
 121: Connections of two embedded devices at L1  
 x x x x - L2-U122 L2: Device is embedded in L2 (2<sup>nd</sup> layer).  
 U: Terminals are connected upward.  
 122: Connection of two embedded devices at L1

e) Names of layers in via connection (devices are embedded in more than 2 layers)



**Figure 34 – Layer names in via connection (III)**

Table 17 shows examples of layer names shown in Figures 31 to 34.

**Table 17 – Layer names of device embedding substrate**

| Example   | Embedding device |        |                   |        | Embedding device and interconnection |        |                    |                   |                           |       |
|---|------------------|--------|-------------------|--------|--------------------------------------|--------|--------------------|-------------------|---------------------------|-------|
|   | Device           | Hyphen | Terminal No./name | Hyphen | Embedding                            | Hyphen | Terminal direction | Connec-ting layer | No. of devices in a layer |       |
|   |                  |        |                   |        |                                      |        |                    |                   | Num-ber                   | Layer |
| Figure 31   | Active device    | -      | A12               | -      | L2                                   | -      | U                  | 1                 | 1                         | Omit  |
|   | Passive device   | -      | 1                 | -      | L5                                   | -      | D                  | 6                 | 1                         | Omit  |
| Figure 32   | Active device    | -      | A13               | -      | L2                                   | -      | U                  | 1                 | 1                         | Omit  |
|   | Passive device   | -      | 2                 | -      | L5                                   | -      | D                  | 6                 | 1                         | Omit  |
| Figure 33   | Active device    | -      | A13               | -      | L2                                   | -      | U                  | 1                 | 2                         | 1     |
|   | IPD              | -      | 4                 | -      | L2                                   | -      | U                  | 1                 | 2                         | 2     |
|   | Capacitor        | -      | +                 | -      | L5                                   | -      | D                  | 6                 | 1                         | Omit  |
| Figure 34   | IPD, etc.        | -      | 12                | -      | L2                                   | -      | U                  | 1                 | 1                         | Omit  |
|   |                  | -      | B1                | -      | L6                                   | -      | D                  | 6                 | 1                         | Omit  |
| NOTE Device information is necessary in embedding substrate design.   |                  |        |                   |        |                                      |        |                    |                   |                           |       |
| Example of device information indication: the device is indicated as ‘Active device-A12-L2-U11’ in the case of Figure 31. |                  |        |                   |        |                                      |        |                    |                   |                           |       |

#### 7.2.4 Definitions of insulation layer thickness, conductor spacing and distance between electrode and conductor spacing (hereafter called “electrode”) at a terminal

The insulation layer thickness and the distance between each conductive layer are defined in reference to the position of each layer.

- 1) The insulation layer thickness is defined as the layer separating the conductor layers. The thickness is not the thickness of each layer to be laminated but the thickness of the actual insulation layer of the substrate.
- 2) The conductor distance is defined as the distance between the conductors formed on one layer.
- 3) The distance between the electrode and the conductor is the thickness of the insulator in between the terminals of the embedding device and the conductor layer to be connected.
- 4) The following terms are used to indicate each distance.
 

|   |                             |
|---|-----------------------------|
| (1) Insulation layer thickness              | DG1 (Dielectric gap)        |
| (2) Distance between conductor layers       | LG1 (Layer gap)             |
| (3) Distance between terminal and conductor | EG11 (Device embedding gap) |

The number used in the indication is the number of layers. The left number in (3) is for the conductor layer and the number on the right shows the step, first, second, etc., of the multi-device embedding into the substrate. See 7.2.3 for the definition of steps (layers). Figures 35 and 36 show the definition of layers of a device embedded substrate for cases of pad and via connections. Additional remarks are added to Figures 37 and 38 for the dielectric gap, layer gap and device embedding gap.

a) Insulation layer thickness, conductor separation and terminal/conductor distance in pad connection

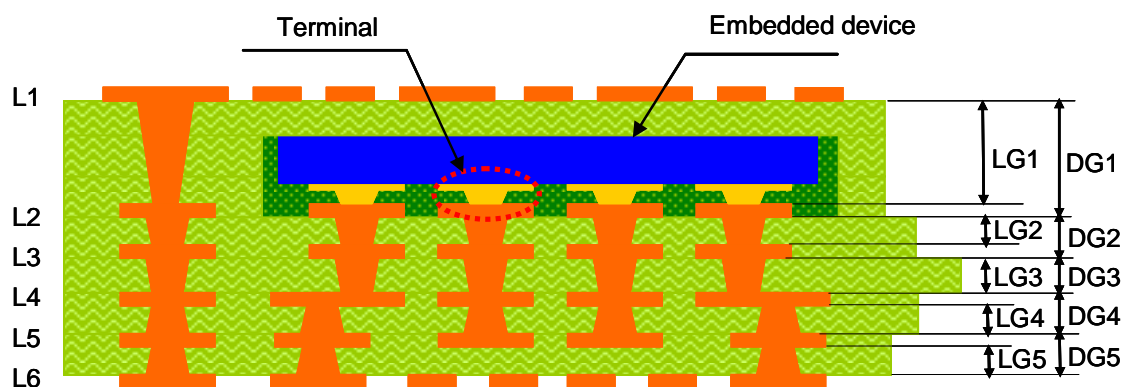


Figure 35 – Definitions of dielectric gap and layer gap in the pad connection method

b) Insulation layer thickness, conductor separation and terminal/conductor distance in via connection

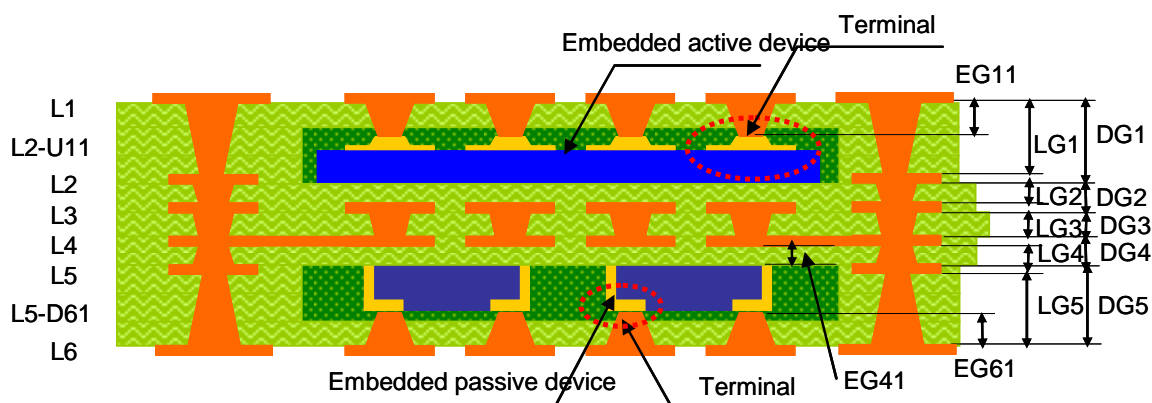


Figure 36 – Definitions of dielectric gap and layer gap in the via connection method

c) Additional remark on insulation layer thickness

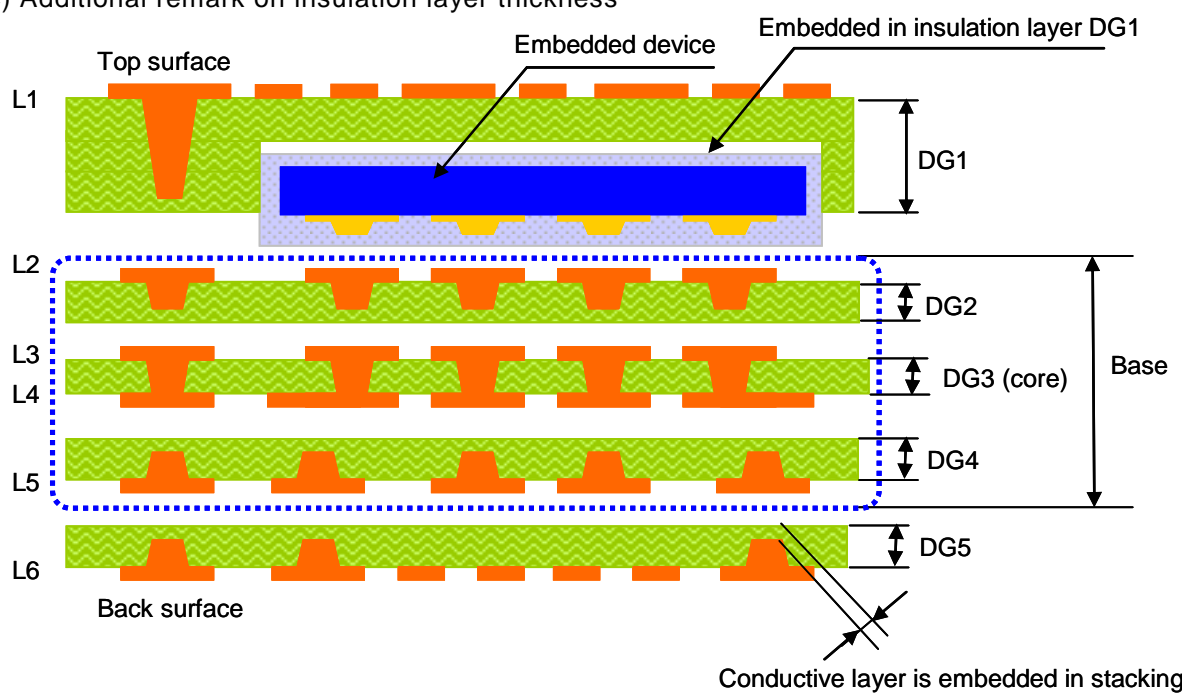


Figure 37 – Additional illustration of dielectric gap

d) Remarks on conductor separation and terminal/conductor distance

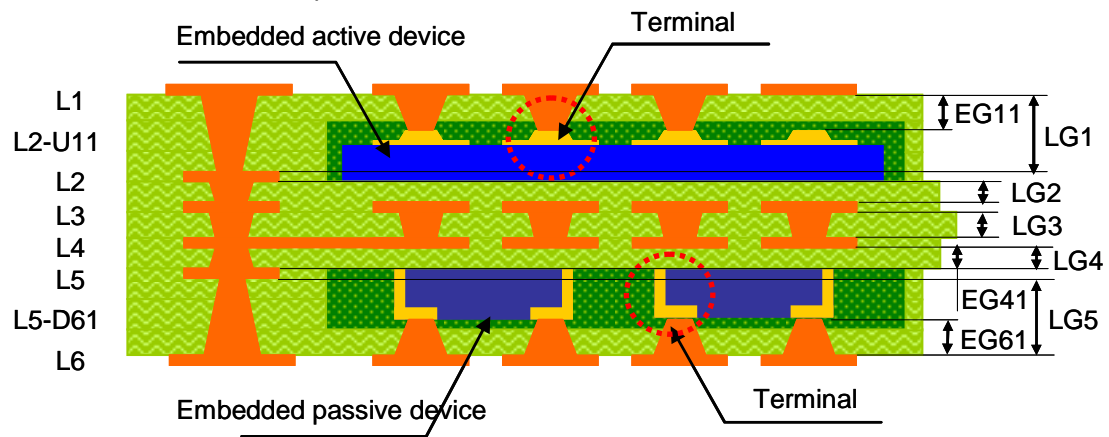


Figure 38 – Additional illustration of layer gap



### 7.3 Conditions for base

Base board and assembly condition are given in Table 18.

**Table 18 – Requirements to device assembly to base substrate of device embedded boards**

| Item  |                                | Condition   | Remarks   |
|---|--------------------------------|---|---|
| Base  | Base material                  | Organic: FR-4, FR-5, BT Resin, polyimide, PPE, PTFE<br>Inorganic: ceramics, LTCC  | Copper foil carrier, metal heat fin for heat radiation, film type carrier, silicon interposer., ceramics interposer |
|   | Board structure                | Single sided, double sided, Multilayer, Build-up multilayer,<br>Single-sided flexible, double-sided flexible, Multilayer flexible,<br>Ceramics, LTCC electronic circuit substrate<br>Passive device embedded ceramics |   |
|   | Number of layers               | 1 layer, 2 layers, ~ arbitrary number of layers   |   |
|   | Copper foil                    | 5 µm, 9 µm, 12 µm, 18 µm, 35 µm, 70 µm  |   |
|   | Insulator                      | > 10 µm   |   |
|   | Maximum size                   | 610 mm × 510 mm   | Variable based on the capability of die Bonder and/or chip mounter  |
|   | Minimum size                   | 340 mm × 250 mm   |   |
| Embedded layer  | Insulation material            | Prepreg such as FR-4, FR-5, BT Resin, polyimide, PPE, PTFE (B stage type)<br>Resin such as FR-4, FR-5, BT resin, polyimide, etc.<br>Sealing resin used for semiconductor packages<br>Others                           | A cut-off may be required for a thick embedding device  |
|   | Number of layers               | 1 layer, 2 layers, ~ arbitrary number of layers   |   |
|   | Copper foil                    | 5 µm, 9 µm, 12 µm, 18 µm, 35 µm, 70 µm  |   |
|   | Board size                     | Depends on the base size  |   |
| Condition   | Die bonder                     | Maximum : 330 mm × 250 mm × 2,5 mm<br>Minimum : 50 mm × 50 mm × 0,5 mm  | A carrier may be necessary if the thickness is less than 0,3 mm   |
|   | Mounter                        | Maximum : 510 mm × 460 mm × 4,0 mm<br>Minimum : 50 mm × 50 mm × 0,3 mm  |   |
|   | Fiducial mark                  | Fiducial mark shall be in accordance to customers process capability  |   |
|   | Position accuracy              | To be agreed by customer based materials and process capability   |   |
| Condition for sheet components  | Die bonder                     | Maximum : 25 mm × 25 mm × 0,5 mm<br>Minimum : 0,25 mm × 0,25 mm × 0,1 mm  |   |
|   | Mounter                        | Maximum : 24 mm × 24 mm × 6,5 mm<br>Minimum : 0,4 mm × 0,2 mm × 0,12 mm   |   |
|   | Thermal resistance             | Withstand for 120 min at 180 °C   |   |
|   | Resistance to pressure         | 3 MPa ~ 4 MPa   |   |
|   | Resistance to chemical solvent | To be agreed by customer based materials and process capability   |   |
| NOTE The above assembly requirements are for reference to the Standard drafting committee for device embedding substrate. Detailed requirements are to be agreed between user and supplier. |                                |   |   |

## 7.4 Conditions for embedding devices

Work panel size, panel thickness and embedding condition are shown in Table 19 when automatic device embedding equipment is used.

**Table 19 – Embedding requirement**

| Assembly  |             | Device                | Shape                                 |                   | Direction<br>(to<br>embedded<br>terminals) | Panel size<br>mm   |                | Thickness<br>mm |            | Fiducial<br>mark |
|---|-------------|-----------------------|---------------------------------------|-------------------|--|--------------------|----------------|-----------------|------------|------------------|
|   |             |                       |                                       |                   |  | Max.               | Min.           | Max.            | Min.       |                  |
| Pad bonding   | Die bonding | Bare die              | WB                                    |                   | Up   | 267×90             | 90×15          | 0,9             | 0,1        | —                |
|   |             |                       | TAB                                   |                   | Up   | —                  | —              | —               | —          | —                |
|   | Mounting    | Bare die              | FC                                    | US                | Down                                       | 330×250            | 50×50          | 2,5             | 0,5        | * 1              |
|   |             |                       |                                       | C4 *4<br>(note 1) | Down                                       | 330×250<br>510×460 | 50×50<br>50×50 | 2,5<br>4,0      | 0,5<br>0,3 | * 1<br>* 2       |
|   |             |                       |                                       | GBS               | Down                                       | 330×250            | 50×50          | 2,5             | 0,5        | * 1              |
|   |             |                       |                                       | ESC、ES<br>C5      | Down                                       |                    |                |                 |            |                  |
|   |             |                       |                                       | ACF(P)            | Down                                       |                    |                |                 |            |                  |
|   |             |                       |                                       | NCF(P)            | Down                                       |                    |                |                 |            |                  |
|   |             |                       |                                       | Others            | Down                                       | —                  | —              | —               | —          | —                |
|   | Mounting    | WLP                   | Reflow<br>Resin bonding               | Down              | 510×460                                    | 50×50              | 4,0            | 0,3             | * 2        |                  |
|   |             | Package               | Reflow<br>Resin bonding               | Down              |  |                    |                |                 |            |                  |
|   |             | Rectan-<br>gular chip | Reflow<br>Resin bonding               | Down              |  |                    |                |                 |            |                  |
|   |             | Rod                   | Reflow<br>Resin bonding               | —                 |  |                    |                |                 |            |                  |
|   |             | Module<br>MEMS        | Reflow                                | Down              |  |                    |                |                 |            |                  |
| Via bonding   | Die bonding | Bare die              | Copper plating<br>Conductive<br>paste | Up                | 310×215                                    | 50×30              | 3,0            | 0,1             | * 3        |                  |
|   |             | WLP<br>Package        | Copper plating<br>Conductive<br>paste | Up                |  |                    |                |                 |            |                  |
|   | Mounting    | Rectan-<br>gular chip | Copper plating<br>Conductive<br>paste | Up                | 510×460                                    | 50×50              | 4,0            | 0,3             | * 2        |                  |
|   |             | Module<br>MEMS        | Copper plating<br>Conductive<br>paste | Up                |  |                    |                |                 |            |                  |
| Size and shape of fiducial mark   |             |                       |                                       |                   |  |                    |                |                 |            |                  |
| Size = * 1 : 0,25 ~ 0,8 mm, * 2 : 0,5 mm ~ 1,6 mm, * 3 : 0,2 ~ 1,6 mm、  |             |                       |                                       |                   |  |                    |                |                 |            |                  |
| Shape = circle, cross, square   |             |                       |                                       |                   |  |                    |                |                 |            |                  |
| NOTE 1 *4 (C4): on upper layer for terminal pitch ≥0,3 mm, on lower layer for terminal pitch <0,3 mm.                       |             |                       |                                       |                   |  |                    |                |                 |            |                  |
| NOTE 2 The above assembly requirements are for reference. Detailed requirements are to be agreed between user and supplier. |             |                       |                                       |                   |  |                    |                |                 |            |                  |

Table 20 shows the embedding methods of semiconductor devices and Table 21 for electronic devices.

**Table 20 – Mounting methods of semiconductor devices**

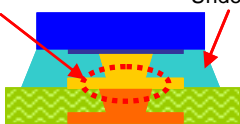
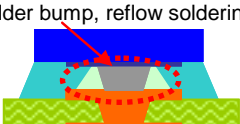
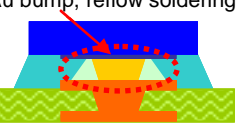

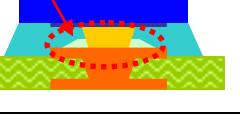


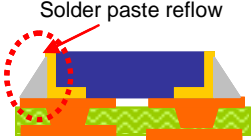

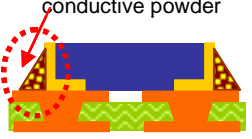
| Method              | Schematic diagram   | Short name | Name                                     | Explanation  |
|---------------------|---|------------|--|--|
| Metal bonding       | Ultrasound connection Underfill<br>      | US         | Ultra Sonic Bonding                      | Ultrasonic energy is applied between semiconductor terminal (bump) and board electrode to metal bond and then underfill thermosetting resin for mechanical reinforcement. Gold is often used for the bumps and connecting pads of the board. |
|                     | Solder bump, reflow soldering<br>        | C4         | Controlled Collapse Chip Connection      | Reflow solder bumps LSI with high temperature solder and underfill resin after cleaning the joints. Solder pre-coat, Au plating, OSP are used.   |
|                     | Au bump, reflow soldering<br>           | GBS        | Gold Bump Soldering                      | LSI with Au bumps are pressed to board with solder pre-coated pads and heated to bond the junctions, then underfill to mechanical reinforcement  |
|                     | Resin with solder powder<br>           | ESC5       | Epoxy Encapsulated Solder Connection 5th | Use solder powder mixed thermosetting adhesive and press and heat to bond the device to board. Au plating or OSP are used for the pads of board.   |
|                     | Au bump, solder pre-coat<br>           | ESC        | Epoxy Encapsulated Solder Connection     | Thermosetting resin is used between LSI bumps and solder pre-coated boards pads. Press and heat to establish electrical interconnection.   |
| Compression bonding | Au bump pressed connection<br>         | NCF (P)    | Non Conductive Film (Paste)              | Thermosetting resin is used between LSI Au bumps and boards pads. Press and heat to establish electrical interconnection. Au plating is usually used for pads on board.  |
|                     | Resin with conductive metal powder<br> | ACF (P)    | Anisotropic Conductive Film (Paste)      | Thermosetting resin mixed with conductive powder is applied to the connecting electrodes and then press and heat to obtain electrical connection. Au plating is usually used for pads on board.  |

Table 21 – Mounting method of devices

| Method | Schematic diagram   | Short name | Name                        | Explanation   |
|--------|---|------------|-----------------------------|---|
| Reflow |  | —          | Soldering                   | Bonding by reflow soldering. It is necessary to clean flux used in reflow soldering.  |
| Resin  |  | —          | Solder-resin Bonding        | Use solder powder mixed adhesive and reflow to bond the device to board.  |
|        |  | —          | Conductive adhesive bonding | Use conductive thermosetting adhesive and harden the resin after mounting a device on a board to attain electrical conduction |

## 7.5 Requirement for embedding devices

Conditions for embedding device are given in Table 22.

**Table 22 – Embedding device**

| Mounting  |             | Device          | Structure                          |          | Terminal direction<br>(to mounting face) | Component size<br>mm |                     |
|---|-------------|-----------------|------------------------------------|----------|--|----------------------|---------------------|
|   |             |                 |                                    |          |  | Max.<br>(l x w x h)  | Min.<br>(l x w x h) |
| Pad bonding   | Die bonding | Bare die        | WB                                 |          | Up                                       | 25×25×0,5            | 0,25×0,25×0,1       |
|   |             |                 | TAB                                |          | Up                                       |                      |                     |
|   | Mounting    | Bare die        | FC                                 | US       | Down                                     | 10×10×0,5            | 3,0×3,0×0,1         |
|   |             |                 |                                    | C4 *4    | Down                                     | 20×20×0,5            | 1,0×1,0×0,1         |
|   |             |                 |                                    | GBS      | Down                                     |                      |                     |
|   |             |                 |                                    | ESC、ESC5 | Down                                     |                      |                     |
|   |             |                 |                                    | ACF(P)   | Down                                     |                      |                     |
|   |             |                 |                                    | NCF(P)   | Down                                     |                      |                     |
|   |             |                 |                                    | Others   | Down                                     |                      |                     |
|   | Mounting    | WLP             | Reflow<br>Resin bonding            | Down     | 24×24×6,5                                | 0,4×0,2×0,12         |                     |
|   |             | Package         | Reflow<br>Resin bonding            | Down     |  |                      |                     |
|   |             | Rectangular     | Reflow<br>Resin bonding            | Down     | 6245                                     | 0402                 |                     |
|   |             | Rod             | Reflow<br>Resin bonding            | —        | 6245                                     | 1608                 |                     |
|   |             | Module<br>MEMS  | Reflow                             | Down     | 24×24×6,5                                | 0,4×0,2×0,12         |                     |
| Via bonding   | Die bonding | Bare die        | Copper plating<br>Conductive paste | Up       | 25×25×0,5                                | 0,25×0,25×0,1        |                     |
|   |             | WLP<br>Packages | Copper plating<br>Conductive paste | Up       | 25×25×0,5                                | 0,25×0,25×0,1        |                     |
|   | Mounting    | Rectangular     | Copper plating<br>Conductive paste | Up       | 6245                                     | 0402                 |                     |
| NOTE The above assembly requirements are for reference. Detailed requirements are to be agreed between user and supplier. |             |                 |                                    |          |  |                      |                     |

## 7.6 Design specification of device embedded substrate

### 7.6.1 General

It is strongly recommended to specify the following items in the design specification as there are many sections related to the design of the device embedded substrates even in the same organization including circuit design, structure design, device embedding board design, and actual circuit pattern design. There are also many sectors of industry to which a design section has technical correlations. There can be mutual misunderstanding leading to erroneous design misses among relevant engineers.

### 7.6.2 Items to be included in the design specification

#### 7.6.2.1 Graphical indication of device embedding substrate

Indication of external form of device embedding substrate, design drawing and of CAD data is as follows:

Perspective drawing seen from top or back surface is used. State if the drawing is seen from top or back.

EXAMPLE: Top perspective or back perspective drawing is shown in Figure 39.

It is recommended to clarify the position of the relevant layer in the cross-section drawing (see Figure 23).

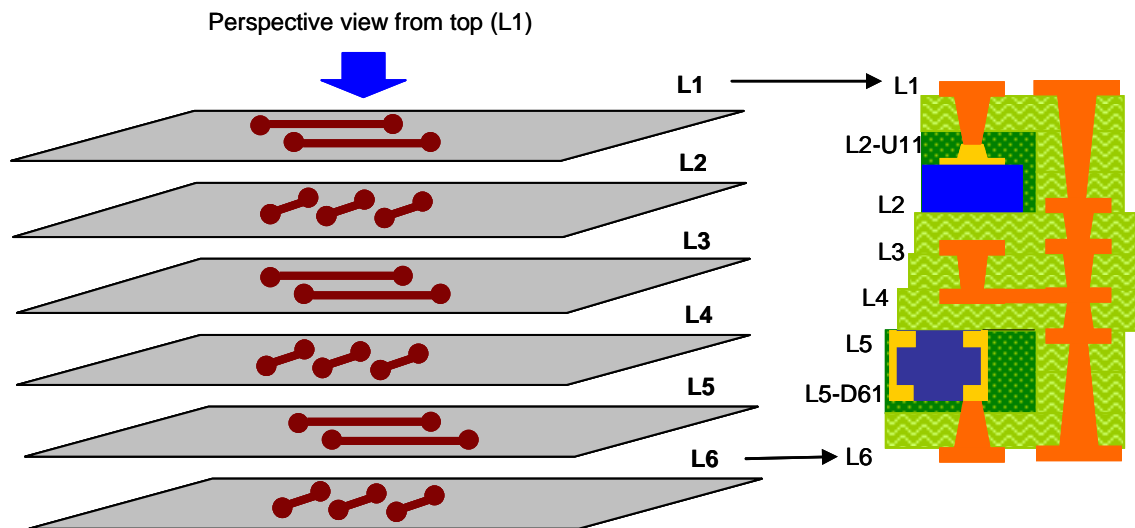


Figure 39 – Additional drawing

#### 7.6.2.2 List of parts of device embedding substrate and items to be stated

- Device name, device number, name of manufacturer
- Possibility of embedding (must be embedded in the substrate, not possible, embedding within the substrate or surface mounting, etc.)
- Table of parts of device embedding substrate and its structure

#### 7.6.2.3 Organization and structure of device embedding substrate

- Entire organization and structure of device embedding substrate
- Number of layers and types of electronic circuit board
- Thickness of each conductor layer (Cu foil + Cu plating, etc.)
- Distance between each insulating layers, and that of conductor and insulating layers
- Position of layer where device is to be embedded
- Forbidden area(s) for wiring in each layer as illustrated in Figure 40

- g) Thickness of the layer to embedded device(s)

#### 7.6.2.4 Specification of device embedding substrate

- Size and thickness of the substrate
- Treatment to the surface where device is not embedded (embedding on one side only)
- Methods of embedding and connection to the device
- Surface treatment to conductor surface (solder flux, Au plating, etc.)

#### 7.6.2.5 Embedding

- Die bonding
- Methods of mounting and interconnection
- Special treatment
  - Underfill
  - Resin mould
  - Potting
  - Others

Embedding device in wiring layer

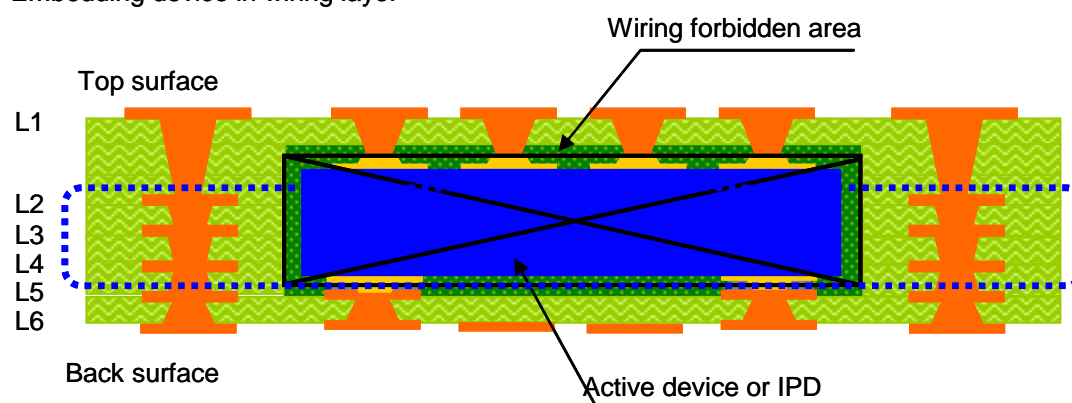


Figure 40 – Forbidden wiring area

#### 7.6.2.6 Specification of device embedding

- Embedding (resin embedding, stacking, etc.)
- Embedding material (resin, prepreg, etc.)
- Embedding conditions (heating, temperature, pressure, etc.)
- Mechanical loading condition

Embedding condition is to be agreed between user and supplier.

#### 7.6.2.7 Design specification of electronic circuit board (pattern design)

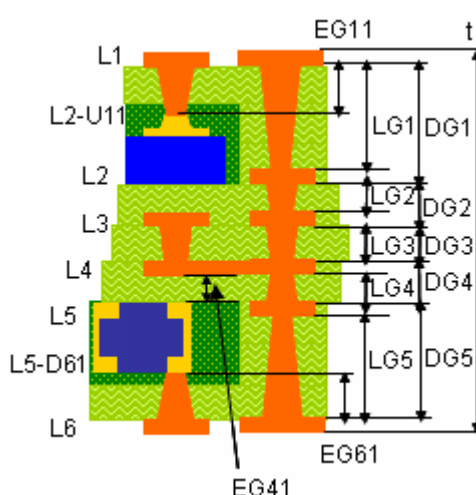
Design principle of conductor gap, via diameter, via land diameter, etc. is basically the same for regular PWB

Details of design specification are to be agreed between user and supplier

### 7.6.2.8 Template of design specification presentation

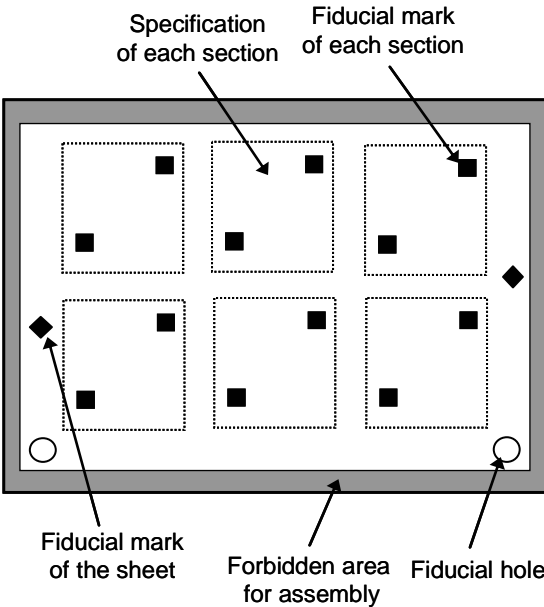
**Table 23 – Specification of device embedded substrate**

| (1) List of embedding devices |                   |                |          |              |                   |                                      |     |    |    |                       |
|-------------------------------|-------------------|----------------|----------|--------------|-------------------|--------------------------------------|-----|----|----|-----------------------|
| No.                           | Device            | Name           | Device # | Manufacturer | Manu-<br>facturer | Specification of<br>embedding device |     |    |    | Remarks               |
|                               |                   |                |          |              |                   | Must                                 | Yes | No | Or |                       |
| Case 1                        | Memory IC         | D-RAM          | MIC-002  | TM-DRAM02    | T                 | ○                                    |     |    |    |                       |
| Case 2                        | Stacked capacitor | Chip C         | CC-003   | CCK-5V10     | M                 |                                      |     |    | ○  |                       |
| Case 3                        | Stacked capacitor | Electrolytic C | DC-004   | DCK-5V200    | P                 |                                      |     | ○  |    | Low heat<br>resistive |
| 1                             |                   |                |          |              |                   |                                      |     |    |    |                       |
| 2                             |                   |                |          |              |                   |                                      |     |    |    |                       |
| 3                             |                   |                |          |              |                   |                                      |     |    |    |                       |
| 4                             |                   |                |          |              |                   |                                      |     |    |    |                       |
| 5                             |                   |                |          |              |                   |                                      |     |    |    |                       |
| 6                             |                   |                |          |              |                   |                                      |     |    |    |                       |
| 7                             |                   |                |          |              |                   |                                      |     |    |    |                       |
| 8                             |                   |                |          |              |                   |                                      |     |    |    |                       |

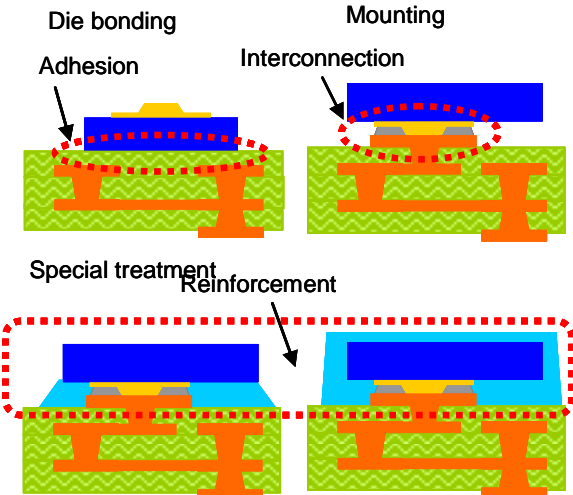
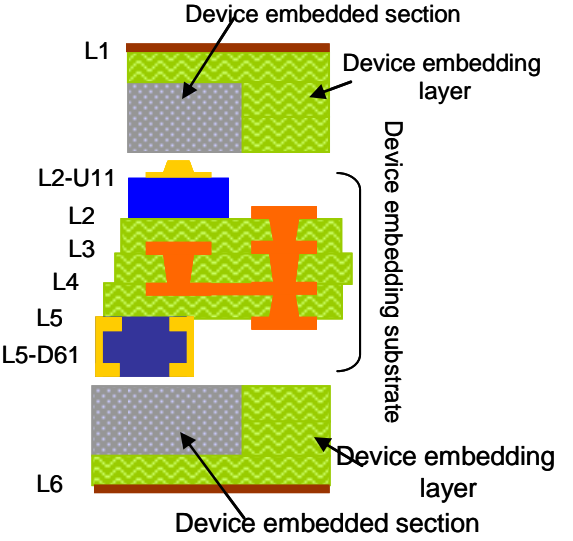
| (2) Device embedded substrate – Construction and structure                          |                |      |   |   |                            |                   |                         |                   |       |           |       |                           |       |               |      |     |      |      |      |      |
|---|----------------|------|---|---|----------------------------|-------------------|-------------------------|-------------------|-------|-----------|-------|---------------------------|-------|---------------|------|-----|------|------|------|------|
| Layer #   | 6              | Base | 4 | №   | Layer and its<br>thickness |                   | Embed-<br>ding<br>layer | Dielectric<br>gap |       | Layer tap |       | Device<br>embedded<br>gap |       |               |      |     |      |      |      |      |
| Type  | Build-up layer |      |   |   | Layer                      | Conductor<br>(µm) |                         | Name              | t(µm) | Name      | t(µm) | Name                      | t(µm) |               |      |     |      |      |      |      |
| Embedding layer   | L2, L5         |      |   |   |                            | Cu foil           |                         |                   |       |           |       |                           |       | Cu<br>plating | DG1  | LG1 | EG11 | DG2  | LG2  | EG11 |
| Construction and structure  |                |      |   |   |                            | DG3               |                         |                   |       |           |       |                           |       | LG3           | EG41 | DG4 | LG4  | EG61 | DG-5 | LG5  |
|  |                |      |   | 1   | L1                         | 12                | 20                      | —                 | —     | —         | —     | —                         | —     |               |      |     |      |      |      |      |
|   |                |      |   | 2   | L2                         | 18                | 20                      | ○                 | DG1   | 138       | LG1   | 100                       | EG11  | 40            |      |     |      |      |      |      |
|   |                |      |   | 3   | L3                         | 18                | 15                      | —                 | DG2   | 73        | LG2   | 40                        | —     | —             |      |     |      |      |      |      |
|   |                |      |   | 4   | L4                         | 18                | 15                      | —                 | DG3   | 80        | LG3   | 80                        | —     | —             |      |     |      |      |      |      |
|   |                |      |   | 5   | L5                         | 18                | 20                      | ○                 | DG4   | 73        | LG4   | 40                        | EG41  | 40            |      |     |      |      |      |      |
|   |                |      |   | 6   | L6                         | 12                | 20                      | —                 | DG-5  | 138       | LG5   | 100                       | EG61  | 40            |      |     |      |      |      |      |
|   |                |      |   | Substrate thickness (exclude solder<br>resist) (mm) |                            |                   |                         |                   | 0,57  |           |       |                           |       |               |      |     |      |      |      |      |



**Table 23 – Specification of device embedded substrate (continued)**

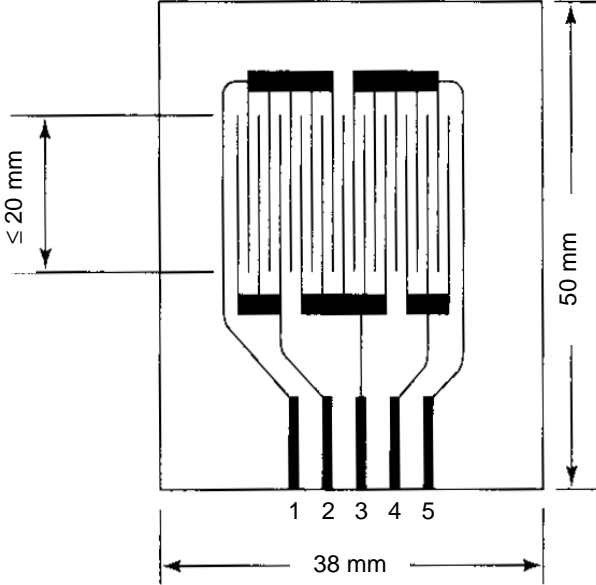
| (3) Specification of device embedding substrate                                    |                             |  |   |  |          |      |                       |           |              |
|--|-----------------------------|--|---|--|----------|------|-----------------------|-----------|--------------|
| Placement of embedding device and condition  | Nº                          | Item   |   | Specification  |          |      |                       |           |              |
|  | 1                           | Device embed-<br>ding<br>substrate                 | <table><tr><td>Layers</td><td>4 layers</td></tr><tr><td>Size</td><td>V: 250 mm X H: 320 mm</td></tr><tr><td>Thickness</td><td><math>t = 0,2</math> mm</td></tr></table> | Layers   | 4 layers | Size | V: 250 mm X H: 320 mm | Thickness | $t = 0,2$ mm |
|  | Layers                      | 4 layers   |   |  |          |      |                       |           |              |
|  | Size                        | V: 250 mm X H: 320 mm                              |   |  |          |      |                       |           |              |
|  | Thickness                   | $t = 0,2$ mm                                       |   |  |          |      |                       |           |              |
|  | 2                           | Embedding surface                                  |   | Double/single side   |          |      |                       |           |              |
|  | 3                           | Treatment of back surface in single-side embedding |   | <input type="checkbox"/> with pattern formation<br><input type="checkbox"/> without pattern formation  |          |      |                       |           |              |
|  | 4                           | Embedding method                                   |   | <input type="checkbox"/> Die bonding<br><input type="checkbox"/> Mounting<br><input type="checkbox"/> Others   |          |      |                       |           |              |
|  | 5                           | Interconnection                                    |   | <input type="checkbox"/> Via connection (Cu plating)<br><div><input type="checkbox"/> Cu plating</div> <input type="checkbox"/> Conductive paste<br><div><input type="checkbox"/> Others</div> <input type="checkbox"/> Pad connection<br><div><input type="checkbox"/> Cu plating<br/><input type="checkbox"/> Conductive paste<br/><input type="checkbox"/> Others</div> <input type="checkbox"/> Others |          |      |                       |           |              |
|  | 6                           | Solder resist                                      |   | <input type="checkbox"/> Yes <input type="checkbox"/> No   |          |      |                       |           |              |
|  | 7                           | Surface treatment                                  |   | <input type="checkbox"/> Flux<br><input type="checkbox"/> Anti-lust treatment<br><input type="checkbox"/> Other  |          |      |                       |           |              |
|  | 8                           | Reference hole                                     |   | <input type="checkbox"/> Yes <input type="checkbox"/> No   |          |      |                       |           |              |
| 9  | Fiducial mark               |  | <input type="checkbox"/> Yes <input type="checkbox"/> No  |  |          |      |                       |           |              |
| 10   | Bending after embedding (%) |  | $\pm 0,5$   |  |          |      |                       |           |              |
| 11   | Others                      |  |   |  |          |      |                       |           |              |

**Table 23 – Specification of device embedded substrate (continued)**

| (4) Specification of device embedding   |    |                            |  |
|---|----|----------------------------|--|
| Construction of device embedding and condition  | No | Item                       | Specification  |
| <p>1. Structure</p>  <p>2. Structure of device embedded substrate</p>  <p>NOTE Cutting of embedded section may be different by embedding method and to be agreed between user and supplier.</p> | 1  | Assembly                   | <input type="checkbox"/> Die bonding<br><input type="checkbox"/> Adhesives<br><input type="checkbox"/> Others<br><input type="checkbox"/> Mounting<br><input type="checkbox"/> Soldering<br><input type="checkbox"/> Conductive paste<br><input type="checkbox"/> Others<br><input type="checkbox"/> Special treatment<br><input type="checkbox"/> Underfill<br><input type="checkbox"/> Resin mold<br><input type="checkbox"/> Potting<br><input type="checkbox"/> Others |
|   | 2  | Embedding method           | <input type="checkbox"/> Stacking<br><input type="checkbox"/> Resin molding<br><input type="checkbox"/> Molding<br><input type="checkbox"/> Others   |
|   | 3  | Embedding material         | <input type="checkbox"/> Glass epoxy prepreg<br><input type="checkbox"/> Epoxy resin<br><input type="checkbox"/> Polyimide prepreg<br><input type="checkbox"/> Polyimide resin<br><input type="checkbox"/> Others  |
|   | 4  | Treatment before embedding | <input type="checkbox"/> Flux cleaning<br><input type="checkbox"/> General cleaning<br><input type="checkbox"/> Baking<br><input type="checkbox"/> Others  |
|   | 5  | Embedding condition        | Temperature ( $\leq 160^{\circ}\text{C}$ )<br>Pressure ( $\leq 3\text{ MPa} \sim 4\text{ MPa}$ )   |
|   | 6  | Mechanical stress          | To be agreed between user and supplier   |
|   | 7  | Check of embedding device  | To be agreed between user and supplier   |
|   | 8  | Others                     |  |
| NOTE Properties of front and back surface after embedding, solder resist, surface treatment and alike should be in accordance with the general specification of electronic circuit boards.  |    |                            |  |

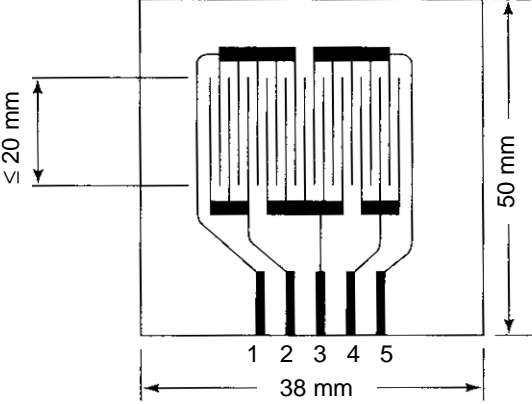
Annex A  
(informative)

Specimen for surface resistance measurement of electronic circuit board

| Item  | Surface insulation resistance of electronic circuit board   |
|---|---|
| Specimen  | <div><p>Specimen has the conductor pattern shown and covered by solder resist. The conductor gap is the minimum conductor gap used in the actual wiring board.</p><p><b>Figure A.1 – Test pattern for surface insulation resistance measurement</b></p></div>  |
| Equipment   | Equipment to be used are the equipment specified in JIS C 1302, insulation resistance meter, standard resistor, universal shunt resistor and galvanometer calibrated to an accuracy of $\pm 10\%$ .   |
| Conditioning  | <p>(1) As is<br/>Specimen is kept at <math>85\text{ }^{\circ}\text{C} \pm 2\text{ }^{\circ}\text{C}</math> for 4 h and then left at <math>20\text{ }^{\circ}\text{C} \pm 2\text{ }^{\circ}\text{C}</math> with relative humidity of <math>60\% \pm 10\%</math> for <math>24\text{ h} \pm 4\text{ h}</math>.</p> <p>(2) Humidity (temperature – humidity cycle)<br/>Specimen is treated for 10 cycles with the condition specified in JIS C 5012, 9.4 (humidity test – temperature – humidity cycle), and then measured at temperature of <math>20\text{ }^{\circ}\text{C} \pm 2\text{ }^{\circ}\text{C}</math> and relative humidity of <math>60\% \pm 10\%</math> within 30 min to 60 min after conditioning.</p> <p>(3) Humidity (steady state)<br/>Specimen is treated at <math>40\text{ }^{\circ}\text{C} \pm 2\text{ }^{\circ}\text{C}</math> and relative humidity of 90 % to 95 % for 96 h with the condition specified in JIS C 5012, 9.5 (humidity test – steady state), and then measured at temperature at <math>20\text{ }^{\circ}\text{C} \pm 2\text{ }^{\circ}\text{C}</math> and relative humidity of <math>60\% \pm 10\%</math> within 30 min to 60 min after conditioning.</p> |
| Test  | DC voltage of either $10\text{ V} \pm 1\text{ V}$ , $100\text{ V} \pm 15\text{ V}$ or $500\text{ V} \pm 50\text{ V}$ is applied for 1 min and then insulation resistance of the specimen is measured as the DC voltage is applied.  |
| NOTE The test method described above is for information. Actual test method should be agreed between user and supplier. |   |

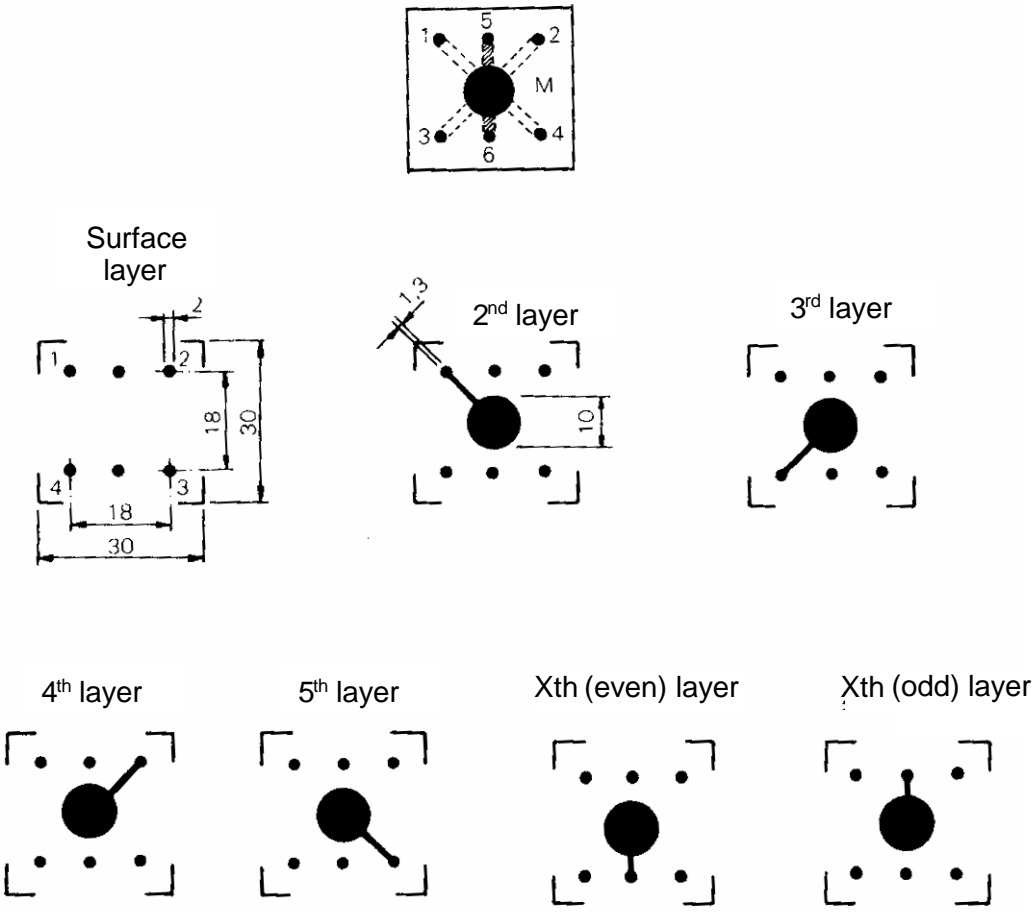
**Annex B**  
(informative)

**Insulation resistance measurement of inner layer  
of electronic circuit board**

|   |  |
|---|--|
| Item  | <div></div> <p>Insulation resistance measurement of inner layer of electronic circuit board (steady state humidity test – temperature – humidity cycle and steady state)</p> <p>Specimen has the conductor pattern shown and covered by solder resist. The conductor gap is the minimum conductor gap used in actual wiring board.</p> <p><b>Figure B.1 – Test pattern for insulation resistance measurement of inner layers</b></p> |
| Specimen  |  |
| Equipment   |  |
| Condition-<br>ing   |  |
| Test  | Same as Annex A  |
| NOTE The test method described above is for information. Actual test method should be agreed between user and supplier. |  |

Annex C  
(informative)

Specimen for interlayer insulation resistance measurement  
for multilayer circuit board

|   |   |
|---|---|
| Item  | Measurement of interlayer insulation resistance measurement for multilayer circuit board (steady state, humidity – temperature-humidity cycle and steady state)   |
| Specimen  | <p>The conductor patterns for this test in specimen are as follows.<br/>Values for the holes are: <math>\phi</math> 10 mm, nominal hole diameter of 0,8 mm, and nominal land diameter of 2 mm.</p> <div></div> <p><b>Figure C.1 – Test patterns for interlayer insulation resistance measurement</b></p> |
| Equipment   | Same as in Annex A  |
| Conditioning  |   |
| Test  | Either 100 V $\pm$ 15 V or 500 V $\pm$ 50 V DC voltage is applied to specimen as specified in the relevant specification for 1 min and then the insulation resistance is measured while the DC voltage is applied to the specimen.  |
| <p><b>NOTE</b> The test method described above is for information. Actual test method should be agreed between user and supplier.</p> |   |

## Annex D (informative)

### Electronic wiring board product system

The relation of electronic wiring board product system and the device embedded system as described in this document is shown in Figure D.1.

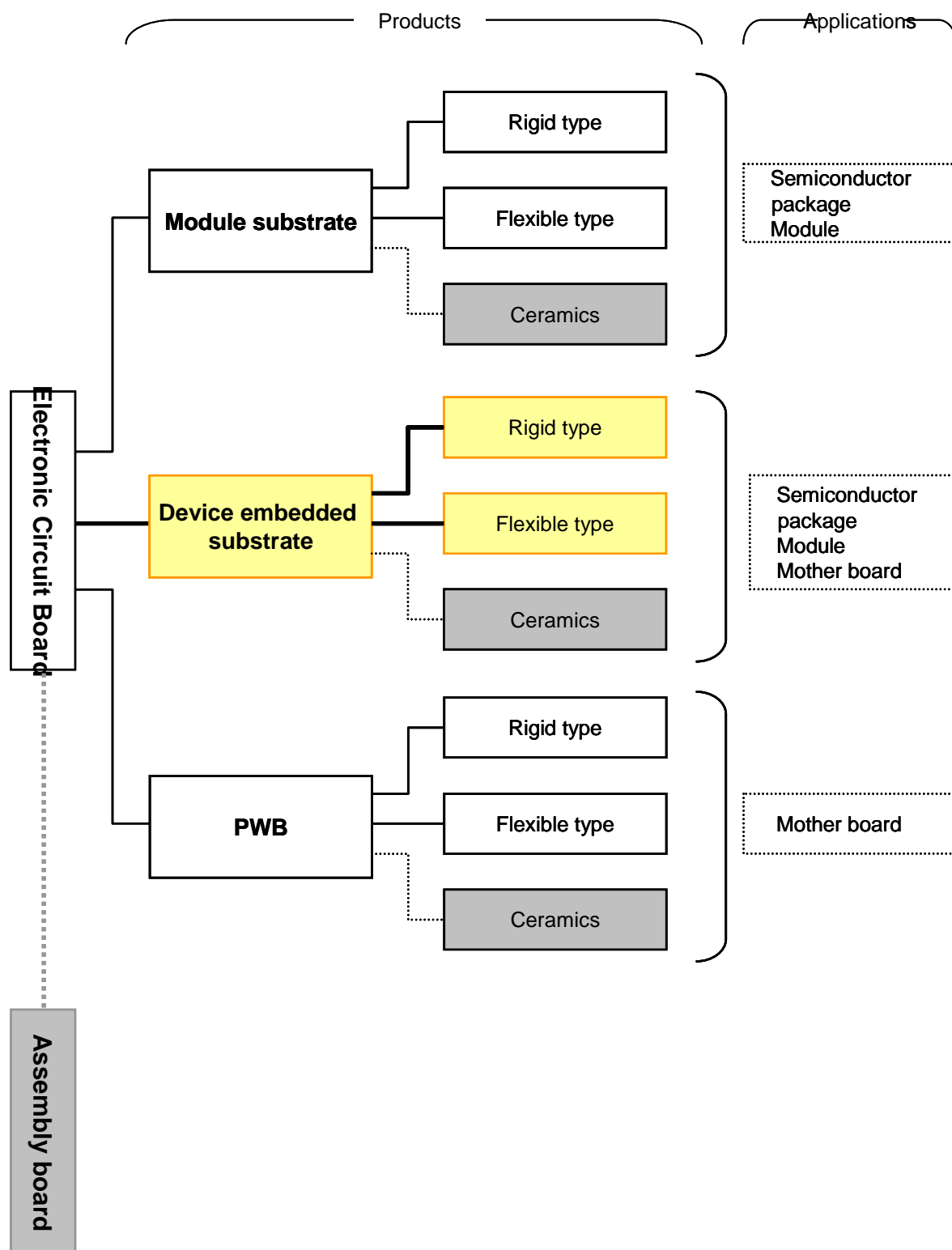


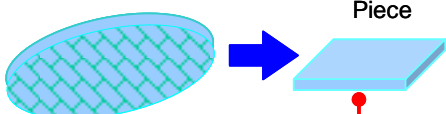
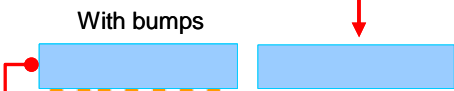

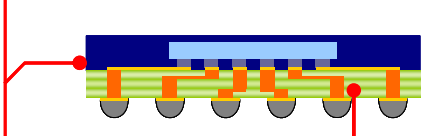



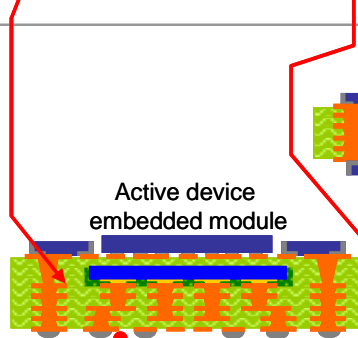
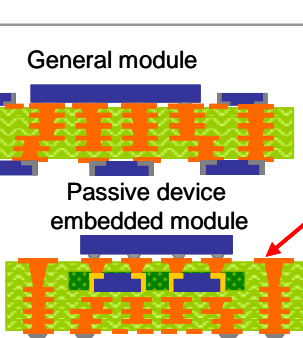
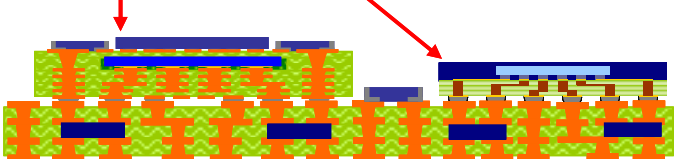
Figure D.1 – Electronic wiring board product system

## Annex E (informative)

### Steps of electronic circuit board assembly and main applications

Steps of electronic circuit board assembly and main applications are shown in Table E.1.

**Table E.1 – Steps of electronic circuit board assembly and main applications**

| Layer | Name  | Schematic structure  |  | Classifications and applications                                |
|-------|---|--|--|---|
|       |   | Active device  | Passive device   |   |
| 0     | Wafer                                       |     |  | Silicon substrate   |
| 1     | Bear die (bear chip)                        |     |  | Silicon substrate   |
| 2     | Wafer level package                         |    |  | Silicon substrate + mold  |
| 3     | package                                     |   |  | Module substrate  |
| 4     | Device embedded board                       |   |  | Module substrate<br>PWB   |
| 5     | Module                                      |   |  | General module<br>Module substrate<br>Device embedded substrate |
| 6     | Mother board (device embedded Mother board) |  |  | PWB   |

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