INTERNATIONAL STANDARD

IEC 62258-5

First edition
2006-08

Semiconductor die products –

Part 5: Requirements for information concerning electrical simulation

Reference number
IEC 62258-5:2006(E)

Publication numbering

As from 1 January 1997 all IEC publications are issued with a designation in the 60000 series. For example, IEC 34-1 is now referred to as IEC 60034-1.

Consolidated editions

The IEC is now publishing consolidated versions of its publications. For example, edition numbers 1.0, 1.1 and 1.2 refer, respectively, to the base publication, the base publication incorporating amendment 1 and the base publication incorporating amendments 1 and 2.

Further information on IEC publications

The technical content of IEC publications is kept under constant review by the IEC, thus ensuring that the content reflects current technology. Information relating to this publication, including its validity, is available in the IEC Catalogue of publications (see below) in addition to new editions, amendments and corrigenda. Information on the subjects under consideration and work in progress undertaken by the technical committee which has prepared this publication, as well as the list of publications issued, is also available from the following:

- **IEC Web Site (www.iec.ch)**

- **Catalogue of IEC publications**

  The on-line catalogue on the IEC web site (www.iec.ch/searchpub) enables you to search by a variety of criteria including text searches, technical committees and date of publication. On-line information is also available on recently issued publications, withdrawn and replaced publications, as well as corrigenda.

- **IEC Just Published**

  This summary of recently issued publications (www.iec.ch/online_news/ justpub) is also available by email. Please contact the Customer Service Centre (see below) for further information.

- **Customer Service Centre**

  If you have any questions regarding this publication or need further assistance, please contact the Customer Service Centre:

  Email: custserv@iec.ch
  Tel: +41 22 919 02 11
  Fax: +41 22 919 03 00

INTERNATIONAL STANDARD

IEC 62258-5

First edition
2006-08

Semiconductor die products –

Part 5:
Requirements for information concerning electrical simulation

International Electrotechnical Commission, 3, rue de Varembé, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch

Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE M

For price, see current catalogue

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DIE PRODUCTS –

Part 5: Requirements for information concerning electrical simulation

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62258-5 has been prepared by IEC technical committee 47: Semiconductor devices.

This standard should be read in conjunction with IEC 62258-1 and IEC 62258-2.

The text of this standard is based on the following documents:

FDIS	Report on voting
47/1869/FDIS	47/1882/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The structure of IEC 62258, as currently conceived, consists of the following parts under the general title *Semiconductor die products*:

Part 1: Requirements for procurement and use

Part 2: Exchange data formats

Part 3: Recommendations for good practice in handling, packing and storage (Technical Report)

Part 4: Questionnaire for die users and suppliers (Technical Report) (in preparation)

Part 5: Requirements for information concerning electrical simulation

Part 6: Requirements for information concerning thermal simulation

Part 7: XML schema for data exchange (Technical Report) (in preparation)

Further parts may be added as required.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

This standard is based on the work carried out in the ESPRIT 4th Framework project GOODDIE which resulted in the publication of the ES 59008 series of European specifications. Organisations that helped prepare this part of IEC 62258 includes the ESPRIT ENCAST project, the Die Products Consortium, JEITA, JEDEC and ZVEI.

SEMICONDUCTOR DIE PRODUCTS –

Part 5: Requirements for information concerning electrical simulation

1 Scope

This part of IEC 62258 has been developed to facilitate the production, supply and use of semiconductor die products, including:

– wafers;
– singulated bare die;
– die and wafers with attached connection structures;
– minimally or partially encapsulated die and wafers.

This part of IEC 62258 specifies the information required to facilitate the use of electrical data and models for simulation of the electrical behaviour and verification of the correct functionality of electronic systems that include bare semiconductor die, with or without connection structures, and/or minimally packaged semiconductor die. It is intended to assist all those involved in the supply chain for die devices to comply with the requirements of IEC 62258-1 and IEC 62258-2.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62258-1, *Semiconductor die products – Part 1: Requirements for procurement and use*

IEC 62258-2, *Semiconductor die products – Part 2: Exchange data formats*

3 Terms and definitions

For the purposes of this document, the terms, definitions and acronyms as given in IEC 62258-1 apply.

4 General

To comply with IEC 62258-1, suppliers of die devices shall furnish information, which is necessary and sufficient for users of the devices at all stages of design, procurement, manufacture and test of products containing them..

Whilst it is expected that much of the information supplied will be in the public domain and available from such sources as manufacturers' data sheets, this standard does not place an obligation on a supplier to make information public. Any information that a supplier considers to be proprietary or commercially sensitive may be supplied under the terms of a non-disclosure agreement.

Requirements and recommendations provided in this standard apply to electrical simulation models used to perform the following simulations:

– analysis of the signal propagation within the electronic system;
– verification of the correct functionality of the electronic system;
– verification of the timing requirements;
– verification of the testability.

Supporting information on the use of electrical simulation models is provided in Annex A.

5 Requirements for information on electrical simulation models

5.1 Information on the electrical simulation model

5.1.1 General

Where a simulation model is provided, the information as defined in the following subclauses shall be given.

5.1.2 Model file name

The name of the file containing the model shall be given.

5.1.3 Creation date

The date on which the model file was created shall be given.

5.1.4 Model description

A description of the model shall be provided in sufficient detail for a user to understand its scope and apply the corresponding simulator correctly.

5.1.5 Model source

The source and originator of the model shall be stated.

5.1.6 Simulation program

The name(s) of the simulation program(s) that will accept the model file as valid input shall be given.

5.1.7 Program version

The version(s) of the simulation program(s) that are compatible with the given file shall be given.

5.1.8 Compliance level

The level(s) of the simulation program(s) with which the model file complies shall be given (for example SPICE level 3).

5.1.9 Model scope

The scope of the model shall be given, including any limitations in its use (for example VHDL behavioural model).

5.2 Information on device connectivity

5.2.1 General

The appropriate information, as data and/or model(s), describing the component's connectivity features or characteristics should be stated.

NOTE Examples of simulation models include IBIS (ANSI/EIA-656), SPICE, IMIC (JEITA ED-5302) and Touchstone.

The following parameters are important for bare die and low frequency devices where terminal-to-terminal interference can be disregarded.

5.2.2 Pad capacitance

The capacitance of the input, output, power and ground pads of the device should be stated. The node to which the capacitance is measured should also be stated.

5.2.3 Input buffer

The electrical model(s) of the input buffer(s) should be stated. The type and compliance level of the model(s) should also be stated.

5.2.4 Output buffer

The electrical model(s) of the output buffer(s) should be stated. The type and compliance level of the model(s) should also be stated, as required in 5.1.

5.2.5 ESD protection

A description of the ESD protection circuitry, if any, should be given. If an ESD model is provided, the type and compliance level of the model shall also be stated, as required in 5.1.

5.3 Information on the timing simulation model

The appropriate model(s) describing the component's behaviour in the time dimension should be provided. Where required by the simulator the model of the device should be provided as an electronic file, so that it can be directly used as input to the simulation program. This is primarily intended for digital devices.

NOTE Examples of timing simulation models include VITAL, VERILOG, IEEE 1029.1 Waveform and Vector Exchange Specification and IEC 61691-3-4, Timing expression in VHDL (in preparation).

5.4 Information on connection redistribution

5.4.1 General

Where the electrical connection points or terminals of the device have been modified or altered by use of one or more redistribution layers, information concerning the electrical parameters of any redistribution traces should be given. Information on multi-pin connections should be given in matrix form.

5.4.2 Redistribution trace resistance

The resistance of the redistribution traces, if any, with respect to the initial or original contact should be stated. Any assumed or known tolerances should also be stated.

5.4.3 Redistribution trace capacitance

The self and mutual capacitance of the redistribution traces, if any, should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.

5.4.4 Redistribution trace inductance

The self and mutual inductance of the redistribution traces, if any, should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.

5.5 Information on package terminals

5.5.1 General

Where the electrical connection points or terminals of the device have been modified by use of an alternate connection method, such as the addition of bumps, balls or bond-wires, information concerning the electrical parameters of any package terminals should be given. Information on multi-pin connections is to be given in matrix form. One suggested format for the matrix could be in CLGR (capacitance-inductance-conductance-resistance) format.

5.5.2 Terminal resistance

The resistance of the package terminal (wire, bump, lead or ball) with respect to the original terminal should be stated. Any assumed or known tolerances should also be stated.

5.5.3 Terminal capacitance

The self and mutual capacitance of the package terminal (wire, bump, lead or ball) should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.

5.5.4 Terminal inductance

The self and mutual inductance of the package terminal (wire, bump, lead or ball) should be stated, preferably in matrix form. Any assumed or known tolerances should also be stated.

Annex A
(informative)

Supporting information

A.1 General

For the purposes of this standard, an electronic system is regarded as being composed of a number of processing elements (active components) that apply non-linear transformations to the electrical signals, connected to each other and to other electronic systems by means of an interconnection network that ideally leaves the electrical signals unaltered (interconnections on the substrate) or applies linear transformations to them (passive components) and consisting of ICs and discrete components assembled on an interconnection substrate or board.

The simulation of the electrical behaviour and verification of the correct functionality of an electronic system are performed at the following levels:

– analysis of the signal propagation;
– verification of the correct functionality;
– verification of the timing requirements;
– verification of the testability.

The simulation of an electronic system aims to check whether its electrical design performs the desired linear and non-linear transformations according to the specifications.

The linear transformations are checked by the analysis of the signal propagation. The non-linear transformations are verified by the verification of the correct functionality and timing requirements. The above applies to digital, analogue and RF electronic systems.

A.2 Analysis of the signal propagation

In order to perform a proper analysis of the signal propagation of an electronic system, an interconnection block is defined as consisting of

– the output buffer of the active component that generates the signal (transmitting component);
– the interconnection network;
– the input buffer of the active component receiving the signal (receiving component).

For this reason the models of the input and output buffers of a device are required.

A.3 Verification of the correct functionality

For analogue and RF systems, this part corresponds to the analysis of the signal propagation.

For digital systems, this part implies the comparison of sequences of logical states against given specifications, including compliance to the time frame.

As far as the verification of the functionality of an electronic system is concerned, there are no additional requirements for systems using bare die, or minimally packaged components, with respect to systems using packaged components.

A.4 Verification of the timing requirements

The timing behaviour of electronic systems using bare die and/or minimally packaged components differs from the situation with packaged components, as the interconnection load to be driven is different. Therefore, timing models describing the component's behaviour with different interconnection loads should be provided.

A.5 Verification of the testability

The level of observability and controllability of electronic systems using bare die and/or minimally packaged components may differ from the situation with packaged components due to a reason, which is independent from the presence of the package. Bare die and minimally packaged components tend to be used in High Density Packaging systems, which traditional board-level testing may not be suited for, due to their small size. In this sense, a good practice in Design For Testability is strongly recommended when designing such systems, and components fulfilling the requirements of the IEEE/ANSI 1149.1 Standard Test Access Port and Boundary Scan Architecture, should be used whenever possible.

Bibliography

IEC 61691-1-1, *Behavioural languages – Part 1-1: VHDL language reference manual*

IEC 61691-2, *Behavioural languages – Part 2: VHDL multilogic system for model interoperability*

IEC 62014-1 *Electronic design automation libraries – Part 1: Input/output buffer information specifications (IBIS version 3.2)*

EIA/JESD49, *Procurement Standard for Known Good Die (KGD) February 1996*

IEEE 1029.1, *Waveform and Vector Exchange Specification*

IEEE 1076, VHSIC *Hardware Description Language*

IEEE/ANSI 1149.1, *Standard Test Access Port and Boundary Scan Architecture*

IEEE 1364, IEEE *Standard Hardware Description Language Based on the Verilog® Hardware Description Language*

SPICE, *as defined by the EECS Department of the University of California at Berkeley*

JEITA ED-5302 IMIC *'I/O interface Model for IC' is a Draft Standard being worked on by the Japan Electronics and Information Technology Industries Association (JEITA).*

Standards Survey

The IEC would like to offer you the best quality standards possible. To make sure that we continue to meet your needs, your feedback is essential. Would you please take a minute to answer the questions overleaf and fax them to us at +41 22 919 03 00 or mail them to the address below. Thank you!

Customer Service Centre (CSC)

International Electrotechnical Commission
3, rue de Varembé
1211 Genève 20
Switzerland

or

Fax to: **IEC**/CSC at +41 22 919 03 00

Thank you for your contribution to the standards-making process.

Nicht frankieren
Ne pas affranchir

Non affrancare
No stamp required

A Prioritaire

RÉPONSE PAYÉE

SUISSE

Customer Service Centre (CSC)
International Electrotechnical Commission
3, rue de Varembé
1211 GENEVA 20
Switzerland

Q1 Please report on **ONE STANDARD** and **ONE STANDARD ONLY**. Enter the exact number of the standard: *(e.g. 60601-1-1)*

.....

Q2 Please tell us in what capacity(ies) you bought the standard *(tick all that apply).* I am the/a:

purchasing agent ❑
librarian ❑
researcher ❑
design engineer ❑
safety engineer ❑
testing engineer ❑
marketing specialist ❑
other.....

Q3 I work for/in/as a: *(tick all that apply)*

manufacturing ❑
consultant ❑
government ❑
test/certification facility ❑
public utility ❑
education ❑
military ❑
other.....

Q4 This standard will be used for: *(tick all that apply)*

general reference ❑
product research ❑
product design/development ❑
specifications ❑
tenders ❑
quality assessment ❑
certification ❑
technical documentation ❑
thesis ❑
manufacturing ❑
other.....

Q5 This standard meets my needs: *(tick one)*

not at all ❑
nearly ❑
fairly well ❑
exactly ❑

Q6 If you ticked NOT AT ALL in Question 5 the reason is: *(tick all that apply)*

standard is out of date ❑
standard is incomplete ❑
standard is too academic ❑
standard is too superficial ❑
title is misleading ❑
I made the wrong choice ❑
other .....

Q7 Please assess the standard in the following categories, using the numbers:
(1) unacceptable,
(2) below average,
(3) average,
(4) above average,
(5) exceptional,
(6) not applicable

timeliness.....
quality of writing.....
technical contents.....
logic of arrangement of contents .....
tables, charts, graphs, figures.....
other .....

Q8 I read/use the: *(tick one)*

French text only ❑
English text only ❑
both English and French texts ❑

Q9 Please share any comment on any aspect of the IEC that you would like us to know:

.....
.....
.....
.....
.....
.....
.....
.....
.....
.....
.....
.....

ISBN 2-8318-8785-2

ICS 31.080.99

Typeset and printed by the IEC Central Office
GENEVA, SWITZERLAND