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TECHNICAL SPECIFICATION

Integrated circuits – Measurement of impulse immunity – Part 2: Synchronous transient injection method

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FOREWORD

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 62215-2, which is a technical specification, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
47A/762/DTS	47A/769A/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62215 series, under the general title *Integrated circuits – Measurement of impulse immunity*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

In future standards, test methods and measurement procedures will be given for transient immunity of integrated circuits:

– ESD pulse with resemblance to IEC 61000-4-2;

– EFT pulse with resemblance to IEC 61000-4-4;

– Surge pulse with resemblance to IEC 61000-4-5.

INTEGRATED CIRCUITS – MEASUREMENT OF IMPULSE IMMUNITY –

Part 2: Synchronous transient injection method

1 Scope

IEC/TS 62215-2, which is a technical specification, contains general information and definitions on the test method to evaluate the immunity of integrated circuits (ICs) against fast conducted synchronous transient disturbances. This information is followed by a description of measurement conditions, test equipment and test set-up as well as the test procedures and the requirements on the content of the test report.

The objective of this technical specification is to describe general conditions to obtain a quantitative measure of immunity of ICs establishing a uniform testing environment. Critical parameters that are expected to influence the test results are described. Deviations from this specification should be explicitly noted in the individual test report.

This synchronous transient immunity measurement method, as described in this specification, uses short impulses with fast rise times of different amplitude, duration and polarity in a conductive mode to the IC. In this method, the applied impulse should be synchronized with the activity of the IC to make sure that controlled and reproducible conditions can be assured.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1 Ω/150 Ω direct coupling method*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 62215-1 (in preparation), as well as the following, apply.

3.1
auxiliary equipment
AE
equipment not under test that is nevertheless indispensable for setting up all the functions and assessing the correct performance (operation) of the equipment under test (EUT) during its exposure to the disturbance

3.2
coupling network
electrical circuit for transferring energy from one circuit to another with well-defined impedance and known transfer characteristics

3.3
device under test
DUT
device, equipment or system being evaluated

NOTE In this technical specification, it refers to a semiconductor device being tested.

3.4
electromagnetic compatibility
EMC
ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment

[IEC 60050(161):1990, definition 161-01-07]

3.5
electrical noise
unwanted electrical signals, which produce undesirable effects in the circuits of the control system in which they occur

[IEEE std 100-1992-518-1982]

3.6
immunity (to a disturbance)
ability of a device, equipment or system to perform without degradation in the presence of an electromagnetic disturbance

3.7
jitter (time related)
short-term variations of the significant instants of a digital signal from their ideal positions in time

3.8
RF ambient
totality of electromagnetic phenomena existing at a given location

3.9
transient
pertaining to or designating a phenomenon or a quantity which varies between two consecutive steady states during a time interval which is short compared with the time-scale of interest

[IEC 60050(161):1990, definition 161-02-01]

4 General

4.1 Introduction

This immunity test method describes synchronous transient injection on digital and mixed-signal ICs. In this method an impulse is injected into the V_{ss}-, V_{dd}-pin(s) or I/Os successively on the IC subjected to the test.

4.2 Measurement philosophy

This method is related to the 1 Ω resistor method, see IEC 61967-4. In this method a 1 Ω resistor is added in series with the V_{dd}, V_{ss} pin(s) of the IC. It is assumed that the voltage drop across the 1 Ω resistor in parallel with the DC by-pass inductance is very small. For injecting the impulse, a broadband coupling network is defined. The impulse injection is synchronized to a program loop signal generated by the IC.

One cycle of this response signal is considered as one program loop. The aim of this measurement method is to insert a synchronous but delayed impulse into the IC, related to the program loop. The total time of one program loop period is calculated and then it is

divided into small time steps. At every delay step, a single impulse per program loop is inserted into the IC and its response is measured.

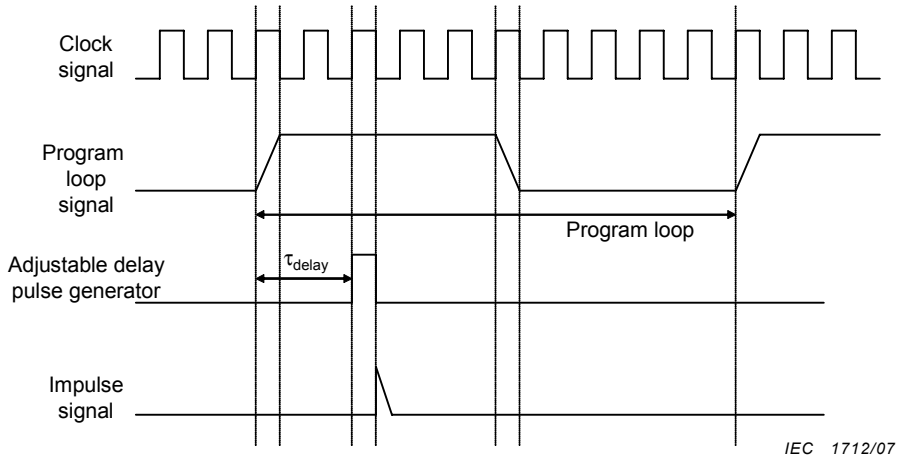


Figure 1 – Synchronous transient injection immunity methodology waveforms

Figure 1 shows the relevant signals occurring in this synchronous transient immunity test. The clock signal is used to run the digital IC and the program loop signal is used as a reference and response signal. A predetermined adjustable delay is used to shift the impulse delay time; τ_{delay}, along the program loop.; τ_{delay} is typically a fraction (≤ 0,1) of the rise time of the clock signal. The rising edge of the program loop signal, synchronized with the rising edge of the clock signal, is considered as a fixed reference point, see Figure 1, second line; program loop sync circuitry. Thereafter, the impulse is inserted and the edges of the response signals have to be observed. After every program loop, the delay step is increased and the injection moment of the impulse is shifted. In this way, the full scan can be completed through the program cycle to evaluate the impulse immunity.

The test method will show sensitive time windows, i.e. modes of operation at which the device is sensitive. The non-sensitive time windows can be skipped thereafter while repeating the measurements.

NOTE This measurement methodology is different from to the stochastic i.e. random application of impulses.

4.3 Set-up concept

In Figure 2, the block diagram of the test set-up for the synchronous impulse immunity test is given. A trigger signal, e.g. generated by the DUT, is used as an indication to start the measurement. This signal is also used to trigger the delay pulse generator to produce the programmable delay. The delayed pulse triggers the impulse generator that produces an impulse. This impulse is then inserted into the DUT through a suitable coupling network. Measurement equipment such as an oscilloscope or time domain analyser is used to measure the response of the DUT versus the delay of the impulse in the program loop. This measuring equipment is also synchronized with the test signal to acquire the response data over a program loop. A computer interface is used to control the measurement test set-up and to acquire the response data from the test set-up.

In general, the test set-up shall be in accordance with the specific test procedure as described in the future IEC 62215-1. All the test relevant parameters shall be recorded as exactly as possible to ensure that the test results become reproducible.

4.4 Response signal

The response signal is a signal generated by the IC under test (DUT). A clock signal may be externally provided. If the DUT is a microcontroller, then the response signal can be

generated by a microcontroller by loading a small software program. If DUT is a logic device, then the output signal of the logic device is considered as the response signal. The immunity can be quantified based on jitter occurring in the response signal (or any other errors) due to the impulse disturbances applied.

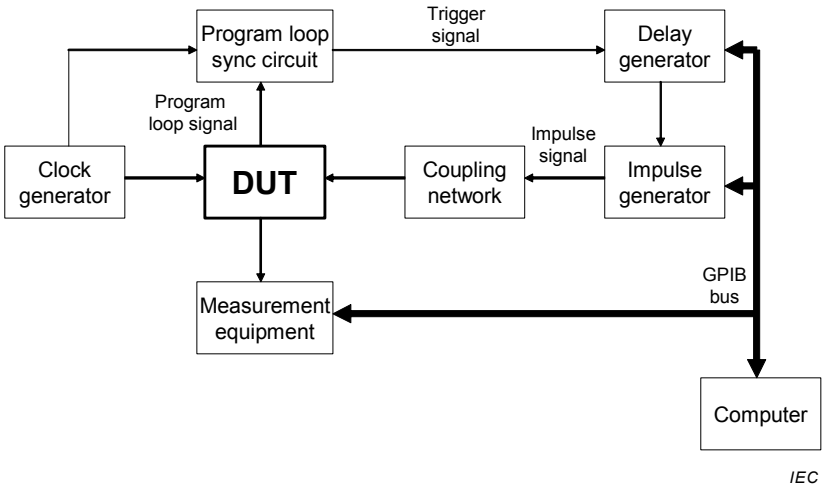


Figure 2 – Test set-up diagram for synchronous transient injection immunity testing

4.5 Coupling networks

4.5.1 General

The coupling network will always introduce a time delay for the applied impulse signal since a network presents a path (line) of a certain physical length for the signal.

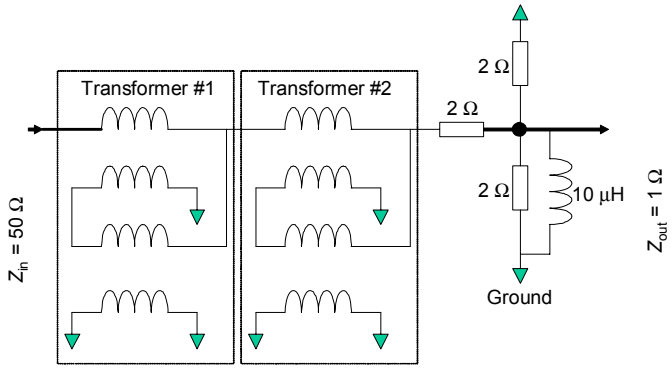
4.5.2 Design of coupling networks

For synchronous transient immunity testing, it is important that the coupling networks have a flat transfer characteristics over a broad frequency range. This flatness will help to couple the impulse to the DUT without disturbing its impulse characteristics and will maintain the normal operating conditions of the DUT. The coupling networks are designed in such a way that the impulses of different amplitude, duration, rise and fall time can be injected into the DUT ports.

4.5.3 Coupling network for the ground/ V_{ss} pin(s)

The principle used to couple the impulse into the ground/ V_{ss} pin(s) is via a 1 Ω resistor connected in series with a ground pin(s) of the IC and where the impulse signal is applied in series equivalently. Figure 3 shows an example of a coupling network.

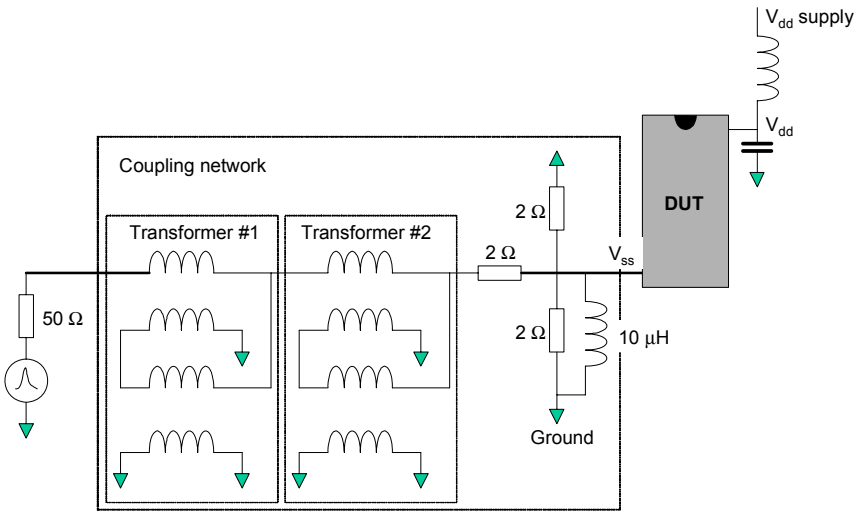
Two 4:1 transmission line (Guanella) transformers are used. A resistor network follows these two transformers together with an RF choke. When the two TL (transmission line) transformers having impedance ratio 4:1 are connected in series, it results in an impedance step down from 50 Ω to about 3 Ω. The resistor network of 3 Ω is connected as an RF load. To minimize the DC voltage drop across the 1 Ω resistor, an RF choke of 10 μH is connected in parallel. This inductor acts as a DC short-circuit and represents high impedance for the impulse signal which is referred to a parallel impedance of 1 Ω. The overall attenuation in the coupling network is approximately 22 dB; 6 dB attenuation by each transformer and 10 dB by the resistive network.



IEC 1714/07

Figure 3 – Circuit diagram of the coupling network for ground/ V_{ss} pin(s) of an IC

While designing the coupling network, care should be taken that the transfer characteristic is flat enough (-3 dB) over the bandwidth of 1 MHz to 1 GHz.



IEC 1715/07

Figure 4 – Method to impose synchronous transient injection into ground/ V_{ss} pin(s)

When an impulse is applied to the coupling network, the impulse energy appears across the 1 Ω resistor with a 22 dB attenuation. Since this 1 Ω resistor is in series with the ground/ V_{ss} pin(s) of the DUT, i.e. the IC, it suffers from such an impulse disturbance. Figure 4 shows how the coupling network is connected to the IC.

4.5.4 Coupling network for the supply/ V_{dd} pin(s)

To couple an impulse to the supply/ V_{dd} pin(s), one can use the same coupling network as used for the ground pin(s), but with a modification as shown in Figure 5 to by-pass the DC voltage on the supply/ V_{dd}.

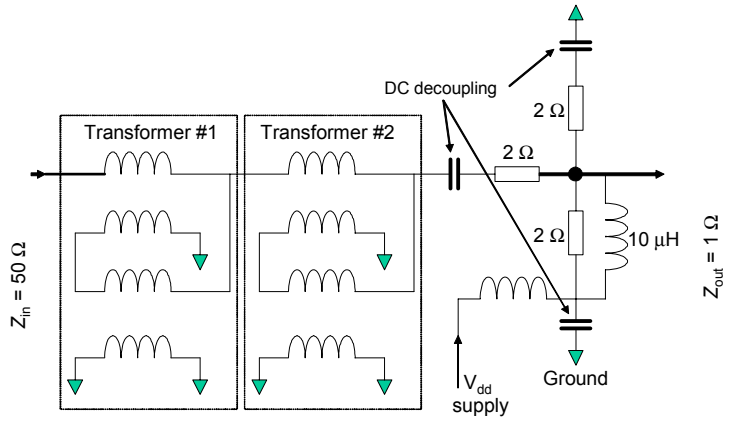


Figure 5 – Circuit diagram of the coupling network for supply/ V_{dd} pin(s) of an IC

The coupling network incorporating the TL transformer and the 1 Ω resistor network is the same as in the ground pin(s) coupling network, but only one DC decoupling capacitor is added between the transformer and the resistor network. This capacitor will pass the impulse to the supply/ V_{dd} circuit; however it decouples the DC voltages to pass towards the transformers (which might cause saturation of the core material used). The decoupling capacitors play a very important roll to have the RF return path for the impulse.

The RF choke provides the necessary DC by-pass for the high supply/ V_{dd} current. An RF lossy inductor and the high pass capacitor will ensure that the impulse does not influence the rest of the supply system. The overall attenuation in the coupling network is again 22 dB approximately, 6 dB attenuation by each transformer and 10 dB by the resistive network. The transfer characteristic of the coupling network needs to be flat (–3 dB) over a frequency range of 1 MHz to 1 GHz.

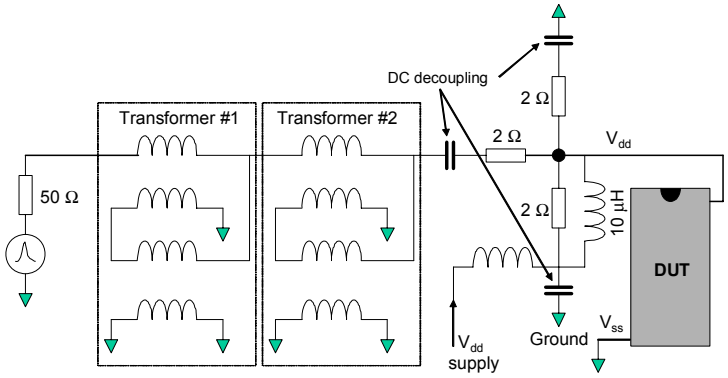


Figure 6 – Method to impose synchronous transient injection into supply/ V_{dd} pin(s)

Figure 6 gives a schematic diagram on the method to insert an impulse into the supply/ V_{dd} pin(s) of the IC. When an impulse is applied to the coupling network, it will be superimposed in series with the supply voltage and this total voltage is applied to a supply pin of the digital/ mixed-signal IC. The coupling network is designed in such a way that the impulse energy will be inserted into the supply/ V_{dd} pin of IC and will not be reflected back to the main power supply.

Since the coupling network has approximately 22 dB attenuation, to get a 4 V to 5 V impulse amplitude across a 1 Ω resistor, the amplitude of the input impulse should be in the range of 48 V to 60 V. It is necessary that the transformers should not saturate under these conditions.

4.5.5 Coupling network for the I/O pin(s)

For coupling synchronous impulses to single I/O pins, three items shall be considered:

- the need for transparency for the functional signal (including loading);
- the broad variety of impedances represented by the I/O circuitry;
- directivity of the fast impulses applied.

As the coupling network will always introduce additional delay, this delay shall be considered when used with multi-wire busses, as the disturbance can only be applied to a single port at the time.

NOTE Considering the set-up of the I/O pin coupling network, it can also be extended to more than just one I/O, e.g. for balanced lines.

For this purpose, an RF "fork" network is defined with suitable bandwidth, see Figure 7.

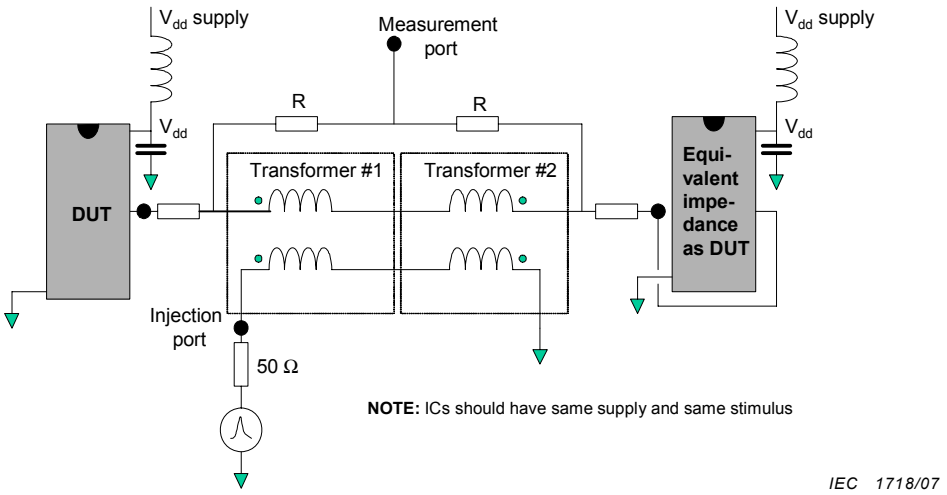


Figure 7 – Method to impose synchronous transient injection into I/O pins

The injection port shall be connected to the synchronous transient generator, typically with a 50 Ω output impedance. The secondary ports of the transformers shall be loaded by a resistance R; 25 Ω each (assuming 1:1 transformer ratios) to satisfy the RF loading for the synchronous transient generator. At the port on the right, an RF impedance equivalent to the IC's I/O pin impedance at the port on the left shall be applied to balance the RF load on the fork. When the loading is balanced, the induced impulse signal is cancelled towards the measurement port and the impulse occurs at the left and right port equally. At the measurement port, either the functional signal to the IC's input is applied or an oscilloscope or time domain analyser measures the IC's output signal; so called measurement equipment in the figures.

4.5.6 Coupling network for the reference pins

For coupling onto e.g. reset and oscillator pins, a 1 Ω coupling network as defined for the ground/ V_{ss} pins shall be applied in series with the components that are referred to ground/ V_{ss}. With a reset pin, the time-constant determining capacitor or pull-down resistor shall be disconnected from ground/ V_{ss} and re-connected through the 1 Ω coupling network. With oscillator pins, e.g. with a Pierce oscillator, the two capacitors (typically used off-chip) shall be disconnected from PCB ground/ V_{ss} and re-connected through the 1 Ω coupling network.

4.5.7 Coupling network verification

The attenuation versus frequency of the coupling networks shall be verified using a voltage network analyser (VNA). To verify the frequency dependent transfer characteristics, two equal coupling networks shall be connected to each other on the 1 Ω side. While assuming than S_{12} = S_{21}, the total attenuation in a 50 Ω impedance domain shall be 44 dB ± 6 dB in the frequency range 1 MHz to 1 GHz. The attenuation versus frequency shall be 44 dB ± 2 dB in the frequency range 3 MHz to 300 MHz.

4.6 Test circuit board

4.6.1 General

While the test PCB to be used may depend on the specific ICs to be tested, a general recommendation for a test board is given in Annex C. It is recommended to follow this layout, unless a specific test board is needed, either for the test set-up, or for other specific reasons. In any case the test PCB configuration is unambiguously described in the specific sub-parts of this specification, for the individual test methods. Any deviation from this description shall be stated in the individual test report, unless a specific test board is defined in the specific measurement standard. All test boards used shall follow good layout practice including an adequate ground plane and impedance structures.

4.6.2 IC pin loading / termination

The pins of the DUT shall be loaded/ terminated according to the default values listed in Table 1, with exceptions, as functionally required, and as stated by the manufacturer. Table 1 shows examples for pin loading for different pin types. The chosen pin loading shall be described in the test report.

Table 1 – IC pin loading recommendations

IC pin type	Pin loading
Analogue	
- Supply	As stated by the manufacturer (or as required)
- Input	10 kΩ to ground/ V_{ss} unless the IC is internally terminated
- Output signal	10 kΩ to ground/ V_{ss} unless the IC is internally terminated
- Output power	Nominal loading as stated by the manufacturer
Digital	
- Supply	As stated by the manufacturer
- Input	Ground/ V_{ss} or 10 kΩ to supply/ V_{dd} if cannot be grounded, unless the IC is internally terminated
- Output	47 pF to ground/ V_{ss}
Control	
- Input	Ground/ V_{ss} or 10 kΩ to supply/ V_{dd} if cannot be grounded, unless the IC is internally terminated
- Output	As stated by the manufacturer
- Bi-directional	47 pF to ground/ V_{ss}
- Analogue	As stated by the manufacturer

Pins that do not fall into any of the listed categories shall be loaded as functionally required and stated in the test report. These are recommended default values; if other values are more appropriate for a particular IC, they may be substituted for the values in Table 1 and shall be stated in the test report.

4.6.3 Power supply requirements

The DUT shall be powered from a DC supply source that is not affected by the applied synchronous transient test signal. If a battery is used, it shall meet the IC requirements and the supply voltage level shall be checked to maintain a consistent operating environment. All power supply lines to the DUT shall be adequately filtered according to the IC manufacturer's recommendation.

4.7 IC specific considerations

4.7.1 IC supply voltage

The supply voltage(s) shall be as specified by the IC manufacturer with a tolerance of ± 5 %.

4.7.2 IC decoupling

The value and layout position of power supply decoupling capacitors shall be stated in the individual test report. The decoupling of each supply pin of the DUT may be as advised by the manufacturer. These shall be provided behind the coupling networks.

4.7.3 Activity of IC

Attempts should be made to fully exercise all available functions and modes of operation that significantly influence the immunity of the IC.

To improve the test speed, the IC may be programmed with sequential small programs to allow the injection of the synchronous transient disturbance signal to the IC while obtaining the responses.

When a relation between the activity of the IC and the test signal exist, it shall be documented in the test report.

4.7.4 Guidelines for IC stimulation

The intention is to describe the parameters to be controlled in order to ensure test repeatability for the particular IC function or type, as agreed to between the manufacturer and user.

If a programmable integrated circuit is to be tested, software that flows in a continuous loop shall be written to ensure that measurements are repeatable. The type of software used to exercise the IC (minimum, typical or worst case) shall be documented with the test report.

4.7.5 IC monitoring

All relevant activity states shall be monitored without unintentional feedback to the immunity performance.

4.7.6 IC stability over time

The functional behaviour of the IC shall be stable over time such that two measurements, separated by an interval of time, shall yield the same results within the expected variation of the measurement technique.

5 Test conditions

5.1 Default test conditions

5.1.1 General

Default test conditions are intended to ensure a consistent test environment. If the users of this procedure agree to other values, these values shall be documented in the test report.

5.1.2 Ambient conditions

Unless otherwise specified in the manufacturer's specifications, the ambient conditions as given in the future IEC 62215-1 shall apply. The RF ambient level shall be sufficiently low that the DUT responses are not inversely affected. For the sake of repeatability of the test, it is recommended not to have wireless telephones in close proximity (≤ 1 m) to the test set-up.

5.1.3 Ambient temperature

The ambient temperature during the test shall be 23 °C ± 5 °C for repeatability.

NOTE The impulse immunity of ICs may vary with temperature.

5.2 Impulse immunity of the test set-up

When carrying out the test, all equipment used in the test set-up, excluding the DUT, shall be sufficiently immune itself such that it will not influence the test results.

6 Test set-up

6.1 General

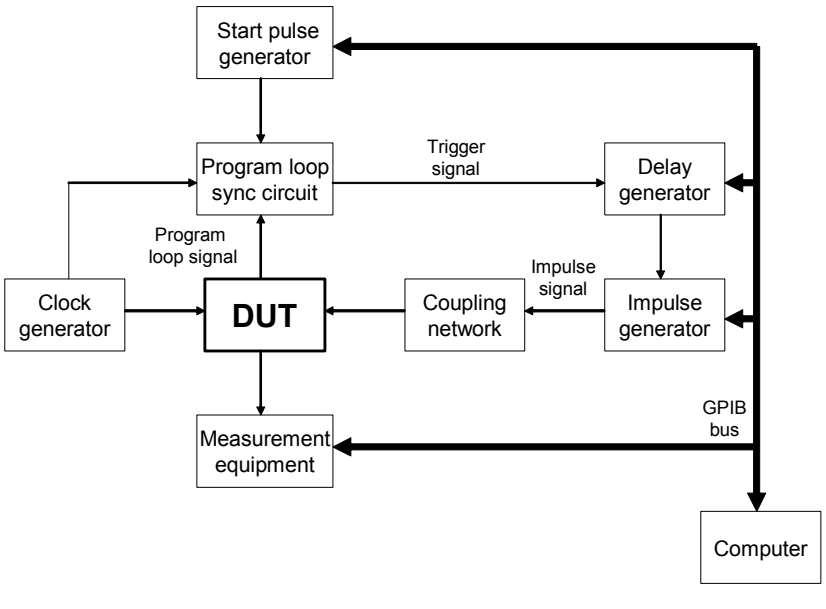


Figure 8 – Measurement set-up for synchronous transient injection

For an explanation of the test set-up, an intelligent digital device such as a microcontroller is considered as an example. Detailed information is given in 6.3.

The same set-up can be modified for non-intelligent digital devices such as logic ICs, state machines, etc.

The aim of this test is to inject an impulse into the ground/ V_{ss}, V_{dd} and I/O pin(s) of the ICs where the responses are noted. The important point is that these impulses should be synchronized with the S/W program running inside the IC.

6.2 Test equipment

The equipment used in Figure 8 consists of the following components:

- a stable clock signal source;
- measurement equipment, e.g. a modulation domain analyser or oscilloscope to measure jitter in the response signal;
- test PCB containing the device under test (DUT);
- picoseconds-precise impulse generator;
- delay pulse generator which can be stepped in picoseconds step size;
- program loop sync circuitry; mostly application specific;
- pulse generator to produce a reference pulse with low jitter;
- set-up controller, i.e. computer for controlling and data acquisition.

6.3 Set-up explanation

Figure 8 shows the details of the impulse immunity test set-up. The test PCB with a microcontroller (DUT) is considered as a test vehicle for the impulse immunity. A small set of instructions is loaded into the microcontroller, which will generate a square waveform generally referred to as a program loop signal. A stable clock signal source is used to generate the clock signal for the microcontroller. A pulse generator is used to generate a reference enable, i.e. an enable/start pulse signal. This pulse has an important role in starting the experiment.

The program loop sync circuitry is one of the key elements in the measurement set-up. This is typically a D-type octal latch with three input signals, e.g. the clock signal, program loop signal and the reference enable/start pulse signal. These three signals, under certain conditions, will produce a trigger pulse. This trigger pulse is used to trigger the delay pulse generator.

The delay pulse generator has the flexibility to produce a delay pulse with variable delay, starting from picoseconds to seconds (typically up to the program loop period). This delay pulse is used to trigger the impulse generator. The impulse generator can generate an impulse having short-time duration with fast rise/fall times and also high-voltage amplitude.

A test PCB with minimum hardware configuration is required for the microcontroller operation. The coupling circuits are also built on the same test PCB. The response signal is fed to the modulation domain analyser or oscilloscope to analyse the jitter in the program loop. A trigger signal/ command from the computer is used to trigger the modulation domain analyser.

All equipment is typically controlled from a GPIB bus with a program running in the computer. The computer program is also used to acquire the response data from the modulation domain analyser or oscilloscope to the computer. This program also ensures that all measurements go smoothly without any interruption. While conducting these experiments, it is possible that equipment may miss a trigger pulse and the total experiment may then halt/fail. In such conditions, commands in the measurement program will take care to fix the error, reset the set-up and/or device and redo the experiment from “failure” point onwards.

In the synchronous transient immunity test method, several parameters can be considered as variables which would affect the response for the impulse disturbance, e.g. impulse duration, impulse amplitude, impulse polarity, the IC pins to which the impulses are applied, software running in microcontroller, etc.

6.4 Explanation of signal relations

Figure 9 (not in scale) shows the waveforms appearing in the test set-up. The first waveform is a clock signal, the second one is the response signal and the third one is a reference enable/start pulse signal generated by the pulse generator. The start signal may hold for several program loop periods in order to acquire the date from the measurement system.

These three signals are feed to the program loop sync circuitry. When the rising edge of the program loop is available and the clock signal and the enable pulse signal goes high state, the latch produces a signal being the trigger pulse (not shown). This pulse is used to trigger the delay pulse generator. Finally, a delayed pulse with adjustable delay is generated. The last signal is an impulse, generated by the impulse generator.

All equipment used in this experiment have their own delays, and these delays are calculated with reference to the rising edge of the response signal. However, any logic circuit and/or equipment may produce small delays between the response signal and the impulse signal. The total equipment delay should be calculated and should be compensated for in the delay pulse generator to ensure that an entire program loop is interrogated with impulses.

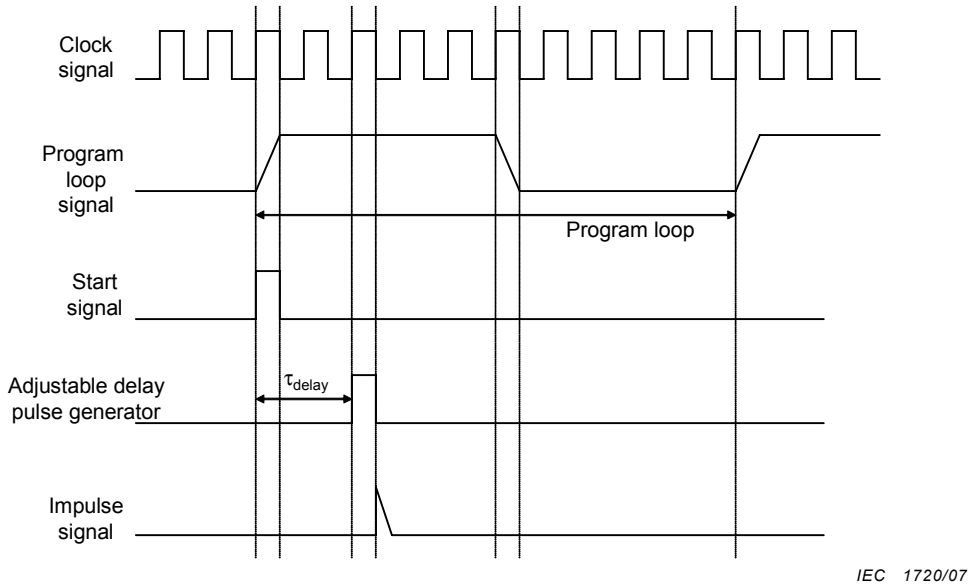


Figure 9 – The waveforms (not in scale) appearing in the test set-up

6.5 Calculation of time step and number of measurements to be conducted

As an example, a program loaded in the microcontroller produced a 48 kHz square waveform (response signal); one cycle of this response signal (48 kHz) is then considered as a program loop signal. The time taken to produce the program loop is 20,833 µs. The aim of this immunity test is to inject an impulse at different positions on the time axis of a program loop, which is called scanning. For scanning purposes a delay pulse is used that will shift the injection point of an impulse on the time axis of the program loop. Typically, 1 ns time steps are used to scan the program loop. This means that with a time step of 1 n,s one has to carry out the same test 20 833 times in order to find the impulse immunity of a given program loop with specific instructions.

The control program is written in such a way that it conducts the experiment according to the procedure explained in 4.3; the computer then stores the response data and the delay is incremented by a step of 1 ns, and the measurements are repeated until a complete program loop is scanned. It is observed that the total time taken by the test set-up to scan a complete program loop is very time-consuming. All responses data from the measurements are stored in a data file and then plotted. From this information one can find the most susceptible time windows in the program loop.

6.6 Test procedure

The following test procedure shall be followed:

a) Connect all the equipment as shown in Figure 8.

b) Set the pulse generator to produced a reference pulse, i.e. enable/start pulse signal, e.g. 200 ns and 3 V amplitude .

c) Set the delay pulse generator to produce a delay pulse as per the specified delay.

d) Set the clock signal e.g. to 12 MHz, to generate the microcontroller, i.e. device's reference clock signal.

e) Connect test signal, clock signal and enable pulse signal to the program loop sync circuitry.

f) Set the impulse generator to produce an impulse, e.g. 1 ns rise time, 8 ns duration and 1 V amplitude (at the output of the coupling network).

g) Set the domain modulation analyser to measure peak-peak jitter value of the response signal.

h) Connect all equipment to the computer through the PC control bus.

When a 12 MHz clock is fed to the microcontroller, it produces a square waveform (toggling response signal). This response signal is fed to the modulation domain analyser and the program loop sync circuit. The control program will send a command to the pulse generator to produce a reference enable/start pulse signal that will appear in the program loop sync circuitry. The necessary condition for obtaining a trigger pulse from the program loop sync circuitry is that the response signal is in the transition state from logic zero to one, and the clock and enable pulse signal should be in the high state. The trigger pulse from the program loop sync circuitry feeds the delay pulse generator. A constant delay step is set in the delay pulse generator. This constant delay step gives fixed references over the time axis in a program loop for the injection of an impulse. The delay pulse triggers the impulse generator that generates an impulse. This impulse is coupled to supply/ V_{dd}, ground/ V_{ss} or I/O pin(s) of the microcontroller. The computer also provides a signal to trigger the domain analyser. The domain analyser calculates the peak-peak jitter value of the response signal due to the impulse disturbance. All response data are sent and stored in the computer.

NOTE It is important to follow the main strategy and use the defined coupling circuits. However, the user can change the test set-up, s/w as required. The modification in the test measurement should be mentioned in the test report.

6.7 Monitoring check

Energize the DUT and complete an operational check to assure proper function of the device under test under normal activity and assure proper function of the failure detection.

6.8 System verification

The DUT can be checked on various responses. Response examples are as follows:

– Jitter;

– spikes and glitches;

– system reset;

– system hang-up;

– latch-up.

7 Test report

7.1 General

Tests shall take place according to a test plan, which shall be included in the test report. This report shall also include:

- a circuit diagram of the application (supply decoupling, peripheral ICs, etc.);
- a description of the PCB on which the IC is applied (layout);
- actual operating conditions of the IC (supply voltage, output signals etc.);
- a description of the type of software exercising the IC(s), if applicable;
- all variations shall be included in the test report. Connection to auxiliary equipment shall not influence the test results.

Other particular requirements are described in the individual test procedure.

7.2 Immunity limits or levels

As this technical specification describes an immunity measurement method, no immunity test levels, criteria or limits are given. Limits in general depend upon the application and functional requirements.

7.3 Performance classes

The following performance grades can be used to characterize IC performance when subjected to the immunity test signal specified by the particular immunity measurement procedure:

A. Normal performance within the specification limits.

B. Temporary degradation or loss of function or performance that is self-recoverable (e.g. when scanning further through the program loop period).

C. Temporary degradation or loss of function or performance, which requires operator intervention or system reset.

D. Degradation or loss of function which is not self-recoverable due to damage of IC(s), or loss of data.

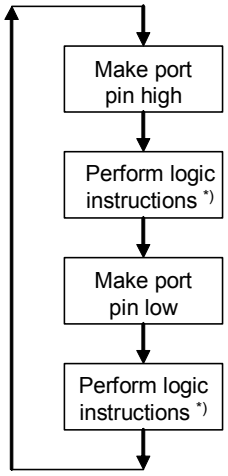
7.4 Interpretation and comparison of results

Results may be directly compared as long as measurements have been carried out under the same conditions. If comparison is intended, the devices shall run the same code and the test environment shall be as consistent as possible. The same kind of test boards shall be used.

Annex A
(informative)

Flow chart of the software used in a microcontroller

This simple routine implements a square waveform (response signal) at given output port/pin of a microcontroller. The port pin is toggled to high logic, then a delay is added, the same port pin is toggled to the logic zero and the same delay occurs. The instructions put into the program loop should have a continuous program delay.



IEC 1721/07

Figure A.1 – Test code flow chart

Annex B
(informative)

Flow chart for the set-up control S/W (bus control program)

The flow chart in Figure B.1 illustrates the equipment control and data acquisition flow. This flow chart may apply for the test set-up as defined in 6.1.

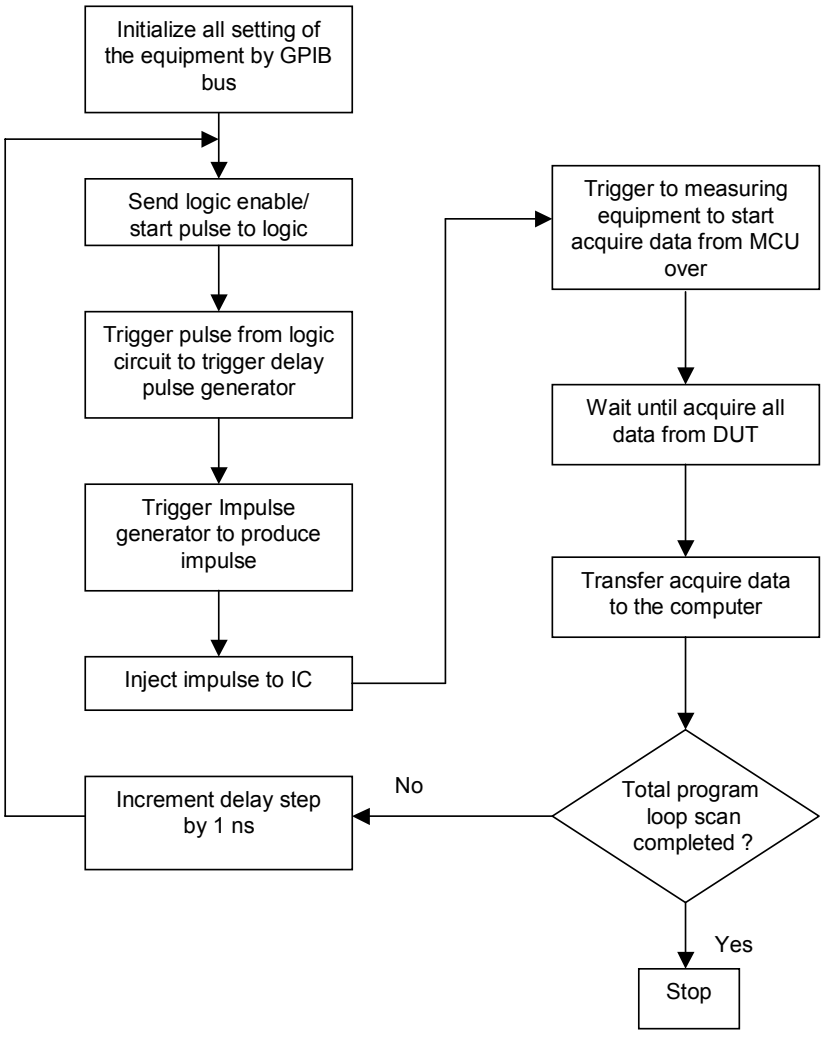


Figure B.1 – Test measurement flow chart

Annex C
(informative)

Test board requirements

C.1 Board description – mechanical

The typical board size is 100 $^{+3}_{-1}$ mm^2 (such that it can be used with other tests). Holes may be added at the corners of the board, as shown in Figure C.1. All edges of the board at least shall be tinned for 5 mm, or made conductive in order to make proper contact. As an alternative, edges may be gold-plated.

The vias at the outer edge of the board shall be at least 5 mm away from that edge.

C.2 Board description – Electrical

C.2.1 General

The test PCB drawing in Figure C.1 shall be taken as a guide. A double layer board is proposed as a minimum requirement. However, if functionally needed, layers 2 and 3, or others, may be added inbetween such that a multilayer board appears.

Layer 1 shall always be used as the ground plane. Layer 4 allows other signals but shall be left as much intact as possible, so as to be a ground plane as well. As a minimum, the area in layer 1, underneath the IC, shall be left as a ground plane to which the characteristic impedances need to be defined.

The PCB shall be made such that only the IC package remains on one side (layer 1) and all other components and trace patterns remain on the opposite layer (layer 4 (2)).

C.2.2 Ground planes

The ground planes (layers 1 and 4) shall be interconnected by means of vias. These vias shall be placed at the following positions over the board as described in Table C.1:

Table C.1 – Position of vias over the board

Via position	Location
1	All around, at the edges of the board
2	Just outside the DUT area
3	Just inside, underneath the IC area

The ground plane at layer 1 shall be continued between vias at position 2. As such, the ground plane at layer 1 is continued over the whole board.

If possible the same shall be done for layer 4, but the possibility to do so depends on the IC package and the space available.

C.2.3 Pins

C.2.3.1 General

All functionally necessary components, other than the IC, shall be mounted on layer 4. It is therefore necessary to feed I/O and other required pins from layer 1 to layer 4. The loop areas, trace length, via placement and component orientation shall be optimised such that minimum loop areas are obtained.

C.2.3.2 DIL packages

These packages do not require vias, as plated through-hole pins are considered present or established by the pins themselves.

C.2.3.3 SOP, PLCC, QFP packages

These packages require the use of vias. The vias should preferably be centred in the pads used for soldering the ICs. Preferably, these vias should be placed at position 3 in Table C.1 to minimize the loop area involved in which the IC currents will flow.

C.2.3.4 PGA, BGA packages

Under consideration.

C.2.4 Vias

C.2.4.1 Via type

All vias at position1 shall have a hole diameter of 0,8 mm. All other vias shall have a diameter ≥ 0,2 mm.

C.2.4.2 Via distance

A maximum lateral distance between vias is required for measurements up to 1 GHz.

- Vias connecting layer 1 with layer 4 shall have a maximum distance of 10 mm between them.
- Vias accompanying signal traces shall be as close as possible to those vias connecting layers 1 - 4, to create small return signal loops.

C.2.5 Additional components

All additional components shall be mounted at layer 4. They shall be placed in such a way that they do not interfere with the constraints as set for layers 1 and 4 and vias in-between.

C.2.6 Supply decoupling

To obtain reproducible data of measurement, adequate supply decoupling is required in accordance with the test board specifications. Decoupling capacitors on the test board shall be classified into two groups as described below. The values and layout positions of the decoupling capacitors and other decoupling components shall be stated in the individual test report.

- IC decoupling capacitors

  Supply decoupling for the IC shall be in accordance with the manufacturer's recommendations. IC decoupling capacitors, if any, shall be connected to the ground plane in layer 4, underneath the IC, in order to maintain the proper operation of the DUT. The value and layout position of a decoupling capacitor of each supply pin of the DUT may be as advised by the manufacturer, or otherwise, as long as stated in the test report.

- Power supply decoupling for the test board

Impedance of the test board power supply and impulse signal path may affect the measurement results if these are not adequately designed. To control the supply impedance of the test board from any external power supply that may be used in the measurement, a group of decoupling capacitors shall be located on the test board. Their values and layout positions shall be as described in the individual measurement standards, or otherwise, as long as stated in the test report.

C.2.7 I/O load

Additional components necessary to load or activate the IC shall be mounted on layer 4, preferably directly underneath the IC package area.

Dimensions in millimetres

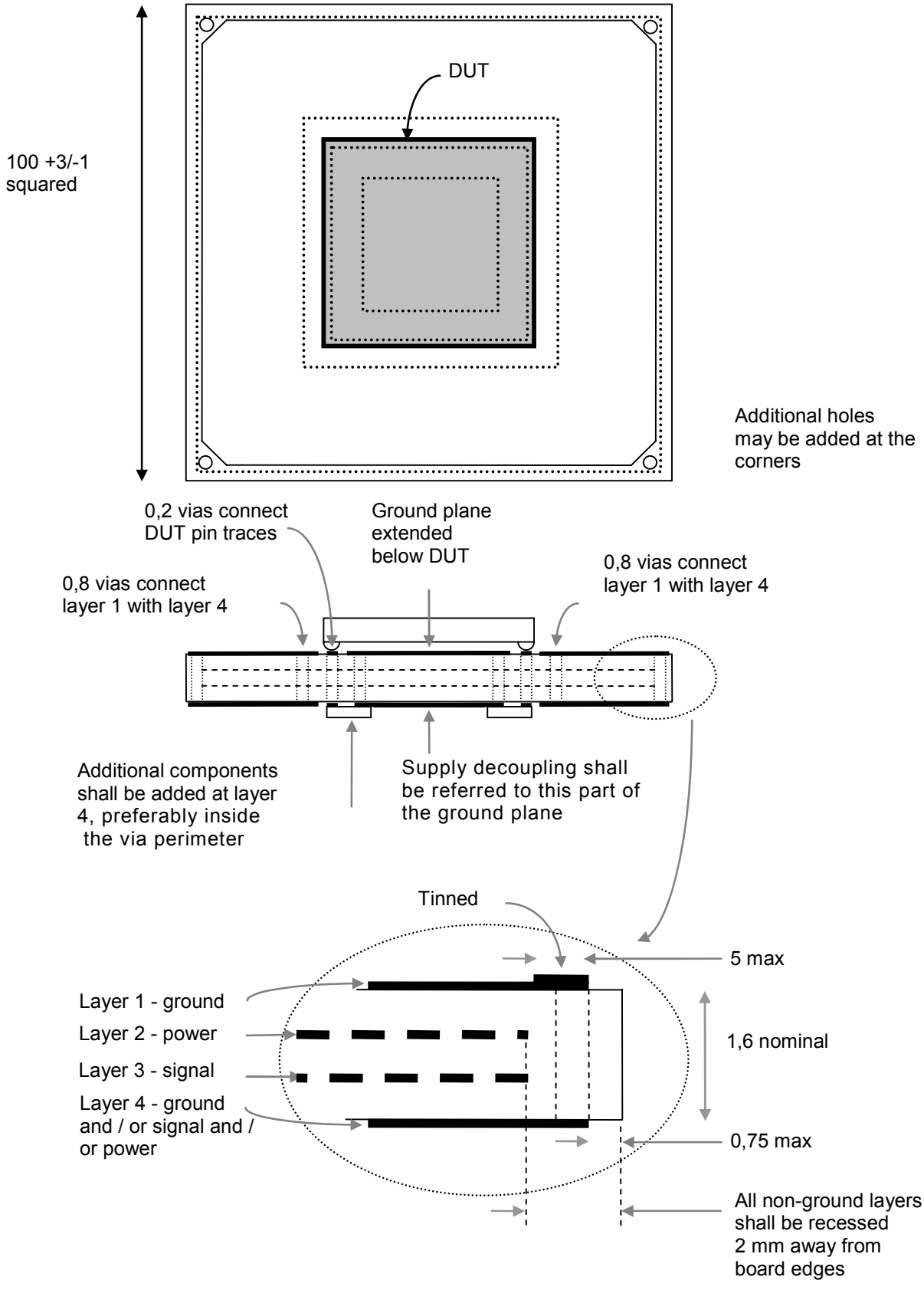


Figure C.1 – Typical test board topology

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