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Field-induced charged-device model test method for electrostatic discharge withstand thresholds of microelectronic components

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Test Method C101

Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components

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FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS

FOREWORD

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The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document:

Draft PAS	Report on voting
47/1462/PAS	47/1495/RVD

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TEST METHOD C101

FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS

1. PURPOSE

This standard describes a uniform method for establishing charged-device model (CDM) electrostatic discharge (ESD) withstand thresholds.

2. SCOPE

All packaged semiconductor components, thin film circuits, surface acoustic wave (SAW) components, opto-electronic components, hybrid integrated circuits (HICS), and multi-chip modules (MCMs) containing any of these components are to be evaluated according to this standard. The test methods described in this standard may also be used to evaluate components that are shipped as wafers or bare chips. To perform the tests, the components must be assembled into a package similar to that expected in the final application. The package used shall be recorded.

3. REFERENCE DOCUMENT

JEDEC Standard No. 42, "Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices."

4. TERMS AND DEFINITIONS

Charged device model (CDM) – A specified circuit characterizing an ESD that occurs where a device acquires charge through some tribe-electric (frictional) processes and then abruptly touches a grounded object or surface.

Electrostatic discharge (ESD) – A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.

Field-induced charging – A charging method using electrostatic induction.

5. CIRCUIT SCHEMATIC FOR THE CDM SIMULATOR

5.1 The waveforms produced by the simulator shall meet the specifications of 6.1 through 9.

5.2 A schematic for the CDM test circuit is shown in figure 1. (Other equivalent circuits are allowed if the generated waveform meets the requirements of 6.1 through 9.) A detachable discharge head (see figure 1), consisting of the pogo probe, radial resistor, top ground plane, semi-rigid coaxial cable, and the support arm, is used to initiate the discharge. The discharge path includes a 1 Ω resistive current probe of at least 4 GHz bandwidth for waveform monitoring. The cable from the 1 Ω resistor to the oscilloscope should also have a bandwidth of at least 3 GHz.

5.3 The Field-Induced Method shall be used to raise the component potential for a subsequent CDM discharge. The component potential is raised by applying the test voltage to the field charging electrode shown in figure 1. The size of the charging electrode shall be larger than the size of the component and the waveform generated shall meet the requirements in table 3.

6. SIMULATOR WAVEFORM VERIFICATION

6.1 The three levels of CDM simulator verification tests are:

- Manufacturer Qualification
- . User Verification
- Routine Verification

The tests are described in table 1:

TABLE 1 WAVEFORM VERIFICATION TESTS

	Routine Verification	Manufacturer Qualification and User Verification
Record of waveforms required	yes	yes
8.1 check	yes	yes
9. Tests	#1	#1, #2, #3

6.2 Manufacturer Qualification – must be done by the manufacturer when the simulator is installed. High-speed instrumentation must be used, including an oscilloscope with a 1 GHz single-shot bandwidth. All three qualification tests of section 9 are required, and the test waveforms must be permanently recorded with copies supplied to the user when requested.

6.3 User Verification – done during initial acceptance testing, whenever the equipment is serviced, and on a regular basis at least once per month. The same tests are done as in the manufacturer's qualification. Waveforms obtained by a 1 GHz oscilloscope must be recorded and stored for comparison with the manufacturer's waveforms and the weekly verification waveforms.

6.4 Routine Verification – done every week the simulator is used. Only test #1 in section 9 is required. The user shall observe the waveforms with the 1 GHz scope and compare them with the previously recorded waveforms.

6.5 If the waveforms do not meet the requirement of section 9, reject any data obtained after the last verification.

7. MEASUREMENT INSTRUMENTATION

7.1 Waveform verification requires the following instrumentation:

- Oscilloscope of at least 1 GHz bandwidth,
- Ohmmeter capable of measuring a resistance of $1.0 \pm 0.1\ \Omega$, and
- Standard test modules – One small and one large disk with the dimensions listed in table 2:

TABLE 2 TEST MODULES

Disk (inches)	Small	Large
Diameter	0.350±0.005	1.000±0.005
Thickness	0.050±0.002	0.050±0.002

7.2 The disks shall be made of brass plated with nickel or gold/nickel and may optionally have a gold flash coating over the nickel. They shall be manufactured to the dimensions specified in table 2 and shall be verified once before the initial use.

8. MEASUREMENT PROCEDURE

8.1 With the ohmmeter, verify that the resistance of the current sensing resistors in all discharge heads to be used is 1 ± 0.1 Ω.

8.2 With the use of the standard test modules in 7.1, perform three tests in section 9. For each test.

1. Raise the potential of the standard test module to the voltage indicated in table 3.
2. Discharge the standard test module at least five times at both positive and negative polarities. Note that with the Field-Induced CDM technique, both discharge polarities are obtained on alternate discharges with a single power supply setting. Therefore the power supply voltage may be set to either polarity. The peak currents should have the same magnitude but opposite sign for the two discharge polarities.
3. Record the waveforms using the oscilloscope and take the average values of the parameters specified in table 3.
4. Repeat the step 1 through step 3 for additional discharge heads as needed.
5. If the waveform characteristics do not meet the requirements in table 3, clean the test modules (see 13.5) and repeat step 1 through step 3.
6. If the waveform still can not meet the requirements in table 3, any data obtained since the last verification shall be invalidated and the simulator shall be serviced.

9. WAVEFORM CHARACTERISTICS

The waveforms shall appear as shown in figure 2 for the positive polarity and its reverse for the negative polarity. The average values specified in 8.2 shall meet the specifications in table 3:

TABLE 3 CDM WAVEFORM CHARACTERISTICS

		Test Number		
		#1	#2	#3
standard test module		Small	Small	Large
test voltage (V)		500	1000	200
peak current magnitude (A)	Ip	4.5 ±0.5	9 ± 1	3.5 ± 0.5
rise time (ps)	tr	<400	<400	
full width at half height (ns)	Td	1 .0±0.5	1.0±0.5	
undershoot (A, max.)	u-	<50% Ip	<50% Ip	
overshoot (A, max.)	u+	<25% Ip	<25% Ip	

10. VOLTAGE LEVELS

10.1 The recommended voltage levels for CDM ESD testing are:

100 V	1000 V
200 V	2000 V
500 V	

10.2 To determine the threshold more accurately, it is permitted to test at other voltage levels in addition to those specified above.

11. TEST PROCEDURE

11.1 The test shall be carried out at room temperature.

11.2 Testing may begin at any convenient voltage level from 10.1.

11.3 Obtain at least three samples which have been verified to meet their data specifications.

11.4 For each component, apply five positive and five negative discharges to each pin. (For Field-induced CDM simulators, a negative pulse automatically follows a positive pulse or vice versa.) Allow enough time (>200 ms) between discharges for the component to reach the full test voltage level. During the test, either watch the oscilloscope connected to the current monitoring resistor to verify that the discharges take place, or verify the scope trigger using software in computer-controlled systems. Apply the CDM stresses to all three components.

11.5 Test each of the components, using the failure criteria of section 12.

11.6 Components that pass the test may be reused at other voltage levels. Components that fail may not be used in tests at other levels. It is permitted to use new components for every voltage level. That is, step-stressing is not required.

11.7 The component code passes a voltage level if all three samples stressed at this level pass. The component code fails at the voltage level if one or more samples fail at this level.

11.8 The CDM WITHSTAND THRESHOLD of the COMPONENT CODE is the highest level for which three out of three stressed samples pass. If the component code does not pass any level, its threshold is O V. (Note: For the threshold level only, the rule for zero failures out of three samples is relaxed to allow one failure out of six samples or two failures out of twelve samples, etc. However, no sample failure shall occur at any test voltage level lower than the withstand threshold.) For example, if five out of six samples pass at 500 V and five out of six pass 1000 V, the assigned withstand threshold would be 500 V.

12. FAILURE CRITERIA

A component will be defined as a failure if, after exposure to ESD pulses and within 96 hours of ESD testing, it no longer meets the component drawing requirements. Parametric and functional testing shall be performed at room temperature and, if applicable, at high temperature.

13. SUPPLEMENTARY INFORMATION

13.1 Components used for CDM test shall not be used for any prior or future qualification tests.

13.2 All operators shall wear grounding straps when handling the components. The test components shall be handled with extreme care, using ESD preventive procedure outlined in JEDEC Standard 42.

13.3 Components should not be placed within 24 inches (610 mm) of the discharge head while the tester is operating to avoid potential damage from the radiated transient signal.

13.4 Components shall be transported in appropriate ESD-protective packaging. If the CDM withstand threshold is 200 V or less, shipping tubes or tape-and-reel packaging should not be used. Contact customers for information on special packing materials.

13.5 The standard test modules for the CDM simulator can be cleaned in an ultrasonic bath using isopropanol for about 20 seconds and dried in a moderate air stream to prevent charge leakage.

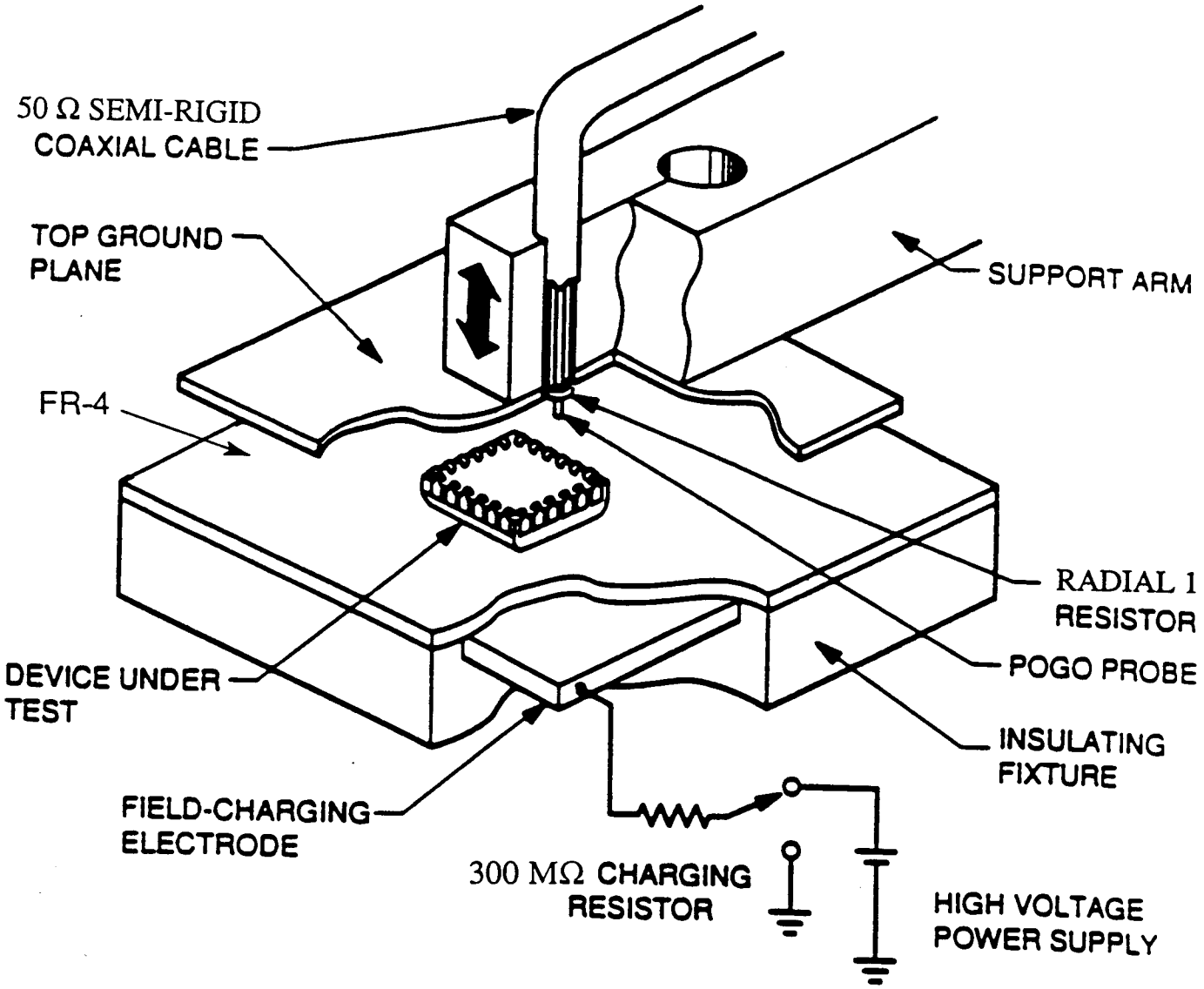

FIGURE 1: FIELD-INDUCED CDM SIMULATOR

FIG 1
ISSUE 1

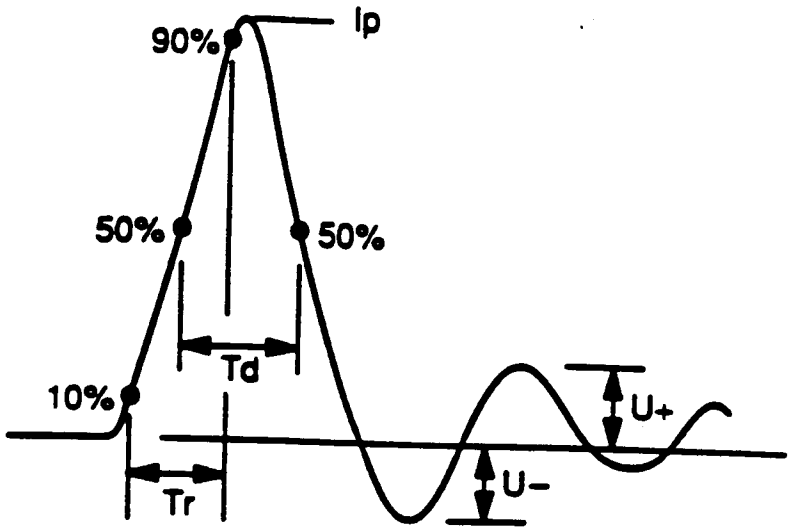

FIGURE 2: CDM CURRENT WAVEFORM

FIG 2
ISSUE 1

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