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INTERNATIONAL STANDARD

Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) – Part 2: Actuator sensor interface (AS-i)

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LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR – CONTROLLER-DEVICE INTERFACES (CDIs) –

Part 2: Actuator sensor interface (AS-i)

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International Standard IEC 62026-2 has been prepared by subcommittee 17B: Low-voltage switchgear and controlgear, of IEC technical committee 17: Switchgear and controlgear.

This second edition of IEC 62026-2 cancels and replaces the first edition published in 2000. This second edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below:

- doubling the number of slaves from 31 to 62 by introduction of sub-addresses;
- introduction of AS-I safety system.

The text of this standard is based on the third edition and the following documents:

FDIS	Report on voting
17B/1579/FDIS	17B/1584/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62026 series, under the general title *Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs)*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under “http://webstore.iec.ch” in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR – CONTROLLER-DEVICE INTERFACES (CDIs) –

Part 2: Actuator sensor interface (AS-i)

1 Scope and object

This part of IEC 62026 specifies a method for communication between a single control device and switching elements, and establishes a system for the interoperability of components with the specified communication interfaces. The complete system is called “Actuator Sensor interface (AS-i)”.

This standard describes a method for connecting switching elements, such as low-voltage switchgear and controlgear, standardized within IEC 60947, and controlling devices. The method may also be applied for connecting other devices and elements.

Where inputs and outputs I/O are described in this standard, their meaning is regarding the master, the meaning regarding the application is the opposite.

The object of this standard is to specify the following requirements for control circuit devices and switching elements:

– requirements for a transmission system and for interfaces between a slave, a master and electromechanical structures;

– requirements for a complete interoperability of different devices within any network, when meeting this standard;

– requirements for an interchangeability of devices within a network, when fulfilling the profiles of this standard;

– normal service conditions for the slaves, electromechanical devices and master;

– constructional and performance requirements;

– tests to verify conformance to requirements.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-6:1995, *Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-27:1987, *Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock*

IEC 60204-1:2005, *Safety of machinery – Electrical equipment of machines – Part 1: General requirements*

IEC 60227-2:1997, *Polyvinyl chloride insulated cables of rated voltages up to and including 450/750 V – Part 2: Test methods*
Amendment 1 (2003)

IEC 60228:2004, *Conductors of insulated cables*

IEC 60304:1982, *Standard colours for insulation for low-frequency cables and wires*

IEC 60352-6:1997, *Solderless connections – Part 6: Insulation piercing connections – General requirements, test methods and practical guidance*

IEC 60364-4-41:2005, *Low-voltage electrical installations – Part 4-41: Protection for safety – Protection against electric shock*

IEC 60529:1989, *Degrees of protection provided by enclosures (IP code)*
Amendment 1 (1999)

IEC 60947-1:2007, *Low-voltage switchgear and controlgear – Part 1: General rules*

IEC 60947-4-1:2000, *Low-voltage switchgear and controlgear – Part 4-1: Contactors and motor-starters – Electromechanical contactors and motor-starters*
Amendment 1 (2002)
Amendment 2 (2005)

IEC 60947-4-2:1999, *Low-voltage switchgear and controlgear – Part 4-2: Contactors and motor-starters – AC semiconductor motor controllers and starters*
Amendment 1 (2001)
Amendment 2 (2006)

IEC 60947-5-2:1997, *Low-voltage switchgear and controlgear – Part* 5-2: Control circuit devices and switching elements – Proximity switches
Amendment 1 (1999)
Amendment 2 (2003)

IEC 61000-4-2:1995 *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*
Amendment 1 (1998)
Amendment 2 (2000)

IEC 61000-4-3:2006, *Electromagnetic compatibility (EMC) – Part 4-3: Testing and measurement techniques – Radiated, radio-frequency, electromagnetic field immunity test*

IEC 61000-4-4:2004, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 61131-2:2007, *Programmable controllers – Part 2: Equipment requirements and tests*

IEC 61140:2001, *Protection against electric shock – Common aspects for installation and equipment*
Amendment 1 (2004)

IEC 61508 (all parts), *Functional safety of electrical/electronic/programmable electronic safety-related systems*

IEC 61800-2:1998, *Adjustable speed electrical power drive systems – Part 2: General requirements – Rating specifications for low-voltage adjustable frequency a.c. power drive systems*

IEC/TS 61915:2003, *Low-voltage switchgear and controlgear – Principles for the development of device profiles for networked industrial devices*

IEC 62026-1:2007, *Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) – Part 1: General rules*

CISPR 11:2003, *Industrial, scientific and medical (ISM) radio-frequency equipment – Electromagnetic disturbance characteristics – Limits and methods of measurement*
Amendment 1 (2004)
Amendment 2 (2006)

3 Terms, definitions, symbols and abbreviations

For the purposes of this document, the terms, definitions, symbols and abbreviations given in IEC 62026-1 as well as the following apply.

3.1 Terms and definitions

Alphabetical index of definitions

Reference

3.1.1
active slave
slave connected to the AS-i line and capable to communicate properly

3.1.2
Actuator Sensor interface (AS-i)
set of interfaces and serial communication method for the connection of low-voltage switchgear and controlgear, and other simple field devices with a controller

3.1.3
address
numerical parameter out of the address space of the AS-i slaves which specifies a node of an AS-i network

NOTE Address 0 is reserved for slaves which have not had an address assigned.

3.1.4
address assignment
replacement of the existing address of the AS-i slave with a new address

3.1.5
Analogue Input Data Image (AIDI)
input data stored in the master, containing the latest actual copies of the received data from the inputs of all active slaves using combined transactions type 1 to 5

3.1.6
Analogue Output Data Image (AODI)
output data stored in the master to be transmitted cyclically to the active slaves with outputs using combined transactions types 1 to 5

3.1.7
AS-i cycle
set of up to 33 transactions

NOTE 1 A cycle may, in case of a detected communication failure, include one message retransmission.

NOTE 2 In the case of extended addressing mode, two cycles will be needed for data transfer of all slaves that are in extended addressing mode.

3.1.8
AS-i input
physical or logical slave port providing an input from the process

3.1.9
AS-i line
two-wire line for transferring information and power to the AS-i slaves and the AS-i master

3.1.10
AS-i master
unit on the AS-i line that manages the communication between the slaves and the controller

3.1.11
AS-i network
network composed of an AS-i control circuit, interfaces and switching elements, for example master, slaves, power supply, cable, taps, repeaters

3.1.12
AS-i output
physical or logical slave port providing an output to the process

3.1.13
AS-i power supply
special power supply combining a d.c. supply and a symmetrizing and decoupling circuit needed in an AS-i network

3.1.14
AS-i slave
physical and logical means to connect the application devices (actuator, sensor, or other components) to the AS-i line

NOTE A slave may be a stand alone device or part of another device.

3.1.15
bit time
T_{Bit}
duration of the transmission of one bit

3.1.16
configuration data (CD)
value of the I/O configuration and the identification code (optional extended identification codes) of a specific slave

3.1.17
configuration data image (CDI)
image of the configuration data of all slaves, stored in the AS-i master

3.1.18
controller
host or operator of the master, for example a programmable logic controller, a personal computer, a gateway, or a human operator

3.1.19
controller interface
logical interface between the master and the controller

3.1.20
data exchange phase
period of time during which the master sends output data to the slaves and receives input data from the slaves

3.1.21
decoupling circuit
part of the AS-i power supply for decoupling the d.c. source and the physical data transmission within the AS-i network

3.1.22
detection phase
period of time when the execution control of the master tries to find all slaves connected and operating

NOTE All slaves found are listed in the list of detected slaves (LDS).

3.1.23
earth-fault detector
special insulation monitoring device compatible with the requirements of the AS-i transmission system which allows to detect the asymmetrical deterioration of the insulation between the AS-i network and ground

3.1.24
execution control
master function that controls the message exchange and provides several functions to the controller interface

3.1.25
extended addressing mode
doubles the maximum number of slaves from 31 (addresses in the range of 1 to 31) to 62 (addresses in the range of 1A/1B to 31A/31B)

3.1.26
field devices
items connected to the AS-i slave, for example actuators, sensors, push-buttons, indicator lights, etc.

NOTE "intelligent" field devices also include integrated AS-i circuitry.

3.1.27
I/O-configuration (I/O-code)
set of four bits which defines the direction of data flow at the slave I/O ports.

3.1.28
identification code (ID-code)
set of four bits which defines the type of slave for a given I/O-configuration (optional: extended ID-codes consisting of additional 2x4bits)

3.1.29
input data image (IDI)
input data stored in the master, received from the slaves

3.1.30
list of active slaves (LAS)
list of all slaves at the AS-i line that are activated and capable of communicating properly with the master

NOTE The list is available in the master.

3.1.31
list of detected slaves (LDS)
list of all slaves actually detected by the master

NOTE The list is available in the master.

3.1.32
list of peripheral faults (LPF)
list of all slaves with peripheral fault bit set to “1”

NOTE The list is available in the master.

3.1.33
list of projected slaves (LPS)
list of all configured slaves of the interface system as the target configuration

NOTE The list is available in the master and it includes the configuration data (CD) of all configured slaves.

3.1.34
master
control unit on the AS-i line that communicates serially with the slaves

3.1.35
master pause
time between the last bit of a master request and the first bit of the slave response, measured at the master ports

3.1.36
master request
data or parameter or function sent from the master to a single slave (exception: broadcast)

NOTE The content of this master request is either data (to be moved to the output ports of the slave), parameters or a command

3.1.37
non-volatile stored data
data that remains unchanged after power interruption

3.1.38
operation address
address of the AS-i slave other than the zero address

3.1.39
output current limit
I_{Lim}
output current of the power supply not to be exceeded under all environmental and load conditions

3.1.40
output data image
ODI
output data stored in the master to be transferred to the AS-i slaves

3.1.41
parameter image
PI
parameters (sets of 4 bits) that define the functionality of all the different slaves in the AS-i network

3.1.42
p-fault
appliance in a slave for signalling peripheral faults to the master

NOTE In case of a peripheral fault and a "Read_Status_Request" of the master the slave response will be "1" in S1 bit.

3.1.43
repeater
device that regenerates the AS-i signal and provides galvanic separation between parts of the AS-i network so that network lengths of more than 100 m are possible

3.1.44
select bit
bit in the master request used in extended address mode to distinguish between the A-slave and B-slave

3.1.45
send pause
period after receipt of the slave response during which no subsequent transmission occurs

3.1.46
slave
network device or part of another device that provides an interface to the AS-i line and communicates with the master

3.1.47
slave pause
time between the last bit of a slave response and the start of sending the first bit of the next master request, measured at the master ports

3.1.48
slave response
message from the slave to the master after a master request has been received and processed without error

NOTE The content of this response is either data or the result of a command.

3.1.49
symmetrizing circuit
part of the AS-i power supply for conditioning the physical data transmission within the AS-i network

3.1.50
transaction
(single) comprises a master request and a slave response within the master pause

NOTE Distinction is made between a single transaction, as defined above, and combined transactions of various types. The latter are combined of a series of several single transactions in which the information content is related in a well-defined way.

3.1.51
transmission control
master function that controls the data transmission, transmission pauses and retransmissions in case of failures (e.g. transmission failures, missing response from the slave, invalid response received, etc.)

3.1.52
volatile stored data
data that may change following power interruption

3.1.53
zero address
special address reserved for the online assignment of a new address to an AS-i slave

3.2 Symbols and abbreviations

AIDI Analogue Input Data Image
AODI Analogue Output Data Image
APF AS-i power failure
APM Alternating pulse modulation
APO AS-i power ON
AS-i Actuator Sensor Interface
ASI+ positive potential of the AS-i network
ASI− negative potential of the AS-i network
CB control bit
CD configuration data
CDI configuration data image
EB end bit
IDI input data image
I_e rated current of AS-i power supply

I_{lim} current limit of AS-i power supply

LAS list of active slaves

LDS list of detected slaves

LPF list of slaves that signal peripheral fault condition

LPS list of projected slaves

MAN Manchester II code

ODI output data image

PB parity bit

PCD permanent configuration data

PI parameter image

PP permanent parameter

PSK phase shift keying

SEL Select Bit used for extended addressing

ST start bit

T_{Bit} bit time

TS transaction status

00_{Hex} hexadecimal representation of values, for exampel $1F_{Hex}$ = 31 , F_{Hex} = 15

00_{Bin} binary representation of values, for example 1100_{Bin} = 12 , 0110_{Bin} = 6

4 Classification

4.1 Overview

The Actuator Sensor Interface system will be applied mainly at the lowest level of a multi-level automation hierarchy. AS-i concentrates on the typical requirements for connecting binary elements with a controlling device. Thus, AS-i meets the requirements in machinery and plant construction, where real-time processing, cost effective design, installation, operating, maintenance, and service are essential.

AS-i can be used as an interface physically integrated into actuators, sensors, or other devices and elements themselves, opening an option for "intelligent" binary actuators, sensors, or other devices and elements. AS-i may, as well, be used in separate modules providing an interface for typically four conventional actuators, sensors or other devices and elements already available on the market.

To connect this variety of actuators, sensors, or other devices and elements with a controlling device, AS-i is embedded in a structure of two different units which present three interfaces as shown in Figure 1.

Logically, the AS-i system is a master-slave communication system composed of a single master and up to 31 (62 with extended addressing) slaves. The master sends data and parameters to a specific slave. The slave passes the data to the output ports or processes the requested procedure (e.g. Reset_Slave) and returns the input data or the result of the successful processed procedure to the master, respectively.

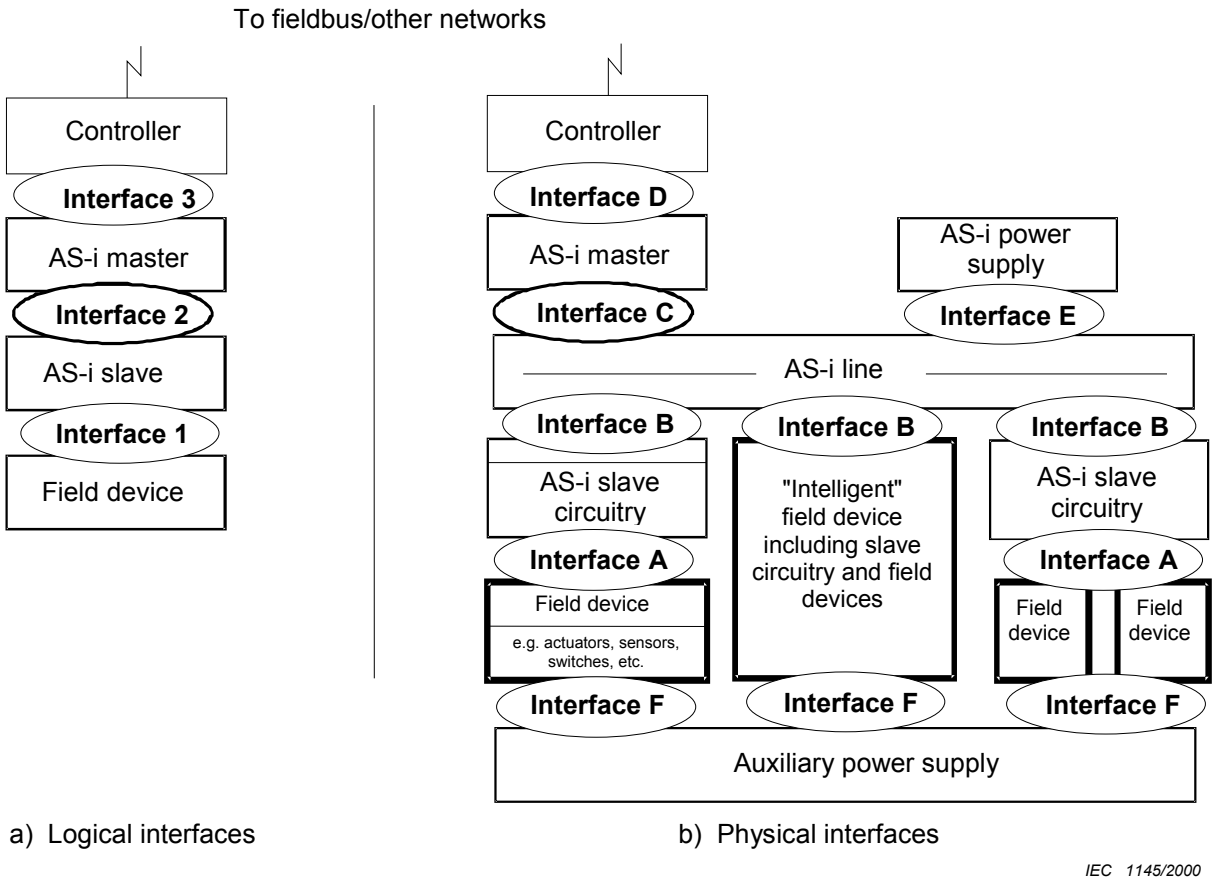


Figure 1 – AS-i components and interfaces

The AS-i concept is independent of the specific type of actuators, sensors, or other devices and elements. It defines the mechanisms and all the components for the communication with a controlling device and it offers electromechanical structures for a standardized "plug and play technique" for installing very simply actuators, sensors, or other devices and elements into an AS-i-network.

The annexes define slave and master profiles of common types of actuators, sensors, or other devices and elements, that will often be used in AS-i systems.

4.2 Components and interfaces

As shown in Figure 1, the AS-i system comprises the following components and interfaces.

4.2.1 Components

AS-i slave The unit that can be accessed by the master via the AS-i line for data exchange, parametrization, and monitoring. The slave has a well-defined logical and functional behaviour. It responds immediately with slave response to a specific request from the master and it ensures that a malfunction of the attached actuator, sensor or other device or of the slave itself will not disturb the communication between the master and the other slaves in the network.

NOTE 1 The definition of an AS-i slave is logical in nature, but covers the physical requirements for data transmission through the AS-i network, too. The concrete realization of a slave depends on the implementation; for example a specific pinout of an integrated slave chip is not defined in this standard.

AS-i master The unit that organizes and monitors the network and schedules the exchange of data, parameters and commands with the AS-i slaves via the AS-i line. The master has a well-defined logical and functional behaviour. It sends master requests to the AS-i slaves and receives the immediate slave responses from them.

NOTE 2 The definition of an AS-i master is mainly logical in nature but covers the physical requirements on data transmission through the AS-i network, too. The concrete realization of a master depends on its implementation. The 'Master Profiles' in Annex B define minimal sets of functions and commands of different master types.

AS-i power supply Provides power to the AS-i network and includes the decoupling circuitry.

AS-i repeater The unit that regenerates the AS-i signal and provides galvanic separation between parts of the AS-i network so that network lengths of more than 100 m are possible.

AS-i line Provides the signalling and d.c. power connections between the AS-i devices.

4.2.2 Logical interfaces

Interface 1 The slave interface to connect the AS-i slave with the actuators, sensors, or other devices and elements. It is characterized by several ports, which define the input, output or bi-directional input/output behaviour and the parametrization behaviour of the AS-i slave, the timing of the signals, and the power supply for actuators, sensors, or other devices and elements.

NOTE 1 Interface 1 is only a concept. The concrete representation of the interface depends mainly on the implementation. Only by the more restrictive slave profiles given in Annex A it is defined to some further extent.

Interface 2 The interface that provides all logical, physical, and mechanical requirements for data exchange and power distribution. It comprises signalling of encoded information, the AS-i transactions, mechanical and electrical requirements on the network and the AS-i power supply.

NOTE 2 Interface 2 is concrete in nature. It comprises the bus structure. The requirements of interface 2 are defined in this standard to ensure the interoperability of all components.

Interface 3 The interface between the controller and the AS-i master that provides all functions used by the controller to access the AS-i master for sending and receiving data to and from slaves, sending a cyclical command to a slave, to set or to obtain flags and values for several lists in the master. This interface allows the controller to manage the master's behaviour and thus the behaviour of the AS-i system. Supported functions are classically "set something" in the master, "get some information" from the master.

NOTE 3 Interface 3 is only a concept. The concrete representation of the interface depends on the implementation. To a large extent, it depends on features of the specific controller system.

4.2.3 Physical interfaces

Interface A Defines the physical connection between the field device and the AS-i slave circuitry including physical interface, signal levels and power requirements if any.

Interface B Defines the physical connection of the AS-i slave circuitry to the AS-i line including physical interface (mechanical/electrical), signal characteristics and power requirements.

Interface C Defines the physical connection of the AS-i master circuitry to the AS-i line including physical interface (mechanical/electrical), signal characteristics and power requirements.

Interface D Definition of the physical interface is outside of the scope of this standard and shall be provided by the manufacturer.

Interface E Defines the physical connection of the AS-i power supply including the signal decoupling circuit, to the AS-i line.

Interface F Defines the physical interface between the field device and an external auxiliary power supply if any.

5 Characteristics

5.1 Overview

The AS-i system defines digital, serial, multidrop data communication of a master with actuators and sensors or other devices including a power supply. Data and energy are transmitted on the same 2-wire cable.

The AS-i system is designed for protection class III (PELV) according to IEC 61140 (see 8.2). Therefore all components shall meet the corresponding requirements.

The AS-i transmission system provides the communication between up to 62 AS-i slaves and a single AS-i master, i.e. it represents the interface 2 between a master and the slaves (see Figure 1). The AS-i master shall call the individual slaves and get their responses immediately.

Subclauses 5.2 to 5.4 define the physical requirements and 5.5 to 5.7 the logical requirements of this transmission system (messages to be exchanged).

Additional requirements specific for the transmission medium (8.1), for the power supply (8.2), for the repeater and other components (8.3), for the slave (8.4) and for the master (8.5) are defined in the subclauses below.

5.2 Signal characteristics

The characteristics of the transmitted signal and the modulation are defined in this subclause.

5.2.1 Transmission coding

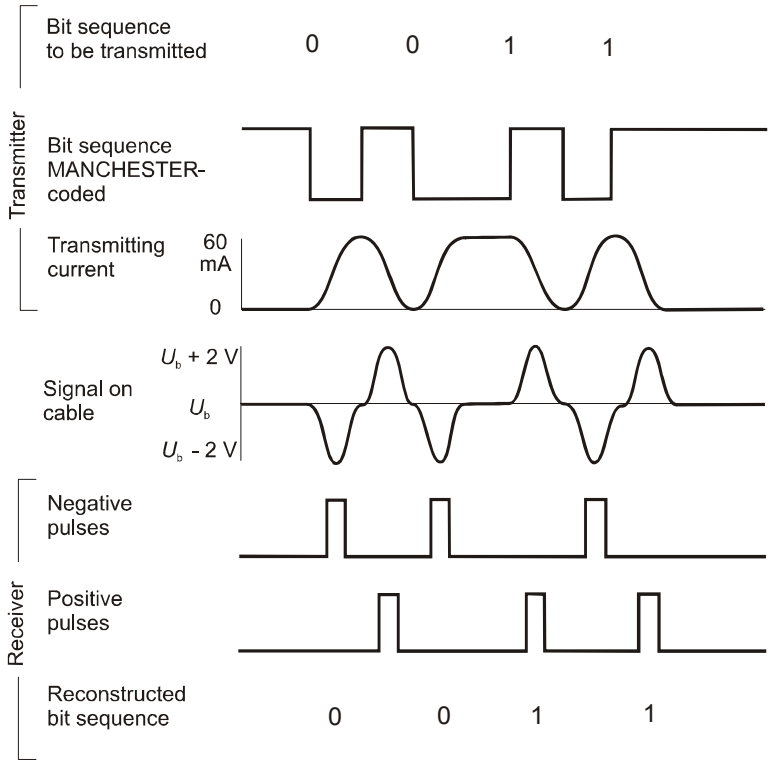


Figure 2 – Transmission coding

NOTE Because the information signal is superimposed on a d.c. supply voltage, a modulation must be employed that does not contain a d.c. voltage part. The transmission is asynchronous. To simplify synchronization of the slave a serially embedded synchronization information in the data signal flow is provided.

All messages are encoded in Manchester II format. Each message includes a start and an end bit. The idle state is represented by a "1". A "0" is encoded by a half bit time with high level followed by a half bit time of low level. A "1" is encoded by a half bit time of low level followed by a half bit time of high level.

The modulation shall be realized by the alternating pulse modulation (APM) with a $\sin^2$ signal wave form. The rising edge of the Manchester II format shall be represented as a positive and the falling edge as a negative pulse.

The transmission encoding and decoding is shown in Figure 2.

5.2.2 Transfer speed

The bit time (T_{Bit}) is defined as 6 µs. Thus, the bit sequence frequency shall be $166^2/_3$ kBit/s.

5.2.3 Transmitter requirements

The transmitter in both the master and the slave shall be implemented as a current sink. The current signal is superimposed on the d.c. voltage of the AS-i network. A falling edge of the Manchester II coded signal shall cause a current of

$$i(t) = I_{\text{send}} * \left(\frac{t}{3\mu s} - \frac{1}{2\pi} \sin\left(\frac{2\pi}{3\mu s} t \right) \right)$$

A rising edge shall cause a current of

$$i(t) = I_{\text{send}} * \left(1 - \frac{t}{3\mu s} + \frac{1}{2\pi} \sin\left(\frac{2\pi}{3\mu s} t \right) \right)$$

The amplitude I_{send} of the modulation current shall be between 55 mA and 68 mA.

The maximum deviation from the nominal bit time shall be less or equal to ± 0,1 % for the master and ± 0,2 % for the slave.

5.2.4 Receiver requirements

Together with the decoupling inductances of the decoupling circuit in the power supply, the send current waveform as defined in 5.2.3 will lead to a negative (positive) voltage pulse at each rising (falling) edge. The waveform of the pulses will be ideally

$$u(t) \approx \pm U_{\text{send}} * \sin^2\left(\frac{2\pi}{6\mu s} t \right)$$

with $U_{\text{send}} = const \approx 2\,V$

NOTE 1 In a real AS-i System, the declining edge of the pulses is flattened due to the characteristics of the decoupling circuit. In addition, amplitudes and waveform will be influenced by the physical properties of the AS-i line. The receivers therefore must be able to detect a more complex pulse spectrum.

The receiver shall be able to receive and decode a message as described below (see Figure 3).

The maximum pulse amplitude U_{max} of a message may vary between 1,5 V peak and 4 V peak.

NOTE 2 The differences in the amplitude U_{max} between consecutive Master requests will not vary in one configuration. Shown are the extreme values in different configurations and locations of the slave on the AS-i line. In a constant configuration, the relation of U_{max} between two slave responses at different locations of the line is up to 1:1,5.

– The amplitude of a valid pulse within a message may vary from 65 % to 100 % of the maximum amplitude U_{max}.

NOTE 3 For slaves according to previous versions of this standard it may vary from 80 % to 100 %.

Valid pulses start in a time window from $(n * 3\,\mu s)^{+1,0\,\mu s}_{-0,5\,\mu s}$ in relation to the initial pulse U_{init}.These pulses shall be accepted by the receiver.

Pulses outside a window from $(n * 3\,\mu s)^{+1,6\,\mu s}_{-0,8\,\mu s}$ shall not be accepted by the receiver.

Pulses (noise, ringing) of up to 30 % of U_{max} shall not disturb the message reception.

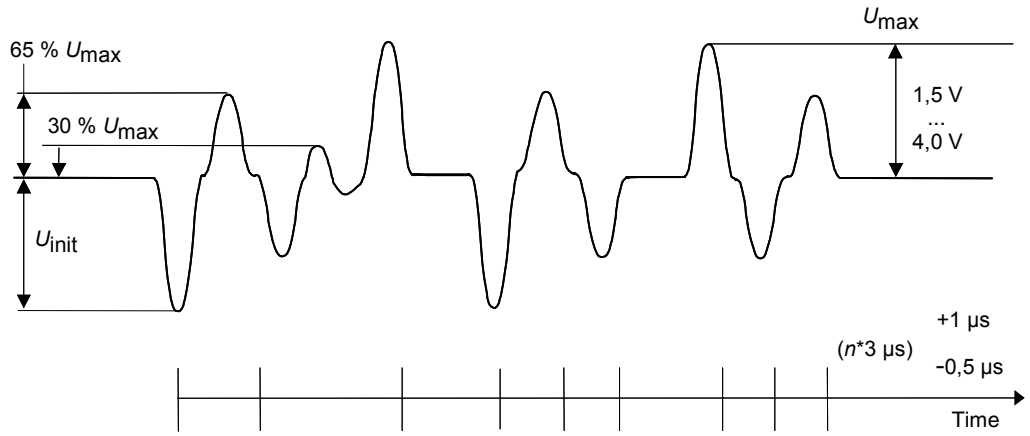


Figure 3 – Receiver requirements

NOTE 4 Pulse deviations from –0,8 µs up to +1,6 µs may occur due to a combination of different effects, for example capacitive load on the AS-i line, deviations from the oscillator frequency in the transmitter and in the receiver.

5.3 Power and data distribution

5.3.1 General

The simultaneous transmission of data and power on the AS-i line requires technical provisions for decoupling data and power.

The AS-i power supply has to provide the d.c. power for the whole network. On the other hand, it has to realise the conditioning of physical data transmission within the system. This feature comprises symmetrization and forming and adapting transmission signals according to the signal requirements defined in 5.2. The adapting circuit will furthermore be called "decoupling circuit".

Although the functions of these components are independent, it is useful to combine them for practical reasons.

The combination of a d.c. power supply, a symmetrization circuit and a decoupling circuit is called "AS-i power supply".

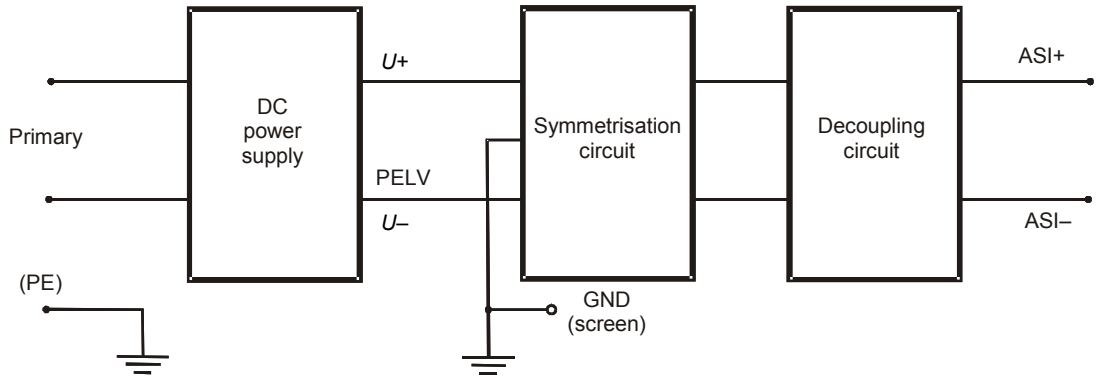


Figure 4 – AS-i power supply

5.3.2 AS-i power supply requirements

The AS-i power supply requirements are shown in Table 1:

Table 1 – AS-i power supply specifications

Characteristic	Specification
Output voltage at ASI+/ASI- (over the whole load range)	U_{ASI} = 29,5 V d.c. to 31,6 V d.c.
Rated output current	I_e as stated by the manufacturer
Additional current to meet charging processes for connecting additional slaves during normal operation	I_a = 0,4 A (12,5 mA for each standard slave / 6,5 mA for each slave in extended addressing mode)
Current limit	$I_{lim} > I_e + I_a$
Amplitude noise in the current range (measured at ASI+/ASI-)	50 mV_{pp} within 10 kHz to 500 kHz (visible noise band on oscilloscope)
Low frequency ripple (except overload)	300 mV_{pp} in the frequency range of 0 kHz to 10 kHz
Power on delay	≤ 2 s after reaching 5 V at output terminals

NOTE Any regulation of input and load changes should not affect the communication on the AS-i line; the AS-i transmission activity should not affect the power supply. The total effect on the AS-i line should not exceed the value of 50 mV_{pp} or 300 mV_{pp}, respectively, see above.

5.3.3 Start-up behaviour

Within 2 s after reaching 5 V the first time, the voltage level shall reach the maximum value of the master starting voltage (26,5 V). The time span between the minimum master starting voltage (22,5 V −1 V, see 8.5.2.1) and the min. AS-i voltage level (29,5 V) shall be less than 1 s. The voltage level has to increase steadily from 5 V up to normal operation voltage (29,5 V to 31,6 V).

NOTE The second demand is important because the master begins to work if the voltage exceeds its starting voltage of 22,5 V ± 1 V.

During start-up the power supply shall supply an increased current to meet the charging process in the system. This additional load will be equal to a capacitance of 15 mF.

Beginning from a voltage level of 5 V, the power supply shall give the rated output current I_e plus an additional current to load the above mentioned capacitance of 15 mF to meet the time restrictions.

5.3.4 Symmetrization and decoupling circuit

The symmetrization and decoupling circuit ensures several functions of the AS-i transmission system:

– providing the d.c. power to the AS-i line;
– signal shaping;
– terminating impedance (for the physical line);
– symmetrizing the AS-i line with respect to GND;
– rejection of common mode noise.

The equivalent decoupling network consists of two inductances and two resistors as well as the symmetrizing capacitors C_s as shown in Figure 5.

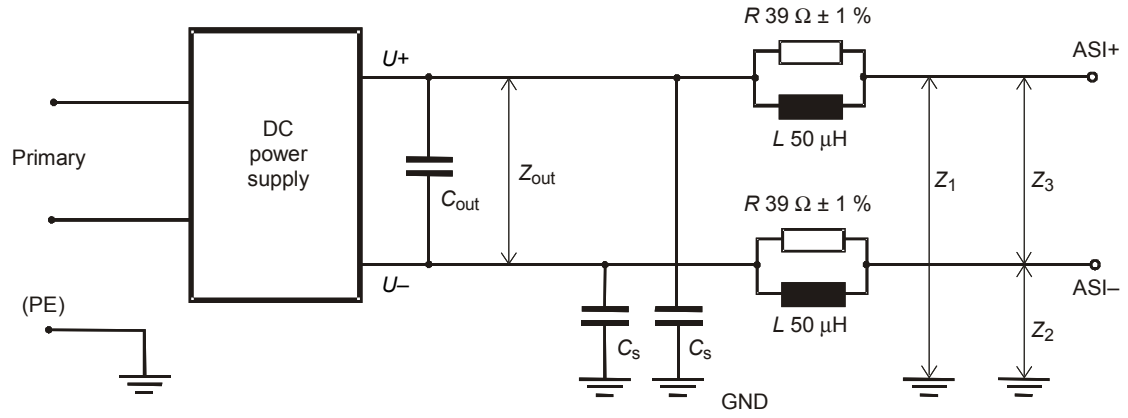


Figure 5 – Equivalent schematic of symmetrization and decoupling circuit

The symmetry capacitors C_s shall be located as close as possible to the decoupling circuit. These capacitances provide a symmetrical relation of ASI+/ASI− to ground. Equal values of at least 100 nF are recommended.

Table 2 – Symmetrization and decoupling circuit specifications

Characteristic	Specification
Inductance between ASI+/ASI−	100 µH ± 10 % (I_L=0 to I_{Lmax})
Short circuit / overload	May be applied for infinite time without causing defects in the decoupling circuit
Symmetry of ASI+/− against GND	$0,98 \leq \lvert Z_1\rvert / \lvert Z_2\rvert \leq 1,02$ within the frequency range of 10 kHz to 300 kHz and the whole load range
Source impedance	$\lvert Z_{out}\rvert < 0,5\ \Omega$ in the range of 10 kHz to 300 kHz
Decoupling impedance (C_s)	$\lvert Z_s\rvert < 5\ \Omega$ in the range above 300 kHz

5.4 AS-i topology and other components

5.4.1 AS-i line (minimum requirements)

The AS-i transmission medium can be any cable, shielded or non-shielded at which the following characteristics shall be provided for the full operating range:

at a frequency of 167 kHz:

R': < 90 mΩ/m

C': < 80 pF/m

Z : 70 Ω to 140 Ω

G': ≤ 5 μS/m

L': 400 nH/m to 1 300 nH/m

t': ≤ 8,3 ns/m

The recommended cross-section is 2 × 1,5 mm^2.

For short trunk lines without further branching cables with other specifications are tolerable, if the d.c. voltage drop on these lines does not affect the function of the connected devices.

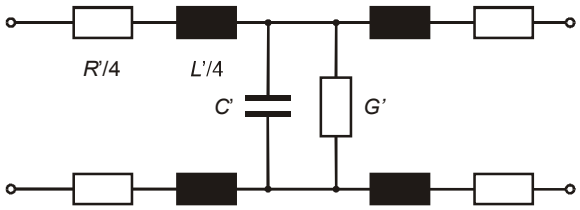


Figure 6 – Model of the AS-i transmission medium

NOTE 1 The characteristic impedance *Z* of a transmission line is defined by its distributed constants *R´*, *L´*, *C´*, *G´* and the frequency in use by the equation

$$Z = \left| \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \right|$$

The distributed constants can be measured at an electrical short length of the transmission line with open (*G´*, *C´*) respectively, shorted (*R´*, *L´*) end. The additional limitations of *Z* and the propagation delay time *t'* result from excluding such combinations of distributed constants which would lead to unfavourable high or low values of the characteristic impedance.

NOTE 2 Any cable that meets the above mentioned data may be used as the AS-i line. Nevertheless, several requirements and tolerances of this standard are intended to meet a total voltage drop (d.c.) along the AS-i transmission medium of up to 3 V. It is recommend to use a cross-section so that no higher voltage drop will occur. If a cable is to be used as the AS-i-line that does not meet the above-mentioned data, the total length of 100 m for the complete network may be affected.

NOTE 3 The propagation delay of a signal on the AS-i line is defined by the equation

$$t' = \sqrt{L'C' - \frac{R'G'}{\omega^2}}$$

and is typically 0,6 μs/100 m in one direction.

5.4.2 AS-i topology

The AS-i topology is the tree structure. The total length of the AS-i line shall not exceed 100 m. This length shall be calculated as the sum of all trunk lines.

There shall be no connection to GND in the network apart from the port GND at the power supply.

NOTE AS-i has been designed as a symmetrical system. The better the symmetry, the better the rejection of undesirable emission of AS-i signal components as well as incidence of AS-i relevant noise, even if the system is relatively large and distributed. This is important because the network is unshielded and may act as an antenna.

During normal operation, a voltage drop between the power supply and any point of the network of more than 3 V shall not occur unless a possibly higher voltage drop is specified in the product documentation of a particular slave.

5.4.3 AS-i repeater

The total length of the AS-i line is restricted to 100 m. An AS-i repeater regenerates the AS-i signal and provides galvanic separation between parts of the AS-i network so that network lengths of more than 100 m are possible.

Because of timing restrictions, it is not allowed to connect more than two repeaters in series. It is possible, however, to use several repeaters in parallel as long as they are connected to different branches of the tree structure of the network.

5.4.4 AS-i earth-fault detector

According to IEC 60204-1, earth faults on any control circuit shall not cause unintentional starting, potentially hazardous motions or prevent stopping of the machine. To fulfil this requirement, IEC 60204-1 indicates that control circuits that are not connected to the protective bonding circuit shall be provided with an insulation monitoring device that either indicates an earth fault or interrupts the circuit automatically after detecting an earth fault.

If an AS-i network is used to control potentially dangerous movements of a machine and IEC 60204-1 applies, an isolation monitoring device shall be installed. If the AS-i network is composed of separate parts that are isolated from each other, an insulation monitoring device shall be used for each isolated part of the network.

The insulation monitoring device used in AS-i networks shall be compatible with the requirements of the AS-i transmission system. Details are given in 8.3.2.

5.5 Communication

5.5.1 Communication principles

The AS-i system is a master-slave communication system composed of a single master and up to 31 (62 with extended addressing) slaves. Each slave shall have a unique address in the range of 1 to 31 (1A/1B to 31A/31B with extended addressing). This address is called operation address. The operation address shall be stored non-volatile. Only slaves with an operation address shall respond to data and parameter requests from the master.

The zero address is used during the change of a slave address. Normally, the zero address is stored volatile, except in factory new slaves. For details see 8.4.

A single transaction is composed of a master request and a slave response. A combined transaction is composed of several single transactions.

5.5.2 Transmission control

The exchange of data between the single master and up to 31 (62 with extended addressing) slaves is implemented by the processing of transactions (see Figure 7). A transaction starts with a master request. The master expects a slave response within a certain time. If the master does not receive a valid response from the slave within this time, it shall interpret this as a negative response. It may retransmit the master request once more. After receiving a valid response, the master shall start the next transaction after the send pause has elapsed. A slave shall not respond if it detects a faulty master request or if the master issues an unsupported request. The slave shall not give any negative response.

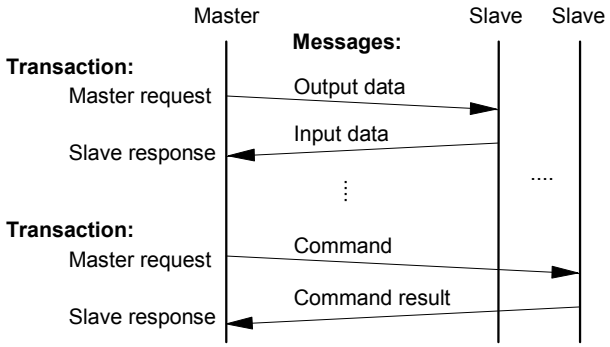


Figure 7 – Transactions

5.5.3 Timing requirements

All times specified in this paragraph are related to the signals on the AS-i line at the location of the master terminals.

An example of how to measure the master pause is shown in Figure 9. Other pauses shall be measured respectively. Both the master request and the slave response start with a zero as the first bit. Due to the Manchester II format this start bit leads only to a negative voltage pulse in the second half of the first bit time.

NOTE 1 Each receiver samples the voltage pulses with a certain threshold value. Therefore, and due to analogue filters, the start of the internal bit times may vary from those shown in Figure 9.

NOTE 2 The “master pause” is controlled by the slave and the “slave pause” is controlled by the master. These names, although illogical, are maintained for historical reasons.

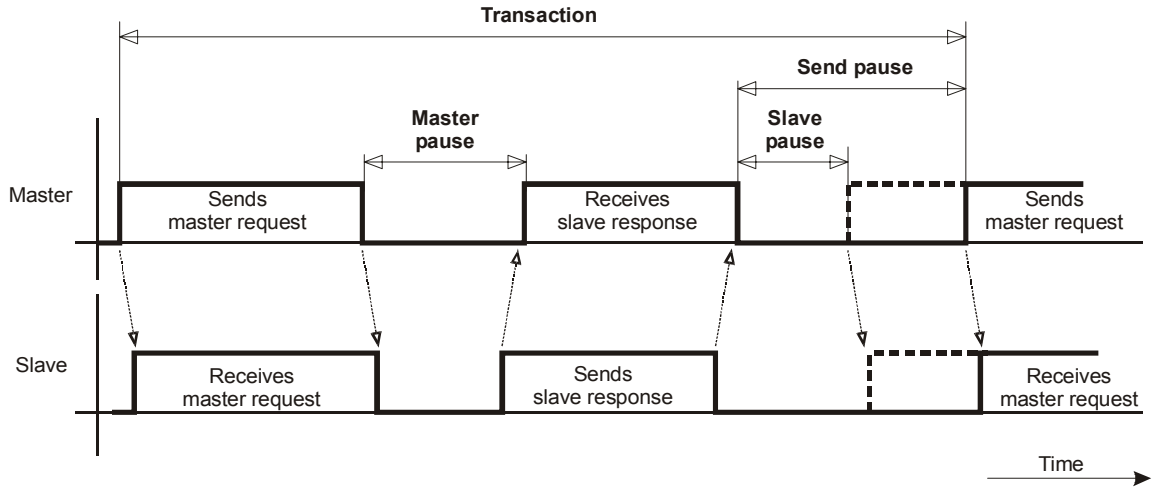


Figure 8 – Master and slave pause as viewed from master/slave point of view

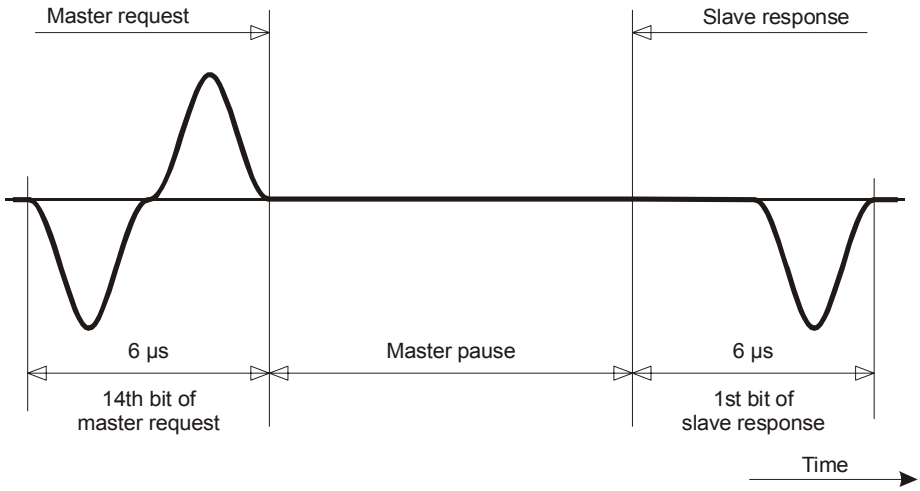


Figure 9 – Representation of the master pause

A transaction is split into two actions (master request and slave response) and two time intervals (master pause and send pause). A slave response time-out monitors a possible absence of a slave response:

1. **Master request**: sending a message from the master to a single slave and expecting a response from the slave.
2. **Master pause**: During this time the slave processes the requested function, produces the response data and starts within this time to send the response to the master. If a slave responds to a master request, it shall start its response within a period of 2 to 5 bit times after the end of a master request. The master shall be able to accept the start of a slave response within a period of 12 to 63 µs after the end of its request.

NOTE 3 For optimized noise suppression the AS-i master receiver should be switched off during the master pause for ≥1,5 bit times.

3. **Slave response**: Sending the slave data or the command result to the master.
4. **Slave pause**: After receipt of the slave response there shall be a minimum period during which a subsequent transmission shall not occur. The duration of this pause shall be 1,5 to 2 bit times. The slave shall be able to accept the start of a master request after a slave pause of 6 µs.
5. **Send pause**: After receipt of the slave response there shall be a minimum period during which a subsequent transmission does not occur. During normal operation the time of this pause shall be one slave pause in case of more than 30 transactions per AS-i cycle. In the case of 30 or less transactions per AS-i cycle the send pause may be prolonged to a maximum of 500 µs; but in this case the AS-i cycle time shall not be longer than 5 ms, including management and inclusion phase.
6. **Slave response time-out**: In case of no response from the slave in a certain time interval (the slave response time-out), the master shall end the transaction or repeat the transmission. This time shall be 11 bit times $\frac{+0\,\mu s}{-3\,\mu s}$.

NOTE 4 This is with respect to propagation delay on the line and the possible use of repeaters.

The time-out timer shall be started at the end of the transmission of the master request.

NOTE 5 Within the slave response time-out the master expects the beginning of a response telegram from the slave. After this time, the transmission function determines the absence of a slave response.

7. **Delay time for repeater**: The maximum delay time for a repeater shall be less than or equal to 7 µs for each direction.

NOTE 6 The master pause has to be less than or equal to 63 µs (see slave response time out). In the case of two repeaters in series, an asynchronous slave behind the second repeater and a propagation delay time of a 300 m line of about 5 µs appears. The maximum delay time for one repeater is 7 µs for each direction. The delay time of a repeater is to be measured as the time between a certain incoming voltage pulse to the respective outgoing voltage pulse on the other line.

NOTE 7 With presently available components, a stated AS-i cycle time shall be calculated as follows:

					If n = 33
	*n * Master request*	*= n * (14 Bit)*	*= n * 84 µs*	=	*2 772 µs*
+	*n * Master pause*	*= n * (3 Bit)*	*= n * 16 µs (synchr. slave)*	=	*528 µs*
+	*n * Slave response*	*= n * (7 Bit)*	*= n * 42 µs*	=	*1 386 µs*
+	*n * Send pause*	*= n * (2 Bit)*	*= n * 12 µs (min.)*	=	*396 µs*
=	T_{cycle}	*= n * (26 Bit)*	*= n * 154 µs (min.)*	=	*5 082 µs*

where *n* is the number of all AS-i requests during data exchange in the AS-i cycle and in the inclusion phase, including one repetition. In normal operation, *n* will be the number of activated slaves plus 2. This calculation is not affected by use of up to 62 slaves in extended addressing mode.

5.6 AS-i single transactions

5.6.1 Summary of transactions

Four single transaction types support data exchange, parametrization, network management and diagnostics. All master requests and all slave responses have the same structure and the same length of 14 bits (master) and 7 bits (slave), respectively.

A master may be able to issue all or some of the master requests listed in Tables 4 and 5 to start a transaction. Any slave shall be able to process and respond to all those master requests with the possible exception of the Address_Assignment request and R1 request. (For details see Annex B, AS-i Master Profiles)

5.6.2 Definition of master requests

The following types of master requests are defined:

Data_Exchange Serves for delivering and/or receiving the bit pattern to/from the data output/input of the slave.

Write_Parameter Serves for delivering and/or receiving the bit pattern to/from the parameter ports of the slave.

Address_Assignment Serves for assigning a non-volatile address (0...31 for standard addressing mode / 0,1A/1B,..31A/31B for extended addressing mode) to the slave with a zero address.

Commands Serve for miscellaneous functions like reset, reading the configuration, and reading the status of the slave.

A summary of all master requests is given in Tables 4 and 5. All other possible codes (not yet used in this standard) are reserved and shall not be implemented by any master or slave implementation used for AS-i networks.

5.6.3 Structure and semantics of the master requests

The requests sent by the master and received by the slave are composed of six elements as follows:

Start bit	Control bit	Address	Information	Parity bit	End bit

The bits of a master request shall be as follows:

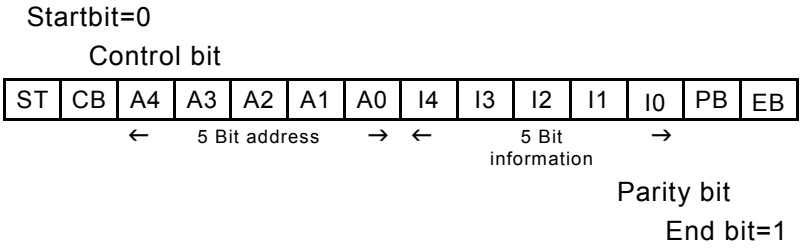


Figure 10 – Structure of a master request

Table 3 – Bit strings of the master requests

Bit string	Semantic	Comments
ST:	Start bit	Identifies the beginning of the master request always: ST = 0
CB:	Control bit	Identifies the type of request in the information cell; 0 = data/parameter transmission/address assignment; 1 = command transmission
A4..A0:	Address (5 bit)	To address the listed slaves 00_{Hex} = zero address. 01_{Hex} .. $1F_{Hex}$ = slave 1 through 31
I4..I0:	INFORMATION	These 5 bits contain the information to be transferred to the slave for every request type. Individual bits are described by the respective call type. For extended addressing I3 is used as an address extension (Sel-bit) to address the A- and B-slaves. Definition of Sel-bit: Sel=0 A-slave Sel=1 B-slave
PB:	Parity bit	Part of verification of the correctness of the master request at the slave. A correct message has even parity. 0 = even count of "1"-symbols in (CB, A4..A0, I4..I0) 1 = odd count of the "1"-symbols in (CB, A4..A0, I4..I0)
EB:	End bit	Identifies the end of the master request always: EB = 1

Table 4 – Master requests (standard addressing mode)

	ST	CB						I4	I3	I2	I1	I0		EB
Data_Exchange	=0	=0	A4	A3	A2	A1	A0	=0	D3	D2	D1	D0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Write_Parameter	=0	=0	A4	A3	A2	A1	A0	=1	P3	P2	P1	P0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Address_Assignment	=0	=0	=0	=0	=0	=0	=0	A4	A3	A2	A1	A0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Write_Extended_ID-Code_1	=0	=1	=0	=0	=0	=0	=0	=0	ID 3	ID 2	ID 1	ID 0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Delete_Address	=0	=1	A4	A3	A2	A1	A0	=0	=0	=0	=0	=0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Reset_Slave	=0	=1	A4	A3	A2	A1	A0	=1	=1	=1	=0	=0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Read_I/O-Configuration	=0	=1	A4	A3	A2	A1	A0	=1	=0	=0	=0	=0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Read_ID-Code	=0	=1	A4	A3	A2	A1	A0	=1	=0	=0	=0	=1	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Read_Extended_ID-Code_1	=0	=1	A4	A3	A2	A1	A0	=1	=0	=0	=1	=0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Read_Extended_ID-Code_2	=0	=1	A4	A3	A2	A1	A0	=1	=0	=0	=1	=1	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Read_Status	=0	=1	A4	A3	A2	A1	A0	=1	=1	=1	=1	=0	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
R1	=0	=1	A4	A3	A2	A1	A0	=1	=1	=1	=1	=1	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		
Broadcast	=0	=1	=1	=1	=1	=1	=1	=1	=0	=1	=0	=1	PB	=1
			←	5 Bit Address			→	←	5 Bit Information			→		

Table 5 – Master requests in the extended addressing mode

	ST	CB						I4	I3	I2	I1	I0		EB
Data_Exchange	=0	=0	A4	A3	A2	A1	A0	=0	$\overline{\text{Sel}}$	D2	D1	D0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Write_Parameter	=0	=0	A4	A3	A2	A1	A0	=1	$\overline{\text{Sel}}$	P2	P1	P0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Address_Assignment	=0	=0	=0	=0	=0	=0	=0	A4	A3	A2	A1	A0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Write_Extended_ID-Code_1	=0	=1	=0	=0	=0	=0	=0	=0	ID 3	ID 2	ID 1	ID 0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Delete_Address	=0	=1	A4	A3	A2	A1	A0	=0	Sel	=0	=0	=0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Reset_Slave	=0	=1	A4	A3	A2	A1	A0	=1	$\overline{\text{Sel}}$	=1	=0	=0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Read_I/O-Configuration	=0	=1	A4	A3	A2	A1	A0	=1	Sel	=0	=0	=0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Read_ID-Code	=0	=1	A4	A3	A2	A1	A0	=1	Sel	=0	=0	=1	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Read_Extended_ID-Code_1	=0	=1	A4	A3	A2	A1	A0	=1	Sel	=0	=1	=0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Read_Extended_ID-Code_2	=0	=1	A4	A3	A2	A1	A0	=1	Sel	=0	=1	=1	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Read_Status	=0	=1	A4	A3	A2	A1	A0	=1	$\overline{\text{Sel}}$	=1	=1	=0	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
R1	=0	=1	A4	A3	A2	A1	A0	=1	$\overline{\text{Sel}}$	=1	=1	=1	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		
Broadcast	=0	=1	=1	=1	=1	=1	=1	=1	=0	=1	=0	=1	PB	=1
			←	5 Bit Address			→	←		5 Bit Information		→		

NOTE Sel denotes the Select Bit, $\overline{\text{Sel}}$ the inverted Select Bit.

5.6.4 Structure and semantics of the slave responses

The responses sent by the slave have no control bit and no address and are composed of 4 elements as follows:

Start bit	Information	Parity bit	End bit

The bits of a slave response shall be as follows:

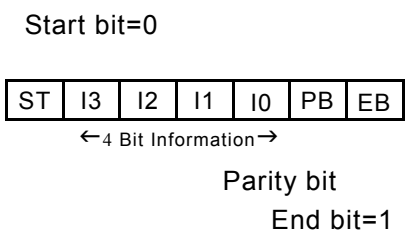


Figure 11 – Structure of a slave response

Table 6 – Bit strings of the slave responses

Bit string	Semantic	Comments
ST:	Start bit	Identifies the beginning of the slave response always: ST = 0
I3..I0:	Information	These 4 bits contain the information to be transferred to the master for every response type. Individual bits are described by the respective call type
PB:	Parity bit	Part of verification of the correctness of the slave response. Each correct message has even parity. 0 = even count of "1"-symbols in (I3..I0) 1 = odd count of the "1"-symbols in (I3..I0)
EB:	End bit	Identifies the end of the slave response always: EB = 1

5.6.5 Individual single transactions

5.6.5.1 Data_Exchange

The "Data_Exchange Request" shall be used by the master to transfer 4 bits of data (I3..I0) (3 bits of data plus Sel-Bit in case of extended addressing mode) to the data output register of the slave and to obtain 4 bits of data from the slave inputs. (For the behaviour of the input/output ports of the slave see 8.4).

The data exchange request shall have the following structure:

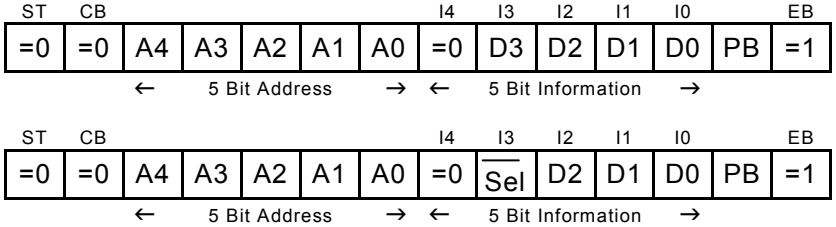


Figure 12 – Structure of a data exchange request (top: standard address mode; bottom: extended address mode)

The bits A4..A0 shall contain an operation address (1..31).

The slave response shall have the following structure:

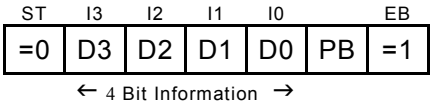


Figure 13 – Structure of the slave response (Data_Exchange)

If the slave is not activated, no answer shall be generated.

5.6.5.2 Write_Parameter

The "Write_Parameter Request" shall be used by the master to transfer the 4 parameter bits (I3..I0) to the parameter output register of the slave and to obtain 4 bits of data from the slave parameter inputs. (For the behaviour of the parameter input/output ports of the slave see 8.4).

The Write_Parameter request shall have the following structure:

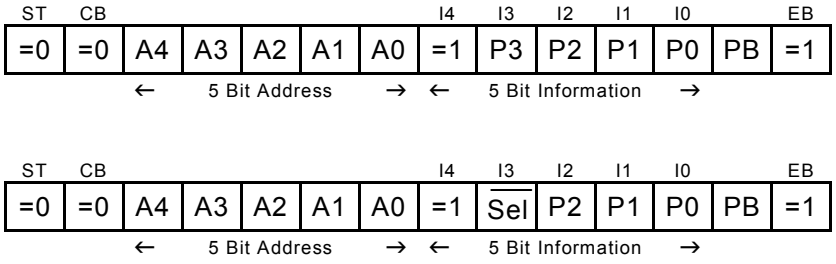


Figure 14 – Structure of the Write_Parameter request (top: standard addressing mode; bottom: extended addressing mode)

The bits A4..A0 shall contain an operation address (1..31).

The slave response shall have the following structure:

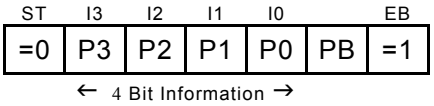


Figure 15 – Structure of the slave response (Write_Parameter)

The Write_Parameter request may affect the slave's state machine (see 8.4 for further details).

5.6.5.3 Address_Assignment

The "Address_Assignment request" shall be used by the master to enforce the slave to store the given address (I4..I0) non-volatile and to use this address when responding to master requests.

The address_assignment request shall have the following structure:

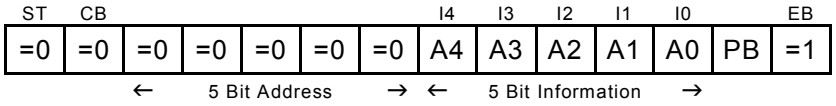


Figure 16 – Structure of the Address_Assignment request

The bits A4..A0 shall contain the zero address (00_{Hex}).

The slave response shall have the following structure:

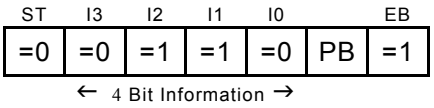


Figure 17 – Structure of the slave response (Address_Assignment)

After a successful Address_Assignment, a slave shall respond under the new address.

5.6.5.4 Write_Extended_ID-Code_1

The "Write_Extended_ID-Code_1" request is a command request and shall be used by the master to write the variable ID-Code nibble of the slave with address =0.

The ”Write_Extended_ID-Code_1” command shall have the following structure:

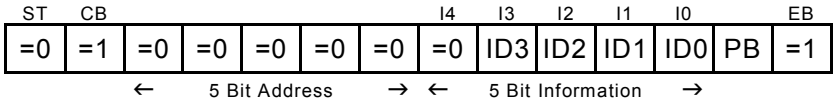


Figure 18 – Structure of the Write_Extended_ID-Code_1 request

For compatibility reasons with previous versions of this standard the response of a slave to this command is optional. After a successful Write_Extended_ID-Code_1 command, the slave response shall have the following structure:

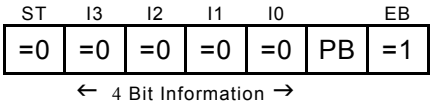


Figure 19 – Structure of the slave response (Write_Extended_ID-Code_1)

The new ID-Code nibble shall be stored non-volatile.

In extended addressing mode it is permitted for the manufacturer to block the write access by the user to the extended ID-Code 1. This allows to distinguish between more specific products. The manufacturer shall set all bits of the blocked extended ID Code 1 to "1" or as it is defined in the profile. Some ID-Code 1 may be fixed in specific profiles. In case of ID_Code2=F_{Hex} and ID_Code1=F_{Hex} the ID-Code 1 may be blocked by the manufacturer.

NOTE 1 If the slave is in the process of storing the new ID-Code nibble into the non-volatile memory (processing the "Write_Extended_ID-Code_1" request), a new "Write_Extended_ID-Code_1" request should not be issued by the master. The result of the storage process would otherwise be undefined.

NOTE 2 If the slave is used in Extended Address Mode ID3 is used as SEL to select A and B address. In this mode the user programmable part of the Extended ID-Code_1 (ID2..ID0) is limited to the range of 0 to 7.

5.6.5.5 Reset_Slave

The "Reset_Slave request" is a command request and shall be used by the master to reset a specific slave.

The Reset_Slave command shall have the following structure:

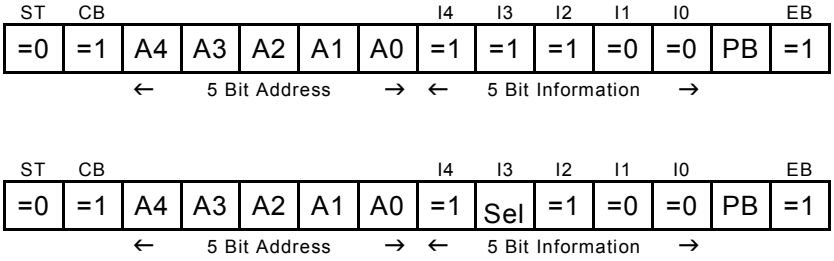


Figure 20 – Structure of the Reset_Slave request (top: standard addressing mode; bottom: extended addressing mode)

The slave response shall have the following structure:

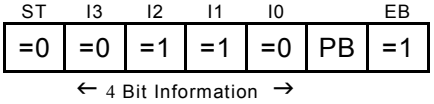


Figure 21 – Structure of the slave response (Reset_Slave)

The Reset_Slave request affects the slave's state machine. (see 8.4 for further details).

5.6.5.6 Delete_Address

The "Delete_Address request" is a command request and shall be used by the master to delete the operation address of a specific slave.

The Delete_Address command shall have the following structure:

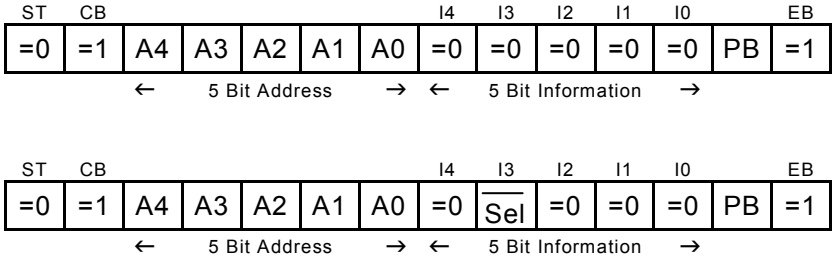


Figure 22 – Structure of the Delete_Address request (top: standard addressing mode; bottom: extended addressing mode)

The slave response shall have the following structure:

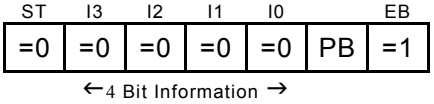


Figure 23 – Structure of the slave response (Delete_Address)

After a successful Delete_Address command, a slave shall respond with the zero address. This request does not cause the slave to store the address non-volatile.

The Delete_Address request does not affect the slave's state machine.

NOTE 1 A "Delete_Address" request to a slave with a zero address is identical to the "Write_Extended_ID-Code_1" request (see 5.6.5.4).

NOTE 2 If the slave is in the process of storing its address into the non-volatile memory (processing the "Address_Assignment" request), a "Delete_Address" request should not be issued by the master. The result of the storage process would be undefined.

5.6.5.7 Read_I/O_Configuration

The "Read_I/O_Configuration Request" is a command request and shall be used by the master to read the I/O configuration of a specific slave.

The Read_I/O_Configuration request shall have the following structure:

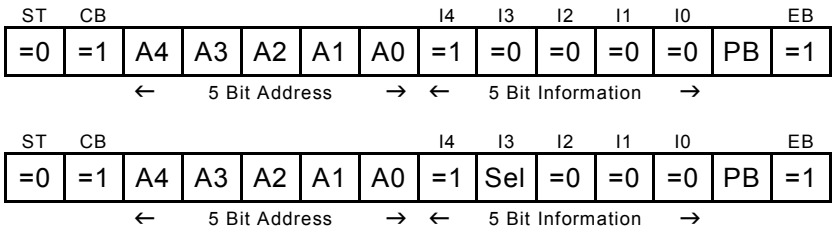


Figure 24 – Structure of the Read_I/O_Configuration request top: standard addressing mode; bottom: extended addressing mode)

The slave response shall contain the I/O-Code and shall have the following structure:

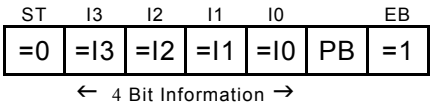


Figure 25 – Structure of the slave response (Read_I/O_Configuration)

The input/output data bits are configured to function as input only, as output only, as bi-directional input/output, or as tristate. This configuration depends on the environment and the required functionality. It is fixed for any particular slave, therefore. 16 different configurations as shown in Table 7 are defined. They are identified by the Identification Code, which shall be stored non-volatile in the slave.

The encoding of the I/O configuration shall be as follows:

NOTE 1 I/O configuration examples include:
– 4-bit input data to transmit the switching signals of 4 binary sensors,
– 4-bit output data to activate four actuators,
– 2-bit output plus 2-bit input to activate and monitor a double working actuator (e.g. bi-directional pneumatic valve that also transmits the sensor signals indicating the end positions)

Table 7 – I/O Codes (IN = Input; OUT = Output; TRI = Tristate; I/O = Input/Output or Bidirectional (B))

I/O Code (4-Bit)	I/O-Configuration D0	D1	D2	D3
0_{Hex}	IN	IN	IN	IN
1_{Hex}	IN	IN	IN	OUT
2_{Hex}	IN	IN	IN	I/O
3_{Hex}	IN	IN	OUT	OUT
4_{Hex}	IN	IN	I/O	I/O
5_{Hex}	IN	OUT	OUT	OUT
6_{Hex}	I/O	I/O	I/O	I/O
7_{Hex}	I/O	I/O	I/O	I/O
8_{Hex}	OUT	OUT	OUT	OUT
9_{Hex}	OUT	OUT	OUT	IN
A_{Hex}	OUT	OUT	OUT	I/O
B_{Hex}	OUT	OUT	IN	IN
C_{Hex}	OUT	OUT	I/O	I/O
D_{Hex}	OUT	IN	IN	IN
E_{Hex}	OUT	I/O	I/O	I/O
F_{Hex}	TRI	TRI	TRI	TRI

NOTE 2 In previous versions of this standard, I/O code 6_{Hex} was defined as IN I/O I/O I/O.

5.6.5.8 Read_Identification_Code

The "Read_Identification_Code request" is a command request and shall be used by the master to read the identification code of a specific slave.

The Read_Identification request shall have the following structure:

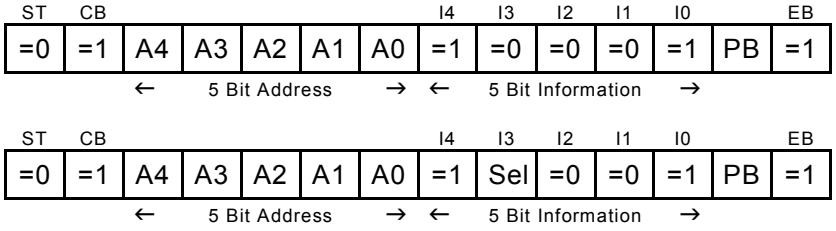


Figure 26 – Structure of Read_Identification_Code request (top: standard addressing mode; bottom: extended addressing mode)

The slave response shall contain the ID-Code and shall have the following structure:

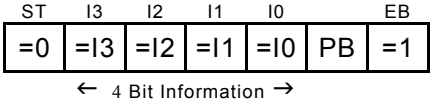


Figure 27 – Structure of the slave response (Read_Identification_Code)

If the Identification_Code of a slave is "A_{Hex}" the slave uses the extended addressing mode.

If the Identification_Code of a slave is "B_{Hex}" the slave transfers safe signals.

NOTE For further details, see Table 8 and Annex A.

5.6.5.9 Read_Extended_ID-Code_1/2

The "Read_Extended_ID-Code_1/2 Requests" are two command requests and shall be used by the master to read the content of the (optional) extended ID-Code register of a specific slave. These commands are optional.

The Read_Extended_ID-Code_1/2 command request shall have the following structure:

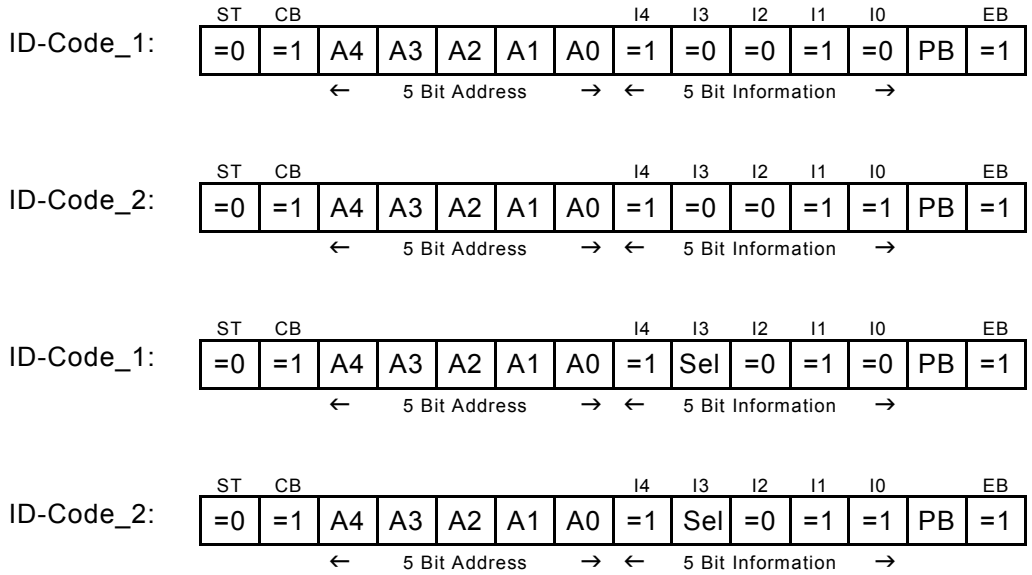


Figure 28 – Structure of Read_Extended_ID-Code_1/2 Request (top: standard addressing mode; bottom: extended addressing mode)

The slave response shall have the following structure:

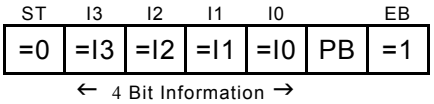


Figure 29 – Structure of the slave response Read_Extended_ID-Code_1/2

NOTE If the slave is used in the Extended Address Mode I3 in the slave response to Read_Extended_ID-Code_1 is used as SEL to show A/B address. In this mode the Extended ID-Code 1 (I2..I0) is limited to the range from 0 to 7.

5.6.5.10 Read_Status

The "Read_Status Request" is a command request and shall be used by the master to read the status of a specific slave.

The Read_Status request shall have the following structure:

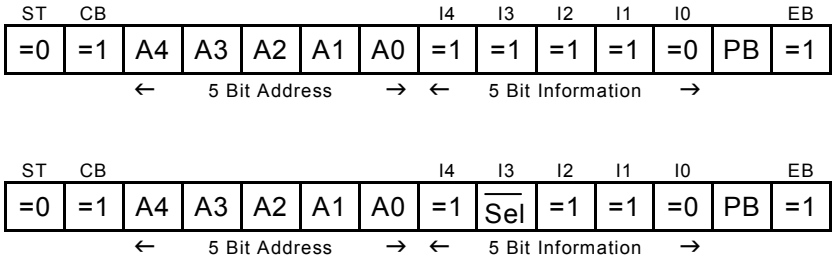


Figure 30 – Structure of Read_Status request (top: standard addressing mode; bottom: extended addressing mode)

The slave response shall have the following structure:

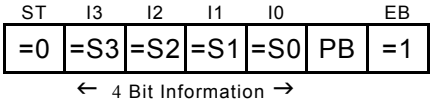


Figure 31 – Structure of the slave response (Read_Status)

5.6.5.11 R1

The "R1" is a command request. It is reserved and is optional.

This command will be coded in the information part of the master request as $1F_{Hex}$. The Reserve request shall have the following structure:

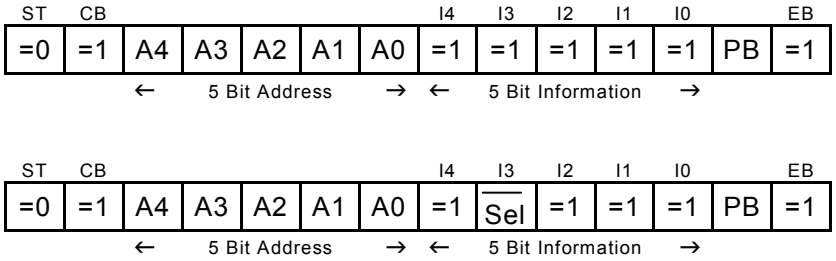


Figure 32 – Structure of R1 request (top: standard addressing mode; bottom: extended addressing mode)

The slave response may have the following structure:

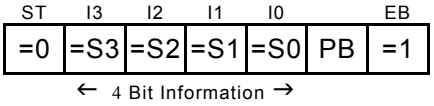


Figure 33 – Structure of the slave response (R1)

NOTE For compatibility reasons, the slave response may contain the content of the status register. This command has been a Read_Reset_Status in the first implementations of the system (up to version 2.0 of this standard). It is recommended not to use the command in new developments.

5.6.5.12 Broadcast (Reset)

The "Broadcast (Reset)" is a command request and is optional.

The Broadcast (Reset) request shall have the following structure:

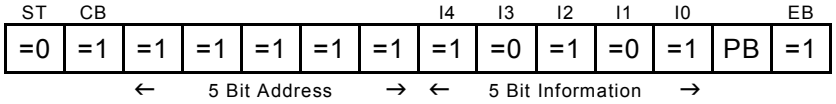


Figure 34 – Structure of the Broadcast (Reset) request

The slaves shall react with a Reset. There shall be no slave response to this request.

NOTE 1 In a network, this command may be used by the master to reset all slaves which realise the command. Thus it is used to perform an action similar to an emergency stop. As the Reset_Slave request, the “Broadcast (Reset)” affects the slave’s state machine. (see 8.4 for further details).

NOTE 2 For future expansion of the system the information part 15_{Hex} is reserved for broadcast commands.

5.7 AS-i combined transactions

5.7.1 General

AS-i Single Transactions contain a maximum of 4 bits of information. If more than 4 bits of consistent information is to be transferred an additional set of rules has to be established to control the data transfer. There are several sets of rules available for different types of applications (e.g. single direction word transfer for analogue sensors or actuators, full duplex data exchange for intelligent slaves etc.). These are defined in the subsequent paragraphs.

To identify slaves that are capable to communicate via combined transactions the ID-codes (see 5.6.5.8) or extended ID-codes (see 5.6.5.9) are used. Masters that are capable to communicate via combined transactions are identified by their master profiles (see Annex B). Table 8 lists all presently defined combined transaction types.

Table 8 – List of combined transaction types

Combined transaction type	Slave profile	Master profile	Remarks
Type 1	S-7.1	Not supported	*For new designs it is recommended to use S-7.3*
Type 1	S-7.2	Not supported	*For new designs it is recommended to use S-7.4*
Type 1	S-7.3	M3	16 bit inputs or outputs
Type 1	S-7.4	M3	Complex field devices
Type 2	S-7.5.5	M4	Combi field devices
Type 2	S-7.A.5	M4	Combi field devices
Type 2	S-B.A.5	M4	Serial communication field devices
Type 3	S-7.A.7	M4	4I/4O in extended address mode
Type 3	S-7.A.A	M4	8I/8O in extended address mode
Type 4	S-7.A.8	M4	16 bit inputs in extended address mode
Type 4	S-7.A.9	M4	Dual 16 bit inputs in extended address mode
Type 5	S-6.0	M4	High speed 16 bit inputs and outputs
AS-i safety	S-0.B	Any	AS-i safety input slaves
AS-i safety	S-7.B	Any	AS-i safety input slaves with standard outputs

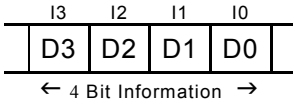
5.7.2 Combined transaction type 1

The combined transaction type 1 mechanism is handled according to the method given below. It uses the standard AS-i data transfer mechanisms to build a half duplex data transfer channel for byte transfer between the master and the slave with the profiles given in Table 8.

NOTE Combined transaction type 1 may be used for analogue sensors and actuators; replacement of 4 mA to 20 mA interfaces, for scanners and displays with 8 characters maximum. It may further be used for complex field devices with variable parameters; replacement for 4 mA to 20 mA interfaces with parameter exchange.

5.7.2.1 Definition of I/O data and parameter bits

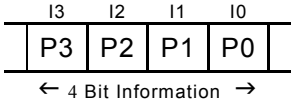
The definition of the I/O data bits (Single transaction “Data_Exchange”) is given in Figure 35.



Bit	Type	Definition
D3	I/O	Control bit for data transfer (“toggle bit”)
D2	I/O	Most significant data bit of the data triple
D1	I/O	Data bit of the data triple
D0	I/O	Least significant data bit of the data triple

Figure 35 – Definition of the I/O data bits in combined transaction type 1

The definition of the parameter bits (Single transaction „Write_Parameter“) is given in the following figure. This definition is valid for the slave profile S-7.4 only. For details see Annex A.



Px (hex)	P3	P2	P1	P0	Definition
F	1	1	1	1	Normal data cycle
E	1	1	1	0	Normal data cycle (optional)
D	1	1	0	1	Read ID string
C	1	1	0	0	Read diagnosis
B	1	0	1	1	Read parameter string
A	1	0	1	0	Write parameter string
0	0	0	0	0	Used to generate unequal slave responses

Figure 36 – Definition of the parameter bits in combined transaction type 1

When “Normal data cycle” is selected by the parameters, the data transfer direction is determined by the extended ID2 code as defined in 5.7.2.2. It cannot be changed during operation. The master acts as data source in case of an analogue output and as a data sink in case of an analogue input.

When “Read ID String”, “Read Diagnosis” or “Read parameter string” is selected by the parameters, the slave acts as data source and the master acts as data sink. When “Write parameter string” is selected by the parameters, the master acts as data source and the slave acts as data sink.

NOTE Due to this definition of data and parameter bits, combined transaction type 1 can only be used with standard addressing mode.

5.7.2.2 Definition of data transfer direction and number of channels

The data transfer direction and the number of data channels is defined by the extended ID2 code (Single transaction “Read_ID2-Code”) stored in the slave (see Annex A for details).

NOTE For AS-i slaves that do not support the extended ID1/ID2 codes, the AS-i master should assume the default value extended ID2 = F_{Hex}. This corresponds to an analogue input slave with 4 channels. It is allowed to implement less than 4 channels with extended ID2 code = F_{Hex}. In this case, the slaves send data for the

implemented channels only. The master should mark the input values of the unused channels in its analogue input data image as invalid. Slaves that support the extended ID1/ID2 codes should not use the default value extended ID2 = F_{Hex}.

5.7.2.3 Data transfer

If the slave is defined as data source and the master as data sink the data transfer is controlled by the master in a way shown in Table 9. The master issues a request consisting of a 3 bit command as shown. The slave answers in the same or in one of the next "Data_Exchange" telegrams with 3 bit data.

If the master is defined as data source and the slave as data sink, the data transfer is controlled by the slave in a similar manner as shown in Table 10. The slave issues a request consisting of a 3 bit command as shown. The master answers in one of the next "Data_Exchange" telegrams with 3 bit data.

Irrespective of the data transfer direction, the control bit K (the "Toggle Bit") is inverted by the master every time the content of the command or data bits change.

Table 9 – Data transfer from slave to master in combined transaction type 1

Master (request)		Slave (answer)	Remarks
K 1 1 1	>	$\overline{K}$ D2 D1 D0	
K 1 1 0	>	$\overline{K}$ D2 D1 D0	
K 1 0 1	>	$\overline{K}$ D2 D1 D0	
K 1 0 0	>	$\overline{K}$ D2 D1 D0	
K 0 1 1	>	$\overline{K}$ D2 D1 D0	
K 0 1 0	>	$\overline{K}$ D2 D1 D0	
K 0 0 1	>	$\overline{K}$ D2 D1 D0	
K 0 0 0	>	$\overline{K}$ D2 D1 V	

NOTE 1 The data in this table is shown at controller level. On the AS-i line the master requests will be transmitted in inverted form (see 5.6.5.4).

The request "K111" also serves as "latch" command. After having received this command the data bits of the whole sequence shall not be updated by the data source until completion of the whole sequence. This ensures data consistency.

Table 10 – Data transfer from master to slave in combined transaction type 1

Master (request)		Slave (answer)	Remarks
K X X X	>	$\overline{K}$ 1 1 1	
K D2 D1 D0	>	$\overline{K}$ 1 1 0	
K D2 D1 D0	>	$\overline{K}$ 1 0 1	
K D2 D1 D0	>	$\overline{K}$ 1 0 0	
K D2 D1 D0	>	$\overline{K}$ 0 1 1	
K D2 D1 D0	>	$\overline{K}$ 0 1 0	
K D2 D1 D0	>	$\overline{K}$ 0 0 1	
K D2 D1 D0	>	$\overline{K}$ 0 0 0	
K D2 D1 V	>	$\overline{K}$ 1 1 1	Start of the next cycle (or "K000" if transactions are to be terminated)

NOTE 2 The data in this table is shown at controller level. On the AS-i line, the master requests will be transmitted in inverted form (see 5.6.5.4).

The transfer is started with the request "K111". It ends with the request "K000". These two requests are mandatory. If less than 23 bits are to be transferred, the requests beginning with "K110" may be omitted. Length of data and definition of the individual bits are given in the slave profiles (see Annex A for details) or in the manufacturer's documentation.

The last bit of the sequence is the Valid Bit “V”. If it is set = 1 the sequence was transferred correctly and the data received is marked valid.

5.7.2.4 Slave response times

5.7.2.4.1 Input data slaves

When the master addresses a new data triple of the input slave (that is, the toggle bit of the data has changed) the slave shall respond within 250 µs with a new value. This ensures that maximum data transfer times can be calculated.

5.7.2.4.2 Output data slaves

After having received the command “K111” the master changes the Toggle Bit and sends new data. The slave shall respond with a new command data triple within 250µs. This sequence continues until the slave addresses the last data triple and the master responds with the data triple containing the Valid Bit “V”.

The slave then may wait up to a maximum of 3 s until it starts a new sequence with “K111”. The maximum time delay that the output slave will wait until a new data transfer cycle starts shall be stated in the manufacturers documentation. This item shall be named “max. delay between two consecutive data transfer cycles”.

5.7.2.5 Read ID, Read Diagnosis, Read and Write Parameter

If the normal data transfer cycle is to be interrupted to insert a Read ID, Read Diagnosis, Read Parameter, the master shall follow the sequence shown in Figure 37 (Slave profiles S-7.2 and S-7.4 only).

NOTE The 500 ms waiting time is needed because the Write_Parameter request is issued acyclically by the master. The 1 ms waiting time is needed by the slave to perform its internal changeover process.

After the first call “Write_Parameter (xxxx) to Slave” the master shall not change the four output bits. When the waiting time of 1 ms is exceeded, the master shall change the toggle bit D3 and at the same time it shall set the bits D2, D1 and D0 to “111” (host level).

If the normal data transfer cycle is to be interrupted to insert a Write Parameter, the master shall follow the sequence shown in Figure 38 and the slave shall follow the sequence shown in Figure 39 (Slave profiles S-7.2 and S-7.4 only).

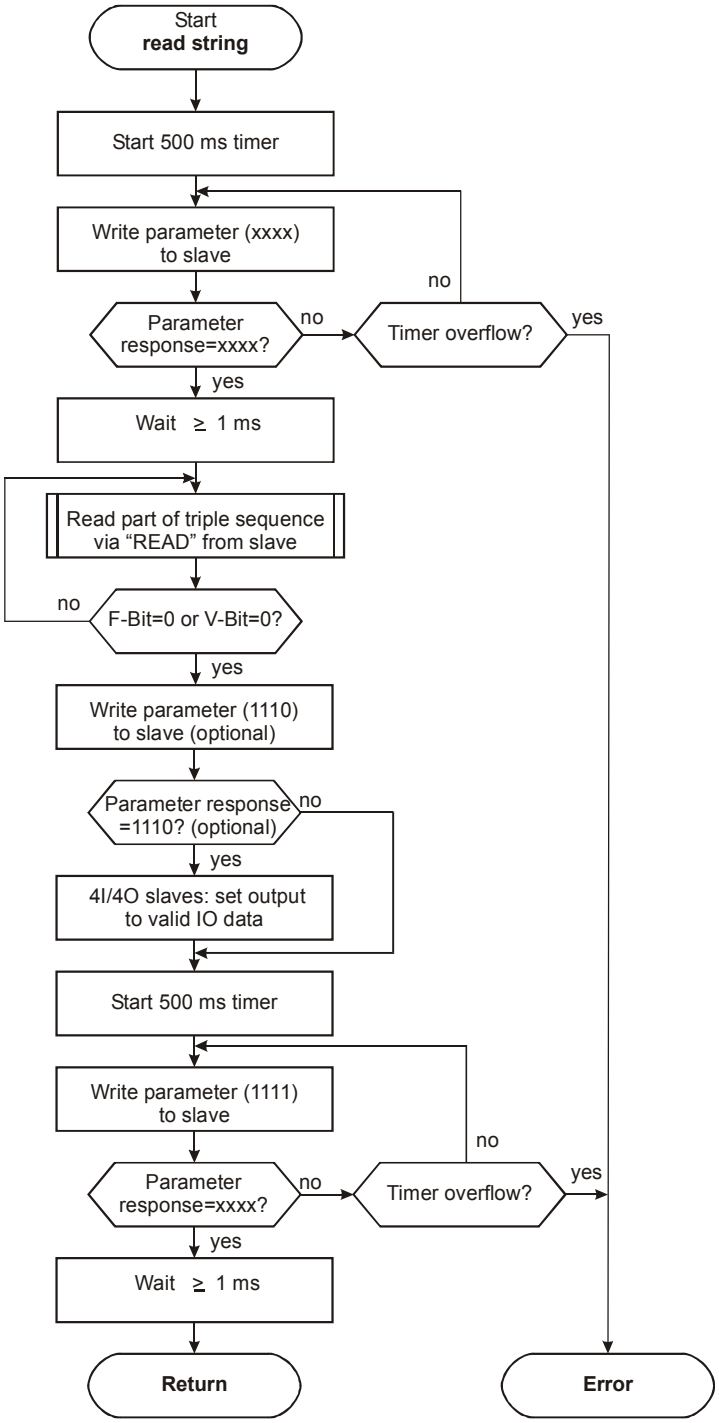


Figure 37 – Function sequence to Read ID, Read Diagnosis, Read Parameter in combined transaction type 1

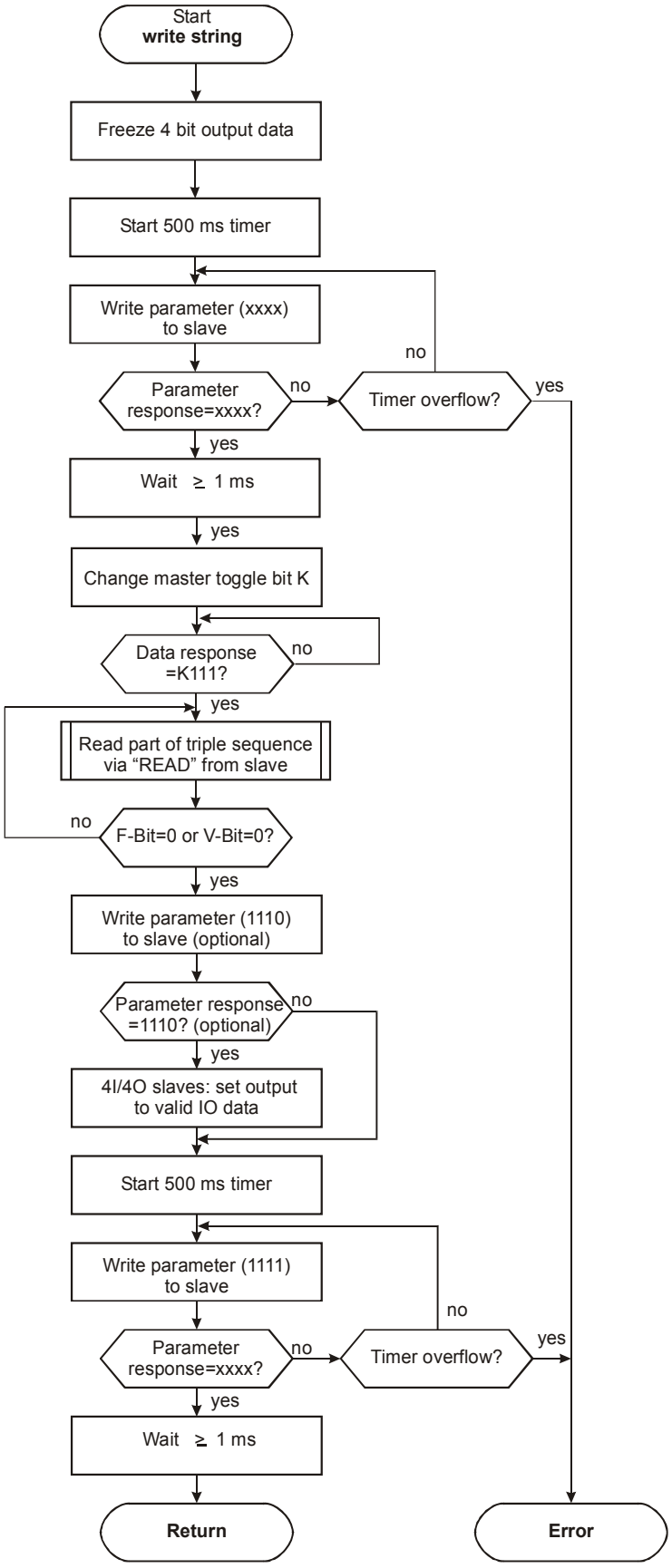


Figure 38 – Function sequence to Write Parameter in combined transaction type 1

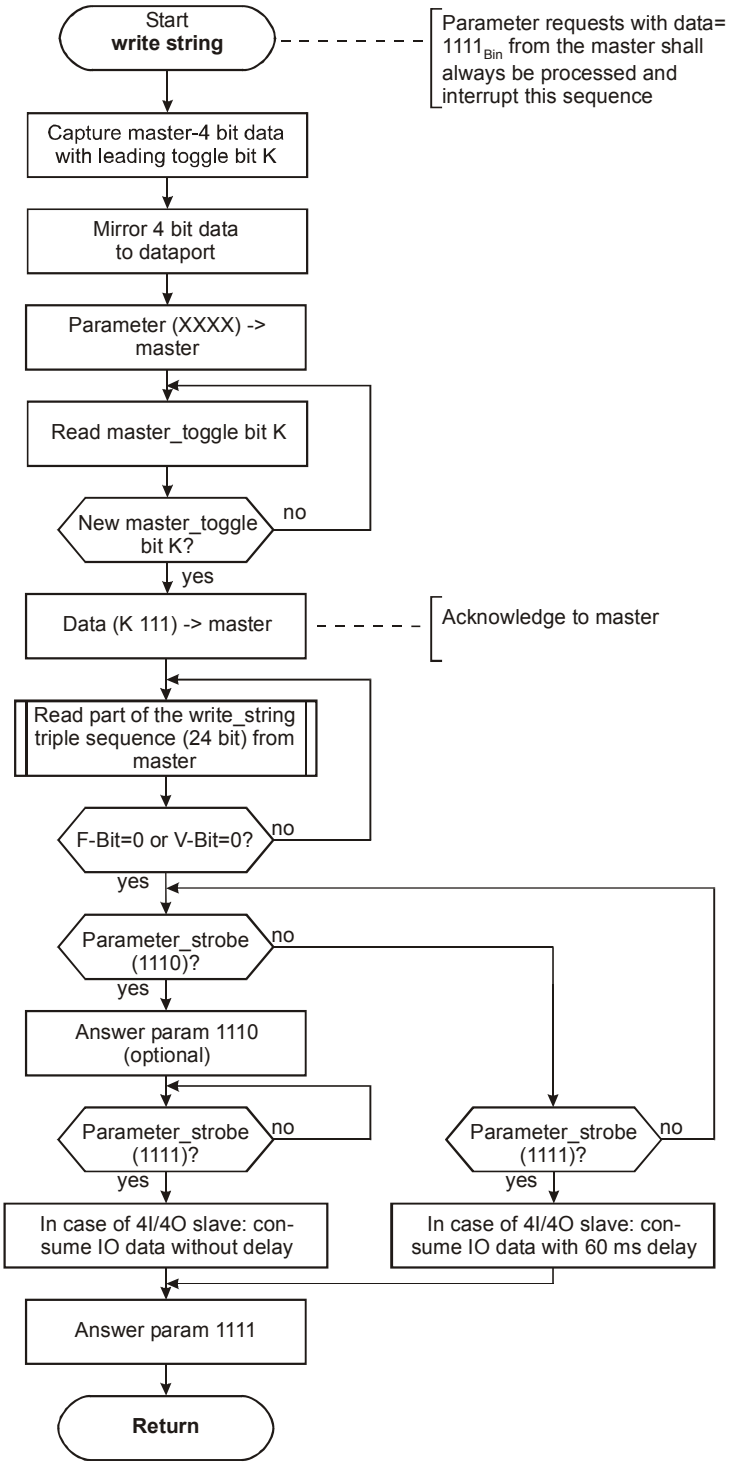


Figure 39 – Behaviour of the slave receiving a complete parameter string from the master in combined transaction type 1

5.7.2.6 Error handling

5.7.2.6.1 Power-up

The data transferred is marked as not valid via the Valid Bit until a complete and error free cyclical transfer of data has been completed after a power-up condition.

5.7.2.6.2 Data triples in wrong sequence

The data source checks that the data triples are called for in the correct sequence by the data sink. If this is not the case it marks the data as erroneous via the Valid Bit. It may also respond to other commands with “K000” until a new cycle begins.

5.7.2.6.3 Data in varying length

The data source checks that data is transferred cyclically and with constant length. If the data length changes during operation, the data is marked as erroneous via the Valid Bit until a new cycle has been completed correctly.

5.7.2.6.4 Recognition of an acknowledgement phase

After interruption of the data traffic between AS-i master and AS-i slave, the input data in the AS-i master is set to “0_{Hex}”. To ensure that this does not lead to a wrong interpretation of the data, the values in question are to be marked erroneous via the Valid Bit.

5.7.2.6.5 Toggle bit timeout

If both communication partners are waiting for the control bit K to change, it is recommended to monitor the toggle period and perform a timeout after 1 s. When the timeout has occurred, the master and/or the slave shall mark the transmitted data as erroneous. If the slave monitors the Toggle Bit timeout, this has to be stated in the manufacturer’s documentation.

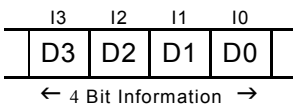
5.7.3 Combined transaction type 2

The combined transaction type 2 mechanism is handled according to the standard given below. It uses the standard AS-i data transfer mechanisms to build a full duplex bit-serial data transfer channel between the master and the slave with the profiles listed in Table 8.

NOTE Combined transaction type 2 may be used for analogue sensors, actuators and field devices with variable parameters; for sensors, actuators and field devices both analogue and digital; for displays with more than 8 characters; replacement for 4 mA to 20 mA interfaces with parameter exchange.

5.7.3.1 Definition of I/O data and parameter bits

The definition of the I/O data bits (Single transaction “Data_Exchange”) is given in Figure 40:



Bit	Type	Definition
D3	I	Serial data in
D2	I	Serial clock in
D1	O	Serial data out
D0	O	Serial clock out

Figure 40 – Definition of the I/O data bits in combined transaction type 2

The AS-i parameter bits (Single transaction „Write_Parameter“) are not used for combined transaction type 2. They may be defined in the respective slave profiles.

NOTE Due to this definition of data bits, combined transaction type 2 can be used with standard address mode and/or with extended address mode. The input data bits D0 and D1 and the output data bits D2 (and D3 if standard addressing mode is used) are not needed for combined transaction type 2 and may be used for additional normal bit information transfer.

The combination of the serial clock and serial data bits are defined as follows:

Table 11 – Definition of serial clock and data in combined transaction type 2

Serial clock	Serial data	Definition
0	0	Data bit: 0
0	1	Data bit: 1
1	0	Separator / clock
1	1	Idle / no data

5.7.3.2 Data transfer

The data transfer is controlled by the following rules:

If there is no data to be transferred between the master and the slave (both data channels run idle), then both sides transfer the telegram "SEP" and "IDLE" continuously. The master begins the transfer and the slave answers with the same information:

Table 12 – Data transfer in combined transaction type 2

Master request		Slave response		
Serial clock (D0 Out)	Serial data (D1 Out)	Serial clock (D2 In)	Serial data (D3 In)	
1	0	1	0	Separator / clock
1	1	1	1	Idle / no data

In this state the slave shall always echo the information received from the master. The master shall send the alternative next telegram only after it has received the correct echo to the last telegram from the slave.

An oscilloscope connected to the respective inputs and outputs of the slave will typically display a picture as shown in Figure 41.

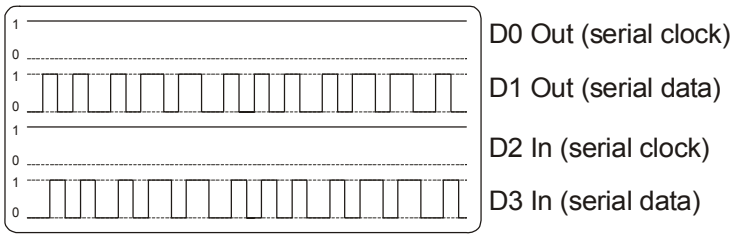


Figure 41 – Typical combined transaction type 2 signals as viewed by an oscilloscope (both data channels run idle)

A timeout error is detected if master or slave do not receive the expected information from the other side within a time of 100 ms.

If the master wants to transmit data to the slave it shall replace its "idle" telegram by the respective data telegram. If the slave wants to transmit data to the master it shall replace its "idle" telegram by the respective data telegram. The separator / clock telegram exchange between the data or idle telegrams remains unchanged.

The most significant bit is transmitted first. The data information may have any length. Two different data information are separated by at least one "idle" telegram.

An oscilloscope connected to the respective inputs and outputs of the slave will, for example display the picture shown in Figure 42.

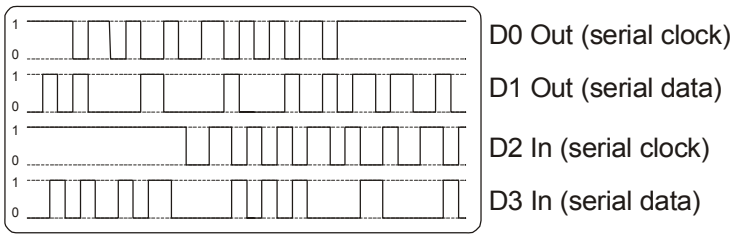


Figure 42 – Typical combined transaction type 2 signals (the master transmits the byte 10101011_{Bin}, the slave transmits 01110101_{Bin}):

5.7.3.3 Slave response times

When the master transmits a new information (that is, the state of the serial clock changes) the slave shall respond in the actual or next cycle at the latest with a new information. This ensures that maximum data transfer times can be calculated.

5.7.3.4 Exception handling

5.7.3.4.1 Power-up

The user data in the master are marked as invalid until a complete and error-free data transfer has been performed.

5.7.3.4.2 Interruption of data traffic

When a master with integrated support of combined transaction type 2 detects that a slave of a corresponding profile is not in the LAS anymore, it marks the corresponding input values of all channels of this slave as invalid and sets them to default values if applicable.

A slave that supports combined transaction type 2 shall implement a watchdog function to monitor interruptions of data traffic. In case of interruption of data transfer detected by the watchdog the following actions shall be taken:

An output slave shall set its outputs to default values, if applicable.

– The slaves resets its state machine, that means it does not respond any more to data telegrams until it receives a new parameter telegram from the AS-i master.
– A timeout error is detected if the slave does not receive the expected information from the master within a time of 100 ms.

5.7.3.4.3 Interruption/error of data communication

The master and slave shall check incoming data for violation of the coding rules.

If a master with integrated support of combined transaction type 2 detects that the rules of the serial data communication are not followed by the slave (e.g. timeout) it will interrupt the serial data communication immediately, mark all data as invalid and return to the state "start serial communication".

When a slave detects that the rules of the serial data communication are not followed by the master (e.g. timeout) it will interrupt the serial data communication immediately, set outputs to default values and return to the state "start serial communication".

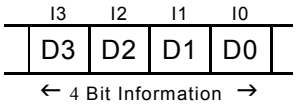
5.7.4 Combined transaction type 3

The combined transaction type 3 mechanism is handled according to the specification given below. It uses the standard AS-i data transfer mechanisms to build a full duplex 4 bit or 8 bit data transfer channel between the master and the slave in extended address mode with the profiles given in Table 8.

NOTE Combined transaction type 3 is intended for use in keypads, signal towers, valve terminals and similar devices. It may further be used for 8 bit sensors, actuators and field devices.

5.7.4.1 4I/4O data transfer

The definition of the I/O data bits (Single transaction “Data_Exchange”) for the 4I/4O data transfer is given in Figure 43:



Bit	Type	Definition
D3	I	Data Bit DI3
D2	I	Data Bit DI2
D1	I	Data Bit DI1
D0	I	Data Bit DI0
D3	O	Select Bit
D2	O	Output Multiplex Bit
D1	O	Data Bit DO1, DO3
D0	O	Data Bit DO0, DO2

Figure 43 – Definition of the I/O data bits in combined transaction type 3 (4I/4O)

The 4 output-bits are transferred cyclically in 2 groups. If the information bit D2 (Output Multiplex Bit) = 1 (ASI-level) then DO0 and DO1 are transferred to the slave, if the information bit D2 = 0 (ASI-level) then D2 and D3 are transferred to the slave in a data exchange request. The slave shall reassemble the two groups of data to the 4 appropriate output ports (Out 1 to Out 4) dependent on the information bit D2.

To ensure that both groups of output data are refreshed continuously the alternation of the D2 bit shall be supervised by the slave. If there is no alternation of the D2 bit at least every 300 ms (after the activation of the slave) the slave shall stop communication and switch all outputs into the OFF-state (protocol-watchdog).

NOTE In the case of a protocol watchdog event, it is recommended to stop communication.

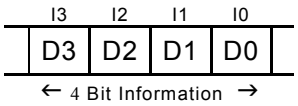
The AS-i parameter bits (Single transaction „Write_Parameter“) are not used for combined transaction type 3. They may be defined in the respective slave profiles.

The data is transferred to the IDI and from the ODI of the master.

5.7.4.2 8I/8O data transfer

5.7.4.2.1 Definition of data and parameter bits

The definition of the I/O data bits (Single transaction “Data_Exchange”) for the 8I/8O data transfer is given in Figures 44a and 44b:



Bit	Type	Definition
D3	I	Input Multiplex Bit 1
D2	I	Input Multiplex Bit 0
D1	I	Data Bit DI1, DI3, DI5, DI7
D0	I	Data Bit DI0, DI2, DI4, DI6
D3	O	Select Bit
D2	O	Inverted Input Multiplex Bit 0 from previous data transfer
D1	O	Data Bit DO1, DO3, DO5, DO7
D0	O	Data Bit DO0, DO2, DO4, DO6

Figure 44a – Definition of the I/O data bits in combined transaction type 3 (8I/8O)

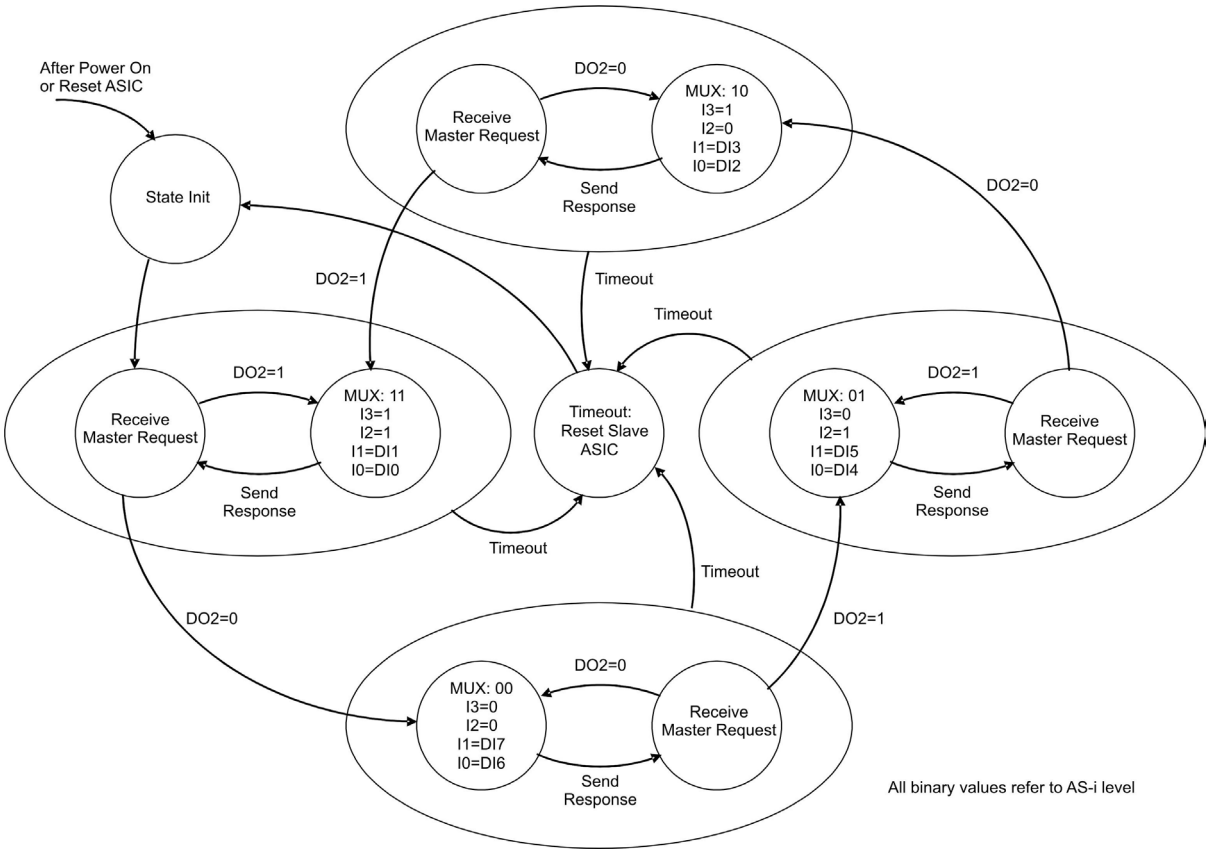


Figure 44b – State diagram of the slave for combined transaction type 3 (8I/8O)

Figure 44 – Definition and state diagram of the slave for combined transaction type 3

The 8 input bits are transferred cyclically in 4 groups of 2 data bits each. Each group is addressed with the Input Multiplex Bits DI2 and DI3, the data are the bits D0 and D1. If the Multiplex Bits are 00_{Bin} then the input bits DI6, DI7 are transferred to the master and the master sends the output bits DO6, DO7 in the following data telegram. If the Multiplex Bits are

01_{Bin} then the input bits DI4, DI5 are transferred to the master and the master sends the output bits DO4, DO5 in the following data telegram. If the Multiplex Bits are 10_{Bin} then the input bits DI2, DI3 are transferred to the master and the master sends the output bits DO2, DO3 in the following data telegram. If the Multiplex Bits are 11_{Bin} then the input bits DI0, DI1 are transferred to the master and the master sends the output bits DO0, DO1 in the following data telegram.

For transmission security a client / server structure is required. The AS-i slave acts as the server and provides the Input Multiplex Bits. The AS-i master acts as the client and reflects the inverted Input Multiplex Bit DO2 to acknowledge the data transfer. With the data bit DO0 and DO1 the master transfers the corresponding output bits.

The Multiplex Bits 00_{Bin} denote the start of a transfer sequence. If consistent data output is required the master shall update the output byte only before sending output bits DO6, DO7.

To ensure that all groups of data are refreshed continuously the alternation of the D2 bit shall be supervised by the slave and the master. If there is no alternation of the D2 bit at least every 300 ms (after the activation of the slave) the slave shall stop communication and switch all outputs into the OFF-state (protocol-watchdog). In this case, the master shall signal the invalidity of the input data to the controller with a "Valid Bit" set to 0.

NOTE In the case of a protocol watchdog event, it is recommended to stop communication.

The AS-i parameter bits (Single transaction „Write_Parameter“) are not used for combined transaction type 3. They may be defined in the respective slave profiles.

The data is transferred to the AIDI (high byte of channel 0 for Slave A and high byte of channel 2 for Slave B) and from the AODI of the master.

5.7.4.2.2 Response times

The slave starts a sequence of data transmission by sending "0 0 DI7 DI6". After receiving this information, the master shall respond in less than 10 ms with an inverted DO2 bit. The slave shall respond to the changed DO2 bit with new data within 250 µs. The sequence then continues until DO1 and DO0 has been sent and the cycle repeats. This ensures that maximum data transfer times can be calculated.

5.7.4.2.3 Exception handling

5.7.4.2.3.1 Power-up

The user data in the master are marked as invalid until a complete and error-free data transfer has been performed.

5.7.4.2.3.2 Interruption of data traffic

When a master with integrated support of combined transaction type 3 detects that a slave of a corresponding profile is not in the LAS anymore, it marks the corresponding input values of all channels of this slave as invalid and sets them to default values if applicable.

If the master detects a wrong sequence or no change of the input multiplex bits, it shall stop reflecting the inverted DI2 bit and transmit "011_{Bin}" at ASI-level. All input bits and the valid bit shall be set to 0.

5.7.5 Combined transaction type 4

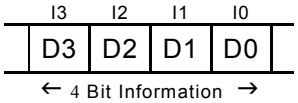
The combined transaction type 4 mechanism is handled according to the specification given below. It uses the standard AS-i data transfer mechanisms to build a single or dual channel

16 bit data transfer channel from the slave to the master in extended address mode with the profiles given in Table 8.

NOTE Combined transaction type 4 is intended for use in single or dual channel 16 bit sensors; replacement for 4 mA to 20 mA interfaces.

5.7.5.1 Definition of data and parameter bits

The definition of the I/O data bits (Single transaction “Data_Exchange”) for the data transfer is given in Figure 45:



Bit	Type	Definition
D3	I	Data bit DI3, DI7, DI11, DI15
D2	I	Data bit DI2, DI6, DI10, DI14
D1	I	Data bit DI1, DI5, DI9, DI13
D0	I	Data bit DI0, DI4, DI8, DI12
D3	O	Select bit
D2	O	Channel select bit (Profile S-7.A.9 only)
D1	O	Nibble select bit 1
D0	O	Nibble select bit 0

Figure 45 – Definition of the I/O data bits in combined transaction type 4

The 16 input bits are transferred cyclically in 4 groups of 4 data bits each. Each group is addressed with the Nibble Select Bits DO1 and DO0 by the master. If the Nibble Select Bits are 00_{Bin} then the input bits DI12 to DI15 are transferred to the master. If the Multiplex Bits are 01_{Bin} then the input bits DI8 to DI11 are transferred to the master. If the Nibble Select Bits are 10_{Bin} then the input bits DI4 to DI7 are transferred to the master. If the Multiplex Bits are 11_{Bin} then the input bits DI0 to DI3 are transferred to the master.

If only 12 bits are to be transferred the Multiplex Bit combination 11_{Bin} may be omitted by the master in order to speed up the net data transfer. If only 8 bits are to be transferred the Multiplex Bit combinations 11_{Bin} and 10_{Bin} may be omitted.

The AS-i parameter bits (Single transaction „Write_Parameter“) are not used for combined transaction type 4. They may be defined in the respective slave profiles.

The cyclic input data of an A-Slave is copied into channel 0 and 1 of the AIDI of the corresponding slave address. The cyclic input data of a B-Slave is copied into channel 2 and 3. In case of single byte data, the high byte of the AIDI is used.

5.7.5.2 Data transfer

The request with the Nibble select bits set to 00_{Bin} also serves as "latch“ command. After having received this command the data bits of the whole sequence shall not be updated by the data source until completion of the whole sequence. This ensures data consistency.

5.7.5.3 Slave response times

When the master transmits a new select information the slave shall respond with the requested information in the same telegram. This ensures that maximum data transfer times can be calculated.

5.7.5.4 Exception handling

5.7.5.4.1 Power-up

The user data in the master are marked as invalid until a complete and error-free data transfer has been performed.

5.7.5.4.2 Interruption of data traffic

When a master with integrated support of combined transaction type 4 detects that a slave of a corresponding profile does not provide consistent data or is not in the LAS anymore, it marks the corresponding input values of all channels of this slave as invalid and sets them to default values if applicable.

A slave that supports combined transaction type 4 shall implement a watchdog function to monitor interruptions of data traffic after the activation of the slave. In case of interruption of data transfer detected by the watchdog the following action shall be taken:

– the slave resets its state machine, that means it does not respond any more to data telegrams until it receives a new parameter telegram from the AS-i master.

5.7.6 Combined transaction type 5

The combined transaction type 5 mechanism is handled according to the specification given below. It uses the standard AS-i data transfer mechanisms to build a fast 8, 12 or 16 bit full duplex data transfer channel from the master to the slave using 2, 3 or 4 standard addresses with the profiles given in Table 8.

NOTE 1 Combined transaction type 5 is intended for use in high speed 16 bit sensors, actuators and field devices; replacement for 4 mA to 20 mA interfaces for control loops.

A slave supporting combined transaction type 5 may be seen as one "physical slave". This slave occupies the lowest address of a group of 2, 3 or 4 consecutive addresses. The next 1, 2 or 3 addresses in ascending order shall not be used by any other "physical slave" as they are also occupied by the physical slave supporting this transaction type.

NOTE 2 Changing the address of a slave of this type may not function the same way as with other slaves. In particular, the auto-address assignment (see 5.6.5.4) will need special attention of the user as this edition of the standard does not contain auto-addressing procedures for slaves supporting transaction type 5.

5.7.6.1 Definition of number of channels

The number of data channels and the type of data is defined by the extended ID2 code (Single transaction “Read_ID2-Code”) stored in the slave (see Annex A for details). The following definitions apply:

Table 13 – Definition of the ID2 code in combined transaction type 5

$ID2_{Hex}$	I3	I2	I1	I0	Definition
2	0	0	1	0	Lowest address of an 8 bit transparent slave
3	0	0	1	1	Lowest address of a 12 bit transparent slave
4	0	1	0	0	Lowest address of a 16 bit transparent slave
5	0	1	0	1	Highest address of a group of slaves of combined transaction type 5
6	0	1	1	0	Second address of a 12 bit slave, third address of a 16 bit slave
7	0	1	1	1	Second address of a 16 bit slave
A	1	0	1	0	Lowest address of an 8 bit analogue slave
B	1	0	1	1	Lowest address of a 12 bit analogue slave
C	1	1	0	0	Lowest address of a 16 bit analogue slave

5.7.6.2 Definition of I/O data and parameter bits

There is no specific definition of the I/O data bits (Single transaction “Data_Exchange”) and for the parameter bits (Single transaction "Write_Parameter") for the data transfer according to this combined transaction type.

The data bits of the slave with the lowest address are the data bits D0 to D3, the data bits of the slave with the highest address are the data bits D12 to D15. If only 12 bits are to be transmitted according to this combined transaction type the highest address may be omitted. If only 8 bits are to be transmitted the highest two addresses may be omitted.

The AS-i parameter bits (Single transaction „Write_Parameter“) are not used for combined transaction type 5. They may be defined in the respective slave profiles.

5.7.6.3 Data transfer

Master and slave shall keep the data to be transmitted consistent for all addresses that take part in combined transaction type 5 during one AS-i cycle.

Data is transferred from the AODI and to the AIDI of the slave with the lowest address.

The slaves shall only accept output data if the data for all addresses that take part in combined transaction type 5 was received successfully.

The master shall only accept input data and copy it into the analogue input data image (AIDI) if the data from all addresses that take part in combined transaction type 5 were received successfully.

5.7.6.4 Slave response times

When the master transmits an output information the slave shall respond with the respective input information in the same telegram. This ensures that maximum data transfer times can be calculated.

5.7.6.5 Exception handling

5.7.6.5.1 Configuration error

If the slave addresses that take part in combined transaction type 5 are not configured in the way defined above, the master shall treat each slave address as binary slave. Output data is then taken from the ODI, input data is transferred to the IDI. The analogue input data image (AIDI) is set to 0000_{Hex} in case of a transparent slave or to $7FFF_{Hex}$ in all other cases. Additionally, the master's valid bit is reset for this channel.

5.7.6.5.2 Power-up

The slave shall only start to answer master requests for data exchange until it can provide consistent data. If this is not possible (e.g. for timing reasons) the slave may provide default values.

Slave and master shall only update their received data after they have successfully received a complete data sequence for all addresses that take part in combined transaction type 5.

5.7.6.5.3 Master time-out

If the master does not receive valid data for all addresses that take part in combined transaction type 5, it shall keep the last valid value.

If no new valid value is received for more than 20 ms, the master may set the default value in the AIDI and reset the valid bit. If no new valid value is received for more than 100 ms, the master shall set the default value in the AIDI and reset the valid bit.

5.7.6.5.4 Slave time-out

If the slave does not receive

– valid data for all addresses taking part in combined transaction type 5 within one cycle, or

– valid data with less than 380 µs time between two consecutive addresses

it shall keep the last valid value.

If no new valid value was received for more than 40 ms, the slave may set a fail safe value to its output. If no new valid value was received for more than 100 ms, the slave shall set a fail safe value to its output. The fail safe value (e.g. minimum output, last value or maximum output) shall be stated in the manufacturer's documentation.

5.7.7 Combined transaction for safety related signal transfer

The combined transaction for safety related signal transfer mechanism is handled according to the specification given below. It uses the standard AS-i data transfer mechanisms to build a single bit or two bit (depending on required safety integrity) safety related information channel between safety slaves with the profiles given in Table 8 and a safety control unit.

Safety related signal transfer and standard data transfer may be handled on the same network. The safety relevant information consists of one or two bits per slave only (e.g. the output of a safety light barrier, the contact of an emergency stop device). A coding unit is placed between the sensor and the transmission system which transforms the net information into a sequence of 8 sets of 4 bits of information ("dynamic coding"). On the receiver side, a safety related control unit interprets the signal. It compares the received codes with internally stored reference codes and from this, the state of the slave and the transmission system can be derived. The safety related control unit may be a part of the master; alternatively it may be a separate device, called "Safety monitor“.

NOTE 1 At present, only the safety related signal transfer from a slave to the safety related control unit is realized.

NOTE 2 Reference to IEC 61508 for safety product standards or common reference to safety relevant standards should be taken into account when using safe signal transfer on AS-i.

5.7.7.1 Safety related input slaves

If a safety related input slave has two switching states, these states directly control the 4 bits of information transferred from the slave to the master. If the input of the slave is in "ON"-state (e.g. the light path of a safety light curtain is free, a safety door is closed) this state is signalled by transmitting a sequence of 8 sets of 4 bits of information. Every AS-i cycle transfers the next set of 4 bits of information. If 8 cycles have been transmitted the complete sequence has been sent. In the 9^{th} cycle the first set is transferred again. If the input of the slave is in "OFF"-state the information "0_{Hex}" is sent.

If a safety related input slave has two inputs (e.g. redundant contacts) each of the two contacts act independently of each other on two bits of the 4 bits of information. The Table 14 shows the 4 possible states of the inputs:

Table 14 – Input states of safety related input slaves

Contact 1	Contact 2	Data D0..D3	Meaning
ON	ON	X X X X	Input in "ON"-state
ON	OFF	X X 0 0	Input in "OFF"-state, only one contact is open
OFF	ON	0 0 X X	Input in "OFF"-state, only one contact is open
OFF	OFF	0 0 0 0	Input in "OFF"-state, both contacts open
NOTE "X" means bit value from code sequence.			

The data channel from the safety related input slave to the safety control unit is permanently supervised by the dynamic coding technique. It has to be ensured by design of the slave that the requirements of IEC 61508 are fulfilled.

Only slaves with standard addressing mode shall be used as safety related input slaves.

5.7.7.2 Coding rules

The data bits D0...D3 in the slave answer form a code nibble. 8 code nibbles form a code sequence.

Rules for the assembly of a code sequence:

S1: A sequence consists of eight 4-bit-values where each code nibble is different from each other.
S2: The values 0000_{Bin} and 1111_{Bin} do not exist within a sequence
S3: Exactly one value of 0001_{Bin}, 0010_{Bin} or 0011_{Bin} exists in a sequence.
S4: Exactly one value of 0100_{Bin}, 1000_{Bin} or 1100_{Bin} exists in a sequence.
S5: Between two values with only 1 bit set are at least 2 values with two or three bits set.
S6: The value 0000_{Bin} indicates the OFF-state of the sensor.
S7: The value 1111_{Bin} is reserved for future extensions.
S8: The stepping of the sequence is delayed by 200 – 900 µs after a data-request.

Following the rules S1 and S2 results in further requirements.

SA1: In all 8 code nibbles of the sequence a data bit is never constant 0 or 1.
SA2: In all 8 code nibbles of the sequence two data bits are never completely equal.

The series of code nibbles is stored permanently in the slave or in an associated external device (e.g. light sender).

NOTE 200 µs to 900 µs after the reception of a data request from the master, the slave should switch from one code nibble to the next. The minimum delay time of 200 µs is intended to allow for a single repetition of a data exchange if the slave answer was not received correctly by the master. The safety related control unit needs 6 AS-i-telegrams (900 µs (5 slaves + management_phase)) at minimum for internal processing. These 900 µs are supervised by the safety related control unit and can otherwise be used inside the safety related slave to handle critical timing conditions.

Within an AS-i network only different code-sequences are allowed.

Following these rules more than 900 000 different code-sequences are available. The correctness of the code sequence shall be supervised by the safety related control unit.

5.8 AS-i error detection

Any master request and slave response on the AS-i line shall be checked by the receivers in the slave or in the master respectively for the following possible transmission errors:

Start_bit_error The initial pulse following a pause shall be of negative polarity. This pulse is the reference for bit decoding. The first bit detected shall be of the value 0. Violation of this rule shall be detected as start_bit_error.

Alternating_error Two consecutive pulses shall be of different polarity. A negative pulse shall be followed by a positive pulse and vice versa. Violation of this rule shall be detected as alternating_error.

No_information_error Within any request or response, pulses (of positive or negative polarity) shall be detected in periods of $(n * 3\mu s)^{+1,0\mu s}_{-0,5\mu s}$ after the initial pulse of a request or response, where n = 1 ... 26 for a master request and n = 1 ... 12 for a slave response. Violation of this rule shall be detected as no_information_error.

Parity_error The sum of all information bits of the request or response (excluding start and end bits, including parity bit) shall be even. Violation of this rule shall be detected as parity_error.

End_bit_error The pulse to be detected n * 6 μs after the start pulse shall be of positive polarity, where n = 13 (78 μs) for a master request and n = 6 (36 μs) for a slave response. This stop pulse shall finish the request or response. Violation of this rule shall be detected as a end_bit_error.

Length_error A length supervision shall be processed. If during the first bit time after the end pulse of a master request (equivalent to the 15th Bit time) for synchronised slaves (during the first three bit times for not synchronised slaves, equivalent to the Bit times 15 to 17) or during the first bit time after the end pulse of a slave response (equivalent to the 8th Bit time) a signal different from a pause is detected, a Length_error shall be detected.

If at least one of these errors occurs, the request or response shall be handled as invalid.

The master shall be able to detect and handle the following communication errors:

– Missing slave response
– Error in slave response

For details see 8.5.

Any slave shall be able to detect and handle the following communication errors:

Error in master request

For details see 8.4.

6 Product information

6.1 Instructions for installation, operation and maintenance

Subclause 6.1 of IEC 62026-1 applies.

6.2 Profiles

Subclause 6.2 of IEC 62026-1 applies with the following additions.

All AS-i components shall be marked with, or shall include in the components instructions for operation, identification of the profile(s) supported.

Masters and slaves shall carry the markings specified in the appropriate annex.

Markings shall be indelible and easily readable, and shall not be placed on parts normally removable in service.

6.3 Marking

Subclause 6.3 of IEC 62026-1 applies with the following additions.

6.3.1 Basic rated values

Manufacturers shall state the current ratings.

6.3.2 Connection and wiring identification

Table 15 defines the connection and wiring identification.

Table 15 – Connection and wiring identification

Physical interface	Type	Function	Wire colour	Terminal number
B,C,E	AS-i line	AS-i (+) AS-i (–)	Brown Blue	1 3
A	INPUT port (with connectors according to Annex D of IEC 60947-5-2)	Power supply (+) Input data 1 Power supply (–) Input data 2	a	1 2 [b] 3 4 [b]
A	INPUT port solid state (with terminals)	Power supply (+) (4x) Input data (4x) Power supply (–) (4x)		11…41 12/14…42/44 13…43
A	OUTPUT port solid state (with connectors according to Annex D of IEC 60947-5-2)	Power supply (+) (npn) (4x) Power supply (–) (pnp) (4x) Output, parameter, etc. (4x)		1 3 4
A	OUTPUT port relays	Change-over contact Normally closed contact (NC) Normally open contact (NO)		1 2 4
A	OUTPUT port solid state (with terminals)	Power supply (+) (npn) (4x) Power supply (–) (pnp) (4x) Output data bit (4x)		11…41 13…43 14…44
F	Auxiliary power port	Aux. power (+) Aux. power (–)	Brown Blue	1 3
B+F	AS-i line + auxiliary power port [c]	AS-i (+) AS-i (-) U_{aux} (+) (-) PE [d]	Brown Blue Black White Green/Yel-low	1 3 4 2 5

[a] Wire colours for proximity switches shall conform to Table 3 of IEC 60947-5-2.

[b] When only one INPUT pin per connector is used, the connector pins 2 and 4 shall be bridged internally.

[c] When the same connector or cable is used for both voltages, the auxiliary power supply shall be of the SELV or PELV type.

[d] If used.

6.3.3 AS-i standard cable

The AS-i standard cable shall be coloured yellow and the "+" and "−" conductors shall be clearly identified. If colours are used for identification they shall be: brown = + and blue = −.

6.3.4 AS-i power supply

The connections of an AS-i power supply shall be as defined in Table 16 if it is a single phase a.c. power supply. This marking is mandatory.

Table 16 – AS-i power supply marking

Power supply sides	Marking	Specification
Primary	L	Phase
	N	Neutral
	PE	protective earth
Secondary (Interface E)	ASI+	AS-i line positive
	ASI−	AS-i line negative
	GND	Equipment earth and/or shield

6.3.5 AS-i slave

The IP protection rating of the slave shall be stated in the documentation according to Annex C of IEC 60947-1.

6.3.6 AS-i master

The type of isolation between AS-i ports at the master and the controller shall be stated by the manufacturer.

7 Normal service, mounting and transport conditions

7.1 Normal service conditions

Subclause 7.2 of IEC 62026-1 applies with the following additions.

7.1.1 Ambient air temperature

AS-i components shall operate between the ambient temperatures of –5 °C to +40 °C if not otherwise specified, for example in conjunction with a specific actuator or sensor type. The operating characteristics shall be maintained over the permissible range of ambient temperatures.

7.1.2 Altitude

Subclause 6.1.2 of IEC 60947-1 applies.

7.2 Conditions during transport and storage

A special agreement shall be made between the user and the manufacturer if the conditions during transport and storage, for example temperature and humidity conditions, differ from those defined in 7.1 except that unless otherwise specified, the following temperature range applies during transport and storage: between –25 °C and +55 °C and, for short periods not exceeding 24 h, up to +70 °C.

7.3 Mounting

Mounting dimensions and conditions of the AS-i components shall be specified in the other parts of this standard or if not specified shall be stated in the manufacturer's documentation.

8 Constructional and performance requirements

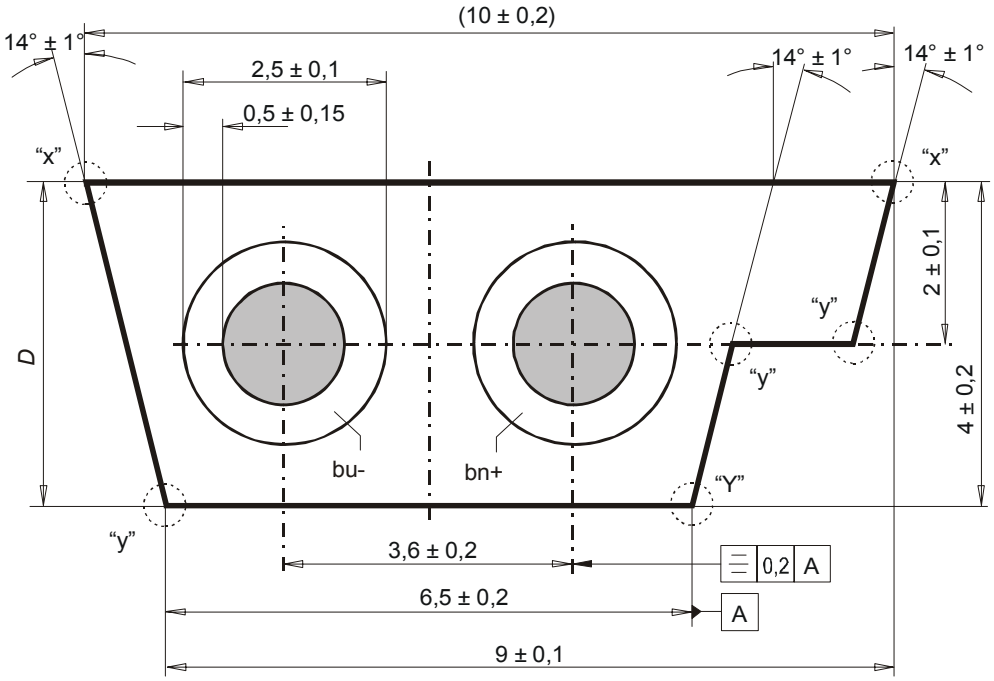
8.1 AS-i transmission medium

The AS-i transmission medium shall meet the requirements given in 5.4.1. Additionally, the following constructional and performance requirements apply as specified or are recommended.

8.1.1 AS-i standard cable

For easy and quick field installation the use of an insulation piercing connection (IEC 60352-6) is recommended. It depends on the AS-i standard cable. Its inner and outer geometrical dimensions are shown in Figure 46.

Dimensions in millimetres



"x": R = max. 0,2; "y": R = max. 0,5

Figure 46– AS-i standard cable for field installation

The AS-i standard cable for field installation shall meet the following technical requirements:

- conductor cross-section: $2 \times 1{,}5\ mm^2$
- conductor resistance: 13,7 Ω/km according to IEC 60227-2
- insulation resistance of cores: $= 10^{11}\ \Omega * cm$ according to IEC 60227-2
- temperature range: −25 °C to +85 °C (fixed installation)
  −10 °C to +85 °C (flexible installation)

– conductor structure:	extra finely stranded according to IEC 60228, class 6. Strands have to be tinned
– turn of the strands	= 20 mm to 40 mm
– bending radius (in y-direction)	minimum 3 × D = 12 mm (fixed installation) minimum 6 × D = 24 mm (flexible installation)
– internal friction	the conductor insulation shall not be glued with the cable sheath
– hardness of insulation material	cable sheath: max. 90 Shore A; the hardness of the conductor insulation shall not exceed the cable sheath hardness
– flammability	Method FH, cat. FH 2-25
– rated voltage:	300 V
– insulation test voltage:	1,5 kV
– colour of cable sheath:	similar to yellow RAL 1012 according to IEC 60304
– chemical resistance	as per manufacturer's technical data
– marking:	the + and − conductors shall be clearly marked.

If colours are used, they have to indicate:

brown = +
blue = −

8.1.2 AS-i cabinet cable

For easy and quick installation in IP20 environments (e.g. inside switching cabinets) the use of an insulation penetrating connection (IEC 60352-6) is recommended. It depends on the AS-i standard cable shown in Figure 47.

Dimensions in millimetres

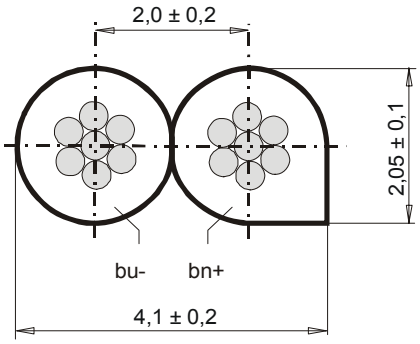


Figure 47 – AS-i cabinet cable

The AS-i standard cable for IP20 environments shall meet the following technical requirements:

– conductor cross-section:	2 × 0,8 mm^2 (AWG 18)
– conductor resistance:	= 22,5 Ω/km according to IEC 60227-2
– insulation resistance of cores:	= 10^{11} Ω∗cm according to IEC 60227-2
– temperature range:	−5 °C to +80 °C
– conductor structure:	two stranded tinned copper wires 7x0,4 side by side
– turn of the strands	= 20 mm to 40 mm
– hardness of insulation material	max. 90 Shore A;
– rated voltage:	300 V

- insulation test voltage: 1,5 kV
- chemical resistance as per manufacturer's technical data
- marking: the + and − conductors shall be clearly marked.

If colours are used, they have to indicate:

brown = +
blue = −

8.1.3 Auxiliary power supply

AS-i slaves may be powered with auxiliary power (see 8.4.4.9). If, for this purpose, a flat cable similar to the AS-i standard cable according to 8.1.1 is used, it shall have the following different requirements:

- operating voltage: ≤ 30 V d.c.
- colour of cable sheath: similar to black RAL 9005 according to IEC 60304.

8.1.4 Contacting the AS-i line

Any contacts between parts of an AS-i line shall meet the following requirements, independent of whether a conventional technology or an insulation piercing or penetrating technology is used:

- contacting cycles min. 5 times (if connections are detachable)
- protection class according to IEC 60529 as per manufacturers technical data
- contact resistance max. 6 mΩ according to IEC 60352-6
- min. allowable current per connection as per manufacturer's technical data
- rated voltage 10 V to 48 V d.c.
- temperature range –25 °C to +70 °C
- shock according to IEC 60068-2-27
- vibration according to IEC 60068-2-6
- strain relief according to IEC 60947-5-2, Annex C

8.1.5 Pinning of M12 and M8 connectors

If M12 (4-pin) or M8 (3-pin) plugs and sockets, according to IEC 60947-5-2, Annex D, are used for the interconnection of the AS-i line or of auxiliary power lines, the following rules shall apply:

NOTE See Slave Profiles in Annex A for the interconnection of peripheral elements to slaves.

If a 12 mm or 8 mm plug is used for the interconnection of the AS-i line only, the plug shall be male for energy input and female for energy output with the following pinning:

- pin 1 = ASI+
- pin 2 not used (not available for 8 mm connector)
- pin 3 = ASI-
- pin 4 not used

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary power only, the plug shall be male for energy input and female for energy output with the following pinning:

- pin 1 = (+) auxiliary power
- pin 2 not used (not available for 8mm connector)

– pin 3 = (−) auxiliary power

– pin 4 not used

If a 12 mm plug is used for both the interconnection of the AS-i line and the interconnection of the auxiliary energy, the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = ASI+

– pin 2 = (−) auxiliary power

– pin 3 = ASI-

– pin 4 = (+) auxiliary power

8.1.6 Profiles and electromechanical interface

Within this standard no further restrictions for the method of interfacing the AS-i line with different components are defined, beside the ones stated in 8.1.4. All sensors, actuators, or other devices and elements, that only meet the mentioned restrictions in contacting the AS-i system, are declared as conform with an electromechanical profile.

8.2 AS-i power supply

The AS-i power supply and decoupling network shall fulfil the requirements given in 5.3.2. Additionally, the constructional and performance requirements given below apply.

8.2.1 Environmental conditions and electromagnetic compatibility

The protection class according to IEC 61140 of the system demands a power supply delivering protective extra low voltage (PELV). All necessary tests concerning the power line side will be declared by the manufacturer in accordance with the designated operation conditions.

The function of the power supply shall not be impaired by the data transmission on the AS-i network.

Table 17 – Environmental conditions (minimum conditions)

Protection class	III (PELV)
EMC-burst	IEC 61000-4-4: normal function (see 9.3)

For normal function of all components in an AS-i-system the voltage measured at the terminals of the power supply shall be between 29,5 V and 31,6 V. Therefore, the voltage produced by the power supply during the burst period shall be kept within this range to reach performance criteria A and B (see also 9.3).

The electrical isolation of the AS-i line from machine ground causes the need to prevent static electricity. It is mandatory to use the ground connection (see Figure 48).

The AS-i power supply shall be installed in such a way that it is not subject to line surges on the output side.

8.2.2 Start-up, overload and indication

The power supply shall be protected against short circuit and overload. A short circuit or overload condition may last for infinite time and shall not damage the power supply. After removing the overload the AS-i power may come back automatically.

Optionally the overload condition may be indicated. If used, either the undervoltage/ overcurrent condition shall be indicated by a red LED or the power ready LED (green) shall not light up.

After the start-up time has elapsed an overload condition is detected when either the AS-i voltage level does not reach the low-limit value or the load current exceeds the current limit

$$U_{ASI} < U_{ASI\ min} \qquad \text{or} \qquad I_L > I_{LIM}.$$

Within 2 s after reaching 5 V the first time the voltage level shall reach the maximum value of the master starting voltage (26,5 V). The time interval between the minimum master starting voltage (22,5 V − 1 V, see 8.5) and the rated AS-i voltage level (29,5 V) shall be less than 1 s. The voltage level has to increase steadily from 5 V up to normal operation voltage (29,5 V to 31,6 V).

NOTE 1 The second demand is important because the master begins to work if the voltage exceeds its starting voltage of 22,5 V ± 1 V.

During start-up the power supply shall supply an increased current to meet the charging process in the system. This additional load will be equal to a capacitance of 15 mF.

NOTE 2 For every connected slave a maximum capacitance of 470 µF is assumed (31 × 470 µF ≈ 15 mF). If extended addressing is used a maximum capacitance of 240 µF for each slave is assumed (62 × 240 µF ≈ 15 mF). Concerning the data exchange all these capacitors are individually choked in the respective slaves.

Beginning from a voltage level of 5 V the power supply shall give the rated output current I_e plus an additional current to load the above-mentioned capacitance of 15 mF to meet the time restrictions.

The rated output current I_e and the current limit shall be stated by the manufacturer.

8.2.3 Ports, voltages and currents

The terminal connectors of ASI+, ASI- and ground shall be able to contact conductor cross-sections of 0,75 mm^2 to 2,5 mm^2.

Table 18 – General requirements for an AS-i power supply

Line voltage level	U_N
Voltage lower limit	U_{Nmin}
Line voltage, tolerances (and frequency)	According to designated operation conditions
Power interrupts	Interrupts of power on the primary side as long as 10ms in the state of permanent low limit voltage U_{Nmin} (= U_N-15%) shall not impair normal function of the supply.
Protection class	3 (protective extra low voltage)
NOTE No influence means that the voltage between ASI+/ASI− never lies outside the range of 29,5 V to 31,6 V.	

8.2.4 Symmetrization and decoupling circuit

The equivalent symmetrization and decoupling network consists of two inductances and two resistors as well as the symmetry capacitors C_s as shown in Figure 48.

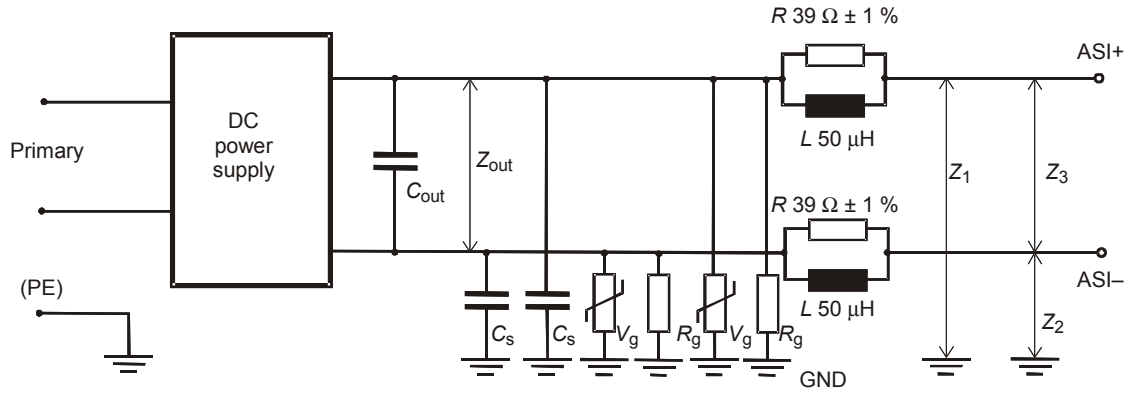


Figure 48 – Equivalent schematic of decoupling circuit

The symmetry capacitors C_s shall be located as close as possible to the decoupling circuit. These capacitances ensure the symmetry of ASI+/ASI- to ground. Equal values of at least 100 nF are recommended.

NOTE 1 It is recommended to also provide resistors R_g (recommended value 1 MΩ) and varistors V_g to ground in order to prevent static voltage build-up.

Even though it is possible to design the circuit as shown in Figure 48, the symmetry requirements can better be met by the use of a transformer. The decoupling circuit using a transformer is shown in Figure 49.

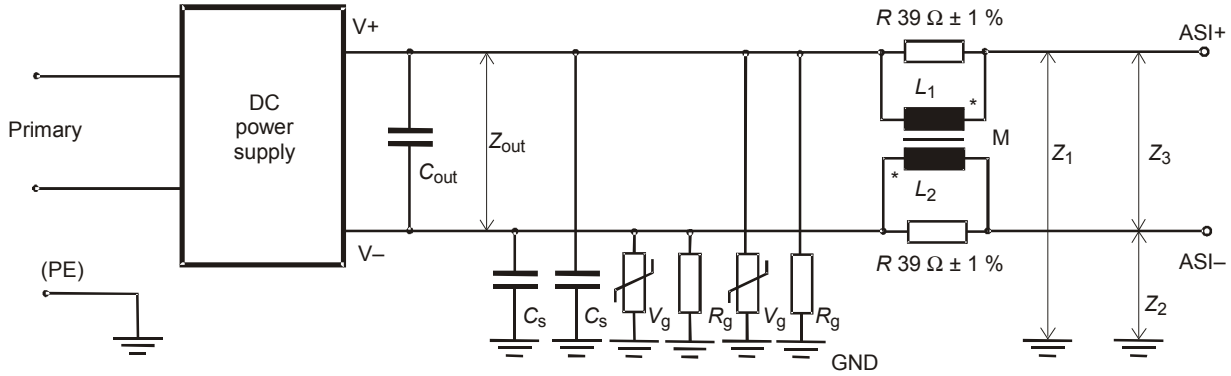


Figure 49 – Decoupling circuit using a transformer

The two inductances shall be designed as bifilar but not flux-compensating windings on a common core.

NOTE 2 AS-i has been designed as a symmetrical system. The better the symmetry, the better the rejection of undesirable emission of AS-i signal components as well as incidence of AS-i relevant noise, even if the system is relatively large and distributed. This is important because the network is unshielded and may act as an antenna.

8.3 AS-i repeater and other components

8.3.1 AS-i repeater

The AS-i repeater shall regenerate (not only amplify) and transfer the AS-i signals bi-directionally.

The maximum signal delay time of a repeater shall be less than or equal to 7 µs for each direction.

The repeater shall provide galvanic separation between the two parts of the AS-i network. The minimum test voltage shall be stated by the manufacturer.

8.3.2 AS-i earth fault detector

The AS-i earth fault detector's supply voltage range shall be stated by the manufacturer. It is recommended to specify a supply voltage range between 26,5 V and 31,6 V. If the AS-i earth fault detector uses an auxiliary voltage, it shall fulfil the same requirements as an AS-i slave which is powered by an auxiliary voltage.

The current consumption of the AS-i earth fault detector has to be stated in the manufacturer's documentation. The equivalent impedance and the symmetry shall be within the same limits that are given for an AS-i standard slave.

The manufacturer shall declare the impedance range that can be detected by the earth fault detector between ASI+ and Ground and ASI- and Ground. It shall be compatible with the requirements for the detection of an earth fault according to IEC 60204-1.

The manufacturer shall declare the maximum response time between the earth fault event and the switching of the output of the earth fault detector.

8.4 AS-i slave

8.4.1 Overview

The AS-i slave provides all physical and logical means to connect the application (actuator, sensor, or any other devices and elements) to the AS-i line and to receive and send the messages on the AS-i line as described in Clause 5.

Subclause 8.4 describes the elements of a slave, its function and the general requirements of a slave.

8.4.2 Elements of a slave

8.4.2.1 Slave port

The slave shall have at least two physical ports ASI+ and ASI−, i.e. to interface 2, to connect the slave to the AS-i line.

Other ports form the interface 1 to the electronic device that communicates with the controller may be physically realized within an electronic circuit and thus be accessible by simple physical means ('physical ports'). But these ports may also be hidden, for example within a joint integrated circuit for the AS-i slave and the connected device. In this case, the ports are called 'logical' and the interface 1 shall not be accessible by physical means. Both, physical and logical ports may be mandatory or optional according to Table 19.

Table 19 – Physical and logical ports of an AS-i slave

	Physical ports	Logical ports
ASI±	m	-
D0 – D3	o	m
P0 – P3	o	m
Data strobe	o	o
Parameter strobe	o	o
RESET	o	-
Power supply	o	-
Others	o	o

If they exist, the ports have the following functions:

ASI+/ASI- These ports form the electrical connection to the AS-i network to interface 2. They are mandatory. For details of signals and electromechanics see Clause 5.

D0 ... D3 These ports shall be configured as data input or output or bidirectional ports as described in 8.4.2.2.

Data: If data input/output ports are implemented, the four Information bits I0 ... I3 data of a message (as described in 5.6.5.) correspond to the levels of the data input/output ports. An input signal with a HIGH level at the port Dx shall lead to a “1” of the corresponding data bit Ix in the information element of the slave response, a LOW level to a “0”. A “1” in a data bit I0 to I3 in the information element of a master request shall lead to a HIGH level at the corresponding output port, a “0” to a LOW level.

NOTE 1 Output ports shall have a HIGH level as default values (e.g. after power on or after a reset). Output levels are inverted in AS-i master.

Bidirectional ports: If data input/output ports are implemented and if they can be used for bidirectional transmission of data, first output data and then input data shall be transmitted. The typical timing of the signals is shown in Figure 50.

Typical times in µs

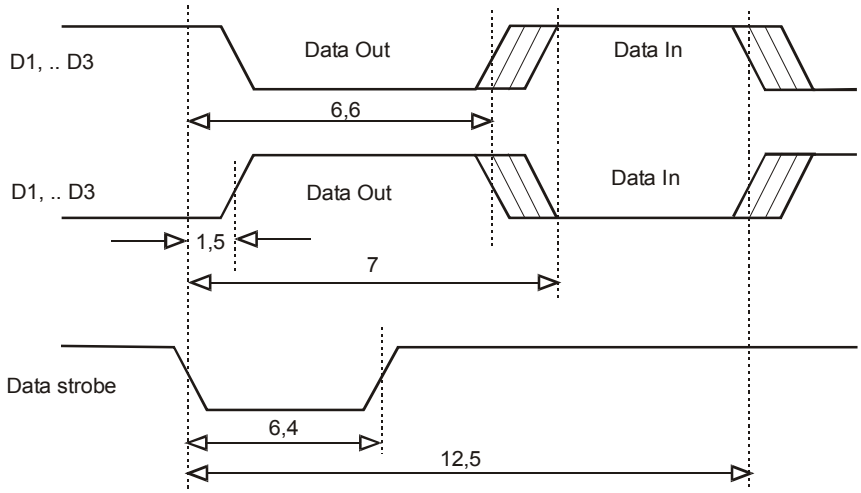


Figure 50 – Typical timing diagram for bidirectional input/outputs (D1, .. D3 = voltage level at respective data port)

P0 ... P3: If parameter output ports P0 ... P3 are implemented, the parameter output data of the master request (as described in 5.6.5.2) correspond to the level of the parameter output ports. A “1” in a parameter bit Ix in the information element of the master request "Write_parameter” shall lead to a HIGH level at the corresponding parameter output port Px, a “0” to LOW level. A HIGH level at a port Px shall be reflected by a “1”' of the corresponding data bit Ix in the information element of the slave response, a LOW level by a “0”.

NOTE 2 Parameter ports should have a HIGH level as default values after power on or after a reset.

RESET port to perform a reset of the slave externally

Data strobe: data valid signalling

Parameter strobe: parameter valid signalling

Power supply: supplying the connected application device with energy from the AS-i line

8.4.2.2 I/O configuration, ID codes and slave profiles

Each slave shall have mandatorily an I/O configuration, an identification code (ID code) and optionally two extended identification codes (ID1 and ID2 codes) for further distinction of slaves with the same I/O configuration. Either both, ID1 and ID2, shall be implemented or none of them. Each of the three identification codes (ID, ID1 and ID2) shall have 4 bits (16 different possibilities). If implemented they shall be readable by the master. The values of ID and ID2 for a particular slave depend on the implementation. Therefore, they are stored in the slave by the manufacturer and shall not be changeable by any means.

The value of ID1 may be set by the user of the system with the command Write_Extended_ID-Code_1. It shall also be stored non-volatile.

In extended address mode (ID_Code = A_{Hex}) it is allowed for the manufacturer to block the write access by the user to the Extended_ID_Code_1.

The combination of the I/O configuration and the identification codes ID and ID2 of a particular slave characterises its “slave profile” (Annex A). Any slave that does not represent a specific slave profile exactly, shall have the ID-code E_{Hex} or F_{Hex} (free profiles, see Annex A).

Upon delivery of the product the manufacturer shall set the extended identification code to ID1 = F_{Hex} (standard addressing mode) or to ID1 =7_{Hex} (extended addressing mode), respectively. In case of a blocked ID1 the manufacturer shall set the ID1 to the value which is defined in the Slave Profiles (Annex A).

The manufacturer shall state the actual slave's profile in the product documentation in the form S - [I/O-code].[ID-code].[ID2-code].

NOTE 1 The definition of slave profiles has the goal to increase the interchangeability of actuators and sensors on the one hand, and - with free profiles - to ensure a high degree of flexibility of the system on the other hand.

NOTE 2 The profiles S - 0.A ... S - E.A are used for the extended address mode.

NOTE 3 The profile of slaves which have not implemented the optional extended ID codes ID1/2 may be designated in the form S - [I/O-code].[ID-code] instead of S - [I/O-code].[ID-code].F

NOTE 4 The blocking of the ID_Code_1 in extended address mode allows more specific products to be identified by the mechanism of reading the I/O Configuration and the ID_Codes.

8.4.2.3 Non-volatile memory

A non-volatile memory of the slave shall contain the I/O configuration and the ID codes.

A non-volatile memory shall also contain the slave address. It may be realized as an electronic memory, by switches, or by fixed assignments.

The address shall be readable and loadable into the address register of the slave. Changing of the address shall be possible at least 10 times.

In case of manual or fixed assignment of the slave address, the zero address shall not be selectable.

The address shall be stored in a way that any other address beside the address intended to be stored can never occur as proper address of the slave. For interrupted address assignment either the old or zero-address will be allowed.

8.4.2.4 Registers and flags

The slave shall have the following internal registers and flags. These are volatile memories, their contents will be lost in case of a power failure.

address register (5 bits): contains the address of the slave

I/O_Code register (4 bits): contains the information which data port is configured as output, input, bi-directional I/O, or as tristate

ID_Code register (4 bits): contains the ID code of the slave

extended ID_Code register (8 bits): contains the optional extended ID code of the slave

NOTE 1 The extended ID-Code is optional. As another option the first nibble may be modified by the master using the "Write_Extended_ID_Code_1" request in case the write access is not blocked by the manufacturer. The extended ID-Code is handled in the same manner as the 4 bit standard ID-Code.

Data_Output register (4 bits): contains the latest output information transmitted via a "Data_exchange" request. After power on or a reset the default values 1 shall be put into the output register.

Data_Input register (4 bits): Optional, only necessary for Synchronous Data I/O Mode. Contains the input information at sample point in Synchronous Data I/O Mode.

Parameter_Output register (4 bits): contains the latest output information transmitted via a "Write_parameter" request. After power on or a reset the default values 1 shall be put into the parameter output register.

Receive register: contains the latest received master request (start and end bit omitted)

Transmit register: contains slave response prior to transmission

Status register (4 bits): contains four bits for slave status. These four bits are independent of each other and shall have the following semantics:

address/extended ID-code 1 stored in a volatile memory:

S0: 0 address/ID1-code permanent
1 address/ID1-code volatile

NOTE 2 The address and the extended ID_code 1 can be changed independently thus the bit S0 has to be processed after each storing procedure.

periphery fault condition:

S1: 0 no periphery fault detected
1 periphery fault detected

undefined:

S2: 0 undefined
1 undefined

error reading non-volatile memory:

S3: 0 no error reading non-volatile memory
1 error reading non-volatile memory

The implementation of S1 as periphery fault condition is mandatory (inside the AS-i ASIC) if the option to implement the extended ID1/ID2 codes has been chosen. Otherwise, it is optional.

NOTE 3 The information given in the Status Register may be used for diagnostic purposes or for the master to determine what action may be taken to recover from a fault condition.

Sync_flag: the flag shall indicate the slave's synchronization to master requests.

Data_Exchange_Disable_flag: is set by RESET and reset by the first received "Write_Parameter" request. The flag shall indicate the inability to exchange data.

8.4.2.5 Watchdog

A watchdog function may be realised optionally either internally in the slave circuitry between the ASI± ports and the other ports or externally in the connected device (“behind” interface 1).

The watchdog, if activated, forces outputs of the slave to their default values.

The watchdog shall be retriggered (i.e. kept in its inactive state) by a successfully received Data_Exchange request and (optionally) by a successfully received Write_Parameter request.

The minimum watchdog time shall be equal or more than 40 ms and the maximum watchdog time shall be less than or equal to100 s.

NOTE It is recommended that the watchdog should perform a reset of the slave if activated.

8.4.3 Functions of a slave

8.4.3.1 State diagram of a slave

A slave shall perform the following main functions (see Figure 51):

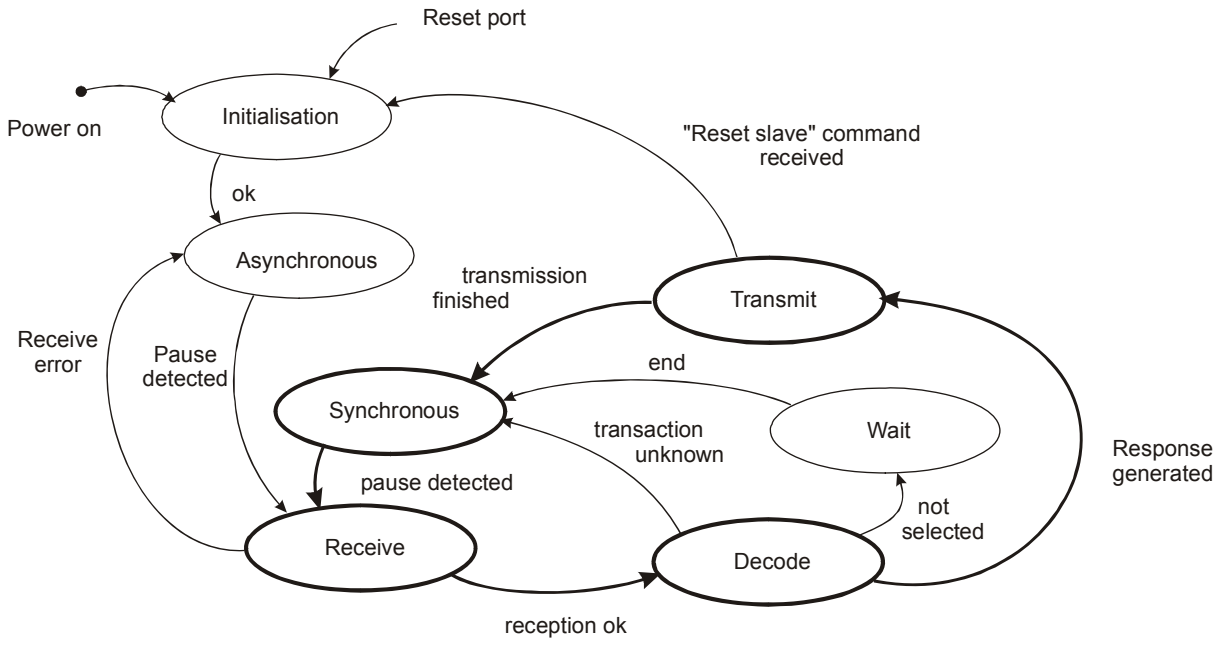


Figure 51 – Main state diagram of an AS-i slave

After power-on or after resetting the slave via the "RESET"-port or after receiving a "Reset_AS-i_Slave" request the slave shall be set to the state "INIT".

In the state ”INIT” the following functions shall be performed:

– load Data_Output and Parameter_Output registers with default values F_{Hex};

– move the contents of Data-Output and Parameter-Output registers to the corresponding ports;

– reset the Status register to 0_{Hex};

– load address, I/O configuration and ID codes from the non-volatile memory into the appropriate registers;

– set Data_Exchange_Disable flag to TRUE (for reset see 8.4.3.3);

– change to state "ASYNC".

In the state "ASYNC" the following functions shall be performed:

– reset Sync flag;

– poll the incoming data stream and detect a pause;

– if a pause is detected, change state to "RECEIVING" (see 5.5.3).

In the state "RECEIVING" the following functions shall be performed:

– wait for start bit and load master request into receive register;

– perform all error check routines (see 8.4.3.4);

– check master pause (if coming from ASYNC);

– if any error is detected, change state to "ASYNC", else to "DECODING".

In the state "DECODING" the following functions shall be performed:

– compare received address with address register; if not equal, change state to "WAIT";

– analyse information; if request unknown, change state to "SYNC";

– if data_exchange_disable flag is set and master requests "Data_Exchange", change state to "SYNC";

– perform the requested task (see 8.4.3.3) and load appropriate response into transmit register;

– change state to "TRANSMIT".

In the state "WAIT" the slave shall perform the following functions:

– wait for detectable signal (from another slave response);

– if no signal was detected, wait for end of response time (this end of response time shall be in a window from 7 to 9 bit times);

– if signal was detected, wait for end of slave response;

– change state to "SYNC".

NOTE 1 A slave has to accept a late response of another slave and should not mix it up with a master request, but at the same time it has to expect a new master request before the start of a request. With the restrictions of the end of response time mentioned above, every slave stays synchronized if not more than one repeater in a row is installed in the system. If there are two repeaters in a row, a slave response which comes from behind the second repeater is later than 54 µs and the following slave, if it is before the first repeater, is not synchronous but the master request will be received correctly.

In the state "TRANSMIT" the slave shall perform the following functions:

– wait for end of master pause (master pause is minimum of 2 bit times, if Sync flag is set; it is a maximum of 5 bit times, if Sync flag is reset);

– send slave response;

– if "Reset_Slave" request was received, change state to "INIT", else to "SYNC".

NOTE 2 It is recommended to implement a master pause of 2 to 3 bit times, if Sync flag is set, even in slaves, which are not realized with a slave-ASIC but with a µP, for example in order to avoid trouble in a topology with two repeaters in a row and a cable with a long propagation delay time concerning the slave response time-out.

In the state "SYNC" the slave shall perform the following functions:

– set Sync flag;

– poll the incoming data stream and detect a pause;

– if pause detected, change state to "RECEIVING".

8.4.3.2 Synchronous data I/O mode

As defined in this AS-i standard, a master successively polls the network slaves raising the slave addresses from the lowest to the highest. Hence, data input and output operations normally take place at different times on different slaves. To support applications that require simultaneous Data I/O operations on a certain number of slaves in the network, a Synchronous Data I/O Mode is provided. Synchronous Data I/O Mode is optional.

The idea is to exchange data in the normal cycle, but have an additional trigger event which moves the data from Output_Data register to the output and sample data from the inputs. The change from the Data_Exchange call from highest to lowest address defines this trigger event.

Once activated, input data sampling as well as output data driving events are moved to different times synchronized to the polling cycle of the AS-i network. Nevertheless, the communication principles between master and slave remain unchanged compared to regular operation.

The following rules apply:

– Data I/O is triggered by the Data_Exchange call to the slave with the lowest slave address in the network. Based on the fact that a master is calling slaves successively with rising slave addresses, the AS-i slave considers the trigger condition true, if the slave address of a received Data_Exchange call is less than the slave address of the previous (correctly received) Data_Exchange call.

– Data I/O is only triggered, if the slave has (correctly) received data during the last cycle. If the slave did not receive data (i.e. due to a communication error) the Data Outputs are not changed (arm+fire principle). The inputs however, are always sampled at the trigger event.

– If the slave with the lowest address in the network is operated in the Synchronous Data I/O Mode, it postpones the output event for the received data for a full AS-i cycle. This is to keep all output data of a particular cycle image together.

NOTE To make this feature useful, the master should generate a data output cycle image once before the start of every AS-i cycle. The image is derived from the input data of the previous cycle(s) and other control events. Once an AS-i cycle has started, the image should not change anymore. If A- and B-Slaves are installed in parallel at one address, the master should address all A-Slaves in one cycle and all B-Slaves in the other cycle.

– The input data, sampled at the slave with the lowest slave address in the network, is sent back to the master without any delay. Thus, the input data cycle image is fully captured at the end of an AS-i cycle, just as in networks without any Synchronous Data I/O Mode slaves. In other words, the input data sampling point has simply moved to the beginning of the AS-i cycle for all Synchronous Data I/O Mode slaves.

– The first Data_Exchange call that is received by a particular slave after the activation of the Data Port (Data_Exchange_Disable flag was cleared by a Write_Parameter call) is processed like in regular operation. This is to capture valid input data for the first slave response and to activate the outputs as fast as possible.

- The Data I/O operation is repeated together with the I/O cycle of the other Synchronous Data I/O Mode slaves in the network at the common trigger event. By that, the particular slave has fully reached the Synchronous Data I/O Mode.
- To avoid a general suppression of Data I/O in the special case that only one slave is visible to the master (i.e. use of a handheld programming device), the Synchronous Data I/O Mode is temporarily turned off, once the slave receives three consecutive Data_Exchange calls to its own slave address. The slave resumes to Synchronous Data I/O Mode operation if a Data_Exchange call to a different slave address is detected.

8.4.3.3 Tasks of the slave

Within the state "DECODING", the slave shall perform the following tasks depending on the particular master request (see Tables 4 and 5):

8.4.3.3.1 Function of the Data_Exchange

In performing the Data_Exchange request in non-synchronous mode the slave (with address ≠ 0) moves the received output bit pattern I0 ... I3 to the corresponding data output ports and shall signal the validity of these data bits at the data strobe output (if realized) by a pulse of 1 T_{bit} duration.

NOTE In case a slave IC is used which has multiplexed input/output ports, the data ports of the slave function as inputs or outputs, or as bi-directional inputs/outputs when the I/O configuration is established. Therefore, the programmed I/O configuration and the four data bits transferred in the master request determine the bit pattern which is moved to the output ports.

After the received data have been moved to the data output ports, the slave shall load the bit pattern of the input ports into the transmit register.

In performing the Data_Exchange request in synchronous mode, the slave (with address ≠ 0) moves the received output bit pattern I0 ... I3 to the corresponding Data_Output register.

After the received data have been moved to the Data_Output register, the slave shall load the Data_Input register into the transmit register.

8.4.3.3.2 Function of the Write_Parameter

In performing the Write_parameter request, the slave (with address ≠ 0) shall move the received bit pattern I0 ... I3 to the corresponding parameter output ports and shall signal the validity of these parameters at the parameter strobe port (if implemented) by a pulse of 1 T_{bit} duration.

After the received parameters have been moved to the parameter ports, the slave shall load the bit pattern of the parameter ports into the transmit register and shall set the Data_Exchange_Disable flag to FALSE.

NOTE 1 It is permitted to use the Parameter ports the same way as defined for the Data port. In particular, parameter input and output are independent.

NOTE 2 The first parameter call after POWER-ON or RESET activates the slave. Until then, all outputs of the slave should be in the default state. By disabling the data exchange prior to a first successful Write_parameter request after each RESET, it is assured that a slave will always have the expected parametrization, even after an unnoticed RESET due to a short power fail.

8.4.3.3.3 Function of the Address_Assignment

In performing the Address_Assignment request the slave (with address = 0) shall move the received bit pattern I0...I4 to the address register.

With the slave response, the slave signals to the master that the Address_Assignment has been processed without error. In the case of positive Address_Assignment, the slave shall immediately respond with a bit pattern "0110_{Bin}" in the slave response.

The address shall be stored in the non-volatile memory.

If the address is reprogrammable, the procedure of storing data in the non-volatile memory shall take less than 500 ms. During this procedure, the Status Register Bit S0 is set to High.

NOTE The master may perform the "Read_Status_request" to determine whether the slave has finished the storage process.

If the AS-i master did not receive a valid slave response, it shall determine, whether the Address_Assignment process was successful or not by using appropriate master requests.

After a valid Address_Assignment, a slave shall respond with the new address.

8.4.3.3.4 Function of the Write_Extended_ID-Code_1

The optional extended ID-Code (ID1) is variable and may be set by the master. In performing the Write_Extended_ID-Code_1 request, the slave (with address =0) shall move the received bit pattern I0 ... I3 to the corresponding internal ID-Code register and start the storage process to the non-volatile memory.

The procedure of storing data in the non-volatile memory shall take less than 500 ms. During this procedure the Status Register Bit S0 is set to High.

After the received bit pattern has been loaded to the corresponding register, the slave shall immediately respond with a bit pattern "0000_{Bin}" in the slave response.

If the write access to the Extended_ID_Code_1 is blocked by the manufacturer, the slave shall show the following reactions when receiving a Write_Extended_ID_Code_1 request:

– the slave shall respond to a "write ID1" request with the bit pattern "0000_{Bin}" if the information of the ID1 in the slave is identical to the information of the "write ID1" request;
– the slave shall not respond to a "write ID1" request if the information of the ID1 in the slave is different from the information of the "write ID1" request.

8.4.3.3.5 Function of the Reset_Slave

This command initiates the routine that is also performed during power-up or when the external Reset_input is activated.

This routine performs the following functions:

– load Data_Output and Parameter_Output registers with default values F_{Hex};
– reset the Status register to 0_{Hex};
– load address, I/O_Configuration and ID_Code from the non-volatile memory into the appropriate registers;
– set Data_Exchange_Disable flag to TRUE;
– bitpattern ”0110_{Bin}” shall be given in the slave response.

Thus it is possible with this command to reassign the previous operating address after having issued a "Delete_address" requests (e.g. for test purposes).

The Reset_Slave processing shall take less than 3 ms. During this time the slave may not respond to any other requests issued by the master.

8.4.3.3.6 Function of the Delete_Address

The deletion of the operation address shall be done by overwriting the operation address stored in the internal address register of the slave with the zero address. The zero address shall not be stored in the non-volatile memory. The deletion of the operating address is, therefore, temporary only until the next "Address_Assignment" request or "Reset_Slave" request is received or the slave_reset-input is activated or a power failure occurs.

In the case of positive Delete_ Address, the slave shall immediately respond with a bit pattern "0000_{Bin}" in the slave response.

After a valid Address_Assignment, a slave shall respond with the new address.

NOTE If the slave is in the process of storing its address into the non-volatile memory (processing the "Address_Assignment" request), a "Delete_Address" request should not be issued by the master. The result of the storage process would be undefined.

8.4.3.3.7 Function of the Read_I/O_Configuration

The actual I/O code of the slave shall immediately be read from the slave and transferred to the master in the slave response.

There are four types of configuration of the 4-bit input/output ports (see Table 7):

– no configuration;
– input;
– output;
– bi-directional I/O only.

In the Read_I/O_Configuration response, the slave shall respond the actual I/O configuration of the input/output ports. The I/O configuration is related to the data inputs and outputs of the slave ports only.

8.4.3.3.8 Function of the Read_Identification_Code

The identification code of the slave shall immediately be read from the slave and transferred to the master in the slave response.

8.4.3.3.9 Function of the Read_Extended_ID-Code_1/2

The optional extended identification code of the slave shall immediately be read from the slave and transferred to the master in the slave response.

8.4.3.3.10 Function of the Read_Status

The current status of the slave shall immediately be read from the slave and transferred to the master in the slave response. The actual values S1 to S3 of the status shall remain unchanged.

The state change of S0 (H->L) shall be valid not later than 2 ms after a Read_status request. The updated status of S0 can be read with a further Read_status request.

NOTE The Read_Status_Request may be used by the slave circuitry to update the status flags. The new status can be read by a new Read_Status_Request which follows at least 2ms after the first Read_Status_Request.

8.4.3.3.11 Function of R1

Reserved.

8.4.3.3.12 Function of the broadcast (Reset)

This command initiates the same routine that is also performed during power-up or when the external Reset_input is activated or the "Reset_Slave" request is issued (see 5.6.5.5). However, there shall be no slave response to this command request.

8.4.3.3.13 Function of a slave with profiles S-0.A to S-F.A

Slaves with the I/O-Configuration set to "0, 1, ... F" and the ID-Code set to "A_{Hex}" are in the "extended address mode" and shall always interpret the information bit I3 according to Table 5 as additional Select bit "Sel" in the following requests:

- Data_Exchange
- Write_Parameter
- Delete_Address
- Reset_Slave
- Read_I/O_Configuration
- Read_ID-Code
- Read_Status
- Read_Extended_ID-Code_1/2

Only the Address_Assignment request, the Write_Extended_ID-Code_1 request and the Broadcast (Reset) are interpreted as usual. Slaves using these profiles can receive a maximum of 3 bits of output data and parameter information only (instead of 4 bits).

The bit I3 of the extended ID1-Code is interpreted as additional select bit "Sel", when these slave profiles are selected. It may be modified by the master via the "Write_Extended_ID-Code_1" request (see 5.6.5.4).

Slaves with one of these profiles can be connected in pairs of two to the AS-i-network. Thus a maximum of 62 slaves with these profiles may operate in one network. To ensure compatibility with masters not supporting the extended address mode, a slave with the additional select bit "Sel" set to "0" performs like a slave with any other profile. Therefore, the interpretation of the select bit "Sel" in some master requests is inverted (refer to Table 5 for details). A slave with profile S 0.A to S F.A and "Sel" set to "1" will not respond to command requests of a master not supporting this profile.

Therefore, the use of ID code "A_{Hex}" is restricted to slaves which have this option to operate as pairs in a network. Slaves with the non-volatile address "00_{Hex}" and ID-code "A_{Hex}" shall not be programmed as "B-slaves".

The use of these slave profiles is subject to assignment by the standardisation body of the AS-i Association (see Annex A).

NOTE Slaves using this profile have to meet a different impedance specification than standard slaves (see 8.4.4.4).

8.4.3.4 Error handling

8.4.3.4.1 Communication errors

The slave shall be able to detect communication errors while in the "RECEIVING" state (see 5.8).

8.4.3.4.2 Slaves errors

If the slave has one of the following internal failures, the communication between the master and the other slaves shall not be affected. The slave may be disconnected from the AS-i line by, for example a fuse. This process shall not be reversible at least until a Power-On-Reset.

– If due to an internal fault of the slave, the slave shall try to send data for longer than 1 ms, the slave shall be disconnected from the bus line by a self-interrupt capability ("Jabber inhibit"). This process shall be reset by a Power-On-Reset only.

– If the slave receives a master request, which does not pass the error detection circuitry due to a detected error in the transaction, it must not send a slave response.

NOTE 1 This behaviour is mandatory because the error may have occurred in the address section of the master request and the receiving slave may not be the one being addressed. Thus multiple answers to one master request are avoided.

– If, during the RESET-procedure (State "INIT") the slave reads its address from the non-volatile memory and detects a read error, it shall load the zero address into its address register and shall set Bit S3 of the status register to HIGH.

NOTE 2 It may happen to the slave that, during the process of writing its address into the non-volatile memory, a supply voltage breakdown occurs. In this case, the stored address may be invalid. The master may be able to recover from this condition by repeating the "Address_assignment" request.

– If, during the RESET-procedure (State "INIT") the slave reads its I/O configuration and ID Code from the non-volatile memory and detects a read error, it shall load F_{Hex} into both appropriate registers and shall set Bit S3 of the status register to HIGH.

– If the Slave detects a peripheral fault (e.g. overload of the power supply) it may disconnect the power supply. To signal this state bit S1 of the status register shall be set to HIGH. This is an optional feature.

8.4.3.4.3 Network errors

A missing communication may be handled by the slave with the watchdog function (for details see 8.4.2.5). Other network errors are handled by the master (see 8.5.2.2).

NOTE Errors in the connected device may be handled by the device and may be signalled to the controller, for example by communication through the network during the next data exchange. Another possible way to communicate an error condition of the device is to reset the slave. The slave then will not respond to data requests any more, so the master will report a "Config Error".

8.4.4 General technical requirements

8.4.4.1 Voltages

The slave and the AS-i device shall be capable of operating with any d.c. voltage which is applied at the ASI+ and ASI- ports and is between 31,6 V and 26,5 V, or with any lower voltage that is stated by the manufacturer in the product documentation. The slave itself shall communicate with the master between 18,5 V d.c. and 31,6 V d.c.

If the AS-i supply voltage (measured between ASI+ and ASI− of the slave) drops below the limit of 18,5 V d.c. no master request needs to be processed.

No internal reset shall be issued if the voltage drops below 18,5 V d.c. for less than 1 ms, but the connected device may cause a RESET if the voltage drops below a given limit.

If ASI+ and ASI− are inversely connected to the AS-i network (e.g. because of faulty installation), the slave shall not be damaged in any way and the communication between master and other slaves of the network shall not be disturbed.

8.4.4.2 Currents

The maximum of the total current consumption (in the range 0 V to 31,6 V d.c. of the slave) shall be stated by the manufacturer. In normal operating conditions, the current slew rate of the slave is allowed to effect a noise $\leq 20\ mV_{pp}$ on the AS-i-line in the frequency range 10 kHz to 500 kHz. Switching actuators from off-state to on-state and vice versa is considered a normal operating condition; connecting or disconnecting a slave during installation ("life insertion") or short-circuits at external ports of the slave are considered irregular operating conditions.

For start-up charging a maximum capacitance of 470 µF is allowed in a slave. If extended addressing is used, the maximum capacitance is limited to 240 µF.

Overload and short-circuit conditions at external ports of the slave shall not disturb communication between the master and other slaves on the network. Under overload or short-circuit conditions at all the terminals of a slave, the total current consumption from the AS-i line shall not exceed the total current consumption stated in the documentation plus 150 mA.

8.4.4.3 Time delay before availability

Within 1 s after 26,5 V d.c. (U_{min} of AS-i power supply minus 3 V voltage drop) is put to the ports ASI+ and ASI− a slave shall become able to communicate with the master.

The value 26,5 V d.c. has also to be reached under a current limit of the maximum total current consumption (as stated in the documentation) plus 12,5 mA (6,5 mA for extended address mode slaves) within a time of 1 s.

8.4.4.4 Impedance

The input impedance of a slave, measured between the ASI+ and the ASI− connections under normal operating conditions with the slave installed on a grounded metal plate, shall be in accordance with the limits of the equivalent circuit of the slave. Limits are given in Table 20. During test all parts shall be grounded. The equivalent circuit is shown in Figure 52.

To determine the values of *R*, *L* and *C* of the equivalent circuit, the values of |*Z*| shall be measured at several frequencies in the range of 50 kHz to 300 kHz. The R-L-C model then is fitted to the measured values of |*Z*| using an algorithm that determines the best fit, i.e. the minimum of the sum of the squared relative errors.

For further details see "Test Requirements Slave".

The impedance to ground, measured between either ASI+ or ASI- to ground while all metal parts of the slave (except electrical ports) shall be grounded, shall not be below 1 MΩ at d.c..

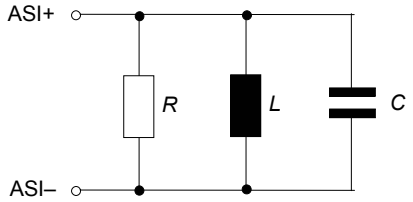


Figure 52 – Equivalent circuit of a slave for frequencies in the range of 50 kHz to 300 kHz

Table 20 – Limits for *R*, *L* and *C* of the equivalent circuit of a slave

	R (kΩ)	*L* (mH)	*C* (pF)
Valid values (standard slave)	> 8 kΩ	> 9 mH	< 100 pF
Valid values (standard slave)	> 8 kΩ	6 ... 9 mH	< 70 pF + (*L* – 6 mH) ∗ 10 pF/mH
Valid values (slave with profile S - X.A)	> 13,5 kΩ	> 13,5 mH	< 50pF
Valid values (slave with profile S - X.A)	> 13,5 kΩ	12 ... 13,5 mH	< 35 pF + (*L* – 12 mH) ∗ 10 pF/mH

$$|Z| = \frac{1}{\sqrt{\left(\frac{1}{R}\right)^2 + \left(2\pi f C - \frac{1}{2\pi f L}\right)^2}}$$

The calculated values of *R*, *L* and *C* shall be in accordance with the values given in Table 20.

8.4.4.5 Symmetry

For high noise immunity it is recommended to minimize the difference of both impedances (ASI+ to ground and ASI− to ground) within the frequency range in which noise is expected.

In the frequency range of 50 kHz to 300 kHz the quotient $|Z_1|/|Z_2|$ of these impedances (Z_1, Z_2) shall meet:

– $0{,}90 \le |Z_1|/|Z_2| \le 1{,}10$

or

– $|Z_1|/|Z_2| < 0{,}90$ or $1{,}10 < |Z_1|/|Z_2|$ and compensation with C3 < 30 pF for slaves in standard address mode

or

– $|Z_1|/|Z_2| < 0{,}90$ or $1{,}10 < |Z_1|/|Z_2|$ and compensation with C3 < 15 pF for slaves in extended address mode

The measuring point M can be the auxiliary power for the sensor if the slave has external ports.

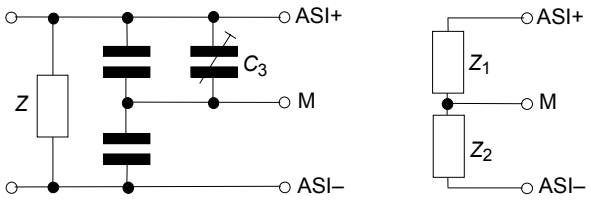


Figure 53 – A slave with C3 to compensate for $Z_1 = Z_2$

If there is no external port this measuring point M may be:

– the metal case of the slave with integrated AS-i-IC, or

– the metal on which the slave with integrated AS-i-IC is mounted (see 9.5.5)

If the slave can be connected to external components (e.g. standard inductive proximity switches connected to a module) and if these may influence the impedance to ground, limits shall be stated in the documentation of the slave. If no limits are stated, the connection of an impedance of 100 nF in parallel to 10 MΩ to any of the external ports of the slave module

(except ASI+, ASI-) and ground shall be allowable. This shall not influence the measured impedance to ground, as stated above, in a way that the given limits are not met.

8.4.4.6 Electrical and mechanical protection

The protection class according to IEC 61140 of the slave shall allow its connection to systems with protective extra low voltage (PELV).

The IP rating of the slave according to IEC 60529 shall be stated by the manufacturer.

8.4.4.7 Status indication

Status indications on a slave are optional. If any status indication (e.g. a LED) is used, it shall be used in the following manner:

- a yellow indicator shall indicate a "switching status"; this indicator shall be active when the corresponding Data_Exchange bit or Parameter Bit is set to Low (if the port is an output port). If the port is an input port, the indicator shall be active, when the corresponding Data_Exchange Bit is set to HIGH;
- a green indicator shall indicate a "power on". It shall be marked "POWER" or "PWR" if it indicates the voltage on the AS-i line. It shall be marked "AUX" if it indicates the auxiliary voltage;
- a red indicator shall indicate a "fault"; this indicator shall be active when the slave detects a periphery fault or a no data exchange fault condition. It shall be marked "FAULT";
- the FAULT indicator shall be in a steady state in order to display a "No data exchange fault" and shall flash with a rate of approximately 1 Hz to 3 Hz to display a "periphery fault";

NOTE 1 A "No data exchange fault" condition may result if the master is in STOP mode, the slave has zero address, the slave has an address which is not in the LPS, the slave has a wrong I/O/ID-configuration or the slave has detected an internal hardware fault. The "No data exchange fault" will lead to a "Config Error" indication in the master.

NOTE 2 A "periphery fault" condition may result if an overload, short circuit or open loop at an output, an earth fault, not interpretable data (e.g. in case of analogue data transfer) or any other periphery fault is detected by the slave. The "periphery fault" indication will correspond to the optional S1 bit of the Status register (see 8.4.2.4) and lead to a "Periphery Fault" indication in the master.

- if more than one fault occurs at the same time, only the fault with highest priority will be displayed. Highest priority has "periphery fault";
- if there is limited space on the slave, an alternative indication with a two-colour-LED which is marked "POWER/FAULT" or "PWR/FAULT" and the following signals is allowed:
  - power on: green, steady state
  - no data exchange: red, steady state
  - periphery fault: red/green, alternating flashing

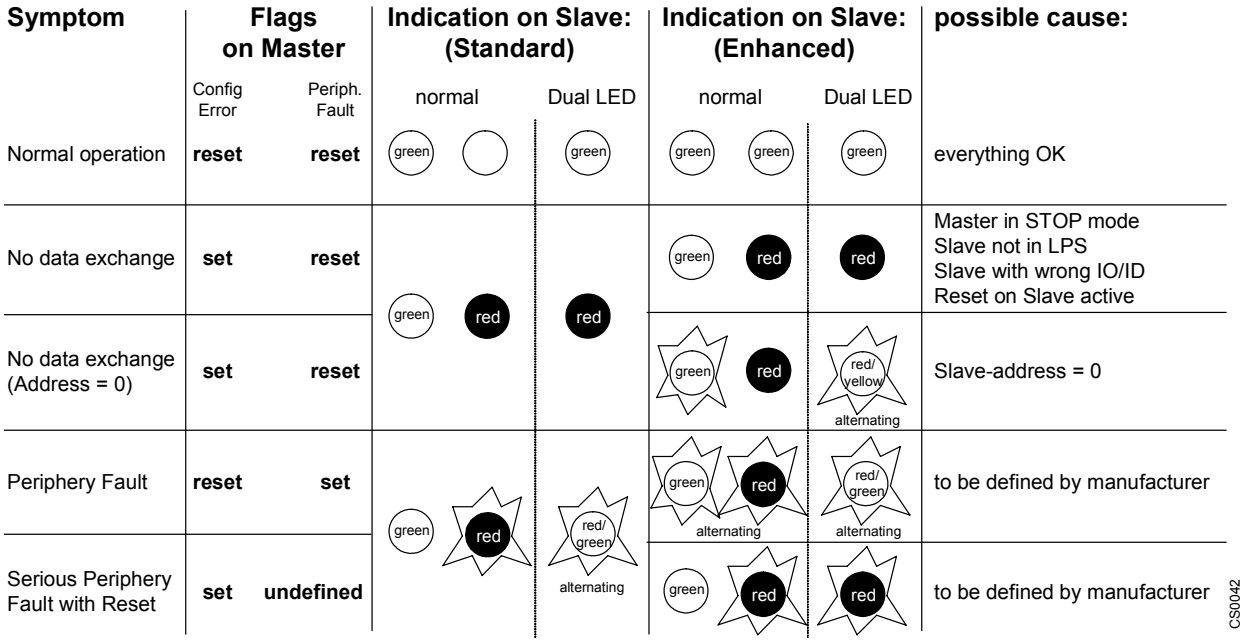


Figure 54 – Status indication on slaves

– for an enhanced status indication it is optionally allowed to use the "power on" indicator in flashing mode to display additional information on the kind of fault. In this case, the LED shall be marked "AS-i". Details shall be described in the manufacturer's documentation;

  In the case of the enhanced status indication, the following signals are defined:

  – power on: green, steady state
  – no data exchange: green and red, steady state
  – address = 0: red, steady state; green, flashing
  – periphery fault: red/green, alternating flashing
  – serious periphery fault with reset: red, flashing; green steady state

  If a two-colour-LED is used, the marking is "AS-i/FAULT" and the following is defined:

  – power on: green, steady state
  – no data exchange: red, steady state
  – address = 0: red/yellow, alternating flashing (see Note)
  – periphery fault: red/green, alternating flashing
  – serious periphery fault with reset: red, flashing

NOTE 3 A two-colour-LED (red/green) lights up in a shade of yellow if both LEDs are activated simultaneously. This is what is meant in this case.

– other functions must be indicated with other indicators, which may have any colour or any colour in flashing mode. These indicators must be marked in a way that they cannot be confused with the indicators defined above.

8.4.4.8 Receiver and transmitter requirements

The slave shall be able to receive and decode a message as described in 5.2.

The slave shall be able to transmit its information by a current signal, superimposed on the d.c. voltage of the AS-i network as specified in 5.2.

8.4.4.9 Slaves with auxiliary power supply

AS-i slaves may be powered with auxiliary power. In this case, the following additional conditions shall be met:

The AS-i line shall be protective isolated from any non-PELV voltage outside in accordance with IEC 60364-4-41. This may be achieved by one of the following measures:

The auxiliary voltage itself is a PELV.

The isolation within the slave is equivalent to the protection provided by PELV. In this case, the auxiliary voltage may be a non-PELV voltage.

The rating of and the safety requirements for the auxiliary power supply shall be stated by the manufacturer.

If an AS-i standard cable according to 8.1.1 is used for the interconnection of the auxiliary power supply in the slave, its outer sheath shall be of any colour except yellow. The connecting points for the AS-i line and the auxiliary power supply shall be clearly marked at the device. A colour indication is sufficient. If the marking is made by using letters, the identification shall be made by “POWER” or “PWR” (for the AS-i line) and “AUX” (for auxiliary power).

NOTE Reasons for an auxiliary power supply may include:

a) power consumption if the slave cannot meet the specification in 8.4.4.2,

b) exceeding limits of AS-i power supply,

c) slew rate of current exceeding specified limits, or

d) emergency stop.

8.5 AS-i master

8.5.1 Overview

The AS-i master provides all means to exchange data between a controller and the slaves in an AS-i system (see Figure 1).

In this standard, a master is described which polls all slaves in a cyclical order. The maximum number of slaves (MAX_SL) is defined in the relevant master profiles. The master works transparently and does not interpret the slave data in any way if interpretation is not required by combined transaction types. In addition to the cyclic exchange of data with connected slaves, it organises and monitors the network and supports the controller with diagnostic data.

Subclause 8.5.2 defines the master specific physical requirements and 8.5.3 the logical requirements for controlling all the telegrams to be exchanged.

The interface between AS-i-Master and the controller (i.e. PLC) (controller interface) depends on the physical and logical features of the different controllers.

The master has a layered structure which is composed of two functional parts as shown in Figure 55.

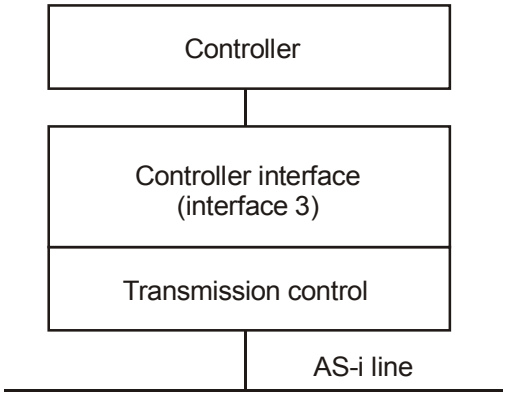


Figure 55 – Structure of an AS-i master

Controller interface acting as the logical interface between the master and the controller. The controller uses the functions provided by the controller interface to communicate with the AS-i system. It shall be responsible for initialization of the master and the AS-i system, cyclic data exchange, acyclic commands and execution control functions.

Transmission control responsible for the physical transmission of master request as well as the automatic retransmission of requests in case of failure. The AS-i master shall send and receive, respectively (i.e. request and response) as defined in 5.6.3

NOTE The controller and the controller interface are not within the scope of this standard.

8.5.2 Master specific requirements for transmission

The following definition contains the master specific requirements for the transmission system which are not part of the definition of the transmission system itself.

NOTE The AS-i transmission system is defined in Clause 5.

8.5.2.1 Line interface

A master shall conform to the standards of the transmission given in 5.2 of this standard as long as there are no master specific definitions described in the following.

The AS-i line shall be protectively isolated from all other non-PELV power supplies in accordance to IEC 61140. The isolation shall be realized especially to the controller power supply but also to all other power supplies which are connected indirectly to the controller.

8.5.2.2 General requirements

The following defined values shall be applied to the master:

– under normal operating conditions, the current slew rate of the Master shall not generate a noise on the AS-i-line of more than 50 mV_{pp} in a frequency range of 10 kHz to 500 kHz;

– the manufacturer shall state in his document the precautions needed to assure the PELV condition of the AS-i-system;

– after power-on, the operating voltage at the master terminals (ASI+ and ASI−) shall reach 26,5 V d.c. (i.e. U_{min} of the AS-i power supply) within at least 1 s. This value has to be reached under a current limit of the maximum total current consumption (as stated in the documentation) plus 12,5 mA;

– if the master terminals (ASI+ and ASI−) are inversely connected to the AS-i network (e.g. because of faulty installation), the master shall not be damaged in any way;

NOTE 1 These requirements are intended to ensure a defined power-on behaviour, the defined function of an AS-i network even under certain fault conditions and the symmetry of the AS-i line so that the interference immunity will be optimized.

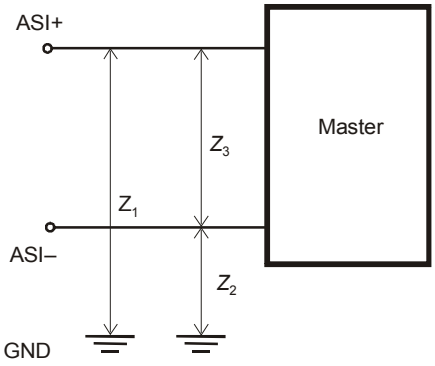


Figure 56 – Impedances of the master

– the values for C, R and L according to the equivalent circuit (Figure 57) shall be calculated as described for the slaves in 8.4.4.4;

Table 21 – Limits for *R*, *L* and *C* of the equivalent circuit of a master

R	*L*	*C*
> 5 kΩ	> 3 mH	< 400 pF

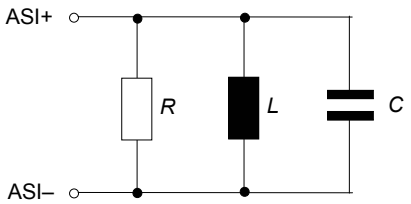


Figure 57 – Equivalent circuit of a master for frequencies in the range of 50 kHz to 300 kHz

– the impedance to ground, measured between either ASI+ (Z_1) or ASI− (Z_2) to ground or the controller's power supply while the Master (and controller) is mounted on a grounded metal plate, shall not be below 250 kΩ at d.c.. During test, all metal parts of Master and controller shall be grounded;

– for high noise immunity, it is recommended to minimize the difference of both impedances (ASI+ to ground and ASI− to ground) within the frequency range in which noise is expected. In the frequency range of 50 kHz to 300 kHz the difference $|\Delta Z|$ of these impedances (Z_1, Z_2) (Figure 56) shall meet the same symmetry requirements which are defined for the slaves (see 8.4.4.5);

NOTE 2 In order to improve the noise immunity of the system, the differential impedance should be as low as possible.

– the signal AS-i Power On (APO) shall be set, as long as the d.c. voltage of the AS-i line is not below the threshold of 22,5 V ± 1 V. It shall be reset if the voltage is below this threshold for more than 2,0 ms. It shall not be reset if the voltage is below this threshold for less than 0,7 ms.

8.5.2.3 Receiver and transmitter requirements

The transmitter of the master shall conform to the specification of the transmitter given in 5.2.3 in a d.c. voltage range between 16,5 V and 31,6 V on the AS-i line.

NOTE This voltage range guarantees that a slave may receive a Reset_Slave request in cases where voltage is low at the AS-i line.

The master shall be able to receive and decode a slave response as specified in 5.2.4.

8.5.2.4 Transmission control

The transmission control provides a means for sending one request by the master to one single slave and receiving a response from the slave. At a given time, the transmission control processes one and only one request. After a transaction has been finished, the next transfer can be processed by the transmission control. In case of failure, no more than one retransmission shall be processed by the transmission control.

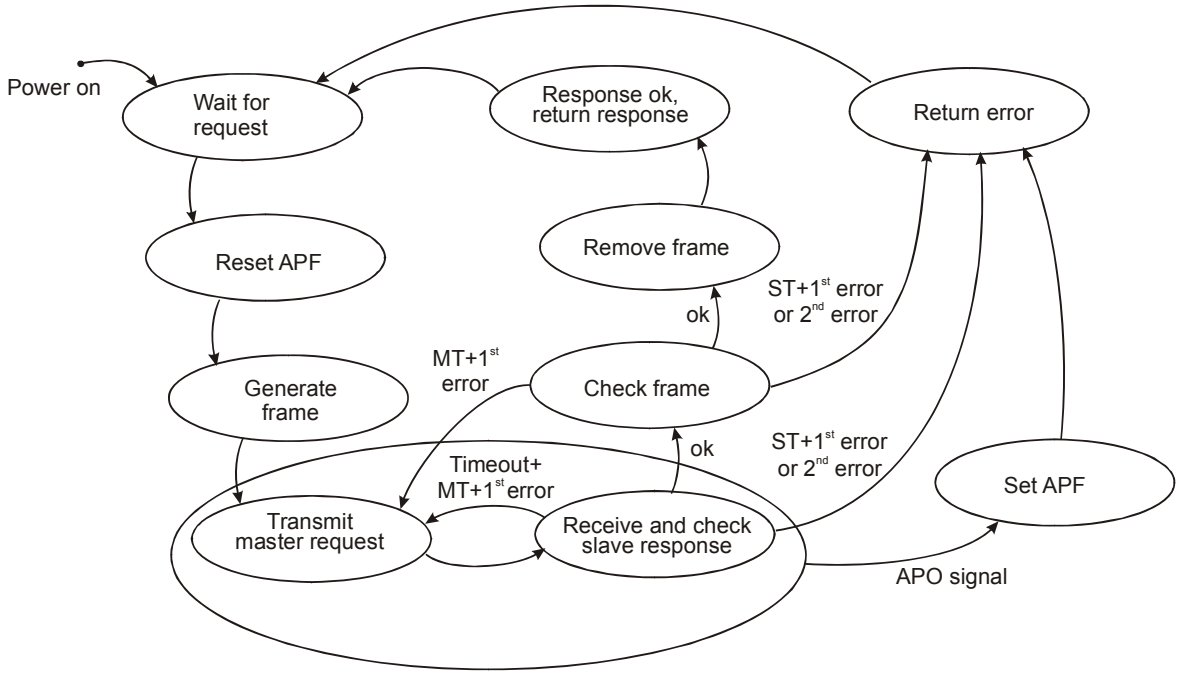


Figure 58 – Transmission control state machine

8.5.2.5 Error detection

The master's transmission control shall be able to detect the following errors:

a) Missing slave responses

There is no slave response if, for example, the respective slave

- is not connected to the AS-i line;
- does not have a valid address;
- has detected a failure in the received master request;
- has a receiver defect;
- cannot answer anymore because of a defect or a reset;
- did not receive a parameter prior to a data exchange request after power-on or reset.

The master is responsible for determining this as exceeding the allowed response time (slave response time-out).

b) Failure in slave responses

A disturbed slave response results when, for example

– several slaves transmit simultaneously;

– disturbances through energy coupling from a harsh environment occur.

While receiving a slave response, the transmission control shall be able to evaluate all the transmission errors described in 5.8.

NOTE With implementation of the appropriate functions, the master can recognize and report the failure condition "Slave Response Failure", for example to the controller as a separate message. These functions are beyond the scope of this standard.

8.6 Electromagnetic compatibility (EMC)

8.6.1 General

The operating characteristics of the AS-i-system shall be maintained at the relevant levels of electromagnetic compatibility (EMC).

All immunity and emission tests are type tests and shall be carried out under representative conditions, both operational and environmental, using the recommended wiring practices and including all equipment necessary for communication and data transfer on the AS-i- line.

This requirement can be met by the use of one master, one slave and one power supply.

A length of 100 m of cable shall be used for the AS-i line unless otherwise stated in the test instructions.

The AS-i device to be tested shall have all the essential design details of the type which it represents and shall be in a clean and new condition.

Maintenance or replacement of parts during or after a testing cycle is not permitted.

8.6.2 Immunity

Subclause 8.2.1 of IEC 62026-1 applies with the following modifications.

The test results are specified using the following performance criteria:

– A. Normal performance within the specification limits and a maximum of one disturbed message per communication cycle.

– B. During the tests a temporary loss of the data communication may occur, thereafter the ASInterface device shall continue to operate as intended. No change of actual operating state or stored data is allowed.

8.6.2.1 Electrostatic discharges

Performance criterion B shall apply.

8.6.2.2 Radiated radio frequency electromagnetic fields

Performance criterion A shall apply.

8.6.2.3 Conducted radio frequency disturbances

This test is not applicable, since data signal is carried on the power wires.

NOTE The operating environment of these devices using an AS-i power supply with a decoupling network is considered to be well-protected against conducted radio frequency disturbances.

8.6.2.4 Electrical fast transients/bursts

The minimum test voltage shall be 1 kV with performance criterion A and 2 kV with performance criterion B and both test voltages shall be applied with a repetition rate of 5 kHz by the capacitive coupling clamp.

8.6.2.5 Surges

AS-i devices shall not be tested for surge immunity.

The operating environment of these devices is considered to be well-protected against surge voltages caused by lightning strikes.

8.6.2.6 Voltage dips

No internal reset shall be issued if the voltage drops below 18,5 V d.c. for less than 1 ms, but the connected device may cause a reset if the voltage drops below a given limit. This value is valid for slaves only. The value for master is defined in 8.5.2.2.

8.6.3 Emission

Subclause 8.2.2 of IEC 62026-1 applies with the following additions.

The measurement shall be made in the operating mode including grounding conditions producing the highest emission in the frequency band being investigated which is consistent with normal applications.

Each measurement shall be performed in defined and reproducible conditions.

9 Tests

9.1 Kinds of tests

9.1.1 General

Clause 9 of IEC 62026-1 and 8.1 of IEC 60947-1 apply with the following modifications.

This subclause specifies test requirements for logical, electrical and mechanical specifications. These test requirements specify those requirements which are not implicitly defined in the previous subclauses, for example distance between AS-i master and AS-i slave during a specific test.

Tests are divided into three parts:

– logical testing (e.g. behaviour of the slave after receiving a message);

– electrical testing (e.g. testing the signals and time constraints);

– mechanical testing (e.g. dimensions of AS-i standard cable).

If AS-i specifications are implemented as an integral part of a product, for example a specific actuator, the logical test is highly dependent on the behaviour of the product. To verify the compliance of the AS-i part to this standard, the specific environment in which AS-i has been integrated shall be taken into account.

Compliance to this standard does not necessarily mean compliance to a specific standard of the whole product in which AS-i is integrated. A test under specific applications of the AS-i functions is outside the scope of this standard.

If a manufacturer claims conformity of an AS-i slave to this standard, it shall be marked that the conformity comprises the conformity to the AS-i specific parts only. The conformity of, for example, a sensor is independent of the AS-i conformity testing.

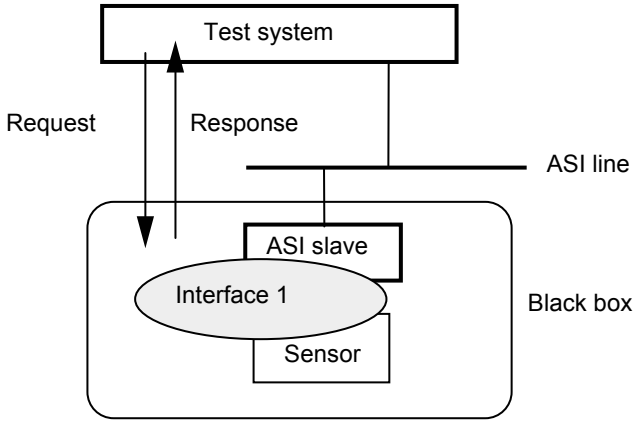


Figure 59 – AS-i interfaces

The test system shall only test if the response sent by the slave is correct. Because interface 1 is conceptual in nature, the concrete representation of the interface depends mainly on the environment in which it is used. The logical tests shall be restricted to the test of the AS-i slave treated as a black box.

All measurements of the electrical and mechanical tests shall be at an accuracy of ±1 % if not otherwise stated.

9.1.2 Type tests

Type tests are intended to verify compliance with this standard.

These include:

– test of the transmission system (9.2);
– test of the AS-i power supply (9.3);
– test of an AS-i repeater and other components (9.4);
– test of an AS-i slave (9.5);
– test of the AS-i master (9.6).

9.2 Test of transmission medium

Tests of the transmission medium comprise the test of the AS-i standard cable, the AS-i cabinet cable or any other cable intended for use in an AS-i network.

The dimensions and other mechanical properties of the AS-i standard cable or the AS-i cabinet cable shall be verified according to Figures 46 and 47 and the other technical data given in 8.1.

The electrical properties shall be verified according to the data given in 5.4.1.

9.3 Test of the AS-i power supply

9.3.1 Impedance

9.3.1.1 General

The test instruction allows to test the impedance of an AS-i power supply "in operative state" under laboratory conditions on the basis of a compensation method (bridge circuit). It is not the absolute impedance which is determined, but only the observation or exceeding of the required tolerance limit.

9.3.1.2 Test circuit

Figure 60 shows the necessary measurement set-up.

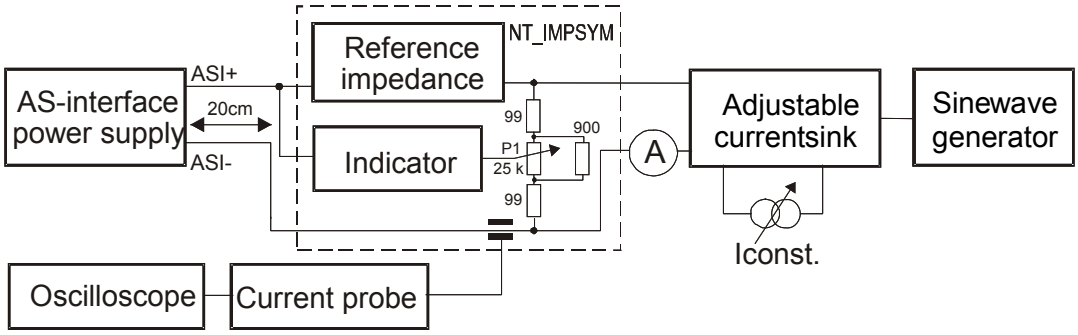


Figure 60 – Test circuit for impedance measurement

Figure 61 shows the circuit of the used adjustable current sink, Figure 62 shows a schematic diagram for the indicator. The display (Figure 63), for determination of the minimum, can be realized, for example by a 10-digit LED chain control via the circuit LM 3914 N (resolution: 250 mV/LED). At the measurement frequencies of 50 kHz and 300 kHz, the reference inductance must have a value of 100 µH ± 0,5 %, possibly it has to be realized by two inductances or by alignment. The recommended design is an air-cored coil.

9.3.1.3 Measuring and test equipment for ASI-power supply

This shall include:

– sine wave generator;
– current meter;
– oscilloscope with current probe;
– adjustable current sink (test circuit: NT_MODSENKE, Figure 61);
– indicator (potential-free peak detector according to Figure 62, test circuit: NT_IMPSYM);
– reference impedance (100 µH ±0,5 % || 78 Ω ± 1 %).

9.3.1.4 Test procedure

The following steps shall be taken:

1. Establish the measurement set-up according to Figure 60, taking into account additional resistive loads (0,1 A at U_{ASI} as well as I_E) of the voltage output not under test, for non-standard AS-i power supplies.

2. By means of the adjustable current sink, adjust output currents of 0,1 A or I_E, respectively, and a modulation amplitude of the current sink of 75 mA_{pp} ± 10 % (check by means of an oscilloscope) at 50 kHz.

3. Align the bridge circuit on the potentiometer (range: −10 % to +10 %), checking at the same time the minimum display on the indicator.

4. Repeat items 2 and 3 at 300 kHz.

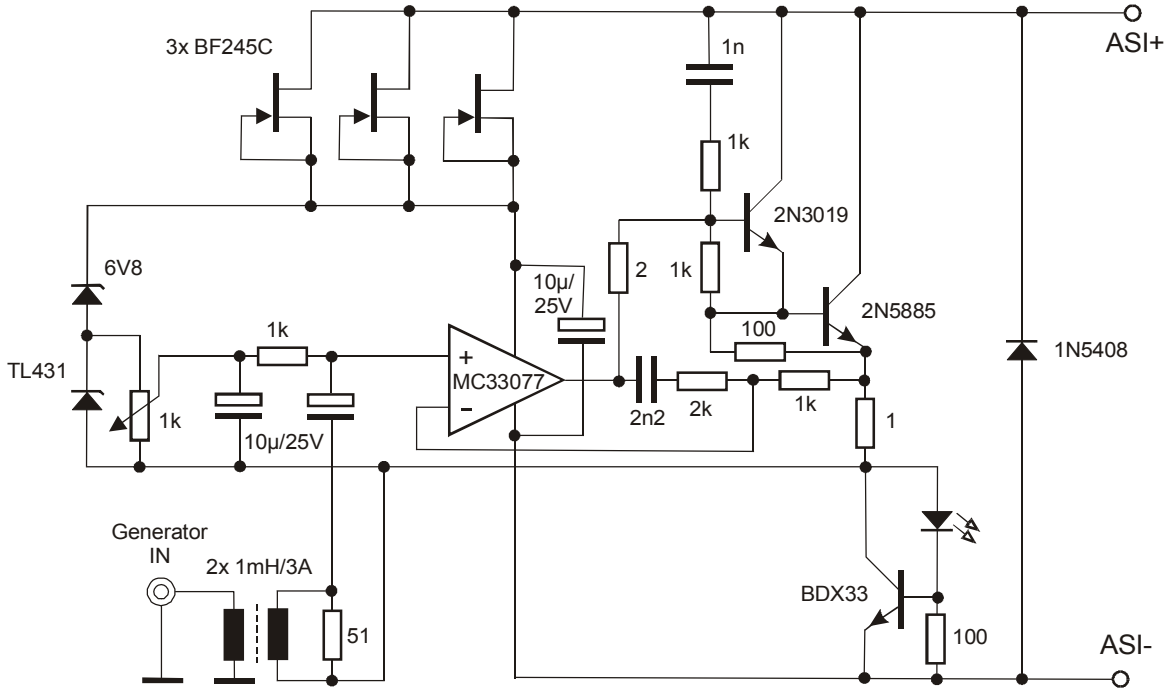


Figure 61 – Adjustable current sink (test circuit: NT_MODSENKE)

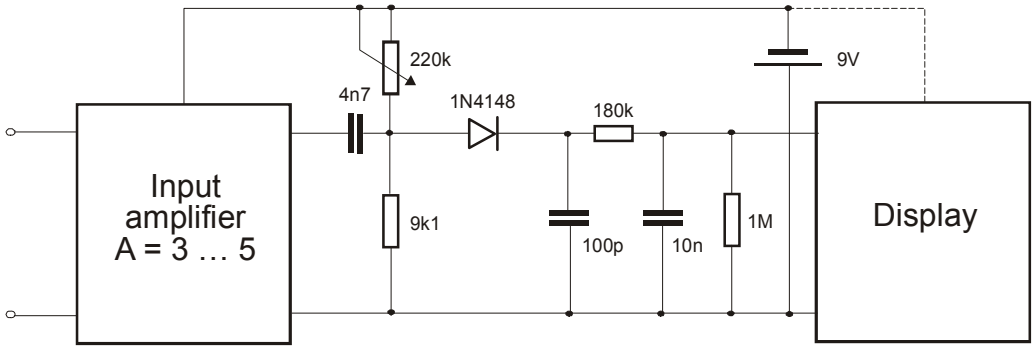


Figure 62 – Indicator (test circuit NT_IMPSYM)

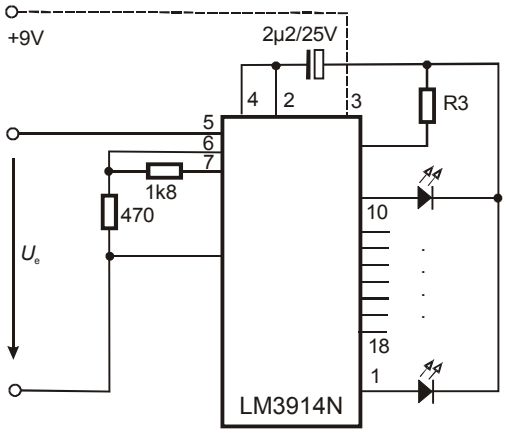


Figure 63 – Display (part of test circuit NT_IMPSYM)

9.3.1.5 Evaluation of the results

With the bridge circuit, cf. Figure 60, verify on potentiometer P1 (detuning range ±10 %, corresponding to the required tolerance limit for the impedance) at both output currents (0,1 A and I_E) and at the measurement frequencies (50 kHz and 300 kHz, modulation amplitude 75 mA_{pp}) the adjustability to the indicator minimum, taking into account additional loads for non-standard AS-i power supplies.

9.3.2 Symmetry

9.3.2.1 General

The test instruction allows to test the symmetry of an AS-i power supply "in operative state" under laboratory conditions on the basis of a compensation method (bridge circuit). It is checked whether the required tolerance limit is observed or exceeded.

9.3.2.2 Test circuit

Figure 64 shows the necessary measurement set-up.

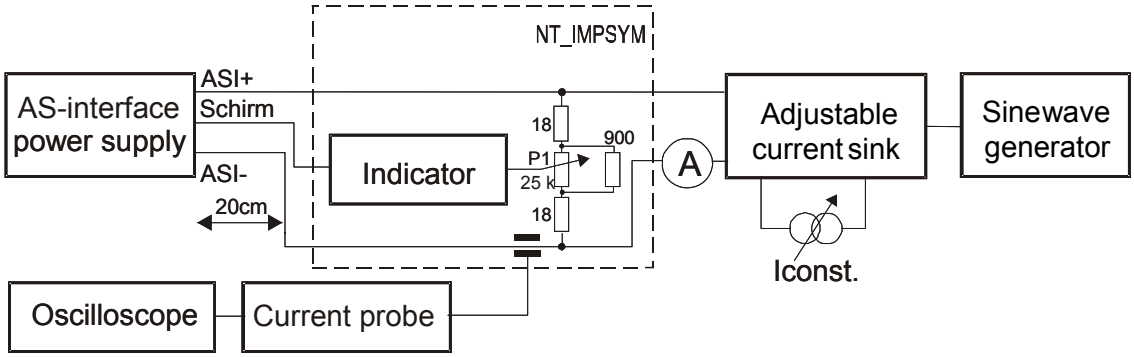


Figure 64 – Test set-up for symmetry measurement

The circuits of the used adjustable current sink and the indicator correspond to those of the test instruction: impedance for AS-i power supplies.

9.3.2.3 Measuring and test equipment

This shall include:

- sine wave generator;
- current meter;
- oscilloscope with current probe;
- adjustable current sink (test circuit: NT_MODSENKE, Figure 61);
- indicator (potential-free peak detector, test circuit: NT_IMPSYM, Figures 62 and 63).

9.3.2.4 Test procedure

The following steps shall be taken:

1. Establish the measurement set-up according to Figure 64, taking into account additional resistive loads (0,1 A at U_{ASI} as well as I_E) of the voltage output not under test, for non-standard AS-i power supplies.
2. By means of the adjustable current sink, adjust output currents of 0,1 A or I_E, respectively, and a modulation amplitude of the current sink of 300 mA_{pp} ± 10 % (check by means of an oscilloscope) at 50 kHz.
3. Align the bridge circuit on the potentiometer (range: −2 % to +2 %), checking at the same time the minimum display on the indicator.
4. Repeat items 2 and 3 at various frequencies up to 300 kHz.

9.3.2.5 Evaluation of the results

With the bridge circuit, cf. Figure 64, verify on potentiometer P1 (adjusting range ±2 %, corresponding to the required tolerance limit for the symmetry) at both output currents (0,1 A and I_E) and at all measurement frequencies (50 kHz to 300 kHz, modulation amplitude 300 mA_{pp}) the adjustability to the indicator minimum.

9.3.3 Noise emission

9.3.3.1 General

The test instruction allows to verify the noise emission of an AS-i power supply in steady state in the specified nominal-load range of 0,1 A ... I_E under laboratory conditions. It is checked whether the required tolerance limit is observed.

9.3.3.2 Test circuit

Figure 65 shows the necessary measurement set-up. For dual or combination power supplies, load the power supply which is not being tested by means of a resistive load first with 0,1 A and then with I_E / I_{max}. Using the adjustable current sink, see 9.3.3.1 (test instruction: impedance), vary the output current at the power supply to be tested between 0,1 A and I_E, determined by means of an oscilloscope in operating mode. Turn peak detection on, with a limit frequency > 10 MHz, the noise voltage between connections ASI+ and ASI− at the power supply in the frequency range of 0 Hz (d.c.) to 500 kHz. Operate the oscilloscope by means of an isolation transformer to avoid earth circuits, or by a battery. For measuring, split the frequency range into 2 partial ranges (0 Hz to 10 kHz and 10 kHz to 500 kHz) by interposing filters. Figures 66 and 67 show the circuits of the used filters. The measurement shall be made with an accuracy of 5 %.

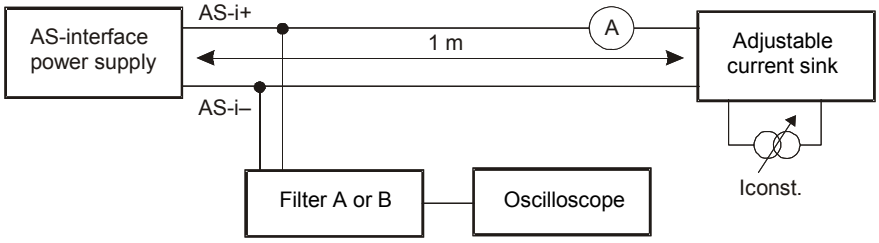


Figure 65 – Test circuit for noise emission

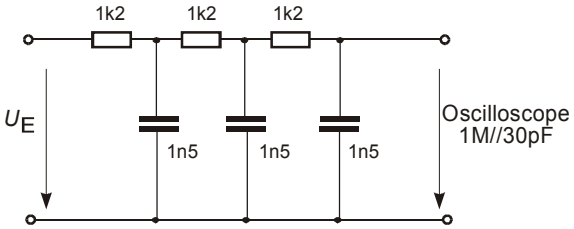


Figure 66 – Filter A (low-pass filter 0 Hz to 10 kHz)

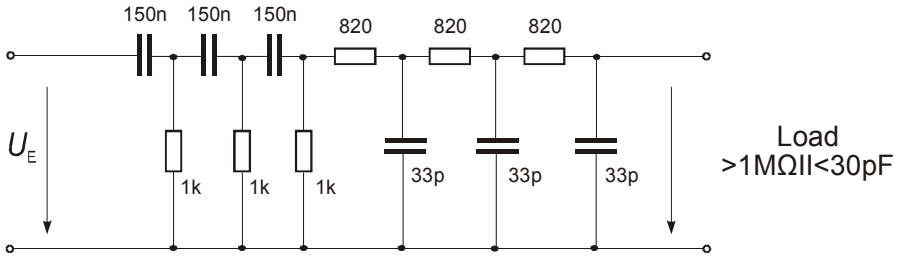


Figure 67 – Filter B (bandpass filter 10 kHz to 500 kHz)

9.3.3.3 Measuring and test equipment

This shall include:

– current meter;
– oscilloscope;
– isolation transformer or accumulator for oscilloscope;
– adjustable current sink (test circuit: NT_MODSENKE, Figure 61);
– filters A and B;
– resistive load.

9.3.3.4 Test procedure

The following steps shall be taken:

1. Establish the measurement set-up according to Figure 60.
2. For dual or combination power supplies, adjust on the power supply which is not being tested, with a resistive load, first 0,1 A and then I_E / I_{max}.
3. By means of the adjustable current sink, vary the output current on the power supply being tested between 0,1 A and I_E as a "ramp function" without modulation.

4. Doing so, check the noise emission between ASI+ and ASI− one by one in both frequency ranges, using filter A (0 Hz to 10 kHz) and filter B (10 kHz to 500 kHz), in the entire output current range.

9.3.3.5 Evaluation of the results

The noise emission between ASI+ and ASI−, in the entire output current range in the frequency range of 0 Hz to 10 kHz, shall not exceed the level of 300 mV_{pp} as well as in the frequency range of 10 kHz to 500 kHz, the level of 50 mV_{pp}.

9.3.4 Power-on behaviour

9.3.4.1 General

The test instruction allows to verify the power-on behaviour (time of readiness for service) of an AS-i power supply under maximum load of I_E under laboratory conditions. It is checked whether the required tolerance limits are observed.

9.3.4.2 Test circuit

Figure 68 shows the necessary measurement set-up. Determine by means of an oscilloscope the rise of the AS-i voltage after switch-on of the power supply under load (15 mF and I_E (according to documentation) of the current sink) according to Figure 68. For dual power supplies, each AS-i output has to be wired with 15 mF and the current sink. Load the AS-i power supply output not being tested in each case via the current sink with 0,1 A or I_E. For combination power supplies load the auxiliary power output with a resistive load (0,1 A or maximum load (I_{max}) according to documentation). The measurement shall be performed with an accuracy of 5 %.

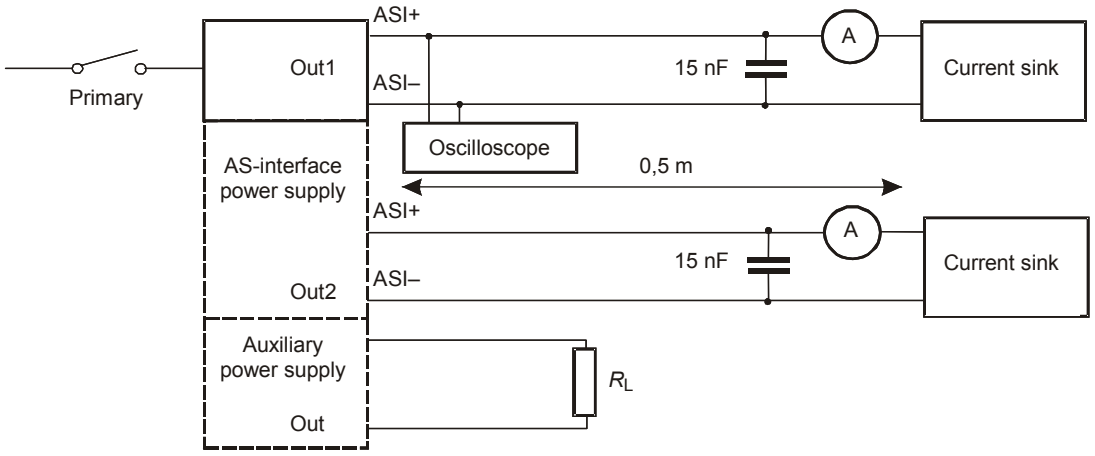


Figure 68 – Test circuit for start-up behaviour

9.3.4.3 Measuring and test equipment

This shall include:

- current meter;
- oscilloscope;
- adjustable current sink (NT_MODSENKE);
- electrolytic capacitor 15 mF;
- load resistor R_L.

9.3.4.4 Test procedure

The following steps shall be taken:

1. Establish the measurement set-up according to Figure 60.
2. Adjust the current sink on the switched-on AS-i power supply to be tested in stationary state to the output current I_E of the test sample.
3. Wire the power supply branch not being tested of dual or combination power supplies with 0,1 A and, in a second test, with maximum load (current sink or R_L).
4. Switch the power supply off.
5. Switch the power supply on and record the AS-i voltage waveform.

9.3.4.5 Evaluation of the results

The AS-i voltage shall rise within 2 s from 5 V to 26,5 V (min. master voltage of 23,5 V plus maximum line voltage drop of 3 V). Furthermore, the time difference between 21,5 V and 29,5 V shall not exceed 1 s. The voltage increase shall be continuous.

9.4 Test of an AS-i repeater and other components

9.4.1 Impedance

9.4.1.1 General

This test determines the impedance of the test sample in "operative state".

9.4.1.2 Test circuit

Figure 69a shows the test circuit for the impedance measurement with an impedance analyzer, alternatively Figure 69b shows the conventional test circuit with the oscilloscope.

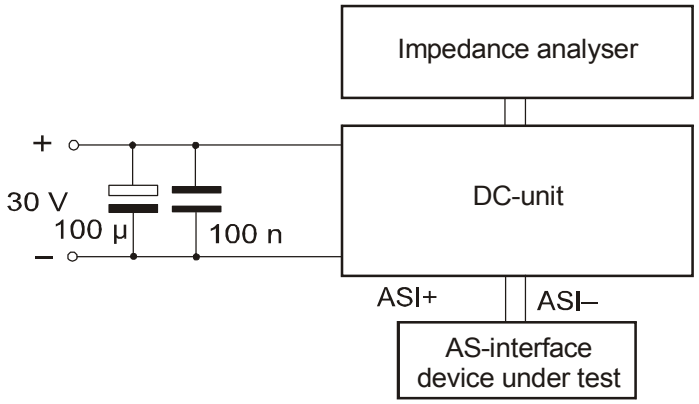


Figure 69a – Impedance analyzer

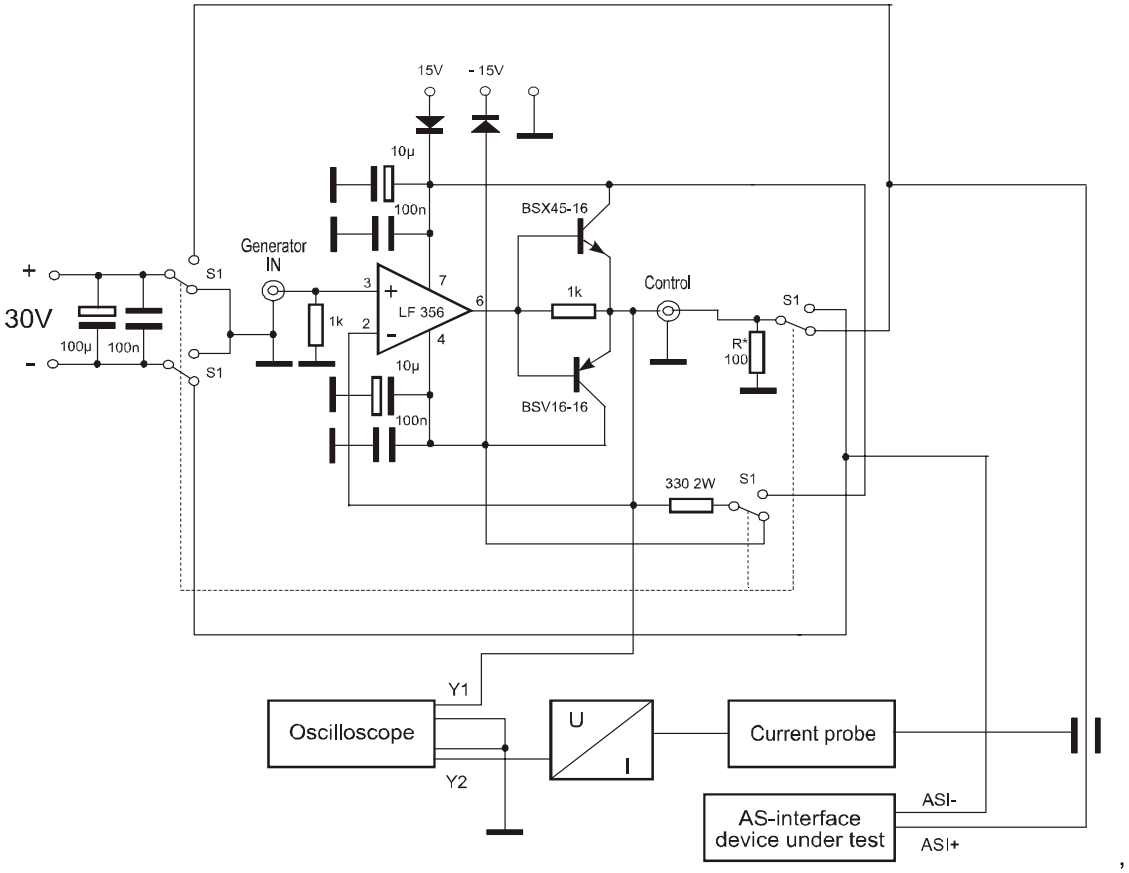


Figure 69b – Oscilloscope, current probe and sine wave generator

Figure 69 – Measurement set-up for impedance measurement

The operation of the test sample in switch position "Measurement" is deliberately asymmetrical, i.e. metallic parts of the test sample must not be grounded. With switch S1 (Figure 69b), the a.c. grounding can be switched over(switch position in the drawing: ASI− = GND (grounding)). Measure the input a.c. current with the current probe. The length of the AS-i line between test sample and measurement circuit shall be 20 cm maximum.

The amount of the input impedance is calculated as follows: | *Z* | = | *U*~ | / | *I*~ |

9.4.1.3 Measuring and test equipment

This shall include:

a) with an impedance analyzer:
   - power supply,
   - impedance analyzer with d.c. unit;

b) with an oscilloscope (alternative):
   - power supply,
   - sine wave generator,
   - current probe,
   - oscilloscope,
   - test circuit according to Figure 69b;

c) for d.c. resistance:

– d.c. R-meter (Wheatestone brigde).

9.4.1.4 Test procedure

The following steps shall be taken:

impedance:

a) with an impedance analyzer:
   – connect the test sample on the impedance analyzer via the dc-unit,
   – measure the input impedance for frequencies of 50 kHz, 100 kHz, 125 kHz, 150 kHz, 175 kHz, 200 kHz, 250 kHz and 300 kHz. If at one of the test frequencies the test sample has a resonant frequency, the test frequency shall be varied ±10 kHz;
b) with an oscilloscope:
   – overlay the AS-i d.c. voltage with an a.c. voltage signal U~ with Ri ≤ 1 Ω. Measure this a.c. voltage and the resulting a.c. current flowing through the test sample,
   – switch S1: position "ASI- = GND", cf. Figure 69b,
   – measurement of a.c. *I*~ at *U*~ = 6 Vpp for frequencies of 50 kHz, 100 kHz, 125 kHz, 150 kHz, 175 kHz, 200 kHz, 250 kHz and 300 kHz. If at one of the test frequency the test sample has resonant frequency the test frequency shall be varied ±10 kHz;

d.c. resistance:

– measure the d.c. resistance between ASI+, ASI− and all metallic parts of the test sample, except external connections. Measuring conditions: $R \geq 1$ MΩ.

9.4.1.5 Evaluation

9.4.1.5.1 Input impedance

Reproduce the input impedance |*Z*| by means of an equivalent circuit from a parallel circuit of *R*, *L*, and *C*. |*Z*| is calculated as follows:

$$|Z| = \frac{1}{\sqrt{\frac{1}{R^2} + \left(\omega C - \frac{1}{\omega L}\right)^2}}$$

Table 20 (8.4.4.4) indicates the limit values of the impedance wave form for a slave equivalent.

The limit values of the slave equivalents according to documentation are calculated from the series circuit (< 1 slave equivalent) or parallel circuit (> 1 slave equivalent) of equivalent circuits.

The impedance waveform (measured slave equivalents) must be higher than the “slave equivalents“ indicated in the manufacturer's documentation, i.e. measured slave equivalents < slave equivalents according to documentation.

9.4.1.5.2 DC resistance

The d.c. resistance between ASI+, ASI− and all metallic parts of the test sample, except external connections, shall be ≥ 250 kΩ.

9.4.2 Symmetry

9.4.2.1 General

This test determines the symmetry of an AS-i component without separate communication when operating.

9.4.2.2 Test circuit

Figure 70 shows the test circuit for the symmetry measurement.

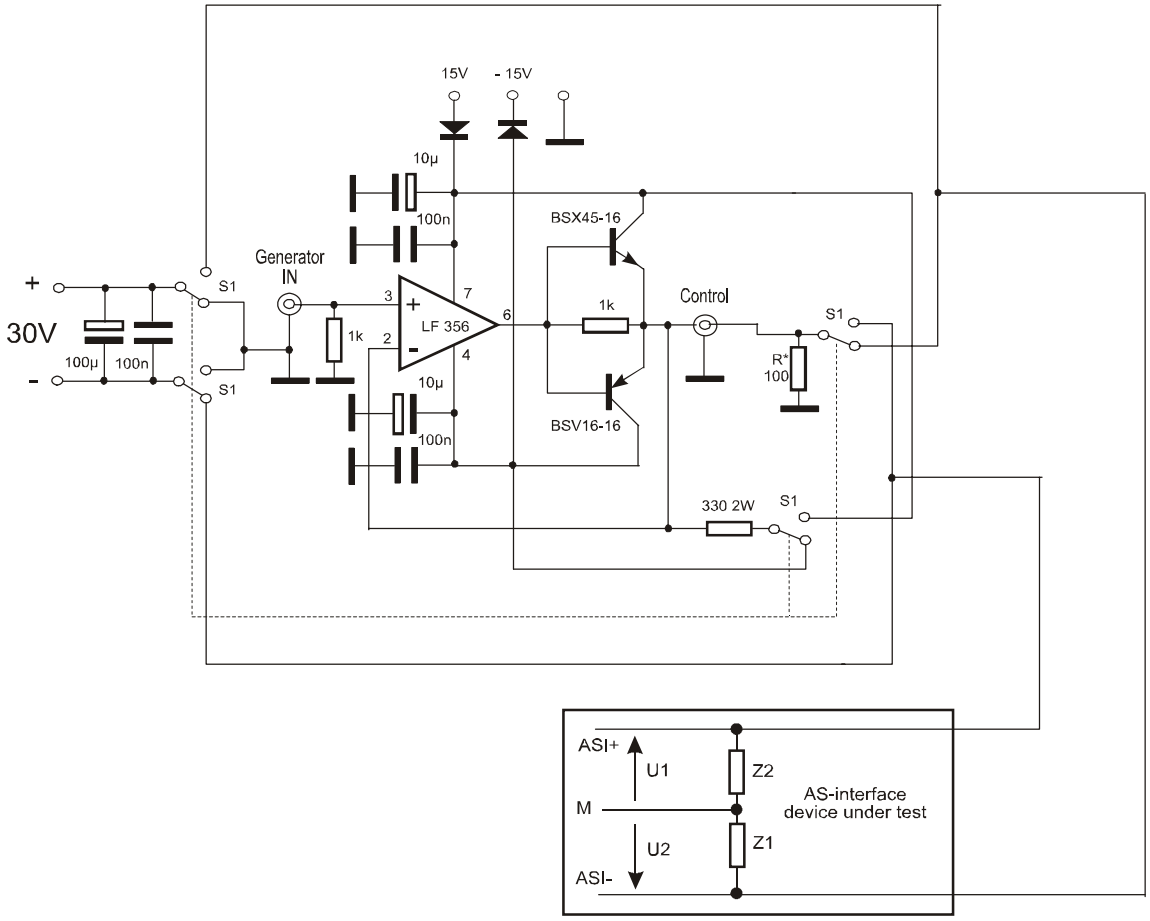


Figure 70 – Test circuit for symmetry measurement

The partial impedances Z_1 and Z_2, respectively, form in the measurement point M (grounding connection) a voltage divider.

In unloaded state, identical currents flow through Z_1 and Z_2.

With 10 % asymmetry, the following results:

$$0{,}90 \leq \frac{\left|\vec{U}_1\right|}{\left|\vec{U}_2\right|} = \frac{|Z_1|}{|Z_2|} \leq 1{,}10$$

$\vec{U}_1$: Voltage between M and ASI+ at ASI+ = GND

$\vec{U}_2$: Voltage between M and ASI- at ASI- = GND

9.4.2.2.1 Test circuit details

1: galvanic coupling between ASI+ (ASI−) and the measurement point M (d.c. resistance ≤ 250 kΩ)

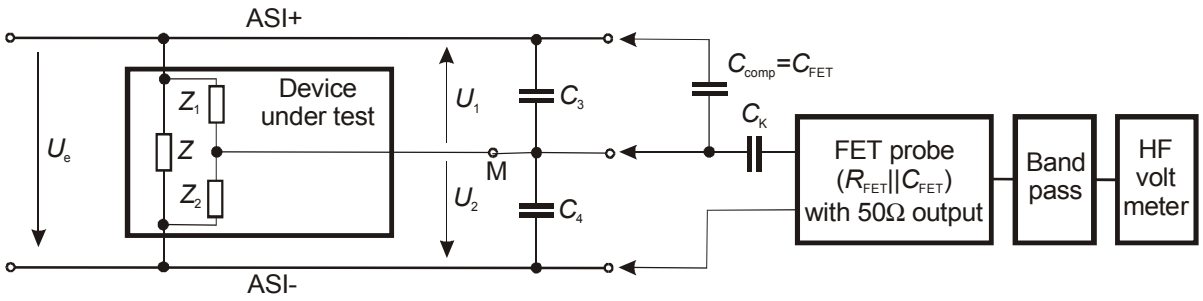


Figure 71 – Test circuit (detail 1)

2: electrical isolation between ASI+ (ASI−) and the measurement point M (d.c. resistance > 250 kΩ)

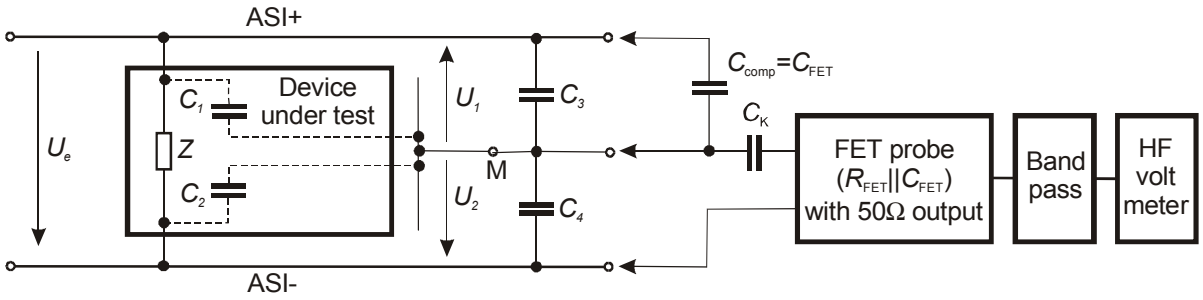


Figure 72 – Test circuit (detail 2)

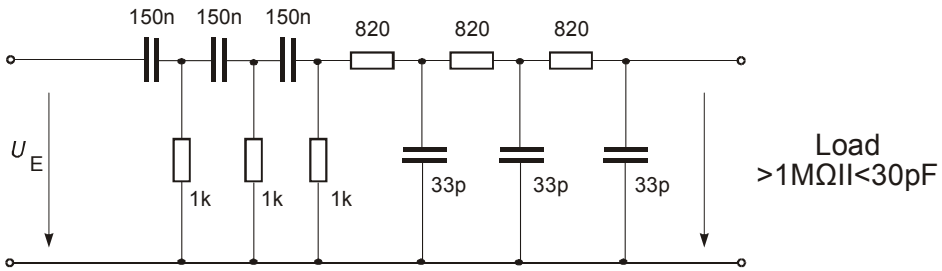


Figure 73 – Bandpass (10 kHz ... 500 kHz)

9.4.2.3 Measuring and test equipment

This shall include:

- AS-i master;
- oscilloscope;
- FET probe with 50 Ω line impedance;
- bandpass;
- HF voltmeter;
- capacitor C_S = 30 pF.

9.4.2.4 Test procedure

The following steps shall be taken:

The measurement set-up corresponds to that of the impedance measurement (cf. Figure 69b). Measure, according to Figures 70 to 72, the voltage drops U_1 between ASI+ and M, and U_2 between ASI− and M, using an FET probe (R_i = 1MΩ||2pF) with a.c. coupling $C_k \geq 1$ nF and an HF voltmeter (frequency range up to 300 kHz, R_i = 10 MΩ||30 pF). To compensate the probe capacity, take into account the capacity $C_{comp} = C_{FET}$ in the circuit. Terminate the FET probe with an output impedance of 50 Ω.

Any measuring error of the HF voltmeter in the higher frequency range is eliminated by forming the ratio $|U_1| / |U_2|$.

– Measurement voltage is 2,0 V_{rms}

– External capacitor for symmetry test C_S = 30 pF.

– Symmetry test procedure has to be performed at frequencies of 50 kHz, 100 kHz, 150 kHz, 200 kHz, 250 kHz and 300 kHz.

9.4.2.5 Evaluation

The symmetry test is passed if the test procedure (Figure 74) is finished with “Symmetry OK” for each test frequency.

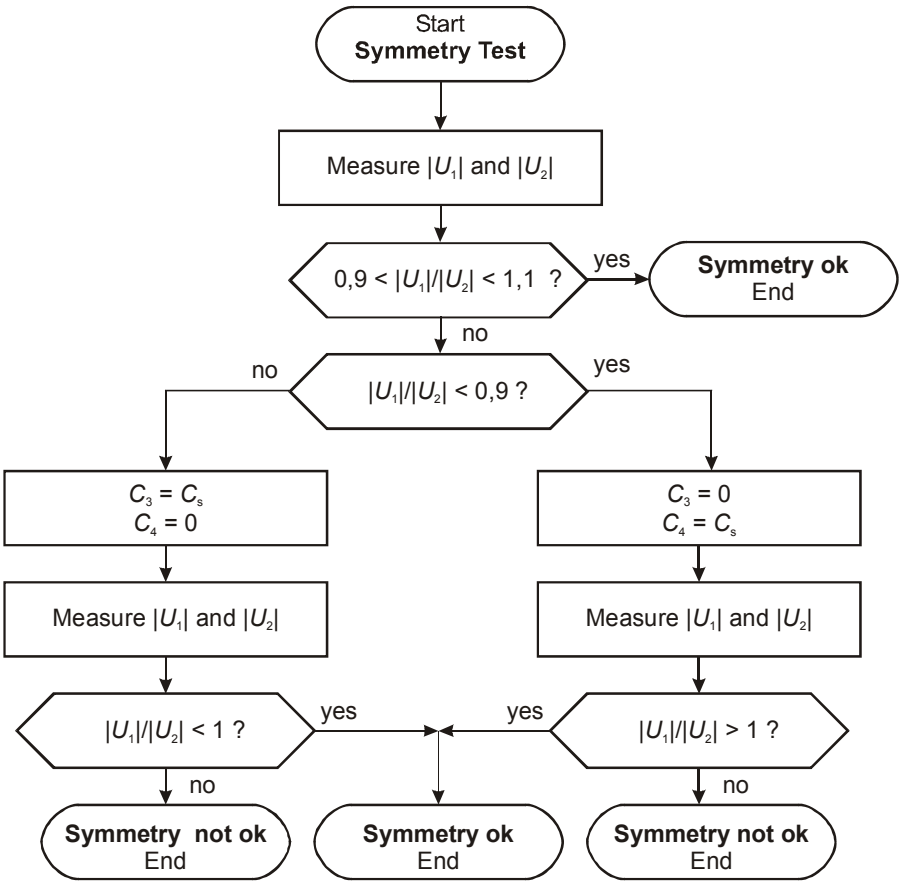


Figure 74 – Procedure for symmetry test

9.4.3 Coexistence in AS-i networks

9.4.3.1 General

The purpose of the operation on a reference network is to find out whether an AS-i earth-leakage detector or another component without separate communication is liable to disturb the error-free communication of an AS-i network.

9.4.3.2 Test circuit

Figure 75 shows the test circuit (schematic diagram) for the interoperability test for earth-leakage detectors and other components without separate communication in AS-i networks. For repeater refer to modified test circuits according to Figures 76 and 77.

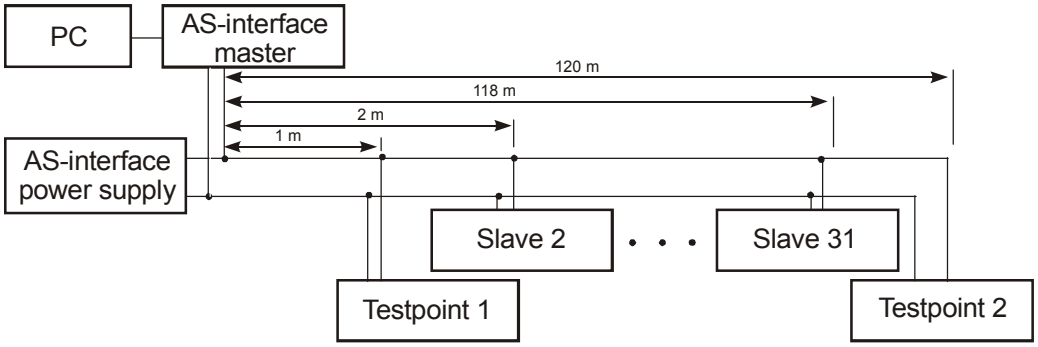


Figure 75 – Test circuit for interoperability in AS-i networks

The AS-i reference network consists of 120 m AS-i cable (type: EPDM), to which are connected (at the master node)

– an AS-i master,

– an AS-i power supply.

Every 4 m, starting at 2 m from the master node, connect a slave (30 slaves). At a distance of 1 m from the master node, there is measurement point 1, at 120 m from the master node, there is measurement point 2, to which the test sample being tested is connected one after the other.

9.4.3.2.1 Test conditions

All components connected to the network shall be certified AS-i components. If possible, use different types of slaves. If no certified products are available, you can also use products corresponding to the respective valid specifications.

Between master, power supply, slaves and the AS-i line, short connection lines (max. 30 cm) are admissible.

Evaluate the error rate, i.e. the number of AS-i messages registered as communication errors, referred to the total number of AS-i messages.

If during the period of observation, the master eliminates a slave from the LAS, abort the test with the result "not passed".

Minimum observation time: 1 min (at least 10 000 calls per slave).

9.4.3.2.2 Modified test circuit for repeater

Based on the reference network according to Figure 75 the following additional tests for repeater shall be performed:

a) repeater with single slave and power supply connected to test point 1 according to Figures 75 and 76;

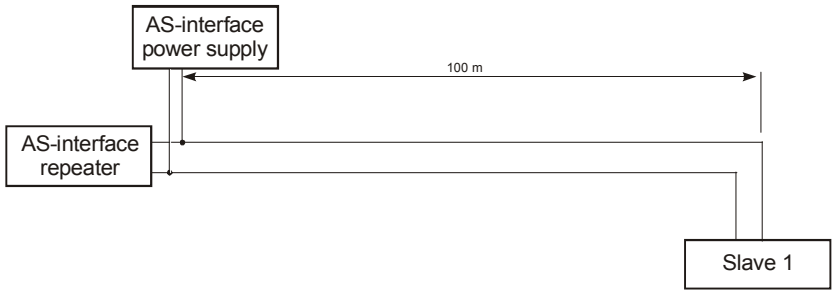


Figure 76 – Additional test circuit 1 for repeater

b) repeater with single slave and power supply connected to test point 2 according to Figures 75 and 76;

c) repeater with master and power supply connected to test point 1 according to Figures 75 and 77. The master in the network defined in Figure 75 is removed for this test.

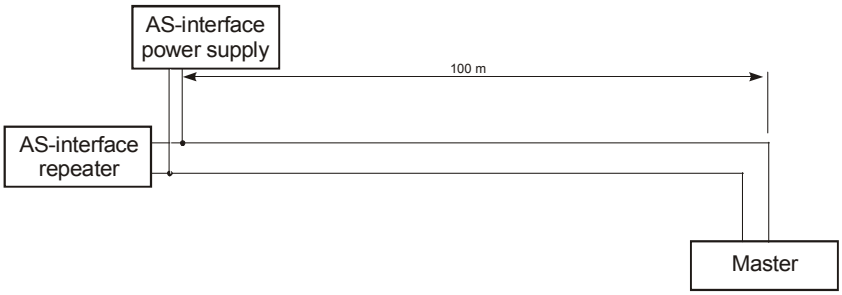


Figure 77 – Additional test circuit 2 for repeater

9.4.3.3 Measuring and test equipment

This shall include:

– EMC-Tool (AS-i master with test software;

– PC;

– 31 standard slaves, (alternatively: 31 A/B slave pairs or mixed standard and A/B slaves with all possible addresses);

– one or two AS-i power supplies.

9.4.3.4 Test procedure

The following steps shall be taken:

a) operate the reference network without the test sample being tested. Measure error rate 1 (total number of error rates of slaves No. 1 to 31, referred to the total number of calls made to these slaves);

b) connect the test sample being tested at measuring point 1. Measure error rate 2 caused by the test sample being tested (total number of errors of slaves No. 1 to 31, referred to the total number of calls made to these slaves);

c) connect the test sample being tested at measuring point 2. Measure error rate 3 caused by the test sample being tested (measurement like under item 2.);

d) repeat steps 2 and 3 with reversed connection of the test sample being tested;

e) for repeater: use the modifications in the test circuits and test in the same way.

9.4.4 Evaluation

For all measurements, only one error during the test time (at least 1 min) is admissible.

9.5 Test of an AS-i slave

9.5.1 Logical behaviour, current consumption and test of total current consumption under short-circuit condition on slaves with external ports

9.5.1.1 General

This test determines the profile of an AS-i slave and the some additional requirements as stated in the slave profiles, the limits of the operating voltage, the measurement of the maximum current consumption of the AS-i slave and test the total current consumption under short-circuit condition in those slaves which have external input or output ports.

9.5.1.2 Test circuit

The slave shall be connected to the test system as shown in Figure 78 and Figure 79:

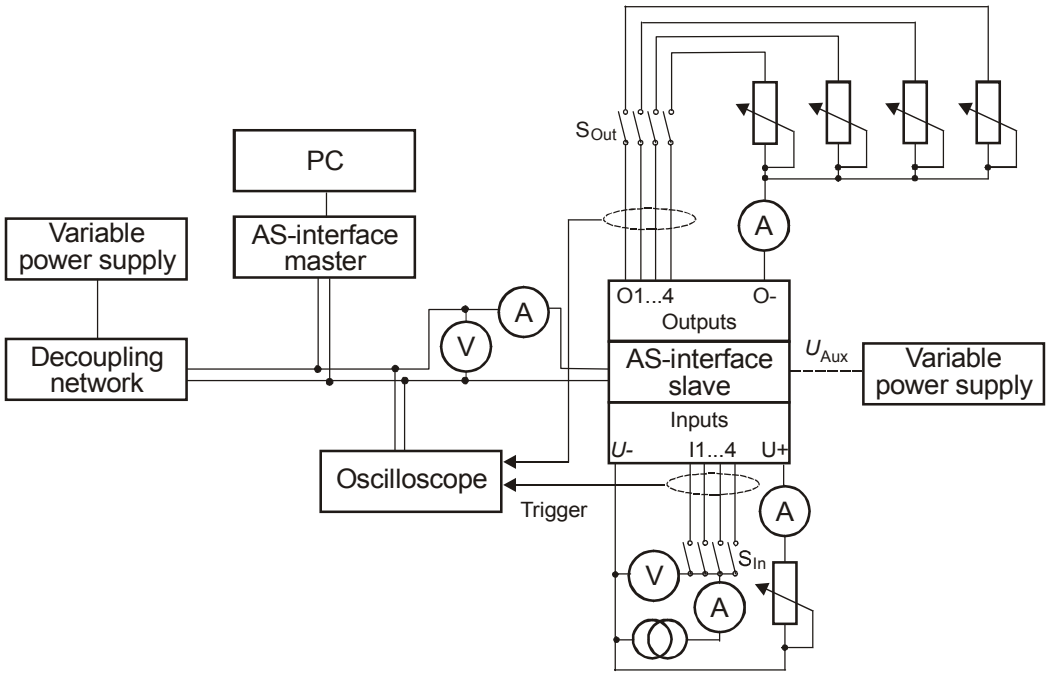


Figure 78 – Test circuit

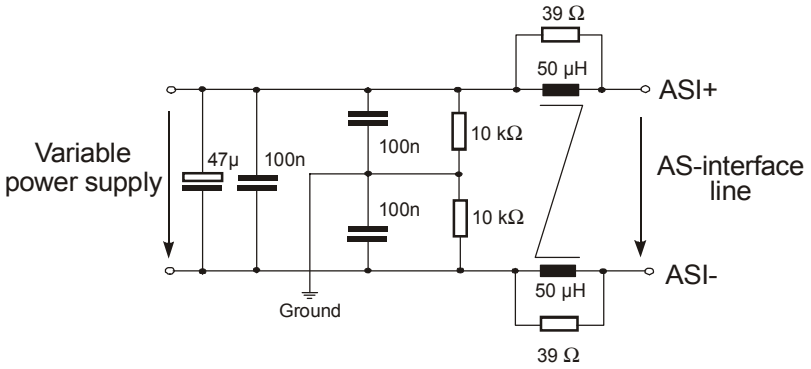


Figure 79 – Test circuit decoupling network

9.5.1.3 Measuring and test equipment

This shall include:

– variable power supply;
– decoupling network;
– AS-i master;
– oscilloscope;
– multimeters;
– variable resistors;
– PC.

9.5.1.4 Test procedure

The following steps shall be taken:

- the master shall issue the I/O code, the ID code, the ID2 code and the easily accessible messages as described in the defined slave profiles (see Annex A) or in the documentation (for free profiles, e.g. ID=F_{Hex} or ID=A_{Hex}; ID2=E_{Hex}). The correctness of the slave response shall be tested at the following voltages:

– 31,6 V, 26,5 V and the minimum voltage stated by the manufacturer at which the slave still functions;

- the voltage shall be measured near to the slave. If external loads of the slave are supplied by the AS-i line, they shall be connected at the maximum current as allowed according to the documentation (I/O-Ports: Inputs high or low. Outputs high or low; U_{out} with I_{max});
- the current at the AS-i line shall be measured under communication with all messages in the logical test beginning at U = 31,6 V down to the minimum voltage stated by the manufacturer at which the slave still functions correctly.

If the load current at the external ports is drawn from the AS-i line, the current has to be increased and measured continuously until short-circuit.

9.5.1.5 Evaluation of test results

The test is successful

– if the slave is working at all tested voltages;
– if the slave is communicating at all tested voltages;
– if the slave answers correspond to the stated slave profile;
– if the behaviour of the LEDs corresponds to this standard;

– the current shall be not greater than the maximum current stated by the manufacturer, and

– under overload or short-circuit conditions at all the terminals of a slave, the total current consumption from the AS-i line shall not exceed the total current consumption stated by the manufacturer plus 150 mA.

9.5.2 Noise emission

9.5.2.1 General

This test determines the emissions of an AS-i slave into the AS-i network in the steady-state operation of the slave.

9.5.2.2 Test circuit

The test shall be performed with the AS-i slave connected to a test circuit as shown in Figure 80. The inputs and/or outputs of the AS-i slave shall be connected to their nominal load. If the slave normally switches off some loads during the test because of its watchdog function, the manufacturer shall provide an especially prepared slave, for example deactivated watchdog, for a proper measurement.

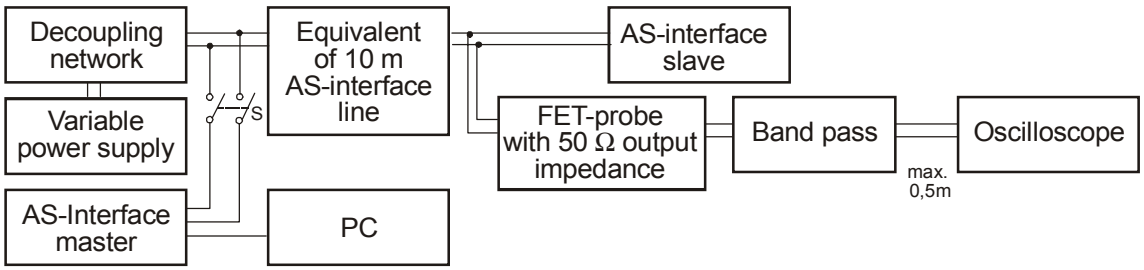


Figure 80 – Test circuit

The decoupling network used in Figure 80 shall have the same characteristics as the circuit shown in Figure 81.

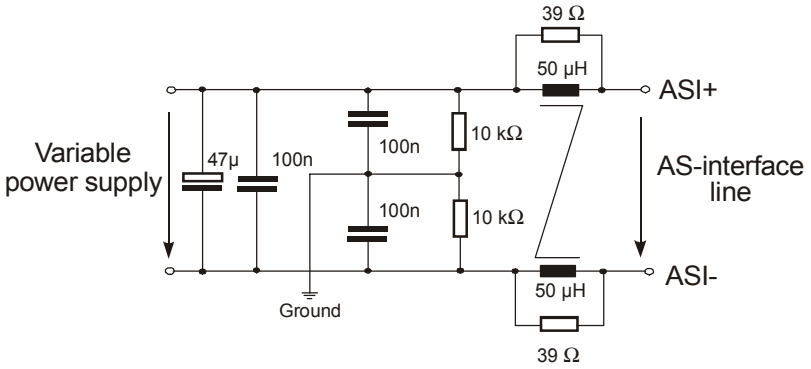


Figure 81 – Test circuit decoupling network

The equivalent of 10 m AS-i line used in Figure 80 shall have the same characteristics as the circuit shown in Figure 82.

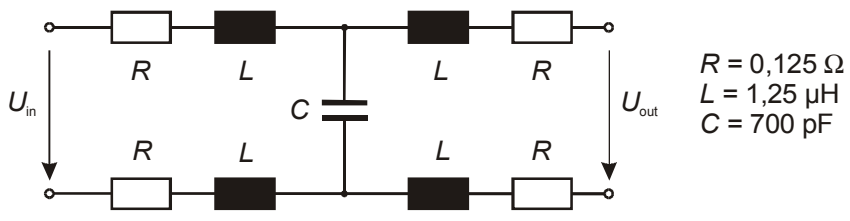


Figure 82 – Test circuit (equivalent of 10 m AS-i line)

The bandpass filter used in Figure 80 shall have the same characteristics as the circuit shown in Figure 83.

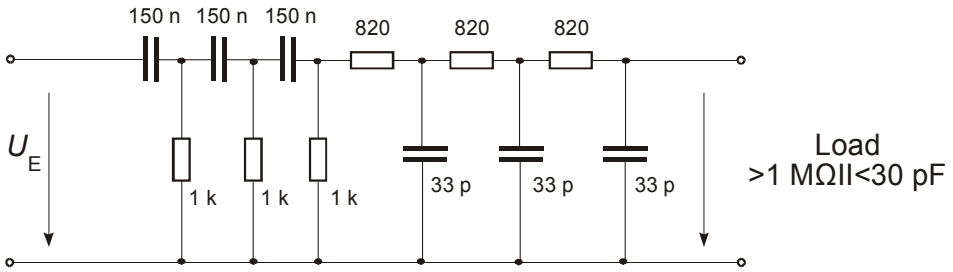


Figure 83 – Test circuit (bandpass 10 kHz to 500 kHz)

9.5.2.3 Measuring and test equipment

This shall include:

- variable power supply;
- decoupling network;
- equivalent of 10 m AS-i line;
- bandpass;
- oscilloscope;
- FET-probe;
- 50 Ω line impedance;
- PC;
- optional: AS-i master.

9.5.2.4 Test procedure

The following steps shall be taken:

a) if the parameter and/or data bit combination of the slave influence the noise behaviour of the slave, set the combination with the maximal noise by the master. The watchdog shall be disabled for this test if the data outputs influence the noise behaviour;

b) after the slave configuration, disconnect the master from the AS-i line;

c) the emissions shall be determined with and without the AS-i slave connected between $U_{ASI} = U_{min}$ to 31,6 V (U_{min} as defined in the documentation).

9.5.2.5 Evaluation of test results

The difference of the emitted interference between ASI+ and ASI− measured without and measured with the AS-i slave connected to the AS-i line shall not exceed 20 mV_{pp}.

9.5.3 Power-on behaviour

9.5.3.1 General

This test determines the power-on behaviour of an AS-i slave in the AS-i network.

9.5.3.2 Test circuit

All AS-i slave inputs or outputs shall be connected with their rated load. Test with constant current source with I = (I stated by the manufacturer +12,5 mA for standard slaves, +6,5 mA

for A/B-slaves in extended address mode). No monitoring of communication is possible, because the current source prevents the communication.

The test shall be performed with the AS-i slave connected to a test circuit as shown in Figure 84 and Figure 85.

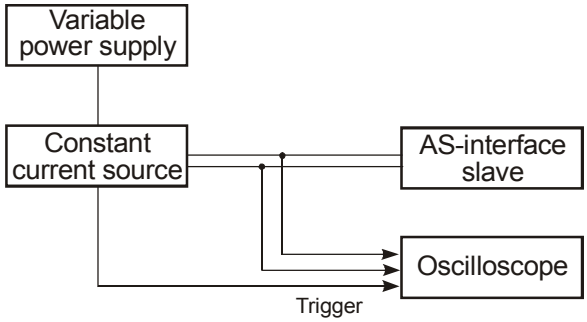


Figure 84 – Test circuit

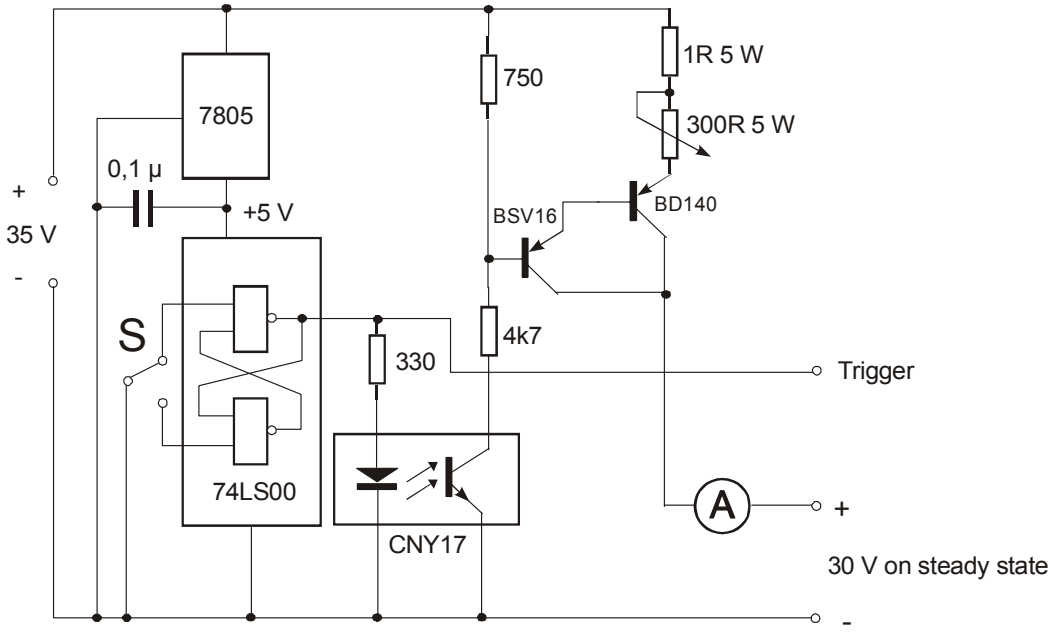


Figure 85 – Constant current source

9.5.3.3 Measuring and test equipment

This shall include:

– variable power supply;
– oscilloscope;
– constant current source.

9.5.3.4 Test procedure

The following steps shall be taken:

– the time t_1 from connecting the AS-i slave to the AS-i line up to the time where the minimum voltage of 26,5 V has been reached shall be determined;
– if the slave has external output ports, the state of these ports shall be monitored.

9.5.3.5 Evaluation of test results

The time t_1 shall be less than or equal to 1 s.

If the slave has external output ports, the default values of these ports shall be kept during the whole power-on procedure.

9.5.4 Impedance

9.5.4.1 General

This test determines the impedance of an AS-i slave when operating.

9.5.4.2 Test circuit

The test shall be performed with the AS-i slave connected to a test circuit shown in Figure 86.

If the slave normally switches off some loads during the test because of its watchdog function, the manufacturer shall provide an especially prepared slave for a proper measurement.

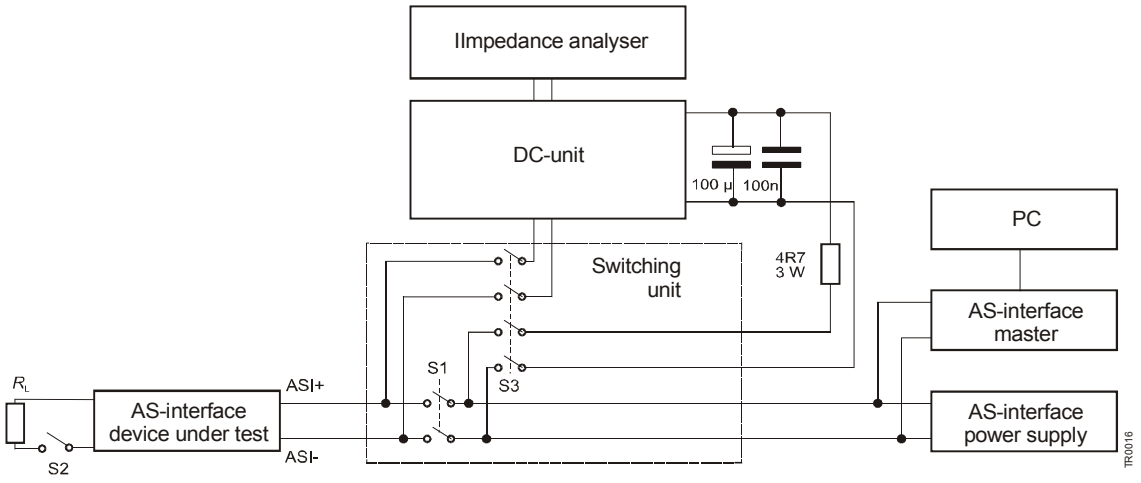


Figure 86a – Test with impedance analyzer

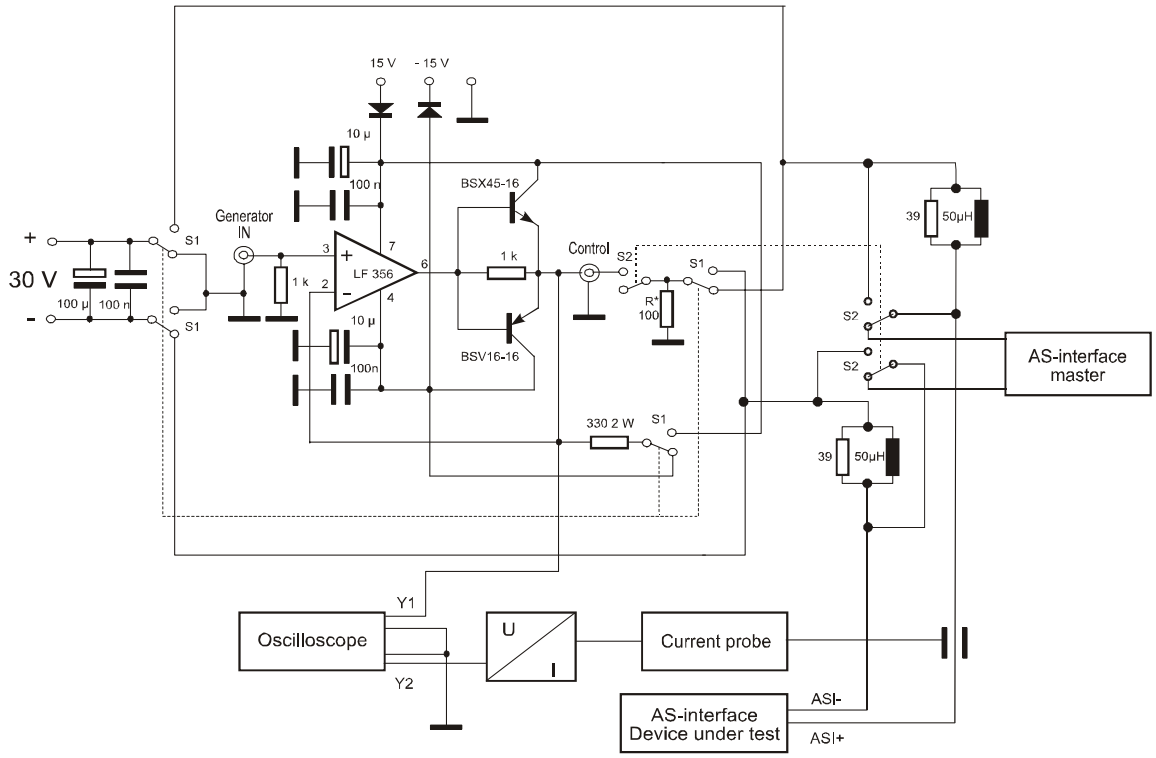


Figure 86b – Test with generator, current probe and oscilloscope

Figure 86 – Test circuit

9.5.4.3 Test procedure

9.5.4.3.1 Test procedure with impedance analyzer (Figure 86a)

The following steps shall be carried out:

a) switch S1: ON, switch S3: OFF;

b) set data and parameter bit combination according to the documentation of the manufacturer to that combination at which the value of the impedance is the minimum and at which the symmetry is the minimum;

c) change switch S3 to ON;

d) change Switch S1 to the position to OFF;

e) close switch S2, if the slave uses power from the AS-i® line to feed a nominal load of I_L;

f) determination of Z (or R_p, L_p, C_p if applicable) with 6 V_{pp} at 50 kHz, 100 kHz, 125 kHz, 150 kHz, 175 kHz, 200 kHz, 250 kHz and 300 kHz. If at one of the test frequencies, the slave has a resonant frequency ,the test frequency shall be varied up to ±10 kHz.

9.5.4.3.2 Test procedure with current probe and oscilloscope (Figure 86b)

A standard d.c. power supply feeds the set-up. Either ASI+ or ASI− can be connected to ground by switch 1. An a.c. sinus signal with an internal resistance of $R_i \leq 1\ \Omega$ shall be superimposed on the AS-i d.c. voltage. The a.c. voltage and a.c. current shall be determined at different frequencies.

Switch S1 allows to provide the AS-i slave either with a the signal from the master (to switch the slave in the desired state) to with the a.c. sinus signal to determine the impedance. For

slaves with external ports, switch S2 allows the maximum load I_L from the AS-i® line according to the documentation of the manufacturer.

The distance between AS-i slave and AS-i master shall be 20 cm. The d.c. resistance between ASI+, ASI− and all metallic parts of the slave (with the exception of the outer connections) shall be ≥ 1 MΩ.

The following steps shall be carried out:

a) switch S1/S2 to position: "Data transmission";
b) set data and parameter bit combination according to the documentation of the manufacturer to that combination at which the value of the impedance is the minimum and at which the symmetry is the minimum;
c) change switch S1/S2 to the position "Impedance measurement";
d) close switch S3, if the slave uses power from the AS-i® line to feed a nominal load of I_L;
e) determination of $|Z|$ with 6 V_{pp} at 50 kHz, 100 kHz, 125 kHz, 150 kHz, 175 kHz, 200 kHz, 250 kHz and 300 kHz. If at one of the test frequencies the slave has a resonant frequency, the test frequency shall be varied ±10 kHz.

9.5.4.4 Evaluation of test results

The d.c. resistance between ASI+, ASI− and all metallic parts of the slave (with the exception of the outer connections) shall be ≥ 1 MΩ.

They shall be within the limit values of this standard for slaves with ID-code = A_{Hex} and ID-code ≠ A_{Hex}, respectively.

9.5.5 Symmetry

9.5.5.1 General

This test determines the symmetry of an AS-i slave when operating.

9.5.5.2 Test circuit

The test shall be performed with the AS-i slave connected to a test circuit having the same characteristics as the test circuit shown in Figure 87.

If the slave normally switches off some loads during the test because of its watchdog function, the manufacturer shall provide an especially prepared slave for a proper measurement.

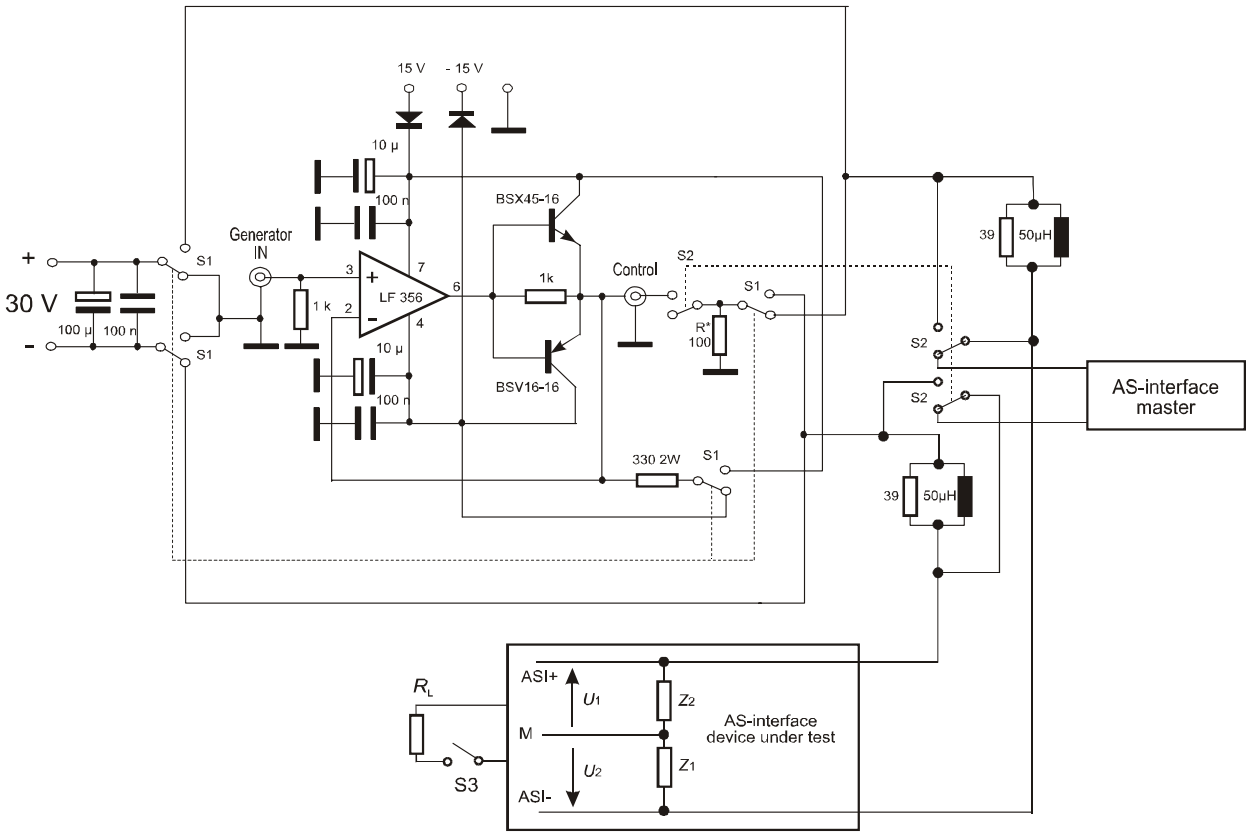


Figure 87 – Test circuit

NOTE For AS-i slaves with external connections the measurement point M should be the galvanically coupled power supply. For AS-i slaves with no galvanically coupled external connections, the measurement point M shall be their metal housing. For AS-i slaves with an insulating package and no galvanically coupled external connections the measurement point M may be the metallic part on which the plastic package is installed.

1: galvanic coupling between ASI+ (ASI−) and the measurement point M (d.c. resistance ≤ 1 MΩ)

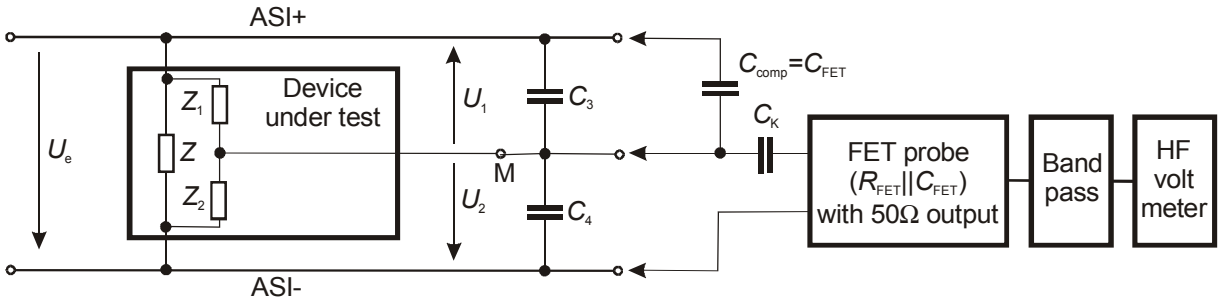


Figure 88 – Test circuit (detail 1)

2: electrical isolation between ASI+ (ASI−) and the measurement point M (d.c. resistance > 1 MΩ)

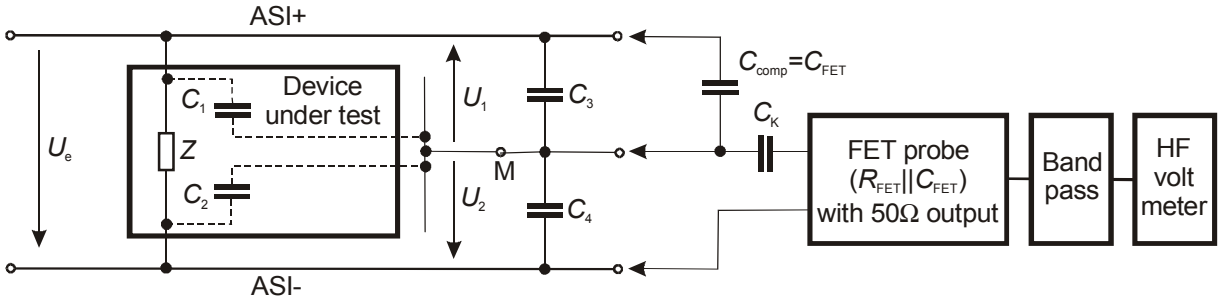


Figure 89 – Test circuit (detail 2)

9.5.5.3 Measuring and test equipment

This shall include:

- AS-i master;
- oscilloscope;
- FET probe;
- bandpass (see Figure 73);
- HF voltmeter;
- capacitor C_S = 30 pF / 15 pF; (standard slaves / A/B slaves).

9.5.5.4 Test procedure

The following steps shall be taken:

a) measurement voltage is 2,0 V_{rms};

b) external capacitor for symmetry test C_S = 30 pF for standard slaves and C_s = 15 pF for extended addressing mode slaves;

c) symmetry test procedure has to be performed at data and parameter combination with minimum impedance and worst case symmetry;

d) symmetry test procedure has to be performed at frequencies of 50 kHz, 100 kHz, 150 kHz, 200k Hz, 250 kHz and 300 kHz.

9.5.5.5 Evaluation

The symmetry test is passed if the test procedure (Figure 90) is finished with “Symmetry OK” for each test frequency.

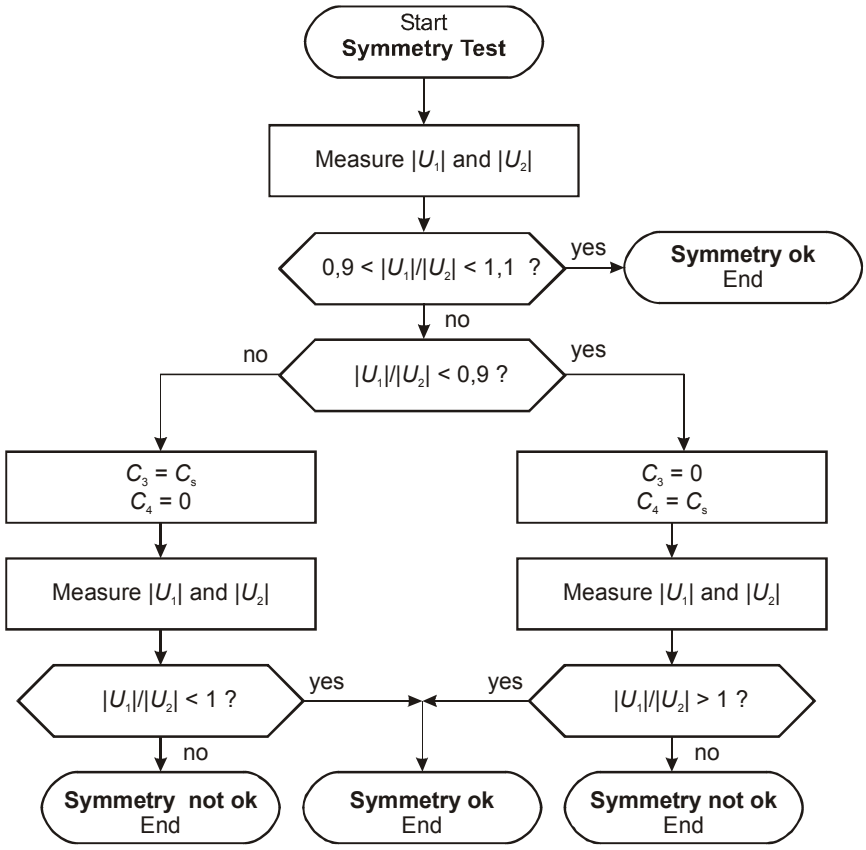


Figure 90 – Procedure for symmetry test

9.5.6 Interoperability in AS-i networks

9.5.6.1 General

This test determines the interoperability of the slave in AS-i networks.

9.5.6.2 Test circuit

The tests shall be performed in an AS-i network as shown in Figure 91. The master used shall be able to communicate in the extended address mode. The slaves 2 to 31 shall be standard slaves (ID ≠ A_{Hex}), pairs of slaves in extended address mode (A/B-slaves with ID = A_{Hex}) or a mix of standard slaves and pairs of extended address mode slaves. All components should be connected directly to AS-i main line. If this is not possible, the maximum length of the stub lines shall be less than 30 cm. All components in the AS-i network shall be certified.

Slave under test shall be connected first at testpoint1 (TP1) to the network and thereafter at testpoint 2 (TP2). If the slave under test has the ID-Code "A_{Hex}" two samples shall be used as A/B-slaves at TP1 and TP2, respectively.

It shall be made possible to switch the slave under test and some of the other slaves in the network from outside (for sensor functions) and from the master (for actuator functions). A slave under test with external ports shall be connected to its nominal loads.

For monitoring purposes, a test software shall be used in the AS-i master that allows to count each single repetition of a telegram.

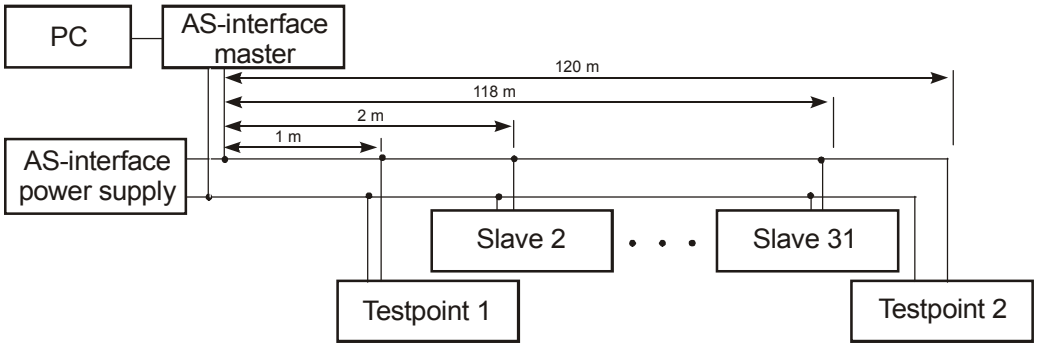


Figure 91 – Test circuit AS-i network

9.5.6.3 Measuring and test equipment

This shall include:

- AS-i master;
- AS-i power supply;
- PC with test software;
- reference network.

9.5.6.4 Test procedure

The following steps shall be taken:

a) error rate of slave under test:
   - measure error rate of slave under test at TP1 and TP2,
   - measure error rate slave 2 to 31;

Measure the error rate of slave 2 to 31 under following conditions:

b) error rate of AS-i network after having connected the slave under test in wrong polarity;

c) error rate of AS-i network after short-circuiting the external slave connections (if applicable);

d) error rate of AS-i network with overload current on external slave connections (if applicable).

The tests a) shall be conducted with a minimum of 10 switching actions of easily accessible functions of the slave under test. The tests a) to d) shall have a minimum duration of 1 min.

9.5.6.5 Evaluation of test results

The error rate in test a) shall be less than or equal to 1 error per 10 switching actions, The error rate in tests b) to d) less than or equal to 1 error /min.

9.5.7 Additional test for safety related slaves (profile S-X.B)

9.5.7.1 General

This test checks the correctness of the implemented safety code table.

9.5.7.2 Test circuit

Figure 2 shows the test set-up in principle.

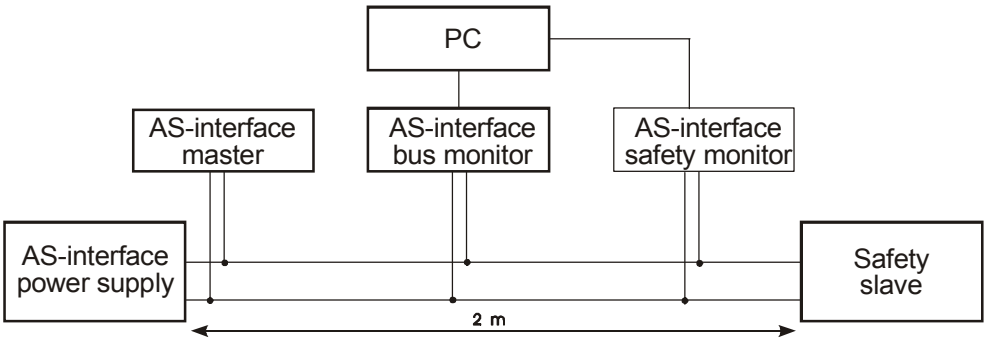


Figure 92 – Test circuit for safety related slaves

9.5.7.3 Measuring and test equipment

This shall include:

– AS-i power supply;
– AS-i master;
– AS-i bus monitor (analyzer);
– AS-i safety monitor;
– PC with test software.

9.5.7.4 Test procedure

The following steps shall be taken:

- the behaviour of the slave regarding the safety code table is checked by means of a bus monitor and by teaching this code table of a safety monitor.

9.5.7.5 Evaluation of test results

All tests shall be conform to this standard.

A teaching of a safety monitor must be possible.

A printout of the monitor recording shall be enclosed to the protocol in case of a fault.

9.5.8 Additional test for slaves supporting combined transactions

This test shall verify that the data exchange, timing requirements and error handling are conform to the specification of 5.7.

9.5.9 Verification of the electromagnetic compatibility

9.5.9.1 Test conditions

Unless otherwise stated, the tests shall be carried out at an ambient air temperature of 23 °C ± 5 °C.

The tests shall be performed under the following conditions:

a) the AS-i device mounted in free air shall be connected to the AS-i line and supplied with its rated operational voltage (U_e); Terminals and connectors if any, shall be connected to the intended sensors or actuators according to the manufacturer's instructions. Any connecting leads for external sensors or actuators shall be at least 2 m. For devices not

having integral cables the type of cable used shall be specified by the manufacturer and recorded in the test report;

b) The test shall be performed:

For sensors:

1) with the target set at a position such that the switching element is in the OFF-state;
2) with the target set at a position such that the switching element is in the ON-state;

For actuators:

1) with the actuator in the ON-state;
2) with the actuator in the OFF-state;

For remote I/Os:

1) with the I/Os activated;
2) with the I/Os deactivated;

For master:

according to 9.4 without repetition of any message in case of a fault.

NOTE The master should have provisions for detecting disturbed messages.

For the test of 8.6.2.4 the following additional mounting conditions apply.

Metal enclosures of AS-i devices, if any, shall be connected to the reference ground plane.

AS-i devices with non-metallic enclosures shall be mounted on a metal plate which shall be connected to the reference ground plane.

The method of connection to the reference ground plane shall be in accordance with the manufacturer's instructions, if given, and shall be recorded in the test report.

9.5.9.2 Electrostatic discharge (ESD) immunity

The test is performed according to IEC 61000-4-2 and 8.6.2.1 and shall be repeated ten times at each measuring point, with a minimum time interval of 1 s between pulses.

9.5.9.3 Radiated radio frequency electromagnetic fields immunity

The test is performed according to IEC 61000-4-3 and 8.6.2.2.

9.5.9.4 Electrical fast transient immunity

The test shall be performed according to IEC 61000-4-4 and 8.6.2.4, with all the connecting leads placed in the capacitive coupling clamp. The test voltage for the auxiliary power ports shall be applied via the coupling network.

9.5.9.5 Emission requirements

The test shall be performed according to CISPR 11, group 1, class A, and to 8.6.3.

9.5.9.6 Test results and test report

The test results shall be documented in a comprehensive test report. The test report shall present the objective, the results and all relevant information of the tests. The test report shall

define the AS-i device under test, including the cable layout, the necessary auxiliary equipment and the target position if any. Any deviation from the test plan shall be mentioned.

Where a range of AS-i devices are made according to the same principle and design, and using the same type of components, tests may be performed on representative samples. Furthermore, based on first results, the testing laboratory may limit the tested frequency range for radiation or conduction tests; then, it shall include in the report the frequency range used.

9.6 Test of a AS-i master

9.6.1 Current consumption

9.6.1.1 General

The test requirements allow measurement of the current consumption of an AS-i master. These test requirements become obsolete if the master has an integrated AS-i power supply. In that case, however, all tests of the test requirements for AS-i power supplies have to be additionally fulfilled by the master.

The manufacturer shall provide the following information:

a) current documentation,

b) profile used.

9.6.1.2 Test circuit

Figure 93 shows the required test circuit.

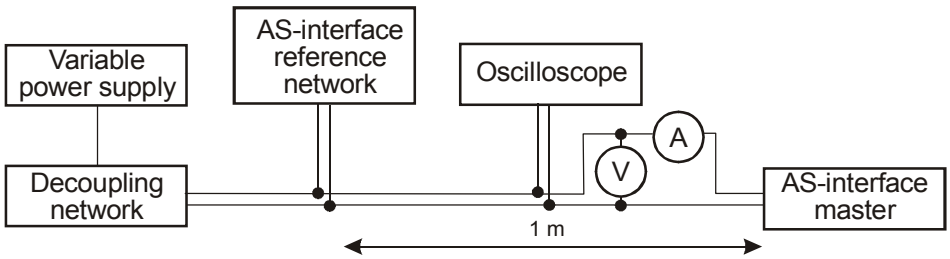


Figure 93 – Test circuit for current consumption test

Figure 94 shows the decoupling network and the position of the ammeter. At this position, the average current can be measured.

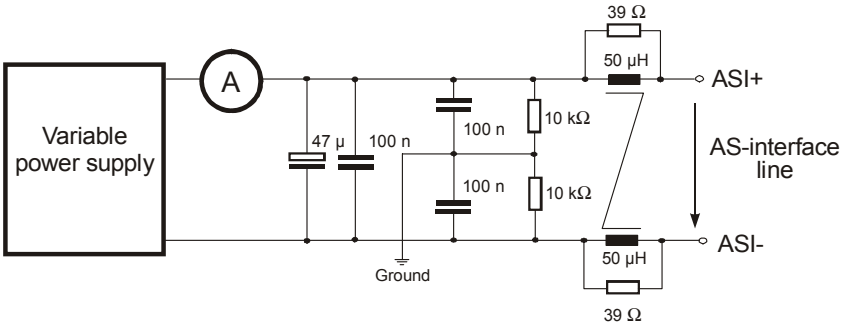


Figure 94 – Decoupling network, ammeter and power supply

9.6.1.3 Measuring and test equipment

This shall include:

- AS-i reference network;
- AS-i data decoupling network,
- ammeter;
- voltmeter;
- oscilloscope;
- decoupling network to Figure 94;
- variable power supply.

9.6.1.4 Test procedure

The following steps shall be taken:

a) set up test circuit to Figure 93;
b) operate the master to be tested in normal operation;
c) check the master functions at the following d.c. voltages on the AS-i line: 31,6 V, 26,5 V, 23,5 V, 21,5 V and again at 23,5 V;
d) check the maximum current consumption.

9.6.1.5 Evaluation

The maximum current consumption shall be not greater than the value stated in the documentation nor the requirements of the specification.

The function test at the operating voltage limits shall correspond to the data stated in the documentation and the applicable specifications, i.e. at d.c. voltages on the AS-i line of 31,6 V, 26,5 V and 23,5 V the master has to function, but there must not be any master activity at 21,5V. The master activity is detected by means of an oscilloscope directly on the AS-i line.

9.6.2 Noise emission

9.6.2.1 General

This test instruction allows the measurement of the noise emission of an AS-i master in a power-fail state on the AS-i network.

9.6.2.2 Test circuit

Figure 95 shows the required test circuit.

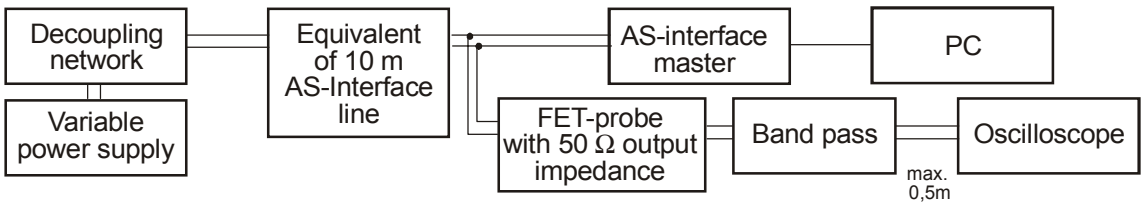


Figure 95 – Test circuit noise emission AS-i master

Figure 96 shows the decoupling network.

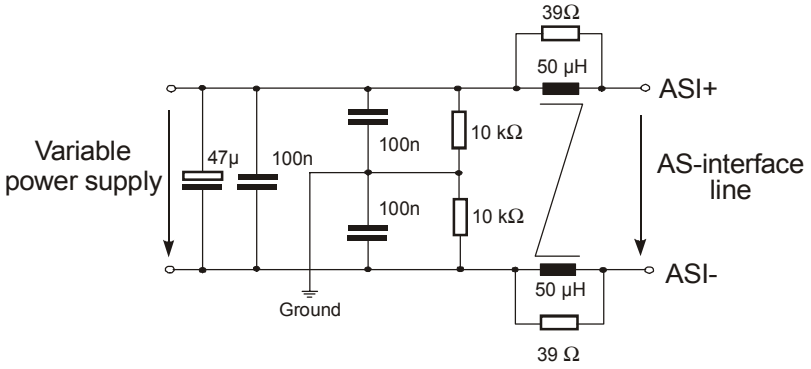


Figure 96 – Decoupling network

The change in current consumption in a master should only cause a noise voltage ≤ 50 mV_{pp} on the AS-i line in the frequency range between 10 kHz and 500 kHz. The voltage on the AS-i line is measured by means of an oscilloscope via a bandpass (see Figure 97). The oscilloscope is to be operated in the mode envelope, peak detection on at a cut-off frequency > 10 MHz. The FET probe is to be terminated with an impedance of 50 Ω and connected via a line impedance of 50 Ω/1 W to the bandpass. The test circuit is to be screened from noise so that the measured maximum noise voltage without the master is smaller than 15 mV. For this purpose, the cable length between master and AS-i equivalent line (see Figure 98) is to be limited to a maximum of 20 cm. The master shall be operated in the power-fail state (d.c. voltage on the AS-i line of 21 V).

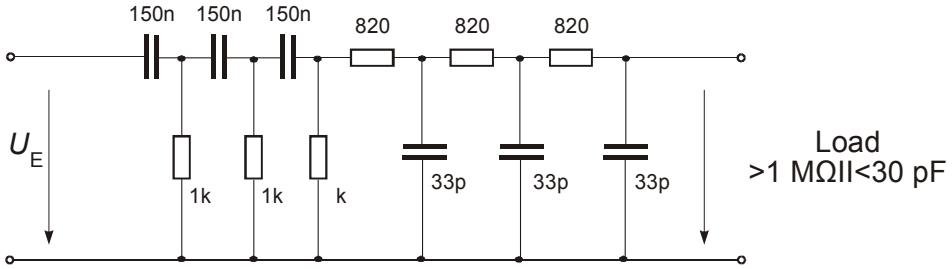


Figure 97 – Bandpass 10 kHz to 500 kHz

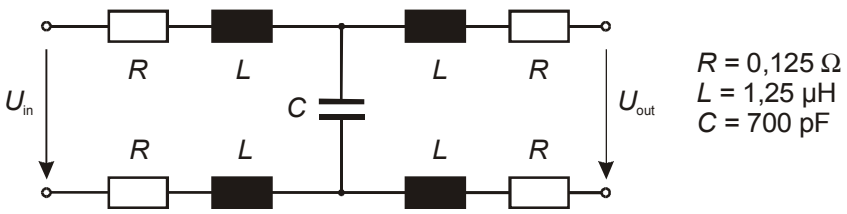


Figure 98 – Equivalent circuit of the 10 m AS-i line

9.6.2.3 Measuring and test equipment

This shall include:

– variable power supply;
– oscilloscope with FET probe;
– line impedance 50 Ω / 1 W;

– decoupling network;
– equivalent circuit of 10 m AS-i line;
– bandpass.

9.6.2.4 Test procedure

The following steps shall be taken:

a) apply a voltage of 21 V to the AS-i line;
b) measure the noise voltage without the master by means of the oscilloscope over 60 s;
c) connect the master;
d) check the power-fail state of the master;
e) measure the noise voltage with the master on the AS-i line by means of an oscilloscope over 60 s.

9.6.2.5 Evaluation

The noise voltage on the AS-i line must not be increased by more than 50 mV_{pp} by the master in the power-fail state.

9.6.3 Impedance measurement

9.6.3.1 General

The impedance measurement of the master is to be performed in the "ready state" under laboratory conditions.

An a.c. signal *U*~ with $R_i \leq 20\ \Omega$ is to be superimposed on the AS-i d.c. voltage. This a.c. voltage and the resulting a.c. current *I*~ of the master are to be measured.

9.6.3.2 Test circuit

Figure 99 shows the test circuit for the impedance measurement. The operation of the master in switch position "test" has been purposefully selected as asymmetrical, i.e. metal parts of the master must not be grounded. Switch S1 allows a switching of a.c. ground (switch position shown: ASI- = GND).

The a.c. input current *I*~ is measured by means of the current probe. The input impedance is calculated as follows:

$$| Z | = | U\sim | / | I\sim |$$

The distance to the AS-i master shall be 20 cm.

The d.c. voltage is to be set to 21 V to put the master in the offline state.

9.6.3.3 Measuring and test equipment

9.6.3.3.1 For point 6.3.1 (impedance measurement)

This shall include:

– variable power supply;
– impedance analyzer (Figure 99a);

alternatively:

– sine wave generator;

– current probe;
– oscilloscope;
– test circuit (IMP_SYM) to Figure 99b.

9.6.3.3.2 For point 6.3.1.6 (d.c. resistance)

This shall include:

– R-meter (Wheatstone bridge).

9.6.3.3.3 For point 6.3.2 (symmetry measurement)

This shall include:

– FET probe with 50 Ω output impedance;
– line impedance (50 Ω / 1 W);
– HF voltmeter;
– bandpass;
– test circuit (IMP_SYM) as shown in Figure 100.

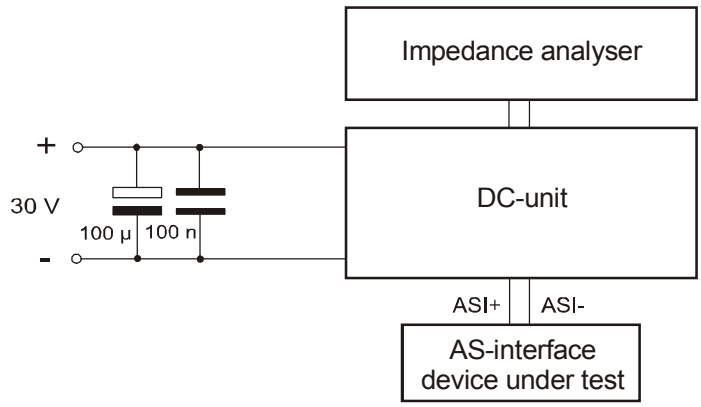


Figure 99a – Test with impedance analyzer

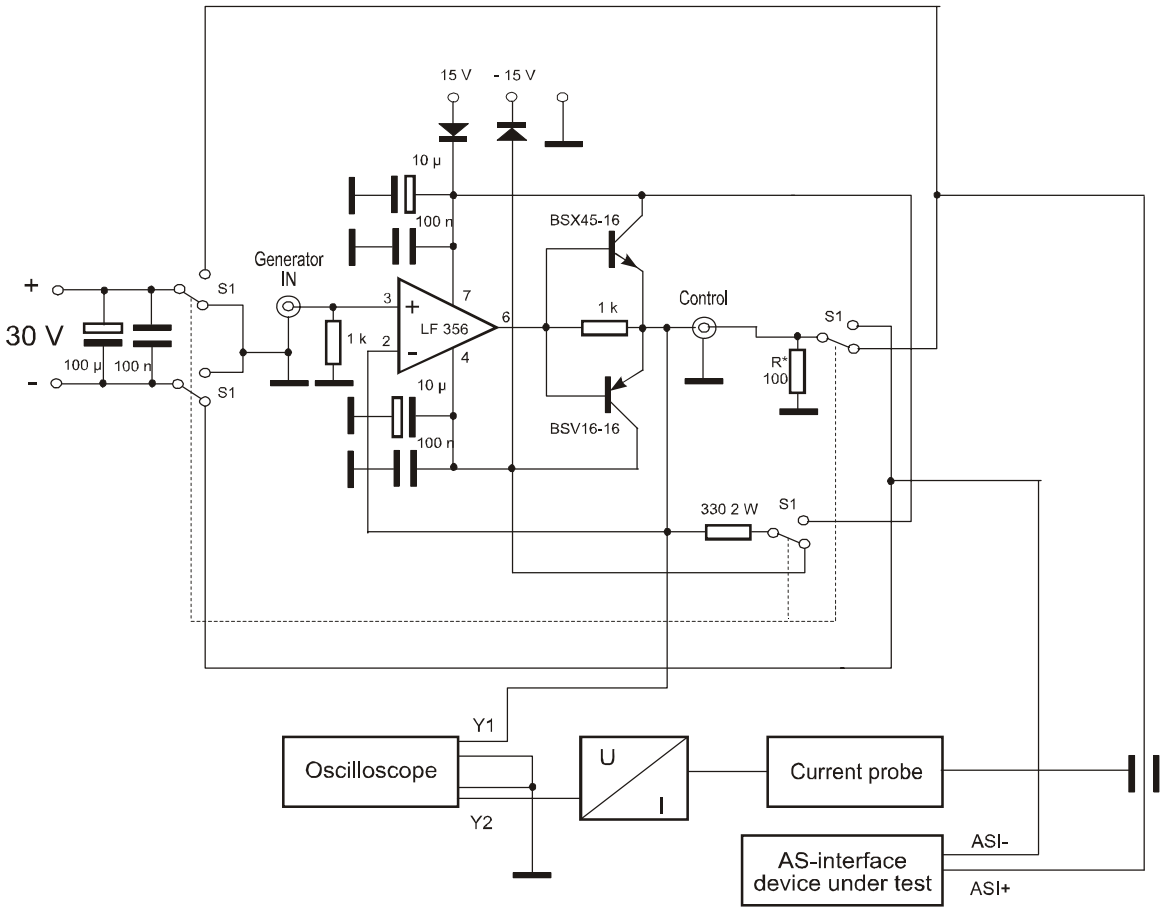


Figure 99b – Test with sine wave generator, current probe, oscilloscope and test circuit (IMP_SYM)

Figure 99 – Test circuit impedance measurement

9.6.3.4 Test procedure

The following steps shall be taken:

a) test procedure with impedance analyzer as shown in Figure 99a:

   Determination of Z (or R_p, L_p, C_p if applicable) with 6 V_{pp} at 50 kHz, 100 kHz, 125 kHz, 150 kHz, 175 kHz, 200 kHz, 250 kHz and 300 kHz. If at one of the test frequencies the master has a resonant frequency, the test frequency shall be varied ±10 kHz.

b) test procedure with test circuit IMP_SYM as shown in Figure 99b:

   1) switch S1: position "ASI- = GND";

   2) determine the a.c. current I~ at U~ = 6 V_{pp};

   3) the measurement is to be carried out as described in 8.5.2.1.

9.6.3.5 Evaluation of impedance

The evaluation is to be carried out as described in 8.5.2.1 and shall not exceed the limit values stated there.

9.6.3.6 Evaluation of d.c resistance

The d.c. resistance between ASI+, ASI− and all metallic parts of the master with the exception of outer connections shall be ≥ 250 kΩ.

9.6.4 Symmetry measurement

9.6.4.1 General

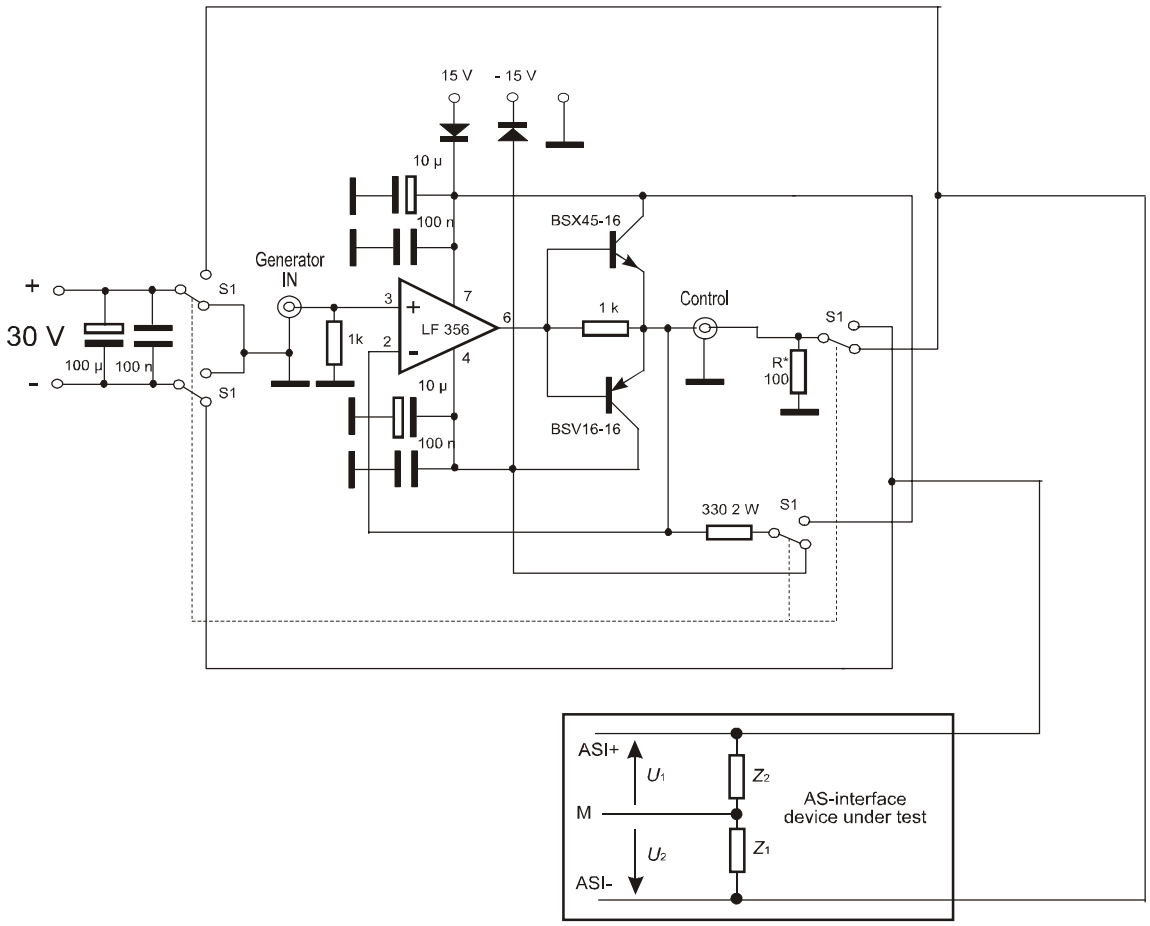


Figure 100 – Master connection for symmetry measurement

The partial impedances Z_1 and Z_2 respectively form a voltage divider at measurement point M. This measurement point may be the metallic housing or a metallic mounting plate. The measurement point shall be connected to the external supplies of the master or the controller respectively.

In the off-load state the currents through Z_1 and Z_2 are identical.

For an asymmetry of 10 % this means

$$0{,}90 \leq \frac{\left|\vec{U}_1\right|}{\left|\vec{U}_2\right|} = \frac{|Z_1|}{|Z_2|} \leq 1{,}10$$

$\vec{U}_1$: voltage between M and ASI+ for ASI+ = GND

$\vec{U}_2$: voltage between M and ASI− for ASI- = GND

9.6.4.2 Test circuit

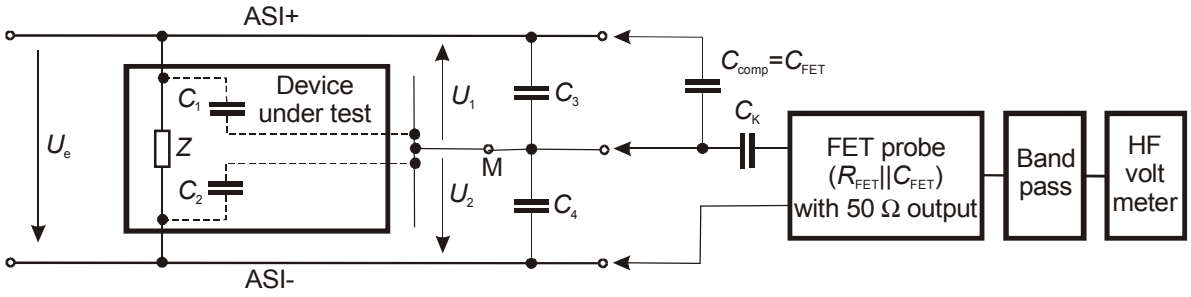


Figure 101 – Test circuit symmetry measurement of the AS-i master

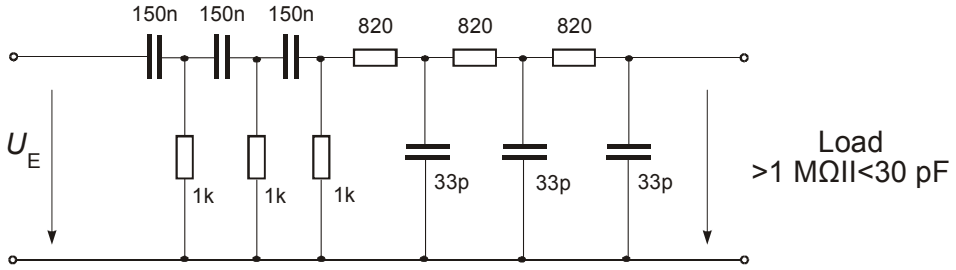


Figure 102 – Bandpass 10 kHz to 500 kHz

The test circuit corresponds to the one of the impedance measurement (compare Figure 99b). With the test circuit in Figure 100 the voltage drops U_1 of ASI+ to M and U_2 of ASI− to M are determined by means of a FET-probe (R_i=1 MΩ//2 pF) with a.c. coupling $C_k \geq$ 1nF at an output impedance of 50 Ω, a line impedance of 50 Ω/1 W between FET-probe and bandpass and an HF voltmeter (frequency range up to 300 kHz, R_i = 10 MΩ//30 pF). The capacitance $C_{komp} = C_{fet}$ is to be taken into account in the circuit to compensate for the probe capacitance.

By means of calibrating C_3, $|U_1| = |U_2| = U_E/2$ can be achieved and the capacitances of C_1 and C_2 can be determined independently of Z.

A possible measurement error of the HF voltmeter in higher frequency ranges is eliminated by means of the ratio $|U_1| / |U_2|$.

9.6.4.3 Test procedure

a) Set a measurement voltage of 2,0 V_{rms} displayed on the evaluation meter at a frequency of 150 kHz.

b) Determine $|U_1|$ and $|U_2|$ at frequencies of 50 kHz, 100 kHz, 150 kHz, 200 kHz, 250 kHz and 300 kHz without C_3.

c) Check the condition:

$$0{,}90 \leq \frac{\left|\vec{U}_1\right|}{\left|\vec{U}_2\right|} = \frac{|Z_1|}{|Z_2|} \leq 1{,}10$$

If this condition is met at all frequencies, the symmetry test is passed.

If this condition is not met, add C_S (3 or 4) between ASI+ and M or ASI− and M, external capacitor for symmetry test C_S = 30 pF for all masters.

d) Symmetry test procedure has to be performed at frequencies of 50 kHz, 100 kHz, 150 kHz, 200 kHz, 250 kHz and 300 kHz.

9.6.4.4 Evaluation

The symmetry test is passed if the test procedure (Figure 103) is finished with “Symmetry OK” for each test frequency.

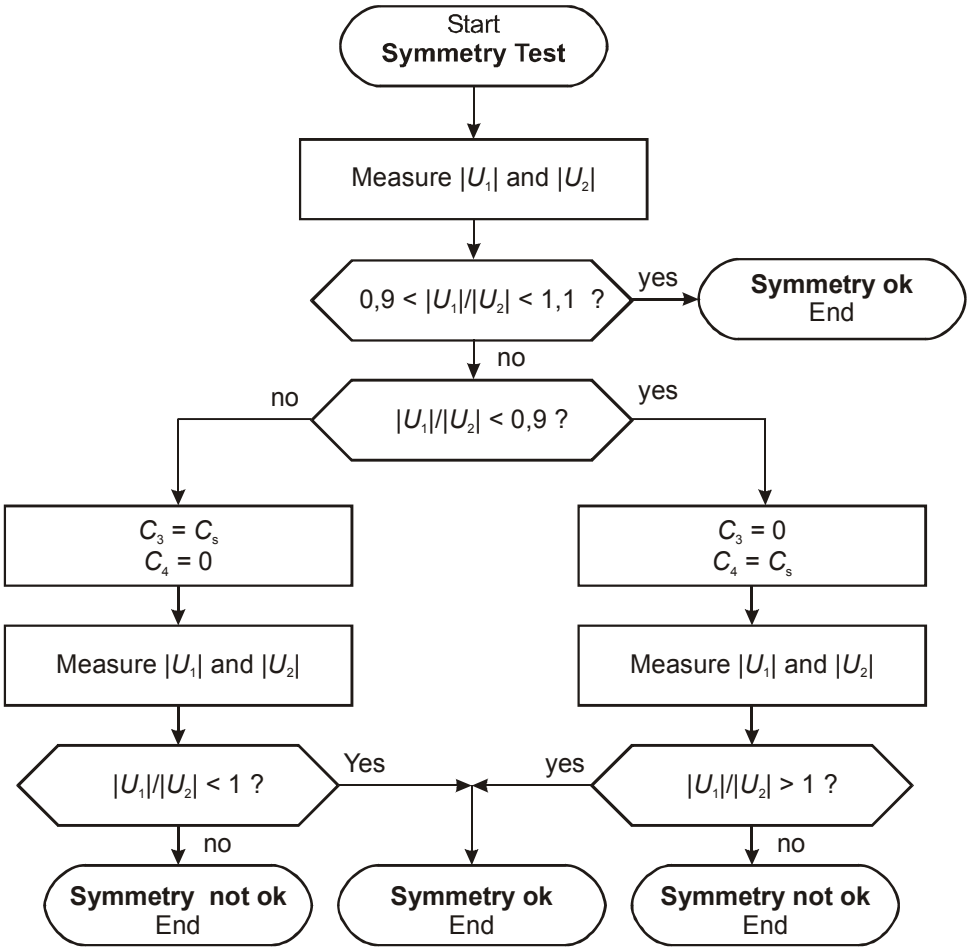


Figure 103 – Procedure for symmetry test

9.6.5 Test instruction: Power-on behaviour

9.6.5.1 General

By testing the power-on behaviour, the switch-on delay time t_E of the AS-i master and its current consumption shall be tested. The settings of the oscilloscope can be seen on the oscillograms.

AS-i masters with integrated AS-i power supply must have an internal voltage supply which is accessible and can be interrupted for this test so that the external AS-i supply can be connected.

9.6.5.2 Measuring and test equipment

This shall include:

– AS-i power supply;

– variable power supply;

– ammeter;
– oscilloscope;
– constant current source (KONST_I).

9.6.5.3 On-delay

9.6.5.3.1 General

The offline flag of the master is reset (normal operation). In the initial state, the master is not connected with the AS-i line (switch S is open). The master shall communicate with the slaves at the earliest 1 s after switch S has been closed. The oscilloscope shall be triggered by the rising edge of the supply voltage on the AS-i line. The start of communication is shown on the oscilloscope via peak detection on and d.c. coupling.

9.6.5.3.2 Test circuit

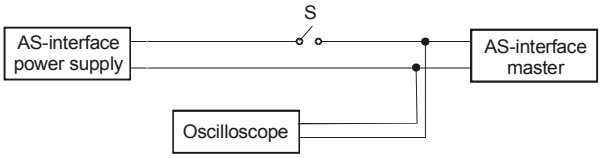


Figure 104 – Test circuit – On-delay

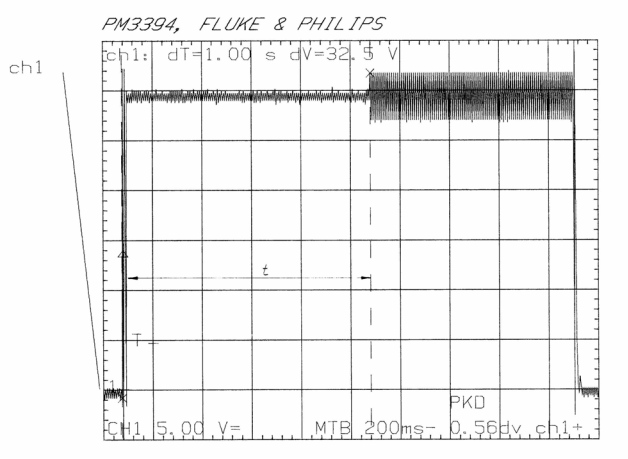


Figure 105 – Oscillogram on-delay (example)

9.6.5.3.3 Evaluation

The time t_E shall be determined from the oscillogram. It shall be shorter than 1,00 s.

9.6.5.4 Current consumption

9.6.5.4.1 General

If the master is supplied (see circuit Figure 106) with a current corresponding to the total current consumption as stated in the documentation +12,5 mA (to be set with an accuracy of ±2,5 mA), the master shall have reached an operating voltage of 26,5 V within 1 s after closing switch S in Figure 107. The final operating voltage value to be reached shall be 30 V at the output of the circuit with a set constant current.

9.6.5.4.2 Test circuit

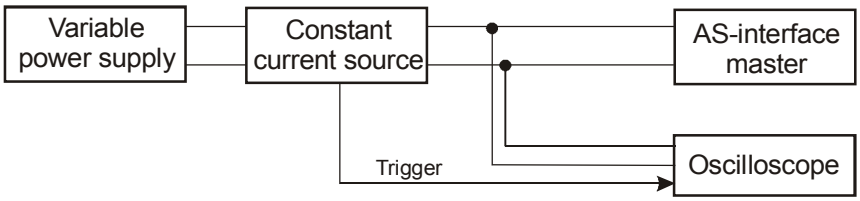


Figure 106 – Block circuit diagram current consumption measurement of the AS-i master

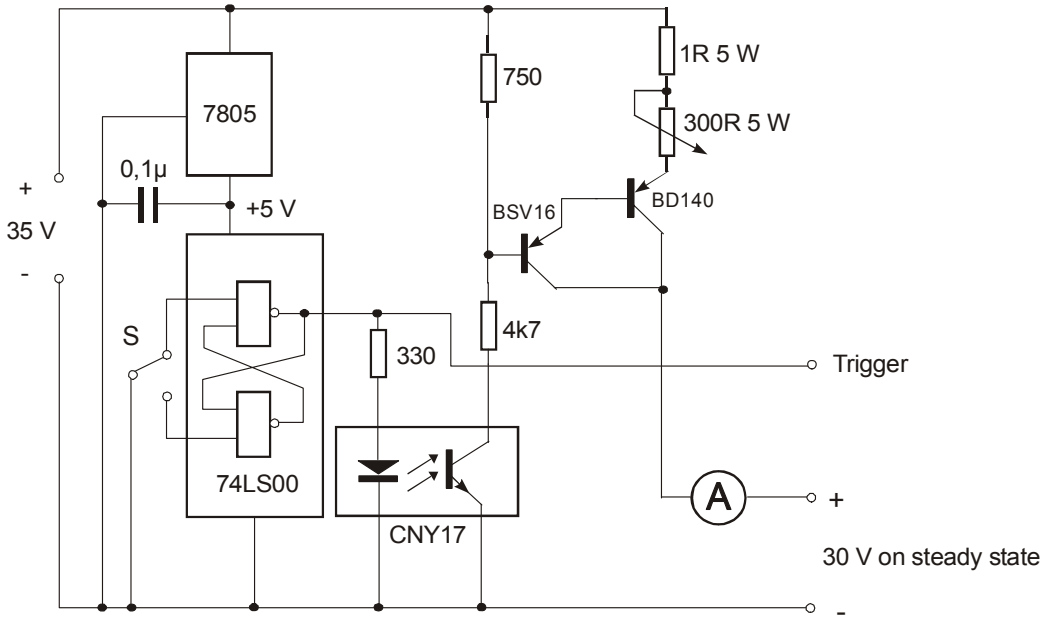


Figure 107 – Constant current source with trigger output (KONST_I)

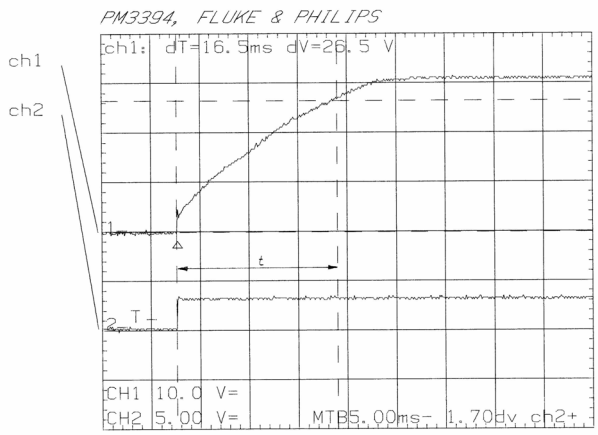


Figure 108 – Oscillogram current consumption (example)

9.6.5.4.3 Evaluation

The time *t* shall be determined from the oscillogram to Figure 108. It shall be shorter than 1 s.

9.6.6 Logical start-up behaviour

9.6.6.1 General

These test instructions will check the logical behaviour of the master during start-up as well as in the protected mode and the configuration mode. For this purpose, the master shall be operated in an AS-i network. Test circuit and test procedure are the same for the standard master and the extended master. The different reactions are taken into consideration during evaluation.

9.6.6.2 Measuring and test equipment

This shall include:

– AS-i master;
– AS-i power supply;
– AS-i slaves (number depending on test circuit or logical test slave);
– AS-i bus monitor.

9.6.6.3 Test circuit

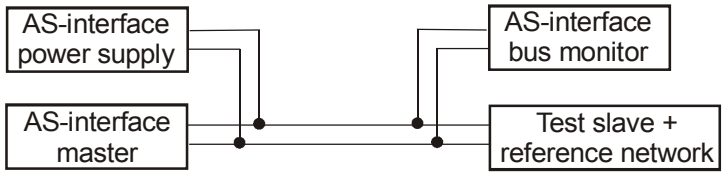


Figure 109 – Test circuit for checking start-up operation

Figure 109 shows the test circuit for checking the logical behaviour of the AS-i master during start-up operation. The required slaves shall be connected to the AS-i network with the corresponding settings in accordance with the test procedure. The data exchange shall be monitored via the bus monitor.

9.6.6.4 Test procedure

The following steps shall be taken.

9.6.6.4.1 Protected operation, projected parameters = 0xF

a) Check start-up behaviour without error

   The following slaves are in the network and are correctly projected:

   – Standard addresses: 1, 2, 4, 6, 7, 9, 10, 12, 15, 17, 20, 22, 24, 26, 27, 28, 29, 30, 31
   – A addresses: 3A, 5A, 13A, 16A, 21A, 25A
   – B addresses: 5B, 8B, 14B, 16B, 23B, 25B (B addresses are only projected in the Extended Master).

b) Check start-up behaviour as in a) but with slave 10 missing.

c) Check start-up behaviour as in a) but with wrong ID code of slave 10.

d) Check start-up behaviour as in a) but with wrong I/O configuration of slave 10.

e) Check start-up behaviour as in a) but with additional slave 0.

f) Check start-up behaviour as in a) but with additional slave 18.

g) Check start-up behaviour as in b) but with additional slave 0 with correct configuration data for missing slave 10.

h) Check start-up behaviour as in a) but with additional slave 10, which replies to Read_ID_Code with parity error.

i) Check start-up behaviour as in a) but with power fail in activation phase.

The following two points are only checked for the Extended Master:

j) Check start-up behaviour as in a) but with wrong ext. ID1 code of slave 5A.

k) Check start-up behaviour as in a) but with missing slave 16B and additional slave 0 (bit I3 of ext.ID1 code equals 0) with correct configuration data of slave 16B.

The message sequence shall be checked via the bus monitor.

The controller shall output the flags in accordance with PICS.

9.6.6.4.2 Configuration mode

All checks of 9.6.6.4.1 shall also be executed in the configuration mode.

9.6.6.5 Evaluation

A standard master shall communicate with all standard slaves and with all A slaves, an extended master shall communicate with all slaves.

All checks shall run conform to the AS-i master specification.

A printout of the monitor recordings shall be enclosed in the case of errors.

9.6.7 Logical behaviour in normal operation

9.6.7.1 General

These test instructions shall check the logical behaviour of the master in normal operation. Test circuit and test procedure are the same for standard master and extended master. The different reactions are taken into consideration during evaluation.

9.6.7.2 Measuring and test equipment

This shall include:

– AS-i master;
– AS-i power supply;
– AS-i slaves (number depending on test circuit or logical test slave);
– AS-i bus monitor.

9.6.7.3 Test circuit

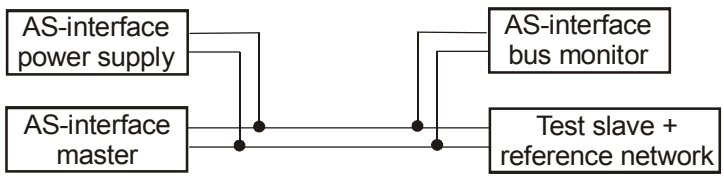


Figure 110 – Test circuit for checking normal operation

Figure 110 shows the test circuit for checking the logical behaviour of the AS-i master in normal operation. The required slaves shall be connected to the AS-i network with the corresponding settings in accordance with the test circuit. The data exchange shall be monitored via the bus monitor.

9.6.7.4 Test procedure

The following steps shall be taken.

Protected mode, projected parameters = F_{hex}

a) Check behaviour without errors.

   The same slaves as described in 9.6.6.4.1 are in the network.

   Data exchange is active.

b) Check behaviour as in a) but slave 10 shows 1, 2, 3, 4, 5, 6 ... subsequent transmission errors, then total failure.

c) Check behaviour as in a) but with additional slave 18, which is not projected.

d) Check behaviour as in a) but with missing slave 10.

e) Check behaviour, when slave 10 is inserted with data previously projected by the master.

f) Check behaviour when slave 10 is inserted with modified configuration.

g) Check automatic addressing

   initial state: Project slaves to a), remove slave 10, i.e.: Config=NOK, protected mode, Auto Prog Avail, Auto Prog, normal operation.

h) Insert slave 0 with configuration of removed slave 10.

i) Insert slave 0 with wrong configuration (i.e. with a profile different from the profile of the removed slave).

j) As in e) and additionally remove slave 6.

k) Insert slave 0 with correct configuration of slave 10.

l) As in e) and insert slave 0 with wrong configuration.

The following two points are only checked for the extended master:

m) Check behaviour as in a) but slave 16B shows 1, 2, 3, 4, 5, 6 ... subsequent transmission errors, then total failure.

n) Check automatic addressing

   initial state: Project slaves to a), remove slave 8B, i.e. Config=NOK, protected mode, Auto Prog Avail, Auto Prog, normal operation.

o) Insert slave 0 with configuration of removed slave 8B.

p) Insert slave 0 with wrong configuration (i.e. with a profile different from the profile of the removed slave).

q) As in g) and additionally remove slave 5A.

9.6.7.5 Evaluation

A standard master shall communicate with all standard slaves and with all A slaves. An exchange of data shall take place with these slaves in each AS-i cycle.

An extended master shall communicate with all slaves and exchange data with the slaves as described in this standard in 8.5.

Neither a standard master nor an extended master shall display a configuration error in point a) of 8.5.2.5.

All checks shall be conform to the AS-i master specification.

A printout of the monitor recordings shall be enclosed in the case of errors.

9.6.8 Time response

9.6.8.1 General

This test instruction shall test if the cycle time of 5 ms is kept at full complement of the AS-i network or the master behaviour with only one slave (shortened cycle time or insertion of dummy messages).

9.6.8.2 Measuring and test equipment

This shall include:

– AS-i master;
– AS-i power supply;
– AS-i reference network (number of slaves depending on test circuit);
– AS-i bus monitor.

9.6.8.3 Test circuit

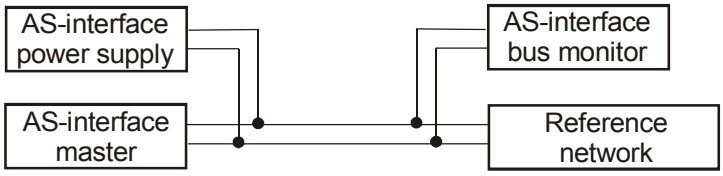


Figure 111 – Test circuit

Figure 111 shows the test circuit for testing the time response of the AS-i master. The necessary slaves shall be connected to the AS-i network depending on the requirements shown in the test circuit. The communication on the AS-i line shall be monitored via an AS-i bus monitor.

9.6.8.4 Test procedure

The following steps shall be taken:

The time response of the master (AS-i cycle) shall be tested for the following conditions:

– 28 standard slaves and 3 A/B slave pairs in LAS;
– one standard slave is missing, execution of the function automatic addressing;
– one B slave is missing, execution of the function automatic addressing (only for extended master);
– 1 standard slave in LAS.

9.6.8.5 Evaluation

The time response of the master shall be assessed via the bus monitor with regard to conformity to this standard and to the product specification. The master shall start a request after a slave response in a window from 8 µs to 14 µs.

9.6.9 Additional test for masters supporting combined transactions

Under consideration.

Annex A
(normative)

Slave profiles

This annex provides specific information concerning the definition of profiles for the AS-i slaves. It explains the concept of profiles and states the particular features for the individual slave profiles.

A.1 Introduction

The AS-i system supports the communication of four I/O data bits and four parameter bits between the master and individual slaves. For each slave, there are sixteen different configurations for the I/O data bits, i.e. the bits may be defined as input, output, bidirectional, or if unconfigured, tristate. Furthermore, two particular slaves with the same I/O configuration may have different meanings of the data and parameter bits.

To facilitate usage in applications AS-i defines profiles for the slaves. Slave profiles define the use of the data and parameter values for the most common applications and assign specific meanings to them.

A slave profile contains all the additional definitions and restrictions needed for a slave in a specified application.

A slave profile contains the well-defined and fixed data:

– I/O configuration (I/O code) with meanings for the I/O data and parameter values;
– identification code (ID code);
– definition of meanings of the levels (HIGH or LOW) of the I/O data and parameters;
– list of minimum requirements for the physical implementation.

The installation of slaves according to specific slave profiles may be supported by standard function blocks (if available) in the controller. Replacing a slave with another having the same slave profile shall need no changes in the application software, provided the physical specification of the old and the replacement slave are identical in the application.

The ID code of the slave is used to distinguish between different slave profiles with the same I/O code. It is stored within the slave in a non-volatile and irreversible format.

A.2 Definitions

A.2.1
I/O data bit
AS-i supports a cyclic communication of 4 I/O data bits between master and slave

A.2.2
parameter bit
AS-i supports an acyclic communication of 4 parameter bits between master and slave

A.2.3
I/O type
each I/O data bit of a slave is configured as input, output, bidirectional, or tristate type

A.2.4
I/O code
AS-i allows 16 different combinations of I/O types for the 4 I/O data bits

NOTE These 16 different I/O configurations are identified by the I/O code.

A.2.5
ID and ID2 codes
ID code and extended ID2 code (where applicable) identify the slave profile to which the slave of a specific I/O configuration conforms

A.2.6
controller level
representation of the logic level (0/1) of inputs or outputs at the interface between the AS-i master and the controller

A.2.7
AS-i level
logic level (low/high) within the AS-i system

NOTE The logic level for the I/O bits is inverted at the inputs of the AS-i master, i.e. for I/O bits the AS-i level is inverse to the controller level.

A.2.8
default levels
defaults for the ASI levels of the I/O data bits and parameter bits

NOTE These levels are high.

A.2.9
physical signal
in some slave profiles, the level definition uses the terms “Physical signal detected” and “Physical signal not detected”

NOTE In this context, the “physical signal detected” is defined for several different groups of binary sensors:

– for photoelectric and ultrasonic sensors: light or sound is detected on the detecting element within the specified range of geometry, intensity or time window;

– for inductive or capacitive sensors: the frequency or the amplitude of the internal oscillator is changed due to the presence of an object within the specified range;

– for pressure sensors: the higher one of two pressure ranges is detected by the switch;

– for flow sensors: the higher one of two flow rates is detected by the switch;

– for level sensors: the sensor detects the presence/level of the medium.

A.3 Overview: existing slave profiles

A.3.1 General rules

Only the Slave profiles defined in this standard may be used. All other Slave profiles are reserved for future use.

The profiles do not distinguish between Synchronous Data I/O Mode and Non-Synchronous Data I/O Mode. If this function can be activated with a Parameter Call P2=0 shall be used to activate Synchronous Data I/O Mode.

NOTE If there was an error in transferring the codes from the non-volatile to the volatile memory, the codes $I/O=F_{Hex}$ and $ID=F_{Hex}$ are stored in the volatile memory of a slave.

A.3.2 Profile table standard slaves

An overview of the so far defined slave profiles and their combinations of the configuration (IO code) and profile identification (ID code) is given in Table A.1 and Table A.2. The detailed definitions of the slave profiles are given in the following subclauses.

Table A.1 – Overview of existing slave profiles for standard slaves

Slave-profiles			ID code														
			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	I, I, I, I	0.0	0.1									0.A	0.B				0.F
	1	I, I, I,O	1.0	1.1									1.A					1.F
	2	I, I, I,B	2.0										R					2.F
	3	I,I,O,O	3.0	3.1									3.A					3.F
I/	4	I ,I ,B,B	4.0										4.A					4.F
O	5	I,O,O,O	5.0										5.A					5.F
	6	B,B,B,B	6.0										6.A					6.F
C	7	B,B,B,B	7.0	7.1	7.2	7.3	7.4	7.5					7.A	7.B		7.D	7.E	7.F
o	8	O,O,O,O	8.0	8.1									8.A					8.F
d	9	O,O,O,I	R										9.A					9.F
e	A	O,O,O,B	A.0										R					A.F
	B	O,O,I ,I	R	B.1									B.A					B.F
	C	O,O,B,B	C.0										C.A					C.F
	D	O, I ,I, I	R	D.1									D.A					D.F
	E	O,B,B,B	E.0										E.A					E.F
	F	T,T,T,T	For future use															V

Configuration: I = input, O = output, B = bidirectional, T = tristate; profiles: R = reserved).

Table A.2 – List of existing profiles for standard slaves

Profile name	IO	ID	Subclause
Remote I/Os (X = 0 … E, not 9, B, D)	X	0	A.4.2
Free profiles for standard slaves (X = 0 … E)	X	F	A.4.1
Remote I/Os with dual signals(X = 0, 3, 8)	X	1	A.4.3
Safety sensors	0	B	A.6.9
Single sensor with extended control	1	1	A.4.4
High speed slave profile for combined transaction type 5	6	0	A.6.8
Slave profile for combined transaction type 1 (analogue profile)	7	1	A.6.1
Extended slave profile for combined transaction type 1 (Ext. analogue profile)	7	2	A.6.2
Slave profile for combined transaction type 1 (integrated analogue profile)	7	3	A.6.3
Extended slave profile for combined transaction type 1 (extended integrated analogue profile)	7	4	A.6.4
Slave both analogue and digital with support of combined transaction type 2	7	5	A.6.5
Safety sensors with non-safe outputs	7	B	A.6.9
Motor control devices (electromechanical)	7	D	A.4.5
Motor control devices (semiconductor)	7	E	A.4.5
Dual actuator with feedback	B	1	A.4.6
Single actuator with monitoring	D	1	A.4.7

A.3.3 Profile table slaves with extended addressing

Slaves with these profiles shall be capable of communicating in the extended addressing mode according to this standard.

The I/O code may have any value between 0_{Hex} and E_{Hex} with the exceptions of I/O=2 and I/O=A.

The ID code shall be A_{Hex}.

NOTE As ID=A has the special function to allow for A/B-slaves, free profiles for A/B-slaves can only be marked by ID2 (S-X.A.E).

An overview of the so far defined slave profiles and their combinations of the configuration (IO code) and profile identification (ID2 code) is given in Table A.3 and Table A.4. The detailed definitions of the slave profiles are given in the following subclauses.

Table A.3 – Overview of existing slave profiles with extended address

Slave-profiles			ID2 code														
			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	I, I, I, I	0.A.0		0.A.2												0.A.E	R
	1	I, I, I, O	1.A.0														1.A.E	R
	2	I, I, I, B	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	3	I, I, O, O	3.A.0	3.A.1	3.A.2												3.A.E	R
I/	4	I , I , B, B	4.A.0														4.A.E	R
O	5	I, O, O, O	5.A.0														5.A.E	R
	6	B, B, B, B	6.A.0														6.A.E	R
C	7	B, B, B, B	7.A.0		7.A.2			7.A.5		7.A.7	7.A.8	7.A.9	7.A.A				7.A.E	R
o	8	O, O, O, O	8.A.0		8.A.2												8.A.E	R
d	9	O, O, O, I	9.A.0														9.A.E	R
e	A	O, O, O, B	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	B	O, O, I , I	B.A.0		B.A.2			B.A.5									B.A.E	R
	C	O, O, B, B	C.A.0														C.A.E	R
	D	O, I , I, I	D.A.0														D.A.E	R
	E	O, B, B, B	E.A.0														E.A.E	R
	F	T, T, T, T	For future use															V

Configuration: ID-Code = A. I = input, O = output, B = bidirectional, T = tristate; profiles: R = reserved.

Table A.4 – List of existing profiles for slaves in extended address mode (ID=A)

Profile name	IO	ID2	Subclause
Remote I/Os (X = 0 ... E, not 2, A)	X	0	A.5.2
Free profiles for slaves in extended address mode (X = 0 ... E)	X	E	A.5.1
Remote I/Os with dual signals (X = 0, 3, 7, 8, B)	X	2	A.5.4
Single sensor with extended control	3	1	A.5.3
Slave both analogue and digital with support of combined transaction type 2	7	5	A.6.5
4I/4O in extended addressing mode	7	7	A.6.6
Slave profile for combined transaction type 4 (single channel)	7	8	A.6.7
Slave profile for combined transaction type 4 (dual channel)	7	9	A.6.7
8I/8O in extended addressing mode	7	A	A.6.6
Slave with support of combined transaction type 2	B	5	A.6.5

A.3.4 Sub-profiles

Sub-profiles may be defined to each existing profile S-x.x by using ID2 to describe more detailed and strictly fixed profiles S-x.x.0 to S-x.x.D. Additionally, ID2 is used to indicate whether a slave is built with or without a slave-IC that has the optional features ID1, ID2, Broadcast and Peripheral Fault Indication of the AS-Interface version 2.1 and higher.

Presently the following ID2 Codes are fixed:

ID2-values according to the Profiles in A.4.2 to A.4.4.

ID2 = F_{Hex} for all slaves according to the I/O-ID-table if they can be realised with ICs not having the ID1/ID2-capability (ICs according to the specifications before 2.1) or they are intended to replace an older slave without the ID2-capability. This is independent whether the IC used for the implementation is an IC according to previous versions of this specification or an IC according to this version.

NOTE In these cases the “peripheral fault bit” will not be interpreted by the master.

ID2 = E_{Hex} for all slaves according to the I/O-ID-table which can be realised in its functions only with a slave having the new options of C.S. 2.1 (e.g. peripheral fault handling) and which do not fit the conditions on other ID2-codes (Free sub-profile for "new slaves").

In general, the extended ID Code 1 is user configurable and therefore not defined in the following subclauses. The manufacturer shall set all bits of the extended ID Code 1 to "1". In extended addressing mode, it is permitted for the manufacturer to block the write access by the user to the extended ID Code 1. This allows to distinguish between more specific products. The manufacturer shall set all bits of the blocked extended ID Code 1 to "1" or as it is defined in the profile. Some ID Code 1 may be fixed in specific profiles. In case of ID_Code2=F_{Hex} and ID_Code1=F_{Hex} the ID_Code1 may be blocked by the manufacturer.

A.4 Slave profiles for standard slaves

A.4.1 Free profiles (S-X.F)

A.4.1.1 S-X.F – Definition

Slaves with free profiles are all the slaves which do not respect the definition of a particular profile. As an example, these are slaves with special communication functions, features or physical realisations for a single unique application. Nevertheless, such slaves have to follow all the AS-i specifications.

A.4.1.2 S-X.F – Codes

The I/O code may have any value between 0_{Hex} and E_{Hex}.

The ID code shall be F_{Hex}.

If an ID2 code exists in the slave, it shall be E_{Hex} or F_{Hex} according to A.4.1.4.

NOTE As ID=A_{Hex} has the special function to allow for A/B-slaves, free profiles for A/B-slaves can only be marked by ID2 (S-X.A.E).

A.4.1.3 S-X.F – Semantics of I/O data and parameters

No particular semantics for the I/O data and parameter values are defined.

A.4.1.4 S-X.F – Additional requirements

There are no additional restrictions for these slaves.

A.4.2 Remote I/Os (S-X.0)

A.4.2.1 S-X.0 – Definition

These profiles collect all the AS-i-slaves which are used as remote I/O ports with no particular meaning of the I/O data bits. Each I/O data bit is an individual remote I/O bit and there is no particular relation between the single bits. The remote I/O ports may be used to connect, for example conventional actuators, 2 and 3 wire sensors and other devices and elements to an

AS-i network. These profiles offer to the user the free access to the I/O data at the interface 1 between the AS-i-device and the AS-i-slave, as it is described in the AS-i-specification. Remote I/O devices may also have ports for energy supply from the AS-i line.

NOTE The profiles S-X.0 should also be given to push buttons with or without lamps, if there are no parameters used in the device.

A.4.2.2 S-X.0 – Codes

The I/O code may have any value between 0_{Hex} and E_{Hex}, except 9_{Hex}, B_{Hex}, and D_{Hex}.

The ID code shall be 0_{Hex}.

A.4.2.3 S-X.0 – Semantics of I/O data

The semantic of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	-	Remote I/O	0	-	-
			1	-	-
D1	-	Remote I/O	0	-	-
			1	-	-
D2	-	Remote I/O	0	-	-
			1	-	-
D3	-	Remote I/O	0	-	-
			1	-	-

For D0 to D3 no particular semantics exists. There is no particular meaning of the I/O data bits. Each I/O data bit is an individual remote I/O bit and there is no particular relation between the single bits.

A.4.2.4 S-X.0 – Semantics of parameters

The semantic of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Param.	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Param.	Input filter	0	Low	Input filter on
			1	High	Input filter off
P2	Param.	Synchronized Data I/O Mode	0	Low	Synchronized Data I/O Mode enabled
			1	High	Synchronized Data I/O Mode disabled
P3	Param.	To be defined	0	Low	To be defined
			1	High	To be defined

The meaning of P3 will be defined later. At the moment, this parameter shall not be used.

P0 shall only be used to disable a watch dog function monitoring the continuity of the communication activity of the slave.

The parameter P1 may be used to switch on an input filter that suppresses input pulses in all input channels.

For a slave to be conform with this profile, the parameter bits P0, P1 and P2 may not be used.

A.4.2.5 S-X.0 – Ports and plugs

A.4.2.5.1 S-X.0 – Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI−). On their realization there are no restrictions in addition to the specifications.

A.4.2.5.2 S-X.0 – Port of input data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, the plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = input data bit;
– pin 3 = (−) power supply;
– pin 4 = input data bit.

If Pin 2 and Pin 4 are available, Pin 2 and 4 of such a 12 mm or 8 mm plug shall be electrically bridged. The bridge shall be built in such a way, that it cannot be removed with simple tools.

A.4.2.5.3 S-X.0 – Port of output data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator) the plug shall be female with the following pinning:

– pin 1= (+) power supply in the case of a npn logic;
– pin 2= not connected;
– pin 3= (−) power supply in the case of a pnp logic;
– pin 4 = output, parameter, etc.

On the other hand, for a passive output (e.g. relay contacts) the plug shall be male with the following pinning:

– pin 1 = change-over contact;
– pin 2 = normally closed (NC) contact;
– pin 4 = normally open (NO) contact.

A.4.2.5.4 S-X.0 – Power port

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line, the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;
– pin 3 = (−) power;
– pin 4 = not used.

A.4.2.6 S-X.0 – Marking

On the enclosure the remote I/O ports shall have a clear unique identification of the available ports, such as I/O data bits and energy supply from the AS-i-system, as well as a clear identification of the pnp- or npn- logic used for the ports.

The ports for the 4 I/O data bits D0 to D3 shall be marked by the numbers 1 to 4. In general, for the unique identification of the ports, a single letter may be used, such as, for example I for input data, O for output data, etc. Only capital letters shall be used. The letters A, B, and P are reserved for antivalent I/Os, bidirectional I/Os, and parameter outputs, respectively.

A.4.2.7 S-X.0 – Additional requirements

For pnp-logic, the voltage levels and currents at the ports of a remote I/O device shall conform to IEC 61131-2. For npn-logic, the same IEC 61131-2 shall be used accordingly.

The value of the time delay for an I/O signal between the arrival at the port of a remote I/O device and the availability on the AS-i line shall be less than 5 ms for input data and 20 ms for output data. The actual value of the time delay shall be given in the product documentation.

As an option, the remote I/O output ports may have an integrated watch dog function monitoring the continuity of the communication. Such a watch dog function, however, shall not have a response time less than 40 ms. In the product documentation, it must be stated whether the remote I/O ports contain a watch dog function or not.

NOTE For remote I/O ports with an auxiliary energy supply, the availability, overload, or short circuit, etc. of the auxiliary energy may be monitored by electronic means. If such a monitor function is used, it should be realized either by using the local reset function of the slave, which inhibits the communication to the master and/or by setting the peripheral fault bit. The use of this monitor function in the remote I/O ports should be stated in the product documentation.

A.4.3 Remote I/Os with dual-signals (S-0.1, S-3.1, S-8.1)

A.4.3.1 S-X.1 – Definition

This slave profile comprises the applications of one or two binary sensors or actuators which have two data signals each. The slave profile offers the possibility to use a single monitor function for each sensor or actuator, such as, for example a warning, a failure message, a breakdown signal, etc. The slave profile includes also remote I/O devices for the connection of conventional antivalent output sensors to the AS-i line or Y-Cables for inputs and outputs.

A.4.3.2 S-X.1 – Codes

The I/O code shall be 0_{Hex}, 3_{Hex} and 8_{Hex}

The ID code shall be 1_{Hex}.

A.4.3.3 S-X.1 – Semantics of I/O data

A.4.3.3.1 X = 0 (4 inputs)

The semantics of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Input	Sensor 1	0	Low	Physical signal not detected
			1	High	Physical signal detected
D1	Input	Monitor signal 1	0	Low	Warning/failure
			1	High	Normal operation
D2	Input	Sensor 2	0	Low	Physical signal not detected
			1	High	Physical signal detected
D3	Input	Monitor signal 2	0	Low	Warning/failure
			1	High	Normal operation

D0 and D2 shall only be used as input signals from the switching elements of sensor 1 and 2, respectively, the term “physical signal” in the column “level definition” being defined in Clause A.2. If the slave is a remote I/O port to which the two sensors may be connected, then

the terms 'physical signal detected' and 'physical signal not detected' are to be replaced by “switching element in the (external) sensor closed” and “switching element in the (external) sensor open”, respectively

D1 and D3 shall only be used as monitor signal for the sensor 1 and 2, respectively. The monitor signals may indicate, for example when the corresponding sensor has a reduced functionality, is in a critical state or broken down, gives a warning, needs an inspection, etc.

The monitor signals D1 and D3 may also be the antivalent signals to the sensor function signals D0 and D2, respectively. Then, the semantics of the data bits shall be as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Input	Sensor 1	0	Low	Physical signal not detected
			1	High	Physical signal detected
D1	Input	Sensor 1	0	Low	Physical signal detected
			1	High	Physical signal not detected
D2	Input	Sensor 2	0	Low	Physical signal not detected
			1	High	Physical signal detected
D3	Input	Sensor 2	0	Low	Physical signal detected
			1	High	Physical signal not detected

A.4.3.3.2 X = 3 (2 inputs/2 outputs) or X = 8 (4 outputs)

If the slave is a remote I/O port to which sensors/actuators may be connected, then the semantics of the data bits shall be as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	-	Remote I/O	0	-	-
			1	-	-
D1	-	Remote I/O	0	-	-
			1	-	-
D2	-	Remote I/O	0	-	-
			1	-	-
D3	-	Remote I/O	0	-	-
			1	-	-

For D0 to D3 no particular semantics exists but in a common port or plug only the combination of D0/D1 or D2/D3 is allowed. There is no particular meaning of the I/O data bits. Each I/O data bit is an individual remote I/O bit and there is no relation between the single bits.

A.4.3.4 S-X.1 – Semantics of parameters

The semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Param.	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Param.	Input filter	0	Low	Input filter on
			1	High	Input filter off
P2	Param.	Synchronized Data IO Mode	0	Low	Synchronized Data IO Mode enabled
			1	High	Synchronized Data IO Mode disabled
P3	Param.	To be defined	0	Low	To be defined
			1	High	To be defined

The meaning of P3 is not defined and is reserved for future use.

The parameter P1 may be used to switch on an input filter that suppresses input pulses in all input channels.

For a slave to be conform with this slave profile the parameter bits P0, P1 and P2 may not be used.

A.4.3.5 S-X.1 – Ports and plugs

A.4.3.5.1 S-X.1 – Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI-). On their realization there are no restrictions in addition to the specifications.

A.4.3.5.2 S-X.1 – Port of input data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, the plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = input data bit D1 or D3;
– pin 3 = (−) power supply;
– pin 4 = input data bit D0 or D2.

NOTE Only the combinations D0/D1 or D2/D3 are allowed.

Appendant to each plug a second plug is allowed to provide more universal connection possibilities. This plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = not used;
– pin 3 = (−) power supply;
– pin 4 = input data bit D1 or D3.

A.4.3.5.3 S-X.1 – Port of output data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator) the plug shall be female with the following pinning:

– pin 1 = (+) power supply in the case of a npn-logic;
– pin 2 = output D1 or D3;
– pin 3 = (−) power supply in the case of a pnp-logic;
– pin 4 = output D0 or D2.

NOTE Only the combinations D0/D1 or D2/D3 are allowed.

Appendant to each plug, a second plug is allowed to provide more universal connection possibilities. This plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = not used;
– pin 3 = (−) power supply;
– pin 4 = output D1 or D3.

A.4.3.5.4 S-X.1 – Port for auxiliary energy

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;
– pin 3 = (−) power;
– pin 4 = not used.

A.4.3.6 S-X.1 – Marking

On the enclosure, the remote I/O ports shall have a clear unique identification of the available ports, such as I/O data bits and energy supply from the AS-i-system, as well as a clear identification of the pnp- or npn- logic used for the ports.

The ports for the 4 I/O data bits D0 to D3 shall be marked by the numbers 1 to 4. In general, for the unique identification of the ports a single letter may be used, such as, for example I for input data, O for output data, etc. Only capital letters shall be used. The letters A, B, and P are reserved for antivalent I/Os, bidirectional I/Os, and parameter outputs, respectively.

A.4.3.7 S-X.1 – Additional requirements

For pnp-logic, the voltage levels and currents at the ports of a remote I/O device shall conform to IEC 61131-2.

The value of the time delay for an I/O signal between the arrival at the port of a remote I/O device and the availability on the AS-i line shall be less than 5 ms for input data and 20 ms for output data. The actual value of the time delay shall be given in the product documentation.

As an option, the remote I/O output ports may have an integrated watch dog function monitoring the continuity of the communication. Such a watch dog function, however, shall not have a response time of less than 40 ms. In the product documentation, it shall be stated whether the remote I/O ports contain a watch dog function or not.

NOTE For remote I/O ports with an auxiliary energy supply, the availability, overload, or short circuit, etc. of the auxiliary energy may be monitored by electronic means. If such a monitor function is used, it should be realized either by using the local reset function of the slave, which inhibits the communication to the master and/or the periphery fault bit. The use of this monitor function in the remote I/O ports should be stated in the product documentation.

A.4.4 Single sensor with extended control (S-1.1)

A.4.4.1 S-1.1 – Definition

This profile collects the applications of single binary sensors with an increased functionality, i.e. the profile offers the possibility to use different sensor monitor and control functions and allows a binary parametrizing of the sensor.

A.4.4.2 S-1.1 – Codes

The I/O code shall be 1_{Hex}.

The ID code shall be 1_{Hex}.

A.4.4.3 S-1.1 – Semantics of I/O data

The semantics of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Input	Sensor function	0	Low	Physical signal not detected
			1	High	Physical signal detected
D1	Input	Warning	0	Low	Warning on
			1	High	Warning off
D2	Input	Availability	0	Low	Not available
			1	High	Available
D3	Output	Test	0	High	Test function inactive
			1	Low	Test function active

D0 shall only be used as input for the status of the switching element in the sensor, the term "physical signal" in the column "level definition" being defined in Clause A.2. If the slave is a remote I/O port to which the two sensors may be connected, then the terms "physical signal detected" and "physical signal not detected" shall be replaced by "switching element in the (external) sensor closed" and "switching element in the (external) sensor open", respectively

D1 shall only be used as a warning signal. It indicates that the sensor is working, but, has a reduced functionality or needs an inspection.

D2 shall monitor the availability of the sensor only. A breakdown of the device may be signalized by this bit.

D3 shall start a functional test of the sensor only.

For a slave to be conform with this profile, the data bits D1 to D3 do not have to be used. A master request on data bits not used shall always yield an AS-i high level.

A.4.4.4 S-1.1 – Semantics of parameters

A.4.4.4.1 S-1.1 – Inductive proximity switches

For inductive proximity switches, the semantic of the parameter bits is summarised as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Param.	Timer	0	Low	Timer function on
			1	High	Timer function off
P1	Param.	Inversion of D0	0	Low	Inversion of D0
			1	High	D0 as specified
P2	Param.	Range	0	Low	Low range
			1	High	High range
P3	Param.	Special function	0	Low	Special function
			1	High	Basic function

P0 shall only be used to activate a timer function.

P1 shall only be used to invert the level-definition of D0.

P2 shall only be used to select between two different ranges of the sensor, for example between single and double distance range.

P3 shall only be used to set a special function of the sensor. Such a function may be, for example a special mode, a teach-in, a reset of the sensor, etc.

For a slave to be conform with this profile, the parameter bits P0 to P3 do not have to be used.

A.4.4.4.2 S-1.1 – Photoelectric proximity switches

For photoelectric proximity switches the semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Param.	Working frequency	0	Low	Low working frequency
			1	High	High working frequency
P1	Param.	Inversion of D0	0	Low	Inversion of D0
			1	High	D0 as specified
P2	Param.	Timer	0	Low	Timer function on
			1	High	Timer function off
P3	Param.	Special function	0	Low	Special function
			1	High	Basic function

P0 shall only be used to change the working frequency of the sensor.

P1 shall only be used to invert the level-definition of D0.

P2 shall only be used to activate a timer function.

P3 shall only be used to set a special function of the sensor. Such a function may be, for example a special mode, a teach-in, a reset of the sensor, etc.

For a slave to be conform with this profile the parameter bits P0 to P3 do not have to be used. A master request on parameter bits not used shall always yield an AS-i high level.

A.4.4.4.3 S-1.1 – Other sensors

For other sensors, the semantics of P0 to P3 will be defined later. At the moment, this profile may be applied, but the parameters P0 to P3 shall not be used.

For a slave to be conform with this profile, the parameter bits P0 to P3 do not have to be used. A master request on parameter bits not used shall always yield an AS-i high level.

A.4.4.5 S-1.1 – Additional requirements

The detailed functions of the single data bits and parameter bits used for a particular sensor shall be described in the product documentation of the sensor.

A.4.5 Motor control devices (S-7.D and S-7.E)

A.4.5.1 S-7.D/E – Definition

This slave profile applies to devices for the command and control of one motor.

These devices are divided into two groups and are described below.

A.4.5.2 S-7.D – Electromechanical motor control devices

Electromechanical contactors and motor-starters (IEC 60947-4-1):

– direct on line (full voltage) a.c. starters (non reversing or reversing);
– reduced voltage a.c. starters:
  • star-delta starters,

- part winding starters,
- auto transformers starters;

– combination starters;

– protected starters.

NOTE Starters or protected starters equipped with solid-state overload relays should be considered as electromechanical starters (IEC 60947-4-1).

A.4.5.3 S-7.E – Semiconductor motor control devices

Semiconductor motor controllers and starters (IEC 60947-4-2):

– semiconductor direct on line motor starters;

– semiconductor soft-start motor starters.

Low voltage adjustable frequency a.c. power drive systems (as defined in IEC 61800-2):

– simple drives controlled by pre-set speeds;

– etc.

NOTE When the motor starter is hybrid (semiconductor and electromechanical) it is considered as a semiconductor starter (3.1.2 of IEC 60947-4-2).

This profile enables the connection of auxiliary devices to the starter, such as, for example sensors or lamps, for decentralized applications.

A.4.5.4 S-7.D/E glossary

In addition to the definitions given in this standard, and in Clause A.2, the following definitions apply:

Definition	Index
‘’a’’ contact - make contact	22
‘’b’’ contact - break contact	23
a.c. semiconductor motor controller	9
Auxiliary contact	21
Combination starter	4
Contactor (mechanical)	1
Control contact	20
Direct on line starter	5
Over-current	14
Overload	16
Protected starter	3
Reduced voltage starter	7
Relay (electrical)	18
Release (of a mechanical switching device)	19
Reversing starter	6
Semiconductor direct on line (DOL) motor controller (form 3)	12
Semiconductor motor controller (form 1)	10
Semiconductor motor starter	13
Semiconductor soft start motor controller (form 2)	11
Semiconductor switching device	8
Short circuit	15
Starter	2
Tripping (operation)	17

Index:

1. Contactor (mechanical)
A mechanical switching device having only one position of rest, operated otherwise than by hand, capable of making, carrying and breaking currents under normal circuit conditions including operating overload conditions (2.2.12 of IEC 60947-1).

2. Starter
The combination of all the switching means necessary to start and stop a motor, in combination with suitable overload protection. (2.2.15 of IEC 60947-1).

3. Protected starter
Equipment consisting of a starter, a manually-operated switching device and a short-circuit protective device, mounted and wired, enclosed or unenclosed according to the instructions of the starter manufacturer. (3.2.8 of IEC 60947-4-1).

4. Combination starter
Equipment consisting of a starter, a manual externally-operated switching device and a short-circuit protective device, mounted and wired in a dedicated enclosure. The switching and short-circuit protective devices may be a fuse combination unit, a switch with fuses or circuit breaker with or without an isolating function (3.2.7 of IEC 60947-4-1).

5. Direct on line starter
A starter which connects the line voltage across the motor terminals in one step. (3.2.2 of IEC 60947-4-1).

6. Reversing starter
A starter intended to cause the motor to reverse the direction of rotation by reversing the motor primary connections while the motor may be running. (3.2.3 of IEC 60947-4-1).

7. Reduced voltage starter
A starter which connects the line voltage across the motor terminals in more than one step or by gradually increasing the voltage applied to the terminals. (3.2.5 of IEC 60947-4-1)

8. Semiconductor switching device
A switching device designed to make and/or break the current in an electric circuit by means of the controlled conductivity of a semiconductor. (2.2.3 of IEC 60947-1)

9. AC semiconductor motor controller
A semiconductor switching device that provides a starting function for an a.c. motor and an OFF-state.

NOTE Because dangerous levels of leakage currents can exist in semiconductor motor controller in the OFF-state, the load terminals should be considered as being live at all times (3.1.1.1 of IEC 60947-4-2).

10. Semiconductor motor controller (form 1)
An a.c. semiconductor motor controller, in which the starting function may comprise any starting method specified by the manufacturer, and that provides control functions which may include any combination of manoeuvring, controlled acceleration, running, or controlled deceleration of an a.c. motor. A FULL-ON state may also be provided (3.1.1.1 1 of IEC 60947-4-2).

11. Semiconductor soft start motor controller (form 2)
A special form of a.c. semiconductor motor controller, in which the starting function is limited to a voltage and/or current ramp which may include controlled acceleration, and where the additional control function is limited to providing FULL-ON (3.1.1.1.2 of IEC 60947-4-2).

12. Semiconductor direct on line (DOL) motor controller (form 3)
A special form of a.c. semiconductor motor controller, in which the starting function is limited to a full voltage, unramped starting method only, and where the additional control function is limited to providing FULL-ON (3.1.1.1.3 of IEC 60947-4-2).

13. Semiconductor motor starter
An a.c. semiconductor motor controller with suitable overload protection, rated as a unit (3.1.1.2 of IEC 60947-4-2).

14. Over-current
A current exceeding the rated current (2.1.4 of IEC 60947-1).

15. Short circuit
The accidental or intentional connection, by a relatively low resistance or impedance, of two or more points in a circuit which are normally at different voltages (2.1.5 of IEC 60947-1, modified).

16. Overload
Operating conditions in an electrically undamaged circuit which cause an over-current (2.1.7 of IEC 60947-1).

17. Tripping (operation)
An opening operation of a mechanical switching device initiated by a relay or release (2.4.22 of IEC 60947-1).

18. Relay (electrical)
A device designed to produce sudden, predetermined changes in one or more electrical output circuits when certain conditions are fulfilled in the electrical input circuits controlling the device (2.3.14 of IEC 60947-1).

19. Release (of a mechanical switching device)
A device, mechanically connected to a mechanical switching device, which releases the holding means and permits the opening or the closing of the switching device (2.3.15 of IEC 60947-1).

20. Control contact
A contact included in a control circuit of a mechanical switching device and mechanically operated by this device (2.3.9 of IEC 60947-1).

21. Auxiliary contact
A contact included in an auxiliary circuit and mechanically operated by the switching device (2.3.10 of IEC 60947-1).

22. ''a'' contact - make contact
A control or auxiliary contact which is closed when the main contacts of the mechanical switching device are closed and open when they are open (2.3.12 of IEC 60947-1).

23. ''b'' contact - break contact
A control or auxiliary contact which is open when the main contacts of the mechanical switching device are closed and closed when they are open (2.3.13 of IEC 60947-1).

A.4.5.5 S-7.D/E – Semantics of outputs (commands from controller to device)

A.4.5.5.1 S-7.D/E – Run forward

If a main run forward command for the motor is used it shall be D0 output.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D0	Output	Run forward	0	High	Stop motor in forward direction
			1	Low	Run motor in forward direction

A.4.5.5.2 S-7.D/E – Run reverse

For a reverser, D0 and D1 outputs shall only be used as run commands for the motor, D0 in a sense and D1 in the other sense. These commands are mandatory for reversers.

D0 shall correspond to the direct connection of the line voltage to the motor terminals, D1 to the reverse connection.

The semantics of the run commands is summarized as follows:

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D0	Output	Run forward	0	High	Stop motor in forward direction
			1	Low	Run motor in forward direction
D1	Output	Run reverse	0	High	Stop motor in reverse direction
			1	Low	Run motor in reverse direction

D0-D1 output controller-level	D1 output controller-level	D0 output controller-level	Meaning
0	0	0	Stop
1	0	1	Run forward
2	1	0	Run reverse

When D0 and D1 have controller-level 1 at the same time, the behaviour of the device depends on the product.

It may either

– stop, or
  go into default, or
– stay in the state it had before, or
– be reset (see reset command), or
– have another behaviour depending on the product.

A.4.5.5.3 S-7.D/E – Brake

If a brake command is used, it shall be D2.

When a starter drives two motors, this command can be used to drive the two brakes at the same time.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D2	Output	Brake	0	High	Brake contact inactive, motor blocked
			1	Low	Brake contact active, motor free

A.4.5.5.4 S-7.D/E – Fault reset

Through this command, the device is remote reset from the controller.

This command may be used to reset:

– an overload trip (semiconductor overload relay);
– a stored external fault signal (this signal can be available through a special information);
– a stored inappropriate local operation;
– any other resetable fault depending on the type of starter.

During the fault reset command, the device may go in a predefined reset state.

If a fault reset command is used, it shall be D3.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D3	Output	Fault reset	0	High	Reset inactive
			1	Low	Reset active

If a fault reset command is needed, and the command D3 is not available for this purpose, a combination of D0 and D1 may be used.

D0-D1 output controller-level	D1 output controller-level	D0 output controller-level	Meaning
0	0	0	Stop
1	0	1	Run forward
2	1	0	Run reverse
3	1	1	Fault reset

When D3 is available, it is recommended to use it instead of this combination of D0 and D1.

A.4.5.5.5 S-7.D/E – Special commands

The use of D2 and D3 outputs is not restricted to those mentioned above. It may be dedicated to special commands, for example:

– auxiliary lamp control;
– auxiliary actuator (e.g. cam);
– etc.

A.4.5.5.6 S-7.D/E – Semantics of inputs (control signal from device to controller)

A.4.5.5.7 S-7.D/E – Ready

D0 input shall only be used to indicate a fault or a missing condition to allow a command coming from controller. This control signal is mandatory.

Faults are described below.

The missing condition for starting can consist of

– local power switch off (e.g. for a combination starter),
– local operation,
– etc.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D0	Input	Ready	0	Low	Not ready or fault
			1	High	Ready

A.4.5.5.8 S-7.D/E – Running

D1 input shall only be used for the running signal from the device. This control signal is mandatory.

In a reverser, the running indication has to be active, in each sense, whatever the direction control signal is used or not.

As different technologies can be used to obtain this running signal (make or break auxiliary contact, voltage or/and current control), this information depends on the type of device. It is precisely defined in the sub-profile (see A.4.2.5.2 or A.4.2.5.3).

If the device is an electromechanical starter, the running information indicates if the starter is switched on or off. It does not necessarily mean that the motor is running (for example in case a loss of power not detected by the starter).

If the device is an a.c. motor drive, the running information generally means that the drive provides current to the motor.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D1	Input	Running	0	Low	Starter inactive
			1	High	Starter active

If the device is a electromechanical starter, equipped with break auxiliary contact, the AS-i slave interface should invert the signal so that the running information is directly used by the controller.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D1	Input	Running	0	Low	Motor not in rotation or motor in free wheel stop
			1	High	Motor running (acceleration ramp, regulation at speed reference, deceleration ramp, …)

NOTE If the starter is in manually controlled operation, it is not ready (because a command from the controller has no effect). In this case, the running information can indicate that the actuator is active because of a local forced command to on.

A.4.5.5.9 S-7.D/E – Fault

If a fault control signal is used, it shall be D2.

A fault can consist of

– the reaction of a protective device which has produced a tripping operation (overcurrent, motor overheating, phase failure, phase imbalance, underload, etc.),
– an internal failure of the motor control device (starter overheating, welding of a contactor, needs commissioning, power on test failed, etc.),
– a periphery fault (overload of the power supply, loss of power supply, etc.),
– etc.

A warning indication does not produce a fault.

If the device is a electromechanical starter, equipped with break auxiliary contact, the AS-i slave interface should invert the signal so that the fault information is directly used by the controller.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D2	Input	Fault	0	-high-low	No fault
			1	-low-high	Fault

A.4.5.5.10 S-7.D/E – Warning

If a warning indication is used, it shall be D3 or diagnosis parameters.

A warning indication can consist of

– an indication of overcurrent or motor overheating which will cause a trip if it lasts longer,
– etc.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D3	Input	Warning	0	-high-low	No warning
			1	-low-high	Warning

A.4.5.5.11 S-7.D/E – Direction

If a direction indication is used, it shall be D3.

This information is valid only when the device is running.

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition
D3	Input	Direction	0	-high-low	Forward
			1	-low-high	Reverse

Running D1 input controller-level	Direction D3 input controller-level	Meaning
0	0	Not running (stopped)
1	0	Running forward
1	1	Running reverse
0	1	Not used

A.4.5.5.12 S-7.D/E – Special information

The use of D2 and D3 is not restricted to those mentioned above. It may be used to monitor a special function related to the type of device, for example

– signal from auxiliary sensor;
– local / remote control;
– indication of short-circuit trip (differentiation with overload trip);
– etc.

If the motor control device is in remote mode, it accepts the commands from the controller via the bus.

If the motor control device is in local mode, the controller cannot command the device.

The choice local mode / remote mode is generally done:

– by a selector connected (hard-wire) on the device,
– by a keypad located on the device,
– etc.

A combination of fault and warning signals is accepted to differentiate overload trip from short-circuit trip. It should be:

Inputs (controller-level)		Meaning
D2	D3	
0	0	No fault nor warning
0	1	Overload warning
1	0	Overload trip
1	1	Short-circuit trip

A.4.5.5.13 S-7.D/E – Semantics of parameters

The use of parameters is optional.

For the slave conformance to the motor control device profile, the parameter bits P0 to P3 do not have to be used. A master request on parameter bits not used shall always yield an AS-i high level (controller-level 1).

A.4.5.5.14 S-7.D/E – Watchdog

If a parameter is used to enable a watchdog function, monitoring the continuity of the communication activity of the slave, it shall be parameter P0.

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Watch dog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled

The watchdog function shall be realized in such a way that it has a response time larger than 40 ms and sets the actuators inactive or in a predefined state (fallback position).

If the watchdog is disabled, whenever a communication failure occurs, the last command is maintained.

The default controller-value for the parameters of the slaves is 1, which corresponds to an enabled watchdog. So that, if no particular configuration of the parameters is done (for example master with M0 profile), the device will be in a safe configuration regarding most applications.

A.4.5.5.15 S-7.D/E – Fallback

If the fallback position can be configured by a parameter, it shall be parameter P1. The default controller-value for the P1 parameter is 1, which corresponds to a fallback position to off.

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Parameter	Fallback position	0	Low	Fallback position to run
			1	High	Fallback position to stop

If there is no possibility to configure the run fallback position (P2, P3, switches or others), it shall be forward.

A.4.5.5.16 S-7.D/E – Extended diagnosis

An extended diagnosis function can be implemented optionally. If it is, it shall be as described below.

When the motor control device or the motor are not in order, which is indicated by

– ready signal (mandatory),
– fault signal (optional),
– warning signal (optional),

the controller can get more details using the extended diagnosis procedure based on input parameters.

Fault and warning are encoded as defined in the table below. The use of any value not defined yet, is not allowed.

Parameter (controller-level)				Meaning
P0	P1	P2	P3	
0	0	0	0	No fault nor warning
0	0	0	1	Overload warning
0	0	1	0	Overload trip
0	0	1	1	Short-circuit trip
0	1	0	0	Switched off (main power switch)
0	1	0	1	Local operation (local / remote selector)

A.4.5.5.17 S-7.D/E – Codes

The I/O code shall be 7_{Hex}.

The ID code shall be

– D_{Hex} for electromechanical motor control devices,

– E_{Hex} for semiconductor motor control devices.

NOTE The motor control devices have to be divided into at least two classes because electromechanical motor control devices provide for an isolation function, but semiconductor motor control devices do not. So, it can be dangerous for the user to interchange products from different classes. The differentiation by the ID code enables the controller to detect hazardous maintenance operations.

The profiles for simple devices such as basic direct on line starters or reversers are very similar in the two classes. But more complex devices require totally different commands and control signals. For example a two-speed motor starter for two separate winding motors will not be defined like a variable speed drive.

To ensure a maximum of interchangeability provided by the extended ID2 code, the D3 optional commands and control signals have to be limited. This can be performed only if these options are related to a restricted class. For ID2 codes see tables below.

A.4.5.5.18 S-7.D/E – Minimum requirements for motor control profile

A minimum set of I/O is required to fulfil the motor control profile. The use of special data is either open (subprofile 0) or defined in the subprofile.

The semantics of the minimum set of I/O data bits is summarized as follows:

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run command 1	0	High	Motor command 1 off	Mandatory
			1	Low	Motor command 1 on	
D1	Output	Run command 2	0	High	Motor command 2 off	Optional
			1	Low	Motor command 2 on	
D2	Output	Special command 1	0	High	Special command 1 off	Optional
			1	Low	Special command 1 on	
D3	Output	Special command 2	0	High	Special command 2 off	Optional
			1	Low	Special command 2 on	

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Not running	Mandatory
			1	High	Running	
D2	Input	Special information 1	0	Low	Special information 1 off	Optional
			1	High	Special information 1 on	
D3	Input	Special information 2	0	Low	Special information 2 off	Optional
			1	High	Special information 2 on	

According to the type of motor control device, the run commands can be different. But they shall be as follows, if listed:

Type of motor control device	D0 run command 1	D1 run command 2
Direct on line starter	Run forward	
Reverser	Run forward	Run reverse
2 speed starter	Run speed 1	Run speed 2
Dual starter	Run starter 1	Run starter 2

The use of parameters is free.

A.4.5.6 S-7.D – Profiles for electromechanical motor control devices

A.4.5.6.1 S-7.D – Profile catalogue

Table A.5 – Profile catalogue of S-7.D profiles

IO conf	ID code	Extended ID code 2	Definition
7	D	0	Motor control device open sub-profile
7	D	1	Electromechanical direct starter
7	D	2	Electromechanical reverser
7	D	3	Electromechanical direct starter with brake
7	D	4	Electromechanical reverser with brake
7	D	5	Electromechanical direct starter with auxiliaries
7	D	6	Electromechanical reverser with auxiliaries
7	D	7 to D	Reserved

A.4.5.6.2 S-7.D – Overview of data

Table A.6 – Overview of data of S-7.D profiles

Profile code	Profile definition	Semantics of I/O							
		Outputs				Inputs			
		D0	D1	D2	D3	D0	D1	D2	D3
7.D.0	Electromechanical motor control device open sub-profile	Run command 1	Run command 2	Free	Free	Ready	Running	Free	Free
7.D.1	Electromechanical direct starter	run forward	Not used	Not used	Free	Ready	Running	Fault	Free
7.D.2	Electromechanical reverser	Run forward	Run reverse	Not used	Free	Ready	Running	Fault	Free
7.D.3	Electromechanical direct starter with brake	Run forward	Not used	Brake	Free	Ready	Running	Fault	Free
7.D.4	Electromechanical reverser with brake	Run forward	Run reverse	Brake	Free	Ready	Running	Fault	Free
7.D.5	Electromechanical direct starter with auxiliaries	Run forward	Not used	Auxiliary actuator	Free	Ready	Running	Sensor signal	Free
7.D.6	Electromechanical reverser with auxiliaries	Run forward	Run reverse	Auxiliary actuator	Free	Ready	Running	Sensor signal	Free

The use of parameters is free.

A.4.5.6.3 S-7.D – Sub-profiles for electromechanical motor control devices

A.4.5.6.4 S-7.D.0 – Electromechanical motor control device open sub-profile

Extended profile code 7.D.0

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run command 1	0	High	Motor command 1 off	Mandatory
			1	Low	Motor command 1 on	
D1	Output	Run command 2	0	High	Motor command 2 off	Optional
			1	Low	Motor command 2 on	
D2	Output	Special command 1				Optional
D3	Output	Special command 2				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Not running	Mandatory
			1	High	Running	
D2	Input	Special information 1				Optional
D3	Input	Special information 2				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.6.5 S-7.D.1. Electromechanical direct starter

Extended profile code 7.D.1

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor	Mandatory
			1	Low	Run motor	
D1	Output	Not used				Mandatory
D2	Output	Not used				Mandatory
D3	Output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller -level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.6.6 S-7.D.2. Electromechanical reverser

Extended profile code 7.D.2

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor in forward direction	Mandatory
			1	Low	Run motor in forward direction	
D1	Output	Run reverse	0	High	Stop motor in reverse direction	Mandatory
			1	Low	Run motor in reverse direction	
D2	Output	Not used				Mandatory
D3	Output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.6.7 S-7.D.3. Electromechanical direct starter with brake

Extended profile code 7.D.3

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor	Mandatory
			1	Low	Run motor	
D1	Output	Not used				Mandatory
D2	Output	Brake	0	High	Motor blocked	Mandatory
			1	Low	Motor free	
D3	Output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.6.8 S-7.D.4. Electromechanical reverser with brake

Extended profile code 7.D.4

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor in forward direction	Mandatory
			1	Low	Run motor in forward direction	
D1	Output	Run reverse	0	High	Stop motor in reverse direction	Mandatory
			1	Low	Run motor in reverse direction	
D2	Output	Brake	0	High	Motor blocked	Mandatory
			1	Low	Motor free	
D3	Output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional
						Optional

A.4.5.6.9 S-7.D.5. Electromechanical direct starter with auxiliaries

Extended profile code 7.D.5

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor	Mandatory
			1	Low	Run motor	
D1	Output	Not used				Mandatory
D2	Output	Auxiliary actuator 1	0	High	Set auxiliary actuator 1 inactive	Mandatory
			1	Low	Set auxiliary actuator 1 active	
D3	Output	Special command (auxiliary actuator 2)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Sensor signal 1	0	High	Signal from sensor 1 not detected	Mandatory
			1	Low	Signal from sensor 1 detected	
D3	Input	Special information (sensor signal 2)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.6.10 S-7.D.6. Electromechanical reverser with auxiliaries

Extended profile code 7.D.6

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor in forward direction	Mandatory
			1	Low	Run motor in forward direction	
D1	Output	Run reverse	0	High	Stop motor in reverse direction	Mandatory
			1	Low	Run motor in reverse direction	
D2	Output	Auxiliary actuator 1	0	High	Set auxiliary actuator 1 inactive	Mandatory
			1	Low	Set auxiliary actuator 1 active	
D3	Output	Special command (auxiliary actuator 2)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Sensor signal 1	0	High	Signal sensor 1 not detected	Mandatory
			1	Low	Signal from sensor 1 detected	
D3	Input	Special information (sensor signal 2)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.7 S-7.E – Profiles for semiconductor motor control devices

A.4.5.7.1 S-7.E – Profile catalogue

Table A.7 – Profile catalogue of S-7.E profile

IO conf	ID code	Extended ID code 2	Definition
7	E	0	Motor control device open sub-profile
7	E	1	Semiconductor direct starter
7	E	2	Semiconductor reverser
7	E	3	Semiconductor direct starter with brake
7	E	4	Semiconductor reverser with brake
7	E	5	Semiconductor direct starter with auxiliaries
7	E	6	Semiconductor reverser with auxiliaries
7	E	7 to D	Reserved

A.4.5.7.2 S-7.E – Overview of data

Table A.8 – Overview of data of S-7.E profiles

Profile code	Profile definition	Semantics of I/O							
		Outputs				inputs			
		D0	D1	D2	D3	D0	D1	D2	D3
7.E.0	Semiconductor motor control device open sub-profile	Run command 1	Run command 2	Free	Free	Ready	Running	Free	Free
7.E.1	Semiconductor direct starter	Run forward	Not used	not used	Free	Ready	Running	Fault	Free
7.E.2	Semiconductor reverser	Run forward	Run reverse	Not used	Free	Ready	Running	Fault	Free
7.E.3	Semiconductor direct starter with brake	Run forward	Not used	Brake	Free	Ready	Running	Fault	Free
7.E.4	Semiconductor reverser with brake	Run forward	Run reverse	Brake	Free	Ready	Running	Fault	Free
7.E.5	Semiconductor direct starter with auxiliaries	Run forward	Not used	auxiliary actuator	Free	Ready	Running	Sensor signal	Free
7.E.6	Semiconductor reverser with auxiliaries	Run forward	Run reverse	Auxiliary actuator	Free	Ready	Running	Sensor signal	Free

The use of parameters is free.

A.4.5.7.3 S-7.E – Sub-profiles

A.4.5.7.4 S-7.E.0 Semiconductor motor control device open sub-profile

Extended profile code 7.E.0

Bit	Type for controller	Meaning	Controller -level	As-i-level	Level-definition	
D0	Output	Run command 1	0	High	Motor command 1 off	Mandatory
			1	Low	Motor command 1 on	
D1	Output	Run command 2	0	High	Motor command 2 off	Optional
			1	Low	Motor command 2 on	
D2	Output	Special command 1				Optional
D3	Output	Special command 2				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Not running	Mandatory
			1	High	Running	
D2	Input	Special information 1				Optional
D3	Input	Special information 2				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.7.5 S-7.E.1 Semiconductor direct starter

Extended profile code 7.E.1

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor	Mandatory
			1	Low	Run motor	
D1	Output	Not used				Mandatory
D2	Output	Not used				Mandatory
D3	Output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.7.6 S-7.E.2 Semiconductor reverser

Extended profile code 7.E.2

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor in forward direction	Mandatory
			1	Low	Run motor in forward direction	
D1	Output	Run reverse	0	High	Stop motor in reverse direction	Mandatory
			1	Low	Run motor in reverse direction	
D2	Output	Not used				Mandatory
D3	output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.7.7 S-7.E.3. Semiconductor direct starter with brake

Extended profile code 7.E.3

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor	Mandatory
			1	Low	Run motor	
D1	Output	Not used				Mandatory
D2	Output	Brake	0	High	Motor blocked	Mandatory
			1	Low	Motor free	
D3	Output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller -level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.7.8 S-7.E.4. Semiconductor reverser with brake

Extended profile code 7.E.4

Bit	Type for controller	Meaning	Controller -level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor in forward direction	Mandatory
			1	Low	Run motor in forward direction	
D1	Output	Run reverse	0	High	Stop motor in reverse direction	Mandatory
			1	Low	Run motor in reverse direction	
D2	Output	Brake	0	High	Motor blocked	Mandatory
			1	Low	Motor free	
D3	output	Special command (fault reset)				Optional

Bit	Type for controller	Meaning	Controller -level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Fault	0	High	No fault	Mandatory
			1	Low	Fault	
D3	Input	Special information (warning)				Optional

Bit	Type	Meaning	Controller -level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.7.9 S-7.E.5. Semiconductor direct starter with auxiliaries

Extended profile code 7.E.5

Bit	Type for controller	Meaning	Controller -level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor	Mandatory
			1	Low	Run motor	
D1	Output	Not used				Mandatory
D2	Output	Auxiliary actuator 1	0	High	Set auxiliary actuator 1 inactive	Mandatory
			1	Low	Set auxiliary actuator 1 active	
D3	Output	Special command (auxiliary actuator 2)				Optional

Bit	Type for controller	Meaning	Controller -level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Sensor signal 1	0	High	Signal sensor 1 not detected	Mandatory
			1	Low	Signal from sensor 1 detected	
D3	Input	Special information (sensor signal 2)				Optional

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.5.7.10 S-7.E.6. Semiconductor reverser with auxiliaries

Extended profile code 7.E.6

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Output	Run forward	0	High	Stop motor in forward direction	Mandatory
			1	Low	Run motor in forward direction	
D1	Output	Run reverse	0	High	Stop motor in reverse direction	Mandatory
			1	Low	Run motor in reverse direction	
D2	Output	Auxiliary actuator 1	0	High	Set auxiliary actuator 1 inactive	Mandatory
			1	Low	Set auxiliary actuator 1 active	
D3	Output	Special command (auxiliary actuator 2)				Optional

Bit	Type for controller	Meaning	Controller-level	As-i-level	Level-definition	
D0	Input	Ready	0	Low	Not ready or fault	Mandatory
			1	High	Ready	
D1	Input	Running	0	Low	Actuator is inactive	Mandatory
			1	High	Actuator is active	
D2	Input	Sensor signal 1	0	High	Signal sensor 1 not detected	Mandatory
			1	Low	Signal from sensor 1 detected	
D3	Input	Special information (sensor signal 2)				Optional

Bit	Type	Meaning	Controller -level	As-i-level	Level-definition	
P0	Parameter	Special parameter 1				Optional
P1	Parameter	Special parameter 2				Optional
P2	Parameter	Special parameter 3				Optional
P3	Parameter	Special parameter 4				Optional

A.4.6 Dual actuator with feedback (S-B.1)

A.4.6.1 S-B.1 – Definition

This slave profile collects the applications of dual actuators with feedback signals, such as, for example, two-directional pneumatic or hydraulic cylinders, two-directional motors, etc. The actual position or movement of the actuator is indicated by two feedback signals.

A.4.6.2 S-B.1 – Codes

The I/O code shall be B_{Hex}.

The ID code shall be 1_{Hex}.

A.4.6.3 S-B.1 – Semantics of I/O data

The semantic of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Output	Command actuator 1	0	High	Set actuator 1 inactive
			1	Low	Set actuator 1 active
D1	Output	Command actuator 2	0	High	Set actuator 2 inactive
			1	Low	Set actuator 2 active
D2	Input	Feedback from 1	0	Low	Actuator 1 is inactive
			1	High	Actuator 1 is active
D3	Input	Feedback from 2	0	Low	Actuator 2 is inactive
			1	High	Actuator 2 is active

D0 and D2 shall only be used as command outputs for the actuator 1 and 2, respectively.

D2 and D3 shall only be used for the feedback signals of actuator 1 and 2, respectively. A feedback signal indicating an active actuator always means that the actuator is in action/movement or has reached a defined state/position.

A.4.6.4 S-B.1 – Semantics of parameters

The semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Parameter	Interlock 1 and 2	0	Low	1 and 2 interlocked
			1	High	No interlock
P2	Parameter	Remote reset	0	Low	Start remote reset
			1	High	Normal operation
P3	Parameter	Special function	0	Low	Special function
			1	High	Basic function

P0 shall only be used to disable a watchdog function monitoring the continuity of the communication activity of the slave.

P1 shall only be used to activate an interlock of the actuators 1 and 2. If P1 is in operation and set to its AS-i low level it shall be prohibited to set both actuators active at the same time. A simultaneous activation of both actuators shall then result in setting both actuators inactive.

P2 shall only be used as remote reset. A remote reset may, for example restart the actuator out of a fault state, set the actuator to a defined initial state/position, etc.

P3 shall only be used to activate special functions, such as, for example timer, speed-up, test, etc.

For a slave to be conform with this profile, the parameter bits P0 to P3 do not have to be used.

A.4.6.5 S-B.1 – Additional requirements

The detailed function of the single data bits and parameter bits used shall be described in the product documentation.

A.4.7 Single actuator with monitoring (S-D.1)

A.4.7.1 S-D.1 – Definition

This slave profile collects the applications of single actuators with extended monitor functions, such as, for example for motor feeders, etc. The state of the actuator may be monitored by up to three bits of information.

A.4.7.2 S-D.1 – Codes

The I/O code shall be D_{Hex}.

The ID code shall be 1_{Hex}.

A.4.7.3 S-D.1 – Semantics of I/O data

The semantic of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Output	Command	0	High	Set actuator inactive
			1	Low	Set actuator active
D1	Input	Feedback	0	Low	Actuator is inactive
			1	High	Actuator is active
D2	Input	Fault	0	Low	Fault
			1	High	No fault
D3	Input	Availability	0	Low	Not available
			1	High	Available

D0 shall only be used as command output for the actuator.

D1 shall only be used for the feedback signals of the actuator. The feedback signal indicating an active actuator always means that the actuator is in action/movement or it has reached a defined state/position.

D2 shall only be used to indicate a fault condition. The fault messages are the reaction of a protection device and may indicate, for example overload, overtemperature, overcurrent, tripping of a motor, etc.

D3 shall monitor the availability of the actuator only.

A.4.7.4 S-D.1 – Semantics of parameters

The semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Parameter	Timer	0	Low	Timer enabled
			1	High	Timer disabled

P2	Parameter	Remote reset	0	Low	Start remote reset
			1	High	Normal operation
P3	Parameter	Special function	0	Low	Special function
			1	High	Basic function

P0 shall only be used to disable a watchdog function monitoring the continuity of the communication activity of the slave.

P1 shall only be used to activate a timer function in the actuator.

P2 shall only be used as remote reset. A remote reset may, for example restart the actuator out of a fault state, set the actuator to a defined initial state/position, etc.

P3 shall only be used to activate special functions, such as, for example speed-up, test, etc.

For a slave to be conform with this profile, the parameter bits P0 to P3 do not have to be used.

A.4.7.5 S-D.1 – Additional requirements

The detailed function of the single data bits and parameter bits used shall be described in the product documentation.

A.5 Slave profiles for slaves in extended addressing mode (S-X.A)

A.5.1 Free profiles in extended addressing mode (S-X.A.E)

A.5.1.1 S-X.A.E – Definition

Slaves with free profiles are all the slaves which do not respect the definition of a particular profile. As an example, these are slaves with special communication functions, features or physical realisations for a single unique application. Nevertheless, such slaves have to follow all the AS-i requirements.

A.5.1.2 S-X.A.E – Codes

The I/O code may have any value between 0_{Hex} and E_{Hex}, except 2_{Hex} and A_{Hex}.

The ID code shall be A_{Hex}.

If an ID2 code exists in the slave, it shall be E_{Hex} according to 4.1.4.

NOTE As ID=A_{Hex} has the special function to allow for A/B-slaves, free profiles for A/B-slaves can only be marked by ID2.

A.5.1.3 S-X.A.E – Semantics of I/O data and parameters

No particular semantics for the I/O data and parameter values are defined.

A.5.1.4 S-X.A.E – Additional requirements

There are no additional restrictions for these slaves.

A.5.2 Remote I/Os in extended addressing mode (S-X.A.0

A.5.2.1 S-X.A.0 – Definition

These sub-profiles collect all the AS-i-slaves for extended address capabilities which are used as remote I/O ports with no particular meaning of the I/O data bits. Each I/O data bit is an individual remote I/O bit and there is no particular relation between the single bits. The remote I/O ports may be used to connect, for example conventional actuators, 2 and 3 wire sensors and other devices and elements to an AS-i network. These profiles offer to the user the free access to the I/O data at the interface 1 between the AS-i-device and the AS-i-slave, as it is described in this standard. Remote I/O devices may also have ports for energy supply from the AS-i line.

NOTE The profiles S-X.A.0 should also be given to push buttons with or without lamps.

A.5.2.2 S-X.A.0 – Codes

The I/O code may have any value between 0_{Hex} and E_{Hex}, except 2_{Hex} and A_{Hex}.

The ID code shall be A_{Hex}.

The ID2-code shall be 0_{Hex}.

A.5.2.3 S-X.A.0 – Semantics of I/O data

The semantics of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	-	Remote I/O	0	-	-
			1	-	-
D1	-	Remote I/O	0	-	-
			1	-	-
D2	-	Remote I/O	0	-	-
			1	-	-
D3	-	Remote I	0	-	-
			1	-	-

For D0 to D3 no particular semantics exists. There is no particular meaning of the I/O data bits. Each I/O data bit is an individual remote I/O bit and there is no particular relation between the single bits.

D3 is not available as an output.

A.5.2.4 S-X.A.0 – Semantics of parameters

The semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Parameter	Input filter	0	Low	Input filter on
			1	High	Input filter off
P2	Parameter	Synchronous data I/O mode	0	Low	Synchronous data I/O mode enabled
			1	High	Synchronous data I/O mode disabled
P3	Parameter	Not available			

P0 shall only be used to disable a watchdog function monitoring the continuity of the communication activity of the slave.

The minimum watchdog time shall be equal to or more than 40 ms and the maximum watchdog time shall be less than or equal to 100 ms to set the actuators/outputs inactive.

The parameter P1 may be used to switch on an input filter that suppresses input pulses in all input channels.

For a slave to be conform with this profile, the parameter bits P0, P1 and P2 do not have to be used.

A.5.2.5 S-X.A.0 – Ports and plugs

A.5.2.5.1 S-X.A.0 – Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI−). On their realization there are no restrictions in addition to the requirements.

A.5.2.5.2 S-X.A.0 – Port of input data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2,Annex D, is used for the interconnection the plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = input data bit;
– pin 3 = (−) power supply;
– pin 4 = input data bit.

If Pin 2 and Pin 4 are available, Pin 2 and 4 of such a 12 mm or 8 mm plug shall be electrically shunted. The connection shall be built in such a way that it cannot be removed with simple tools.

A.5.2.5.3 S-X.A.0 – Port of output data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator) the plug shall be female with the following pinning:

– pin 1 = (+) power supply in the case of a npn-logic;
– pin 2 = not connected;
– pin 3 = (−) power supply in the case of a pnp-logic;
– pin 4 = output, parameter, etc.

On the other hand, for an externally powered output (e.g. relay contacts) the plug shall be male with the following pinning:

– pin 1 = change-over contact;
– pin 2 = normally closed (NC) contact;
– pin 4 = normally open (NO) contact.

A.5.2.5.4 S-X.A.0 – Power port

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;

– pin 3 = (−) power;

– pin 4 = not used.

A.5.2.6 S-X.A.0 – Marking

On the enclosure the remote I/O ports shall have a clear unique identification of the available ports, such as I/O data bits and energy supply from the AS-i-system, as well as a clear identification of the pnp- or npn- logic used for the ports.

The ports for the 4 I/O data bits D0 to D3 shall be marked by the numbers 1 to 4. In general, for the unique identification of the ports a single letter may be used, such as, for example I for input data, O for output data, etc. Only capital letters shall be used. The letters A, B, and P are reserved for antivalent I/Os, bidirectional I/Os, and parameter outputs, respectively.

A.5.2.7 S-X.A.0 – Additional requirements

For pnp-logic, the voltage levels and currents at the ports of a remote I/O device shall conform to IEC 61131-2, input port. For npn-logic, the same IEC 61131-2 shall be used accordingly.

The value of the time delay for an I/O signal between the state change at the port of a remote I/O device and the availability on the AS-i line shall be less than 5 ms for input data and 20 ms for output data. The actual value of the time delay shall be given in the product documentation.

As an option, the remote I/O output ports may have an integrated watchdog function monitoring the continuity of the communication. Such a watchdog function, however, shall not have a response time less than 40 ms. In the product documentation, it must be stated whether the remote I/O ports contain a watchdog function or not.

NOTE For remote I/O ports with an auxiliary energy supply, the availability, overload, or short cut, etc. of the auxiliary energy may be monitored by electronic means. If such a monitor function is used, it should be realized either by using the local reset function of the slave, which inhibits the communication to the master, and/or the periphery fault bit. The use of this monitor function in the remote I/O ports should be stated in the product documentation.

A.5.3 Single sensor with extended control (S-3.A.1)

A.5.3.1 S-3.A.1 – Definition

This profile collects the applications of single binary sensors with an increased functionality, i.e. to use different sensor monitor and control functions and allows a binary parametrization of the sensor.

A.5.3.2 S-3.A.1 – Codes

The I/O-configuration shall be 3_{Hex}.

The ID-code shall be A_{Hex}.

The ID-code 2 shall be 1_{Hex}.

A.5.3.3 S-3.A.1 – Semantics of I/O data

The semantic of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Input	Sensor function	0	Low	Physical signal not detected
			1	High	Physical signal detected

D1	Input	Warning	0	Low	Warning on
			1	High	Warning off
D2	Output	Test	0	High	Test function inactive
			1	Low	Test function active
D3	--	Not available for data			

D0 shall only be used as input for the status of the switching element in the sensor, the term "physical signal" in the column "level definition" being defined in Clause A.2.

D1 shall only be used as a warning signal. It indicates that the sensor is working, but, has a reduced functionality or needs an inspection.

D2 shall start a functional test of the sensor only.

The availability of the sensor shall be monitored. A device failure shall be signalled via the periphery fault bit of the status register.

For a slave to be conform with this profile, the data bits D1 to D2 do not have to be in operation. A master request on input data bits not used shall always yield an AS-i high level.

A.5.3.4 S-3.A.1 – Semantics of parameters

A.5.3.4.1 S-3.A.1 – Inductive proximity switches

For inductive proximity switches, the semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Timer	0	Low	Timer function on
			1	High	Timer function off
P1	Parameter	Inversion of D0	0	Low	Inversion of D0
			1	High	D0 as specified
P2	Parameter	Special function	0	Low	Special function
			1	High	Basic function
P3	--	Not available			

P0 shall only be used to activate a timer function.

P1 shall only be used to invert the level-definition of D0.

P2 shall only be used to set a special function of the sensor. Such a function may be, for example a special mode, a teach-in, a reset of the sensor, etc.

For a slave to be conform with this profile, the parameter bits P0 to P2 do not have to be used.

A.5.3.4.2 S-3.A.1 – Photoelectric proximity switches

For photoelectric proximity switches, the semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Working frequency	0	Low	Low working frequency
			1	High	High working frequency
P1	Parameter	Inversion of D0	0	Low	Inversion of D0
			1	High	D0 as specified
P2	Parameter	Special function	0	Low	Special function
			1	High	Basic function
P3	--	Not available			

P0 shall only be used to change the working frequency of the sensor.

P1 shall only be used to invert the level-definition of D0.

P2 shall only be used to set a special function of the sensor. Such a function may be, for example a special mode, a teach-in, a reset of the sensor, etc.

For a slave to be conform with this profile, the parameter bits P0 to P2 do not have to be used.

A.5.3.4.3 S-3.A.1 – Level switches

For level switches ,the semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Time delay	0	Low	Timer function on
			1	High	Timer function off
P1	Parameter	Sensitivity 1	0	Low	Low sensitivity 1
			1	High	High sensitivity 1
P2	Parameter	Sensitivity 2	0	Low	Low sensitivity 2
			1	High	High sensitivity 2
P3	--	Not available			

P0 shall only be used to switch the timer function of the sensor on or off.

P1 and P2 shall only be used to set the sensitivity of the level switch according to the following:

P2	P1	Sensitivity level
0	0	Lowest sensitivity
0	1	Low sensitivity
1	0	High sensitivity
1	1	Highest sensitivity

For a slave to be conform with this profile, the parameter bits P0 to P2 may not be used.

A.5.3.4.4 S-3.A.1 – Other sensors

For other sensors, the semantics of P0 to P2 are under consideration. At the moment, this profile may be applied, but the parameters P0 to P2 shall not be used.

A.5.3.5 S-3.A.1 – Additional requirements

The detailed functions of the single data bits, the periphery fault bit and the parameter bits used for a particular sensor shall be described in the product documentation of the sensor.

A.5.4 Remote I/Os with dual-signals in extended addressing mode (S-0.A.2, S-3.A.2, S-7.A.2, S-8.A.2, S-B.A.2)

A.5.4.1 S-X.A.2 – Definition

These slave sub-profiles use the extended address capabilities and comprise the applications of one or two binary sensors or actuators which have two data signals each. The slave profiles offer the possibility to use a single monitor function for each sensor or actuator, such as, for example, a warning, a failure message, a breakdown signal, etc. The slaves profiles include also remote I/O devices for the connection of conventional antivalent output sensors to the AS-i line or split connection (Y) for inputs and outputs.

A.5.4.2 S-X.A.2 – Codes

The I/O code shall be 0_{Hex}, 3_{Hex}, 7_{Hex}, 8_{Hex} and B_{Hex}.

The ID code shall be A_{Hex}.

The ID2-code shall be 2_{Hex}.

A.5.4.3 S-X.A.2 – Semantics of I/O data

A.5.4.3.1 X = 0 (4 inputs)

The semantics of the I/O data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Input	Sensor 1	0	Low	Physical signal not detected
			1	High	Physical signal detected
D1	Input	Monitor signal 1	0	Low	Warning/failure
			1	High	Normal operation
D2	Input	Sensor 2	0	Low	Physical signal not detected
			1	High	Physical signal detected
D3	Input	Monitor signal 2	0	Low	Warning/failure
			1	High	Normal operation

D0 and D2 shall only be used as input signals from the switching elements of sensor 1and 2, respectively, the term 'physical signal' in the column “level definition” being defined in Clause A.2. If the slave is a remote I/O port to which the two sensors may be connected, then the terms 'physical signal detected' and “physical signal not detected” shall be replaced by “switching element in the (external) sensor closed” and “switching element in the (external) sensor open”, respectively.

D1 and D3 shall only be used as monitor signal for the sensor 1 and 2, respectively. The monitor signals may indicate, for example when the corresponding sensor has a reduced functionality, is in a critical state or faulty, gives a warning, needs an inspection, etc.

The monitor signals D1 and D3 may also be the antivalent signals to the sensor function signals D0 and D2, respectively. Then, the semantic of the data bits shall be as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	Input	Sensor 1	0	Low	Physical signal not detected
			1	High	Physical signal detected
D1	Input	Sensor 1	0	Low	Physical signal detected
			1	High	Physical signal not detected
D2	Input	Sensor 2	0	Low	Physical signal not detected
			1	High	Physical signal detected
D3	Input	Sensor 2	0	Low	Physical signal detected
			1	High	Physical signal not detected

A.5.4.3.2 X = 3, 7, 8, B

If the slave is a remote I/O port to which sensors/actuators may be connected, then the semantic of the data bits shall be as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	-	Remote I/O	0	-	-
			1	-	-
D1	-	Remote I/O	0	-	-
			1	-	-
D2	-	Remote I/O	0	-	-
			1	-	-
D3	-	Remote I	0	-	-
			1	-	-

For D0 to D3 no particular semantics exists but in a common port or plug only the combination of D0/D1 or D2/D3 is allowed. There is no particular meaning of the I/O data bits. Each I/O data bit is an individual remote I/O bit and there is no relation between the single bits.

D3 is not available as an output.

A.5.4.4 S-X.A.2 – Semantics of parameters

The semantics of the parameter bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter	Watchdog function	0	Low	Watch dog disabled
			1	High	Watch dog enabled
P1	Parameter	Input filter	0	Low	Input filter on
			1	High	Input filter off
P2	Parameter	Synchr. Data IO Mode	0	Low	Synchr. Data IO Mode enabled
			1	High	Synchr. Data IO Mode disabled
P3	Parameter	Not available			

P0 shall only be used to disable a watchdog function monitoring the continuity of the communication activity of the slave.

The minimum watchdog time shall be equal to or more than 40 ms and the maximum watchdog time shall be less than or equal to 100 ms to set the actuators/outputs inactive.

The parameter P1 may be used to switch on an input filter that suppresses input pulses in all input channels.

For a slave to be conform with this slave profile, the parameter bits P0, P1 and P2 may not be used.

A.5.4.5 S-X.A.2 – Ports and plugs

A.5.4.5.1 S-X.A.2 – Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI−). On their realization there are no restrictions in addition to the requirements.

A.5.4.5.2 S-X.A.2 – Port of input data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2,Annex D, is used for the interconnection, the plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = input data bit D1 or D3;
– pin 3 = (−) power supply;
– pin 4 = input data bit D0 or D2.

NOTE Only the combinations D0/D1 or D2/D3 are allowed.

Appendant to each plug, a second plug is allowed to provide more universal connection possibilities. This plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = not used;
– pin 3 = (−) power supply;
– pin 4 = input data bit D1 or D3.

A.5.4.5.3 S-X.A.2 – Port of output data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2,Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator) the plug shall be female with the following pinning:

– pin 1 = (+) power supply in the case of a npn-logic;
– pin 2 = output D1;
– pin 3 = (−) power supply in the case of a pnp-logic;
– pin 4 = output D0 or D2.

NOTE Only the combinations D0/D1 are allowed.

Appendant to each plug, a second plug is allowed to provide more universal connection possibilities. This plug shall be female with the following pinning:

– pin 1 = (+) power supply;
– pin 2 = not used;
– pin 3 = (−) power supply;
– pin 4 = output D1.

A.5.4.5.4 S-X.A.2 – Power port

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;
– pin 3 = (−) power;
– pin 4 = not used.

A.5.4.6 S-X.A.2 – Marking

On the enclosure the remote I/O ports shall have a clear unique identification of the available ports, such as I/O data bits and energy supply from the AS-i system, as well as a clear identification of the pnp- or npn- logic used for the ports.

The ports for the 4 I/O data bits D0 to D3 shall be marked by the numbers 1 to 4. In general, for the unique identification of the ports a single letter may be used, such as, for example I for input data, O for output data, etc. Only capital letters shall be used. The letters A, B, and P are reserved for antivalent I/Os, bidirectional I/Os, and parameter outputs, respectively.

A.5.4.7 S-X.A.2 – Additional requirements

For pnp-logic, the voltage levels and currents at the ports of a remote I/O device shall conform to IEC 61131-2, input port. For npn-input the same IEC 61131-2 shall be used accordingly.

The value of the time delay for an I/O signal between the arrival at the port of a remote I/O device and the availability on the AS-i line shall be less than 5 ms for input data and 20 ms for output data. The actual value of the time delay shall be given in the product documentation.

As an option, the remote I/O output ports may have an integrated watchdog function monitoring the continuity of the communication. Such a watchdog function, however, shall not have a response time less than 40 ms. In the product documentation, it must be stated whether the remote I/O ports contain a watchdog function or not.

NOTE For remote I/O ports with an auxiliary energy supply, the availability, overload, or shortcut, etc. of the auxiliary energy may be monitored by electronic means. If such a monitor function is used it should be realized either by using the local reset function of the slave, which inhibits the communication to the master and/or the periphery fault bit. The use of this monitor function in the remote I/O ports should be stated in the product documentation.

A.6 Slave profiles for slaves with combined transaction support

A.6.1 Slave profile for combined transaction type 1 (S-7.1, analogue profile)

NOTE This profile has been replaced by profile S-7.3. It is not recommended to use this profile for new developments.

A.6.2 Extended slave profile for combined transaction type 1 (S-7.2, extended analogue profile)

NOTE This profile has been replaced by profile S-7.4. It is not recommended to use this profile for new developments.

A.6.3 Slave profile for combined transaction type 1 (S-7.3, integrated analogue profile)

A.6.3.1 S-7.3 – General

Slave profile S-7.3 is especially designed to support the transfer of analogue values in the firmware of AS-i Masters. Furthermore, it allows the data exchange of digital two byte values with sensors and actuators. Profile S-7.3 permits the AS-i master to present the data of AS-i analogue sensors in the same way as with conventional analogue input-/output modules. To achieve this it defines the data length and format for the analogue values to be transferred.

It uses the combined transaction type 1 as specified in 5.7.2 for data transfer.

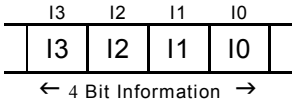
NOTE The fixed data format allows fast and easy transfer of analogue data to or from the controller in the same data format as with conventional analogue I/O cards. The fixed data length has the advantage, that the data length does not have to be configured for each slave by the user. Furthermore, error handling and implementation of algorithms are simplified. The main advantage of integrating the transfer of analogue values in the firmware of AS-i-masters is the increase of speed of data transfer and the easier handling for the user.

A.6.3.2 S-7.3 – Codes

The I/O code shall be 7_{Hex}.

The ID code shall be 3_{Hex}.

The extended ID-Code 2 shall be used as defined in Figure A.1:



I3	*I2*	*I1*	*I0*	Definition	Restriction
X	X	0	0	Slave has 1 channel	
X	X	0	1	Slave has 2 channels	
X	X	1	0	Slave has 4 channels	
1	1	1	1	Slave has 4 channels	Only for slaves that do not support extended ID1/2 code
X	0	X	X	Transparent mode	
X	1	X	X	Transfer of analogue values	
0	X	X	X	Output slave	
1	X	X	X	Input slave	

Figure A.1 – Definition of the extended ID2 code bits for S-7.3

A.6.3.3 S-7.3 – Semantics of I/O data and parameters

The semantics of the I/O data bits are given in 5.7.2.1. The use of the parameter bits is optional and shall be stated in the product documentation.

A.6.3.4 S-7.3 – Ports and plugs

A.6.3.4.1 S-7.3 – Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI−). On their realization there are no restrictions in addition to the requirements.

A.6.3.4.2 S-7.3 – Port of input data

If a 12 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection the plug shall be female with the following recommended pinning:

Voltage/current input

– pin 1 = (+) power supply;
– pin 2 = positive current/voltage input;
– pin 3 = (−) power supply;
– pin 4 = negative current/voltage input;
– pin 5 = functional earth (optional).

Resistance input, e.g. Pt100

– pin 1 = positive current output;

– pin 2 = positive voltage input;
– pin 3 = negative current output;
– pin 4 = negative voltage input;
– pin 5 = functional earth (optional).

A.6.3.4.3 S-7.3 – Port of output data

If a 12 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator) the plug shall be female with the following recommended pinning:

– pin 1 = positive current/voltage output;
– pin 2 = not connected;
– pin 3 = negative current/voltage output;
– pin 4 = output, parameter, etc.
– pin 5 = functional earth (optional).

A.6.3.4.4 S-7.3 – Power port

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line, the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;
– pin 3 = (−) power,
– pin 4 = not used.

A.6.3.5 S-7.3 – Additional requirements

The data is transferred in portions of 3 bit data plus a control bit K as specified in 5.7.2.3. The upper line denotes the information sent from the data sink, the lower line the corresponding response from the data source.

Extension bits	**User information data**												**Add. info bits**	
1	1	1	1	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0
E3	E2	E1	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	O	V

NOTE The data in this table is shown at controller level. On the AS-i line, the master requests will be transmitted in inverted form.

In/output data are transferred from the slave to the AS-i Master and from the AS-i Master to the slave as binary number, represented by a two's complement value. As the most significant bit D16 of this number is also the sign bit (for analogue values) no additional sign bit is necessary.

The data width is fixed to 16 net data bits D1 ... D16, three multiplex bits E1... E3 and O,V. The sequence always starts with the multiplex bits and ends with the additional information bits (from left to right as shown above). The data request "K110" is omitted.

E3, E2, E1 indicate the address of the in/output data channel in form of a binary number. If the slave have more than one channel, the in/output data of the channels are transferred cyclically and the corresponding channel No. is assigned via E3, E2, E1.

The additional information bits have the following meaning (controller level):

– O = overflow (0 means value in the measuring range, 1 means value out of range);

– V = valid (1 means valid value, 0 means not valid value).

The maximum number of channels is restricted to 4. Overflow is used for analogue input slaves, and may optionally also be used for transparent input slaves. For output slaves the AS-i Master sets the overflow bit always to zero.

A.6.3.6 AS-7.3 – Data representation

Slaves of profile S-7.3 may transfer analogue values or digital two byte values (transparent mode). The data representation and data handling is different for these two types of slaves.

A.6.3.6.1 S-7.3 – Slaves with transparent mode

Slaves with transparent mode may be input or output slaves. They transfer digital two byte values from/to the AS-i-Master. These values may be for example counter values or digital input / outputs.

There is no under range/over range or out of range for transparent values.

A.6.3.6.2 Default value for transparent input slaves

When one of the following conditions occur the AS-i Master will set the input data of a transparent input channel to the default value 0000_{Hex}:

– after initialization of the AS-i Master no valid data transfer according to profile S-7.3 has been accomplished for this channel;

– slave is not in List of Active Slaves (LAS);

– the AS-i Master has detected a toggle bit error for this input slave (see 5.7.2.6).

– the last data transfer for this channel was finished with valid bit set to “0”;

By means of that it indicates to the controller that the measurement value is invalid.

A.6.3.6.3 S-7.3 – Analogue slaves

Data of S-7.3 analogue input / output slaves are represented as two’s complement values with a fixed length of 16 data bits. For sensors / actuators which need less resolution the least significant bits are filled with zeros.

Example:

Data bit #	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
16 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1
12 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	**0**	**0**	**0**	**0**
8 bit analogue value	0	1	0	0	0	1	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

As data is represented as two’s complement values bit D16 represents the sign bit.

A.6.3.6.4 Measurement range of analogue slaves

Example for the value range of an analogue input slave:

Units		Range	Remarks
Decimal	**Hexadecimal**		
32767	$7FFF_{Hex}$	Out of range	Overflow bit set
32511 . 27649	$7EFF_{Hex}$. $6C01_{Hex}$	Over range (optional)	Analogue value is still valid, but as it is out of nominal range it may have a wider tolerance than in nominal range
27648 . -27648	$6C00_{Hex}$. 9400_{Hex}	Nominal range	Measurement value meets the specified tolerance
-27649 . -32512	$93FF_{Hex}$. 8100_{Hex}	Under range (optional)	Analogue value is still valid, but as it is out of nominal range it may have a wider tolerance than in nominal range
-32768	8000_{Hex}	Out of range	Overflow bit set

The possible measurement range is from 8001_{Hex} to $7FFE_{Hex}$. The limits of nominal range, over range and under range depend on the specific slave implementation. There may also be implementations that use the full possible nominal range from 8001_{Hex} to $7FFE_{Hex}$ and do not implement under range/over range.

8000_{Hex} always represents underflow, $7FFF_{Hex}$ represents always overflow condition.

The overflow bit shows that the measurement value is not valid (overflow or underflow).

A.6.3.6.5 Default value for analogue input slaves

When one of the following conditions occurs the AS-i Master will set the input data of an analogue input channel to the default value $7FFF_{Hex}$:

– after initialization of the AS-i Master, no valid data transfer according to profile S-7.3 has been accomplished for this channel;

– the slave is not in List of Active Slaves (LAS);

– the AS-i Master has detected a toggle bit error for this input slave (see 5.7.2.6);

– the last data transfer for this channel was finished with valid bit set to “0”;

– the overflow bit is set;

In this way, it indicates to the controller that the measurement value is invalid.

A.6.4 Extended slave profile for combined transaction type 1 (S-7.4, Extended integrated analogue profile)

A.6.4.1 S-7.4 – General

Slave profile S-7.4 uses the identical mechanism for data transfer as profile S-7.3 for analogue slaves. Additionally, it defines a slave with four bit mode (4I/4O). Profile S-7.4 is especially designed for integrated support in AS-i-Masters. In addition to profile S-7.3, it offers extended functions, among other things to load parameter sets into the slave for the operation of more complex slaves.

It uses the combined transaction type 1 as specified in 5.7.2 for data transfer.

NOTE The extended functions are defined identically to the functions in profile S-7.2.

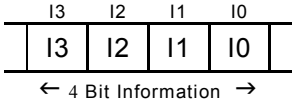
Transmission and dynamic response are controlled by means of operator control of the controller functions (AS interface master calls) in the controller itself or by means of a master featuring an extended scope of functions.

A.6.4.2 S-7.4 – Codes

The I/O code shall be 7_{Hex}.

The ID code shall be 4_{Hex}.

The extended ID-Code 2 shall be used as defined in Figure A.2:



I3	*I2*	*I1*	*I0*	*Definition*	*Restriction*
X	1	0	0	Slave has 1 channel	
X	1	0	1	Slave has 2 channels	
X	1	1	0	Slave has 4 channels	
1	1	1	1	Slave has 4 channels	Only for slaves that do not support extended ID1/2 code
0	0	0	0	4 Bit mode (4I / 4O)	
0	1	X	X	Output slave	
1	1	X	X	Input slave	

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Figure A.2 – Definition of the extended ID2 code bits for S-7.4

A.6.4.3 S-7.4 – Semantics of I/O data and parameter bits

The semantics of the I/O data bits and of the parameter bits are given in 5.7.2.1. The implementation of the functions assigned to the parameter nibbles F_{Hex} and D_{Hex} are mandatory, the others are optional and shall be stated in the manufacturer's product documentation.

A.6.4.4 S-7.4 – Ports and plugs

A.6.4.4.1 S-7.4 – Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI−). On their realization there are no restrictions in addition to the requirements.

A.6.4.4.2 S-7.4 – Port of input data

If a 12 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, the plug shall be female with the following recommended pinning:

Voltage/current input:

– pin 1 = (+) power supply;
– pin 2 = positive current/voltage input;
– pin 3 = (−) power supply;
– pin 4 = negative current/voltage input;
– pin 5 = functional earth (optional).

Resistance input, for example Pt100:

– pin 1 = positive current output;
– pin 2 = positive voltage input;

– pin 3 = negative current output;
– pin 4 = negative voltage input;
– pin 5 = functional earth (optional).

A.6.4.4.3 S-7.4 – Port of output data

If a 12 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator) the plug shall be female with the following recommended pinning:

– pin 1 = positive current/voltage output;
– pin 2 = not connected;
– pin 3 = negative current/voltage output;
– pin 4 = output, parameter, etc.
– pin 5 = functional earth (optional).

A.6.4.4.4 S-7.4 – Power port

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line, the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;
– pin 3 = (−) power;
– pin 4 = not used.

A.6.4.5 S-7.4 – Additional requirements

The data is transferred in portions of 3 bit data plus a control bit K as specified in 5.7.2.3. The upper line denotes the information sent from the data sink, the lower line the corresponding response from the data source.

Extension bits	**User information data**						**Add. info bits**
1 1 1	1 0 1	1 0 0	0 1 1	0 1 0	0 0 1	0	0 0
E3 E2 E1	D16 D15 D14	D13 D12 D11	D10 D9 D8	D7 D6 D5	D4 D3 D2	D1	O V

NOTE The data in this table is shown at controller level. On the AS-i line, the master requests will be transmitted in inverted form.

Measured variables are transferred from the slave to the AS-i Master and from the AS-i Master to the slave as a binary number, represented by a two's complement value. As the most significant bit D16 of this number is also the sign bit (for analogue values) no additional sign bit is necessary.

The data width is fixed to 16 net data bits D1 ... D16, three multiplex bits E1... E3 and O,V. The sequence always starts with the multiplex bits and ends with the additional information bits (from left to right as shown above). The data request "K110" is omitted.

E3, E2, E1 indicate the address (the measuring channel) in the form of a binary number. If the slave measures a variable on several channels, the measuring values of the channels are transferred cyclically and the corresponding channel No. is allotted via E3, E2, E1.

The additional information bits have the following meaning (controller level):

– O = overflow (0 means value in the measuring range, 1 means value out of range)

– V = valid (1 means valid value, 0 means not valid value)

The maximum number of channels is restricted to 4. Overflow is used for analogue input slaves.. For output slaves the AS-i Master sets the overflow bit always to zero.

A.6.4.6 S-7.4 – Data representation

Slaves of profile S-7.4 may transfer analogue values, digital two byte values (transparent mode) or 4I/4O data. The data representation and data handling is different for these three types of slaves.

A.6.4.6.1 S-7.4 – Slaves with transparent mode

Slaves with transparent mode may be input or output slaves. They transfer digital two byte values from/to the AIDI/AODI of the AS-i-Master. These values may be, for example counter values or digital input / outputs.

There is no under range/over range or out of range for transparent values.

A.6.4.6.2 Default value for transparent input slaves

When one of the following conditions occurs, the AS-i Master will set the input data of an transparent input channel to the default value 0000_{Hex}:

– after initialization of the AS-i Master, no valid data transfer according to profile S-7.4 has been accomplished for this channel;

– the slave is not in List of Active Slaves (LAS);

– the AS-i Master has detected a toggle bit error for this input slave (see 5.7.2.6);

– the last data transfer for this channel was finished with valid bit set to “0”.

By means of that, it indicates to the controller that the measurement value is invalid.

A.6.4.6.3 S-7.4- Analogue slaves

Data of S-7.4 analogue input / output slaves are represented as two’s complement values with a fixed length of 16 data bits. For sensors / actuators which need less resolution, the least significant bits are filled with zeros.

Example:

Data bit #	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
16 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1
12 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	**0**	**0**	**0**	**0**
8 bit analogue value	0	1	0	0	0	1	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

As data is represented as two’s complement values, bit D16 represents the sign bit.

A.6.4.6.4 Measurement range of analogue slaves

Example for the value range of an analogue input slave:

Units		Range	Remarks
Decimal	**Hexadecimal**		
32767	$7FFF_{Hex}$	Out of range	Overflow bit set
32511 . 27649	$7EFF_{Hex}$. $6C01_{Hex}$	Over range (optional)	Analogue value is still valid, but as it is out of nominal range, it may have a wider tolerance than in nominal range
27648 . -27648	$6C00_{Hex}$. 9400_{Hex}	Nominal range	Measurement value meets the specified tolerance
-27649 . -32512	$93FF_{Hex}$. 8100_{Hex}	Under range (optional)	Analogue value is still valid, but as it is out of nominal range, it may have a wider tolerance than in nominal range
-32768	8000_{Hex}	Out of range	Overflow bit set

The possible measurement range is from 8001_{Hex} to $7FFE_{Hex}$. The limits of nominal range, over range and under range depend on the specific slave implementation. There may also be implementations that use the full possible nominal range from 8001_{Hex} to $7FFE_{Hex}$ and do not implement under range/over range.

8000_{Hex} always represents underflow, $7FFF_{Hex}$ represents always overflow condition.

The overflow bit shows that the measurement value is not valid (overflow or underflow).

A.6.4.6.5 Default value for analogue input slaves

When one of the following conditions occur the AS-i Master will set the input data of an analogue input channel to the default value $7FFF_{Hex}$:

– after initialization of the AS-i Master no valid data transfer according to profile S-7.4 has been accomplished for this channel M;
– the slave is not in List of Active Slaves (LAS);
– the AS-i Master has detected a toggle bit error for this input slave (see 5.7.2.6);
– the last data transfer for this channel was finished with valid bit set to “0”;
– the overflow bit is set.

By means of that, it indicates to the controller that the measurement value is invalid.

A.6.4.6.6 S-7.4 – Slaves with 4 Bit mode

Data of S-7.4 4I/4O slaves is exchanged with the IDI and ODI of the master. The meaning of the data bits shall be stated in the manufacturer's documentation.

A.6.4.7 S-7.4 – Identification of slaves

In profile S-7.4, three types of slaves are possible:

– analogue slaves (input/output);
– slaves that transfer 16 bit digital values (transparent mode);
– slaves with 4 Bit mode (4I/4O).

The type is identified by the E-Type field of the ID string of the slave.

A.6.4.7.1 S-7.4 – Analogue slaves (E-type = 1)

For analogue slaves according to profile S-7.4, the transfer of analogue data is handled identically to the data transfer of analogue slaves of profile S-7.3 (see A.4.4.3). The E-type in the ID string of this slave shall be set to the value 1 (see below).

Additionally, analogue slaves of profile S-7.4 support the extended functions like Read ID string, etc. (see below).

A.6.4.7.2 S-7.4 – Slaves in transparent mode (E-type = 2)

Instead of transferring analogue values with profile S-7.4, it is optionally possible to transfer digital 16 bit input or output values. In this case, the E-type in the ID string of this slave shall be set to the value 2 (see below).

A.6.4.7.3 S-7.4 – Slaves with 4 bit mode (E-type = 3)

Slaves belonging to this type are capable of offering all S-7.4 functions. When transferring user information data, however, they do not use the triple transfer described in conformity with S-7.3 but, instead, as with a normal 4I/4O slave the user information data is transferred with a maximum width of 4 bits. This type is mainly encountered in slaves that only exchange up to 4 bits of digital information during normal operation. Extensive settings and an extended scope of functions are possible by the transfer of parameter sets.

If a slave with a 4 Bit mode is not in the list of activated slaves (LAS) the AS-i Master sets the corresponding input value in its input process image to 0_{Hex}.

A.6.4.8 S-7.4 – Read ID, Read Diagnosis, Read and Write Parameter

If the normal data transfer cycle is to be interrupted to insert a Read ID, Read Diagnosis, Read or Write Parameter, the master and slave shall follow the sequence described in 5.7.2.5.

A.6.4.8.1 S-7.4 – Read ID string from slave

With this function, the ID string is read out of the slave by the master.

The data structures used are defined below. The maximum length of the ID string in profile S-7.4 is limited to 219 Bytes. It is recommended to limit the ID String to a length of 33 Bytes to allow an easier handling in the AS-i Master.

NOTE This function is identical with the corresponding function of profile S-7.2

For a S-7.4.0 slave (4I/4O) the master shall ensure the binary output is valid immediately after the parameter response is "1111_{Bin}" if the optional parameter call "1110_{Bin}" (End of Communication) is used.

For an S-7.4.0 slave (4I/4O) the master shall change the data to binary output 30 ms after the parameter response is "1111_{Bin}" at the latest if the optional parameter call "1110_{Bin}" (End of Communication) is not used.

In case of a 7.4.0 slave (4I/4O) and if there was no parameter call "1110_{Bin}" or the parameter call "1110_{Bin}" was not answered by the slave, the slave shall not use the master's output data until 60 ms after it answered the parameter request "1111_{Bin}" with "1111_{Bin}".

If there was a parameter call "1110_{Bin}" which was answered by the slave with "1110_{Bin}" within 1 ms, the master's output data is valid immediately after the parameter call "1111_{Bin}".

The slave shall answer the first data request after it answered the parameter request "1111_{Bin}" with "1111_{Bin}" with valid input data.

The identification block (ID string) that can be read out of the slave provides information about its operating behaviour.

The block is structured as follows:

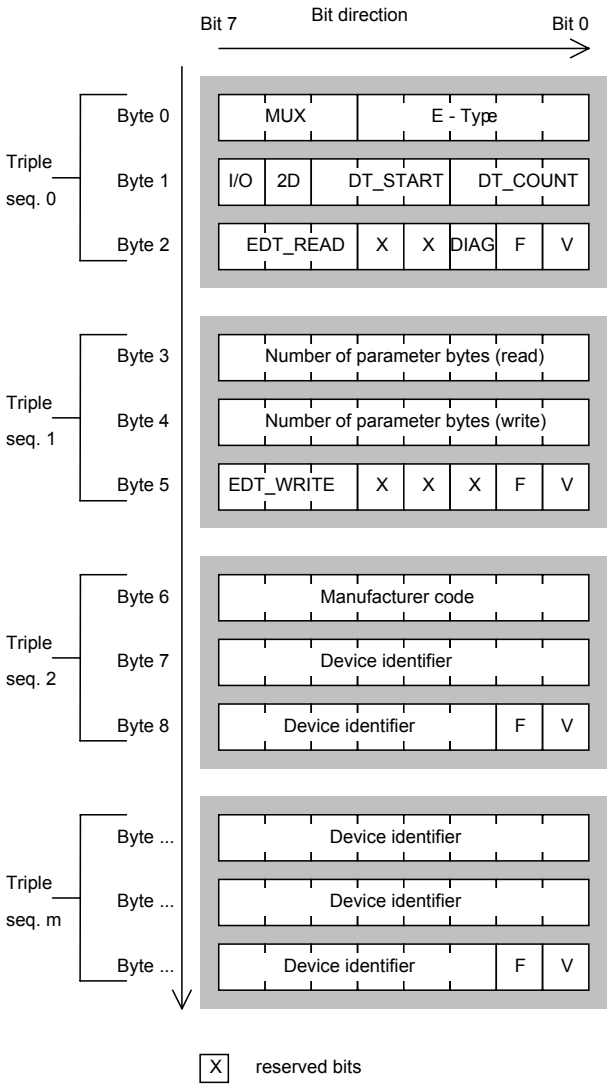

Figure A.3 – Data structure of the ID string (S-7.4)

A.6.4.8.2 S-7.4 – Description of the objects in the ID string

MUX

Shows the number of multiplexed channels of the slave. The number of the channels shall always be set as "Number = MUX number + 1"

Object name	id_mux	
Object length	3 bits	
Value range	0 – 3	
Meaning	0	Slave has one channel
	1	Slave has 2 channels
	2	Slave has 3 channels
	3	Slave has 4 channels

E-Type

Specifies the slave type in relation to its functional behaviour and structuring of the user information data. It is used to classify the S-7.4 slaves.

Object name	id_e_type	
Object length	5 bits	
Value range	0 – 31	
Meaning	1	Transfer of analogue values
	2	Transfer of 16 bit digital values
	3	Four bit mode (4I/4O-Operation)
	0; 4-31	Reserved for later applications

I/O

This bit indicates whether the slave offers outputs or inputs during user information data transfer.

Object name	id_io	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	Transfer user information data from the slave to the controller (input)
	1	Transfer user information data from the controller to the slave (output)

2D

This bit indicates whether or not double data transfer is supported. Note S-7.4 slaves support only single data transfer.

Object name	id_2d	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	Single data transfer

DT_START

Indicates with which data triple a normal data transfer (triple sequence) has to begin. In profile S-7.4, data length is fixed to 16 data bits and OV.

Object name	id_dt_start	
Object length	3 bits	
Value range	5	
Meaning	5	From D16 + OV

DT_COUNT

Indicates which quantity of triples can be transferred during a normal data transfer after the DT start triple. In profile S-7.4, DT quantity is fixed to 5.

Object name	id_dt_count	
Object length	3 bits	
Value range	5	
Meaning	5	Number of triples transferred (without the last triple with D1, O,V)

EDT_READ

Reserved for future extensions. This shall be assigned 0 until it is finally defined.

Object name	id_edt_read	
Object length	3 bits	
Value range	0	
Meaning	0	Function not available

EDT_WRITE

Reserved for future extensions. This shall be assigned 0 until it is finally defined.

Object name	id_edt_write	
Object length	3 bits	
Value range	0	
Meaning	0	Function not available

X bits

These reserved bits are currently not used and shall not be used otherwise.

Object name	id_x	
Object length	1 bit	
Value range	0	Reserved
Meaning	0	Permanently set to 0

DIAG

This bit indicates whether or not the slave offers the possibility of reading the diagnostic string.

Object name	id_diag	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	Function not available; Parameter changeover shall not be used
	1	Diagnostic string is available

F – Follow bit

This bit indicates whether or not the string to be transferred has a further triple sequence for reading.

Object name	id_f	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	No further triple sequence; end of string
	1	Further triple sequence available; string not yet ended

V – Valid bit

This bit indicates whether the previously transferred triple sequence was valid or contained errors. In the event of an error, the complete sequence shall be discarded.

Object name	id_v	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	Triple sequence invalid
	1	Triple sequence valid

Read number of parameter bytes

This byte specifies how many parameter bytes the slave provides for read access and is the upper limit. The actual number during a string transfer is determined by the Follow bit.

Object name	id_p_count_read	
Object length	8 bits	
Value range	0 – 219	
Meaning	0	Function not available; parameter changeover shall not be used
	N	Number of parameter bytes that can be read

Write number of parameter bytes

This byte specifies how many parameter bytes the slave provides for write access and is the upper limit. The actual number during a string transfer is determined by the Follow bit.

Object name	id_p_count_write	
Object length	8 bits	
Value range	0 – 219	
Meaning	0	Function not available; parameter changeover shall not be used
	N	Number of parameter bytes that can be written

Manufacturer code

This byte contains a manufacturer code (Vendor ID) The vendor ID shall not equal 0 and is assigned by the authority. The code shall be specified on the slave's documentation.

Object name	id_vendor	
Object length	8 bits	
Value range	0 – 255	
Meaning	0	Reserved
	1 – 254	Code for member companies
	255	Group code for all non-members

Device identifier

These bytes contain a device identifier, which respective manufacturers may assign themselves. Management of the device ID and definition of its meaning are the responsibility of the manufacturer. The code is specified on the slave's documentation.

Object name	id_device	
Object length	14 bits	
Value range	0 –	
Meaning	N	To be defined by the manufacturer

A.6.4.8.3 S-7.4 – Read diagnostic string from slave

The diagnostic string, which can be read out of the slave, offers diagnostic information to support detailed troubleshooting.

NOTE This function is identical with the corresponding function defined in profile S-7.2.

The maximum length of the diagnostic string in profile S-7.4 is limited to 220 Bytes user data (i.e. the length of the diagnostic string is 330 Bytes). It is recommended to limit the diagnostic string to a length of 32 Bytes user data to allow an easier handling in the AS-i Master.

A.6.4.8.4 S-7.4 – Data structure of the diagnostic string

The diagnostic string, which can be read out of the slave, offers diagnostic information to support detailed troubleshooting. As the contents of this string depends considerably on the respective slave and its functions, only the external structure of the string is defined. Structuring and the meanings of the objects it contains depend on the respective slave and are given in its description.

The block is structured as follows:

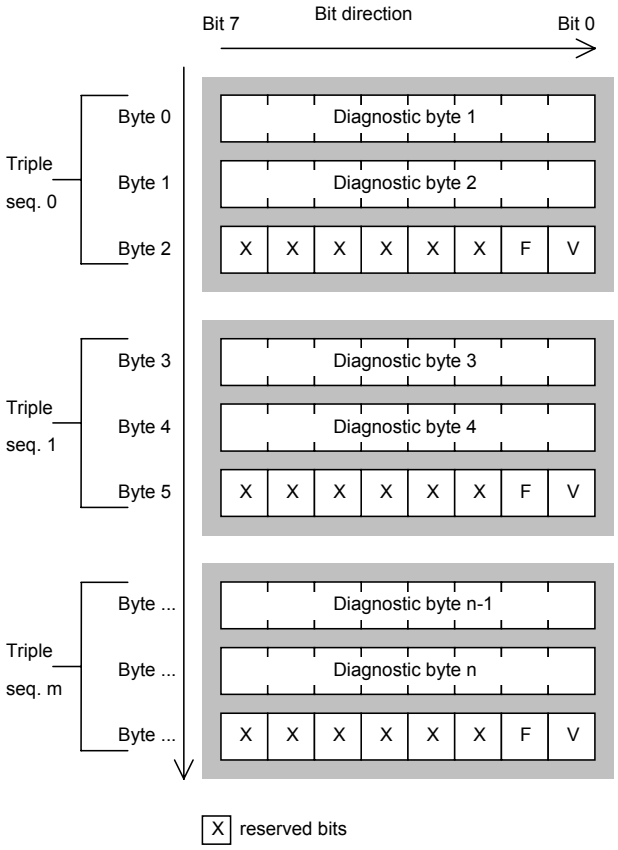

Figure A.4 – Data structure of the diagnostic string (S-7.4)

A.6.4.8.5 S-7.4 – Description of the objects in the diagnostic string

X bits

These reserved bits are currently not used and shall not be used otherwise.

Object name	id_x	
Object length	1 bit	
Value range	0	Reserved
Meaning	0	Permanently set to 0

F – Follow bits

This bit indicates whether the string to be transferred has a further triple sequence for reading.

Object name	id_f	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	No further triple sequence; end of string
	1	Further triple sequence available; string not yet ended

V – Valid bit

This bit indicates whether the previously transferred triple sequence was valid or contained errors. In the event of an error, the complete sequence shall be discarded.

Object name	id_v	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	Triple sequence invalid
	1	Triple sequence valid

A.6.4.8.6 S-7.4 – Read parameter string

With this function, the parameter string is read out of the slave by the master.

The data structures used are defined below. The maximum length of the ID string in profile S-7.4 is limited to 220 Bytes. It is recommended to limit the ID String to a length of 32 Bytes to allow an easier handling in the AS-i Master.

A.6.4.8.7 S-7.4 – Data structure of the parameter string

The parameter string, which can be read from written to the slave, contains operating information and operating settings for the slave. As the contents of this string depend very considerably on the respective slave and its functions, only the external structure of the string is defined. The structuring of the objects it contains and their meanings depend on the respective slave and are given in its description.

The block is structured as follows:

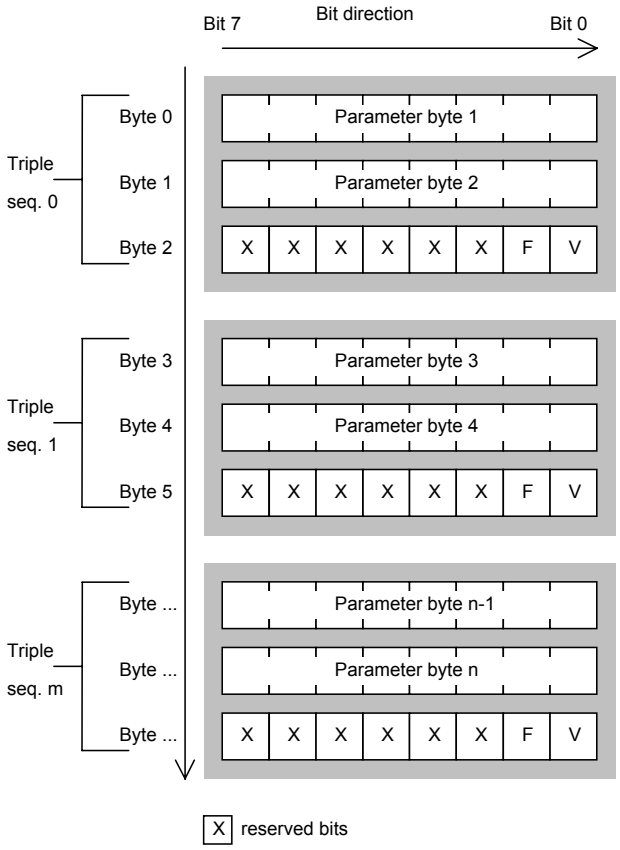

Figure A.5 – Data structure of the parameter string (S-7.4)

A.6.4.8.8 S-7.4 – Description of the objects in the parameter string

X bits

These reserved bits are currently not used and shall not be used otherwise.

Object name	id_x	
Object length	1 bit	
Value range	0	Reserved
Meaning	0	Permanently set to 0

F – Follow bits

This bit indicates whether the string to be transferred has a further triple sequence for reading.

Object name	id_f	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	No further triple sequence; end of string
	1	Further triple sequence available; string not yet ended

V – Valid bits

This bit indicates whether the previously transferred triple sequence was valid or contained errors. In the event of an error, the complete sequence shall be discarded.

Object name	id_v	
Object length	1 bit	
Value range	0 – 1	
Meaning	0	Triple sequence invalid
	1	Triple sequence valid

A.6.4.8.9 S-7.4 – Write parameter string

This function is used to write the complete parameter string from the master to the slave. The string transfer is finished by the slave. For details see 5.7.2.3. and Table 10.

The maximum length of the parameter string in profile S-7.4 is limited to 220 Bytes. It is recommended to limit the parameter string to a length of 32 Bytes to allow an easier handling in the AS-i Master.

Note that the parameter string is stored non-volatile in S-7.4 slaves.

For an S-7.4.0 slave (4I/4O) the master shall ensure that the binary output is valid immediately after the parameter response is "1111_{Bin}" if the optional parameter call "1110_{Bin}" (End of Communication) is used.

For an S-7.4.0 slave (4I/4O) the master shall change the data to binary output 30 ms after the parameter response is "1111_{Bin}" at the latest if the optimal parameter call "1110_{Bin}" (End of Communication) is not used.

In the case of a 7.4.0 slave (4I/4O) and if there was no parameter call "1110_{Bin}" or the parameter call "1110_{Bin}" was not answered by the slave, the slave shall not use the master's output data until 60 ms after it answered the parameter request "1111_{Bin}" with "1111_{Bin}".

If there was a parameter call "1110_{Bin}" which was answered by the slave with "1110_{Bin}" within 1 ms, the master's output data is valid immediately after the parameter call "1111_{Bin}".The slave shall answer the first data request after it answered the parameter request "1111_{Bin}" with "1111_{Bin}" with valid input data.

A.6.4.9 Error handling

If the AS-i master is switching over from the normal data cycle to extended functions (Read ID-string, read diagnosis, read / write parameter string) the AS-i Master may interrupt the normal data cycle immediately, that means it is not necessary for the master to terminate a running triple transfer for an analogue value. The slave detects the parameter telegram and shall resynchronize its triple transfer mechanism again.

A.6.5 Slave profiles for combined transaction type 2 (S-7.5.5, S-7.A.5, S-B.A.5)

A.6.5.1 General

The profiles S-7.A.5 and S-7.5.5 are intended for "combined field devices", i.e. AS-i slaves that have digital inputs/outputs as well as serial inputs/outputs. The digital inputs and/or

outputs may be used to transmit switching signals (similar to profile S-1.1). The serial interface may be used to exchange device identification, complex configuration and parameter data, detailed diagnosis information and digital input and/or output data (similar to profile S-7.4).

The profile S-B.A.5 is intended for “serial field devices” that have only serial inputs/outputs.

The serial interface is a full duplex data channel with a minimum capacity of approx. 100 baud in each direction for standard slaves and 50 baud for slaves in extended address mode.

With this profile, it shall be possible to support the integration of AS-i slaves into FDT/DTM (Field Device Tool / Device Type Manager) applications and into OPC (Object Linking and Embedding for Process Control) environments.

Slaves with profile S-7.A.5 or S-B.A.5 shall be capable to work in the extended addressing mode, slaves with profile S-7.5.5 shall be capable to work in standard addressing mode according to this standard.

It uses the combined transaction type 2 as specified in 5.7.3 for data transfer.

A.6.5.2 Codes

The following code combinations shall support combined transaction type 2:

Combined field device in standard address mode: I/O code 7_{Hex}, ID code 5_{Hex}, ID2 code 5_{Hex}.

Combined field device in extended address mode: I/O code 7_{Hex}, ID code A_{Hex}, ID2 code 5_{Hex}.

Serial communication field device in extended address mode: I/O code B_{Hex}, ID code A_{Hex}, ID2 code 5_{Hex}.

A.6.5.3 Definition of I/O data and parameter bits

The meaning of the I/O bits is:

Bit	Type	Meaning	Controller level	As-interf. level	Level-definition
D0	In	Digital data in	0	Low	(not available in S-B.A.5)
			1	High	
D1	In	Digital data in	0	Low	(not available in S-B.A.5)
			1	High	
D2	In	Serial clock in	0	Low	Data bit is valid
			1	High	Data bit is invalid
D3	In	Serial data in	0	Low	Information bit from slave to master: 0
			1	High	Information bit from slave to master: 1
D0	Out	Serial clock out	0	High	Data bit is invalid
			1	Low	Data bit is valid
D1	Out	Serial data out	0	High	Information bit from master to slave: 0
			1	Low	Information bit from master to slave: 1
D2	Out	Digital data out	0	High	(not available in S-B.A.5)
			1	Low	
D3	Out	Digital data out	0	High	(not available in S-B.A.5 and S-7.A.5)
			1	Low	

For the inputs D0 and D1 and the output D2 and D3, no particular semantics exists. There is no particular meaning of these I/O bits defined in this profile. Each of these I/O data bits is an individual remote I/O bit and there is no particular relation between the single bits.

The inputs D2, D3 and the outputs D0, D1 are used as full duplex serial data communication channels according to the specification given below.

It is recommended to use the parameter bits according to the following:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
P0	Parameter Out	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Parameter Out	Input filter	0	Low	Input filter on
			1	High	Input filter off
P2	Parameter Out	---	0	Low	
			1	High	
P3	Out	---	0	Low	(not available in S-B.A.5 and S-.A.5)
			1	High	

The parameter P0 out shall only be used to disable a watchdog function monitoring the continuity of the communication activity of the slave. The watchdog shall be used to determine the behaviour of outputs (digital and/or analogue) in case of interruption of the communication: if the watchdog is enabled, the outputs shall change to a default state; if the watchdog is disabled the outputs shall remain in their respective state.

The parameter P1 out shall only be used to switch on an input filter (digital and/or analogue inputs).

For a slave to be conform with this slave profile the parameters P0 and/or P1 may not be used.

A.6.5.4 Data structure and objects

The data transferred with this transaction type is byte-granular. The data information is headed by a command/response byte which may be followed by one or several data bytes:

command/response	[data]

If the data type has a length of more than one byte, the most significant byte is sent first.

The commands shown in Table A.9 are defined as follows:

Table A.9 – Commands for combined transaction type 2

Code	Command/response	Data
0_{Dec}	Get cyclic data from slave	Followed by 1...8 byte of data (mandatory only if data exists)
1_{Dec}	Put cyclic data to slave	Followed by 1...8 byte of data (mandatory only if data exists)
16_{Dec}	Acyclic standard read service request	Followed by index, length
80_{Dec}	Acyclic standard read service response	Followed by data
144_{Dec}	Acyclic standard read service response not ok	Followed by standard error code
18_{Dec}	Acyclic Vendor specific read service request	Followed by index, length
82_{Dec}	Acyclic Vendor specific read service response	Followed by data
146_{Dec}	Acyclic Vendor specific read service response not ok	Followed by standard error code

Code	Command/response	Data
17_{Dec}	Acyclic standard write service request	Followed by index, length and data
81_{Dec}	Acyclic standard write service response	
145_{Dec}	Acyclic standard write service response not ok	Followed by standard error code
19_{Dec}	Acyclic Vendor specific write service request	Followed by index, length and data
83_{Dec}	acyclic Vendor specific write service response	
147_{Dec}	acyclic Vendor specific write service response not ok	followed by standard error code

For a slave to be conform with this slave profile, commands apart from those defined above may not be implemented. Further commands are under consideration.

Every service request shall be confirmed by the respective response. Cyclic data is sent without confirmation. It is not allowed to open more than one unconfirmed request at any one time.

Upon start of the communication, the master shall first read the ID object and shall set up the analogue input data image and the analogue output data image according to the information given in byte 4 of the ID object. The cyclic input data of an A-slave is copied into channel 0 and 1 of the respective slave addresses and the cyclic input data of a B-slave into channel 2 and 3. The data of channel 0 and 1 of the analogue output data image is transferred to the A-slave, the data of channel 2 and 3 to the B-slave. In the case of single byte data, the high byte of the analogue input/output data image is used.

The acyclic read and write services use the following data structure:

Table A.10 – Acyclic write service request (Type 2)

Byte	Bits: (0-7 for byte constructions; 0-15 for word constructions)							
	7	6	5	4	3	2	1	0
0	Code							
1	Index							
2	Length (1…(x-2))							
3…x	Data							

Table A.11 – Acyclic read service request (Type 2)

Byte	Bits: (0-7 for byte constructions; 0-15 for word constructions)							
	7	6	5	4	3	2	1	0
0	Code							
1	Index							
2	Length (1…x)							

Table A.12 – Acyclic write service response (Type 2)

Byte	Bits: (0-7 for byte constructions; 0-15 for word constructions)							
	7	6	5	4	3	2	1	0
0	Code							

Table A.13 – Acyclic read service response (Type 2)

Byte	Bits: (0-7 for byte constructions; 0-15 for word constructions)							
	7	6	5	4	3	2	1	0
0	Code							
1…x	Data							

NOTE 1 It is recommended to use values less than or equal to 32 for the variable x.

A timeout condition occurs when a time of more than 1 s elapses between the end of the service request and the beginning of the respective response. In this case, the master shall signal this condition to the controller. If a slave receives a second request without having responded to the first, it shall interrupt its acyclic serial communication.

There is no timeout for cyclic data transfers defined. This allows both master and slave to transmit data cyclically or event driven. If master and/or slave transmit data event driven only, they shall transmit their data at least once after having read the ID object to initialise the analogue input data image of the master and/or the output data of the slave.

The length information shall be handled by master and slave in the following way: If the master requests a data length of more bytes than are defined in the slave, the slave may return the maximum number of defined bytes and then end the transmission. If the master requests less bytes than defined in the slave, the slave shall send as many bytes as requested and then end transmission.

Table A.14 – List of index 0 (mandatory): ID object (R)

Byte	Bits: (0-7 for byte constructions; 0-15 for word constructions)							
	15	14	13	12	11	10	9	8
	7	6	5	4	3	2	1	0
0	Vendor ID (high)							
1	Vendor ID (low)							
2	Device ID (high)							
3	Device ID (low)							
4	0: output analogue; 1: output trans-parent	000_{Bin}: no output 001_{Bin}: 1 byte output 010_{Bin}: 1 word output 011_{Bin}: 2 words output 100_{Bin}: 3 words output 101_{Bin}: 4 words output 110_{Bin} to 111_{Bin}: reserved			0: input analogue; 1: input trans-parent	000_{Bin}: no input 001_{Bin}: 1 byte input 010_{Bin}: 1 word input 011_{Bin}: 2 words input 100_{Bin}: 3 words input 101_{Bin}: 4 words input 110_{Bin} to 111_{Bin}: reserved		
5 to 31	Vendor defined							

NOTE 2 For profiles S-7.A.5 and S-B.A.5, the identifiers for 3 or 4 words should not be used.

NOTE 3 If analogue input and/or analogue output is selected, the input and/or output should be 1 word in INT format for compatibility reasons with profiles S-7.3 and S-7.4.

Table A.15 – List of index 1 (mandatory): diagnosis object (R)

Byte	Bits: (0-7 for byte constructions; 0-15 for word constructions)							
	7	6	5	4	3	2	1	0
0	Standard diagnostic code							
1 to 31	vendor defined							

The vendor ID shall not equal 0 and is assigned by the authority. The product ID and the optional vendor defined data (e.g. serial number of the device) is assigned by the manufacturer

The vendor ID together with the product ID identifies the Device Profile which defines the format, length and content of all information that may be exchanged between the device and the network and the behaviour of the device.

The standard error code is defined as follows:

Error code	Meaning
0	No error
1	Illegal index
2	Illegal length
3	Request not implemented
4	Busy (request was not executed completely within time frame; try again later)

The standard diagnostic code is defined as follows:

Diagnostic code	Meaning
0	No error
255	General error

The vendor defined diagnostic code is optional.

Slaves are not allowed to issue any acyclic service without previous request of the master. If a slave wants to transmit diagnostic data, it may set the Peripheral Fault flag. The controller then shall issue an acyclic read service request for the diagnostic object.

It is recommended that device profiles are defined according to IEC 61915.

A.6.5.5 Additional requirements

If the "combi field device" is a general purpose input module and uses M12 connectors, according to IEC 60947-5-2, Annex D, the plug it is recommended to use the following pinning:

– pin 1 = (+) power supply;
– pin 2 = analogue input (voltage or current);
– pin 3 = (−;) power supply;
– pin 4 = binary input;
– pin 5 = GND (optional).

A.6.6 Slave profiles for combined transaction type 3 (S-7.A.7, S-7.A.A)

A.6.6.1 General

A.6.6.1.1 S-7.A.7

Slave profile S-7.A.7 is intended for 4I/4O slaves in extended addressing mode.

It uses the combined transaction type 3 as specified in 5.7.4 for data transfer.

A.6.6.1.2 S-7.A.A

Slave profile S-7.A.A is intended for 8I/8O slaves in extended addressing mode.

It uses the combined transaction type 3 as specified in 5.7.4 for data transfer.

A.6.6.2 Codes

The I/O configuration shall be 7_{Hex}.

The ID code shall be A_{Hex}.

The Extended ID2 code shall be 7_{Hex} in the case of the 4I/4O slave and A_{Hex} in the case of the 8I/8O slave.

The Extended ID1 code shall be 7_{Hex} (fixed value) in the case of the 4I/4O slave. The Extended ID1 code shall be 7_{Hex} (fixed value) in the case of the 8I/8O slave with non-consistent input and output data. The Extended ID1 code shall be 6_{Hex} (fixed value) in the case of the 8I/8O slave with consistent input and output data.

NOTE The fixed value of ID1 code allows more detailed further extensions of this profile.

A.6.6.3 Semantics of I/O data bits

A.6.6.3.1 S-7.A.7

The meaning of the I/O bits is:

Bit	Type	Meaning	Controller level	As-i-level	Level-definition
D3	Input	Remote in	0	Low	
			1	High	
D2	Input	Remote in	0	Low	
			1	High	
D1	Input	Remote in	0	Low	
			1	High	
D0	Input	Remote in	0	Low	
			1	High	
D3	Output	(used for extended address)			
D2	Output	Output Multiplex-bit	0	High	D0/D1-values transferred
		D0/D1|D2/D3	1	Low	D2/D3-values transferred
D1	Output	D1 if D2=1	0	High	
		D3 if D2=0	1	Low	
D0	Output	D0 if D2=1	0	High	
		D2 if D2=0	1	Low	

At the ports of a slave for D0 to D3 no particular semantics exist. There is no particular meaning of these I/O bits defined in this profile. Each of these I/O data bits is an individual remote I/O bit and there is no particular relation between the single bits.

For further information, see the manufacturer's documentation. The prolonged refresh period for the outputs shall be stated in the documentation. Dependent from the implementation in the slave, all four outputs may operate simultaneously or not simultaneously. The kind of implementation shall be stated in the manufacturers documentation.

A.6.6.3.2 S-7.A.A

The meaning of the I/O bits is:

Bit	Type	Meaning	Controller level	As-i-level	Level-definition
D3	Input	Input Multiplex Bit 1	0	Low	
			1	High	
D2	Input	Input Multiplex Bit 0	0	Low	
			1	High	
D1	Input	Remote in	0	Low	
			1	High	
D0	Input	Remote in	0	Low	
			1	High	
D3	Output	(used for extended address)			
D2	Output	Inverted Input Multiplex Bit 0 of previous data transfer	0	High	
			1	Low	
D1	Output	Remote out	0	High	
			1	Low	
D0	Output	Remote out	0	High	
			1	Low	

At the ports of a slave for D0 to D7 no particular semantics exist. There is no particular meaning of these I/O bits defined in this profile. Each of these I/O data bits is an individual remote I/O bit and there is no particular relation between the single bits.

In case of interruption of the communication or other errors the data shall be set to default 00_{Hex}.

For further information, see the manufacturer's documentation. The prolonged refresh period for the inputs and outputs shall be stated in the documentation. Dependent from the implementation in the slave, all eight outputs may operate simultaneously or not simultaneously. The kind of implementation shall be stated in the manufacturer's documentation.

A.6.6.4 Semantics of parameters

It is recommended to use the parameter bits as follows:

Bit	Type	Meaning	Controller -level	As-i- level	Level-definition
P0	Parameter	Watchdog function	0	Low	Watchdog disabled
			1	High	Watchdog enabled
P1	Parameter	Input filter	0	Low	Input filter on
			1	High	Input filter off
P2	Parameter	---	0	Low	---
			1	High	---
P3	Parameter	Not available			

The meaning of P2 will be defined later.

P0 shall only be used to disable a watchdog function monitoring the continuity of the communication activity and alternation of the information bit I2 of the slave.

The minimum watchdog time (communication activity) shall be equal to or more than 40 ms and the maximum watchdog time shall be less than or equal to 100 ms to set the actuators/outputs inactive.

The parameter P1 may be used to switch on an input filter that suppresses input pulses in all input channels.

For a slave to be conform with this profile, the parameter bits P0 to P2 do not have to be used.

A.6.6.5 Ports and plugs

A.6.6.5.1 Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI-). On their realization there are no restrictions in addition to the specifications.

A.6.6.5.2 Port of input data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, the plug is recommended to be female with the following pinning:

– pin 1 = (+) power supply;

– pin 2 = input data bit,

– pin 3 = (−) power supply;

– pin 4 = input data bit.

If Pin 2 and Pin 4 are available, Pin 2 and 4 of such a 12 mm or 8 mm plug is recommended to be electrically bridged. The bridge is recommended to be built in such a way that it cannot be removed with simple tools.

A.6.6.5.3 Port of output data

If a 12 mm or 8 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator) the plug is recommended to be female with the following pinning:

– pin 1 = (+) power supply in the case of a npn-logic;
– pin 2 = not connected;
– pin 3 = (−) power supply in the case of a pnp-logic;
– pin 4 = output, parameter, etc.

On the other hand, for a passive output (e.g. relay contacts) the plug is recommended to be male with the following pinning:

– pin 1 = change-over contact;
– pin 2 = normally closed (NC) contact;
– pin 4 = normally open (NO) contact.

A.6.6.5.4 Power port

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line the plug is recommended to be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;
– pin 3 = (−) power;
– pin 4 = not used.

A.6.6.6 Marking

On the enclosure the remote I/O ports shall have a clear unique identification of the available ports, such as I/O data bits and energy supply from the AS-i-system, as well as a clear identification of the pnp- or npn-logic used for the ports.

The ports for the 4 I/O data bits D0 to D3 are recommended to be marked by the numbers 1 to 4. In general, for the unique identification of the ports a single letter may be used, such as, for example I for input data, O for output data, etc. Only capital letters shall be used. The letters A, B, and P are reserved for antivalent I/Os, bidirectional I/Os, and parameter outputs, respectively.

A.6.6.7 Additional requirements

In case of pnp-logic, it is recommended that the voltage levels and currents at the ports of a remote I/O device are in accordance with IEC 61131-2 input port. For the npn-logic, the same IEC 61131-2 shall be used accordingly.

The value of the time delay for an I/O signal between the arrival at the port of a remote I/O device and the availability on the AS-i line is recommended to be less than 5 ms for input data (for 4I/4O slaves) or 40 ms (for 8I/8O slaves) and 40 ms for output data. The actual value of the time delay shall be given in the product documentation.

As an option, the remote I/O output ports may have an integrated watchdog function monitoring the continuity of the communication. Such a watchdog function, however, shall not have a response time less than 40 ms. In the product documentation, it shall be stated whether the remote I/O ports contain a watchdog function or not.

NOTE For remote I/O ports with an auxiliary energy supply, the availability, overload, or short circuit, etc. of the auxiliary energy may be monitored by electronic means. If such a monitor function is used, it should be realized either by using the local reset function of the slave, which inhibits the communication to the master, and/or the periphery fault bit. The use of this monitor function in the remote I/O ports should be stated in the product documentation.

A.6.7 Slave profiles for combined transaction type 4 (S-7.A.8, S-7.A.9)

A.6.7.1 General

This profile offers the possibility of transmitting up to 16 bit data from the slave in extended addressing mode to the master. One output bit may be used as binary output of a slave or to switch over between two input channels. It uses the combined transaction type 4 as specified in 5.7.5 for data transfer.

The extended ID1 code determines the format and the length of the data.

A.6.7.2 Codes

The I/O code shall be 7_{Hex}.

The ID code shall be A_{Hex}.

The ID2 code shall be 8_{Hex} for the single channel slave with a 1 bit digital output and 9_{Hex} for the dual channel slave.

The extended ID-Code 1 shall be used as shown in Figure A.6:

	S-7.A.8:	S-7.A.9:
ID1 (Hex)	Definition	Definition
0	Not allowed	Slave transmits 14 bit analogue value(s)
1	Not allowed	Slave transmits 14 bit analogue value(s)
2	Not allowed	Slave transmits 14 bit analogue value(s)
3	Slave transmits 8 bit transparent data	Slave transmits 14 bit analogue value(s)
4	Slave transmits 12 bit transparent data	Slave transmits 14 bit analogue value(s)
5	Slave transmits 16 bit transparent data	Slave transmits 14 bit analogue value(s)
6	Slave transmits 12 bit analogue value	Slave transmits 12 bit analogue value(s)
7	Slave transmits 14 bit analogue value	Slave transmits 14 bit analogue value(s)

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Figure A.6 – Definition of the extended ID1 code bits for S-7.A.8 and S-7.A.9

The ID-Code 1 is fixed in S-7.A.8 and may be user definable in S-7.A.9.

A.6.7.3 Semantics of I/O data and parameters

The semantics of the I/O data bits and of the parameter bits are given in 5.7.5.1. The use of the parameter bits is optional and shall be stated in the product documentation.

A.6.7.4 Ports and plugs

If a 12 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, the plug shall be female with the following recommended pinning.

Voltage/current input:

– pin 1 = (+) power supply;
– pin 2 = positive current/voltage input;
– pin 3 = (−) power supply;
– pin 4 = negative current/voltage input;
– pin 5 = functional earth (optional).

Resistance input, for example Pt100:

– pin 1 = positive current output;
– pin 2 = positive voltage input;
– pin 3 = negative current output;
– pin 4 = negative voltage input;
– pin 5 = functional earth (optional).

1 bit digital port (S-7.A.8 only):

– pin 1 = (+) power supply in the case of a npn logic;
– pin 2 = not connected;
– pin 3 = (−) power supply in the case of a pnp logic;
– pin 4 = output;
– pin 5 = functional earth (optional).

Combined port (S-7.A.8 only):

– pin 1 = (+) power supply;
– pin 2 = analogue input (voltage, current or temperature);
– pin 3 = (−) power supply;
– pin 4 = output;
– pin 5 = functional earth (optional).

A.6.7.5 Additional requirements

Slaves that support combined transaction type 4 may transfer analogue values or digital values (transparent mode). The data representation and data handling is different for these two types of slaves.

A.6.7.5.1 Slaves with transparent mode

Slaves with transparent mode transfer digital values of 8, 12 or 16 bit length to the AS-i-Master. These values may be, for example counter values or digital inputs. Non-transferred bits are filled with 0 by the master.

Example:

Data bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 bit transparent	0	1	0	0	0	1	1	0	0	1	1	1	0	1	1	0
12 bit transparent	0	1	0	0	0	1	1	0	0	1	1	1	**0**	**0**	**0**	**0**
8 bit transparent	0	1	0	0	0	1	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

There is no under range/over range or out of range for transparent values.

A.6.7.5.2 Default value for transparent input slaves

When one of the following conditions occur, the AS-i Master will set the input data of an transparent input channel to the default value 0_{Hex}:

– after initialization of the AS-i Master, no valid data transfer according to combined transaction type 4 has been accomplished for this channel;

– slave is not in List of Active Slaves (LAS).

If applicable, the master signals to the controller via a valid bit that the measurement value is invalid.

A.6.7.5.3 Analogue slaves

Data of analogue input slaves are represented as two's complement values with a fixed length of 12 or 14 data bits. For sensors which need less resolution the least significant nibbles are not transmitted. These are filled with 0 by the master.

Example:

Data bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
14 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	0	0	**0**	**0**
12 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	**0**	**0**	**0**	**0**

As data is represented as two's complement values, bit D15 represents the sign bit.

If the extended ID Code 1 is set to 7_{Hex} the analogue data is transferred in 4 consecutive cycles. Bit D1 in the last cycle contains the overflow bit and Bit D0 the status bit.

If the extended ID Code 1 is set to 6_{Hex} the analogue data is transferred in 3 consecutive cycles. The master shall request the overflow bit and the status bit in the fourth cycle only if the slave data signals overflow ($7FF_{Hex}$) or underflow (800_{Hex}).

The additional information bits have the following meaning:

Bit	Meaning	Controller-level	As-i-level	Level-definition
D1	Overflow	0	Low	Value within measuring range
		1	High	Value out of measuring range
D0	Status	0	Low	Status not ok
		1	High	Status ok

A.6.7.5.4 Measurement range of analogue slaves

Examples for the value range of an analogue input slave.

Units (controller, 16 bit)		Units (slave, 12 bit)		Range	Remarks
Decimal	**Hexadecimal**	**Decimal**	**Hexadecimal**		
32767	$7FFF_{Hex}$	2047	$7FF_{Hex}$	Out of range	Overflow bit set
32736 . -32752	$7FE0_{Hex}$. 8010_{Hex}	2046 . -2047	$7FE_{Hex}$. 801_{Hex}	Nominal range	Measurement value meets the specified tolerance
-32768	8000_{Hex}	-2048	800_{Hex}	Out of range	Overflow bit set

800_{Hex} always represents underflow, $7FF_{Hex}$ represents always overflow condition.

Units (controller, 16 bit)		Units (slave, 14 bit)		Range	Remarks
Decimal	Hexadecimal	Decimal	Hexadecimal		
32767	$7FFF_{Hex}$	8191	$1FFF_{Hex}$	Out of range	Overflow bit set
32760 . -32764	$7FF8_{Hex}$. 8004_{Hex}	8190 . -8191	$1FFE_{Hex}$. 2001_{Hex}	Nominal range	Measurement value meets the specified tolerance
-32768	8000_{Hex}	-8192	2000_{Hex}	Out of range	Overflow bit set

2000_{Hex} always represents underflow, $1FFF_{Hex}$ represents always overflow condition.

The overflow bit shows that the measurement value is not valid (overflow or underflow).

A.6.7.5.5 Default value for analogue input slaves

If one of the following conditions occurs, the AS-i Master will set the input data of an analogue input channel to the default value $7FFF_{Hex}$:

- after initialization of the AS-i Master, no valid data transfer according to combined transaction type 4 has been accomplished for this channel;
- slave is not in List of Active Slaves (LAS);
- the last data transfer for this channel was finished with valid bit set to “0”;
- the overflow bit is set.

In this way, it indicates to the controller that the measurement value is invalid.

A.6.8 Slave profiles for combined transaction type 5 (S-6.0.X)

A.6.8.1 General

This profile describes a method of high speed transmission of 8, 12 or 16 bit bidirectional consistent data using 2, 3 or 4 consecutive slave addresses.

It uses the combined transaction type 5 as specified in 5.7.6 for data transfer.

NOTE Changing the address of a slave of this type may not function the same way as with other slaves. In particular, the auto-address assignment will need special attention of the user as this edition of the standard does not contain auto-addressing procedures for slaves supporting transaction type 5.

A.6.8.2 Codes

The I/O Configuration shall be 6_{Hex} for all slave addresses of the group.

The ID Code shall be 0_{Hex} for all slave addresses of the group.

The extended ID Code 2 shall be set according to the Table 13.

The possible combinations of the IO Configuration and ID Codes are:

	Address n "physical slave"	Address n+1	Address n+2	Address n+3
16 bit data	S-6.0.4 / S-6.0.C	S-6.0.7	S-6.0.6	S-6.0.5
12 bit data	S-6.0.3 / S-6.0.B	S-6.0.6	S-6.0.5	
8 bit data	S-6.0.2 / S-6.0.A	S-6.0.5		

A.6.8.3 Semantics of I/O data bits and parameter bits

The semantics of the I/O data bits and of the parameter bits are given in 5.7.6.2. The use of the parameter bits is optional and shall be stated in the product documentation.

A.6.8.4 Ports and plugs

A.6.8.4.1 S-6.0 – Port of input data

If a 12 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, the plug shall be female with the following recommended pinning:

Voltage/current input:

– pin 1 = (+) power supply;
– pin 2 = positive current/voltage input;
– pin 3 = (−) power supply;
– pin 4 = negative current/voltage input;
– pin 5 = functional earth (optional).

Resistance input, for example Pt100:

– pin 1 = positive current output;
– pin 2 = positive voltage input;
– pin 3 = negative current output;
– pin 4 = negative voltage input;
– pin 5 = functional earth (optional).

A.6.8.4.2 S-6.0 – Port of output data

If a 12 mm plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, then, for an active output (including energy for e.g. an actuator), the plug shall be female with the following recommended pinning:

– pin 1 = positive current/voltage output;
– pin 2 = not connected;
– pin 3 = negative current/voltage output;
– pin 4 = output, parameter, etc.
– pin 5 = functional earth (optional).

A.6.8.4.3 S-6.0 – Power port

If a 12 mm or 8 mm plug is used for the interconnection of the auxiliary energy or the energy from the AS-i line, the plug shall be male for energy input and female for energy output with the following pinning:

– pin 1 = (+) power;
– pin 2 = not used;
– pin 3 = (−) power;
– pin 4 = not used.

A.6.8.5 Additional requirements

The data bits of the up to 4 consecutive slave addresses are arranged in the following way:

Data bit # in the AIDI / AODI		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 bit	Slave address	n+3	n+3	n+3	n+3	n+2	n+2	n+2	n+2	n+1	n+1	n+1	n+1	n	n	n	n
	Slave data bit	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
12 bit	Slave address	n+2	n+2	n+2	n+2	n+1	n+1	n+1	n+1	n	n	n	n				
	Slave data bit	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	**0**	**0**	**0**	**0**
8 bit	Slave address	n+1	n+1	n+1	n+1	n	n	n	n								
	Slave data bit	D3	D2	D1	D0	D3	D2	D1	D0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

If applicable, the data word is filled with 0 in the LSBs that are not transmitted.

A.6.8.6 S-6.0 – Data representation

Slaves of profile S-6.0 may transfer analogue values or digital values (transparent mode) of 8, 12 or 16 bit length. The data representation and data handling is different for these two types of slaves.

A.6.8.6.1 S-6.0 – Slaves with transparent mode

Slaves with transparent mode transfer digital values of 8, 12 or 16 bit length from/to the AS-i-Master. These values may be, for example counter values or digital input / outputs.

There is no under range/over range or out of range for transparent values.

A.6.8.6.2 Default value for transparent slaves

The default value of transparent slaves in the Analogue Input Data Image of the master is 0000_{Hex}. The default value of transparent slaves in the Analogue Output Data Image of the master is 0000_{Hex}.

A.6.8.6.3 S-6.0 – Analogue slaves

Data of S-6.0 analogue input / output slaves are represented as two's complement values with a fixed length of 8, 12 or16 data bits. For sensors that provide less resolution, the least significant bits are filled with zeros.

Example:

Data bit #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	0	0	1	1
12 bit analogue value	0	1	0	0	0	1	1	0	0	1	1	1	**0**	**0**	**0**	**0**
8 bit analogue value	0	1	0	0	0	1	1	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

As data is represented as two's complement values, bit D15 represents the sign bit.

A.6.8.6.4 Measurement range of analogue slaves

The possible measurement range is from 8001_{Hex} to $7FFE_{Hex}$. The limits of nominal range, over range and under range depend on the specific slave implementation.

8000_{Hex} always represents underflow; $7FFF_{Hex}$ represents always overflow condition and shall not be used as regular value. If the slave has only 8 or 12 bit data length the overflow values of $7F_{Hex}$ or $7FF_{Hex}$ are converted to $7FFF_{Hex}$ as well to be consistent with the data formats of other combined transaction types. If the slave has only 8 or 12 bit data length, the underflow values are filled up with 0.

A.6.8.6.5 Default value for analogue slaves

In case of an analogue slave $7FFF_{Hex}$ is the default value in the Analogue Input Data Image (AIDI). The default value of the Analogue Data Output Image (AODI) is always 0000_{Hex}.

A.6.9 Safety related slaves (S-0.B, S-7.B)

A.6.9.1 S-X.B – General

This profile describes AS-i safety related slaves.

It uses the combined transaction for safety related slaves as specified in 5.7.7 for data transfer.

NOTE Reference to IEC 61508 for safety related product standards, or common reference to safety relevant standards should be taken into account.

A.6.9.2 S-X.B – Codes

The I/O-configuration shall be 0_{Hex} for safety related inputs or 7_{Hex} for safety related inputs and standard outputs.

The ID-code shall be B_{Hex}.

The ID2 code shall be 0_{Hex} for safety related inputs for mechanical switches.

The ID2 code shall be 1_{Hex} for safety related inputs for electronic devices (reserved).

The use of ID2 code is optional.

A.6.9.3 S-X.B – Semantics of I/O data

The semantics of the safety related input data bits is summarized as follows:

Input	State	Meaning	As-i-level	Remark (i.e. mechanical switches)
Channel 1 Channel 2	Current flowing Current flowing	On-state	Defined series of 8 different code nibbles	Both contacts closed
Channel 1 Channel 2	No current flowing Current flowing	Off-state (error)	D0, D1 = 0 D2, D3 = X	Contact 1 open Contact 2 closed
Channel 1 Channel 2	Current flowing No current flowing	Off-state (error)	D0, D1 = X D2, D3 = 0	Contact 1 closed Contact 2 open
Channel 1 Channel 2	No current flowing No current flowing	Off-state	D0 … D3 = 0	Both contacts open
“X” means “half” code nibbles.				

The semantics of the standard out data bits is summarized as follows:

Bit	Type	Meaning	Controller-level	As-i-level	Level-definition
D0	-	Remote Out	0	High	-
			1	Low	-
D1	-	Remote Out	0	High	-
			1	Low	-
D2	-	Remote Out	0	High	-
			1	Low	-
D3	-	Remote Out	0	High	-
			1	Low	-

For D0 to D3, no particular semantics exists. There is no particular meaning of the Out data

bits. Each Out data bit is an individual remote Out bit and there is no particular relation between the single bits.

A failure of the device may be signalled via the periphery fault bit of the status register.

A.6.9.4 S-X.B – Semantics of parameters

The use of parameters is optional in this profile, if not otherwise defined in the sub-profiles.

If parameters are used all special functions which were controlled by these parameters shall be disabled by default (parameter bits P0..3 = 1).

A.6.9.5 S-X.B – Ports and plugs

A.6.9.5.1 S-X.B – Port to the AS-i-line

There are two contacts for the interconnection of the slave to the AS-i-line (ASI+/ASI-). On their realisation, there are no restrictions in addition to the specifications.

A.6.9.5.2 S-X.B – Port of input data

If ID-code ID2 = 0_{Hex} and a 12 mm (4(5)-pin) or 8 mm (4-pin) plug, according to IEC 60947-5-2, Annex D, is used for the interconnection, the plug shall be female with the following pinning:

Connection of mechanical switches (NC), [ID2=0_{Hex}]:

- pin 1 = channel 1;
- pin 2 = channel 1;
- pin 3 = channel 2 (optional);
- pin 4 = channel 2 (optional);
- pin 5 (optional) = ground (optional).

The availability of the optional port has to be stated in the documentation.

NOTE Safety related devices with the following pinout may be connected to the ports of the module:

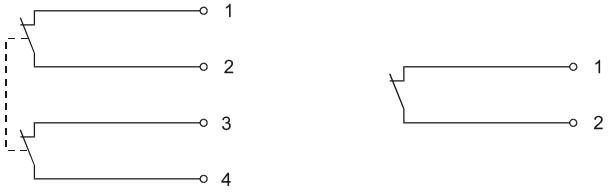

Figure A.7 – Connection of mechanical switches

A.6.9.6 S-X.B – Marking

On the enclosure, the remote safety related input port shall have a clear unique identification of this profile.

A.6.9.7 S-X.B – Additional requirements

The value of the time delay for an input signal between the state change of the port of a remote safety related input device and the availability on the AS-i line shall be less than 5 ms for the input data, if a transition from the on-state to the off-state takes place.

The detailed function of the periphery fault bit shall be described in the product documentation of the device. The maximum possible safety integrity level, according to IEC 61508, shall be described in the product documentation.

NOTE The safe data transfer is only guaranteed in conjunction with a safety related control unit. The safety related control unit controls the correctness of the behaviour of the AS-i master (i. e. linear addressing from the lowest to highest address). That means for future changes in this standard, the behaviour of the safety related control unit has to be taken into account.

Annex B
(normative)

Master profiles

B.1 Standard masters

Standard masters differ from extended masters by the fact that they support only up to 31 standard or A-slaves.

B.1.1 Slave acceptance criteria for standard masters

Standard Masters support up to 31 standard AS-i Slaves or A-slaves. B-slaves will not work with Standard Masters. It is not allowed to connect B-slaves to standard masters.

B.1.2 Profiles for standard masters (M0, M1, M2)

For standard masters the following profiles are available:

Profile identifier	Name	Remark
M0	Minimum standard master	Only for data I/O
M1	Full standard master	Data I/O and parameter and all other functions
M2	Reduced standard master	Data I/O and minimum parameter functions

B.1.3 Definition of data types of the standard master

This subclause contains the data definitions for standard masters in detail.

B.1.3.1 Data

Max_Data

Max_Data defines the maximum number of data elements in the data image (input and output). The data image of a standard master provides the complete input and output data of 31 slaves. Therefore Max_Data is 31.

Max_Data = 31

Input Data (slave_in)

Slave type	Data type	Bit3	Bit2	Bit1	Bit0
Standard slave and Extended slave:	slave_in	D3	D2	D1	D0

Output Data (slave_out)

Slave type	Data Type	Bit3	Bit2	Bit1	Bit0
Standard slave					
IO = x / ID ≠ A	slave_out	D3	D2	D1	D0
Extended Slave IO = x / ID=A	slave_out	Sel = 0	D2(A)	D1(A)	D0(A)
x: don't care.					

NOTE For a slave with extended address mode (ID=A_{Hex}) D3 = 1 addresses a B-slave. This causes an error and is therefore not allowed.

B.1.3.2 Addresses (Addr, Addr_wS0)

Data Type	Address bits	Value range
Addr	A4 A3 A2 A1 A0	1≤ i ≤ 31
Addr_wS0	A4 A3 A2 A1 A0	0≤ i ≤ 31

B.1.3.3 Parameter (Param)

Slave type	Data type	I3	I2	I1	I0
Standard slave	Param	P3	P2	P1	P0
A-Slave	Param	/Sel = 1	P2(A)	P1(A)	P0(A)

B.1.3.4 Configuration Data (Config_Data)

Max_Slaves

Max_Slaves defines the maximum number of slaves which are available in the AS-i system. A standard master supports 31 slaves. Therefore *Max_Slaves* is 31.

Max_Slaves = 31

Slave type	Data type	ID – Code		IO – Code	
		Bit3	Bit0	Bit3	Bit0
Standard slave	Config_Data	ID3	ID0	IO3	IO0
Extended slave	Config_Data	ID3	ID0	IO3	IO0

Optionally a standard master may support extended ID-Code 1 and 2 as defined in 5.6.3.

B.1.3.5 Slave lists (List, List_wS0)

Data type	Bit31 .....Bit1	Bit0
List	S31.....S1	-
List_wS0	S31.....S1	S0
-: not available Sx: bit corresponds to slave x		

B.1.3.6 Info5

Data type	I4	I3	I2	I1	I0	Command
Info5	1	0	0	0	0	Read_IO_Configuration
	1	0	0	0	1	Read_ID_Code
	1	1	1	1	0	Read_Status

B.2 Extended masters

Extended masters support up to 31 standard AS-i- or A-slaves or up to 62 slaves with extended addressing mode or any combination thereof. Slaves with extended addressing mode may be A- or B-slaves.

B.2.1 Slave acceptance criteria for extended masters

Possible combinations of slaves on one single slave address:

Slave type		Remark
Standard slave		One single standard slave on one address
IO = x / ID ≠ A		
Extended slave: ID=A		
A – Slave	B – Slave	
IO = x	-	One single A-slave
-	IO = x	One single B-Slave
IO = x	IO = x	One pair of A/B-Slaves
-: not available x: don't care. Other possibilities not allowed.		

B.2.2 Profiles for extended masters (M3, M4)

Extended masters may have the following profiles:

Profile identifier	Name	Remark
M3	Full extended master	Data I/O and parameter and all other functions at controller interface and support of Combined transaction type 1
M4	Version 3 extended master	M3 functionality plus support of Combined transaction type 2, 3, 4 and 5

NOTE To avoid changes in an existing process image (e.g. adapted from standard masters) the following rule for AS-i system set-up is suggested: If the number of slaves is less than 32, it is recommended not to use B-slaves. It is recommended to first fill up the system with standard slaves and/or A-slaves and then use B-slaves. No additional process image is necessary if there is no B-slave connected. The standard and A-slaves will appear in a process image of the extended master in the same way as they appear in the process image of a standard master. The B-slaves will reside in an additional ("extended") process data image which is only available on an extended master.

B.2.3 Definition of data types of the extended master

B.2.3.1 Data definition

This subclause contains the detailed data definitions for extended masters.

Max_Data

Max_Data defines the maximum number of data elements in the data image (input and output). The data image of an extended master provides the complete input and output data of 31 standard slaves / A-slaves and 31 B-slaves.

The representation and mapping of the slave I/O data image is defined by the master implementation and by the controller-system data- and interface model. Therefore, it is not described in this definitions.

Max_Data = 62

Input Data (slave_in)

Slave type	Data type	Bit3	Bit2	Bit1	Bit0
Standard slave and extended slave (A- and B-slave)	slave_in	D3	D2	D1	D0

Output data (slave_out)

Slave type	Data type	Bit3	Bit2	Bit1	Bit0	
Standard slave						
IO = x / ID ≠ A	slave_out	D3	D2	D1	D0	Part A image
Extended slave (A-slave) IO = x / ID=A	slave_out	Sel = 0	D2(A)	D1(A)	D0(A)	
Extended slave (B-slave) IO = x / ID=A	slave_out	Sel = 1	D2(B)	D1(B)	D0(B)	Part B image
x: don't care.						

NOTE The Select Bit for A-/B-slaves is set internally in the AS-i master. Its value in the output data image is masked out.

B.2.3.2 Addresses (Addr, Addr_wS0)

Data type	Address bits	Value range	I3	Value range	
				A	B
Addr	A4 A3 A2 A1 A0	1≤ i ≤ 31	Sel	0	1
Addr_wS0	A4 A3 A2 A1 A0	0≤ i ≤ 31	Sel	0	1

B.2.3.3 Parameter (Param)

Slave type	Data type	I3	I2	I1	I0
Standard slave	Param	P3	P2	P1	P0
A-Slave	Param	/Sel = 1	P2(A)	P1(A)	P0(A)
B-Slave	Param	/Sel = 0	P2(B)	P1(B)	P0(B)

NOTE The Select Bit for A-/B-slaves is set internally in the AS-i master. Its value in the Parameter Image (PI) and Permanent Parameter (PP) is masked out.

B.2.3.4 Configuration Data (Config_Data)

Max_Slaves

Max_Slaves defines the maximum number of slaves which are available in the AS-i system. An extended master supports 62 slaves. Therefore *Max_Slaves* is 62.

Max_Slaves = 62

Slave type	Data type	ID – Code	IO – Code	Ext. ID – Code_1	Ext. ID – Code_2
		Bit3.....Bit0	Bit3.....Bit0	Bit3..... Bit0	Bit3.....Bit0
Standard slave	Config_Data	ID3..... ID0	IO3..... IO0	ExID1.3..ExID1.0	ExID2.3..ExID2.0
Extended slave	Config_Data	ID3.....ID0	IO3.....IO0	ExID1.3..ExID1.0	ExID2.3..ExID2.0

B.2.3.5 Slave lists (List, List_wS0)

Data type	Bit63 .....Bit33	Bit 32	Bit31 .....Bit1	Bit0
List	S63 .....S33	-	S31.....S1	-
List_wS0	S63 .....S33	-	S31..... .....S1	S0
-: not available Sx: bit corresponds to slave x				

B.2.3.6 String

The data type "String" is an array of bytes with no explicit structure.

B.3 Implementation of profiles / PICS (Protocol Implementation Conformance Statement)

B.3.1 Implementation of different profiles

All profiles are intended to define the functionality of an AS-i master at the interface to the user.

The names of the functions in the list of assignment to the profiles are in the manner of software calls. This does not mean that only software calls are allowed to be implemented. It is only done to have an identical name structure for all functions, which a user could access at his interface.

The implementation of the function at the user interface according to the specific profile depends on the type of AS-i master. It is allowed to provide any function, for example by switches and signalling lights (e.g. LEDs) at the front panel of an AS-i master, if possible, or by software calls, which are accessible for user applications from the controller device to the AS-i master.

B.3.2 Behaviour according to the profiles

It is mandatory to any AS-i master to have a well-defined behaviour for start-up, running and shutdown as described in this standard.

Also error reporting of AS-i master is recommended in all masters. As minimum requirement the flag "Config_OK" shall be available. This flag may be combined with other status or error information. The flag Config_OK may not be evaluated in configuration mode if it is combined with other flags.

If there are several controller interfaces, for example front panel with switches and lights combined with software calls interface, the error flag shall be accessible on all controller interfaces of the AS-i master.

B.3.3 List of functions and profile assignment

The added list will show the names, the results and functionality of the functions in shortcut. They are described in the manner of software calls. The functions are numbered ascending.

See below for a complete list of functions and profile assignment.

A	Function or call at controller interface	Data transfer / function	Profile				
			M0	M1	M2	M3	M4
1	Image, Status = Read_IDI ()	IDI → Controller	M	M	M	M	M
2	Status = Write_ODI (Image)	Controller → ODI	M	M	M	M	M
3	Status = Set_Permanent_Parameter (S_Addr, S_Param)	Controller → PP[x]	O	M	O	M	M
4	S_Param, Status = Get_Permanent_Parameter (S_Addr)	PP[x] → Controller	O	M	O	M	M
5	Status, RS_Param = Write_Parameter (S_Addr, S_Param)	Contr → Slave[x]	O	M	M	M	M
6	Status, S_Param = Read_Parameter (S_Addr)	Pa[x] → Controller	O	M	O	M	M
7	Status = Store_Actual_Parameters ()	Pa → Pp	O	M	M	M	M
8	Status = Set_Permanent_Configuration (S_Addr,S_ Config)	Contr → PCD[x]	O	M	O	M	M
9	Status, S_Config = Get_Permanent_Configuration (S_Addr)	PCD[x] → Contr	O	M	O	M	M
10	Status = Store_Actual_Configuration ()	CDI → PCD	M	M	M	M	M
11	Status, S_Config = Read_Actual_Configuration (S_Addr)	CDI[x] → Controller	O	M	O	M	M
12	Status = Set_LPS (S_List)	Controller → LPS	O	M	O	M	M
13	Status, S_List = Get_LPS ()	LPS → Controller	O	M	O	M	M
14	Status, S_List = Get_LAS ()	LAS → Controller	O	M	O	M	M
15	Status, S_List = Get_LDS ()	LDS → Controller	O	M	O	M	M
16.0	Status, Flags = Get_Flags ()	Flags → Controller	O	M	O	M	M
16.1	Status, Flag = Get_Flag_Config_OK ()	Flag → Controller	M	M	M	M	M
16.2	Status, Flag = Get_Flag_LDS.0 ()	Flag → Controller	O	M	O	M	M
16.3	Status, Flag = Get_Flag_Auto_Address_Assign ()	Flag → Controller	O	M	O	M	M
16.4	Status, Flag = Get_Flag_Auto_Prog_Available ()	Flag → Controller	O	M	O	M	M
16.5	Status, Flag = Get_Flag_Configuration_Active ()	Flag → Controller	O	M	O	M	M
16.6	Status, Flag = Get_Flag_Normal_Operation_ Active ()	Flag → Controller	O	M	O	M	M
16.7	Status, Flag = Get_Flag_APF ()	Flag → Controller	O	M	O	M	M
16.8	Status, Flag = Get_Flag_Offline_Ready ()	Flag → Controller	O	M	O	M	M
16.9	Status, Flag = Get_Flag_Periphery_OK ()	Flag → Controller	O	O	O	M	M
17	Status = Set_Operation_Mode (Mode)	Contr → OM-Flag	M	M	M	M	M
18	Status = Set_Offline_Mode (Mode)	Contr → Offline-Flag	O	M	O	M	M
19	Status = Activate_Data_Exchange (Mode)	Contr → DE-Flag	O	O	O	O	O
20	Status = Change_Slave_Address (S_Addr1, S_Addr2)	Controller → Slave	O	M	O	M	M
21.1	Status = Set_Auto_Address_Enable (Mode)	Controller → AE-Bit	O	O	O	O	O
21.2	Mode = Get_Auto_Address_Enable ()	AE-Bit → Controller	O	O	O	O	O
22.1	Status, Resp = Cmd_Reset_AS-i_Slave (S_Addr, RESET)	Controller → Slave	O	O	O	O	O
22.2	Status, Resp = Cmd_Read_IO_Configuration (S_Addr, CONF)	Controller → Slave	O	O	O	O	O
22.3	Status, Resp = Cmd_Read_Identification_Code (S_Addr, IDCOD)	Controller → Slave	O	O	O	O	O
22.4	Status, Resp = Cmd_Read_Status (S_Addr, STAT)	Controller → Slave	O	O	O	O	O
22.5	Status, Resp = Cmd_Read_Reset_Status (S_Addr, STATRES)	Controller → Slave	O	O	O	F	F
22.6	Status, Resp = Cmd_Read_Ext_ID-Code_1 (S_Addr, IDCOD1)	Controller → Slave	O	O	O	O	O
22.7	Status, Resp = Cmd_Read_Ext_ID-Code_2 (S_Addr, IDCOD2)	Controller → Slave	O	O	O	O	O
23	Status, S_List = Get_ LPF()	LPF → Controller	O	O	O	M	M
24	Status = Write_Extended_ID-Code_1(S_Ext_ID-Code_1)	Contr → Slave 0	O	O	O	M	M
25	AImage, Status = Read_AIDI()	AIDI → Controller	O	O	O	M	M
26	Status = Write_AODI(AImage)	Controller → AODI	O	O	O	M	M
27	String, Status = Read_ParamStr(S_Addr)	ParamStr → Contr	O	O	O	O	M
28	Status = Write_ParamStr(S_Addr, String)	Contr → ParamStr	O	O	O	O	M
29	String, Status = Read_DiagStr(S_Addr)	DiagStr → Contr	O	O	O	O	M
30	String, Status = Read_IdentStr(S_Addr)	IdentStr → Contr	O	O	O	O	M

B	Function at slave interface		Profile				
			M0	M1	M2	M3	M4
1	Support of extended address mode		F	F	F	M	M
2	Support of Combined transaction type 1 integrated (S-7.3 only)		O	O	O	M*	M
3	Full support of Combined transaction type 1 integrated		O	O	O	M*	M
4	Support of Combined transaction type 2 integrated		O	O	O	O	M
5	Support of Combined transaction type 3 integrated		O	O	O	O	M
6	Support of Combined transaction type 4 integrated		O	O	O	O	M
7	Support of Combined transaction type 5 integrated		O	O	O	O	M
M: mandatory. O: Optional. F: Forbidden.							

NOTE 1 The functions 22.1 to 22.7 make use of the execution control function "Execute_Command (Addr, Info)".

NOTE 2 M*: Integrated support of combined transaction type 1 is optional if every controller which can be used with this particular AS-i master is not capable of using COMBINED transaction type 1 data because of technical and performance reasons.

B.3.4 Integrated support of combined transactions

The integrated support of combined transactions shall be according to the specification given in 5.7. For slaves that support combined transactions type 1 and/or type 2 to 5, the master generates a separate analogue input and/or analogue output data image (AIDI and/or AODI). The corresponding bits in the input/output data image (IDI/ODI) shall not be used in this case.

A master with integrated support of combined transactions type 1 and/or type 2 to 5 shall allow for a maximum of 124 analogue input and 124 analogue output channels. (this corresponds to 31 analogue slaves with four channels each).

B.3.5 AS-i Protocol implementation conformance statement (PICS)

For all masters delivered to the customer a Protocol implementation conformance statement (PICS) according to the profile assignment shall be included in the product documentation. The PICS describes the mapping between the functions defined in this standard and the functions available at the controller or user interface.

B.3.6 Stated AS-i cycle time

The declaration of the "stated AS-i-cycle time" is part of the PICS and shall be included in the product documentation. It shall allow the calculation of the cycle time depending on the number of activated slaves.

EXAMPLE:
AS-i cycle time: Up to 19 activated slaves: 3 ms
20 to 31 activated slaves: (1 + number of activated slaves)* 154 µs.

NOTE When a pair of A and B slaves on the same address is activated, they are counted like one single slave in this formula. Pairs of A- and B-slaves are accessed in every second AS-i-cycle.

B.3.7 Time for transferring analogue data

The documentation shall specify the maximum time of a complete transfer of an analogue value according to the combined transaction type 1 through 5 under worst case conditions.

B.3.8 Compatibility with synchronous data IO mode

The documentation shall state the compatibility of the master with Synchronous Data IO Mode.

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