IEC/TS 61800-8

Edition 1.0 2010-05

TECHNICAL SPECIFICATION

colour inside

Adjustable speed electrical power drive systems – Part 8: Specification of voltage on the power interface

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Adjustable speed electrical power drive systems – Part 8: Specification of voltage on the power interface

INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRICE CODE XB

ICS 29.160.30; 29.200

ISBN 978-2-88910-991-3

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

ADJUSTABLE SPEED ELECTRICAL POWER DRIVE SYSTEMS –

Part 8: Specification of voltage on the power interface

FOREWORD

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Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 61800-8, is a technical specification, which has been prepared by subcommittee SC 22G: Adjustable speed electric drive systems incorporating semiconductor power converters, of IEC technical committee TC 22: Power electronic systems and equipment.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
22G/207/DTS	22G/215/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts of IEC 61800 series, under the general title *Adjustable speed electrical power drive systems* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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ADJUSTABLE SPEED ELECTRICAL POWER DRIVE SYSTEMS –

Part 8: Specification of voltage on the power interface

1 Scope

This part of IEC 61800 gives the guidelines for the determination of voltage on the power interface of power drive systems (PDS's).

NOTE The power interface, as defined in the IEC 61800 series, is the electrical connection used for the transmission of the electrical power between the converter and the motor(s) of the PDS.

The guidelines are established for the determination of the phase to phase voltages and the phase to ground voltages at the converter and at the motor terminals.

These guidelines are limited in the first issue of this document to the following topologies with three phase output

- indirect converter of the voltage source type, with single phase diode rectifier as line side converter;
- indirect converter of the voltage source type, with three phase diode rectifier as line side converter;
- indirect converter of the voltage source type, with three phase active line side converter.

All specified inverters in this issue are of the pulse width modulation type, where the individual output voltage pulses are varied according to the actual demand of voltage versus time integral.

Other topologies are excluded of the scope of this International Specification.

Safety aspects are excluded from this Specification and are stated in IEC 61800-5 series. EMC aspects are excluded from this Specification and are stated in IEC 61800-3.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61000-2-4*, Electromagnetic compatibility (EMC) – Part 2-4: Environment – Compatibility levels in industrial plants for low-frequency conducted disturbances*

3 Overview and terms and definitions

3.1 Overview of the system

A power drive system (PDS) consists of a motor and a complete drive module (CDM). It does not include the equipment driven by the motor. The CDM consists of a basic drive module (BDM) and its possible extensions such as the feeding section or some auxiliaries (e.g. ventilation). The BDM contains converter, control and self-protection functions. Figure 1 shows the boundary between the PDS and the rest of the installation and/or manufacturing process. If the PDS has its own dedicated transformer, this transformer is included as a part of the CDM.

For this document the following agreement for all symbols is set, that:

– the index "head" means the peak value and
– the index "star" means bipolar value.

For a given drive topology, the voltage waveform patterns between the later defined sections are in principal constant as shape (including peak values), while their amplitudes depend on the suited operating voltages, assumed as reference values in each section.

Depending on the considered section interface and on the nature of the examined voltages (differential or common mode quantities), the reference voltages between sections are average DC or RMS fundamental AC quantities.

The actual voltage values shown between sections in the differential mode model and in the common mode model are evaluated as peak values: they are obtained starting from the corresponding reference values, multiplied by suited factors including the effect of the overvoltage phenomena.

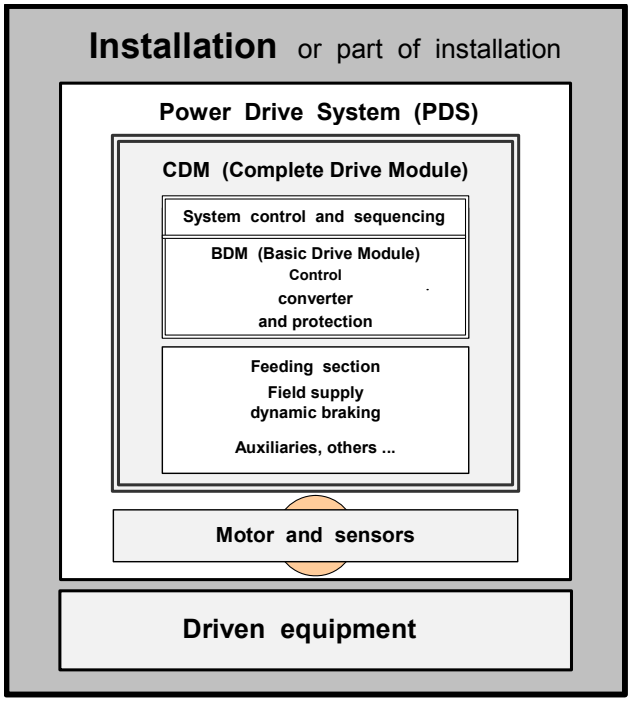


Figure 1 – Definition of the installation and its content

3.2 Terms and definitions

For the purposes of this part of the document, the following terms and definitions apply.

3.2.1
power interface
connections needed for the distribution of electrical power within the PDS

[IEC 61800-3:2004, 3.3.11]

3.2.2
two-port network
two-port network (or four-terminal network, or quadripole) is an electrical circuit or device with two pairs of terminals

3.2.3
converter reference point
NP
NP is the reference point of the converter (V_{D+} + V_{D-}) / 2. The converter reference point can be dedicated for the different topologies. The voltage from NP to ground is generally a common mode voltage

3.2.4
DC link
power DC circuit linking the input converter and the output converter of an indirect converter, consisting of capacitors and/or reactors to reduce DC voltage and/or DC current ripple

3.2.5
DC link voltages
V_d, V_{d+}, V_{d-}
DC link voltage of the converter section. V_{d+} means the positive potential; V_{d-} means the negative potential

3.2.6
f_0
filter resonance frequency

3.2.7
f_1
fundamental frequency of the inverter output voltage

3.2.8
f_P
pulse frequency of the phase

3.2.9
f_S
fundamental frequency of the supply voltage system

3.2.10
f_{sw}
switching frequency of each semiconductor active device

3.2.11
ideal ground
ideal ground is the earth reference point of the installation

3.2.12
$k_{C\mu}$
amplifying factors of the related section in the common mode model (peak values)

3.2.13
k_{Dv}
amplifying factors of the related sections in the differential mode model (peak values)

3.2.14
number of levels N
number of levels N is equal to the number of possible voltages of the output phase to NP-Potential

3.2.15
n_{dcmult}
number of DC links per phase of the multi DC link inverter topology

3.2.16
system star point
SP
SP is the reference point of the inverter output. The system star point can be dedicated at different system points. It is used to define the common mode voltage of a three phase system against ideal ground

3.2.17
rise time
t_r
rise time of the voltage is defined between 10 % to 90 % of the voltage transient peak equal to t_{90}-t_{10} (see Figure 2)

3.2.18
overshoot voltage
V_B
amount of voltage that exceeds the steady state value of a voltage step "V_{step}" (see Figure 2)

3.2.19
grounding potential
V_{Gi}
reference potential to ground at the individual section i sometimes the phrase "earth potential" or "earthing" may be used in the same content.

3.2.20
V_{PP}
phase to phase voltage

3.2.21
V_{PNP}
phase to NP voltage at the inverter output

3.2.22
V_{PSP}
phase to star point voltage at the inverter output

3.2.23
$V_{PG, motor}$
phase to ground voltage at the motor terminals.

3.2.24
$V_{PP, motor}$
phase to phase voltage at the motor terminals

3.2.25
$\hat{V}_{PP}$
peak value of the phase to phase voltage:
$\hat{V}_{PP} = V_{step} + V_B$ (example for the two level case)

3.2.26
$\hat{V}_{PP}^*$
peak value between two bipolar peak voltages

3.2.27
$\hat{V}_{PP\_fp}^*$
peak value of the phase to phase voltage including two times the over voltage spike

3.2.28
V_S
phase to phase supply voltage (feeding voltage) of the converter. This voltage is used in this document to normalize the peak voltages and the DC link voltage as "per unit values" and includes all tolerances according to IEC 61000-2-4

3.2.29
V_{SN}
nominal phase to phase supply voltage (feeding voltage) of the converter, the secondary voltage of the input transformer without tolerances

3.2.30
V_{step}
difference between steady state voltage values before and after a switching transition (see Figure 2)

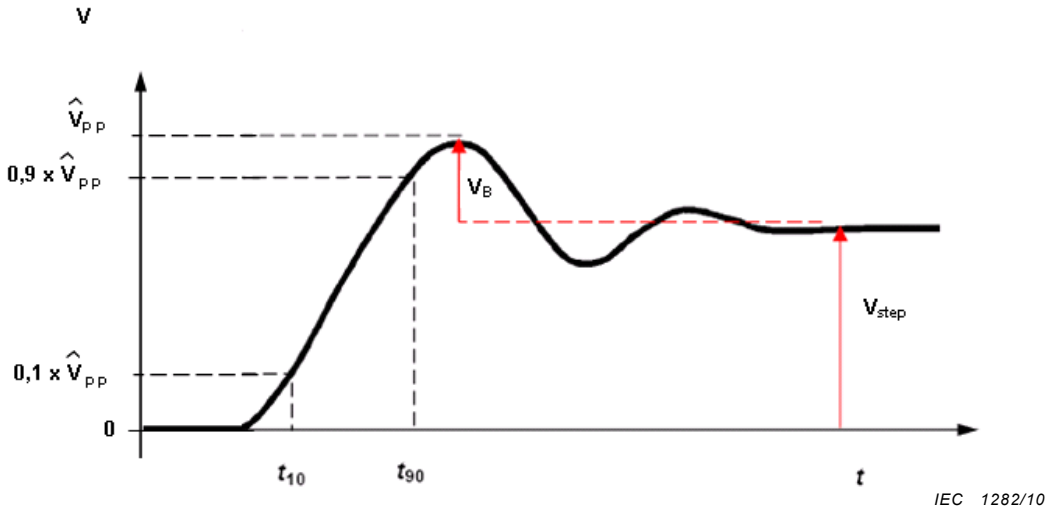


Figure 2 – Voltage impulse wave shape parameters in case of the two level inverter where rise time $t_{ri} = t_{90} - t_{10}$

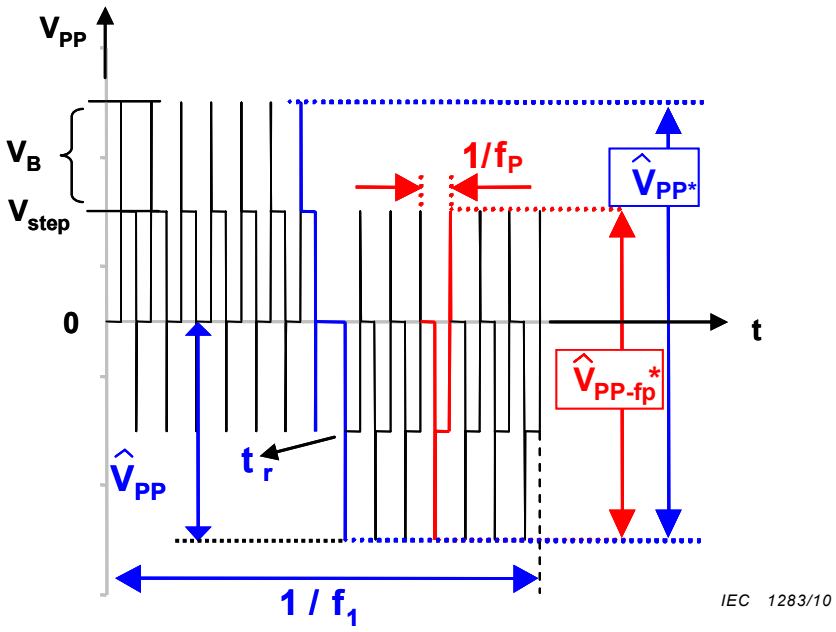


Figure 3 – Example of typical voltage curves and parameters of a two level inverter versus time at the motor terminals (phase to phase voltage)

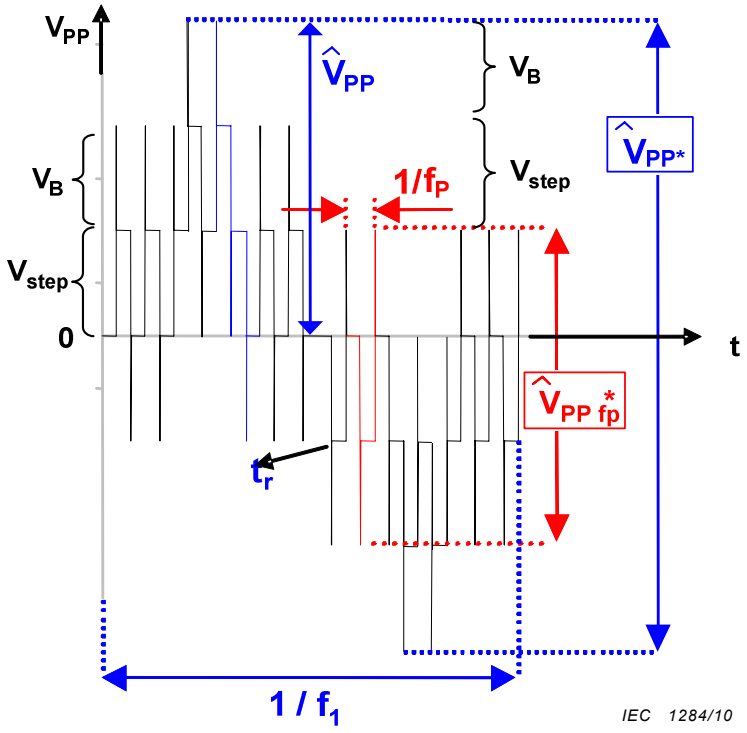


Figure 4 – Example of typical voltage curves and parameters of a three level inverter versus time at the motor terminals (phase to phase voltage)

3.2.31
V_{step_PP}
V_{step} of the phase to phase voltage V_{PP}

3.2.32
V_{step_PNP}
V_{step} of the phase to NP voltage V_{PNP}

3.2.33
V_{step_PSP}
V_{step} of the phase to SP voltage V_{PSP}

3.2.34
V_{step_Gi}
V_{step} of the common mode voltage V_{Gi}

4 System approach

4.1 General

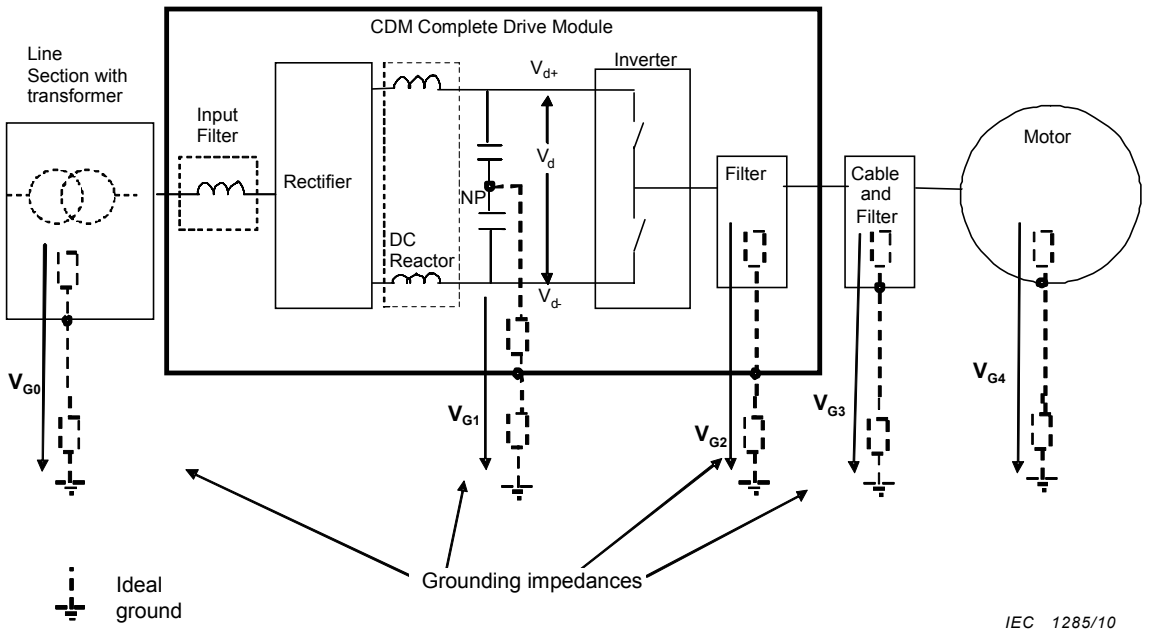


Figure 5 – Voltage source inverter (VSI) drive system with motor

The voltage source type drive system (see Figure 5) essentially consists of the following elements: line section, line side filter (if needed), line-side rectifier, DC reactor (if needed), DC capacitor bank in the DC link, self commutated motor-side converter output filter (if needed), cable system between converter and motor and finally a motor.

4.2 High frequency grounding performance and topology

The PE connection using cables belongs to the so called low frequency based grounding. To specify the dynamic voltage behaviour in the system approach, the high frequency grounding performance and topology is of interest.

The grounding potentials V_{G0} to V_{G4} of the different sections in a real installation are shown in Figure 5. They may be different as far as the grounding impedances are different and they are expected to be high frequency based potentials (if earthing wiring is of poor performance), although they might be of the same value in respect to low frequency based grounding.

– Single point grounding topology provides poor high frequency grounding performance. The high frequency based grounding potentials V_{G0} to V_{G4} may contain additional parasitic voltage fractions.

– Multi point or mesh type grounding topology provides excellent high frequency grounding performance. The high frequency based grounding potentials V_{G0} to V_{G4} will not contain additional parasitic voltage fractions.

4.3 Two-port approach

For the description of the resulting voltage waveforms at the motor terminals the two-port approach is of advantage.

There are basically two kinds of two-port elements which allow separating the system into two superposing parts:

– The amplifying elements in the differential mode model
– The adding elements in the common mode model

4.3.1 Amplifying element

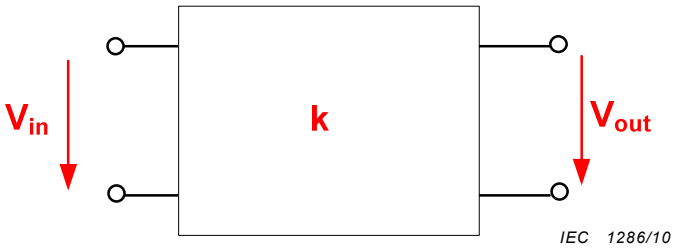


Figure 6 – Amplifying two-port element

In Figure 6, an amplifying element is shown. In this case, the output voltage of the two port can be calculated as follows:

$$V_{out} = k \times V_{in} \tag{1}$$

4.3.2 Adding element

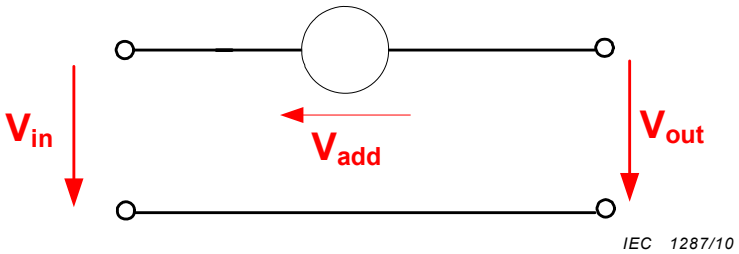


Figure 7 – Adding two-port element

In case of adding elements according to Figure 7, the output voltage of the two-port can be calculated as:

$$V_{out} = V_{add} + V_{in} \tag{2}$$

The relations per element between output voltages V_{out} and input voltages V_{in} in main parameters of chapter 4 like peak voltages, rise times, will lead to an approach for the behaviour of the whole network of line section, converter input, converter output, output filter, cabling, motor input. Grounding conditions may affect or distort the voltage relations and will be covered as a horizontal item of the different grounding potentials.

4.4 Differential mode and common mode systems

4.4.1 General

In signal theory, it is a widely used procedure to separate an existing system into a common mode and a differential mode system. In the differential mode system, all signals that occur between the conductors are included. In the common mode system, all signals that occur in all conductors identically and refer to ground are included.

In a PDS, this separation can be shown at the example of an inverter output section (see Figure 8):

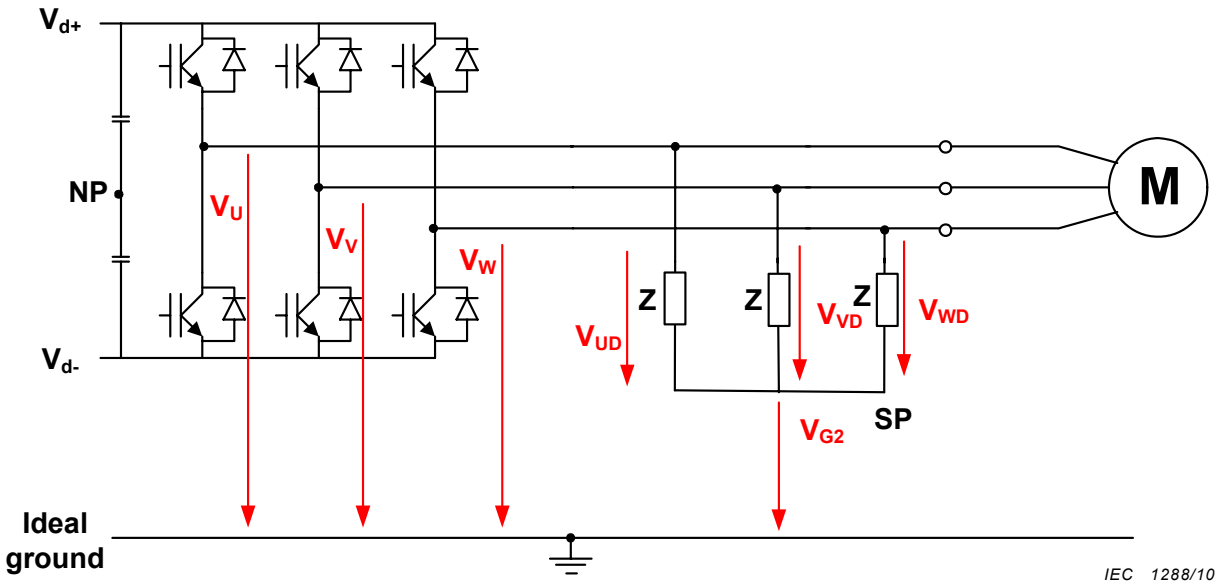


Figure 8 – Differential mode and common mode voltage system

The output voltage of the inverter (V_U, V_V, V_W) can be divided into the differential mode (also known as symmetrical) voltage system (V_{UD}, V_{VD}, V_{WD}) and the common mode (also known as asymmetrical) voltage system (V_{G2}).

The differential mode voltage expresses voltages between the three output phases. For each phase, it can be calculated as the difference of the inverter output voltage and the common mode voltage. This is e.g. for phase U:

$$V_{UD} = V_U - V_{G2} \tag{3}$$

A PDS usually is a symmetrical system, which means that the amplitudes of all AC differential mode voltages (e.g. mains voltage, inverter output voltage) are identical in all phases and the voltage vectors have a phase shift of 120° towards each other (see Figure 9).

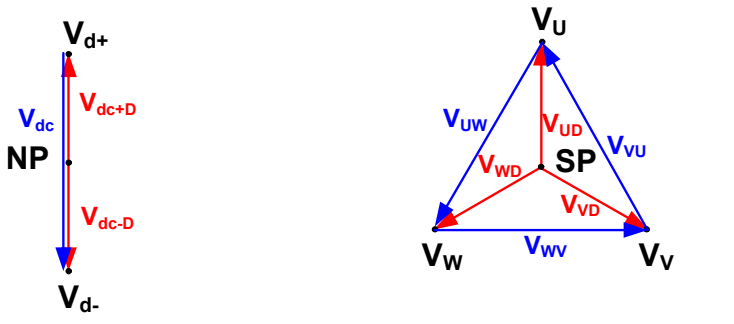


Figure 9 – Voltages in the differential mode system

The DC differential mode voltage is referred to the neutral point of the DC link and the voltages (V_{dc+D} , V_{dc-D}) show an angle of 180°. Therefore, the amplitude of the DC differential mode voltage is always 50 % of the total DC link voltage from positive to negative rail.

The common mode voltage expresses the voltage from an ideal star point of the three output phases to the ideal ground potential. It can be calculated as follows:

$$V_{G2} = \frac{V_U + V_V + V_W}{3} \tag{4}$$

For both differential mode and common mode system, an equivalent circuit diagram can be generated, using the explained two-port elements.

4.4.2 Differential mode system

The differential mode block diagram is shown in Figure 10:

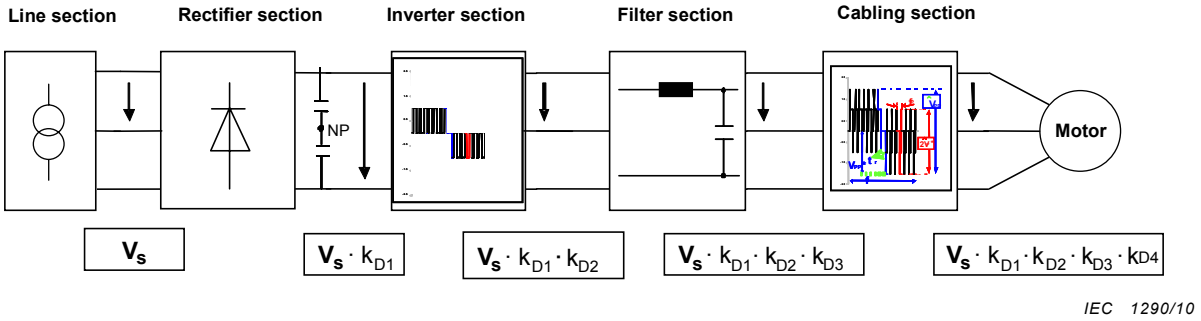


Figure 10 – Block diagram of two-port elements to achieve the motor terminal voltage in the differential mode model

The maximum phase to phase voltage at the motor input can then be calculated as:

$$\hat{V}_{PP,Motor} = V_S \cdot \prod_{i=1}^{4} k_{Di} \tag{5}$$

In the following Figure 11, an example for a practical installation is given:

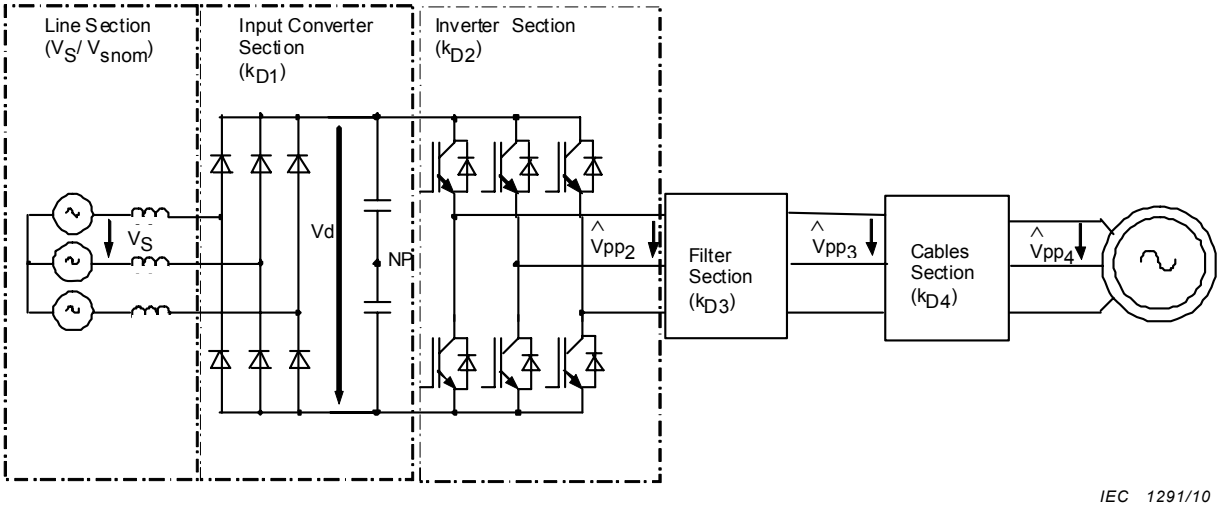


Figure 11 – Equivalent circuit diagram for calculation of the differential mode voltage

In a step by step calculation, the voltages can be calculated as:

Line Section: $$V_S \tag{6}$$

Input Converter Section: $$V_d = k_{D1} \cdot V_S \tag{7}$$

Inverter Section: $$\hat{V}_{PP2} = k_{D2} \cdot V_d \tag{8}$$

Filter Section: $$\hat{V}_{PP3} = k_{D3} \cdot \hat{V}_{PP2} \tag{9}$$

Cabling Section: $$\hat{V}_{PP4} = k_{D4} \cdot \hat{V}_{PP3} = \hat{V}_{PP,Motor} \tag{10}$$

4.4.3 Common mode system

For the common mode system, the block diagram is shown in Figure 12:

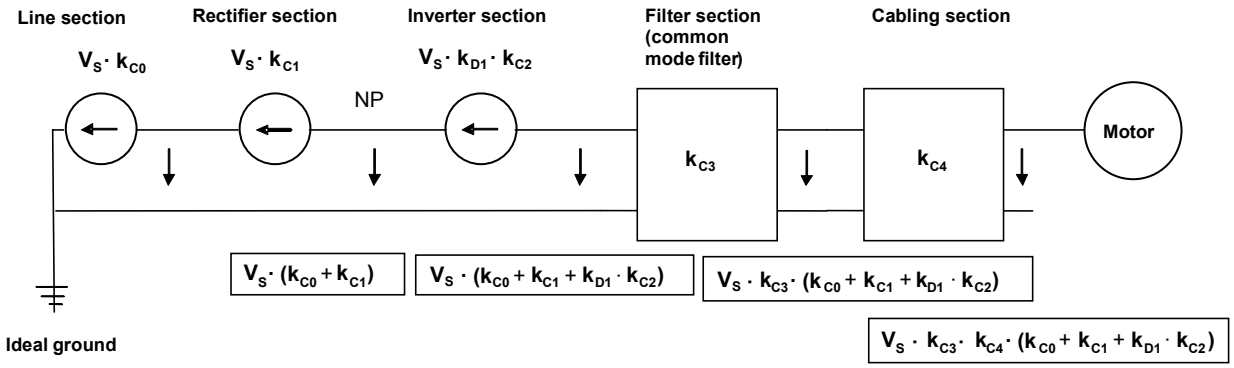


Figure 12 – Block diagram of two-port elements to achieve the motor terminal voltage in the common mode model

In the following Figure 13 an example for a practical installation is shown:

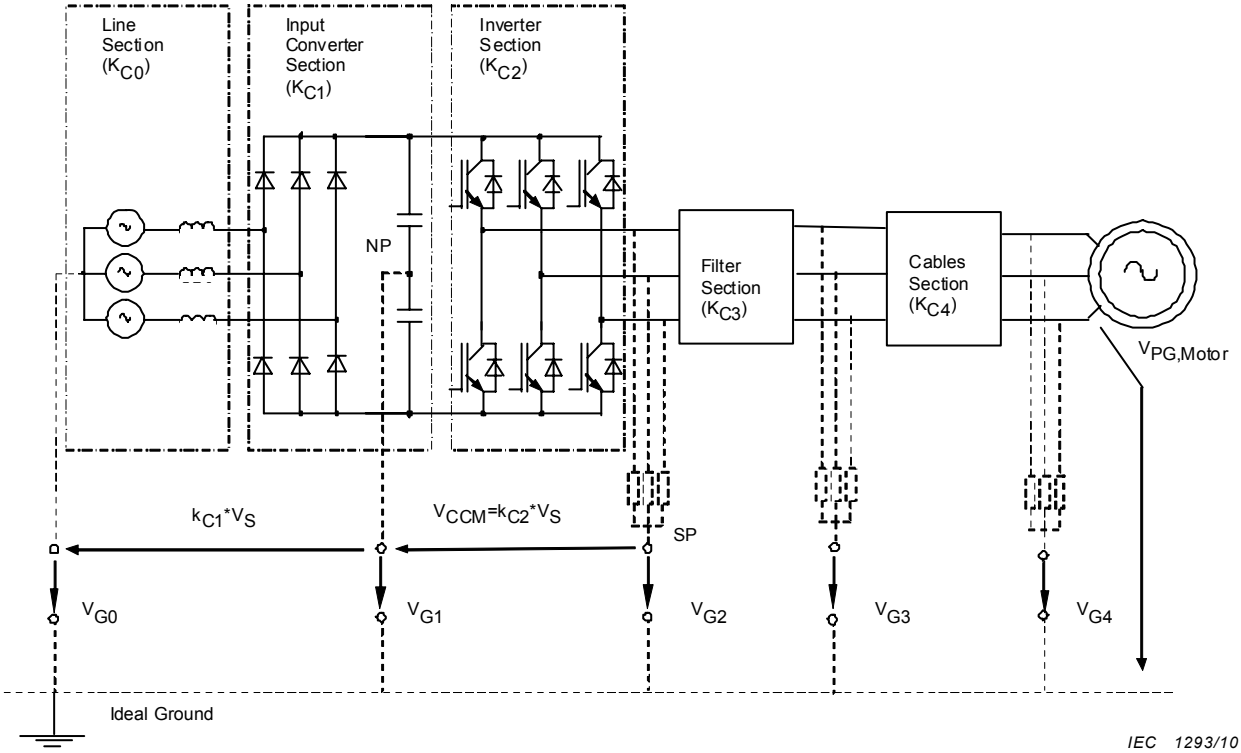


Figure 13 – Equivalent circuit diagram for calculation of the common mode voltage

In a step by step calculation the common mode voltages can be derived as:

Line Section:
$$\hat{V}_{G0} = k_{C0} \cdot V_S \tag{11}$$

Input Converter Section:
$$\hat{\boldsymbol{V}}_{\boldsymbol{G}1} = \hat{\boldsymbol{V}}_{\boldsymbol{G}0} + \boldsymbol{k}_{\boldsymbol{C}1} \cdot \boldsymbol{V}_{\boldsymbol{S}} \tag{12}$$

$$= \left(\boldsymbol{k}_{\boldsymbol{C}0} + \boldsymbol{k}_{\boldsymbol{C}1}\right) \cdot \boldsymbol{V}_{\boldsymbol{S}}$$

Inverter Section:
$$\hat{\boldsymbol{V}}_{\boldsymbol{G}2} = \hat{\boldsymbol{V}}_{\boldsymbol{G}1} + \boldsymbol{k}_{\boldsymbol{C}2} \cdot \boldsymbol{k}_{\boldsymbol{D}1} \cdot \boldsymbol{V}_{\boldsymbol{S}} \tag{13}$$

$$= \left(\boldsymbol{k}_{\boldsymbol{C}0} + \boldsymbol{k}_{\boldsymbol{C}1} + \boldsymbol{k}_{\boldsymbol{C}2} \cdot \boldsymbol{k}_{\boldsymbol{D}1}\right) \cdot \boldsymbol{V}_{\boldsymbol{S}}$$

Filter Section:
$$\hat{\boldsymbol{V}}_{\boldsymbol{G}3} = \boldsymbol{k}_{\boldsymbol{C}3} \cdot \hat{\boldsymbol{V}}_{\boldsymbol{G}2} \tag{14}$$

$$= \boldsymbol{k}_{\boldsymbol{C}3} \cdot \left(\boldsymbol{k}_{\boldsymbol{C}0} + \boldsymbol{k}_{\boldsymbol{C}1} + \boldsymbol{k}_{\boldsymbol{C}2} \cdot \boldsymbol{k}_{\boldsymbol{D}1}\right) \cdot \boldsymbol{V}_{\boldsymbol{S}}$$

In Figure 12, a common mode filter type is shown that is connected to the ground potential. In some applications, common mode output filters are connected to the NP potential. In this case, the filter is only affecting the common mode voltage of the output inverter. Equation 14 has then to be modified to the following term:

$$\hat{\boldsymbol{V}}_{\boldsymbol{G}3} = \hat{\boldsymbol{V}}_{\boldsymbol{G}1} + \boldsymbol{k}_{\boldsymbol{C}3} \cdot \boldsymbol{k}_{\boldsymbol{C}2} \cdot \boldsymbol{k}_{\boldsymbol{D}1} \cdot \boldsymbol{V}_{\boldsymbol{S}} \tag{15}$$

$$= \left(\boldsymbol{k}_{\boldsymbol{C}0} + \boldsymbol{k}_{\boldsymbol{C}1} + \boldsymbol{k}_{\boldsymbol{C}3} \cdot \boldsymbol{k}_{\boldsymbol{C}2} \cdot \boldsymbol{k}_{\boldsymbol{D}1}\right) \cdot \boldsymbol{V}_{\boldsymbol{S}}$$

Cabling Section: $$\hat{V}_{G4} = k_{C4} \cdot \hat{V}_{G3} \quad (16)$$

The maximum phase to ground voltage on the motor terminals can be calculated as:

$$\hat{V}_{PG,Motor} = \frac{1}{\sqrt{3}} \hat{V}_{PP,Motor} + \hat{V}_{G4} = \frac{1}{\sqrt{3}} V_S \cdot \prod_{i=1}^{4} k_{Di} + V_S \cdot (\sum_{i=0}^{2} k_{Ci}) \cdot \prod_{i=3}^{4} k_{Ci} \quad \textbf{(17)}$$

The amplification factors k_{D1} ... k_{D4}, k_{C3} ... k_{C4} and common mode factors k_{C0} ... k_{C2} will be explained and determined in the following sections, depending on the PDS section topology.

5 Line section

5.1 General

Influence of the power supply systems is given in this section. The main different possible power supply systems (TN, TT, and IT systems) are described in Annex A, including grounding and influence.

For that Line section and the Input converter section of Clause 6, the TT power supply system is not separately considered, as it provides no different influence compared to the TN system.

5.2 TN-Type of power supply system

5.2.1 General

TN power supply systems have one point directly earthed, the exposed-conductive-parts of the installation being connected to that point by protective conductors. Three types of TN systems are considered according to the arrangement of neutral and protective conductors, as follows:

– TN-S system: in which throughout the system, a separate protective conductor is used;

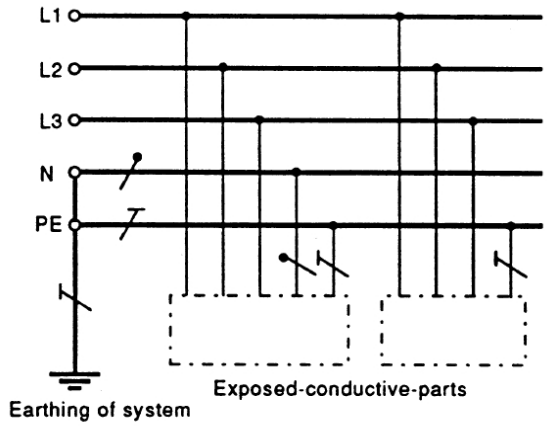
– TN-C-S system: in which neutral and protective functions are combined in a single conductor in a part of the system;

– TN-C system: in which neutral and protective functions are combined in a single conductor throughout the system.

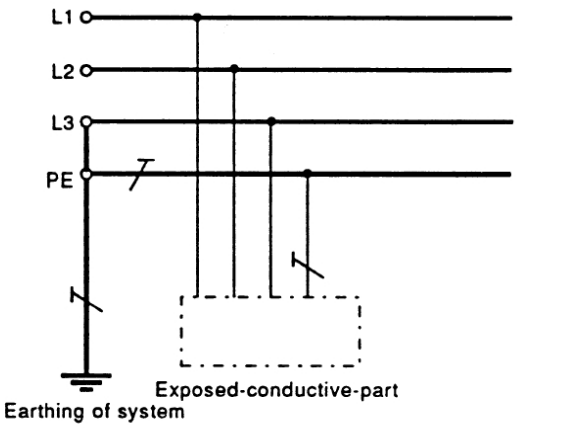
5.2.2 Star point grounding and corner grounding

In general one arbitrary point might be earthed in the mentioned supply systems. Resulting from this earthing point different common mode voltages occur. According to Figures 11 and 14 the common mode voltage will reach values between minimum and maximum:

- where minimum is defined in case of star point grounding with $k_{C0} = 0$
- where maximum is defined in case of corner grounding as $k_{C0} = V_S$ / SQR 3



Separate neutral and protective conductors throughout the system



Separate earthed phase conductor and protective conductors throughout the system

Figure 14 – TN-S power supply system
left: k_{C0} = 0, right: k_{C0} = 1/ SQR 3

5.3 IT-Type of power supply system

In case of IT-power supply system all conductors are insulated from the ground potential. This leads (see Figure 11) to an undefined value of V_{C0}. In practical cases the parasitic impedances are more or less symmetrical which leads to a value of k_{C0} = 0.

Deviations from this case may occur if one earth fault happens in such an installation. In such cases the value might reach k_{C0} = 1 / SQR 3.

5.4 Resulting amplification factors in the differential mode model of the line section

Table 1 – Amplification factors in the differential mode model of the line section

	TN-network	IT-network
V_S / V_{SN}	1	1

NOTE Under worst case conditions the line voltage tolerance has to be included in the V_s value

5.5 Resulting contribution of the line section in the common mode model

Table 2 – Factors in the common mode model of the line section

	TN-network	IT-network
k_{C0} central grounding system Potential related to nominal supply voltage	0 in case of star point grounding $\frac{1}{\sqrt{3}}$ in case of corner grounding	not defined, at least limited to $\frac{1}{\sqrt{3}}$

6 Input converter section

6.1 Analysis of voltages origins

The low frequency grounding potential of the inverter output terminals is determined by the DC link voltage (V_d) and the reference potential of the DC link voltage (V_{G1}) (see Figure 5.)

Grounding potential of the converter output terminals = $V_{G1} \pm V_d/2$ (18)

When the upper side switch of inverter is switched on, the grounding potential $V_{G1} + V_d/2$ appears at the output of the converter. And if the lower side switch of inverter is switched on, the grounding potential $V_{G1} - V_d/2$ appears at the output of the inverter.

6.1.1 The DC link voltage of converter section (V_d)

The DC link voltage is mainly determined by the type of rectifier and by the filtering effect of the impedance at supply line and/or DC line and the large DC capacitor. The DC voltage ripple is usually negligible.

The DC link voltage is affected by the following items;

– Type of rectifier (single phase diode, three phase diode, active converter);
– Type of inverter (single phase/three phase and with/without DC brake);
– Line side commutation impedance;
– Load

6.1.2 The reference potential of NP of the DC link voltage

The reference potential V_{G1} of the DC link voltage is usually very close to the grounding potential, if a TN or IT line side (see Clause 5) grounding system is applied or the neutral point of the DC capacitor is grounded by some means. Even if a non-grounded (IT) supply system is applied, the average value of V_{G1} may remain close to grounding potential. But it is also influenced by the grounding impedance of output filter, cable and motor.

The following items may affect the reference potential V_{G1} of the DC link voltage:

– Grounding system of line section;
– Arrangement of input filter and DC reactor;
– Grounding system of converter;
– Grounding impedance of output filter and cable;
– Grounding impedance of motor;
– Switching condition of converter.

6.2 Indirect converter of the voltage source type, with single phase diode rectifier as line side converter

6.2.1 Voltage source inverter (VSI) with single phase diode rectifier

6.2.1.1 General

The single phase diode rectifier systems are categorised in the following three supply cases, when line side grounding system is taken into consideration.

Figure 15, Figure 16 and Figure 17 show the configuration of voltage source inverters supplied by L and N for a TN or TT system, supplied by L1 and L2 for TN or TT system and supplied by L1 and L2 for IT system, respectively.

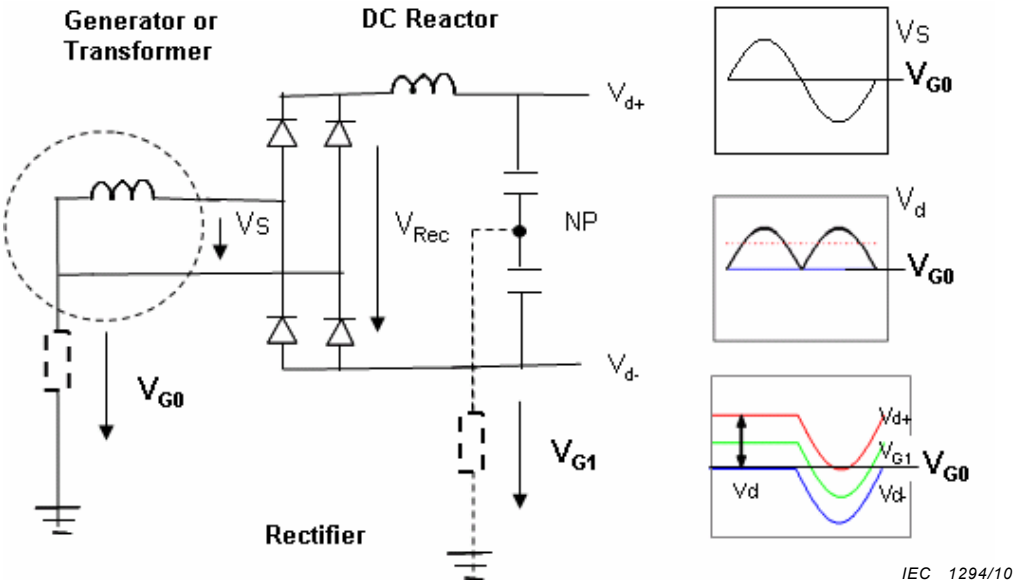


Figure 15 – Typical configuration of a voltage source inverter with single phase diode rectifier supplied by L and N from a TN or TT supply system

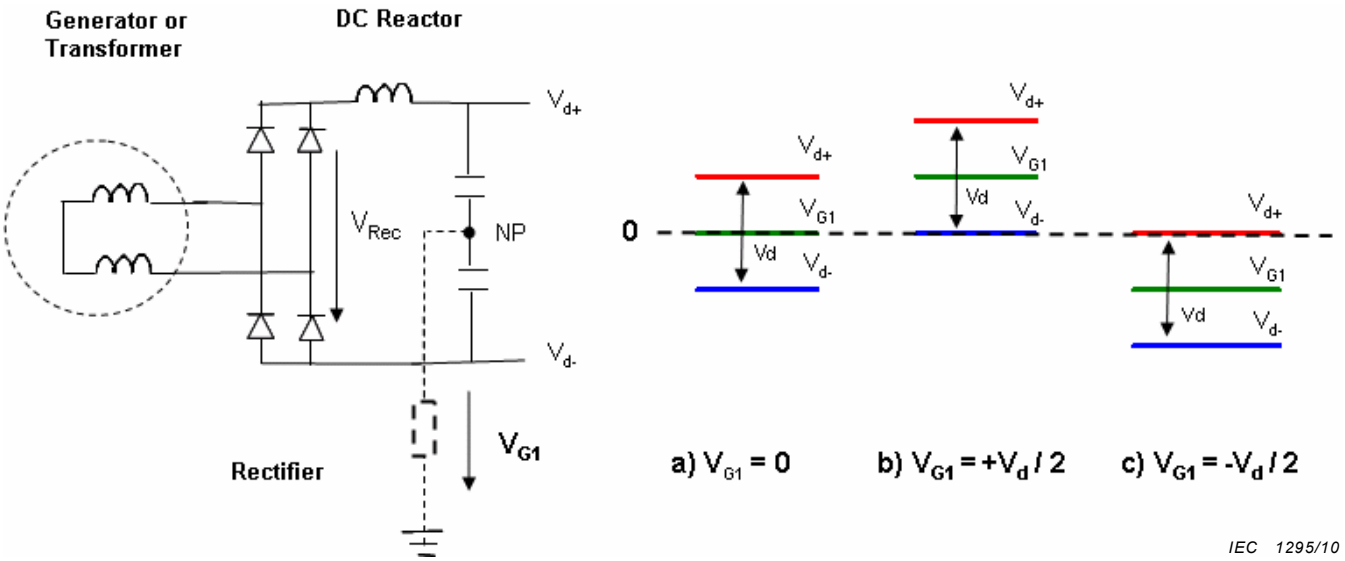


Figure 16 – Typical configuration of a voltage source inverter with single phase diode rectifier supplied by L1 and L2 from an IT supply system

The average values of V_{G1}, V_{d+} and V_{d-} are usually V_{G0}, V_{G0} +V_d/2 and V_{G0} –V_d/2 respectively as shown in Figure 16. But in this case, DC link potential V_{G1} is generally affected by the switching condition of inverter and the grounding condition of the converter, the output filter and the motor.

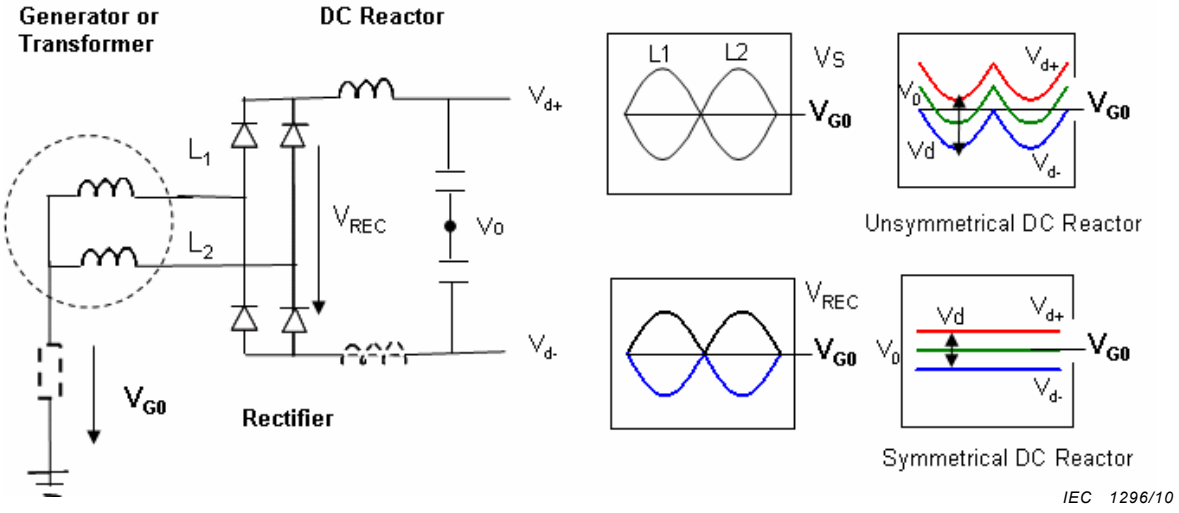


Figure 17 – Typical configuration of a voltage source inverter with single phase diode rectifier supplied by L1 and L2 from a TN or TT supply system

V_{d+} and V_{d-} differ by the arrangement of DC link reactor. DC link reactor is usually installed only at positive side. In this case V_0, V_{d+} and V_{d-} are not constant but fluctuate as shown in Fig. 17. If DC link reactors are installed symmetrically in both side of DC link, V_{d+} and V_{d-} become constant as shown.

6.2.1.2 The DC link voltage

For all of three cases, the DC link voltage of single phase diode rectifier is calculated as follows, if the commutation impedance is neglected under no load condition.

$$V_d = \frac{1}{\pi} \cdot \int_0^{\pi} \sqrt{2} \times V_s \times \sin \omega t \times d\omega t = V_s \times \frac{2 \cdot \sqrt{2}}{\pi} = 0{,}9 \times V_s \qquad (19)$$

As shown in Fig.18, the peak DC voltage of single phase diode rectifier is theoretically 157 % at the no load condition of the converter without considering supply voltage variation. If supply voltage variation and DC braking operation are taken into consideration, the maximum DC voltage will be higher. The set point of the trigger point of the chopper is influencing that.

Sometimes a bleeder resistance (BR) might be used to reduce the peak DC voltage.

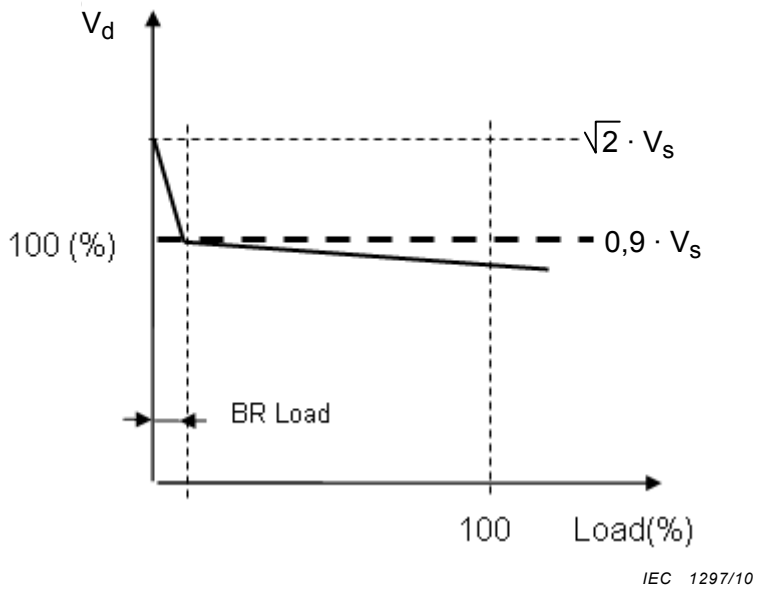


Figure 18 – Typical DC voltage V_d of single phase diode rectifier without breaking mode. BR is the bleeder resistor to discharge the capacitor

6.2.1.3 The grounding potential V_G

The typical voltage values, including the grounding potential VG, are shown in Figure 16 considering the three supply configurations (see 6.2.1).

Table 3 – Maximum values for the potentials of single phase supplied converters at no load conditions (without DC braking mode)

	Single phase diode input converter according to Figure 15 supplied by L and N from a TN or TT supply system	Single phase diode input converter according to Figure 16 supplied by L1 and L2 from an IT supply system	Single phase diode input converter according to Figure 17 supplied by L1 and L2 from a TN or TT supply system with unsymmetrical DC reactor	Single phase diode input converter according to Figure 17 supplied by L1 and L2 from a TN or TT supply system with symmetrical DC reactor
V_{d+} / V_S	$\sqrt{2}$	$V_{G0} / V_S + \sqrt{2}$	$\sqrt{2}$	$\sqrt{2} / 2$
V_{G1} / V_S	$V_{G0} / V_S - + \sqrt{2} / 2$	$V_{G0} / V_S - + \sqrt{2} / 2$	$+ - \sqrt{2} / 2$	V_{G0} / V_S
V_{d-} / V_S	$-\sqrt{2}$	$V_{G0} / V_S - \sqrt{2}$	$-\sqrt{2}$	$-\sqrt{2} / 2$
$(V_{d+} - V_{d-}) / V_S$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$

6.3 Indirect converter of the voltage source type, with three phase diode rectifier as line side converter

6.3.1 Voltage source inverter (VSI) with three phase diode rectifier

6.3.1.1 General

Figure 19 shows the typical configuration of a voltage source inverter.

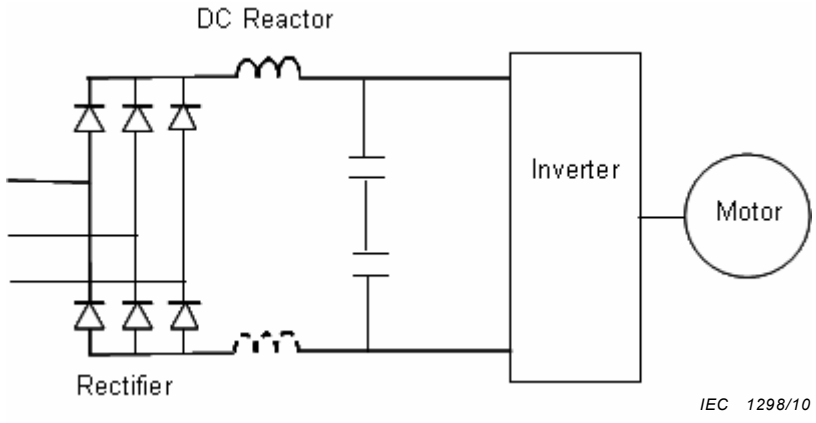


Figure 19 – Typical configuration of a voltage source inverter with three phase diode rectifier

The three phase diode rectifier systems are categorised in two cases, when line side grounding system (TN or TT System) or IT system is taking into consideration.

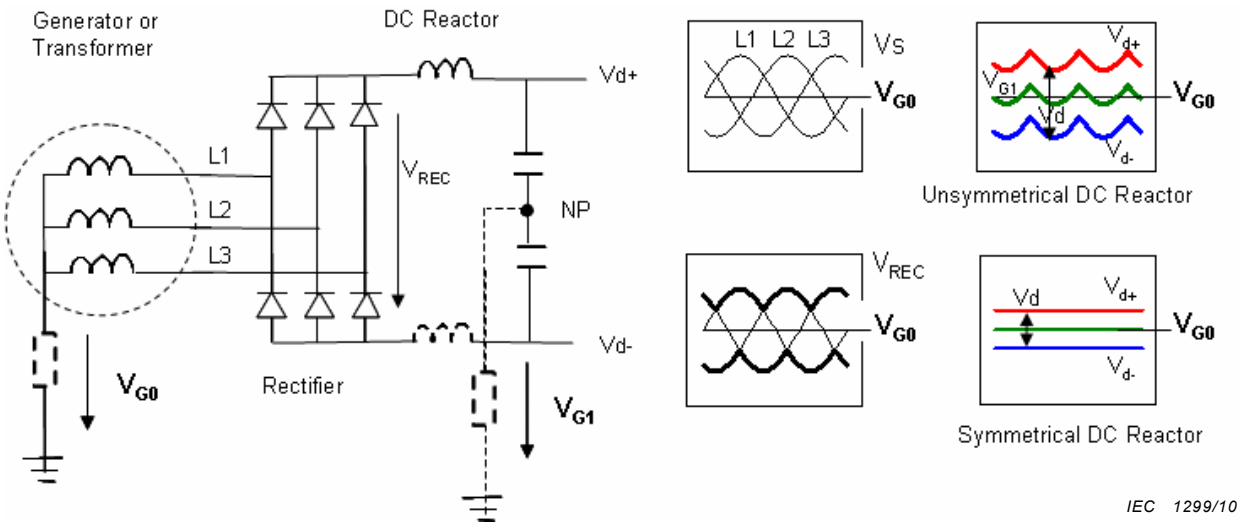


Figure 20 – Voltage source with three phase diode rectifier supplied by a TN or TT supply system

V_{G1}, V_{d+} and V_{d-} differ by the arrangement of DC link reactor. DC link reactor is usually installed only at positive side. In this case V_{G1}, V_{d+} and V_{d-} are not constant but fluctuate as shown in Fig. 20. If DC link reactors are installed symmetrically in both side of DC link, V_{G1}, V_{d+} and V_{d-} become constant as shown.

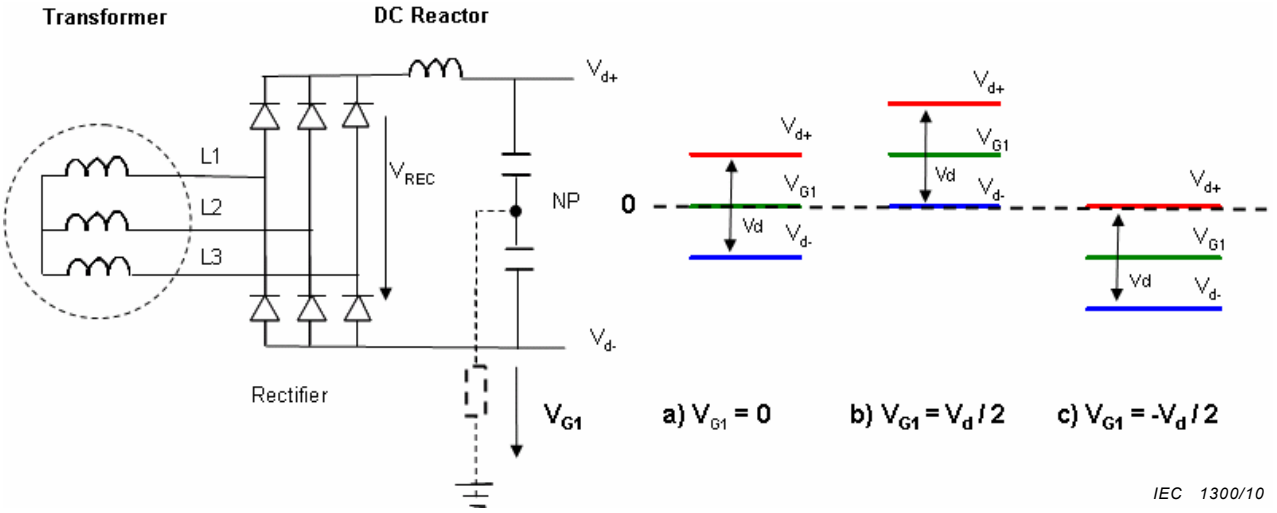


Figure 21 – Voltage source with three phase diode rectifier supplied by an IT supply system

The average values of V_{G1}, V_{d+} and V_{d-} are usually V_{G0}, (V_{G0} +V_d/2) and (V_{G0} –V_d/2) respectively as shown in Figure 21. But in this case, DC link potential V_{G1} is generally affected by the switching condition of inverter and the grounding condition of converter, output filter and motor. Without DC-reactor the Figure 21 remains the same.

In case of active switches in parallel to the rectifier diodes which are switched synchronous with line frequency, the behaviour remains the same.

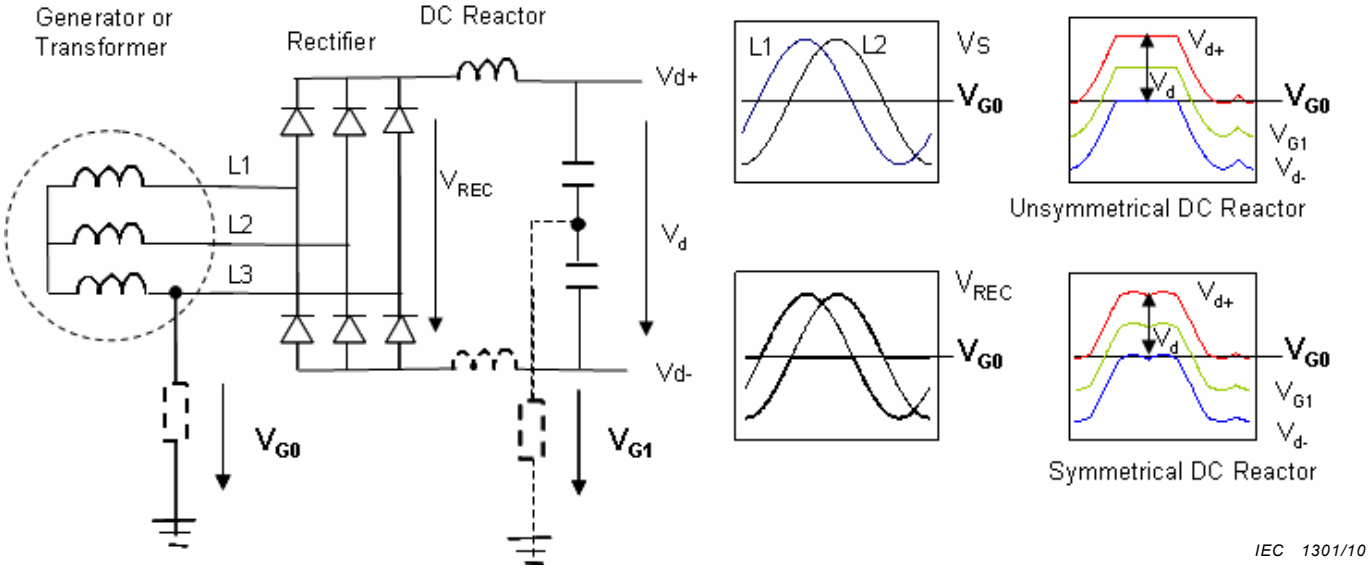


Figure 22 – Voltage source with three phase diode rectifier supplied from a delta grounded supply system

6.3.1.2 The DC link voltage

In both cases, the DC link voltage of three phase diode rectifier is calculated as follows, if the commutation impedance is neglected;

$$V_d = \frac{1}{12 \cdot \pi} \cdot \int_{\pi/2-\pi/6}^{\pi/2+\pi/6} \sqrt{2} \cdot V_s \cdot \sin \omega t \cdot d\omega t = \frac{6 \cdot \sqrt{2}}{\pi} V_s \cdot \sin(\pi/6) = 1{,}35 \cdot V_s \quad (20)$$

The peak DC voltage of three phase diode rectifier is 105 % at no load condition without considering supply voltage change. Figure 23 shows typical relation of the DC link voltage versus load of the three phase diode rectifier without braking mode. If supply voltage change and DC braking operation are taken into consideration, the maximum DC voltage could be higher.

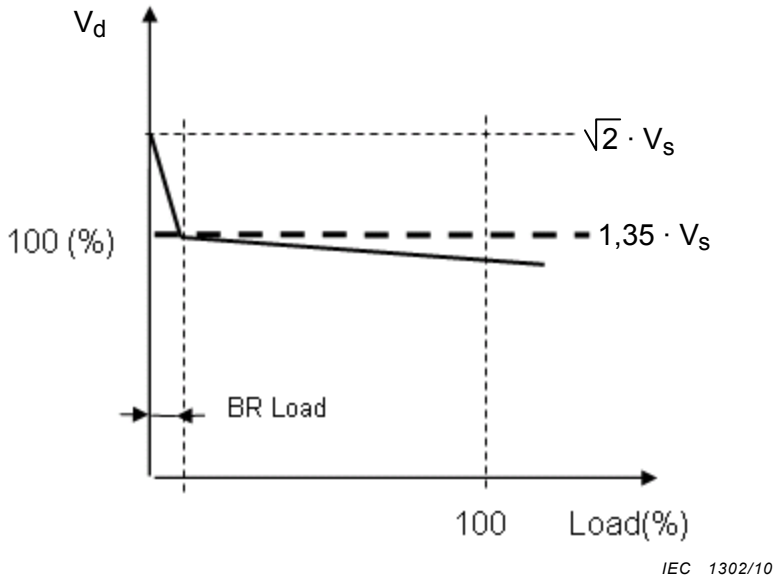


Figure 23 – Typical relation of the DC link voltage versus load of the three phase diode rectifier without braking mode

6.3.1.3 The grounding potential

The typical voltage values for the input rectifier section model, including grounding potential, are shown in Table 4.

Table 4 – Maximum values for the potentials of three phase supplied converters at no load conditions (without DC braking mode)

	Three phase diode input rectifier according to Figure 20 supplied from a TN or TT supply system with symmetrical dc reactor	Three phase diode rectifier according to Figure 21 supplied by L1, L2 and L3 from an IT supply system	Three phase diode rectifier according to Figure 22 supplied from a delta grounded supply system
V_{d+} / V_S	$\sqrt{2}$ * / 2	V_{G0} / V_S + $\sqrt{2}$	$\sqrt{2}$
V_{G1} / V_S	V_{G0} / V_S	V_{G0} / V_S +– $\sqrt{2}$ / 2	+– $\sqrt{2}$ / 2
V_{d-} / V_S	– $\sqrt{2}$ / 2	V_{G0} / V_S – $\sqrt{2}$	– $\sqrt{2}$
(V_{d+} – V_{d-}) / V_S	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$

6.4 Indirect converter of the voltage source type, with three phase active line side converter

6.4.1 Voltage source inverter (VSI) with three phase active infeed converter

6.4.1.1 General

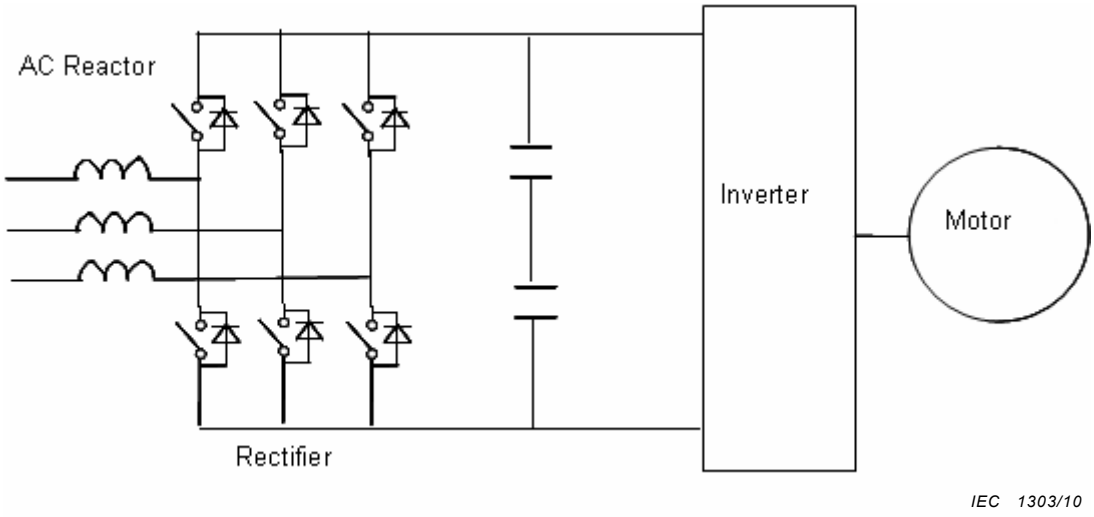


Figure 24 – Typical configuration of a VSI with three phase active infeed converter

The three phase active infeed converters are categorised in two cases, when line side grounding system (TN or TT System) or IT system is taking into consideration.

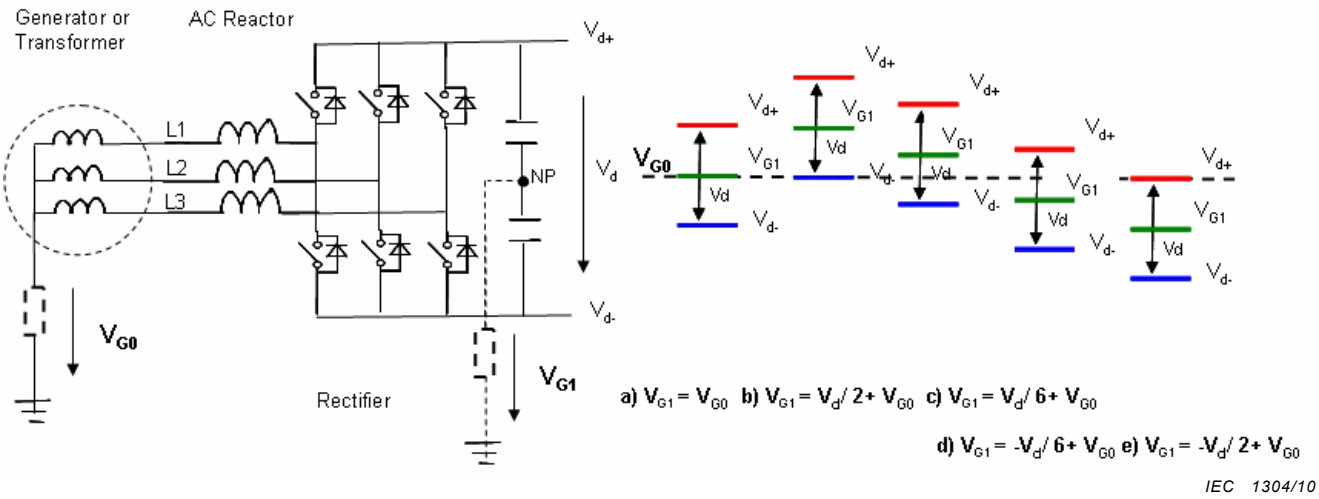


Figure 25 – Voltage source with three phase active infeed supplied by a TN or TT supply system

The average value of reference potential of DC link voltage (V_{G1}) for active infeed converters becomes almost equal to the earth potential. As V_d is larger than in case of a three phase diode rectifier, the grounding potentials, V_{d+} and V_{d-} will become higher than three phase diode rectifier (e.g. 10 % to 15 % from the peak value and 20 % to 25 % from the rated value). Assume that V_{G1} = 0 leads to the following approximation.

$$V_{d+} = (0.74 \sim 0.77) \cdot V_S = (0.82 \sim 0.85) \cdot V_{SN} \quad (21)$$

$$V_{d-} = -(0.74 \sim 0.77) \cdot V_S = -(0.82 \sim 0.85) \cdot V_{SN} \quad (22)$$

The instantaneous value of grounding potentials are affected by the switching mode of active line side converter. In Figure 25 the average grounding potential is shown in different cases which are related to the switching mode of active line side converter.

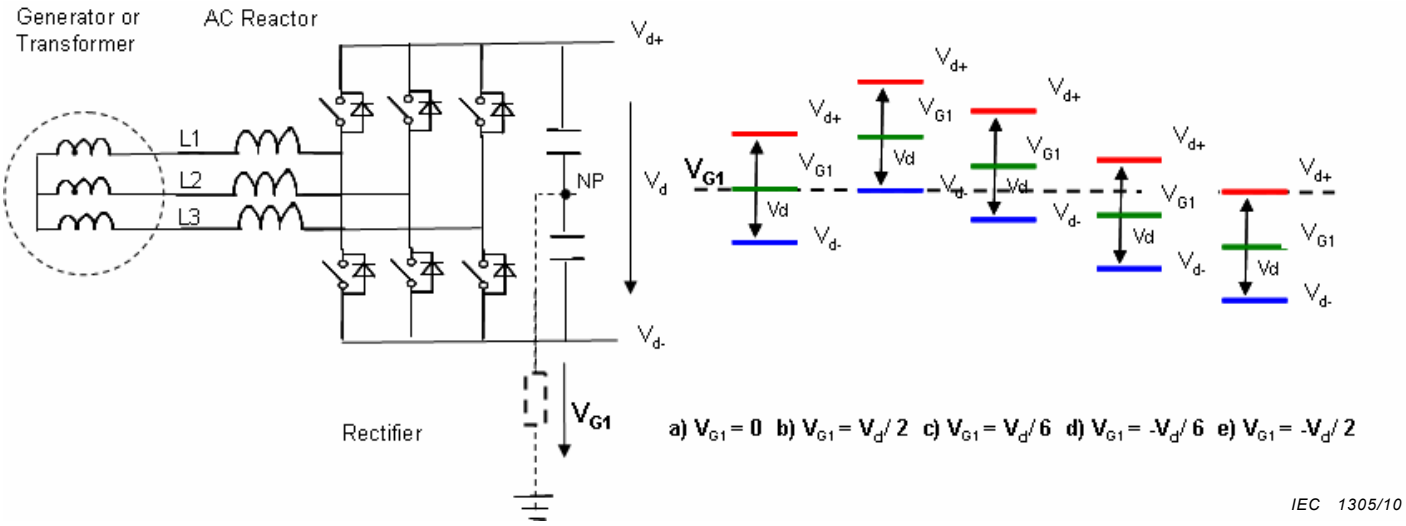


Figure 26 – Voltage source with three phase active infeed supplied by a IT supply system

The grounding potentials for IT system become basically same as shown in Fig. 26. They are also affected by the grounding system of converter, output filter and motor. The instantaneous value of grounding potentials vary as shown in Figure 26 in accordance with the switching mode of converter and inverter.

6.4.1.2 The DC link voltage

In general the DC link voltage of active line side converter is designed to be at least 5 % to 10 % higher than the peak phase to phase voltage to avoid the diode rectifier working in rectification mode.

$$V_d = (1.05 \sim 1.1) \cdot \sqrt{2} \cdot V_S = (1.48 \sim 1.56) \cdot V_S = (1.63 \sim 1.71) \cdot V_{SN} \quad (23)$$

V_d is always controlled to the rated value in this case, but the value is 20 % to 25 % higher than the rated V_d by three phase diode rectifier (10 % to 15 % higher than the peak value).

NOTE Due to the controlled mode this value is nearly independent from the load. In special cases (e.g. high dynamic applications) the DC link voltage could be significantly higher.

6.5 Resulting input converter section voltage reference potential

The interesting values of the voltages V_{G1}, V_d and V_{d+}, V_{d-} of each rectifier type at rated conditions are summarized together in table 5. In case of three phase active infeed Input Converter according to 6.4, the resulting values could be higher than the given typical values depending on the control of the individual application.

Table 5 – Typical range of values for the reference potentials of the DC link voltage, the DC-link voltages themselves and the grounding potentials in relation to supply voltage as "per unit value" for different kinds of input converters sections

	Single phase diode input converter according to 6.2	Three phase diode input converter according to 6.3	Three phase active infeed input converter according to 6.4 (typical values depending on control)	Three phase diode rectifier according to Figure 22 supplied from a delta grounded supply system
V_{G1} / V_S	-0,45...+0,45	-0,675...+0,675	-0,74(-0,78)... +0,74(+0,78)	-0,675...+0,675
V_d / V_S	0,9	1,35 1,6[a]	1,48...1,56	1,35 1,6[a]
V_{d-} /V_S, V_{d+} /V_S	–0,9... + 0,9	–1,35....1,35	–1,48(-1,56) ... +1,48(+1,56)	–1,35....1,35
[a] in case of dynamic braking with resistor and chopper				

6.6 Grounding

Grounding of the PDS, as a whole system, might be made in different ways.

The location of the grounding will be chosen according to the nature of the system:

- neutral of a common transformer if any,
- middle point of a common DC. link,
- the star point of any frequency converter output filter or
- the star point of the motor.

The grounding impedance may be resistive, capacitive or a direct connection. It generally should be connected to a protective grounding conductor.

The grounding impedances and therefore the potentials are strongly affected by these grounding systems.

The instantaneous values are also affected by the configuration of PDS and switching mode of rectifier and inverter.

6.7 Multipulse application

In case of multipulse applications the conditions are quite comparable to the IT power supply system supplied applications described above.

6.8 Resulting amplification factors in the differential mode model of the rectifier section

The amplification factors in differential mode model of rectifier section are shown in Table 6.

Table 6 – Amplification factors in the differential mode model of the rectifier section

	Single phase diode input converter according to 6.2	Three phase diode input converter according to 6.3	Three phase active infeed input converter according to 6.4 (typical values depending on control)
k_{D1}	0,9	1,35* 1,6[a]	1,48 … 1,56
[a] for dynamic braking with resistor and chopper (typical value)			

*NOTE The amplification factor according to Figure 20 depends on the load condition of the rectifier. In case of no-load condition this value may reach SQR 2. As a practical value 1,35 is estimated. See also figures 20 and 15

6.9 Resulting amplification factors in the common mode model of the rectifier section

The amplification factors in common mode model of rectifier section is shown in Table 7.

Table 7 – Amplification factors in the common mode model of the rectifier section

	Single phase Diode Input Converter according to 6.2	Three phase Diode Input Converter according to 6.3	Three phase active infeed Input Converter according to 6.4 (typical values depending on control)
k_{C1}	0[a] 0,45[b]	0[a] ± 0,675[b]	–0,74(-0,78) +0,74(+0,78)
[a] with symmetrical DC reactors or without DC reactors [b] with unsymmetrical DC reactors			

7 Output converter section (inverter section)

7.1 General

N-Level inverters have different possibilities of switching strategies, as e.g. applying only single voltage steps or by using redundant switching states with lowest common mode voltage. This might be discussed between system integrator, converter and motor supplier. This document describes in general the worst-case.

7.2 Input value for the inverter section

The input value for the inverter section is the averaged DC link voltage V_d. V_d is determined by the input converter section (see Clause 6).

7.3 Description of different inverter topologies

This section describes the most commonly used topologies of inverters with a DC link capacitor bank (or several capacitor banks), i.e. voltage source inverters. The number of levels N is equal to the number of possible voltages of the output phase to NP-Potential.

7.3.1 Two level inverter

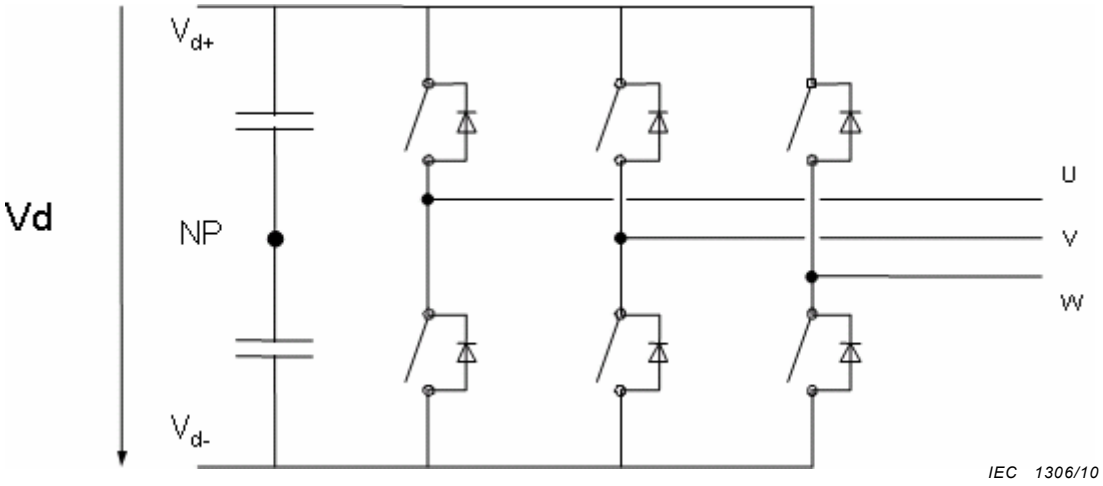


Figure 27 – Topology of a N = 2 level voltage source inverter

Each output phase u, v, w can be switched either to V_{d+} or V_{d-}. NP is the point with potential just in the middle of V_{d+} and V_{d-}.

In cases where the capacitor in Figure 27 is realized as a series connection of an even number of equal capacitors, NP is a physically accessible point.

7.3.2 Three level inverter

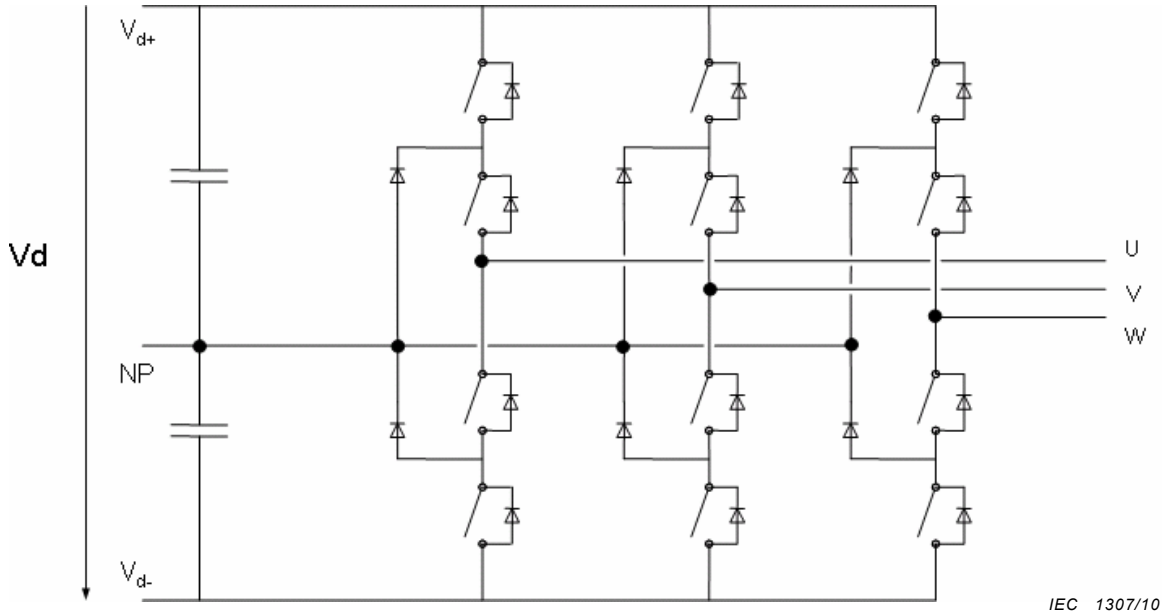


Figure 28 – Topology of a N=3 level voltage source inverter (neutral point clamped)

Each output phase can be switched either to V_{d+}, NP or V_{d-}. NP is a physically accessible point. The voltages of the upper and lower DC link half (i.e. from V_{d+} to NP respectively NP to V_{d-}) are assumed to be equal. This is typically achieved by the input section and DC link design and by means of control of the two voltages V_{d+} and V_{d-}.

7.3.3 N-level inverter

7.3.3.1 General

Two different approaches are used to achieve multi level voltage source inverters. Two examples are shown below. The differences regarding the output section are small. Both approaches can be extended to several levels by adding more stages.

Figures 29 and 30 show the simplest way of the idea of the N-Level inverter, which is a three level inverter. In practice three level inverters are typically built as described in Figure 28, where the N-level inverter topologies are used to achieve more levels.

7.3.3.2 N-level inverter with one DC link voltage and floating symmetrical DC link capacitors

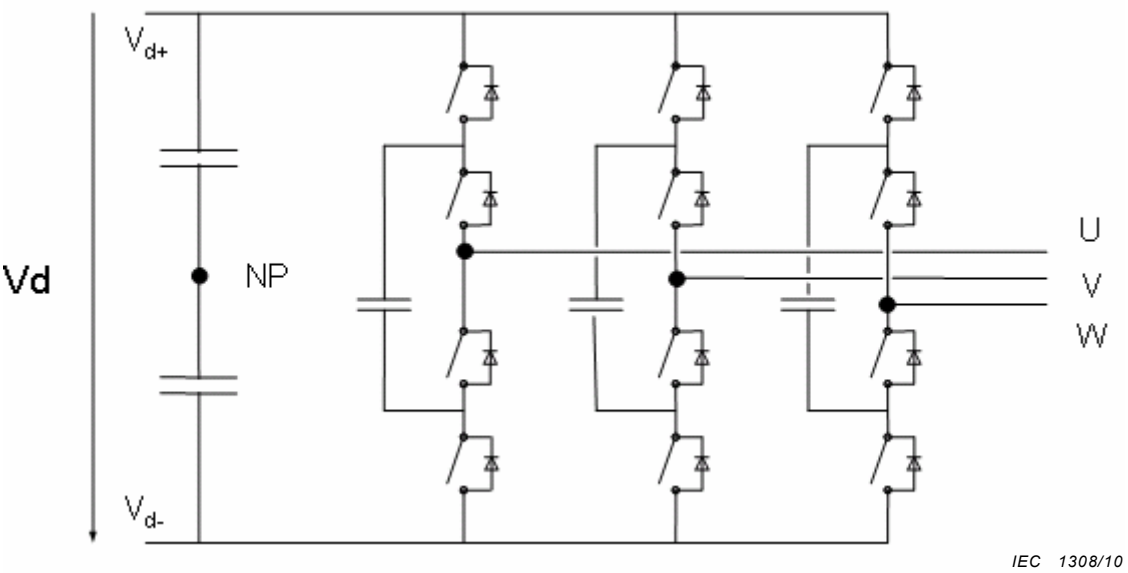


Figure 29 – Topology of a N = 3 level voltage source inverter (floating symmetrical capacitor)

Figure 29 shows the simplest topology with floating symmetrical capacitors. Each phase has in its output section a floating capacitor. It is assumed that the averaged voltage of a floating capacitor is such, that the levels have all the same size, which typically is achieved by means of control.

The number of voltage levels can be extended by adding more floating capacitor stages per phase. NP is dedicated as in case of the N = 2 level topology. Other topologies might be available but will do no fundamental change in effect to the output voltage.

Table 8 – Number of levels in case of floating symmetrical capacitor multi level

number of capacitors stages per phase of topology according to Figure 29	number of voltage levels at the output
1	3
2	4
3	5
m	m + 2

7.3.3.3 N-level inverter with m numbers of DC link voltages

Figure 30 shows the simplest topology with multi DC link. There are three DC links, each connected with two two-level inverter legs. NP is a physically accessible point connecting the output of one inverter leg of each DC link.

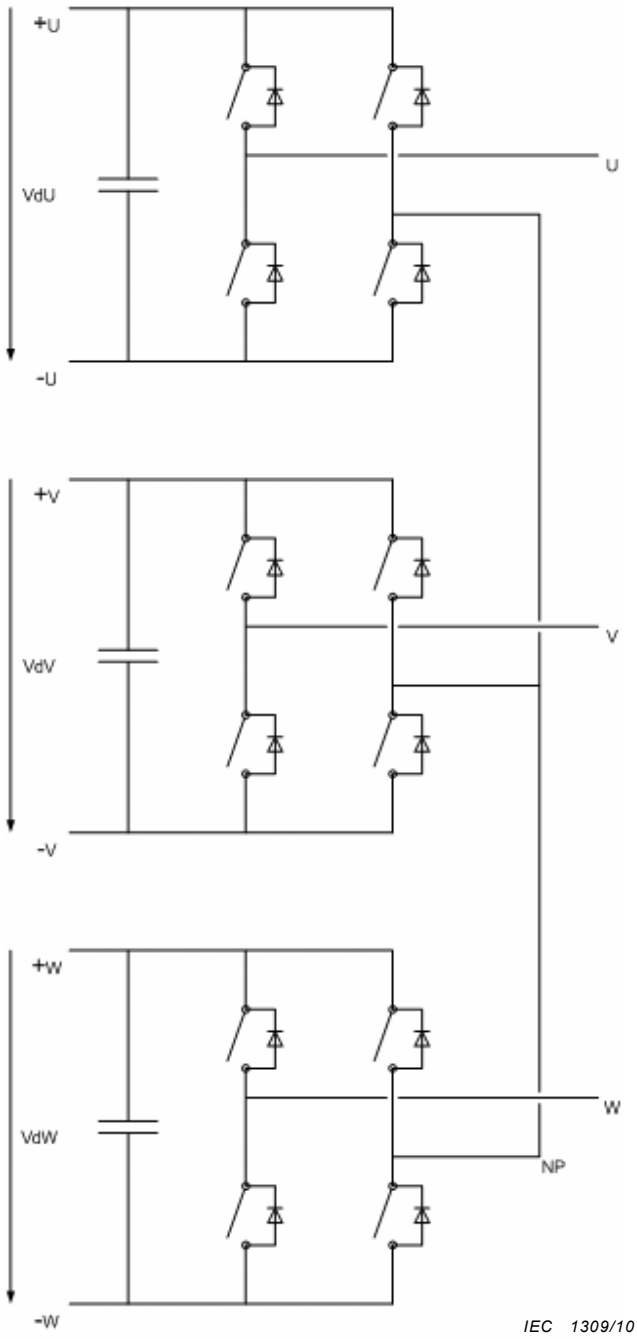
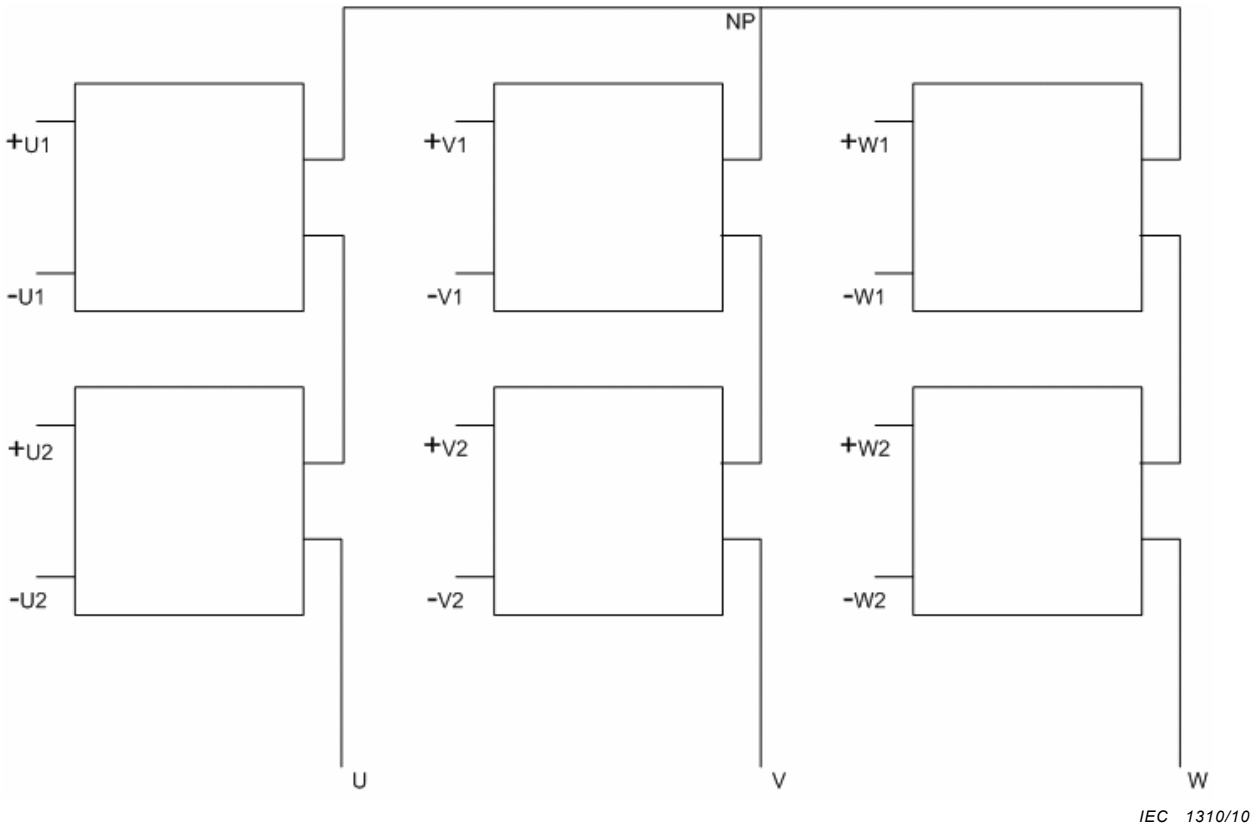


Figure 30 – Topology of a three level voltage source inverter (multi DC link), n_{dcmult} = 1. The voltages V_{dx} are of the same value

The number of voltage levels per inverter or at the output phase can be extended by adding more DC links per output phase and/or by changing the two level inverter legs into three level inverter legs. In this case each DC link would have middle points, but NP still is dedicated for the connecting point.

Table 9 – Number of levels in case of multi DC link inverter

n_{dcmult} – number of DC links per phase of the topology according to Figure 30	number of voltage levels per inverter leg	number of voltage levels at the output
1	2	3
1	3	5
2	2	5
2	3	9
3	2	7
3	3	13
n_{dcmult}	2	$2 \times n_{dcmult} + 1$
n_{dcmult}	3	$4 \times n_{dcmult} + 1$



NOTE In case the boxes are two level inverters the figure corresponds to line 3 of Table 9. In case the boxes are three level inverters the figure corresponds to line 4 of Table 9.

Figure 31 – Topology of an N-level voltage source inverter (multi DC link), $n_{dcmult} = 2$

7.4 Output voltage waveform depending on the topology

7.4.1 General

This section assumes idealized rectangular output waveform, i.e. ideal switches. For real switching conditions see 7.5 and 7.6.

7.4.2 Peak voltages of the output

The peak values of the output voltages are in general independent of the inverter topology. The exception is the multi DC link inverter.

Table 10 – Peak values of the output voltage waveform

	Two level according to Subclause 7.3.1	Three level according to Subclause 7.3.2	Multi level with n levels and floating symmetrical capacitor according to Subclause 7.3.3.2	Multi level with n levels and multi DC link topology according to Subclause 7.3.3.3
$\hat{V}_{PP}/V_d$	1	1	1	2 * n_{dcmult}
$\hat{V}_{PNP}/V_d$	1/2	1/2	1/2	n_{dcmult}
$\hat{V}_{PSP}/V_d$	2/3	2/3	2/3	4/3 * n_{dcmult}
$\hat{V}_{G2}-\hat{V}_{G1}/V_d$	1/2	1/2	1/2	n_{dcmult}

For topologies with more than two levels switching states are partly redundant. A common approach to reduce $\hat{V}_{G2}-\hat{V}_{G1}$ is to take in case of redundant states always the switching state with the lowest $\hat{V}_{G2}-\hat{V}_{G1}$. For the most common topologies, $\hat{V}_{G2}-\hat{V}_{G1}$ might be further reduced with this approach to 1/3 (three level) respectively 1/4 (five level).

7.5 Rise time of the output voltages

The rise times and overshoots for the voltages V_{PP} and V_{PNP} are determined by the behaviour of the switching device together with the snubber circuit of the switching device.

The rise times and overshoots for V_{PSP} and V_{G2}-V_{G1} is determined by the behaviour of the switching device together with the snubber circuit of the switching device and the grounding circuit of the PDS.

Different switching devices with various numbers of snubber circuits are used for different applications. Typically the rise time is so small, that it can be considered as zero for the input of the output filter. The design of the filter determines the rise time seen by the cables (see section 8). The range of rise time varies between tens of nanoseconds and microseconds for V_{PP} and V_{PNP}. Typically the rise time of V_{G2}-V_{G1} is higher, thus the step of V_{PSP} is a superposition of a faster (step of V_{PNP}) and a slower (step of V_{G2}-V_{G1}) step.

Determination of the dv/dt can be done with the voltage step size from Subclause 7.6.2 and the rise time regarding V_{PP} and V_{PNP}.

In case the rise time of V_{G2}-V_{G1} is big compared with the rise time of the switching device, the dv/dt of V_{PSP} tends to the value for V_{PNP}, if the switching occurs in the considered phase. If the switching occurs in one of the two other phases it tends to zero.

The ranges of the expected dv/dt is mainly dependant on the semiconductor technology (as e.g. FET, IGBT, Thyristor, GTO, IGCT, IEGT, GCT) and the range of the output voltage and power or the application. Table 11 gives a typical range of the state of the art technologies.

Table 11 – Typical ranges of expected dv/dt at the semiconductor terminals

Low voltage application	five to several tens of kV per μs
Medium voltage application	One to ten kV per μs

7.6 Compatibility values for the dv/dt

7.6.1 General

The operating principle of the inverter is in general to chop the DC link constant voltage V_d into a PWM (pulse width modulated) voltage impulse in order to synthesize the transient voltages versus time areas. With this sinusoidal approach a variable fundamental frequency and amplitude can be achieved at the terminals of a motor.

For determination of the expected dv/dt this value could be constructed from the knowledge of the voltage step height of the dedicated voltage pulse during a switching of semiconductors divided by the expected rise (fall) times.

7.6.2 Voltage steps

A single voltage step during transition of a switching phase means the lowest possible output voltage step height:

Table 12 – Example for a single voltage step in a three level topology

	State before switching	State after switching
Phase U	NP	NP
Phase V	NP	NP
Phase W	+W	NP

The voltage step height for a single step is given in table 13, where N is the number of levels of the topology. The values for the two and three level inverters can be derived from the formula of the multi level with floating symmetrical capacitor inverter.

The values for the multi DC link inverter is independent of the number of levels N and corresponds to the values of the two respective three level inverter, depending on the number of levels of the individual inverter legs.

The voltage step height is almost linear to the DC link voltage which has in practice a certain ripple (due to the ripple the step height might be increased or decreased depending on the moment of switching). Moreover there are special operation points limited in time (e.g. network over voltage or regenerative braking mode), which might further increase the DC link voltage.

Table 13 – Expected voltage step heights for single switching steps of an n level inverter

	Two level according to Subclause 7.3.1	Three level according to Subclause 7.3.2	Multi level with N levels and floating symmetrical capacitor according to Subclause 7.3.3.2	Multi level with N levels and multi DC link topology according to Subclause 7.3.3.3
V_{step_PP} / V_d	1	$\frac{1}{2}$	$\frac{1}{N-1}$	$\frac{1}{2}$ up to 1
V_{step_PNP} / V_d	1	$\frac{1}{2}$	$\frac{1}{N-1}$	$\frac{1}{2}$ up to 1
V_{step_PSP} / V_d in case the inherent phase is switching	$\frac{2}{3}$	$\frac{1}{3}$	$\frac{1}{N-1} \cdot \frac{2}{3}$	$\frac{1}{3}$ up to $\frac{2}{3}$
V_{step_PSP} / V_d in case an adjacent phase is switching	$\frac{1}{3}$	$\frac{1}{6}$	$\frac{1}{N-1} \cdot \frac{1}{3}$	$\frac{1}{6}$ up to $\frac{1}{3}$
(V_{step_G2}-V_{step_G1}) / V_d	$\frac{1}{3}$	$\frac{1}{6}$	$\frac{1}{N-1} \cdot \frac{1}{3}$	$\frac{1}{6}$ up to $\frac{1}{3}$

7.6.3 Multistep approach

A multi step means a step, where the step size is higher.

Table 14 – Example for multi steps in a three level topology

	Example	
	State before switching	State after switching
Phase U	NP	NP
Phase V	NP	+V
Phase W	+W	NP

The voltage step size in case of a multi step is a multiple of the voltage step size in case of a single step. The biggest possible voltage step is shown in Table 15.

Table 15 – Biggest possible voltage step size for multi steps

	Two level according to Subclause 7.3.1	Three level according to Subclause 7.3.2	Multi level with N levels and floating symmetrical capacitor according to Subclause 7.3.3.2	Multi level with N levels and multi DC link topology according to Subclause 7.3.3.3
V_{step_PP} / V_d	2	2	2	4 * n_{dcmult}
V_{step_PNP} / V_d	1	1	1	2 * n_{dcmult}
V_{step_PSP} / V_d in case the inherent phase is switching	4/3	4/3	4/3	8/3 * n_{dcmult}
V_{step_PSP} / V_d in case an adjacent phase is switching	2/3	2/3	2/3	4/3 * n_{dcmult}
(V_{step_G2}-V_{step_G1}) / V_d	1	1	1	2 * n_{dcmult}

NOTE 1 The values of Table 15 corresponds basically to the doubled values of Table 10

NOTE 2 By measures of control the biggest possible voltage step may be limited to smaller values, even limitation to single steps are possible. Depending on the snubber circuit of the semiconductors such limiting control measures are in certain inverters mandatory.

7.7 Repetition rate

The repetition rate (in the sense of a frequency) of voltage steps of the inverter can be approximated by the pulse frequency f_P independent of the topology:

Table 16 – Repetition rate of the different voltages depending on the pulse frequency

V_{PP}	$2 * f_P$
V_{PNP}	f_P
V_{PSP} in case the inherent phase is switching	f_P
V_{PSP} in case an adjacent phase is switching	$2 * f_P$
V_{G2}-V_{G1}	$3 * f_P$

The pulse frequency f_P is approximated by the switching frequency f_{SW} independent on the topology:

Table 17 – Relation between f_P and f_{SW}

	Two level according to clause 7.3.1	**Three level according to clause 7.3.2**	**Multi level with N levels and floating symmetrical capacitor according to clause 7.3.3.2**	**Multi level with N levels and multi DC link topology according to clause 7.3.3.3**
f_P/f_{SW}	1	2	N - 1	N - 1

The switching frequency is only an internal value of the inverter. From the output only the pulse frequency can be seen.

7.8 Grounding

Depending on the grounding system all characteristic values for the phase to ground voltage at the inverter output lie between the corresponding values for V_{PNP} and V_{PSP}. The voltage V_{G2}-V_{G1} is determined by the inverter, whereas the partition to V_{G1} and V_{G2} is determined by the grounding system.

7.9 Resulting amplification effect in the differential mode model of the inverter section

Table 18 – Resulting amplification factors in the differential mode model

	Two level according to Clause 7.3.1	Three level according to Clause 7.3.2	Multi level with N levels and floating symmetrical capacitor according to Clause 7.3.3.2	Multi level with N levels and multi DC link topology according to Clause 7.3.3.3
$k_{D2} = \hat{V}_{PP} / V_d$	1	1	1	2 * n_{dcmult}

Table 18 shows the resulting differential mode amplification factor k_{D2} of the inverter section as described in Clause 4. This factor is needed for the final calculation of the models.

7.10 Resulting additive effect in the common mode model of the inverter section

Table 19 – Resulting additive effect (amplification factors) in the common mode model

	Two level according to Clause 7.3.1	Three level according to Clause 7.3.2	Multi level with N levels and floating symmetrical capacitor according to Clause 7.3.3.2	Multi level with N levels and multi DC link topology according to Clause 7.3.3.3
$k_{C2} = \hat{V}_{G2} - \hat{V}_{G1} / V_d$	± 1/2	± 1/2	± 1/2	± n_{dcmult}

Table 19 shows the resulting common mode additive effect k_{C2} of the inverter section as described in section 4. This factor is needed for the final calculation of the models.

7.11 Resulting relevant dynamic parameters of pulsed common mode and differential mode voltages

Table 20 – Resulting dynamic parameters of pulsed common mode and differential mode voltages

	Low voltage application	Medium voltage application
t_{r2}	50 ns … 200 ns	100 ns … 1 µs
f_P / f_1	5 … 300	N – 1 … 50

Table 20 shows the resulting dynamic parameters of the inverter section. This factor is needed for the final calculation of the models, especially as input for the cable section.

8 Filter section

8.1 General purpose of filtering

In contrast to the PDS subsystems described in the Clauses 5, 6, 7, 8 and 9, output filters of the inverter are not a mandatory but an optional subsystem of the PDS. Filters at the inverter output can be used to improve the overall system performance of the PDS.

Filters may affect the control, thermal stress and current stress of the inverter. It must be assured that the converter is designed for the operation with a filter. The compatibility of filters with the converter should be clarified with the converter manufacturer.

8.2 Differential mode and common mode voltage system

In the differential mode voltage system, the fundamental frequency f_1 of the inverter output is in the region of the rotating frequency of the motor. This fundamental frequency is the desired part of the output voltage. However, the differential mode spectrum will contain amplitudes in the range of the pulse frequency and its harmonics, higher harmonics usually showing lower amplitudes. The harmonics or at least a part of them are the scope of differential mode filtering.

In the common mode spectrum, the fundamental frequency f_1 could be zero. Depending on the modulation scheme, some amplitude at f_1 and its harmonics might be observed as well. This low frequency common mode voltage is not critical for the application. The side bands of the pulse frequency f_p and its harmonics will be visible in the common mode voltage as well; these amplitudes are the scope of common mode filtering.

In the frequency range between the harmonics of the fundamental frequency f_1 and the pulse frequency f_p as well as between the different harmonics of the pulse frequency f_p, the amplitudes will be small in both common mode and differential mode systems.

In differential mode and common voltage system, the following specific main issues are known which can be improved by filters:

a) Differential mode:
   - Insulation stress of the individual turns of a motor winding
   - Acoustic noise in the motor
   - Motor losses due to harmonic currents that do not contribute to the energy conversion
   - Increased allowed motor cable length
   - Bearing currents
   - Thermal overheating of the inverter due to large differential mode currents in long motor cables

b) Common mode:
   - Insulation stress of the motor winding to the motor housing on ground potential
   - Bearing currents
   - EMI
   - Thermal overheating of the inverter due to large common mode currents in long motor cables

8.3 Filter topologies

8.3.1 General

All commonly used inverter output filter types are low pass filters. The basic topology of a low pass filter is a combination of an inductor and a capacitor as shown in Figure 32:

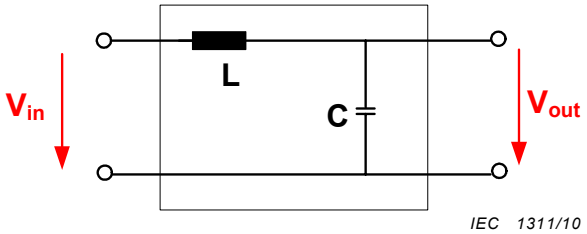


Figure 32 – Basic filter topology

The basic characteristic of a filter is its resonance frequency f_0 which is calculated as follows:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{24}$$

The basic target of the filter is to suppress all amplitudes in the spectrum of V_{in} with frequencies above the resonance frequency f_0. Amplitudes in the region of the resonance frequency will be amplified, therefore it is important to choose the resonance frequency carefully to make sure that V_{in} does not contain remarkable amplitudes in that frequency range.

The filter topologies described can generally be designed either for the common mode or the differential mode voltage system. The overall filter design will consist of the combination of differential mode and common mode filter.

Differential mode filters are connected between the output phases of the inverter. In a three phase application, the filter inductor of a differential mode filter must be a differential mode choke or a single phase choke and cannot be realized as a current compensated choke.

Common mode filters are connected from each output phase to ground. In order to make sure proper operation, the connection to ground shall have as low a resistance and inductance as possible. The higher the filtered frequencies are, the more important the inductance becomes. The inductor of common mode filters is often realized as a current compensated choke.

In some applications, common mode filters are connected to the DC link terminals instead of ground. These filters are able to suppress the common mode voltage of the inverter as well. However, in this case the common mode voltage of the infeed converter of the PDS will not be filtered.

8.3.2 Sine wave filter

The target of a sine wave filter is to suppress all amplitudes in the spectrum of V_{in} in the frequency range of the switching frequency and above. Using a sine wave filter, V_{out} shows a nearly sinusoidal waveform and contains mainly the fundamental frequency of V_{in}. The resonance frequency of the sine wave filter will be chosen between the fundamental frequency and the pulse frequency:

$$f_1 < f_0 < f_p \tag{25}$$

The selection of the filter resonant frequency is a compromise between the following considerations:

a) If the resonance frequency is too low, the sine wave filter might be excited by the harmonics of the fundamental frequency.

b) If the resonance frequency is too high, the suppression of the amplitudes with pulse frequency might be insufficient.

With a sine wave filter, all negative aspects described above can be improved significantly. Especially the motor losses and the acoustic motor noise can only be improved by a sine wave filter. However, as the cost of a sine wave filter is relatively high, sine wave filters are mainly used in the differential mode voltage system only (see Figure 33).

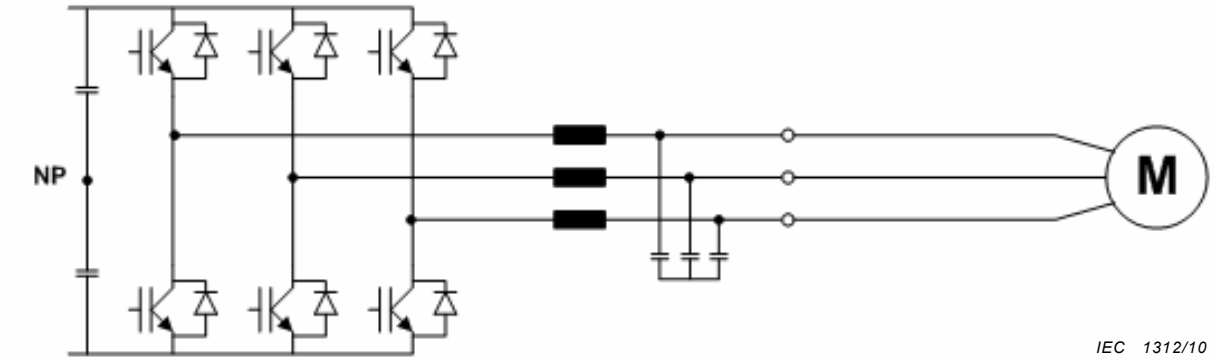


Figure 33 – Topology of a differential mode sine wave filter

The topology of a common mode sine wave filter is shown in Figure 34:

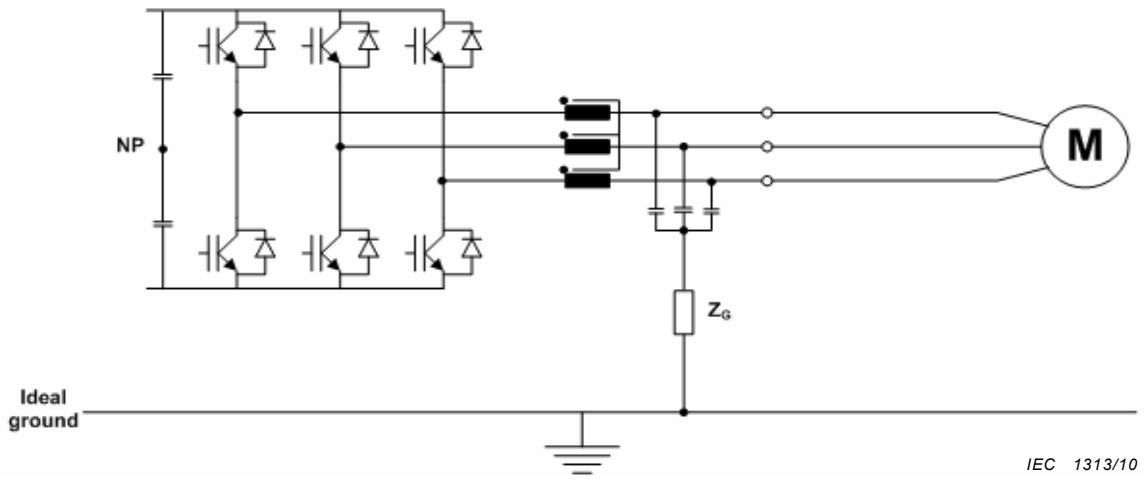


Figure 34 – Topology of a common mode sine wave filter

Due to the relatively low resonance frequency of the sine wave filter, the filter inductor causes a voltage drop at the fundamental frequency f_1. In general applications, up to 6 % of the motor voltage can be observed at the filter inductor. As a consequence, the motor voltage is reduced, resulting in reduced mechanical power at the rotor of the motor.

8.3.3 dV/dt filter

The basic topology of a dV/dt is the same as the topology of the sine wave. The difference between these two filter types is created by the choice of their resonance frequency f_0. The task of a dV/dt filter is to increase the rise time of the inverter output voltage. In order to guarantee a minimum rise time $t_{r\,min}$, the resonance frequency has to be chosen according to:

$$f_0 < \frac{1}{2t_{r\,\min}} \tag{8}$$

If a dV/dt filter is realized by a simple LC combination according to Figure 32, a voltage overshoot by a factor of up to 2 will be observed in the output voltage, as the resonance frequency of the dV/dt filter usually is clearly above the pulse frequency f_p of the inverter. In order to avoid this, additional damping elements can be used. A further possibility to limit the voltage overshoot is to clamp the filter output voltage to the DC link. However, damping elements will still be required in that solution. Depending on the amount of damping a certain voltage overshoot will remain in the output voltage.

dV/dt filters are used for both common mode and differential mode voltage systems. They can also be used in combination with a sine wave filter, e.g. a sine wave filter for the differential mode and a dV/dt filter for the common mode voltage.

By increasing the rise time, dV/dt filters lead to reduced voltage stress of the motor. Bearing currents can be reduced by dV/dt filters as well.

8.3.4 High frequency EMI filters

High frequency EMI filters (see Figure 35) are only used as common mode filters to reduce the EMI noise level of conducted and radiated emissions. The target frequency range is from 150 kHz to 100 MHz. HF EMI filters are very often used at the input terminals of a PDS to the line section, and in some applications, they are used at the inverter output as well.

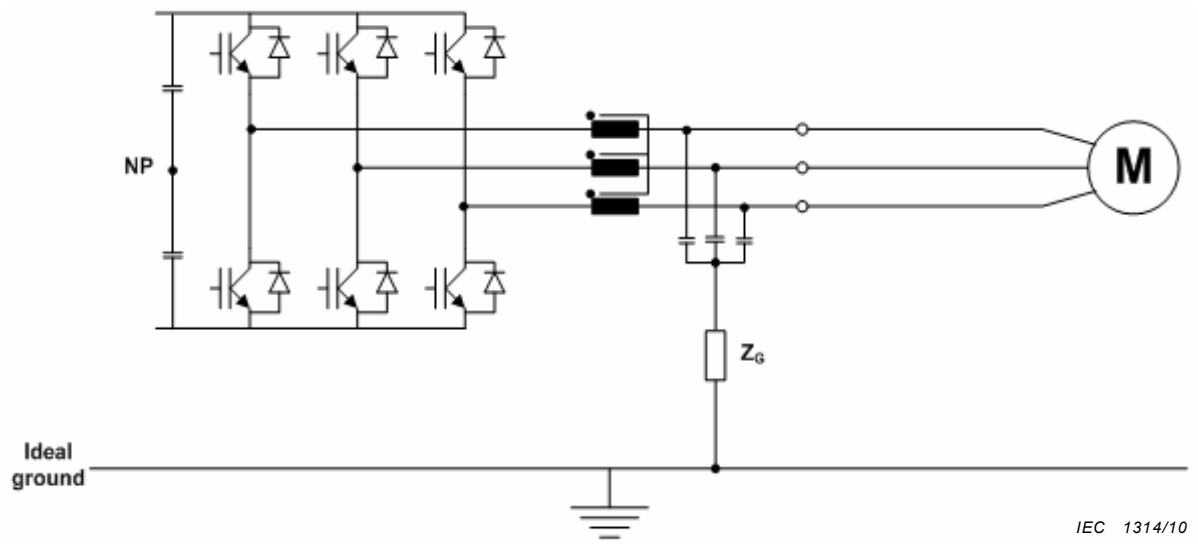


Figure 35 – EMI filter topology

Especially for HF common mode filters, it is extremely important to minimize the grounding impedance Z_G for proper operation.

8.3.5 Output choke

Output chokes (see Figure 36) can be placed at the inverter output as three phase chokes. As this topology does not contain a filter capacitor, it is not a real filter topology in itself. In combination with the parasitic capacitances of the motor cables and the motor windings, output chokes are operating as a small dV/dt filter, reducing dV/dt at the motor terminals. An additional purpose in case of small drives might be the extension of the motor cable length due to common mode current limitations. This behaviour strongly depends on the values of the parasitic capacitances and therefore on the concrete application. The voltage overshoot described in the section of the dV/dt filter might occur at the motor terminals, depending on the damping behaviour of the motor cables and the motor. Without damping, output chokes may increase the probability of double pulse phenomena (see chapter Clause 9).

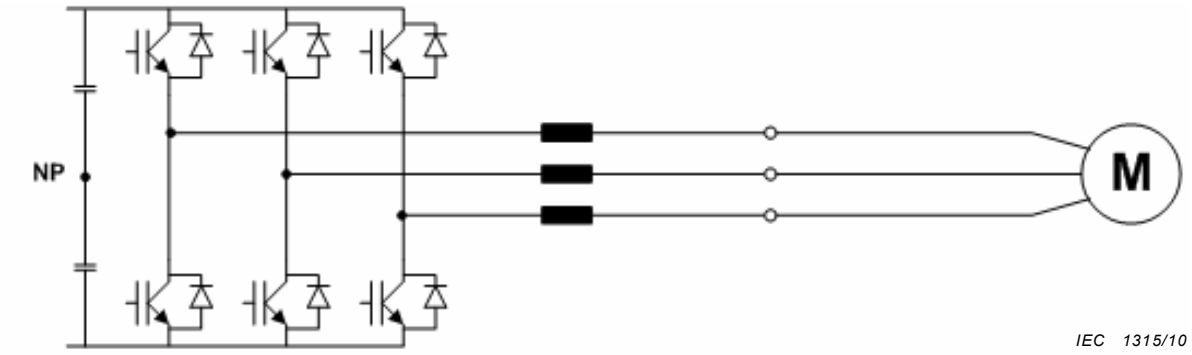


Figure 36 – Topology of the output choke

8.4 Resulting amplification effect in the differential mode model after the filter section

The resulting amplification factors of the filter section in the differential mode system are as shown in table 21:

Table 21 – Typical resulting differential mode filter section parameters for different kinds of differential mode filter topologies

	Sine wave filter	dV/dt filter	HF common mode filter or without differential mode filter	Output choke
k_{D3}	0,97	1,2 ... 1,5	1	1.2 ... 2
t_{r3}	n.a.*	2 µs	50 ns ... 100 ns	500 ns ... 1 µs
f_p / f_1	10 ... 300	5 ... 100	5 ... 100	5 ... 100

*NOTE The rise time definition is not applicable to a sinusoidal waveform. dv/dt-effects related to short rise times are eliminated by this kind of filters.

8.5 Resulting additive effect in the common mode model after the filter section

For the parameters in Table 22 it is assumed that the common mode input voltage of the filter section does not contain any low frequency amplitudes (below f_0) in its spectrum. This depends on the modulation scheme of the inverter and converter and the mains system. If it does, the low frequency common mode voltage will not be filtered in any topology. Low frequency common mode voltages are not critical for the PDS application.

Table 22 – Typical resulting common mode filter section parameters for different kinds of common mode filter topologies

	Sine wave filter	dV/dt filter	HF common mode filter or without differential mode filter	Output choke
k_{C3}	1,2 ... 1,5**	1,2 ... 1,5	1	1,2 ... 2
t_{r3}	2 µs	2 µs	50 ns ... 100 ns	500 ns ... 1 µs
f_p / f_1	10 ... 300	5 ...100	5 ...100	5 ...100

**NOTE Sine wave filters connected to ground will result in $k_{C3} = 0$.

9 Cabling section between converter output terminals and motor terminals

9.1 General

The output voltage of the power converter is a series of trapezoidal pulses with a variable width (pulse width modulation) characterized by a pulse rise-time t_r.

The pulses travel along the motor cable with a propagation velocity given by:

$$v = \frac{1}{\sqrt{L_0 C_0}} \tag{27}$$

Where L_0 is the cable characteristic inductance and C_0 is the cable characteristic capacitance.

Typical values for L_0 are between 200 nH/m and 800 nH/m and for C_0 between 50 pF/m and 600 pF/m. The typical propagation velocity is between 50 m/µs and 300 m/µs.

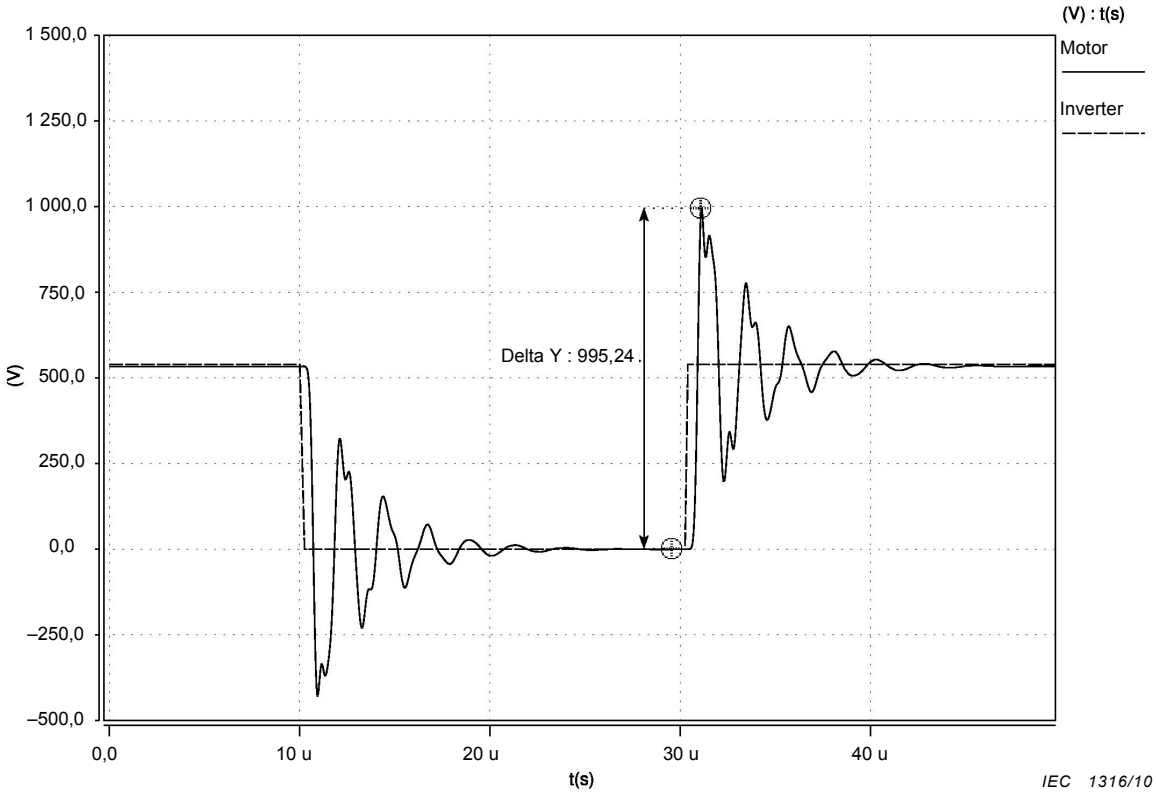


Figure 37 – Example of converter output voltage and motor terminal voltage with 200 m motor cable

The typical rise time t_r is 50 ns to 1 µs (insert the values given in the previous section). A critical cable length l_{cr} can be defined, representing the cable length where a pulse travels along the motor cable, reflects at the motor terminals and returns to the power converter output after a time interval which equals the rise time t_r.

$$l_{cr} = \frac{v \cdot t_r}{2} \tag{28}$$

9.2 Cabling

Because of the impedance mismatch between the cable characteristic impedance Z_0 and the motor surge impedance Z_m a wave reflection occurs causing a ringing voltage overshoot at the motor terminals.

At cable lengths above the critical length l_{cr} the peak voltage at the motor terminals will be:

$$V_{mot} = (1 + \Gamma)V_{inv} \tag{29}$$

At cable lengths below the critical length l_{cr} the maximum peak voltage can be approximated by:

$$V_{mot} = \left(\frac{l_c \cdot \Gamma}{l_{cr}} + 1 \right) \cdot V_{inv} \tag{30}$$

V_{mot} is the peak voltage at the motor terminals, V_{inv} is the power converter output voltage, l_c is the cable length and Γ (Gamma) is a reflection coefficient depending on the impedance mismatch between the motor cable and motor:

$$\Gamma = \frac{Z_m - Z_0}{Z_m + Z_0} \tag{31}$$

The cable impedance Z_0 is well-defined and depends on the cable parameters such as: characteristic inductance L_0, characteristic capacitance C_0, characteristic resistance of the conductors R_0, characteristic conductance of the insulation G_0. Z_0 is expressed by:

$$Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}} \approx \sqrt{\frac{L_0}{C_0}} \tag{32}$$

The motor surge impedance is not well documented and not easy to measure. Some typical values and the resulting reflection coefficient are given in the table below:

Table 23 – Resulting reflection coefficients for different motor frame sizes

Motor power [kW]	Zm [Ω]	Γ
< 3,7	2000 – 5000	0,95
90	800	0,82
355	400	0,6

In the case of parallel cables the cable characteristic impedance is also reduced, resulting in a higher reflection coefficient.

9.3 Resulting parameters after cabling section

This chapter gives the typical resulting cabling section parameters for different kinds of cabling topologies.

Table 24 – Typical resulting cabling section parameters for different kinds of cabling topologies

	After cabling length below critical length and without filter or with a common mode high frequency filter	After cabling length above critical length and without filter or with a common mode high frequency filter	After output chokes, dv/dt filters	After sine wave filters
k_{D4}	$\left(\frac{l_c \cdot \Gamma}{l_{cr}} + 1\right)$	$(1 + \Gamma)$	1*	1
k_{C4}	$\left(\frac{l_c \cdot \Gamma}{l_{cr}} + 1\right)$	$(1 + \Gamma)$	$\left(\frac{l_c \cdot \Gamma}{l_{cr}} + 1\right)$ below critical length $(1 + \Gamma)$ above critical length	$\left(\frac{l_c \cdot \Gamma}{l_{cr}} + 1\right)$ below critical length $(1 + \Gamma)$ above critical length
t_{r4}	$\approx t_{r3} \times \left(\frac{l_c \cdot \Gamma}{l_{cr}} + 1\right)$	$\geq t_{r3} \times (1 + \Gamma)$	2µs	Not applicable
f_p / f_1	5 - 100	5 - 100	5 - 100	1
*NOTE In case of cable length in the range or above the critical value, the value will reach up to 2 / k_{D3}				

10 Calculation guidelines for the voltages on the power interface according to the section models

According to the parameters shown in Figures 3 and 4, the following values may occur at the motor terminals under worst case conditions if the motor is fed by a converter system.

Remembering Formula 17 gives the phase to ground voltage at the motor terminals:

$$\hat{V}_{PG,Motor} = \frac{1}{\sqrt{3}} V_S \cdot \prod_{i=1}^{4} k_{Di} + V_S \cdot \left(\sum_{i=0}^{2} k_{Ci}\right) \cdot \prod_{i=3}^{4} k_{Ci}$$

Concerning the individual factors the formula can be written as:

$$\hat{V}_{PG,Motor} = \frac{1}{\sqrt{3}} \hat{V}_{pp} + V_S \cdot \left(\sum_{i=0}^{2} k_{Ci}\right) \cdot \prod_{i=3}^{4} k_{Ci} \quad (33)$$

The individual parameters are:

$$\hat{V}_{pp} / V_S = \prod_{i=1}^{4} k_{Di} \quad (34)$$

$$\hat{V}_{pp*} / V_S = 2 \cdot \prod_{i=1}^{4} k_{Di} \tag{35}$$

With formula 29:

$$\hat{V}_{pp-fp*} / V_S = (1 + 2 \cdot \Gamma) * \prod_{i=1}^{3} k_{Di} \tag{36}$$

The above values are calculated according to the system approach proposed in this document using the differential mode and common mode equivalent circuit and the related differential mode and common mode amplifying factors. The following figures show the differential mode equivalent circuit and common mode equivalent circuit with related sections and amplifying factors k_{Dv} and $k_{C\mu}$.

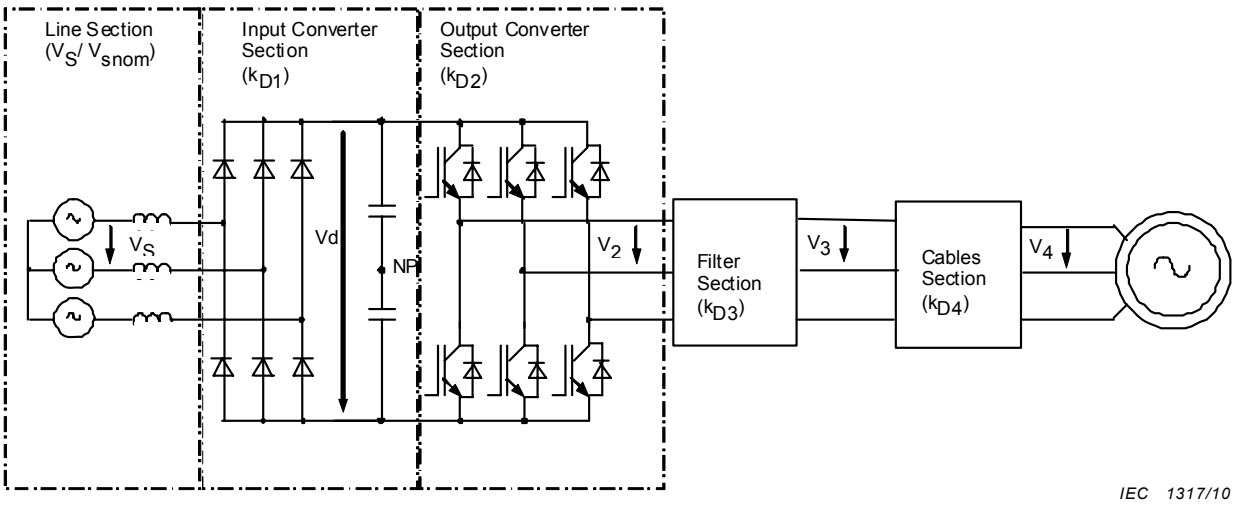


Figure 38 – Differential mode equivalent circuit

Line Section: V_S / V_{sN}

Input Converter Section: $V_d = k_{D1} * V_S$

Output Converter Section: $V_2 = k_{D2} * V_d$

Filter Section: $V_3 = k_{D3} * V_2$

Cables Section: $V_4 = k_{D4} * V_3$

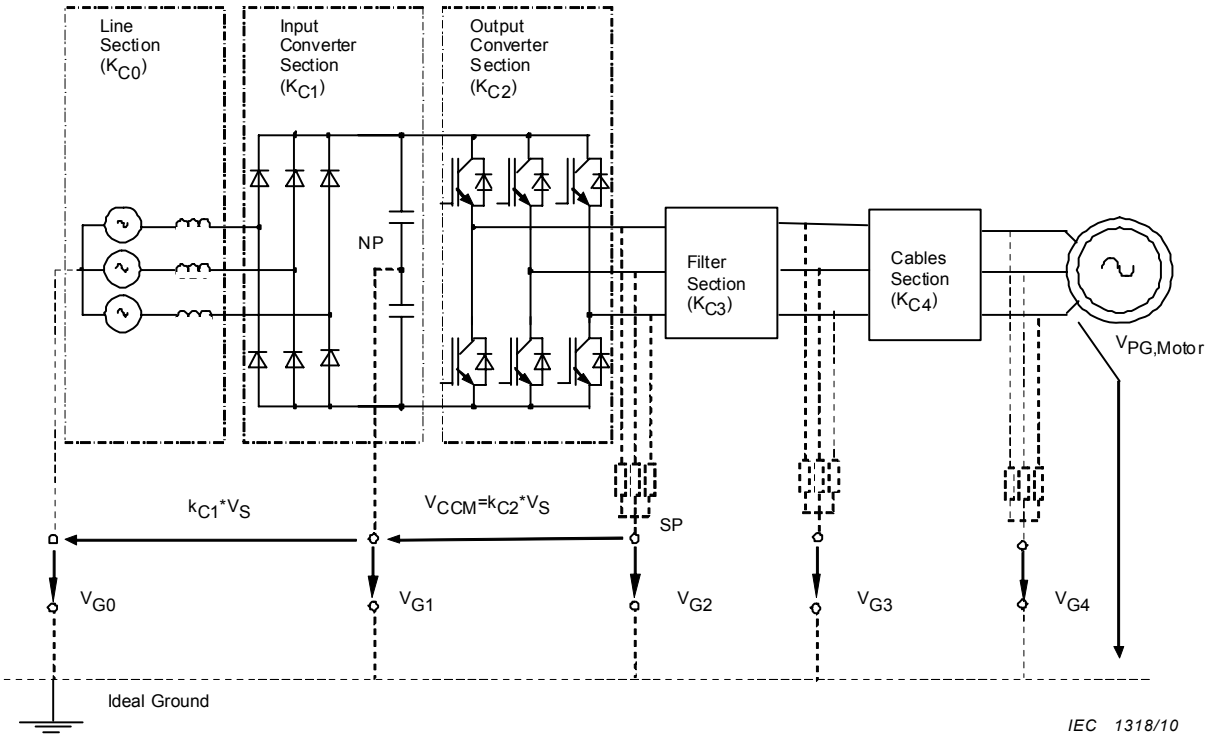


Figure 39 – Common Mode Equivalent Circuit

Line Section: $V_{G0} = k_{C0} * V_S$

Input Converter Section: $V_{G1} = V_{G0} + k_{C1} * V_S = (k_{C0} + k_{C1}) * V_S$

Output Converter Section: $V_{G2} = V_{G1} + k_{C2} * V_S = (k_{C0} + k_{C1} + k_{C2}) * V_S$

Filter Section: $V_{G3} = k_{C3} * V_{G2} = k_{C3} * (k_{C0} + k_{C1} + k_{C2}) * V_S$

Or $V_{G3} = V_{G1} + k_{C3} * k_{C2} * V_S = (k_{C0} + k_{C1} + k_{C2} * k_{C3}) * V_S$

according to filter topology (see Clause 8)

Cables Section: $V_{G4} = k_{C4} * V_{G3}$

Motor phase-to-ground voltage: $V_{PG,Motor} = V_{PP,Motor} / \sqrt{3} + V_{G4}$

11 Installation and example

11.1 General

Scope of this chapter is to analyze common installations as examples to show how to apply the document. The result is a combination of a common mode and a differential mode voltage under worst case conditions.

11.2 Example

– TN network V_{SN}= 400 V plus a tolerance value of 10 % (according to table 1)

– three phase diode rectifier as input section

– symmetrical or without DC reactor

– two level output converter (voltage source), t_{r2} = 50 ns, dv/dt = 10 kV/µs, f_1 = 50 Hz without filter => $t_{r3} = t_{r2}$
– 2,2 kW standard asynchronous motor.
– 100 m cable, "oilflex"(C_0=130 pF/m, L_0= 650 nH/m)

According to Formula 27 the propagation velocity reaches 108,8 m/µs. The critical length according to formula 28: l_{cr} = 2,72 m. The connection with a 100 m cable therefore is the case above the critical length.

The starting data is the value V_S= 400 V + 10 % of the supply voltage of the converter (see 3.2.13): this is the highest RMS value of the phase-to-phase voltage coming from the transformer section.

The target data are the electrical values at converter terminals and motor terminals.

Table 25 – Result of amplification factors and additive effects according to the example configuration and using the models of chapters 5 to 9

	Line Section Chapter 5	Input Converter Section Chapter 6	Output Converter Section Chapter 7	Filter Section Chapter 8	Cabling and Motor Section Chapter 9
Section	5.4, 5.5	6.8, 6.9	7.10, 7.11	8.4, 8.5	9.2
Differential Mode Factors	V_S /V_{SN}= 1,1	k_{D1} = 1,35	k_{D2} = 1	k_{D3} = 1	k_{D4} = 1,95
Common Mode Factors	k_{C0} = 0	k_{C1} = 0	k_{C2} = ±0,5	k_{C3} = 1	k_{C4} = 1,95

The resulting values and factors are calculated according to Equation 17

$$\hat{V}_{PG,Motor} = \frac{1}{\sqrt{3}} V_S \cdot \prod_{i=1}^{4} k_{Di} + V_S \cdot (\sum_{i=0}^{2} k_{Ci}) \cdot \prod_{i=3}^{4} k_{Ci}$$

$$\hat{V}_{PG,Motor} = \frac{1}{\sqrt{3}} \cdot V_S \cdot (1{,}35 \cdot 1 \cdot 1 \cdot 1{,}95\ ) + V_S \cdot (0 + 0 \pm 0{,}5) \cdot 1 \cdot 1{,}95 \approx V_S \cdot (1{,}52 \pm 0{,}98\ ) = V_S \cdot (0{,}54....2{,}50)$$

$$= 440V \cdot (0{,}54....2{,}50) = 238V....1100V$$

According to the parameters which are asked by Figure 3 the following values may occur under worst case conditions.

$$\hat{V}_{pp} / V_S = \prod_{i=1}^{4} k_{Di} = 2{,}63 \Rightarrow V_{pp*} = 1157V$$

$$\hat{V}_{pp*} / V_S = 2 \cdot \prod_{i=1}^{4} k_{Di} = 5{,}26 \Rightarrow \hat{V}_{pp} = 2315V$$

According to formula 36

$$\hat{V}_{pp-fp*} / V_S = (1{,}35 \cdot 1 \cdot 1 \cdot (1 + 2 \cdot 0{,}95\ )) = 3{,}92 \Rightarrow \hat{V}_{pp-fp*} = 1725V$$

According to table 24 the values for t_{r4} ~ 100 ns and f_p ~ 5 kHz according to modulator.

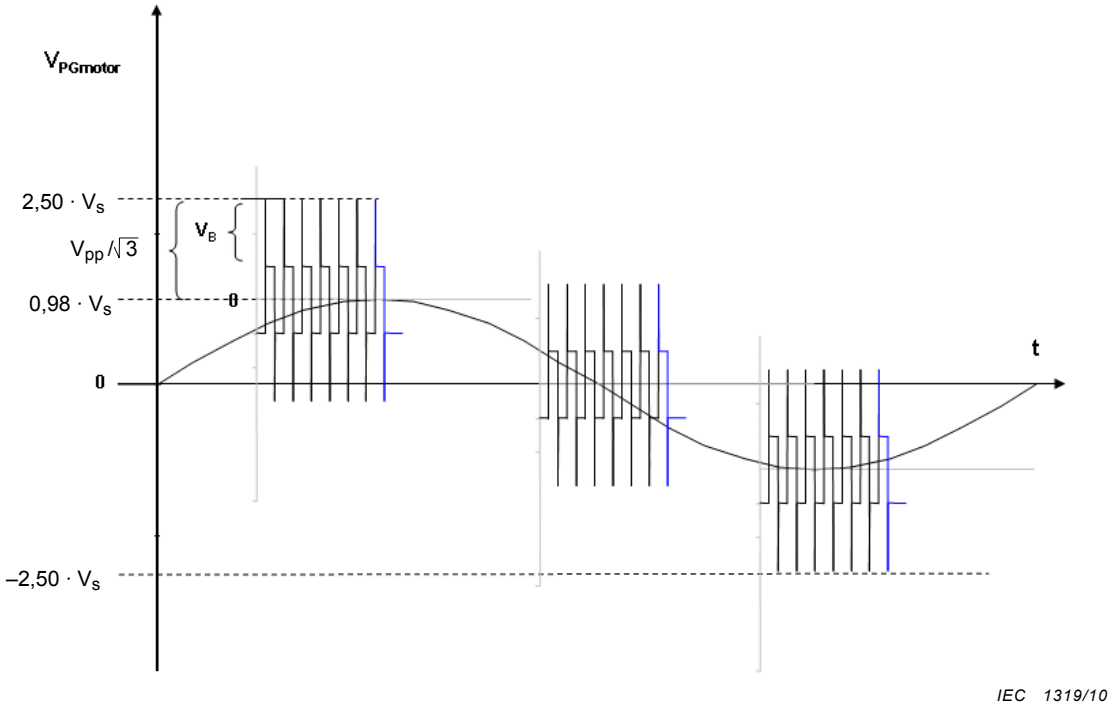


Figure 40 – Resulting phase to ground voltage at the motor terminals for the calculated example under worst case conditions

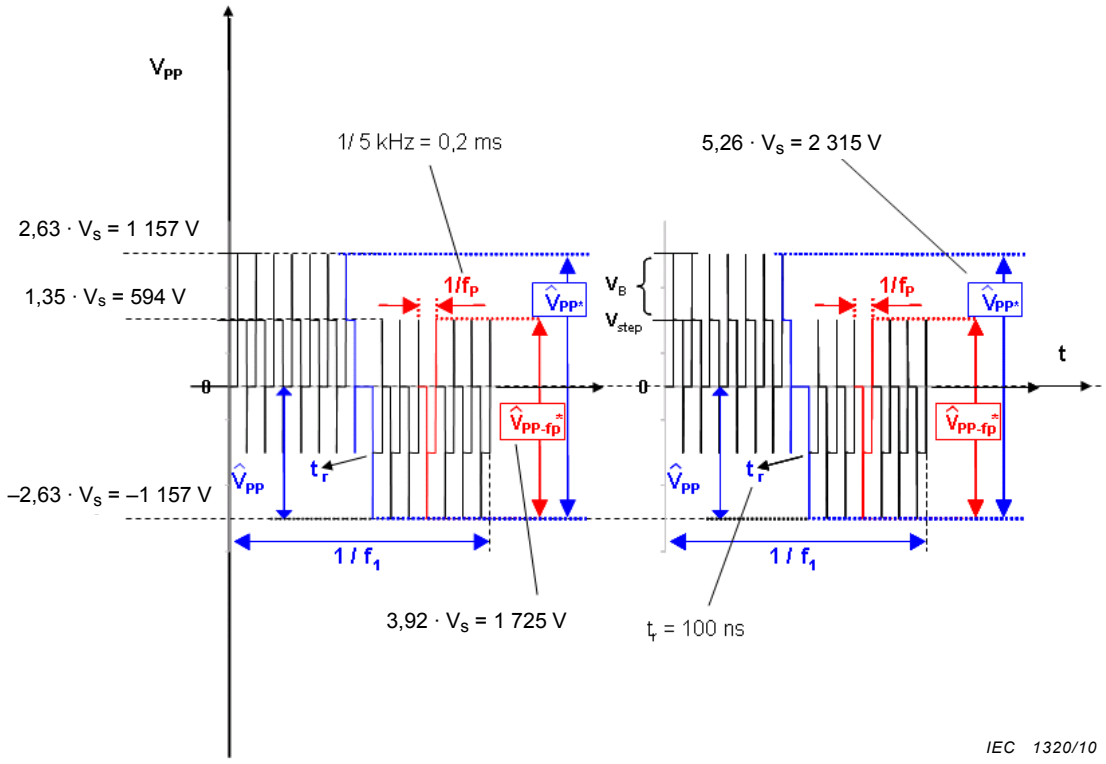


Figure 41 – Resulting phase to phase voltage at the motor terminals for the calculated example under worst case conditions

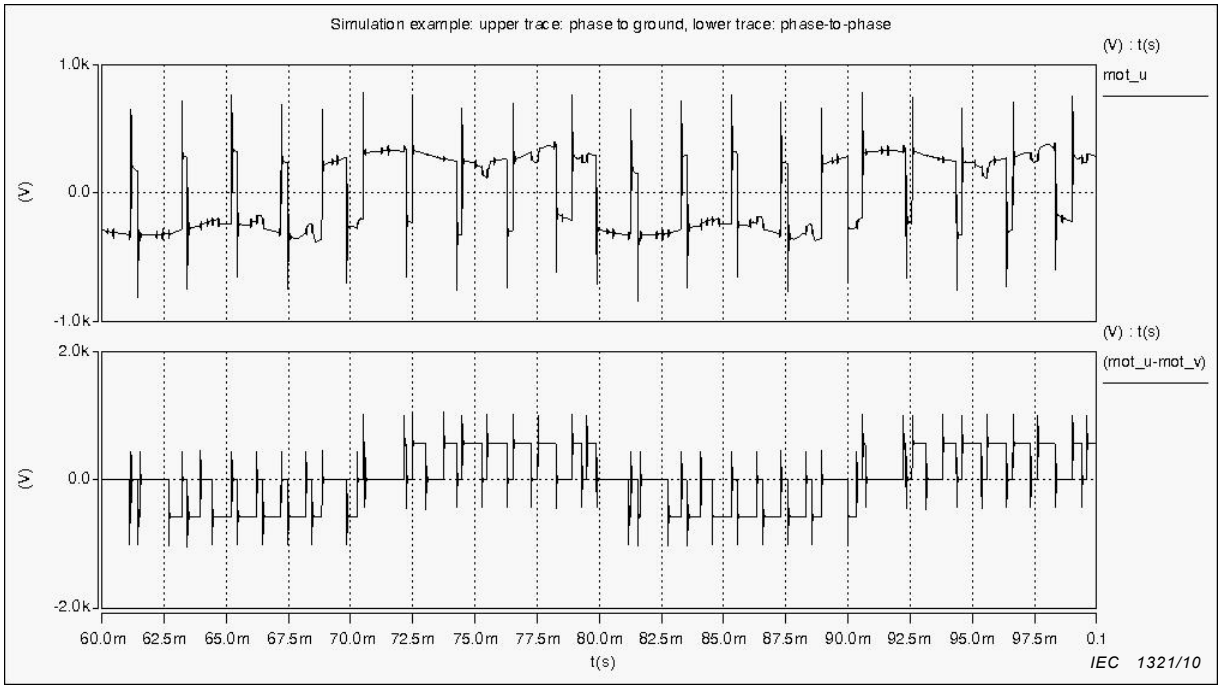


Figure 42 – Example of a simulated phase to ground and phase to phase voltages at the motor terminals (same topology as calculated example, TN- supply system, 50 Hz output frequency, no filters, 150 m of cabling distance, type NYCWY, grounding impedance about 1 mΩ)

Annex A
(informative)
Different types of power supply systems

A.1 Different types of power supply system

The following types of system earthing (TSE) are taken into account with reference to IEC 60364-1.

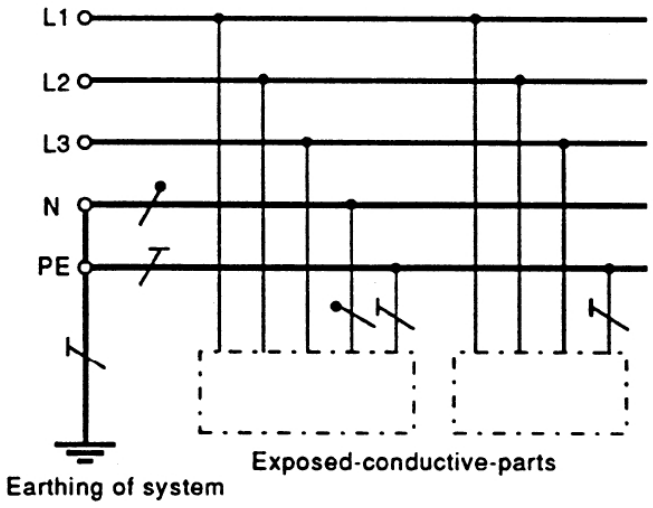
NOTE 1 The codes used have the following meanings:

First letter – Relationship of the power system to earth:
T = direct connection of one point to earth;
I = all live parts isolated from earth, or one point connected to earth through an impedance.

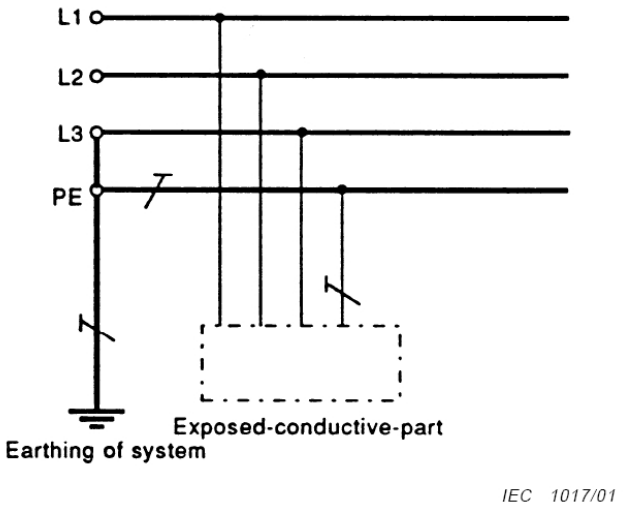
Second letter – Relationship of the exposed-conductive-parts of the installation to earth:
T = direct electrical connection of exposed-conductive-parts to earth, independently of the earthing of any point of the power system;
N = direct electrical connection of the exposed-conductive-parts to the earthed point of the power system (in AC systems, the earthed point of the power system is normally the neutral point or, if a neutral point is not available, a phase conductor).

Subsequent letter(s) (if any) – Arrangement of neutral and protective conductors:
S = protective function provided by a conductor separate from the neutral or from the earthed line (or in AC systems, earthed phase) conductor.
C = neutral and protective functions combined an a single conductor (PEN conductor).

Explanation of symbols for following Figure 5 according to IEC 60617-SN	
	Neutral conductor (N)
	Protective conductor (PE)
	Combined protective and neutral conductor (PEN)

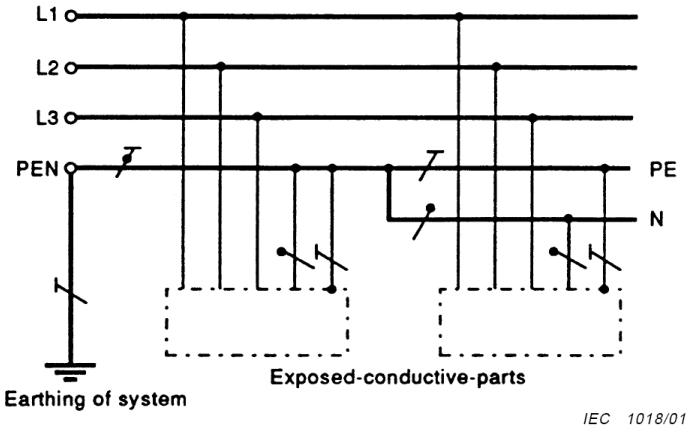


Separate neutral and protective conductors throughout the system

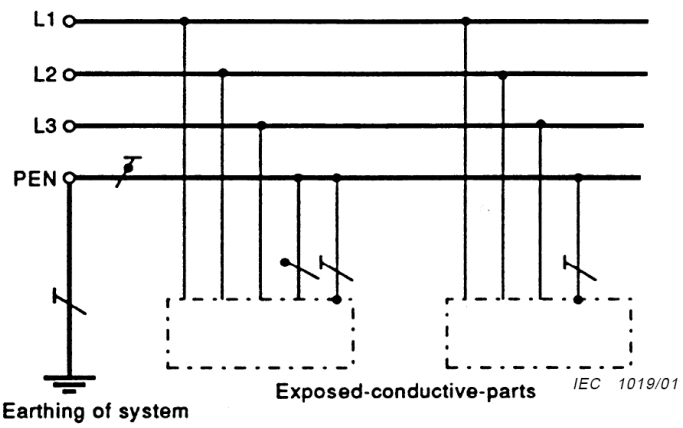


Separate earthed phase conductor and protective conductors throughout the system

Figure A.1 – TN-S system

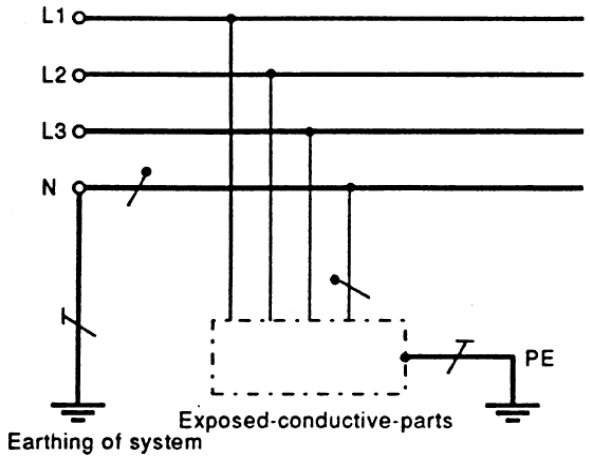


TN-C-S power supply system



TN-C power supply system

**Figure A.2 – TN-C-S power supply system –
Neutral and protective functions combined in a single conductor
as part of the system TN-C power supply system –
Neutral and protective functions combined in a single
conductor throughout the system**



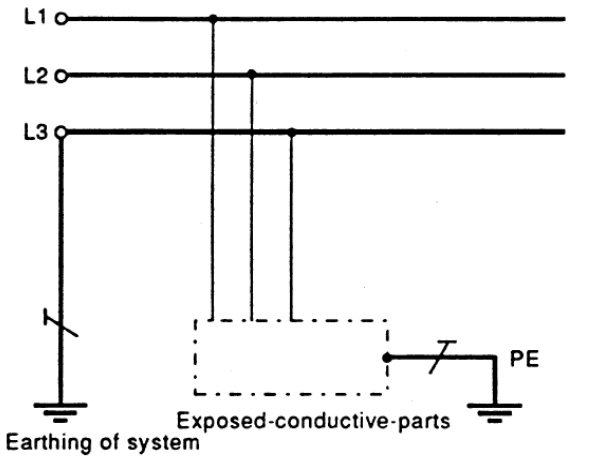
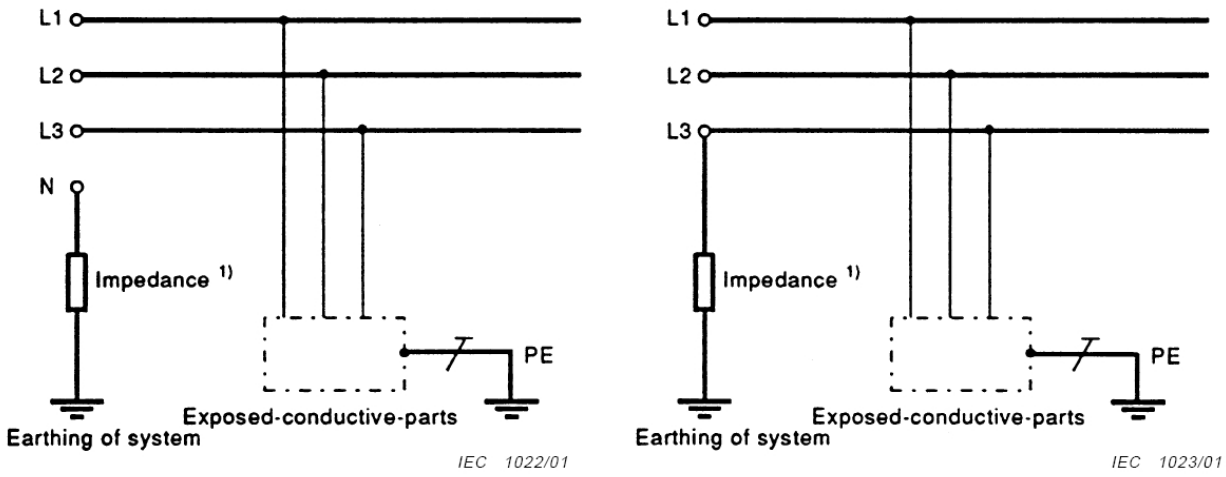


Figure A.3 – TT power supply system

A.2 TT- Type of system earthing

The TT power supply system has one point directly earthed, the exposed-conductive-parts of the installation being connected to earth electrodes electrically independent of the earth electrodes.

The IT power supply system has all live parts isolated from earth or one point connected to earth through an impedance, the exposed-conductive-parts of the electrical installation being earthed independently or collectively or to the earthing of the system (see 411.5 of IEC 60364-4-41:2005).



[1] The system may be isolated from earth. The neutral may or may not be distributed.

Figure A.4 – IT power supply system

A.3 Practical application of grounding

A.3.1 Electrical circuit and parasitic circuit (for high frequencies)

Each part of an electrical circuit provides a stray capacitor to the ground, and sometimes with adjacent circuits.

The identification of these capacitors is mainly done depending on the geometry of circuits. It conducts to models which require some electrical values measurements (currents and voltages) which allow the validation of the models.

In case of an equipment or component, the capacitance values of these stray capacitors are usually about fractional pF up to hundreds pF. But in an installation, the capacitance coming from the cabling may reach values of tens µF or even hundreds of µF.

The components including coil of transformers, coil of inductors, motors provide some capacitance values in a between range.

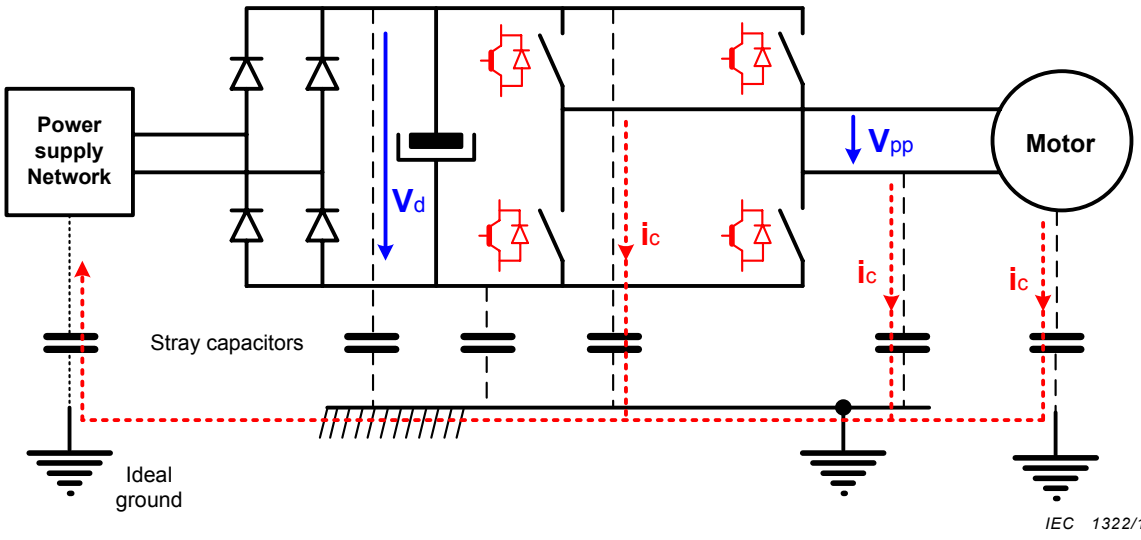


Figure A.5 – Example of stray capacitors to ground potential in an installation

A distinction could be noted between the earthed metal frames and the earthing circuits. It suggests a PDS in which the switching components submit some parts of the circuit to sudden variations of the voltage. These voltage variations lead to the circulation of leakage currents in the stray capacitors.

A.3.2 Influence of the TSE (Type of System Earthing)

According to the description of A.3.2 the type of system earthing can be expected as a high influence on the pathway of capacitive leakage currents.

The Figure A.6 shows the principle of the circulation of leakage currents in a TN TSE. Additional filters placed on the drive, usually at the input, sometimes at the intermediate DC bus section, provide a lower impedance pathway than the pathway going through the main supply network.

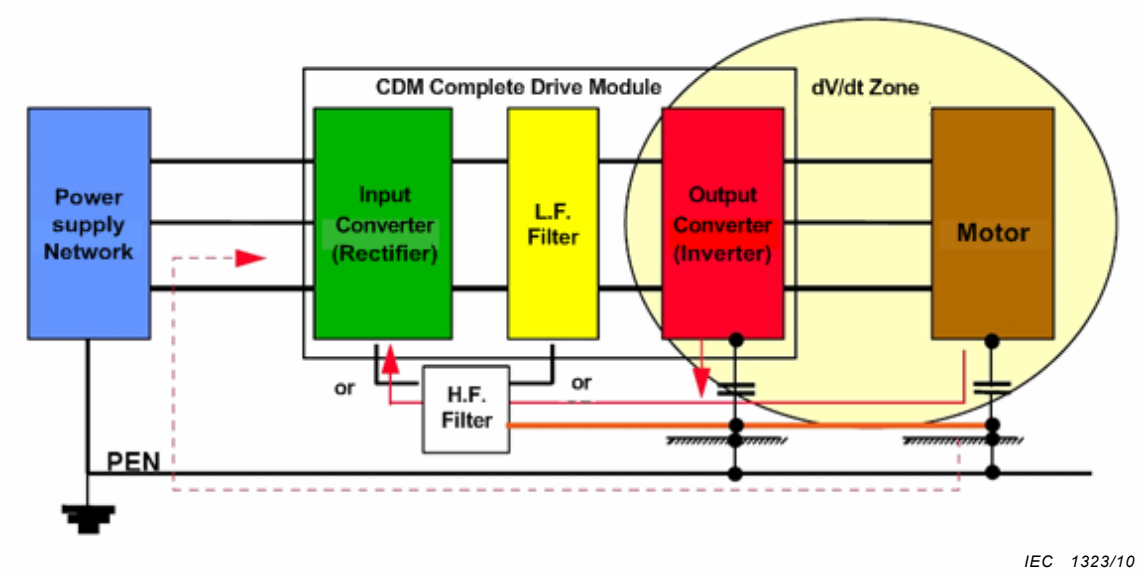


Figure A.6 – Example of a parasitic circuit in a TN type of system earthing

The impedance of the supply network for these common mode currents is different between a TN TSE (Figure A.6) and an IT TSE (Figure A.7). In this IT TSE, the impedance to the Earth can be fixed (High impedance between the neutral point and the earth, intentionally fixed), or not defined (strictly isolated neutral point). In both case, the current pathway make a loop because of the stray capacitors of the installation (cabling of the main supply network, supply transformer).

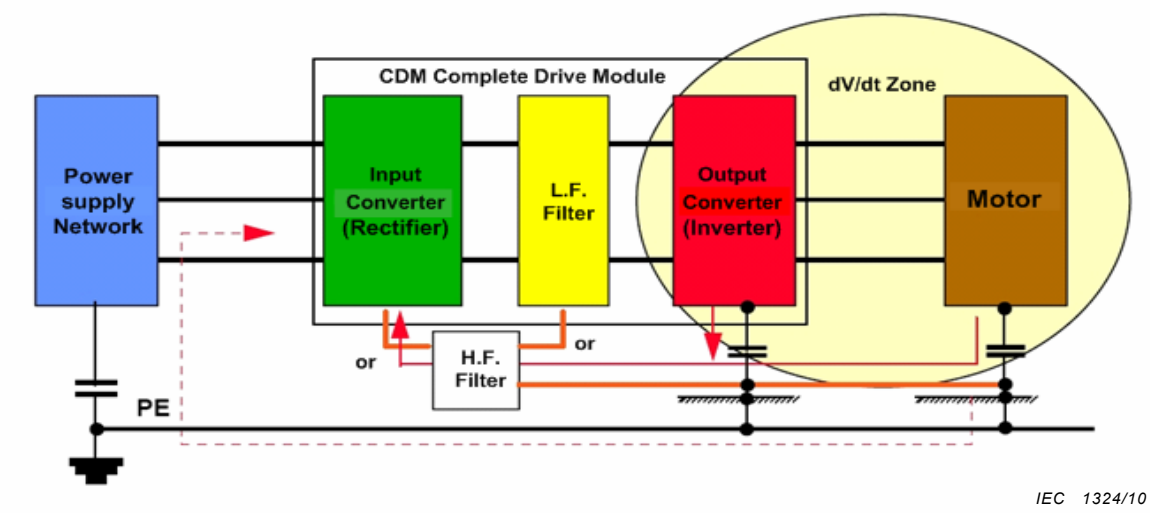


Figure A.7 – Example of a parasitic current flow in an IT type of system earthing

Annex B
(informative)
Inverter voltages

B.1 Inverter voltages

B.1.1 Harmonic content

The inverter section of this document mainly determines peak values of the voltage, which are the most important parameters regarding insulation of motors. By increasing the rms-value also the harmonic content of the waveform might have an influence on the insulation. Table B.1 shows typical approximated values of the total distortion ratio. Out of this value and the fundamental value the rms-value can be calculated.

Table B.1 – Typical harmonic content of the inverter voltage waveform (Total distortion ratio – see IEC 61800-3 for definition)

Number of levels	V_{PP}	V_{PNP}	V_{PSP}
2	51	71	52
3	27	36	25
4	18	29	17
5	13	24	13
6	11	23	11
7	10	22	10

NOTE 1 The given values are in percent of the fundamental.

NOTE 2 The values are valid for full modulation, but without overmodulation, i.e. each level could be fully used. The values increase in case of lower modulation index. They also increase in case of overmodulation.

NOTE 3 The values are mostly determined by the number of levels. The type of modulation and the pulse frequency have only a minor influence on the total harmonic content. The values have been determined with sawtooth PWM modulation with a carrier frequency equal to 11 times the output frequency, where a third harmonic was injected into the carrier signal in order to reach full modulation.

NOTE 4 The type of modulation and the pulse frequency have huge influence on the individual harmonics or interharmonics occurring (amplitude, phase and sequence). Thus only numbers for the total harmonic content can be given, but not for individual harmonics.

NOTE 5 Another effect of voltage harmonics is an increase in temperature, as the voltage harmonics are causing current harmonics. This can not be quantified, as the amount of current harmonics is depending on the individual voltage harmonics, which can not be given according to NOTE 4.

NOTE 6 Most common voltage source inverters are two level, three level or five level. Some additional levels are given, but limited up to seven level.

NOTE 7 All values can be mitigated by filtering (see Clause 8).

NOTE 8 Depending on the grounding system the harmonic content for the phase to ground voltage at the inverter output lies between the values for V_{PNP} and V_{PSP}.

Annex C
(informative)
Output filter performance

C.1 Output filter performance comparison

The performance of the output filter types is compared for differential mode and common mode filters in the following tables:

a) Differential mode

Table C.1 – Comparison of the performance of differential mode filters

	Sine wave filter	dV/dt filter	EMI filter	Output choke
Motor losses	++	--	--	-- *
Acoustic noise	++	--	--	--
Motor winding turn stress	++	++	--	+

++ very effective, + effective, - little effective, -- not effective

*NOTE Output chokes might be designed in a way that they can reduce the motor losses

b) Common mode

Table C.2 – Comparison of the performance of common mode filters

	Sine wave filter	dV/dt filter	EMI filter	Output choke
Motor winding stress	++	+	--	-
Bearing currents	++	+	--	-
EMI noise	++	-	++	--
Thermal stress of the inverter	Depends on concrete application	Depends on concrete application	--	+

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BEMA – GAMBICA Guide

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