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Part 4-3: Interface integrated circuits – Dynamic criteria for analogue-digital converters (ADC)

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SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 4-3: Interface integrated circuits – Dynamic criteria for analogue-digital converters (ADC)

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The text of this standard is based on the following documents:

FDIS	Report on voting
47A/750/FDIS	47A/758/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The list of all the parts of the IEC 60748 series, under the general title *Semiconductor devices – Integrated circuits*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

INTRODUCTION

The use of ADCs has increased significantly in the last few years with the large increase in the use of digital signal processing. The majority of the processing of analogue signals now takes place in the digital domain, and this requires high precision in the conversion of signals from the analogue to the digital form. Consequently, the characterization of ADCs is of great importance.

IEC 60748-4 contains measuring methods for ADCs in which the test conditions are either static or change very slowly. However, some of the characteristics of an ADC can change to some degree with the rate of change of the input signal, and there are other characteristics that cannot be measured except under dynamic conditions. Consequently, a set of dynamic tests is required in order to obtain the response of an ADC when operated under dynamic conditions.

The output of a dynamic test consists of the set of output code values obtained during the test. This record, being the sequence in time of a set of values, gives information in the “time-domain”. The result of applying the Fourier Transform to the record is information that is in the “frequency domain”, and this contains the spectrum of the output over the range of frequencies of interest. In particular, distortion, noise and spurious output frequencies can then be evaluated.

This International Standard introduces a set of dynamic methods, which are now coming into use in industry and which rely mostly on measurements made with sinusoidal input signals, and of which the results are suitable for analysis in the frequency domain. It also includes a further dynamic method that uses a wide-band input signal. For the reasons explained below, industry has shown great interest in this particular method.

Linearity errors of an ADC are dependent on the amplitude of the input signal and its rate of change. Not so well known is that linearity errors also depend on the instantaneous amplitude distribution, i.e. amplitude probability density function (APDF) of the input signal. This source of error is usually a result of localized heating effects in the integrated circuit and is dependent on ADC architecture and internal circuit layout.

Single-frequency signals have an APDF concentrated at the extremes and therefore exaggerate the effect of errors at the ends of the input range compared to those nearer the centre. Conversely, a wide-band signal has an APDF concentrated more around the centre of the input range. A wide-band signal is much closer to the typical input signal in the majority of ADC applications than a single-frequency signal. Therefore, measurements made with such a signal will give more realistic error estimates.

A wide-band signal can be generated from a pseudo-random binary sequence. Although such a signal appears to be noisy, it contains only a set of defined frequencies and is therefore suitable for measuring errors.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 4-3: Interface integrated circuits – Dynamic criteria for analogue-digital converters (ADC)

1 Scope

This part of IEC 60748 specifies a set of measuring methods and requirements for testing ADCs under dynamic conditions, together with associated terminology and characteristics.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60748-4:1997, *Semiconductor devices – Integrated circuits – Part 4: Interface integrated circuits*

IEC 60268-10:1991, *Sound system equipment – Part 10: Peak programme level meters*

3 Terms and definitions

For the purposes of this document, the following definitions, in addition to those found in Chapter II, Clause 2, Terms for category II of IEC 60748-4:1997, apply.

3.1
coherent sampling
process in which the output record contains samples taken from an integral number of input cycles of a repetitive waveform

NOTE In general, this process is limited to the case where the number of input cycles and the number of samples in the record have no common factors.

3.2
equivalent-time sampling
coherent sampling in which consecutive samples of a repetitive waveform, acquired from multiple repetitions of the waveform, are assembled and re-arranged to produce a single record of samples that represent a single repetition of the waveform

NOTE This process is normally used only when the spectrum of the input waveform contains significant amounts of energy at frequencies above half the sampling frequency. It has the result that each frequency in the input appears in the output divided by the number of repetitions. For each successive input cycle, the set of samples is delayed (or advanced) relative to the previous set by a fixed amount.

3.3
(code) transition value
boundary between two adjacent steps

3.4
signal-to-noise-and-distortion ratio
for a pure sine-wave input, ratio of the r.m.s. amplitude of the output signal at the input frequency to the r.m.s. amplitude of all other signals in the output

3.5
(spurious-free) dynamic range
for a pure sine-wave input, ratio of the r.m.s. amplitude of the output signal at the input frequency to the largest r.m.s. amplitude of the output at any other single frequency

3.6
effective number of bits
N_{ef}
practical limit of the resolution of an ADC due to inherent noise and errors

3.7
signal-dependent timing error
effect equivalent to the delay of the instant of sampling, in an ADC, that is proportional to the rate of change of input voltage

NOTE This effect is caused by the inherent voltage-dependent non-linearity of circuit elements in semiconductors.

3.8
spurious frequency
persistent sine wave in the output that is not considered to be a harmonic of the input frequency

3.9
word error rate
probability of an output code having an error not attributable to random noise or to offset, gain, and linearity errors

4 Characteristics

The following characteristics shall be included as characteristics applicable to ADCs and should be read with reference to Chapter III, Section 2, Category II, Clause 4 of IEC 60748-4:1997.

Ref.	Characteristic	Conditions at 25 °C unless specified otherwise	Letter Symbol	Notes	Requirements	
					Max.	Min.
4.1	Settling time	Supply voltages Input step amplitude Specified levels for transition time Clock frequency, as appropriate Conditions at other terminals Tolerance for settling time	t_{tot}		X	
4.2	Long-term settling error		E_{LT}		X	
4.3	Rise and fall times		t_r; t_f		X	
4.4	Limiting rate of change of output (slew rate)		$(\Delta v/\Delta t)_{max}$, SR			X
4.5	Overload recovery times					
4.5.1	Input overload recovery time, where appropriate	Supply voltages Input signal frequency, as appropriate Input signal amplitude Overload signal amplitude and duration Clock frequency, as appropriate Conditions at other terminals	t_{or}		X	
4.5.2	Differential-mode input overload recovery time, where appropriate		t_{ord}		X	
4.5.3	Common-mode input overload recovery time, where appropriate		t_{orc}		X	
4.6	Differential gain, where appropriate	Supply voltages Input signal frequency, as appropriate Input signal amplitude Clock frequency, as appropriate DC input levels Conditions at other terminals Desired accuracy	A_{dif}		X	
4.7	Differential phase, where appropriate		ϕ_{dif}		X	
4.8	Total harmonic distortion	Supply voltages Input signal frequency, as appropriate Input signal amplitude Clock frequency, as appropriate Highest harmonic excluded from noise, if not 10th Conditions at other terminals	THD		X	
4.9	Spurious-free dynamic range		SFDR			X
4.10	Signal-to-noise-and-distortion ratio		SINAD			X
4.11	Effective number of bits		N_{ef}			X
4.12	Signal-to-noise ratio		SNR			X
4.13	Noise floor		NF		X	
4.14	Signal-dependent timing error		E_{SDT}		X	

5 Measuring methods

5.1 Dynamic testing with sinusoidal signals

The following methods are to be read with reference to Chapter IV, Section 3, Category II, Group I of IEC 60748-4:1997. All references below to IEC 60748-4:1997 apply to this clause.

5.1.1 Dynamic testing of ADCs – General requirements

5.1.1.1 Purpose

To specify the general requirements for measuring the characteristics of an ADC under dynamic conditions.

5.1.1.2 Circuit diagram

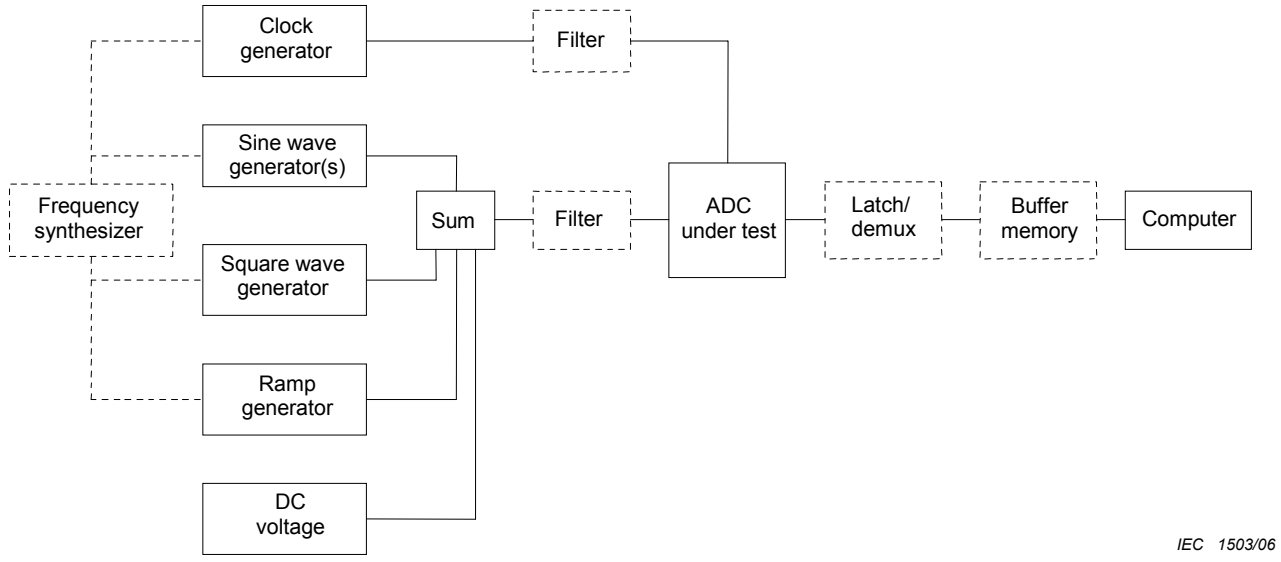

Figure 1 – Test arrangement for measurements on ADCs under dynamic conditions

Optional elements are shown in broken outline.

5.1.1.3 Circuit description and requirements

– Case a) sine wave input

The input voltage generator shall provide an accurate sinusoidal waveform with adjustable and stable amplitude and frequency.

– Case b) step input

The input voltage generator shall provide a stepped wave, usually a square wave, without droop, and with adjustable and stable levels, duty-cycle and periodicity.

– Case c) linear input ramp

The input voltage generator shall provide an accurate linear rising and/or falling waveform with adjustable and stable amplitude, duty-cycle and periodicity.

– All cases:

Precautions shall be taken to avoid coupling between the sampling clock and the input circuits, and between the output and input circuits, and the networks used to combine input signals shall be designed to minimize any stray reactive elements that could affect the bandwidth of applied signals.

Noise at the input should be small compared with the output noise that is generated within the ADC, and preferably no larger in magnitude than the noise that results from the quantization process, i.e. significantly less than 1 LSB in magnitude. When necessary, and normally only for sine waves, input noise can be reduced by passing the signal through a low-pass or band-pass filter. The latter may also be used to reduce any frequency instability in the signal.

Any impurity in the signal waveform and instability in its frequency should be low enough not to affect the accuracy of the measurements. Similarly, any instability in the frequency (jitter) of the clock signal should be equally low. Ideally, the input signal and the clock signal should be synchronized from a common source.

The adjustment range of the input voltage should be such that, at its maximum excursion, the most positive and most negative peaks exceed the working range of the ADC, but do not exceed its limiting input voltages.

Equipment shall be included for the adjustment of offset and gain points of adjustable converters.

For some measurements, both step and sinusoidal inputs are applied together to the ADC.

The recording equipment should be capable of storing each output code obtained during the test duration. In cases where this is physically not possible, or accuracy is reduced in a long test duration due to frequency instability, then the test may be divided into a set of segments of equal length, where the record of each segment is analysed separately, provided that for each segment the phase of the input signal at its start is either randomly chosen or uniformly distributed within the range 0..2π.

For analysis of the histogram of the ADC output, the recording equipment shall count the number of occurrences of each individual output code value during the test. The test duration should be such that each output code value appears enough times to achieve the required accuracy (see Figures 3 and 4 and also Annex A) to determine a suitable number.

For analysis of the spectrum of the ADC output, the recording equipment shall record the code value of each individual sample during the test.

5.1.1.4 Special precautions regarding accuracy

Note the comments above regarding signal purity, frequency stability, and input noise.

In order that each test is carried out with coherent sampling, the duration of each segment of the test shall be set to an integral number of input cycles. However, the periodicity or frequency of the input waveform and that of the sampling clock shall not have a common factor, thus

$$f_i = f_s \cdot J/M \quad (1)$$

where

f_i is the input frequency;

f_s is the sampling frequency;

M is the number of samples in a test record;

J is the number of input periods in a test record, an integer,

the fraction J/M shall be irreducible.

If the requirement for J to be an integer is not met, then the method of analysis will give large errors. Although there is a mathematical procedure that can extract reasonably accurate results when J is not an integer, its use is outside the scope of this standard.

In general, J will be an odd number greater than 1, and M an even number. For certain cases, detailed below (see 5.1.1.5), M should be a power of 2.

Ideally for analysis of the spectrum, each output code should appear at least once in the output record. There are $2N$ possible output codes, when N is the number of bits. In the case of sine-wave input (and a linear ADC), for each output code to appear at least once, it is required that

$$M \geq \pi \cdot 2N \tag{2}$$

When it is required that the input frequency should be very close to a particular input frequency (f_i), then proceed as follows: find an integer, r, near to f_s/f_i, let J equal the integral part of M/r, then

$$fi = fs \cdot J/(r \cdot J - 1) \tag{3}$$

and

$$= r \cdot J - 1 \tag{4}$$

5.1.1.4.1 Histogram testing

For tests that determine the transfer characteristic, and thereby the linearity errors, the dynamic method involves obtaining a histogram of output codes. Provided that the input signal is sufficiently free from error, accuracy increases with the number of samples recorded for each code value. Specific requirements to achieve the required accuracy are given in the corresponding method.

5.1.1.4.2 Spectral analysis

For spectral analysis, provided that M is sufficient to give at least one sample for each code value, the accuracy increases with $\sqrt{M}$, but the error due to frequency instability increases with the product of both J and M, thus J should not be large. Where an increase in accuracy is desired, then multiple records, starting at different points in the input waveform, may be used to give an improvement proportional to $\sqrt{R}$, where R is the number of records. In this case, it is usual to compute the required terms separately for each record and take the average over all the records of each term.

To take account of variations in actual step width, frequency instability and jitter, the value of M should be increased from the theoretical minimum, so that

$$M \geq \frac{\pi \cdot 2^N}{\left(1 - K \cdot \sigma_\phi\right) \cdot \left(1 - \left|E_{Dmax}\right|\right)} \tag{5}$$

where

N is the number of bits of the ADC;

K is the number of standard deviations that give the required confidence level (see Table 1);

σ_ϕ is the r.m.s. value of combined phase jitter, referred to the clock period;

E_{Dmax} is the maximum value of differential linearity error.

Table 1 – Confidence level versus range of variable (in standard deviations)

Confidence level p (%)	80	90	95	98	99	99,5
Range multiplier K	1,282	1,645	1,960	2,326	2,576	2,807

5.1.1.5 Calculations using the Fourier Transform

The Discrete Fourier Transform (DFT) of the set of samples in a record is given by

$$X[n] = \sum_{k=0}^{M-1} x[k] \cdot e^{(-j2\pi.n.k/M)} \tag{6}$$

where

M is the number of samples in the record;

$x[k]$ is the sample number k;

$X[n]$ is the spectral line number n of the transform, representing the frequency given by $f_S \cdot n / M$.

The frequency f of a spectral line is given by

$$f = f_S \cdot n/M \tag{7}$$

To choose the spectral line corresponding to the input frequency F_i, set $n = J$ (see 5.1.1.4). See Annex A for details on evaluating the DFT.

The spectrum of interest normally ranges from n = 0 (d.c.) to $n = M/2 - 1$ (where $M/2$ is the Nyquist frequency). The range from $M/2 + 1$ to M is a mirror of the lower half and should be ignored. In general, the particular frequencies of interest are the fundamental and the 2nd to 10th harmonics for the case of a single input frequency, or the two fundamentals and the lower intermodulation products for the case of two input frequencies.

Any frequencies in the input signal that are above the Nyquist frequency will also appear in the range 0..$M/2 - 1$ and, therefore, shall be excluded from the input.

For the case where M is a power of 2, but only in this case, the Fast Fourier Transform (FFT) can be used to obtain the full spectrum very rapidly. This version of the procedure reduces the number of computations by the factor of $M/\log_2(M)$. Thus when M = 4 096, this factor is approximately 340.

It follows that where the full spectrum is required, and particularly when determining noise power, M should be an exact power of 2 so that the FFT may be used, whereas for the evaluation of a small number of individual frequencies, M may be chosen otherwise and the DFT used.

5.1.2 Differential gain and phase (A_{dif}, ϕ_{dif})

5.1.2.1 Purpose

To measure the change of gain and phase with change of mean d.c. input level to an ADC.

5.1.2.2 Circuit diagram

See Figure 1.

5.1.2.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a sinusoidal signal superimposed on a d.c. voltage. The d.c. voltage shall be capable of being set to any specified value within the full-scale range of the ADC, either manually or automatically with a pre-set waveform generator. The actual d.c. levels and signal amplitude used should be chosen so as to avoid peak clipping.

For one particular application, d.c. levels of 1/7, 2/7, 3/7, 4/7, 5/7, and 6/7 of full scale are used with the sinusoidal signal having a peak amplitude of 1/7 full scale.

5.1.2.4 Special precautions

The amplitude and phase of the a.c. component of the input signal shall be kept constant during the measurement and shall be independent of the value of the d.c. component of the input signal.

5.1.2.5 Measurement procedure

The number of samples in a record necessary to achieve the desired accuracy is calculated as explained in the general requirements, and the exact value of either (or both) the input and clock frequencies, as appropriate, is calculated for the chosen record length.

The temperature of the integrated circuit being measured is set to the specified value.

The input and output terminals, as well as the remaining terminals, are connected as specified. The power supplies and any other additional networks are connected as specified.

Unless otherwise specified, adjustments shall be made to minimize the offset and gain errors as described in 15.1.4 of IEC 60748-4:1997.

The a.c. component of the input signal is set to the specified amplitude and frequency, and the clock frequency is set as specified.

All relevant control input signals shall be applied.

The d.c. input voltage is set to the first of the specified values, and the record of the resulting output codes is stored for subsequent analysis. This action is then repeated for each of the remaining specified d.c. values, ensuring, where possible, that each record starts at the same point on the input sine wave.

Each record is processed using the Fourier Transform to obtain the amplitude and phase of the component at the fundamental input frequency. If the phase of the input signal at the starting point of a subsequent record is not the same as for the first record, then the calculated phase shall be corrected by the amount of its difference before being used as follows.

The differential gain is given by the absolute maximum of the differences in gain between any two records.

The differential phase is similarly given by the absolute maximum of the differences in phase between any two records.

5.1.2.6 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- DC input levels.
- Clock frequency, as appropriate.
- Conditions at other terminals.
- Desired accuracy.

5.1.3 Signal-to-noise-and-distortion ratio, signal-to-noise ratio, noise floor, effective number of bits (N_{ef})

5.1.3.1 Purpose

To measure the ratio of signal power to residual power, to measure the ratio of signal power to noise power, after excluding harmonically-related components, to measure the mean noise amplitude, in the output of an ADC, and to determine its effective resolution when taking account of inherent noise and error.

5.1.3.2 Circuit diagram

See Figure 1.

5.1.3.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a sinusoidal signal.

5.1.3.4 Special precautions

Any inaccuracy in the input signal or the clock period due to noise, frequency or amplitude instability, etc. will contribute to the output noise and should therefore be minimized. The use of filters is recommended to reduce the effect of such sources of error.

5.1.3.5 Measurement procedure

The number of samples in a record and, if required, the number of records needed to achieve the desired accuracy are calculated as explained in the general requirements, and the exact value of either (or both) the input and clock frequencies, as appropriate, is calculated for the chosen record length.

The temperature of the integrated circuit being measured is set to the specified value.

The input and output terminals, as well as the remaining terminals, are connected as specified. The power supplies and any other additional networks are connected as specified.

Unless otherwise specified, adjustments shall be made to minimize the offset and gain errors as described in 15.1.4 of IEC 60748-4:1997.

The input signal is set to the specified amplitude and frequency, and the clock frequency is set as specified.

All relevant control input signals shall be applied.

The record of the resulting output codes is stored for subsequent analysis. Where appropriate, further records are obtained and stored for analysis. With multiple records, accuracy is improved by using, for each frequency, the root mean square of the set of terms for that frequency obtained from the Fourier Transform of each record.

5.1.3.5.1 Signal-to-noise-and-distortion ratio

The value of the signal-to-noise-and-distortion ratio is given by r.m.s. output signal/r.m.s. residual signals.

$$SINAD = \sqrt{\frac{X[J]^2}{\sum_{n=2J}^{n=M/2-1} X[n]^2}} \tag{8}$$

It is usually expressed as the ratio of their powers (output signal power/residual power), where the signal power is obtained as below, and the residual power is calculated by one of the methods below.

5.1.3.5.1.1 Signal power measurement

The amplitude and phase of the output at the input frequency (f_i) are obtained from the Fourier Transform of the record(s) (see formulae given earlier). The r.m.s. output signal is given by the amplitude of this component at f_i.

5.1.3.5.1.2 Residual power measurement – Method a

The instantaneous value of the output at the input frequency is calculated for each successive sample in the record and subtracted from it.

The residual power is given by the mean of the squares of these differences.

5.1.3.5.1.3 Residual power measurement – Method b

The amplitude of each frequency is obtained from the Fourier Transform. The residual power is given by the sum of the squares of all the terms after excluding the d.c. term and the term for the input frequency (f_i).

5.1.3.5.2 Signal-to-noise ratio

The value of signal-to-noise ratio is given by r.m.s. output signal/r.m.s. noise.

$$SNR = \sqrt{\frac{X[J]^2}{\sum_{n=11..J}^{n=M/2-1} X[n]^2}} \tag{9}$$

It is usually expressed as the ratio of their powers, where the noise power is obtained by one of the methods below.

5.1.3.5.2.1 Signal power measurement

The amplitude of the input frequency is obtained from the Fourier Transform and used to give the value of signal power, as in 5.1.3.5.1.1, above.

5.1.3.5.2.2 Noise power measurement – Method a

The amplitude of each frequency is obtained from the Fourier Transform. The d.c. component, the fundamental (f_i) and the 2nd to 10th harmonics (unless otherwise specified) are excluded. The noise power is given by the sum of the squares of all the remaining terms.

Harmonics higher than the 10th should also be excluded if their values are included in total harmonic distortion (see 5.1.4.4.1).

5.1.3.5.2.3 Noise power measurement – Method b

The amplitude and phase of the fundamental and significant harmonic frequencies are obtained from the Fourier Transform. Using the values given by the transform, these frequencies are removed from the record by subtracting the instantaneous value of each from each sample in the record to give the effective noise in each sample.

The noise power is given by the mean of the sum of the squares of these effective noise samples.

5.1.3.5.2.4 Noise power measurement, Method c

Two separate records are obtained under identical conditions. The effective noise is the difference, sample by sample, between the two records.

The noise power is given by the mean of the sum of the squares of the differences.

5.1.3.5.3 Noise floor

The noise floor may be obtained by either of the methods below. It is usually expressed as a power relative to the power of a full-scale sine wave.

5.1.3.5.3.1 Noise floor – Method a

The noise spectrum in the output record is obtained by the method described in 5.1.3.5.2.2. The noise floor, as a power, is given by the mean value of the sum of the squares of the noise terms.

$$NF = \frac{\sum_{n=11}^{n=M/2-1} X[n]^2}{M/2 - 12} \qquad (10)$$

5.1.3.5.3.2 Noise floor – Method b

The effective noise in each sample of the record is obtained by the method in either 5.1.3.5.2.3 or 5.1.3.5.2.4, above, and the noise power is calculated.

The noise floor is given by the noise power divided by the square root of the number of frequencies in the Fourier Transform that contribute to the noise power, i.e. the number of samples less the number of significant components in the output spectrum.

$$NF = \frac{\sum_{k=1}^{M} [x[k] - x_1[k]]^2}{\sqrt{M/2 - 12}} \quad (11)$$

5.1.3.5.4 Effective number of bits

The effective number of bits should be obtained from the signal-to-noise-and-distortion ratio with a full-scale input signal. However, it is usually measured with a smaller input signal and the resulting ratio is then corrected by the ratio of the r.m.s. signal amplitude to the full-scale range.

N_{ef} is given by (signal-to-noise-and-distortion ratio – r.m.s. signal to full-scale ratio - crest factor of quantizing error + crest factor of test signal)/6.02,

where all the quantities are expressed in dB.

$$N_{ef} = \frac{SINAD - V_{in}/V_{FS} - CF[error] + CF[signal]}{6.02} \quad (12)$$

5.1.3.6 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- Clock frequency, as appropriate.
- Highest harmonic excluded from noise, if not 10th.
- Conditions at other terminals.

5.1.4 Total harmonic distortion, spurious-free dynamic range, signal-dependent timing error

5.1.4.1 Purpose

To measure the relative power of the harmonics caused by distortion of an input signal, to determine the ratio of the output signal at the fundamental frequency to the largest signal at any other single frequency, in the output of an ADC, and to determine the amount of error related to the rate of change of the input.

5.1.4.2 Circuit diagram

See Figure 1.

5.1.4.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a sinusoidal signal.

5.1.4.4 Measurement procedure

The procedure in 5.1.3.5 is followed, and one or more output records obtained.

5.1.4.4.1 Total harmonic distortion

From the Fourier Transform of the output record, or the average of the transforms of multiple records, the amplitude of the output signal at the fundamental frequency is obtained. The total harmonic distortion is given by the square root of the sum of the squares of the amplitude of each harmonic from the 2nd to the 10th (unless otherwise specified). See also 5.1.3.5.2.2 for the exclusions.

The total harmonic distortion is given by r.m.s. harmonic components/r.m.s. signal.

$$THD = \sqrt{\frac{\sum_{h=2}^{10} X[h]^2}{X[1]^2}} \tag{13}$$

5.1.4.4.2 Spurious-free dynamic range

The spectrum is analysed over the full range of interest to determine if there are spurious frequencies present, i.e. at a level not attributable to noise alone.

From the Fourier Transform of the output record, or the average of the transforms of multiple records, the amplitude of the output signal at the fundamental frequency is obtained. From all the other frequencies present, the amplitude of the largest is noted.

The spurious-free dynamic range is given by the r.m.s. signal/r.m.s. largest single other component.

$$SFDR = \frac{X[J]}{Max_{n=2}^{n=M/2-1}[X[n]]} \tag{14}$$

5.1.4.4.3 Signal-dependent timing error

The spurious-free dynamic range is measured over a range of frequencies in the region of the cut-off frequency, using a constant input amplitude. The value of spurious-free dynamic range divided by the frequency of measurement is recorded and the frequency at which this value is a minimum is noted.

The signal-dependent timing error is given by the inverse of this frequency.

5.1.4.5 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- Clock frequency, as appropriate.
- Conditions at other terminals.
- Highest harmonic included, if not 10th.

5.1.5 Input overload recovery time, common-mode input overload recovery time

5.1.5.1 Purpose

To measure the time interval needed, after the removal of a signal input overload or a common-mode input overload, for the ADC to return to its normal operating characteristics.

5.1.5.2 Circuit diagram

See Figure 1.

5.1.5.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a sinusoidal signal, together with a step signal for the overload pulse. For measurement of input overload recovery time, the step signal is superimposed on the sinusoidal signal as a single-ended input signal and, for the common-mode input recovery time, it is superimposed as a common-mode input signal.

The amplitude of the overload pulse shall not exceed the limiting value.

5.1.5.4 Measurement procedure

The number of samples in a record necessary to achieve the desired accuracy is calculated as explained in the general requirements, and the exact value of either (or both) the input frequency or the clock frequency, as appropriate, is calculated for the chosen record length.

The temperature of the integrated circuit being measured is set to the specified value.

The input and output terminals, as well as the remaining terminals, are connected as specified. The power supplies and any other additional networks are connected as specified.

Unless otherwise specified, adjustments shall be made to minimize the offset and gain errors as described in 15.1.4 of IEC 60748-4:1997.

The input signal is set to the specified amplitude and frequency, and the clock frequency is set as specified. The amplitude and duration of the overload pulse are set as specified. All relevant control input signals are then applied.

The overload pulse is applied part of the way through the test record.

Using the Fourier Transform, or otherwise, the best-fit amplitude and phase of the output at the fundamental frequency are obtained from that part of the record before the overload pulse is applied. The resulting sine wave is then extrapolated to the end of the record.

If the noise in the output could affect the accuracy, then the average, sample by sample, of several records should be used for comparison with the extrapolated sine wave.

The input overload recovery time or the common-mode input overload recovery time, as appropriate, is given by the time period from the end of the overload pulse to the point in the record where the output samples no longer deviate from the extrapolated wave by more than the specified tolerance.

To check on the accuracy obtainable, the procedure above is repeated but without the overload pulse. The deviation of the output samples from the extrapolated sine wave gives the limit to the accuracy that may be obtained.

5.1.5.5 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- Overload signal amplitude.
- Overload signal duration.
- Clock frequency, as appropriate.
- Conditions at other terminals.
- Tolerance.

5.1.6 Limiting rate of change of output (slew rate), output transition times, overshoot, settling time, settling error

5.1.6.1 Purpose

To measure the response of an ADC to a step input, i.e. to measure the maximum rate of transition of the output, the output rise and/or fall time, the overshoot, the settling time and the long-term settling error.

5.1.6.2 Circuit diagram

See Figure 1.

5.1.6.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a step waveform with adjustable amplitude and with rise and fall times that are short compared with the expected rise and fall times of the ADC under test. The pulse duration shall exceed the duration of each record.

For the transient tests, sufficient records should be taken under identical conditions which are then averaged, sample by sample, to minimize errors due to noise in the output. For the settling time and the long-term settling error, to minimize the effect of noise, a moving average of consecutive output codes should be used from one continuous record. This technique is not appropriate to the measurement of transition times due to the changes in slope around the measurement points.

If the minimum time between consecutive samples is not small compared with the expected rise or fall time, then equivalent-time sampling should also be used to produce a record with sufficient samples during the output transition to give the required accuracy.

5.1.6.4 Special precautions

The input signal both before and after the step shall be maintained sufficiently steady so as not to introduce errors in the output signal other than internally generated noise.

5.1.6.5 Measurement procedure

The temperature of the integrated circuit being measured is set to the specified value.

The input and output terminals, as well as the remaining terminals, are connected as specified. The power supplies and any other additional networks are connected as specified.

Unless otherwise specified, adjustments shall be made to minimize the offset and gain errors as described in 15.1.4 of IEC 60748-4:1997.

The number of input cycles is set as required, the step amplitude is set as specified and the clock frequency is set as specified. All relevant control input signals are then applied.

For all the measurements, the output codes corresponding to the two stable levels of the step wave shall be noted first and used to determine the output code values that represent the specified levels for the measurement of rise, fall, and settling times. These values can include fractional parts.

The precise instant when the output reaches a specified value is obtained by interpolation between the nearest samples in the output record, after the effect of noise has been minimized.

5.1.6.5.1 Case a) limiting rate of change of output (slew rate)

Starting with a low-level step input, the maximum rate of change of the output is obtained from the averaged record of the output codes. Successive measurements are made with the input amplitude increased each time until the maximum rate of change no longer increases.

The limiting rate of change of output is given by the largest of the values obtained.

This value shall be expressed as the time required to traverse the full-scale output range at this rate of change.

5.1.6.5.2 Case b) output transition time, overshoot

Using the averaged record of output codes, the two instants when output reaches the first specified level and the second specified level, are noted. Unless otherwise specified, these two levels are 10 % and 90 % of the output step change.

The output transition time (rise time or fall time, as appropriate) is the interval between these two times.

The record is then examined to determine if there is any overshoot after the output transition or any deviation from the starting level before the output transition (i.e. precursor). If either or both exist, then its magnitude as a fraction of the output step is noted.

5.1.6.5.3 Case c) settling time

The input step signal is applied and then held in its final level long enough for the output of the ADC to recover from any overshoot.

Using the averaged record of output codes, the instant when the output reaches the 50 % level of the output step is noted. The instant when the output last enters the specified tolerance band around its final level is then noted.

The settling time is the interval between these two times.

5.1.6.5.4 Case d) long-term settling error

The test duration shall be 1 s, unless otherwise specified.

The input step is applied and then held in its final level for the duration of the test. The output codes are recorded after the output step has ended. The moving averages of consecutive output codes are then examined.

The value of the averaged output code that represents the steady output level after the settling time is noted. The value of the averaged output code value after 1 s is then noted.

The long-term settling error is the difference between these two code values expressed as a fraction of the step amplitude.

5.1.6.6 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input step amplitude.
- Specified levels for transition time.
- Clock frequency, as appropriate.
- Conditions at other terminals.
- Tolerance for settling time.

5.2 Dynamic tests with wide-band signals

5.2.1 Noise power, total distortion, quantization noise

5.2.1.1 Purpose

To measure the distortion and the noise in the output of an ADC, with a wide-band input signal, where measurements are made of total distortion and noise, total random error and total random noise.

5.2.1.2 Circuit diagram

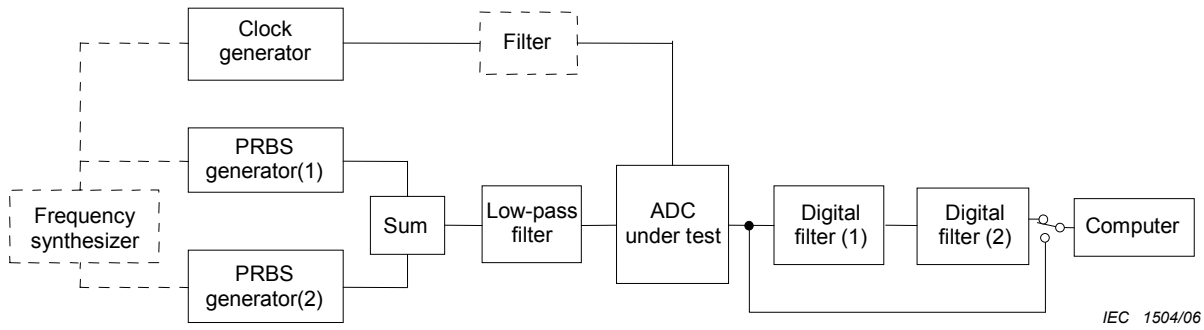

Figure 2 – Test arrangement for measurements on ADCs, using wideband signals

5.2.1.3 Circuit description and requirements

The two pseudo-random binary sequence generators (PRBS) (see Annex B) shall each be designed to produce a set of harmonics with a near-uniform spectrum, and the two repetition rates (i.e. cycle lengths) preferably shall not have a common factor. Use of a single-bit output avoids the possible glitch errors that could occur when using the full word value of the shift register (i.e. all output bits fed into a DAC).

The summing network shall not introduce any non-linearity or other types of error. Where there may be a significant difference in the average power in the two spectra, then appropriate attenuators should be included to produce nominally equal power in each.

The low-pass filter should remove all frequencies above the Nyquist frequency so that there are no aliasing errors, see 5.1.1.5, that could affect the behaviour of the ADC.

Each digital filter (see Annex B) removes the fundamental frequency and all the harmonics generated by the corresponding PRBS, including the components of noise at these frequencies. The filtered output therefore consists only of the noise that is not related to these frequencies. Since a digital filter combines two data streams that contain uncorrelated noise, the noise content in its output is 3 dB larger than at the input.

The record of the output should start after the delay that the analogue input filter and the two digital filters introduce, i.e. after the initial transients have fallen to an insignificant level.

The record length should be at least the sum of the lengths of the two sequences and may extend up to the product of their lengths, after which the pattern repeats.

The clock signal applied to the ADC shall be synchronized with the clock signal applied to the PRBSs for certain measurements, see below.

5.2.1.4 Measurement procedure

The temperature of the integrated circuit being measured is set to the specified value.

The input and output terminals, as well as the remaining terminals, are connected as specified. The power supplies and any other additional networks are connected as specified.

Unless otherwise specified, adjustment shall be made to minimize the offset and gain errors as described in 15.1.4 of IEC 60748-4:1997.

The clock frequency is set as specified, and all relevant control input signals are applied.

An output record is obtained and the r.m.s. output power calculated for the following four cases.

5.2.1.4.1 Case a) total noise and distortion

The clock signals are synchronized, and both PRBSs operate.

5.2.1.4.2 Case b) total random error

The clock signals are not synchronized, and one of the PRBSs is switched off.

5.2.1.4.3 Case c) random noise

The clock signals are synchronized and one of the PRBSs is switched off.

5.2.1.4.4 Case d) total output power

The clock signals are synchronized, both PRBSs operate and the two digital filters are bypassed.

Let

P_E be the value of total noise and distortion power, obtained in case a);

P_q be the total random error power, obtained in case b);

P_r be the random noise power, obtained in case c); and

P_O be the total output power, obtained in case d);

P_n be the quantization noise.

Then

signal power equals $P_O - P_E$;

total noise and distortion power equals P_E;

noise power equals P_q;

quantization noise (P_n) equals $P_q - P_r$;

non-linearity error equals $P_E - P_q$;

signal-to-noise and distortion ratio equals $(P_O - P_E)/P_E$.

5.2.1.5 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input step amplitudes.
- Clock frequencies, as appropriate.
- Conditions at other terminals.

5.2.2 Void

5.3 Linearity error of a linear ADC (E_L) ($E_{L(adj)}$) (E_T)

Subclauses 5.3.1 and 5.3.2 supplement Clause 15 of IEC 60748-4:1997.

5.3.1 Method c (dynamic operation, with linear ramp waveform)

5.3.1.1 General purpose

See the first two paragraphs (cases A, B and C) of Clause 15 of IEC 60748-4:1997.

5.3.1.2 Circuit diagram

See Figure 1.

5.3.1.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a linear ramp waveform.

5.3.1.3.1 Determining the conditions to meet the requirements for accuracy

The input is overdriven sufficiently that, after allowing for noise, the lowest and highest code values will always appear in each input cycle. Appropriate values of overdrive are given in 5.3.2.3.1 below. The test duration, i.e. the number of samples in a record and the number of records, is set so that the count of samples for each of the other code values is not less than the minimum that gives the required accuracy for determining each transition value.

Suitable values for the number of samples in a record and the number of records can be obtained from Figure 3 below. Refer to Annex A for the derivation of the curves.

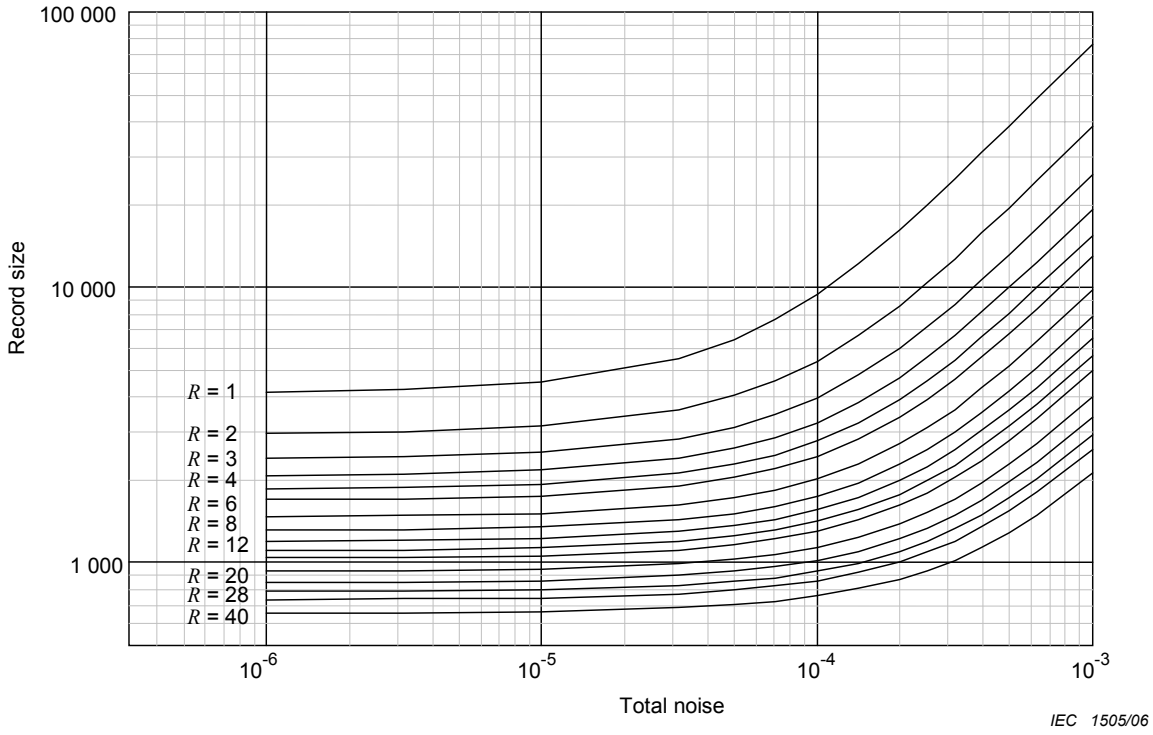

Figure 3 – Record size versus total noise, for various numbers of records, ramp waveform input

The curves in Figure 3 refer to the case of N = 10, D = 1, K/B = 8, c = 1,01. Since R is proportional to $D{\cdot}(2N \cdot K/B)^2$, and M is proportional to c, suitable values for R and M can be obtained for other values of D, N, K, B, and c

where

R is the minimum number of records;

D is 1 for linearity error, 2 for differential linearity error;

N is the number of bits of the ADC;

K is the number of standard deviations that give the required confidence level (see Table1);

B is the desired tolerance as a fraction of the step width;

C is the overdrive factor, i.e. $V_{p\text{-}p}/V_{FS}$;

M is the number of samples per record.

5.3.1.4 Measurement procedure

The lowest and highest transition values, $T[1]$ and $T[2^N-1]$ respectively, are determined according to method (a), where $T[k]$ is the transition value between codes k – 1 and k.

The ramp wave is then applied and the histogram of output codes obtained:
$H[k]$, for k = 0..2^N – 1.

The individual counts for the code values zero and 2^N – 1, i.e. $H[0]$ and $H[2^N - 1]$ are not required in the following calculations, but they should be equal in value.

The input voltage for each transition value is given by the proportion of samples for all the code values below the particular value relative to the total recorded:

$$T[k] = T[1] + A \cdot \sum_{i=1}^{k-1} H[i] \tag{15}$$

where

$H[i]$ is the number of samples with code value I;

$$A = \frac{T[2^N - 1] - T[1]}{S} \tag{16}$$

$$S = \sum_{i=1}^{2^N-2} H[i] \tag{17}$$

5.3.1.4.1 Error estimates using the end-points

The linearity error at each transition k is given by

$$\frac{2^N - 2}{S} \cdot \sum_{i=1}^{k} H[i] - k \tag{18}$$

in LSB.

The end-points linearity error is the maximum of the absolute values of the individual errors.

5.3.1.4.2 Error estimates using straight-line best fit

For the case of straight-line best fit, each value of $T[k]$ is adjusted by subtracting half of the sum of the most negative linearity error and the most positive linearity error from each. The linearity error equals the value of this adjustment.

5.3.1.4.3 Error estimates using method of least squares

For the case of the least-squares best fit, the following procedure is used to obtain the new transfer characteristic:

$$Q_1 = \frac{(2^N - 1)\cdot \sum_{k=1}^{2^N-1} k \cdot T[k] - \sum_{k=1}^{2^N-1} k \cdot \sum_{k=1}^{2^N-1} T[k]}{(2^N - 1)\cdot \sum_{k=1}^{2^N-1} k^2 - \left(\sum_{k=1}^{2^N-1} k\right)^2}$$

determine the new step size: , (19)

$$V_1 = \frac{1}{2^N - 1} \sum_{k=1}^{2^N-1} T[k] - Q_1 \cdot 2^{N-1}$$

determine an offset voltage: (20)

then the new transition values are given by

$$T_1[\mathrm{k}] = V_1 + k \cdot Q_1. \quad (21)$$

The least-squares linearity error is the absolute maximum of: $T[k]$-$T_1[k]$, for k = 0..2^N– 1.

5.3.1.5 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- Duration of input signal transition.
- Clock frequency, as appropriate.
- Conditions at other terminals.

5.3.2 Method d (dynamic operation, with sinusoidal waveform)

5.3.2.1 General purpose

See the first two paragraphs (cases A, B and C) of Clause 15 of IEC 60748-4:1997.

5.3.2.2 Circuit diagram

See Figure 1.

5.3.2.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a sinusoidal signal.

5.3.2.3.1 Determining the conditions to meet the requirements for accuracy

The input is overdriven so that its amplitude exceeds the range of interest of the input voltage, which is usually full scale. The amount of overdrive should exceed one LSB in each direction, see below. The amplitude and offset of the input waveform should be known to the same degree as the required accuracy.

For linearity errors, the overdrive should exceed:

$$Maximum\left\{2\sigma, \frac{2^N \cdot \sigma^2}{V_{FS} \cdot B}\right\} \tag{22}$$

For differential linearity error, the overdrive should exceed:

$$Maximum\left\{3\sigma, \sigma \cdot \sqrt{\frac{3}{2B}}\right\} \tag{23}$$

where

σ is the r.m.s. noise level at output, referred to the input;

N is the number of bits of the ADC;

V_{FS} is the full-scale range of the ADC;

B is the desired tolerance as a fraction of the step width.

Overall accuracy increases with the number of samples recorded for each code value. The test duration, i.e. the number of samples in a record and the number of records, is set so that the count of samples for each of the code values is not less than the minimum that gives the required accuracy for determining each transition value.

Suitable values for the number of records and number of samples in a record may be obtained from Figure 4. Refer to Annex A for the derivation of the curves.

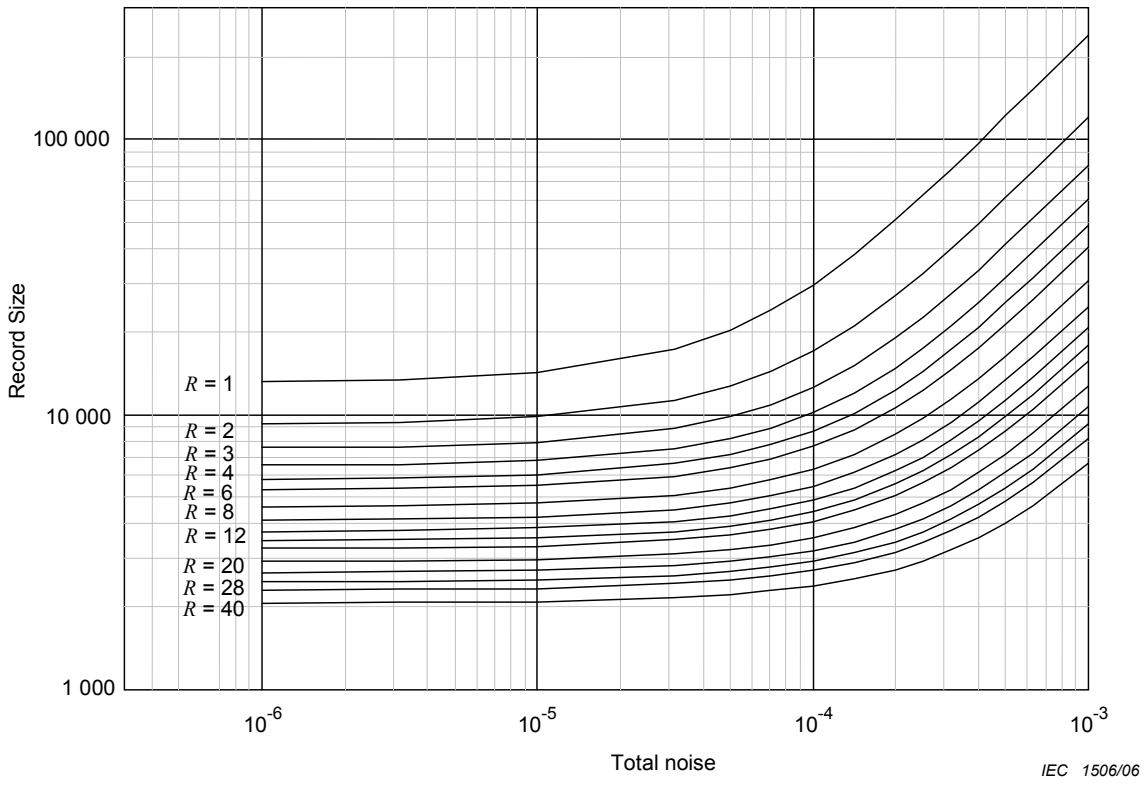

Figure 4 – Record size vs. total noise, for various numbers of records, sine wave input

The curves in Figure 4 apply to the case of N = 10, D = 1, K/B = 8, c = 1,01. Since R is proportional to $D{\cdot}(2^N \cdot K/B)^2$, and M is proportional to c, suitable values for R and M can be obtained for other values of D, N, K, B, and c

where

R is the minimum number of records;

D is 1 for linearity error, 2 for differential linearity error;

N is the number of bits of the ADC;

K is the number of standard deviations that give the required confidence level, see Table 1;

B is the desired tolerance as a fraction of the step width;

c is the overdrive factor, i.e. $V_{\text{p-p}}/V_{\text{FS}}$;

M is the number of samples per record.

5.3.2.4 Measurement procedure

The lowest and highest transition values, $T[1]$ and $T[2^N - 1]$ respectively, are determined according to method a.

The sine wave is then applied and the histogram of output codes obtained.

The measured value of each transition value, $T[k]$, is given by the proportion of samples for all the code values below the particular value relative to the total recorded:

$$T[k] = V_O - V_P \cdot \cos\left(\frac{\pi}{S}\sum_{i=0}^{k-1} H[i]\right) \tag{24}$$

for k = 1..2^N – 2

where

$H[i]$ is the number of samples with code value I;

V_{O} is the offset voltage, for bipolar input; = offset voltage + V_P, for single-ended input;

V_{P} is the amplitude of sine wave;

S is the total number of samples, i.e. $R{\cdot}M$.

Refer to Annex A for the method of determining V_0 and V_{P} if they are not known accurately.

5.3.2.4.1 Error estimates using the end-points

The linearity error, in LSB, at each transition k is given by either:

$$(\text{T[k]} - \text{V}_\text{O})/\text{Q} - \text{k}, \tag{25}$$

or directly from the histogram:

$$\frac{V_P}{Q}\left[\cos\left(\frac{\pi}{S}H[0]\right) - \cos\left(\frac{\pi}{S}\sum_{i=1}^{k} H[\text{i}]\right)\right] + 1 - k \tag{26}$$

where

$$Q = \left(T[2^N - 1] - T[1]\right)\Big/\left(2^N - 2\right) \tag{27}$$

the end-points linearity error is the maximum of the absolute values of the individual errors.

5.3.2.4.2 Error estimates using straight-line best fit

The procedure given in 5.3.1.4.2 above is used with the values obtained in 5.3.2.4.1.

5.3.2.4.3 Error estimates using method of least squares

The procedure given in 5.3.1.4.3 above is used with the values obtained in 5.3.2.4.1.

5.3.2.5 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- Clock frequency, as appropriate.
- Conditions at other terminals.

5.4 Differential linearity error (E_D)

Subclauses 5.4.1 and 5.4.2 supplement Clause 16 of IEC 60748-4:1997.

5.4.1 Method b (dynamic operation, linear ramp waveform)

5.4.1.1 Purpose

See Clause 16 of IEC 60748-4:1997.

5.4.1.2 Circuit diagram

See Figure 1.

5.4.1.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a linear ramp waveform.

Refer to 5.3.1.3.1 for the conditions necessary to achieve the desired accuracy.

5.4.1.4 Measurement procedure

The linearity error is determined as in 5.3.1.4.1, 5.3.1.4.2, or 5.3.1.4.3, as appropriate, after setting offset error and gain error to zero (where appropriate).

Cases A and B: the differential linearity error for each step is the absolute value of the difference: $H[i] - \frac{S}{2^N - 2}$ as determined in 5.3.1.4.1. The differential linearity error is given by the maximum of these values.

Case D (least-squares best fit): the differential linearity errors may be obtained by multiplying those obtained in 5.3.1.4.1 by the ratio Q/Q_1 obtained in 5.3.1.4.3. In practice, since this ratio is very close to 1, those values may be used instead.

5.4.1.5 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- Duration of input signal transition.
- Clock frequency, as appropriate.
- Conditions at other terminals.

5.4.2 Method c (dynamic operation, sinusoidal waveform)

5.4.2.1 Purpose

See Clause 16 of IEC 60748-4:1997.

5.4.2.2 Circuit diagram

See Figure 1.

5.4.2.3 Circuit description and requirements

The circuit description and requirements given in 5.1.1.3 are applicable for this measurement.

The input to the ADC being measured shall be a sinusoidal waveform.

Refer to 5.3.2.3.1 for the conditions necessary to achieve the desired accuracy.

5.4.2.4 Measurement procedure

The linearity error is determined as in 5.3.2.4.1, 5.3.2.4.2, or 5.3.2.4.3, as appropriate, after setting offset error and gain error to zero (where appropriate).

Cases A and B: the differential linearity error for each step k is the absolute value of the difference: $T[k + 1] - T[k]$, for $k = 1..2^N - 2$, as obtained in 5.3.2.4.1. The differential linearity error is given by the maximum of these values.

Case D (least-squares best fit): the differential linearity errors may be obtained by multiplying those obtained in 5.3.2.4.1 by the ratio Q/Q_1 obtained in 5.3.1.4.3. In practice, since this ratio is very close to 1, those values may be used instead.

5.4.2.5 Specified conditions

- Ambient or reference point temperature.
- Supply voltages.
- Input signal frequency, as appropriate.
- Input signal amplitude.
- Clock frequency, as appropriate.
- Conditions at other terminals.

Annex A
(informative)

Mathematical derivations

A.1 Probability distribution of code transition values

The values in Table 1 refer to the normal probability distribution and are obtained from the solution of $p = \int_{\frac{-K}{2}}^{\frac{K}{2}} e^{-\frac{U^2}{2}} du$, where U is a normally distributed variable. The values give the range of the variable, in standard deviations, that contains the proportion p out of all possible values.

A.2 Discrete Fourier Transform

The Discrete Fourier Transform (DFT) of the set of samples in a record is given by

$$X[n] = \sum_{k=0}^{M-1} x[k] \cdot e^{(-j2\pi \cdot n \cdot k / M)}$$

where

M is the number of samples in the record;

n is an integer ranging from 0 to M-1;

$x[k]$ is the sample number k, where k lies between 0 and M-1;

$X[n]$ is the term number n of the transform representing the frequency given by $F_S \cdot n/M$.

Each integral value of *n* produces a spectral line at a frequency that is the nth harmonic of the base frequency F_S/M, and the amplitude and phase at any such frequency are given by

Amplitude = $\sqrt{A^2 + B^2}$, and phase = arctan (B/A),

where

$$A = \frac{2}{M} \sum_{k=0}^{M-1} x[k] \cdot \sin(2\pi \cdot n \cdot k / M) \text{ and } B = \frac{2}{M} \sum_{k=0}^{M-1} x[k] \cdot \cos(2\pi \cdot n \cdot k / M)$$

The frequency f of a spectral line is given by $f = F_S \cdot n/M$. The input frequency F_i may be selected by choosing $n = J$.

The value obtained for the spectral line at $M/2$ (Nyquist frequency) varies with the phase of the input at this frequency, if any, relative to the sampling instant, and should be ignored.

Noise due to quantization is uniformly spread over the spectrum and has an average amplitude $Q/\sqrt{12}$, provided that N > 6, where Q = 1 LSB = $V_{FS}/2^N$. Internally generated noise can be larger.

A.3 Minimum record size

When determining code transition values from the histogram, the minimum number of records and the number of samples in a record are derived from the following equations.

A.3.1 Ramp wave case

$$R = D \cdot \left[\frac{2^{N-1} \cdot K}{B} \right]^2 \cdot \frac{c}{M} \cdot \left\{ 1.125 \left(\frac{\sigma^*}{V_{FS}} + \frac{c}{2} \sigma_\phi \right) + 0.25 \frac{c}{M} \right\}$$

where

R is the minimum number of records;

D is 1 for linearity error, 2 for differential linearity error;

N is the number of bits of the ADC;

K is the number of standard deviations that give the required confidence level (see Table 1);

B is the desired tolerance as a fraction of the step width;

c is the overdrive factor, i.e. $V_{\text{p-p}}/V_{\text{FS}}$;

M is the number of samples per record;

V_{FS} is the full scale range of the ADC;

σ is the r.m.s. noise level at output, referred to the input;

σ^* is σ for linearity error, minimum of σ or LSB/1,1 for differential linearity error;

σ_ϕ is the r.m.s. value of combined phase jitter referred to the clock period;

σ_{T} is the total noise = $\sigma^*/V_{\text{FS}} + c \cdot \sigma_\phi/2$.

The equation above may be rewritten so as to determine the minimum value for M:

$$M = a\left(4.5\sigma_{\text{T}}\right) \pm a\sqrt{\left(4.5\sigma_{\text{T}}\right)^2 + \frac{c}{a}}$$

where

$$a = \frac{c \cdot D \cdot \left(\frac{2^{N-1} \cdot K}{B} \right)^2}{R}$$

and R has been chosen to give a usable value for M. The curves in Figure 3 are solutions of this equation.

A.3.2 Sine-wave case

$$R = D \cdot \left[\frac{2^{N-1} \cdot K}{B} \right]^2 \cdot \frac{c\pi}{M} \cdot \left\{ 1.125 \left(\frac{\sigma^*}{V_{FS}} + \frac{c}{2} \sigma_\phi \right) + 0.25 \frac{c\pi}{M} \right\}$$

This equation may be rewritten so as to determine the minimum value for M:

$$M = a(4.5\sigma_T) \pm a\sqrt{(4.5\sigma_T)^2 + \frac{c\pi}{a}}$$

where $a = \dfrac{c \cdot \pi \cdot D \cdot \left(\dfrac{2^{N-1} \cdot K}{B}\right)^2}{R}$,

and R has been chosen to give a usable value for M. The curves in Figure 4 are solutions of this equation.

A.4 Determining V_0 and V_P

In the method of 15.4.4, if V_0 or V_P are not known accurately, then substitute the known values for $T[1]$, $T[2^N - 1]$, and $H[0]$, $H[2^N - 2]$ into the equations below in order to obtain good estimates; note that $H[0]$ should equal $H[2^N - 2]$.

$$V_P = \frac{T[2^N - 1] - T[1]}{\cos\left(\pi \dfrac{H[0]}{S}\right) + \cos\left(\pi \dfrac{H[2^N - 2]}{S}\right)}, \quad V_0 = \frac{T[2^N - 1] \cdot \cos\left(\pi \dfrac{H[0]}{S}\right) + T[1] \cdot \cos\left(\pi \dfrac{H[2^N - 2]}{S}\right)}{\cos\left(\pi \dfrac{H[0]}{S}\right) + \cos\left(\pi \dfrac{H[2^N - 2]}{S}\right)}$$

Annex B
(informative)

Wideband signal generation and analysis

B.1 Pseudo-random binary sequence generators

The pseudo-random binary sequence generator consists of a shift register, with 1 bit per stage, where the feedback to the first stage is a fixed logic combination of specific bits within the register.

For an N-stage register, there are 2^N possible bit patterns. Different feedback combinations will give different cycle lengths where the sequence of the individual bit patterns exhibits a good degree of randomness. The longest possible cycle length is 2^N-1, although many useful sequences are less than the maximum.

For the measuring system, the sum of the two cycle lengths should be similar to, or exceed, the number of steps in the ADC transfer characteristic, in order to exercise the majority of output code values.

Details of recommended generators are under consideration. Refer also to [1][1].

B.2 Digital filters

The digital filter used here is also known as a digital comb filter, since it removes signals that are simple harmonics of a given fundamental frequency.

The filter is a shift register having a length equal to the cycle length of the corresponding PRBS. Each stage of the register consists of a parallel register with sufficient bits to hold the word length used in the measuring system. For measurements on high-precision ADCs, this could exceed 20 bits.

The output of the filter is the difference (digital subtraction) between the word at the input to the shift register and the word leaving the shift register, i.e. pairs of words that are one cycle length apart.

B.3 Interpolating filters

Under consideration.

B.4 Quasi-peak measurements

In certain circumstances, measurement of the quasi-peak value of the signal gives more information about the output from an ADC than the r.m.s. value of the signal. Refer to IEC 60268-10 for information on the characteristics of a quasi-peak measuring system and its applications.

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[1] Figures in square brackets refer to the bibliography.

Bibliography

[1] GOLOMB, S. W. *Shift Register Sequences*, published by Holden-Day, San Francisco, 1967.

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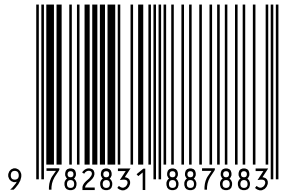

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