INTERNATIONAL STANDARD

IEC 60748-23-5

QC 165000-5

First edition
2003-10

Semiconductor devices – Integrated circuits –

Part 23-5: Hybrid integrated circuits and film structures – Manufacturing line certification – Procedure for qualification approval

Dispositifs à semiconducteurs –
Circuits intégrés –

Partie 23-5:
Circuits intégrés hybrides et structures par films –
Certification de la ligne de fabrication –
Procédure d'homologation

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-5: Hybrid integrated circuits and film structures – Manufacturing line certification – Procedure for qualification approval

FOREWORD

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International Standard IEC 60748-23-5 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the European standard EN 165000-5 and the following documents:

FDIS	Report on voting
47A/672/FDIS	47A/677/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This standard should be read in conjunction with IEC 60748-23-1.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – INTEGRATED CIRCUITS –

Part 23-5: Hybrid integrated circuits and film structures – Manufacturing line certification – Procedure for qualification approval

1 Scope

This part of IEC 60748-23 applies to high quality hybrids (with films) incorporating special customer quality and reliability requirements whose quality is assessed on the basis of Qualification Approval.

NOTE 1 Hybrid integrated circuits may be fully or part completed. Part completed devices are those that may be supplied to customers for further processing.

NOTE 2 Test methods are selected from IEC 60748-23-1. A blank detail specification (BDS) is included to assist manufacturers and users in the preparation of detail specifications.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60748-23-1:2002, *Semiconductor devices – Integrated circuits – Part 23-1: Hybrid integrated circuits and film structures – Manufacturing line certification – Generic specification*

IEC 61340-5-1:1998, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

QC 001002-3:1998, *IEC Quality Assessment System for Electronic Components (IECQ) – Rules of Procedure – Part 3: Approval procedures*

3 Terms and definitions

For the purposes of this part of IEC 60748, related documents, preferred ratings and characteristics, and terminology are given in IEC 60748-23-1.

4 Qualification approval procedures

4.1 General

The procedures in QC 001002-3 shall apply.

Subclause 6.1 of IEC 60748-23-1 applies with the exceptions given in 4.2 to 4.11 of this standard.

4.2 Marking

Clause 5 of IEC 60748-23-1 applies.

4.3 Validity of release for delivery

Circuits may be released under qualification approval subject to the following conditions:

a) the circuits conform with the requirements of the detail specification;

b) the circuits, their added components, piece parts and materials are traceable to original manufacturer's lot numbers.

4.4 Application for qualification approval

Application shall be made to the NSI in accordance with QC 001002-3. In addition, the manufacturer shall:

a) conform with the eligibility requirements of 6.1.1 of IEC 60748-23-1;

b) conform with the relevant detail specification based on the blank detail specification (see Clause 6) and the Qualification – product assessment level schedules (Q-PALS) (see Clause 5) contained in this standard.

4.5 Structural similarity

For the purposes of assessment testing, structural similarity can be used if the testing of one representative type of circuit gives at least the same quality level for the rest of the types which are grouped together.

The designated management representative (DMR) shall declare to the satisfaction of the NSI the method of operating the structural similarity plan within the manufacturing facilities and agree the representative type(s) from each structurally similar group.

For the qualification approval procedure, two or more circuits can be considered structurally similar, and thus the required numbers of specimens for a test shall be selected from the combined production, when they have the same function type, use the same design rules, materials, processes and methods (for example a range of T-cell thick film attenuators using the same line of inks; or thin film D/A convertors using the same film material and same added components from the same supplier).

Only those tests not specifically excluded in the Q-PALS may be considered for structural similarity.

4.6 Materials, piece-parts and added components

Subclause 6.1.3 of IEC 60748-23-1 applies.

4.7 Initial qualification approval

The schedules to be used for qualification approval testing on the basis of lot-by-lot and periodic testing are given in the Q-PALS tables contained in this standard.

The procedure for initial qualification approval is given below.

The relevant Q-PALS for initial qualification approval, release of products (lot-by-lot tests) and maintenance of qualification approval (periodic tests) collectively prescribe the minimum test programme on completed circuits.

1) Sampling

   The sample shall be representative of the range of circuits for which approval is sought (see 6.4.3 of IEC 60748-23-1). The size of the sample and the criterion of acceptability depend on the relevant Q-PALS which it is intended to release against.

2) Tests

The complete series of tests specified in the relevant Q-PALS contained in this standard is required for the approval of circuits covered by one detail specification. The tests shall be carried out in the order given.

Test and measurement procedures are given in Clause 7 of IEC 60748-23-1.

Samples used for Group B, C and D tests shall have passed Group A tests.

One failure is counted when a circuit has not satisfied the whole, or a part, of the tests of a group.

Approval is granted when the number of failures does not exceed the specified number of permissible failures for each group or sub-group.

4.8 Granting of qualification approval

The manufacturer shall submit a report to the NSI covering the qualification approval testing in accordance with the requirements of 4.7 of this standard, and with QC 001002-3.

Qualification approval shall be granted when the requirements of this standard have been satisfied.

A qualification approval certificate will be issued by the responsible national authority in accordance with QC 001002-3.

4.9 Maintenance of qualification approval

4.9.1 General

Qualification approval is maintained after successful completion of the procedures and requirements of quality conformance inspection (see 6.4.2 of IEC 60748-23-1) with the following details:

1) Design evaluation tests

In addition to the initial delivery lot, design evaluation tests shall be carried out at the periodicity specified in the detail specification.

2) Detail specification

The detail specification shall conform to the requirements of the BDS and Q-PALS in this standard.

The manufacturer shall also have maintained continuous production, for example:

a) no change has occurred in the place of manufacture and final test;

b) no break exceeding two years has occurred in the manufacturer's declared periodic test schedule.

4.9.2 Changes to qualification approval

The manufacturer is required to notify the NSI of changes to his qualification approval in accordance with QC 001002-3 and 6.5.2 of IEC 60748-23-1, where applicable.

NOTE All re-verification programmes are to be agreed with the NSI.

4.10 Procedure in the event of a failure in a periodic test

The procedure described in QC 001002-3 shall apply.

4.11 Withdrawal of qualification approval

The procedures in QC 001002-3 shall apply.

5 Qualification-product assessment level schedules

NOTE The following 11 Q-PALS are based upon corresponding PALS in IEC 60748-23-1, Annex A.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 1

Applicability

This assessment schedule is intended for use with solder assembled and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices, which are for use in benign mechanical and temperature environments.

Subgroup A tests: Device screening 100 %	**IEC 60748-23-1 Reference**
1. Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality	7.4

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1.	Electrical test at T_{amb} (other than those specified for screening)	7.4
2.	External visual inspections	7.3.2

Subgroup C tests (6 monthly period): Design evaluation

Minimum sample 8. Accept on 0 failures.

1.	Electrical test. All specified parameters at T_{min} and T_{max}*	7.4
2.	Dimensions	7.3.3

Subgroup D tests (12 monthly period): Design evaluation

Minimum sample 3. Accept on 0 failures.

1.	Resistance of circuits to solder heat	(D)	7.5.11
2.	Solderability	(ND/D)	7.5.10
3.	Robustness of terminations	(D)	7.5.12
4.	Flammability	(D)	7.5.16
5.	Resistance to solvents	(ND)	7.5.15

Process and packaging requirements

1.	Substrate fabrication = class 100 000.	
2.	Substrate assembly (bare die) = class 100 000.	
3.	ESD precautions (where applicable) to IEC 61340-5-1.	
4.	Pre-cap visual at IL S4 AQL 0,4 % minimum.	7.3.1

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 2

Applicability

This assessment schedule is intended for use with solder assembled and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices, which are for use in benign mechanical and temperature environments.

Subgroup A tests: Device screening 100 %	**IEC 60748-23-1 Reference**
1. Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality	7.4

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1.	Electrical test at T_{amb} (other than those specified for screening)	7.4
2.	External visual inspection	7.3.2

Subgroup C tests (6 monthly period): Design evaluation

Minimum sample 8. Accept on 0 failures

1.	Electrical endurance 1 000 h. Release after 160 h*	7.5.14
2.	Electrical test. All specified parameters at T_{min} and T_{max}*	7.4
3.	Dimensions	7.3.3

Subgroup D tests (12 monthly period): Design evaluation

Minimum sample 3. Accept on 0 failures

1.	Resistance of circuits to solder heat	(D)	7.5.11
2.	Solderability	(ND/D)	7.5.10
3.	Robustness of terminations	(D)	7.5.12
4.	Flammability	(D)	7.5.16
5.	Resistance to solvents	(ND)	7.5.15

Process and packaging requirements

1.	Substrate fabrication = class 100 000.	
2.	Substrate assembly (bare die) = class 100 000.	
3.	ESD precautions (where applicable) to IEC 61340-5-1.	
4.	Pre-cap visual at IL S4 AQL 0,4 % minimum.	7.3.1

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 3

Applicability

This assessment schedule is intended for use with solder assembled, and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices. These hybrids are for use in benign mechanical environments but with demonstration of extreme temperature and humidity operation.

Subgroup A tests: Device screening 100 %	**IEC 60748-23-1 Reference**
1. Change of temperature: 10 cycles.	7.5.8.1
2. Electrical test at T_{amb}. Those tests in the detail specification. which define circuit functionality.	7.4

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %	
1. Electrical test at T_{amb} (other than those specified for screening).	7.4
2. Electrical tests at T_{min} and T_{max}. Those tests in the detail specification. which define circuit functionality.	7.4
3. External visual inspection.	7.3.2

Subgroup C tests (6 monthly): Design evaluation

Minimum sample 8. Accept on 0 failures.

1. Electrical endurance 1 000 h. Release after 160 h.*	7.5.14
2. Dimensions.	7.3.3
3. Damp heat cyclic or steady state.	7.5.4, 7.5.3
4. Change of temperature.*	7.5.8.2

Subgroup D tests (12 monthly period): Design evaluation

Minimum sample 3. Accept on 0 failures.

1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Robustness of terminations.	(D)	7.5.12
4. Flammability.	(D)	7.5.16
5. Resistance to solvents.	(ND)	7.5.15

Process and packaging requirements

1. Substrate fabrication = class 100 000.
2. Substrate assembly (bare die) = class 100 000.
3. ESD precautions (where applicable) to IEC 61340-5-1.
4. Pre-cap visual at IL S4 AQL 0,4 % minimum. 7.3.1

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 4

Applicability

This assessment schedule is intended for use with solder assembled and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices, which are for use in non-benign mechanical and temperature environments. It is intended to give a high level of assurance on this type of build standard.

Subgroup A tests: Device screening 100 % PDA = 10 %	**IEC 60748-23-1 Reference**
1. Change of temperature: 10 cycles.	7.5.8.1
2. Electrical tests at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
3. Burn-in 160 h.	7.5.14
4. Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
5. Electrical Tests at T_{min} and T_{max}. Those tests in the detail specification which define circuit functionality.	7.4
6. External visual inspection.	7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1. Electrical test at T_{amb} (other than those specified under 2. of screening).	7.4

Subgroup C1 tests (3 monthly): Design evaluation

Minimum sample 8. Accept on 0 failures.

1. Electrical endurance 2 000 h. Release after 1 000 h.*	7.5.14
2. Dimensions.	7.3.3
3. Damp heat cyclic or steady state.	7.5.4, 7.5.3
4. Change of temperature.*	7.5.8.2

Subgroup C2 tests (6 monthly): Design evaluation

Minimum sample 5. Accept on 0 failures.

1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Resistance to solvents.	(ND)	7.5.15
4. Acceleration.	(ND/D)	7.5.7
5. Shock and/or vibration (as specified in detail specification).	(ND/D)	7.5.5, 7.5.6

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 4, continued

Subgroup D tests (12 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 3. Accept on 0 failures.		
1. Robustness of terminations.	(D)	7.5.12
2. Flammability.	(D)	7.5.16

Process and packaging requirements

1. Substrate fabrication = class 100 000.
2. Substrate assembly (bare die) = class 100 000.
3. ESD precautions (where applicable) to IEC 61340-5-1.
4. Pre-cap visual at 100 %. 7.3.1

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 5

Applicability

This assessment schedule is intended for use with solder assembled, and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices which are for use in non-benign mechanical and temperature environments. It is intended to give the highest level of assurance on this type of product.

Subgroup A tests: Device screening 100 % PDA = 10 %		**IEC 60748-23-1 Reference**
1.	Change of temperature: 10 cycles.	7.5.8.1
2.	Electrical tests at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
3.	Acceleration (5 000 g_n or at design limit).	7.5.7
4.	Burn-in 160 h.	7.5.14
5.	Electrical test at T_{amb}. Those tests in the detail specification. which define circuit functionality.	7.4
6.	Electrical Tests at T_{min} and T_{max}. Those tests in the detail specification which define circuit functionality.	7.4
7.	External visual inspection.	7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1.	Electrical test at T_{amb} (other than those specified under 2. of screening).	7.4

Subgroup C1 tests (3 monthly): Design evaluation

Minimum sample 8. Accept on 0 failures.

1.	Electrical endurance 2 000 h. Release after 1 000 h.*	7.5.14
2.	Dimensions.	7.3.3
3.	Damp heat cyclic or steady state.	7.5.4, 7.5.3
4.	Change of temperature.*	7.5.8.2

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 5, continued

Subgroup C2 tests (6 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 5. Accept on 0 failures.		
1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Resistance to solvents.	(ND)	7.5.15
4. Acceleration.	(ND/D)	7.5.7
5. Shock and/or vibration (as specified in the detail specification).	(ND/D)	7.5.5, 7.5.6

Subgroup D tests (12 monthly): Design evaluation		
Minimum sample 3. Accept on 0 failures.		
1. Robustness of terminations.	(D)	7.5.12
2. Flammability.	(D)	7.5.16

Process and packaging requirements

1. Substrate fabrication = class 100 000.
2. Substrate assembly (bare die) = class 100 000.
3. ESD precautions (where applicable) to IEC 61340-5-1.
4. Pre-cap visual at 100 %. 7.3.1

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 6

Applicability

This assessment schedule is intended for use with bare die, hermetic cavity devices. This assessment is also intended for use with substrates containing solder attached added components all of which are individually hermetic. These devices are for use in benign mechanical environments but with demonstration of extreme temperature operation. The assessment is intended where lower levels of assurance are adequate.

Subgroup A tests: Device screening 100 %		**IEC 60748-23-1 Reference**
1.	Change of temperature: 10 cycles.	7.5.8.1
2.	Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
3.	Sealing fine and gross.	7.5.9
4.	External visual inspection.	7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1.	Electrical test at T_{amb} (other than those specified for screening).	7.4
2.	Electrical tests at T_{min}, T_{max} and T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4

Subgroup C tests (6 monthly): Design evaluation

Minimum sample 8. Accept on 0 failures.

1.	Electrical endurance 1 000 h. Release after 160 h.*	7.5.14
2.	Dimensions.	7.3.3

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 6, continued

Subgroup D tests (12 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 3. Accept on 0 failures.		
1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Robustness of terminations.	(D)	7.5.12
4. Resistance to solvents.	(ND)	7.5.15
5. Damp heat steady state 56 days or salt mist (as specified in the detail specification).	(D)	7.5.3, 7.5.13

Process and packaging requirements

1. Substrate fabrication = class 100 000.
2. Substrate assembly (bare die) = class 100 000.
3. Temperature monitored and controlled, relative humidity 30 % to 65 % prior to hermetic sealing stage.
4. ESD precautions (where applicable) to IEC 61340-5-1.
5. Pre-cap visual at 100 %. 7.3.1
6. Hermetic packaging in glass, metal, ceramic or combinations of these; no adhesive or polymeric materials used for lid attach and no flux used in the final sealing process.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 7

Applicability

This assessment schedule is intended for use with bare die, hermetic cavity devices. This assessment is also intended for use with substrates containing solder attached added components all of which are individually hermetic. These devices are for use in benign mechanical environments but with demonstration of extreme temperature operation. The assessment with the addition of the burn-in requirement is intended to give a medium level of assurance.

Subgroup A tests: Device screening 100 % PDA = 10 %

		IEC 60748-23-1 Reference
1.	Change of temperature: 10 cycles.	7.5.8.1
2.	Burn-in 160 h.	7.5.14
3.	Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
4.	Sealing fine and gross.	7.5.9
5.	External visual inspection.	7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1.	Electrical test at T_{amb} (other than those specified for screening).	7.4
2.	Electrical tests at T_{min}, T_{max} and T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4

Subgroup C tests (6 monthly): Design evaluation

Minimum sample 8. Accept on 0 failures.

1.	Electrical endurance 1 000 h. Release after 160 h.*	7.5.14
2.	Dimensions.	7.3.3

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 7, continued

Subgroup D tests (12 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 3. Accept on 0 failures.		
1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Robustness of terminations.	(D)	7.5.12
4. Resistance to solvents.	(ND)	7.5.15
5. Damp heat steady state 56 days or salt mist (as specified in the detail specification).	(D)	7.5.3, 7.5.13

Process and packaging requirements

1. Substrate fabrication = class 100 000.	
2. Substrate assembly (bare die) = class 100 000.	
3. Temperature monitored and controlled, relative humidity 30 % to 65 % prior to hermetic sealing stage.	
4. ESD precautions (where applicable) to IEC 61340-5-1.	
5. Pre-cap visual at 100 %.	7.3.1
6. Hermetic packaging in glass, metal, ceramic or combinations of these; no adhesive or polymeric materials used for lid attach and no flux used in the final sealing process.	

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 8

Applicability

This assessment schedule is intended for use with bare die, hermetic cavity devices. This assessment is also intended for use with substrates containing solder attached added components all of which are individually hermetic. These devices are for use in non-benign mechanical and temperature environments. The assessment is intended to give a high level of assurance for these devices for use in extreme environment applications.

Subgroup A tests: Device screening 100 % PDA = 7 %		**IEC 60748-23-1 Reference**
1. Change of temperature: 10 cycles.		7.5.8.1
2. Acceleration (5 000 g_n or at design limit).		7.5.7
3. Electrical tests at T_{amb}. Those tests in the detail specification which define circuit functionality.		7.4
4. Burn-in 160 h.		7.5.14
5. Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.		7.4
6. Electrical tests at T_{min} and T_{max}. Those tests in the detail specification which define circuit functionality.		7.4
7. Sealing fine and gross.		7.5.9
8. External visual inspection.		7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %

1. Electrical test at T_{amb} (other than those specified under 3. of screening).		7.4

Subgroup C1 tests (3 monthly): Design evaluation

Minimum sample 8. Accept on 0 failures.

1. Electrical endurance 2 000 h. Release after 1 000 h.*		7.5.14
2. Dimensions.		7.3.3
3. Shock and/or vibration (as specified in the (detail specification).	(ND/D)	7.5.5, 7.5.6
4. Acceleration.	(ND/D)	7.5.7

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 8, continued

Subgroup C2 tests (6 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 5. Accept on 0 failures.		
1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Resistance to solvents.	(ND)	7.5.15
4. Damp heat steady state 56 days or salt mist (as specified in the detail specification).	(D)	7.5.3, 7.5.13

Subgroup D tests (12 monthly): Design evaluation		
Minimum sample 3. Accept on 0 failures.		
1. Robustness of terminations.	(D)	7.5.12

Process and packaging requirements

1. Substrate fabrication = class 100 000.
2. Substrate assembly (bare die) = class 100 000.
3. Pre-cap visual = class 10 000.
4. Temperature monitored and controlled, relative humidity 30 % to 65 % prior to sealing stage.
5. ESD precautions (where applicable) to IEC 61340-5-1.
6. Pre-cap visual at 100 %. 7.3.1
7. Hermetic packaging in glass, metal, ceramic or combinations of these; no adhesive or polymeric materials used for lid attach and no flux used in the final sealing process.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 9

Applicability

This assessment schedule is intended for use with bare die, hermetic cavity devices, which are for use in non-benign mechanical and temperature environments. It is intended to give a very high level of assurance for these devices for use in applications where reliability is paramount.

Subgroup A tests: Device screening 100 % PDA = 5 %		**IEC 60748-23-1 Reference**
1.	Change of temperature: 10 cycles.	7.5.8.1
2.	Acceleration (5 000 g_n or at design limit).	7.5.7
3.	Particle impact noise detection.	7.5.17
4.	Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
5.	Burn-in 160 h.	7.5.14
6.	Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
7.	Electrical tests at T_{min} and T_{max}. Those tests in the detail specification which define circuit functionality.	7.4
8.	Sealing fine and gross.	7.5.9
9.	External visual inspection.	7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %		
1.	Electrical tests at T_{min}, T_{max} and T_{amb} (other than those specified under 4. of screening).	7.4
2.	Electrical endurance 2 000 h.	7.5.14

Subgroup C1 tests (3 monthly): Design evaluation

Minimum sample 8. Accept on 0 failures.

1.	Electrical endurance 2 000 h. Release after 1 000 h.*		7.5.14
2.	Dimensions.		7.3.3
3.	Acceleration.	(ND/D)	7.5.7
4.	Shock (as specified in the detail specification).	(ND/D)	7.5.5
5.	Vibration (as specified in the detail specification).	(ND/D)	7.5.6

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 9, continued

Subgroup C2 tests (6 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 5. Accept on 0 failures.		
1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Resistance to solvents.	(ND)	7.5.15
4. Damp heat steady state 56 days or salt mist (as specified in the detail specification).	(D)	7.5.3, 7.5.13

Subgroup D tests (12 monthly): Design evaluation		
Minimum sample 3. Accept on 0 failures.		
1. Robustness of terminations.	(D)	7.5.12
2. Internal moisture content 5 000 ppm water.*	(D)	7.5.18

Process and packaging requirements

1. Die storage and pre-cap product storage = class 1 000.
2. Substrate fabrication = class 10 000.
3. Substrate assembly (bare die) = class 10 000.
4. Pre-cap visual = class 1 000.
5. Temperature monitored and controlled, relative humidity 30 % to 65 % prior to hermetic sealing stage.
6. ESD precautions (where applicable) to IEC 61340-5-1.
7. Pre-cap visual at 100 %. 7.3.1
8. Hermetic packaging in glass, metal, ceramic or combinations of these; no adhesive or polymeric materials used for lid attach and no flux used in the final sealing process.
9. Destructive bond pull and element shear evaluation on customer product. 7.5.21, 7.5.22

* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 10

Applicability

This assessment schedule is intended for use with bare die, hermetic cavity devices, which are for use in non-benign mechanical and temperature environments. It is intended to give a very high level of assurance for these devices for use in applications where reliability is paramount.

Subgroup A tests: Device screening 100 % PDA = 5 %		**IEC 60748-23-1 Reference**
1.	Dry heat 500 h.	7.5.1
2.	Change of temperature: 10 cycles.	7.5.8.1
3.	Acceleration (5 000 g_n or at design limit).	7.5.7
4.	Particle impact noise detection.	7.5.17
5.	Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
6.	Burn-in 160 h.	7.5.14
7.	Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
8.	Electrical tests at T_{min} and T_{max}. Those tests in the detail specification which define circuit functionality.	7.4
9.	Sealing fine and gross.	7.5.9
10.	External visual inspection.	7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %			
1.	Electrical tests at T_{min}, T_{max} and T_{amb} (other than those specified under 5. of screening).		7.4
2.	Electrical endurance 2 000 h.		7.5.14
3.	Shock (as specified in the detail specification).	(ND)	7.5.5
4.	Vibration (as specified in the detail specification).	(D)	7.5.6

Subgroup C1 tests (3 monthly): Design evaluation

Minimum sample 13. Accept on 0 failures.

1.	Electrical endurance 2 000 h. Release after 1 000 h.*		7.5.14
2.	Dimensions.		7.3.3
3.	Acceleration.	(ND/D)	7.5.7

---

* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 10, continued

Subgroup C2 tests (6 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 5. Accept on 0 failures.		
1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Resistance to solvents.	(ND)	7.5.15
4. Damp heat steady state 56 days or salt mist (as specified in the detail specification).	(D)	7.5.3, 7.5.13
Subgroup D tests (12 monthly): Design evaluation		
Minimum sample 3. Accept on 0 failures.		
1. Robustness of terminations.	(D)	7.5.12
2. Internal moisture content. 5 000 ppm water,*	(D)	7.5.18
100 ppm other contaminants.		

Process and packaging requirements

1. Die storage and pre-cap product storage = class 1 000.	
2. Substrate fabrication = class 10 000.	
3. Substrate assembly (bare die) = class 10 000.	
4. Pre-cap visual = class 1000.	
5. Temperature monitored and controlled, relative humidity 30 % to 65 % prior to hermetic sealing stage.	
6. ESD precautions (where applicable) to IEC 61340-5-1.	
7. Pre-cap visual at 100 %.	7.3.1
8. Hermetic packaging in glass, metal, ceramic or combinations of these; no adhesive or polymeric materials used for lid attach and no flux used in the final sealing process.	
9. 100 % non-destructive bond pull testing.	7.5.21
10. Destructive bond pull and element shear evaluation on customer product.	7.5.21, 7.5.22

* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 11

Applicability

This assessment schedule is intended for use with bare die, hermetic cavity devices, which are for use in non-benign mechanical, temperature and radiation environments. It is intended to give the maximum level of assurance for these devices for use in applications such as space where reliability is paramount.

Subgroup A tests: Device screening 100 % PDA = 5 %		**IEC 60748-23-1 Reference**
1.	Dry heat 500 h.	7.5.1
2.	Change of temperature: 10 cycles.	7.5.8.1
3.	Acceleration (5 000 g_n or at design limit).	7.5.7
4.	Particle impact noise detection.	7.5.17
5.	Radiography.	7.5.19
6.	Electrical tests at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
7.	Burn-in 160 h.	7.5.14
8.	Electrical test at T_{amb}. Those tests in the detail specification which define circuit functionality.	7.4
9.	Electrical tests at T_{min} and T_{max}. Those tests in the detail specification which define circuit functionality.	7.4
10.	Sealing fine and gross.	7.5.9
11.	External visual inspection.	7.3.2

Subgroup B tests (lot-by-lot): Device sample testing – IL S4 AQL 0,4 %			
1.	Electrical tests at T_{min}, T_{max} and T_{amb} (other than those required under 6. of screening).		7.4
2.	Electrical endurance 2 000 h.		7.5.14
3.	Shock (as specified in the detail specification).	(ND)	7.5.5
4.	Vibration (as specified in the detail specification).	(D)	7.5.6

Subgroup C1 tests (3 monthly): Design evaluation

Minimum sample 13. Accept on 0 failures.

1.	Electrical endurance 2 000 h. Release after 1 000 h.*		7.5.14
2.	Dimensions.		7.3.3
3.	Acceleration.	(ND/D)	7.5.7

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* Structural similarity rules do not apply.

Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 11, continued

Subgroup C2 tests (6 monthly): Design evaluation		**IEC 60748-23-1 Reference**
Minimum sample 5. Accept on 0 failures.		
1. Resistance of circuits to solder heat.	(D)	7.5.11
2. Solderability.	(ND/D)	7.5.10
3. Resistance to solvents.	(ND)	7.5.15
4. Damp heat steady state 56 days or salt mist (as specified in the detail specification).	(D)	7.5.3, 7.5.13
5. Radiation hardness assessment.	(D)	7.5.23

Subgroup D tests (12 monthly): Design evaluation		
Minimum sample 3. Accept on 0 failures.		
1. Robustness of terminations.	(D)	7.5.12
2. Internal moisture content. 3 000 ppm water,* 100 ppm other contaminants.	(D)	7.5.18
3. Electrical endurance 8 000 h.		7.5.14

Process and packaging requirements

1. Die storage and pre-cap product storage = class 1 000.	
2. Substrate fabrication = class 10 000.	
3. Substrate assembly (bare die) = class 10 000.	
4. Pre-cap visual = class 1 000.	
5. Temperature monitored and controlled, relative humidity 30 % to 65 % prior to hermetic sealing stage.	
6. ESD precautions (where applicable) to IEC 61340-5-1.	
7. Pre-cap visual at 100 %.	7.3.1
8. Hermetic packaging in glass, metal, ceramic or combinations of these; no adhesive or polymeric materials used for lid attach and no flux used in the final sealing process.	
9. 100 % non-destructive bond pull testing.	7.5.21
10. Destructive bond pull and element shear evaluation on customer product.	7.5.21, 7.5.22

* Structural similarity rules do not apply.

6 Blank detail specification

6.1 General

The blank detail specification contains requirements for style and layout and minimum content of detail specifications. These requirements are applicable when the detail specification is published (e.g. for a standard product). The front page layout is illustrated.

The numbers between square brackets on the front page of the blank detail specification illustrated correspond to the following indications which should be given:

[1] The name of the National Standards Organization under whose authority the detail specification is published and, if applicable, the organization from whom the detail specification is available.

[2] The number allotted to the detail specification by the IEC Central Office.

[3] The number and issue number of the IEC generic or sectional specification as relevant; also national reference if different.

[4] If different from the IEC number, the national number of the detail specification, date of issue and any further information required by the national system, together with any amendment numbers.

[5] A brief description of the technique and the type or function of the hybrid circuit.

[6] Information on typical construction (where applicable).

[7] An outline drawing with main dimensions which are of importance for interchangeability and/or reference to the appropriate national or international document for outlines. Alternatively, this drawing may be given in an appendix to the detail specification.

[8] The product assessment level schedule number covered by the detail specification.

[9] Reference data giving information on the most important properties of the circuit which allow comparison between the various circuit types intended for the same, or for similar, applications.

6.2 FRONT PAGE FOR COMPONENTS ASSESSED BY QUALIFICATION APPROVAL

<table>
<tr><td>Specification available from: [1]</td><td>IEC 60748-23-5 [2]

Page 1 of</td></tr>
<tr><td>Electronic components of assessed quality by qualification approval in accordance with: [3]</td><td>[4]</td></tr>
<tr><td rowspan="3">Outline and dimensions – (see Table 1) (first angle projection): [7]

Dimensions in mm (see NOTE 1)</td><td>Thick/thin film hybrid integrated circuit [5]</td></tr>
<tr><td>Encapsulation (see NOTE 2) [6]</td></tr>
<tr><td>Q-Product assessment Level No. [8]</td></tr>
</table>

NOTE 1 The non-dimensioned details do not affect the performance of the devices.

NOTE 2 State whether the terminations are (are not) suitable for soldering.
State whether the terminations are (are not) suitable for printed wiring applications.

Information about manufacturers having components that are qualified to this detail specification is available in the current QC 001 005: Register of firms, products and services approved under the IECQ system, including ISO 9000. QC 001 005 is available on www.iecq.org

6.3 GENERAL DATA

6.3.1 Recommended methods of mounting

The detail specification shall prescribe the method of mounting to be applied for normal use and for the application of the vibration and the bump or shock tests. The design of the circuit may be such that special mounting fixtures are required in its use. In this case, the detail specification shall describe the mounting fixtures and they shall be used in the application of the vibration and bump or shock tests.

6.3.2 Dimensions, characteristics and conditions of use

Table 1 (see 6.1, item [9])

Where a range of products has the same basic function and is made in the same technology and envelope, a table shall be inserted to detail the differences in characteristics.

The detail specification shall contain all information needed to describe adequately:

6.3.3 Performance and design of the circuit

(1) Schematic circuit diagram.

(2) Resistance and capacitance values, tolerances, matching, tracking, power dissipation, temperature coefficients of resistors/temperature coefficients of capacitors where applicable.

(3) Limitations on resistance of conductors where applicable.

(4) Test circuit or method and performance limits.

(5) Added components (see 6.1.3 of IEC 60748-23-1).

6.3.4 Limiting conditions of use

Examples:

Operating temperature range

Vibration, shock, bump severities

Maximum voltage

Storage temperature range

Climatic category

NOTE Any interrelationship between the details specified in 6.3.3 and 6.3.4 shall be stated.

6.3.5 Derating

Where applicable, a derating curve is to be included in this subclause.

6.3.6 Related documents

A list of related documents with issue/date status should be given in this subclause.

6.3.7 Marking

The marking of the circuit and primary package shall be in accordance with the requirements of Clause 5 of IEC 60748-23-1.

The details of the marking of the circuit and primary package shall be given in full.

6.3.8 Ordering information

Orders for circuits covered by this specification shall contain the following information:

1) Quantity
2) Number of the detail specification with style reference and product assessment level number
3) Function of the circuit, if appropriate
4) Basic functional characteristics with tolerance, if appropriate.

6.3.9 Additional information (not for inspection purposes)

The detail specification may include information (which is not normally required to be verified by the inspection procedure) such as circuit diagrams, curves, drawings and notes for the clarification of the detail specification.

6.3.10 Additional or increased severities or requirements to those specified in the product assessment level schedule

These requirements may be specified in 6.4 of the detail specification, but do not modify the release level.

6.4 Inspection requirements

The detail specification shall prescribe the testing requirements for each delivery lot (see the Q-PALS of Clause 5 of this standard). This shall consist of all tests contained in the product assessment level schedule to which release is required, with the exception of those tests for which structural similarity may be invoked. The tests shall be subdivided into subgroup A, subgroup B, subgroup C and subgroup D. Additional tests or requirements shall be included where applicable. Full details shall be given of test condition, pin-outs, mounting methods, etc.

The content of any additional tests shall be as agreed between the manufacturer and the customer.

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Q1 Please report on **ONE STANDARD** and **ONE STANDARD ONLY**. Enter the exact number of the standard: *(e.g. 60601-1-1)*

.....

Q2 Please tell us in what capacity(ies) you bought the standard *(tick all that apply).* I am the/a:

purchasing agent ❑
librarian ❑
researcher ❑
design engineer ❑
safety engineer ❑
testing engineer ❑
marketing specialist ❑
other.....

Q3 I work for/in/as a: *(tick all that apply)*

manufacturing ❑
consultant ❑
government ❑
test/certification facility ❑
public utility ❑
education ❑
military ❑
other.....

Q4 This standard will be used for: *(tick all that apply)*

general reference ❑
product research ❑
product design/development ❑
specifications ❑
tenders ❑
quality assessment ❑
certification ❑
technical documentation ❑
thesis ❑
manufacturing ❑
other.....

Q5 This standard meets my needs: *(tick one)*

not at all ❑
nearly ❑
fairly well ❑
exactly ❑

Q6 If you ticked NOT AT ALL in Question 5 the reason is: *(tick all that apply)*

standard is out of date ❑
standard is incomplete ❑
standard is too academic ❑
standard is too superficial ❑
title is misleading ❑
I made the wrong choice ❑
other .....

Q7 Please assess the standard in the following categories, using the numbers:
(1) unacceptable,
(2) below average,
(3) average,
(4) above average,
(5) exceptional,
(6) not applicable

timeliness.....
quality of writing.....
technical contents.....
logic of arrangement of contents .....
tables, charts, graphs, figures.....
other .....

Q8 I read/use the: *(tick one)*

French text only ❑
English text only ❑
both English and French texts ❑

Q9 Please share any comment on any aspect of the IEC that you would like us to know:

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