INTERNATIONAL STANDARD

IEC 60747-16-10

QC 210021

First edition
2004-07

Semiconductor devices –

Part 16-10:
Technology Approval Schedule (TAS)
for monolithic microwave integrated circuits

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES –

Part 16-10: Technology Approval Schedule (TAS) for monolithic microwave integrated circuits

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 60747-16-10 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47E/257/FDIS	47E/262/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ-CECC).

This publication has been partially drafted in accordance with the ISO/IEC Directives, Part 2 (2001). It also follows the requirements given in IEC QC 210000:1995, Technology Approval Schedules – Requirements under the IEC Quality Assessment System for Electronic Components (IECQ-CECC).

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

International Electrotechnical Commission Quality Assessment System for Electronic Components (IECQ-CECC)		QC 210021
Responsible NAI:	Name Address Tel: Fax:	Specification available as shown in QC 001004 Specifications List or from any National Authorized Institution (NAI)
TECHNOLOGY APPROVAL SCHEDULE (Monolithic microwave integrated circuits)		  Issue QC 210021 2004-07

Foreword to this particular Technology Approval Schedule (TAS)

The IEC Quality Assessment System for Electronic Components (IECQ) is composed of those member countries of the International Electrotechnical Commission (IEC) that wish to take part in a harmonized system for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of specifications and quality assessment procedures for electronic components and by the granting of an internationally recognized mark or certificate of conformity. The components produced under the System are acceptable in all member countries without further testing.

This TAS has been prepared for use by those countries taking part in the System who wish to issue national harmonized specifications for Technology Approval of manufacturers of monolithic microwave integrated circuits. It should be read in conjunction with the current regulations of the IECQ-CECC System.

At the date of printing of this schedule the member countries of IECQ-CECC are China, Denmark, France, Germany, India, Italy, Japan, Republic of Korea, Netherlands, Norway, Russian Federation, Switzerland, Thailand, Ukraine, United Kingdom, USA and Yugoslavia. Copies of this schedule can be obtained from their National Authorized Institutions, National Standards Organizations or, in case of difficulty, from the Central Office of IEC in Geneva, Switzerland (fax 41 22 9190300) as described in the Specifications List QC 001004 on www.iecq-cecc.org.

Organizations responsible for preparing the present TAS

IEC subcommittee 47E: Discrete semiconductor devices

Preface

This schedule was prepared by SC47E/WG2.

It is based, wherever possible, on the publications of the International Electrotechnical Commission (IEC) and the International Organization for Standardization (ISO) and in particular on:

IEC 60747-16-1: Semiconductor devices – Part 16-1: Microwave integrated circuits – Amplifiers,

IEC 60747-16-2: Semiconductor devices – Part 16-2: Microwave integrated circuits – Frequency prescalers,

IEC 60747-16-3: Semiconductor devices – Part 16-3: Microwave integrated circuits – Frequency converters,

IEC 60747-16-4: Semiconductor devices – Part 16-4: Microwave integrated circuits – Switches.

INTRODUCTION

The requirements for Technology Approval for manufacturers of electronic and electro-mechanical components are given in QC 001002-3, Clause 6. The procedures for approval defined in that clause require the manufacturer to have available an appropriate Technology Approval Schedule (TAS).

This schedule defines how the principles and requirements of QC 001002-3, Clause 6 are applied to monolithic microwave integrated circuits.

SEMICONDUCTOR DEVICES –

Part 16-10: Technology Approval Schedule (TAS) for monolithic microwave integrated circuits

1 General

1.1 Scope

This TAS specifies the terms, definitions, symbols, quality system, test, assessment and verification methods and other requirements relevant to the design, manufacture and supply of monolithic microwave integrated circuits in compliance with the general requirements of the IECQ-CECC System for electronic components of assessed quality.

1.2 Normative documents

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60027 (all parts): *Letter symbols to be used in electrical technology*

IEC 60050: *International Electrotechnical Vocabulary*

IEC 60068 (all parts): *Environmental testing*

IEC 60191-2: *Mechanical standardisation of semiconductor devices – Part 2: Dimensions*

IEC 60617-DB[1] (all parts): *Graphical symbols for diagrams*

IEC 60747-1: *Semiconductor devices – Discrete devices and integrated circuits – Part 1: General*

IEC 60747-16-1: *Semiconductor devices – Part 16-1: Microwave integrated circuits – Amplifiers*

IEC 60747-16-2: *Semiconductor devices – Part 16-2: Microwave integrated circuits – Frequency prescalers*

IEC 60747-16-3: *Semiconductor devices – Part 16-3: Microwave integrated circuits – Frequency converters*

IEC 60747-16-4: *Semiconductor devices – Part 16-4: Microwave integrated circuits – Switches*[2]

IEC 60748-1: *Semiconductor devices – Integrated circuits – Part 1: General*

ISO 1000: *SI units and recommendations for the use of their multiples and certain other units*

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1 "DB" refers to the IEC on-line database.

2 To be published.

1.3 Units, symbols and terminology

Units, graphical symbols, letter symbols and terminology shall, whenever possible, be taken from the following documents:

IEC 60027: *Letter symbols to be used in electrical technology*

IEC 60050: *International electrotechnical vocabulary*

IEC 60617-DB: *Graphical symbols for diagrams*

ISO 1000: *SI units and recommendations for the use of their multiples and certain other units*

Any other units, symbols and terminology specific to the scope of this TAS shall be taken from the relevant IEC or ISO documents listed under Normative documents.

1.4 Standard and preferred values

Technology Approval allows the customization of the component or process to suit each customer. The conventional concept of preferred values may thus have limited application. However, when internationally recognized preferred values apply these should be used, e.g. voltage, temperature and dimensions. Reference shall be made to the appropriate IEC or ISO publications, i.e.:

– voltage IEC 60747-1
– temperature IEC 60747-1
– dimensions IEC 60191-2.

1.5 Definitions

For the purposes of this document, the following definitions apply.

1.5.1 General terms for monolithic microwave integrated circuits

1.5.1.1
microelectronics

(IEC 60748-1, definition 4.1.5)

1.5.1.2
microcircuit

(IEC 60748-1, definition 4.2.2)

1.5.1.3
integrated circuit

(IEC 60748-1, definition 4.2.3)

1.5.1.4
integrated microcircuit
microcircuit in which a number of circuit elements are inseparably associated and electrically interconnected such that for the purpose of specification and testing and commerce and maintenance, it is considered indivisible

NOTE 1 For this definition, a circuit element does not have an envelope or external connection and is not specified or sold as a separate item.

NOTE 2 Where no misunderstanding is possible, the term "integrated microcircuit" may be abbreviated to "integrated circuit".

NOTE 3 Further qualifying terms may be used to describe the technique used in the manufacture of a specific integrated microcircuit. Examples to the use of qualifying terms: semiconductor monolithic integrated circuit; semiconductor multi-chip integrated circuit; thin film integrated circuit; thick film integrated circuit; hybrid integrated circuit.

1.5.1.5
micro-assembly
microcircuit consisting of various components and/or integrated microcircuits which are constructed separately and which can be tested before being assembled and packaged

NOTE 1 For this definition, a component has external connections and possibly an envelope as well and it also can be specified and sold as a separate item.

NOTE 2 Further qualifying terms may be used to describe the form of the components and/or the assembly techniques used in the construction of a specific micro-assembly. Examples of use of qualifying terms: semiconductor multi-chip micro-assembly; discrete component micro-assembly.

1.5.2 List of abbreviations

– ASIC: Application Specific Integrated Circuit

– BDS: Blank Detail Specification
– BICMOS: Bipolar and Complementary Metal Oxide Silicon

– CAD: Computer Aided Design
– CAE: Computer Aided Engineering
– CECC: CENELEC Electronic Components Committee
– CMB: Contract Management Branch
– Cpk: Index of critical process capability

– Die Shear: Test on die attach
– DIL: Dual In Line Package
– DRC: Design Rules Check
– Dye Penetrant (ZYGLO): Seal test

– EDP: Electronic Data Processing
– EFR: Electrical Failure Rate
– ERC: Electrical Rules Check
– ESD: Electro Static Discharge

– GaAs: Gallium Arsenide

– HBT: Hetero-junction Bipolar Transistor
– HEMT: High Electron Mobility Transistor

– ISO 9000: ISO International Quality Rules

– JFET: Junction Field Effect Transistor

– LRM: Line Reflect Match
– LSSD: Level Sensitive Scan Design
– LVS: Layout Versus Schematics

– MESFET: Metal Semiconductor Field Effect Transistor
– MMIC: Monolithic Microwave Integrated Circuits
– MODFET: Modulation Doped Field Effect Transistor
– MTF: Mean Time to Failure
– MTBF: Mean Time Between Failures
– MTTR: Mean Time To Repair

– NMOS: Metal Oxide Silicon N channel

– OS: Operating System

– PAS: Publicly Available Specification
– PCM: Process Control Monitor
– PDA: Percentage Defectives Allowed
– PM: Parametric Monitor
– PMOS: Metal Oxide Silicon P channel
– POST CAP: Inspection after Encapsulation
– PRE CAP: Inspection before Encapsulation

– QA: Quality Assurance
– QCI: Quality Conformance Inspection
– QML: Qualified Manufacturer List

– RIE: Reactive Ion Etching

– SEC: Standard Evaluation Circuit
– SEM: Scanning Electron Microscope
– SI: Supervising Inspectorate
– SOI: Silicon on Insulator
– SOLT: Short Open Load Thru
– SOS: Silicon on Sapphire
– SPC: Statistical Process Control
– Si: Silicon

– TADD: Technology Approval Declaration Document
– TCI: Technology Conformance Inspection
– TCV: Technology Characterization Vehicle
– TDDB: Time Dependent Dielectric Breakdown
– TQM: Total Quality Management
– TRB: Technology Review Board
– TRL: Thru Reflect Line

– VT: Threshold Voltage for FET

– ZYGLO: see Dye Penetrant.

NOTE PCM and PM have the same meaning; however, PCM is the term used in the following subclauses.

1.5.3 Definitions relevant to the scope of the TAS

See QC 001002-3, Clause 6 for definitions specific to Technology Approval.

2 Definition of the component technology

2.1 Scope

The Technology Approval for the declared range or family of components shall include their design and manufacturing processes and their interfaces. The overall management of these interfaces by the Control Site shall be included. These processes and interfaces shall be declared within the Technology Approval Declaration Document (TADD).

More detailed requirements for the listed processes and interfaces to be included within the Technology Approval are given in the relevant clauses of this TAS. The processes are listed below with the identification of the MAIN TECHNICAL PROCESS:

- Process characterization
- Integrated circuit design – This is a MAIN TECHNICAL PROCESS
- Mask manufacture
- Wafer fabrication – This is a MAIN TECHNICAL PROCESS
- Back-side process
- Wafer probe
- Assembly – This is a MAIN TECHNICAL PROCESS
- Test and release – This is a MAIN TECHNICAL PROCESS
- Packaging and shipping

  Shipping includes the temporary storage of finished products before shipment to the customer.

2.2 Description of activities and flow charts

2.2.1 Description of activities

All the activities (processes) shall be identified with the relevant flow charts included. This information may include different processes for different types of components but covered by the same technology. Where applicable, these should address all the processes listed in 2.1.

The design and manufacturing cycle of integrated circuits may involve one or more qualified company or facility handing different tasks within the “life cycle” of an MMIC.

Design, development or specification of an MMIC is performed to the specific requirements of a customer, which may be an external customer (such as for an application-specific MMIC), or an internal department.

The prime contractor is that organization which undertakes the responsibility for the management of all tasks prior to the supply of an MMIC to the specified requirements.

2.2.2 Flow charts

The flow chart in Figure 1 is an example showing such operations, where the specific stages are expected to be defined, referencing the relevant internal documentation.

2.3 Technical abstract

2.3.1 TADD abstract (not for publication)

The Technology Approval technical abstract shall be declared by the technology approval declaration document (TADD).

For each technology declared the following shall be identified:

- Description of design tools used e.g. CAD systems, software;
- Description of wafer fabrication processes including feature size, technology, types and number of interconnects
  - e.g. 0,5 μm gate, GaAs MESFET, double layer metal;

- Description/list of products and/or family of products
  - e.g. low noise amplifiers; power amplifiers; switches;
- Description of packaging types/materials and range of pincounts
  - e.g. chip form: ceramic, DIL 8, 16 pin;
- Description of test equipment, i.e. type of test equipment and scope.

An example of a Technology Approval technical abstract is given in 2.3.3.

2.3.2 QC 001005 abstract

The information to be published within QC 001005:2000, Register of Firms, Products and Services approved under the IECQ-CECC System, including ISO 9000, may be based on the information given to satisfy the Technology Approval technical abstract of 2.3.1. Information marked with an asterisk ("*") may be omitted in the published "Abstract of Technology Approval" if requested by Control Site.

2.3.3 Example of a Technology Approval technical abstract

TECHNOLOGY DESCRIPTION: MONOLITHIC MICROWAVE INTEGRATED CICUIT

Manufacture [Control Site]: *Name and location*
IEC Reference: *QC 210021 – TAS for Monolithic Microwave Integrated Circuits*
Certificate Number: *Reference of the local SI*
TADD Generic: *Control Site's Document Reference*
(Cross references to other TADD shall exist in the Generic Specification where applicable).

LIBRARY/DESIGN
Manufacturer's name of the library:
Information on the library (where applicable):
Purpose: [ ] Microwave Design [ ] Digital Design [ ] Others
Types: [ ] Standard Cells [ ] Element Cells
Contents: Types of cells

WAFER FABRICATION:
Wafer Fabrication Process Name: *(e.g. "AMES0.5" etc.)*
Wafer Fabrication Process Type: *(e.g. FET/Bipolar etc.)*
Function: *(e.g. Standard Cell/Custom etc.)*
Production Families: *(e.g. Low Noise/High Power/Control etc.)*
Details:
Wafer Size: *(e.g. 100 mm)*
Gate Length: *(e.g. 0,5 µm)*
Maximum Interconnect Levels:* *(Triple/Double/Single Level/Metal etc.)**
Transmission line structure: (e.g. microstrip/coplanar waveguide etc.)
Metal Compositions:* *(Al/Si/Al/Cu etc.)**
Gate Material:* *(Metal/Polysilicon etc.)**
Passivation Material:* *(1,2 µm Compressive Nitride etc.)**
Substrate Material:* *(e.g. GaAs)**
Number of masks:* *(e.g. 8)**

ASSEMBLY:
Package types: *(e.g. Thin Plastic Quad Flat Pack, 7,6 mm Small Outline (SO) etc.)*
Details:
Maximum Die Size: *(e.g. TPQFP – 9 x 9 mm: SO300 – 2,3 mm x 2,3 mm)*
Package materials: *(e.g. Ceramic/Epoxy/Plastic etc.)*
Header/Leadframe:* *(e.g. Copper/Alloy 42 etc.)**
Pin/Lead Finish: *(e.g. Gold/Solder Dipped etc.)*
Die Attachment:* *(e.g. Silicon-Gold Eutectic etc.)**
Bond Wire Attachment:* *(e.g. Aluminium, Ultrasonic etc.)**
Package assembly

ELECTRICAL CHARACTERISTICS OF PRODUCTS:
Supply Voltage Range:
Maximum Input Power:
Total Power Dissipation:
Maximum Operating Frequency:
Operating Temperature Range:
Storage Temperature Range:

ENVIRONMENTAL/RELIABILITY LIMITS:
Endurance Test Performance: *(e.g. > x year at 55 °C or > 1 000 h at 125 °C)*
Accelerated Damp Heat Severity: *(e.g. > x year at 55 °C/60 % RH or 1 000 h at 85 °C/85 % RH)*
Temperature Cycling Extremes: *(e.g. –65 °C / +150 °C)*
etc.
AND
Expected Failure Rate *(under specified environments)*
Quality Factor (π_Q).

(The limits of approval shall be made available to the customer, and any tests should correlate to IEC test methods and should be suitable for the intended application.)

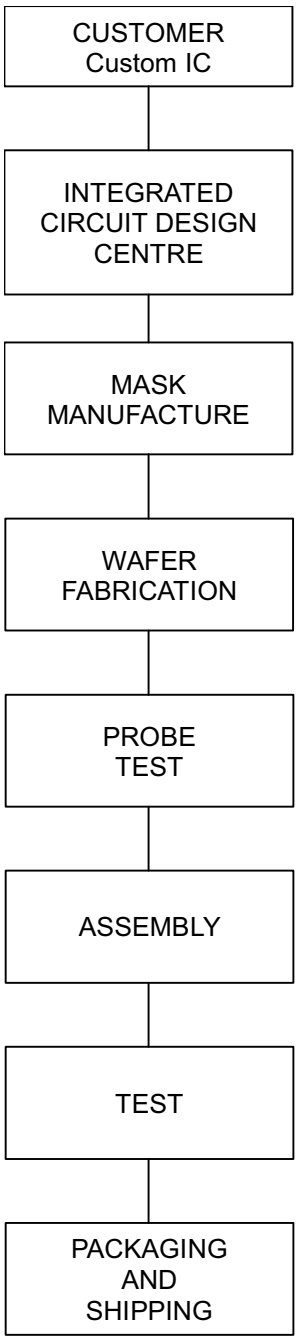
2.4 Requirements for control of subcontractors

Where a technical process as defined in 2.1 is subcontracted, the procedures and criteria employed to demonstrate control shall be specified. This may be achieved either by the demonstration of conformance to the requirements of the appropriate PAS (Publicly Available Specification) in the IECQ-CECC 200000 series, or by demonstrating that the processes have been satisfactorily performed in accordance with criteria defined or referenced from the TADD. Such criteria shall be capable of demonstrating compliance with the declaration of reliability and environmental performance.

The following items shall be specified:

- Reason for subcontracting
- Name and address
- IECQ-CECC Process and Approval or Technology Approval certificate reference (where appropriate)
- Name of CMB (Contract Management Branch) contract within the subcontractor
- Documentation
- Interrelationship documentation.

NOTE Design, mask manufacture, wafer fabrication, wafer probe, assembly, testing, packaging and shipping may be subcontracted provided that the control site has the capability for at least one of the MAIN TECHNICAL PROCESSES as defined in 6.2.1.3 of QC 001002-3.



NOTE This is an example of a packaged device.

Figure 1 – Example flow chart of design/manufacture/test

3 Component design of MMICs

3.1 Scope

Design information relevant to the technology for which approval is sought shall be included in the TADD.

This shall include design of the semiconductor process incorporating modification and publication of the process parameters and related process design rules in the form of written and computer files suitable for use in CAD tools at either internal customers or independent design centres.

Process characterization and circuit design are, in general, separate though inter-related tasks, and so their interfaces with the process design task shall be specified in detail, including management responsibilities, transfer specifications, requirements and deliverables.

The IC design centre is responsible for the design of integrated circuits in accordance with customer requests as defined by product or other specifications, generally by translation from received data into IC specifications, then design and simulation phases followed by production of data, specifications, and computer files (or equivalent) required for manufacturing. This shall generally employ data from the process design task.

Activities may include mask making and writing product test programmes or test data suitable for development into test programmes by a test centre or task.

3.2 Description of activities and flow charts

3.2.1 Description of activities

The activities of design for integrated circuits shall be declared, including flow charts showing all activities, critical steps, check points and quality indicators, referencing the relevant internal documentation. These shall include any or all of items a) to e) below, as appropriate:

a) Feasibility

The availability of equipment and of the design/manufacturing capacity to cover the required production lot quantities shall be verified.

b) Process design

i) Physical characteristics (required for circuit design)

ii) Electrical characteristics

iii) Layout rules.

c) Design services and support

i) Design Rule Checker (DRC)

ii) Layout Versus Schematic (LVS)

iii) Process rules (wafer fab and assembly)

iv) CAD Models.

d) Circuit design tools

i) Linear simulation (frequency domain)

ii) Harmonic balance

iii) SPICE

iv) Electromagnetic analysis

v) Other.

e) Conversion or adaptation of existing designs

Any activities not so described shall be stated with reference to the relevant documentation and interface controls. The information to be listed, where applicable, concerns:

i) basic technologies (processes, layers, elements, geometries, described in design book, etc.);

ii) design rules identification (including physical, electrical and layout for wafer fab and assembly also described in design book);

iii) CAD data and tools for each type of component e.g. hardware, software and cell libraries generally part of the design kit;

iv) verification and validation procedures;

v) package selection or design procedures;

vi) test programmes (e.g. test description language, test parameters, etc.).

3.2.2 Flow charts

For an example of a typical flow chart, see Figure 2.

3.3 Interfaces

3.3.1 Design/manufacture

The manufacturing interrelationship during the design stages shall be declared, including those with

– manufacturing (mask manufacture and/or fabrication),
– management of software configuration and library updates,
– upward compatibility,
– documentation,
– traceability,
– usage limits (model, accuracy),
– usage of verification tools (DRC, ERC, LVS),
– assembly (including package suppliers),
– prototyping (if applicable),
– characterization and test (including equipment and specifications),
– any other requirements.

3.3.2 Customer/user

The design centre defines its policy related to the involvement of the customer during the various design steps:

- Specifications
  - writing the technical need specification.
- Design reviews
  - functional simulation,
  - test oriented simulation ,
  - place and electromagnetic simulation.

- Prototyping (if applicable)
  - characterization and evaluation of prototypes.

The design centre is responsible for the application of the design and fabrication rules related to the identified technology. It is also responsible for the correct test methodology to fulfil the requirements of the technical need specification.

3.3.3 Interface with test centre

An identification and description of the interface between the design centre (responsible for the implementation of testability inside the circuit and test element group generation) and the entity realising, controlling and running the tester and the test programme shall be made.

A description shall be given of the methodology concerning:

– evaluation and tests on characterization of prototypes (if applicable);
– evaluation and tests on wafers (probing);
– evaluation and control of finished products;
– evaluation and tests to investigate failures mechanisms.

3.3.4 Vendor software capability

a) Software transparency/portability

This subclause outlines the steps to be taken to ensure that a piece of software is transparent and portable.

b) Definitions

Portability

The software is applicable to different processes, e.g. several MMIC processes. Portability can be to different levels, e.g. a piece of software can be used

– for 0,5 μm processes only,
– or for all 0,25 μm and 0,5 μm processes,
– or for all MMIC processes from a specific manufacturer, etc.

Transparency

The degree to which the software handles the details of the chip design without detailed knowledge from the user, e.g.:

– Software with little transparency is that currently used for full custom design where the software is merely a tool for layout/simulation etc., and the designer makes all the decisions.

This leads to several issues to be addressed primarily by the software vendor. To identify the degree of transparency/portability, attention is paid to the following points:

i) If vendors claim their software to be portable some sort of benchmarking must be carried out.

ii) The qualification level of personnel used as MMIC designers will vary according to level of transparency/portability, e.g. they may be educated in, say, MMIC design techniques, but need no knowledge of a particular process; or, with a higher level of design software, they need know nothing about microwave elements at all.

iii) The configuration of the design on the computer also needs to be transparent to the user, i.e. the software vendor should take responsibility for the configuration control.

iv) Software vendor sets up and funds a system (e.g. a user group) to ensure that all user problems are identified and corrected.

v) A version of design software may be changed part way through a design, requiring the transfer of files or cells produced using one version to another version. In such a case, the designer shall make a record of the file/cell name thus transferred, giving the name of the file just prior to transfer, the name just after transfer and the date of transfer. This will ensure traceability in the case of errors due to software bugs appearing at a later date.

3.3.5 Subcontractors, vendors and internal suppliers

Design may be subcontracted in accordance with 2.4.

3.4 Validations and control of the processes

3.4.1 Global design methodology

The methodology used to define the overall design process shall be described, and shall include:

– structure of design;
– testability of the design topology;
– documentation.

3.4.2 Validation of simulation results against technical needs specification

The methodology to cover the technical need specification shall be defined. The following points should be covered:

– stability in all frequency range (with a large signal simulation);
– stability in all power supplies for pulsed operating conditions;
– process variations and sensitivity analysis;
– application of Monte Carlo method to yield forecasting;
– thermal analysis for power devices;
– effect of bonding – decoupling capacitors - packaging;
– reverse modelling (if applicable).

3.4.3 Layout verification

Layout verification shall comprehend specific design rules that are process oriented and are used for one specific design and any additional design related information that is not defined in the data sheet (if applicable) such as:

- Geometric definitions and physical limits
- Electrical
  - layout versus schematic,
  - electromagnetic simulation (including proximity effects between microwave elements),
  - reverse modelling.
- Reliability, including electromigration/current density and thermal consideration.

3.4.4 Validation procedure

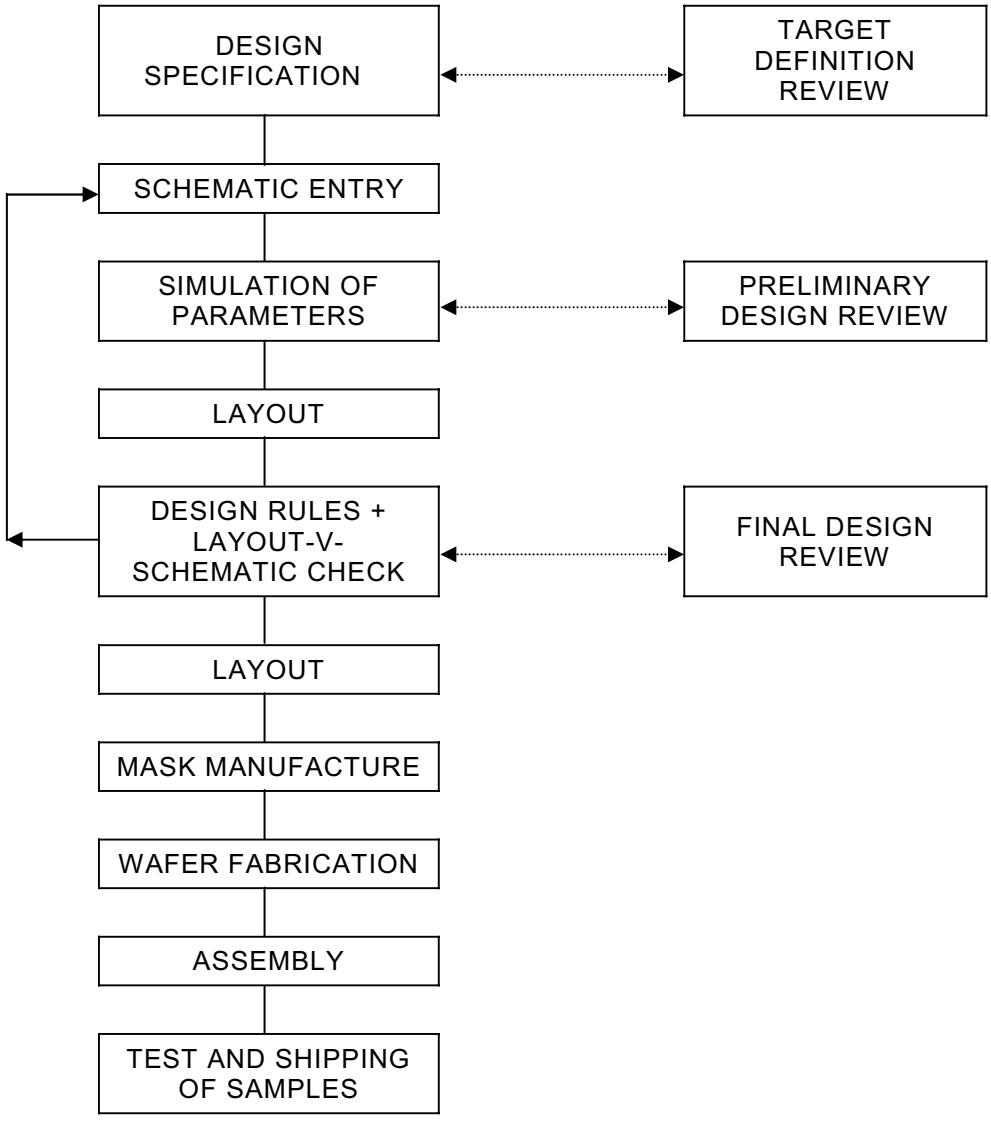
The procedure for validation and control of the design shall be defined.

Where applicable, any information required from processing or testing during the design validation stage shall be identified when it is required to avoid problems during production processing or testing, or which may affect reliability.

Before incorporation into the design system, any new software shall be checked and validated.

Procedures shall be identified which cover:

– testability;
– design rules to minimize failure mechanisms (electromigration, ESD);
– adequacy of test programmes;
– adequacy of test evaluation.



NOTE This is an example of packaged device.

Figure 2 – Example flow chart for an integrated circuit design

4 Mask manufacture

4.1 Scope

This clause defines the requirements for the manufacture of masks used to define circuit elements during wafer fabrication and gives requirements for the validation of processes and subcontractors.

4.2 Description of activities and flow charts

Mask manufacture may be solely owned by the MMIC wafer fabrication company or by an independent company. In either case the activity requirements, control, process checkpoints and quality indicators shall be treated identically.

The requirements for the mask manufacturer shall be declared, showing management and control of hardware/software.

Typically this would include:

– design rules;
– CAD data and rules;
– identification procedures.

4.3 Validation and control of the processes

The method of control and validation of finished masks or their manufacturing processes shall be defined to ensure that the finished masks comply with the original design and procurement requirements:

– name and address;
– proof of approval of the mask manufacturing process for the certified wafer fab process;
– name of the TRB contact within the mask manufacturer;
– identification of the process specifications of the mask manufacturer;
– a summary of the interface between the design centre and the mask manufacturer, listing documents, tools etc. delivered by the design centre, the methodology used to validate the work done by the mask manufacturer and the responsibilities of each party.

4.4 Subcontractors, vendors and internal suppliers

Mask manufacture may be subcontracted in accordance with 2.4.

5 Wafer fabrication of MMICs

5.1 Scope

This clause describes the activities, equipment and re-work rules for the wafer fabrication of monolithic microwave integrated circuits and gives requirements for the validation and control of processes and subcontractors.

The wafer fabrication activities include the physical realization of monolithic microwave integrated circuits on semiconductor substrates by means of the necessary tools, methods, operations and their management, performed in-house by a qualified task of facility or by a separate qualified foundry.

The wafer fabrication facility may either

a) receive and employ suitable masks and/or CAD data from a qualified task or facility, or

b) receive the data from the design task and employ an internal or external mask maker.

For either case, it is responsible for the management of the interfaces, the process materials and equipment and the delivery of wafers to its customers.

Wafer fabrication information relevant to the technology for which approval is sought shall be included in the TADD.

5.2 Description of activities and flow charts

5.2.1 General requirements

The critical operations to be monitored shall be determined based on experience and knowledge of the process. The data coming from the process line shall be analysed using accepted SPC methods to determine their effectiveness in controlling the process. If the effectiveness of the critical operation is found not to adequate, it is necessary to change the measurement condition or to acquire another data. A wafer fabrication monitoring system may use various test structures, measurement methods and techniques.

A TQM (Total Quality Management) methodology shall be employed in which the wafer fabrication centre is responsible for its own quality, has set up the organization and resources to manage it (including TRB) and is able to report its effectiveness to the Supervising Inspectorate (SI) (either directly or via the Control Site).

5.2.2 Description of activities and flow charts

The activities of wafer fabrication for monolithic microwave integrated circuits shall be declared, including flow charts showing all activities, critical process steps, parameters, process check points and quality indicators, used for the validation and control of the process and subcontractors. The major criteria used to describe the technology shall be identified.

Examples of critical operations include:

Environment

Wafer materials preparation

- incoming acceptance/QC;
- substrate (front side, back-side, size, orientation);
- epitaxial wafer (material, dopant, VPE, MBE, MOCVD).

Wafer processing techniques (each layer)

- photolithography;
- electron-beam-lithography;
- doping;
- etching;
- layer deposition:
- coating;
- interconnection;
- step coverage;
- metallization;
- passivation;
- thinning;
- back-side process (via-hole).

Process monitors and acceptance

Documentation shall be referenced to define or control the main properties of the technology, i.e.:

– fabrication location;
– basic technology (MESFET, HEMT, MODFET, HBT, etc.);
– mono or multi level interconnection;
– isolation method (mesa etching, ion implantation, etc.);
– nature of the gate (Al, WSi, WN, Ti, etc.);
– nature of the dielectric (SiO, SiN, etc.);
– nature of the bipolar emitter (walled, nonwalled);
– new manufacturing techniques;
– photo-optic, E-Beam;
– diffusion, implant;
– deposition, growth;
– wet etching, dry etching;
– photo-etching, lift off;
– evaporation, pulverization;
– scribe line.

The control of these processes shall focus upon those parameters, which are critical for the quality assurance of the products in term of performance, yield and reproducibility (capability), and reliability. For example, the following shall be detailed:

– Layer thickness of final products
– Surface dimensions
– Superposition spread (overlapping/alignment)
– Wafer diameter
– Die final thickness
– Back
– Resistivity
– Breakdown voltage
– Threshold voltage.

Example of a typical flow chart: see Figure 3.

5.2.3 Quantitative physical and electrical limits

The characteristics limits used in each step of the flow chart shall be defined for the production process and classified when necessary as

– original – where the processes are not yet used to make products under assessed quality;
– distinguished – where the processes are already used to produce qualified products with lower performing or constraining limits.

5.3 Equipment

The equipment for the manufacturing of the standard evaluation component the technology characterization vehicle the parametric monitor and the finished products shall be specified including a description of the following characteristic parameters:

– General characteristic (manufacturer, date of manufacturing, intended purpose)
– Functional requirements (electrical power consumption, cooling requirements, heating requirements, environmental requirements)
– Installation procedure (parts description, mounting description, interconnection scheme description)
– Commissioning into operation
– Specification for required material
– Reliability (minimum-typical-maximum values, derating expected lifetime, MTBF).

Maintenance programmes for the equipment shall be defined (including detailed, instructions on maintenance procedures, list of tools required for maintenance, periodicity of maintenance).

The whole, or essential parts, of the equipment shall be calibrated periodically in order to maintain accuracy. The calibration system and the applied calibration methods shall be defined, including:

– formal calibration procedure;
– short calibration procedure to monitoring equipment;
– calibration responsibility;
– calibration requirements (list of calibration tools, equipment, meters and gauges);
– calibration periodicity.

5.4 Materials

Control and validation of materials used for fabrication of wafers shall be defined, including:

– follow-up, supplier's quotes, multiple sourcing policy;
– materials inspection (methods, tools, results analysis and use);
– materials management and stocks (store, traceability, limited life time products).

5.5 Re-work

Re-work shall only be allowed where it can be demonstrated that it does not influence the quality and reliability of the product. The documentation shall specify all permitted rework processes/stages together with the criteria for their use, performance and satisfactory completion.

No rework may be performed prior to its approval as a permitted rework operation. The reason for the rework shall be recorded in the lot history, together with all the details of the rework performed, the results of the rework and the consequences of the rework on further manufacturing stages. The criteria for permitting rework shall be fully documented in the TADD.

Repair is not allowed in the wafer fabrication process. For wafer fabrication, repair is redefined as "Any operation which is performed to correct nonconformance or error and which results in the finished wafer having any feature, characteristic, or material which is different to that of a wafer manufactured to the specified approved process."

5.6 Validation methods and control of the processes

The procedures used for validation and control of the processes shall be declared. Procedure for controlling and validating processes using statistical methods based on experimental data and knowledge of the processes shall be declared.

The direct responsibility of the TRB in the control of quality allows control of ongoing minor changes of techniques and technologies for assembly and packaging without requiring recertification. In the wafer fabrication centre, the TRB is either composed of the personnel managing its activities or they are represented in a TRB at a higher level.

5.6.1 Acceptance plan for wafer

The TRB shall create and demonstrate the effectiveness of a plan based on electrical measurements of PCM. If applicable, visual criteria shall also be used. This plan may be a wafer-by-wafer or lot-by-lot acceptance plan, but shall correspond to the production grouping of various types of lots:

– small lots;
– large lots;
– special lots.

PCM data shall be recorded and available during audits.

5.6.2 SPC/Statistical process control programme, applicability

A wafer fabrication data analysis system shall be used by the manufacturer to monitor process critical points and manage yield and reliability. This system shall be contained within the overall qualify plan described within the TADD. The monitoring system may use various test structures, measurement methods and techniques. The critical operations to be monitored are determined by the manufacturer on the basis of its experience and knowledge of its process. The data coming from the process line are analysed according to suitable SPC methods to determine their effectiveness in controlling the processes.

[SPC guidance is given in CECC 00 016: Basic requirements for the use of Statistical Process Control (SPC) in the CECC System, available from the IECQ-CECC Secretariat.]

5.6.3 Process capability demonstration (i.e. statistical capability)

During the certification phase, the manufacturer shall produce circuits, run test and benchmarks in order to demonstrate its ability to evaluate the process capability in terms of quality, reliability and effective capability to run production. Summaries of these tests are submitted to the SI during the validation audit. These tests are carried out in order to establish a continuous capability monitoring apart from the initial demonstration. The TRB determines when these tests shall be done after the initial certification.

5.6.4 Technology validation

The technology flow chart of the process, which is described in 5.2.2, is audited as a whole to verify conformance. Critical operations in 5.2.2 should be described in this flow chart. For an example of a typical flow chart, see Figure 3.

[Critical points are given in the guidance document CECC 00 809: Questionnaire for auditing IC and ASIC manufacturing lines, available from the IECQ-CECC Secretariat, which may be used as a guide for the technical validation audit.]

5.6.5 Test vehicles

The wafer fabrication process is monitored and controlled by a standard evaluation circuit (SEC), a technology characterization vehicle (TCV) and a process control monitor (PCM). The fabrication flow chart leading to finished products shall be established with clear limits for each fabrication step. These limits shall be specified.

5.7 Interrelationship

5.7.1 Customer/user

The customer interrelationship during wafer fabrication which shall be declared for

– design,
– packaging,
– test,
– prototyping (if applicable),
– characterization,
– reviews,
– any other requirements.

5.7.2 Subcontracting

Wafer fabrication may be subcontracted in accordance with 2.4.

Subcontractor arrangements for the initial design phase shall be defined to cover the following topics:

– design reviews;
– availability of process design rules including permissible variable of the physical and electrical characteristics;
– notification of process changes that could affect design, physical and electrical characteristics and performance;
– design and acceptability of PCMs and SECs;
– the manners in the circuits have to be delivered for the prototyping phase, and then for full production (if applicable);
– where applicable, a list of documents and tools to be transferred to the wafer fabricator, and the list of follow-up, control and test documents that shall be delivered with the circuits and allow traceability.

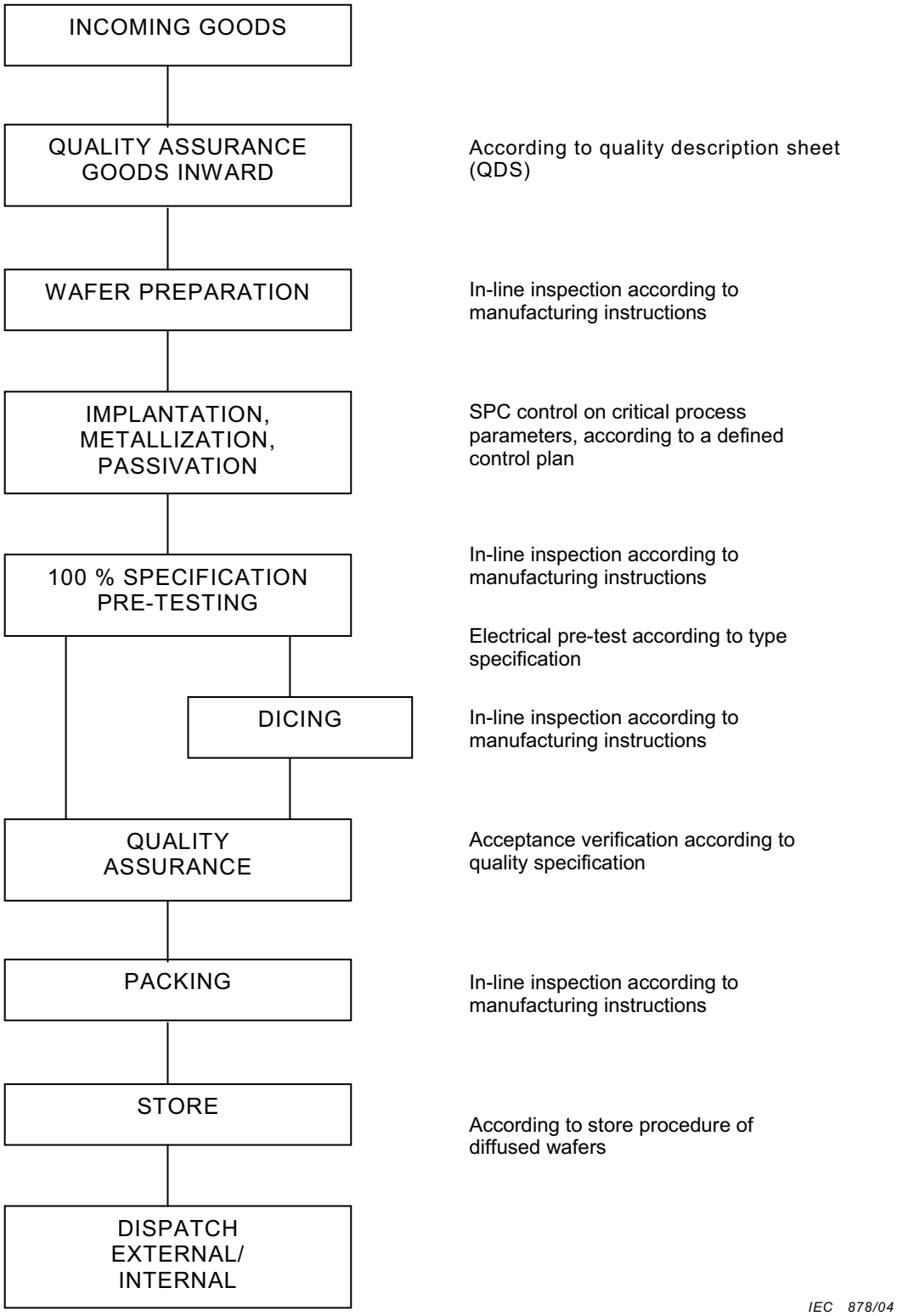


Figure 3 – Technology flow chart of the process

6 Wafer probing of MMICs

6.1 Scope

Wafer probing management and control formation relevant to the technology for which approval is sought shall be declared.

6.2 Description of activities and flow charts

The activities of probing of integrated circuits, showing quality indicators, shall be declared. Examples of such activities include:

– atmospheric and cleanliness control;
– washing and wafer control;
– control and preparation of probe card.

For examples of a typical flow chart, see Figure 4.

6.3 Equipment

Information on the test equipment used, and the intended range shall be provided. Maintenance and calibration programmes for the equipment shall be included. The information should cover:

– test equipment verification;
– device complexity (analogue, digital and mixed);
– types of measurements (DC, RF, dynamic, static, parametric);
– temperature test equipment (e.g. hot chuck);
– registration and control of type specific jigs, tools and fixtures.

6.4 Test procedures

The requirements for detailing procedures for the handling, control and use of test programmes shall be declared, including any relevant information not previously provided (i.e. validation and compliance procedures).

6.5 Interrelationship

6.5.1 Customer/user

The customer interrelationship during design stages shall be declared for:

– specifications;
– design reviews;
– manufacturing/fabrication;
– assembly (including package suppliers);
– prototyping (if applicable);
– characterization and test (including equipment and specifications);
– any other requirements.

6.5.2 Subcontracting

Wafer probing may be subcontracted in accordance with 2.4.

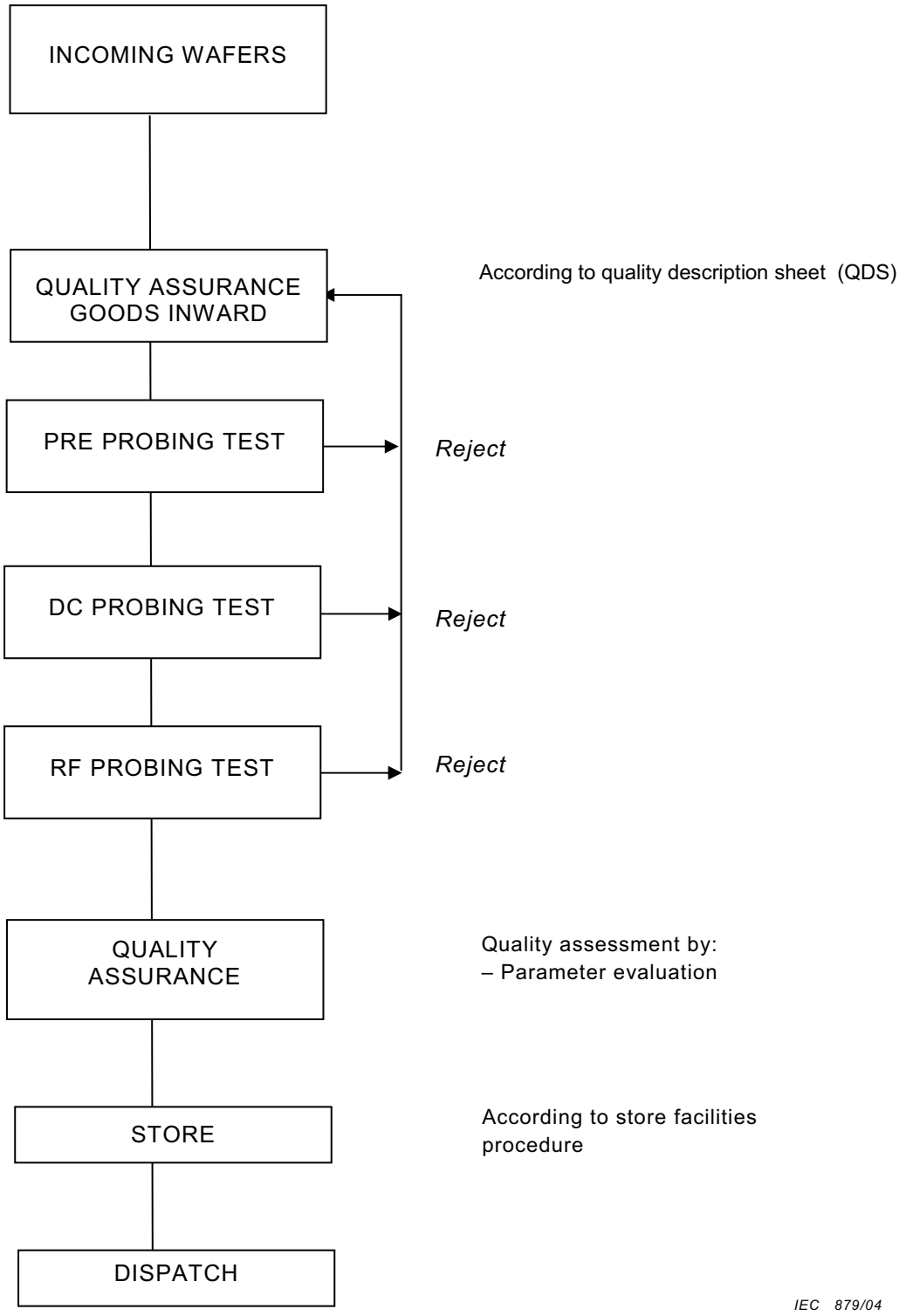


Figure 4 – Example flow chart for a wafer probing

7 Back-side process for bare chip delivery

7.1 Scope

This clause describes the activities, equipment and materials rules of the back-side process for bare chip delivery of monolithic microwave integrated circuits and gives requirements for the validation and control of processes and subcontractors.

The back-side process activities include the thinning wafers and making via-holes on semiconductor substrates by means of the necessary tools, methods, operations and their management, performed in-house by a qualified task of facility, or by a separate qualified foundry.

Back-side process information for bare chip delivery relevant to the technology for which approval is sought should be included in the TADD.

For a delivery of bare chip, on-wafer RF measurement should be carried out after the via-hole process completion; the details of measurement are given in 9.4.

7.2 Description of activity and flow charts

7.2.1 General requirements

The critical operations to be monitored shall be determined based on experience and knowledge of the back-side process.

A TQM (Total Quality Management) methodology shall be employed in which the wafer fabrication centre is responsible for its own quality, has set up the organization and resources to manage it (including TRB) and is able to report its effectiveness to the Supervising Inspectorate (SI) (either directly or via the Control Site).

7.2.2 Flow charts

The activities of back-side process for bare chip delivery of monolithic microwave integrated circuits shall be declared, including flow charts showing all activities, critical process steps, parameters, process check points and quality indicators, used for the validation and control of the process and subcontractors.

The major criteria used to describe the technology shall be identified. Examples of critical operations include:

– mechanical thinning;
– chemical thinning;
– via hole etching;
– metallization;
– dicing;
– etching cut;
– scribing;
– visual inspection;
– expansion;
– picking;
– packing.

The control of these processes shall focus upon those parameters, which are critical for the quality assurance of the products in term of performance, yield and reproducibility (capability), and reliability. For example, the following shall be detailed:

– wafer thickness;
– via hole diameter;
– back-side metal thickness;
– chip size.

The activities for packing and shipping shall be identified for bare chip delivery. Examples of such activities include:

– environment and cleanliness of the area;
– ensuring compliance with customer order;
– protection against environmental change;
– protection against mechanical damage;
– protection against electrical damage;
– documentation/labelling.

For examples of a typical flow chart, see Figure 5.

7.3 Equipment

Information on the back-side process equipment and the intended range shall be declared. Maintenance and calibration programmes should be included. All equipment used for manufacturer of finished products should comply with requirements given in 5.3.

7.4 Materials

Control and validation of materials used for back-side process shall be defined, including:

– follow-up, supplier’s quotes, multiple sourcing policy;
– materials inspection (methods, tools, results analysis and use) ;
– materials management and stocks (store, traceability, limited life time products).

7.5 Validation methods and control of the processes

The procedures used for validation and control of the processes shall be declared. Procedure for controlling and validating processes using statistical methods based on experimental data and knowledge of the processes shall be declared.

The direct responsibility of the TRB in the control of quality allows control of ongoing minor changes of techniques and technologies for assembly and packaging without requiring recertification. In the wafer fabrication centre, the TRB is either composed of the personnel managing its activities or they are represented in a TRB at a higher level.

7.6 Interrelationship

7.6.1 Subcontracting

Back-side process for bare chip delivery may be subcontracted in accordance with 2.4.

7.6.2 Interface with customer

The customer interrelationship during back-side process shall be declared for:

– design;

– visual Inspection;

– reviews;

– any other requirements.

7.7 Validity of release

The validity of release period shall be declared. Evidence shall be made available to assure that product released within this period conforms to the declared IECQ-CECC/customer/application quality and reliability requirements.

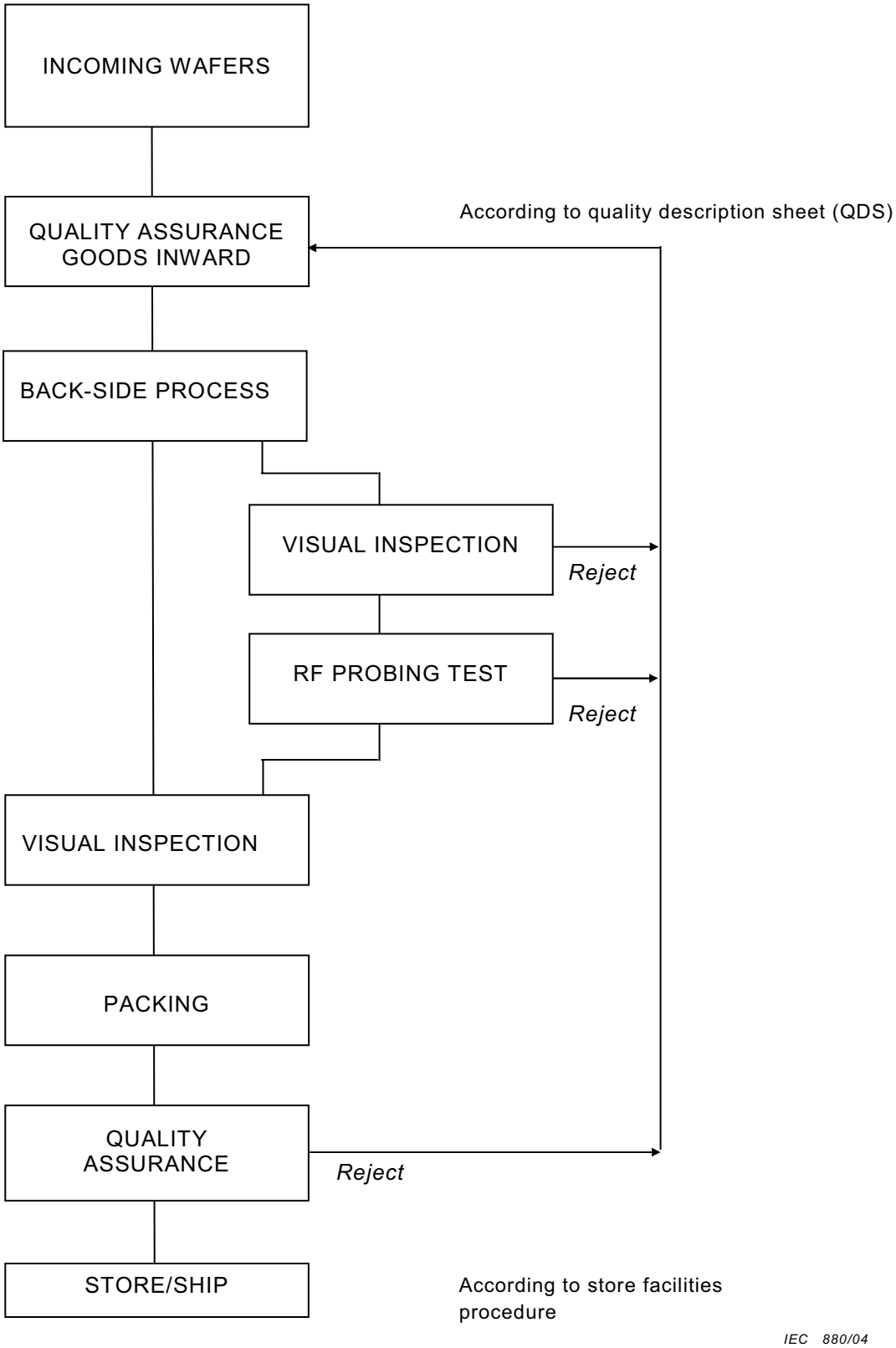


Figure 5 – Example flow chart for a back-side process for bare chip delivery

8 Assembly of MMICs

8.1 Scope

This clause describes the activities, material inspection and handling equipment and rework rules for the assembly of MMICs and gives requirements for the validation and control of processes and subcontractors.

This activity processes wafers or die coming from wafer fabrication or probe tests and delivers packaged MMICs to the test activity; it includes the management of the operations from receipt of wafers (or dice) to supply of packaged products, including assembly, bonding and final scaling/encapsulation.

Assembly information relevant to the technology for which approval is sought shall be declared.

8.2 Description of activities and flow charts

This description takes into account the TQM (Total Quality Management) concept where the concerned entity is responsible for its own quality, has set up the organization and tools to control it (by TRB for example) and is able to demonstrate this to the SI by visible results.

The activities of the assembly of MMICs shall be declared, including flow charts showing all activities, critical steps, check points, tools, parameters or part and quality indicators. Examples of such activities include:

– environment and cleanliness control;
– handling (ESD) ;
– stocking;
– lot formation;
– wafer Inspection;
– dicing;
– scribing;
– etching;
– die separation;
– die preparation;
– optical selection (microscope or automatic equipment) ;
– eutectic die attach (brazing) ;
– non-eutectic die attach (epoxy) ;
– inverted attach;
– die to package interconnect (wire bond, etc.) ;
– bond pull;
– die shear;
– precap inspection (microscope) ;
– packaging (sealing or moulding) ;
– lead trim, form and finish;
– marking (offset, screen printing, laser, etc.) ;
– screening – selection and electrical testing designed to provide feedback to assembly processes.

For an example of a typical flow chart, see Figure 6.

8.3 Materials, inspection and handling

Relevant information regarding the verification and control of incoming materials shall be declared, including their processing, handling and storage requirements. The controls shall include environmental/lifetime requirements.

Where relevant, there shall be vendor approval programmes to minimize the dependency upon incoming inspection with process or quality control requirements (including statistical techniques where appropriate) placed upon the supplier of the materials. The programmes shall include as a minimum:

– a description of the quality plan of the supplier and the change reports covered by the TRB;
– a documented “Certificate of Conformity” approved by the TRB included in the incoming inspection procedure;
– a description of the change notice procedure used by the supplier;
– a quality management procedure that may be split between the supplier and the user or taken over totally by one or the other.

8.4 Equipment

Information on the assembly equipment and the intended range shall be declared. Maintenance and calibration programmes shall be included. All equipment used for manufacturer of finished products shall comply with requirements given in 5.3.

8.5 Re-work

Re-work shall only be allowed where it can be demonstrated that it does not result in the finished component having any feature, characteristic (including quality and reliability performance) or material that is different to that of a component manufactured to the specified approved process. Only rebonding of wire with manual wire bonding equipment is permitted and only prior to encapsulation. Allowable rework of packages includes cleaning, remarking to correct defective marking and lead straightening.

The documentation shall specify all permitted rework process/stages together with the criteria for their use, performance and satisfactory completion. If rework is required on an assembly lot, the reason for the rework shall be recorded on the lot history, together with all the details of the rework, and the consequences of the rework, on further manufacturing stages. The criteria for permitting rework shall be fully documented in the TADD.

Repair is not allowed in the assembly process. For assembly of MMICs, repair is redefined as “Any operation which is performed to correct non-conformance or error and which results in the finished assembly of MMICs having any feature, characteristic or material which is different to that of an assembly of MMICs to the specified approved process.”

8.6 Validation and control of the processes

The procedures used for validation and control of the processes shall be declared. Procedures for controlling and validating processes using statistical methods based on experience and knowledge of the processes shall be declared. Refer to CECC 00016, available from the IECQ-CECC Secretariat, for guidance on SPC and critical parameters.

The direct responsibility of the TRB in the control of quality allows control of ongoing minor changes of techniques and technologies for assembly and packaging without requiring recertification. In the assembly site, the TRB is either composed of the personnel managing its activities or they are represented in a TRB at a higher level.

8.7 Interrelationships

8.7.1 Subcontracting

Assembly may be subcontracted in accordance with 2.4.

8.7.2 Interface with wafer fabrication

The package characteristics required to allow acceptable mounting, bonding and encapsulation of dies within each certified package family or type shall be identified.

8.7.3 Interface with design

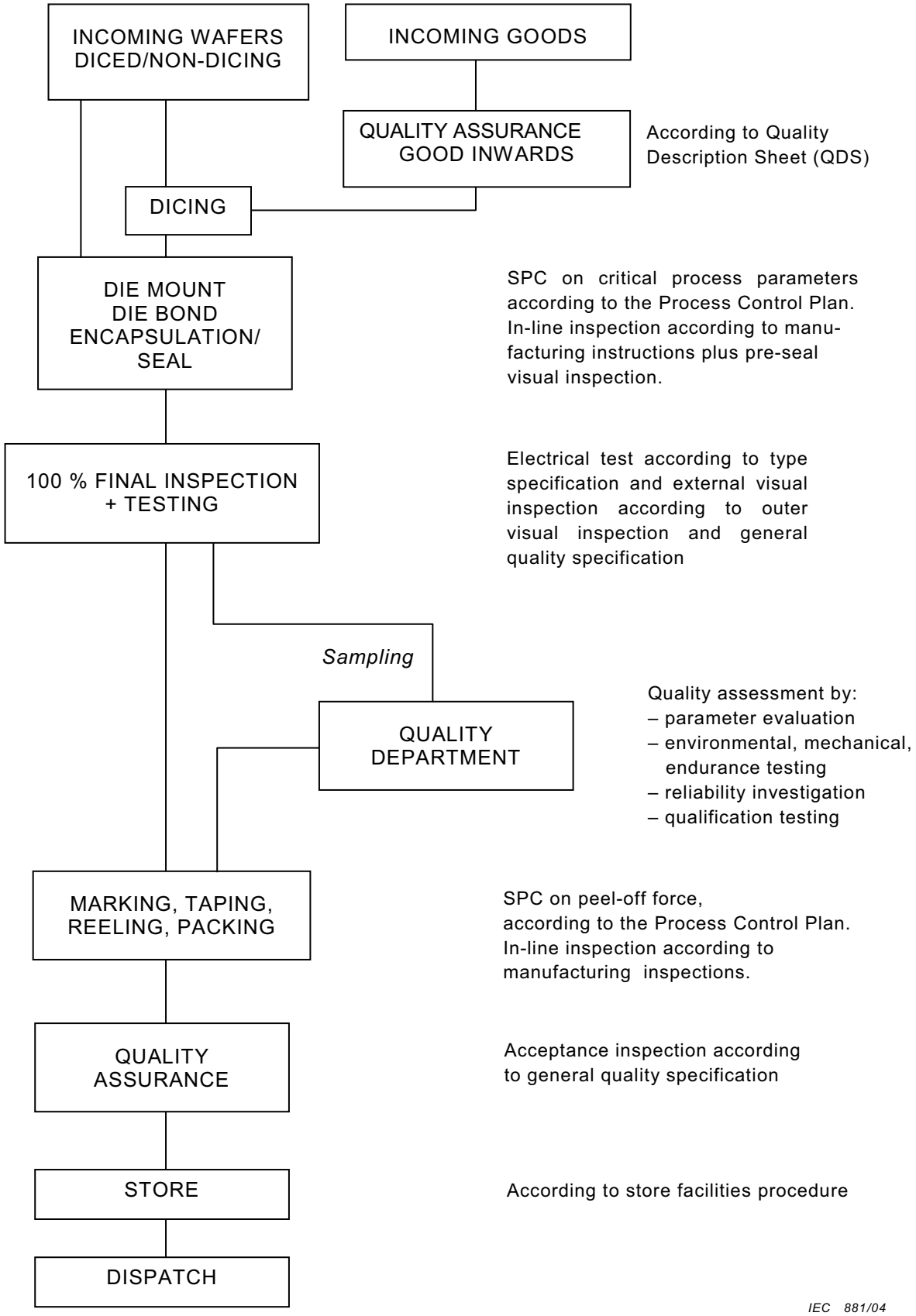
Characterization data shall be available to the design centre containing the following items:

- Thermal
  - identification of elements dedicated to the power dissipation (Inertia block);
  - the value of the thermal resistance.
- Electrical
  - identification of specific characteristics related to the electrical isolation of packages;
  - ground and power supply impedance;
  - cross coupling effects;
  - high voltage effects;
  - high current effects.
- Physical
  - physical constraints (dimensions etc.);
  - limits of environmental qualification;
  - pin layout.

8.7.4 Interface with customer

The customer interrelationship during assembly shall be declared for:

– design;
– fabrication;
– test;
– characterization:
– reviews;
– any other requirements.



NOTE This is an example of a packaged device.

Figure 6 – Example flow chart for an assembly

9 Testing of MMICs

9.1 Scope

The objective of this clause is to identify the elements defining the limits of the capability of the test process, applicable quality procedures and points covered by the certification and qualification by the SI. These shall cover the conformance testing to electrical specifications of partly or wholly finished products (which may include wafers).

The test facility may also undertake the development of software tools and programmes for final testing and/or process characterization. However, these activities may also be performed as part of the CAD/Design process or subcontracted to qualified facilities.

Test centre information relevant to the technology for which approval is sought shall be included in the TADD.

9.2 Description of activities and flow charts

9.2.1 General requirements

A TQM (Total Quality Management) methodology shall be employed in which the test centre is responsible for its own quality, has set the organization and resources to manage it (including TRB) and is able to report its effectiveness to the SI (either directly or via the Control Site).

9.2.2 Description of activities

The activities of the testing of MMIC shall be declared, including interfaces to other tasks and flow charts containing information on quality indicators and the procedures for qualification, acceptance, monitoring and release. Examples of activities include:

– environmental and cleanliness control;
– test programme methodology;
– test specifications, including contact of the test specification file;
– test programme creation and verification procedures, demonstrating how the product technical specification is met;
– test tools gauging procedure;
– maintenance and control of test programmes;
– evaluation procedures for standard or prototype circuits;
– mass production test and delivery procedures;
– acceptance and release procedures;
– recording and traceability procedures, including the test data for individual test lots;
– storage and handling procedures;
– coplanarity and lead integrity;
– marking of product.

For an example of a typical flow chart, see Figure 7.

9.3 Equipment

Information on the test equipment used and the intended range shall be declared. Verification, maintenance and calibration programmes shall be included. All equipment used for testing of prototype or finished products shall comply with the requirements given in 5.3.

9.3.1 Test equipment

A specification shall exist for each piece of equipment, containing:

– general characteristics (number of pads and impedance of each one, number of power supplies, general and optional resources, test type, etc.);

– functional characteristics (network analyser, spectrum analyser, frequency counter, power meter);

– static characteristics (current and voltage, type of loads – both active and passive – accuracy);

– dynamic measurements characteristics (frequency, accuracy, number and type of sources, power level);

– conditions and types of measurements (dynamic, static);

– environmental test equipment.

The calibration and set-up of the test equipment shall be defined, including:

– performance verification and calibration of the tester (SOLT, TRL, LRM, self diagnostic, maintenance, self gauging);

– validation of the interface and specific tools (use of the reference sample);

– validation of the data delivered to the tester (tester resources and external measurements);

– test on a prototype.

9.3.2 Test boards, test fixtures, probes

All test boards related to the component to be tested shall be identified, containing, for example:

– electrical schematics of boards (fixtures, probes) to be made;

– boards (fixtures, probes) layout/wiring;

– wiring rules;

– parts list;

– purchasing specification of components;

– mechanical tools drawings;

– limits of tools (frequency, power level) ;

– registration and control of type specific jigs, tools and boards (fixtures, probes).

The conformance of any subcontracted tools shall be verified.

9.4 Test procedures

The requirements for detailing procedures for the handling, control and use of test programmes shall be declared, including any relevant information not previously provided (i.e. validation and compliance procedures).

9.4.1 Test methods

The nature of tests to be performed shall be defined (continuity test, functional test), together with the test equipment operating mode to be used, e.g.:

– involved parameters;

– requested resources;

– choice of functional states for the component;

– reference board.

9.4.2 Final specification and review

A test specification shall be produced as a record by the test engineering function, and it shall be approved by the customer during a review, where appropriate (e.g. for ASICs). It shall include:

- the test objective;
- the list of reference documents (technical specification of the component);
- the specific test programme flow chart
  - header (programme identification, date, test tools, test interface, test specification, release number),
  - specification (supply voltage and currents, power levels, frequency, recommended bias circuit);
- specific interface and tools.

The involvement of the customer may be requested during the adaptation of the test, if necessary.

The approval review shall demonstrate the conformance of the operations carried out compared to the initial specifications. If a nonconformance is observed compared to the product technical specification, complementary tests and measurements shall be carried out to find the reasons for such discrepancies. Follow-up action shall be taken and recorded.

9.5 Interfaces

9.5.1 Contracting

Testing may be subcontracted in accordance with 2.4. When test tool development and manufacture is subcontracted, the subcontractor controls shall be defined.

9.5.2 Verification of customer specification

The customer may be the circuit designer, a user of an existing circuit, or an IC manufacturer. The procedures used for control and validation shall be declared. The customer interrelationship during testing shall be defined for

– design,
– fabrication,
– probe test,
– prototype (including agreement on conformance to technical need specifications),
– characterization,
– reviews.

The deliverables to customers shall be identified and may include:

– measurement system;
– a test programme (probing or final test);
– tested parts;
– control and interfaces identification.

In order to accept customer specification for test, the following information shall be available:

– technology of the component to be tested (MESFET, HEMT, MODFET, HBT);
– functional description;
– physical characteristics;

– pin layout;
– maximum ratings;
– recommended operating conditions;
– electrical characteristics and measurements conditions.

9.6 Validation and control of the processes

Critical test processes shall be controlled to an acceptable level and the following areas should be included:

- Specification of methods and tests resources;
- Recording and update of existing test programmes;
- Correct implementation of test resources through methodologies such as
  – parameters test (measurements condition, type of approval),
  – evaluation of guarantied but not tested parameters;
- Internal validation methodology of tools and test programmes, e.g.
  – writing test programmes (programme structure, test sequence),
  – follow-up of new release of existing test programmes,
  – validation of interface test tools and test equipment (gauging),
  – periodic control of release number of programs used for production,
  – choice and control of test equipment,
  – definition, fabrication and control of boards, connectors, interface, etc. required for test.

The effective management of the process and its quality shall be validated against the following requirements:

- The test term shall
  – confirm that they understand the content of the circuit technical specification,
  – verify that circuit technical specification is complete.
- The management of the test facility shall ensure the competency of the personnel performing the tests, taking into consideration:
  – knowledge of technological constraints;
  – skill in test practice (handling equipment and software).
- The performance of tools shall be validated, including:
  – validity of standard test modules;
  – software tools in place (post processor, etc.);
  – resources in place (tester language, tester performance).
- Equipment and software shall be validated, including:
  – schematics of boards, connectors, interface and other devices used for test;
  – equipment and software tools and releases approved by the centre;
  – control and periodical gauging of the test tools;
  – maintenance of measurement standards;
  – monitoring of the test tools' performance drift by preventive maintenance;
  – test programmes approved by the centre and used for production.

- Precautions required for testing shall be identified, including:
  - handling of products to be tested;
  - environmental protection (ESD etc.);
  - handling and processing of nonconforming components.
- Test documentation and data shall be validated prior to the release of the lot, including:
  - test results documentation delivered with tested parts;
  - traceability records.

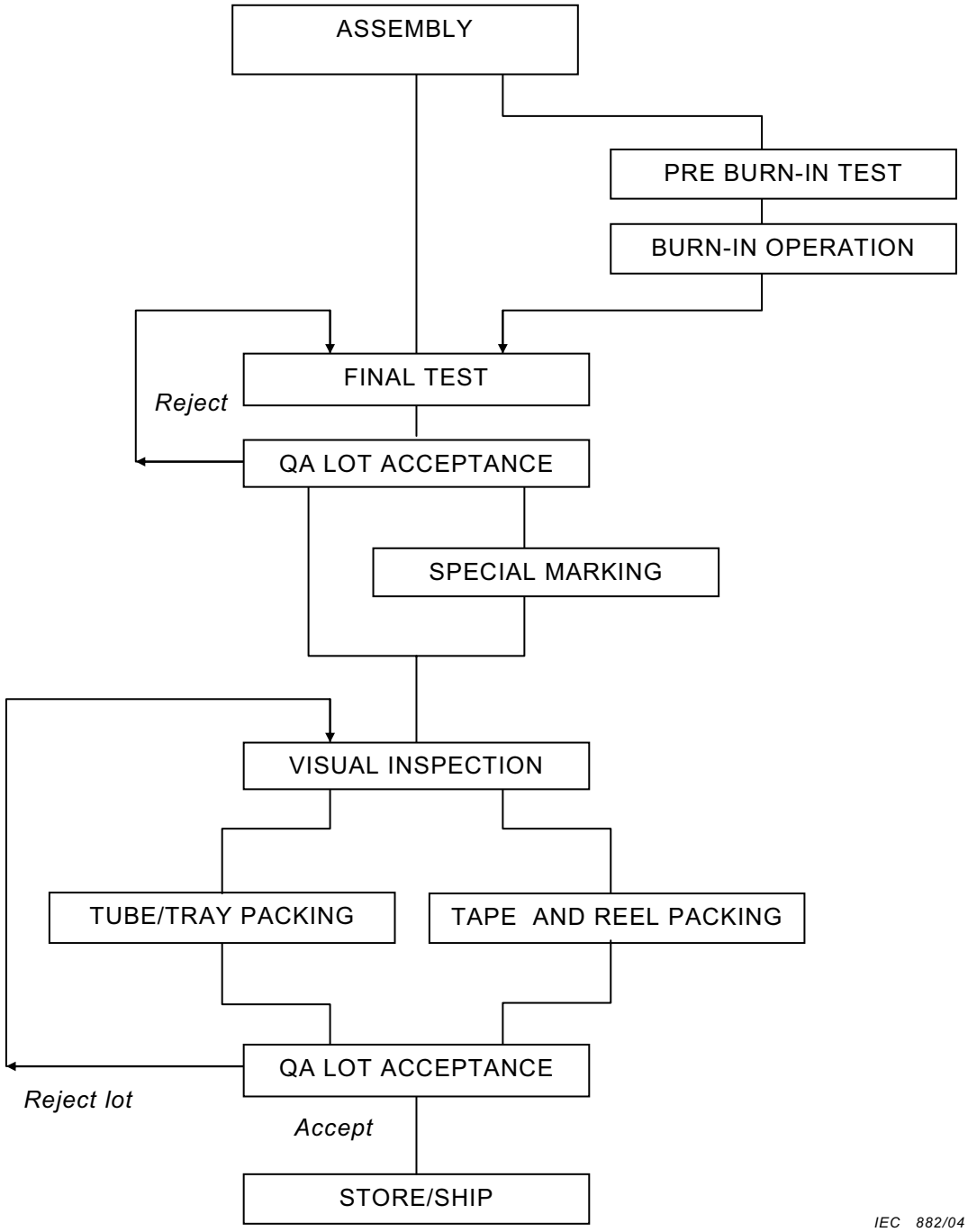


Figure 7 – Example flow chart for a testing

9.7 Process boundary verification

Test vehicles are used to verify, analyse or monitor process or electrical/physical attributes. These may be either specifically designed or standard products. A number or different test vehicles may be required to cover the complete approval.

Where not already detailed elsewhere in the TADD, the following information demonstrating the verification of the technology shall be provided:

– rationale for the selection of the evaluation methods;
– test procedures or measurement;
– description of tools and techniques used for verification of the process;
– test vehicle descriptions and their relationship to end products.

The test vehicle description shall include details of the test vehicles, associated tests, software and other tools, which are used on a regular basis to demonstrate design and manufacturing process(es) and product performance as applicable:

– Technology Characterization Vehicle (TCV);
– Process Control Monitor (PCM);
– Standard Evaluation Circuits (SEC) (optional);
– standard product.

9.7.1 Technology characterization vehicle (TCV) programme

9.7.1.1 TCV programme

The TCV programme shall contain, as a minimum, those test structures needed to characterize a technology's susceptibility to intrinsic reliability failure mechanisms such as electromigration, Time Dependent Dielectric Breakdown (TDDB) and ageing. If other wear-out mechanisms are discovered as integrated circuit technology continues to mature, test structures for the new wear-out mechanisms shall be added to the TCV programme. The TCV programme shall be used for the following purposes: certification of the technology, reliability monitoring and change control.

NOTE The test structures necessary to monitor intrinsic reliability failure mechanisms do not have to be a single die or location, but can appear on the PCM or the SEC or the device itself. The TCV programme shall, however, indicate where the structures are located and how they are tested and analysed.

9.7.1.2 TCV certification

For initial certification, sufficient TCV test structures for each wear-out mechanism from wafers passing the wafer screening requirements (randomly chosen and evenly distributed from three homogeneous wafer lots in the technology to be certified on the fabrication facility to be certified), shall be subjected to accelerated ageing experiments. The accelerated ageing experiments shall produce an estimate of the MTF (Mean-Time-to-Failure) and a distribution of the failure times under worst case operating conditions and circuit layout consistent with the design rules for each wear-out mechanism. From the MTF and distribution of failures a worst-case operating lifetime or a worst-case failure rate can be predicted. Test structures shall be chosen from completed wafers, which have been glassivated. A summary of the accelerated ageing date and analysis shall be available for review by the SI. The initial Certification MTF, failure distribution and acceleration factors shall be used as bench-marks for the technology to which subsequent TCV results shall be compared. Special considerations for ageing, electromigration and time-dependent dielectric breakdown are discussed below.

9.7.1.3 Ageing

The TCV shall use structures that monitor stress ageing applicable to the technology to be used for qualified circuits. Device degradation is to be characterized in terms of both g_m (forward transconductance) and $V_{GS(TO)}$ (gate-source threshold voltage) and the resistance to ageing is to be based on whichever parameter experiences the manufacturer's specified degradation limit first for the minimum channel length allowed in the technology.

a) Step stress tests

If there are no data available on similar devices that can be used to determine the stress temperatures to be used, a step stress shall be used. The step stress should use at least six TCVs, have the same bias and RF input power to be used in the test, start at 150 °C baseplate temperature, proceed in steps of 25 °C for a duration of at least 24 h at each temperature, and with the electrical measurements to be used in the test made between every step. Similar step stress tests using constant temperature and increasing bias or RF input power may also be used to verify reasonable bias conditions.

b) Steady state stress tests

The highest steady-state stress temperature used shall be based on an expected median life of at least 100 h. If the step stress test is used, the highest steady-state stress baseplate temperature shall be at least 20 °C below the step stress test baseplate temperature which produces 50 % failure in 24 h. In addition, if it is known that the dominant failure mechanism changes as the device temperature is raised above the temperature of application, the tests shall be performed at temperatures below that transition temperature.

There shall be at least three temperatures of steady-state stress. The second shall be at least 15 °C below the highest, and the third shall at least 15 °C below the second. In addition, if the lowest of the three baseplate temperatures is greater than 200 °C, a fourth sample of TCVs shall be run at a baseplate temperature 50 °C above the device's maximum operating temperature (or, if it is not specified, at a baseplate temperature of 150 °C) for a minimum 2 000 h to verify the validity of the extrapolation to the operation range. At this temperature, few failures are expected, and the analysis method of MTF can only state with strong certainty that the median life is greater than 2 000 h. (A 2 000 h life at a channel temperature of 200 °C corresponds to 1 year at a device's maximum operating temperature of 150 °C if the failure activation energy is 0,5 eV, or 32 years if the failure activation energy is 2 eV).

Stress other than temperature can also be performed for the purpose of determining acceleration factors. While they cannot be expressed as activation energies, the dependence of device life on voltage, current and other variables relevant to the device can be determined, e.g. the devices can be stressed above normal operating conditions to accelerate the test. Analysis of the data is similar to temperature dependence except that the functional dependence on each variable may be different. When using electrical overstress, the device temperature may change enough to impact device lifetime, and the ambient temperature of each electrical overstress group may have to be different to keep the FET channel temperature equal.

c) Electrical stress

During the step or steady-state stress tests, the TCVs shall be operated under recommended DC operational electrical stress. Unless special circumstances prevail, low-noise and passive devices may be stressed with DC only. General purpose and power devices and circuits not containing FETs shall be stressed with continuous wave RF. It is desirable that the RF stress level drives the device into at least 1 dB compression at the stress temperature; the values of the RF input power, degree of compression and frequency shall be stated in the test report. If the test is being run by, or for, a specific user, the operational DC and RF stress for the application shall be used.

During the tests, the TCVs shall be monitored periodically to detect the occurrence of catastrophic failure and to adjust the equipment so that applied stress (temperature, current, voltage, etc.) are unchanged within tight tolerance.

To facilitate failure analysis, the device stress circuitry should be designed to quickly remove voltage from the device once it has failed; this practice will minimize subsequent damage due to a runaway condition such as shorted FET.

9.7.1.4 Electromigration

The TCV shall contain structures for the worst case characterization of metal electromigration over

– flat surfaces,

– worst case non-contact topography,

– through contacts between conductive layers,

– contacts to the substratum.

The current density and temperature acceleration factors for electromigration shall be determined and an MTF and failure distribution determined for the worst case current, temperature layout geometry allowed in the technology. From the MTF and distribution, a failure rate for electromigration in the technology shall be calculated.

9.7.1.5 Time dependent dielectric breakdown (TDDB)

The TCV shall contain structures for characterizing TDDB of MIM-capacitor (Metal-Insulator-Metal). The structures shall have capacitor area and perimeter dominated structures. The electric field and temperature acceleration factors for TDDB shall be determined and MTF and failure distribution determined for the worst case voltage. From the MTF and distribution, a failure rate for TDDB in the technology shall be calculated.

9.7.2 Process control monitor (PCM)

The manufacturer shall have process control monitors to be used for electrical characteristics of each wafer type in a specified technology. The PCM test structures can be incorporated into the grid (kerf), within a device chip, as a dedicated drop-in die or any combination thereof. Location of the PCM structures shall be optimally positioned on the optimum place to allow for the determination of the uniformity across the wafer. A suggested location scheme is one near the wafer centre and one in each of the four quadrants of the wafer, at least two-thirds of a radius away from the wafer centre. The number of PCM structures on a wafer shall be adequate to determine the quality of the wafer.

The manufacturer's TRB shall establish and document reject limits and procedures for parametric measurements including which parameters will be monitored routinely and which will be included in the SPC programme. Documentation of the PCM shall also include PCM test structure design, test algorithm, including measurement temperature and the relationship between these limits and those used in the manufacturer's circuit simulations, design rules and process rules. Alternate measurement techniques, such as in-line monitors are acceptable if properly documented. The following parameters are to be used as a guide-line by the manufacturer's TRB in formulating the PCM.

9.7.2.1 General electrical parameters

a) Sheet resistance: structures shall be included to measure the sheet resistance of all conducting layers (metallization, diffusion, etc.).

b) Junction breakdown: structures shall be included to measure junction breakdown for all diffusions.

c) Contact resistance: structures shall be included to measure contact resistance of all interlevel contacts.

d) All parasitic components.

9.7.2.2 Process parameters

a) MIM capacitor: structures shall be included to measure the capacitance per MIM capacitor area.

b) Device parameters: a minimum set of test devices shall be included for the measurement of device parameters. If there is more than one nominal threshold voltage for the process, the minimum set shall be included for each threshold. The minimum set shall include a large geometry device of sufficient size that short channel and narrow width effects are negligible and devices that can separately demonstrate the maximum short channel effects and width effects allowed by the geometric design rules.

   For MESFET or HEMT, an example of minimum set consists of

   - gate-source threshold voltage ($V_{GS(TO)}$),
   - gate-source cut-off voltage (V_{GSoff}),
   - forward transconductance (g_m),
   - drain current at zero gate-source voltage (I_{DSS}),
   - gate-source breakdown voltage with drain short-circuited to source ($V_{(BR)GSS}$).

NOTE Care should be taken in the manner and sequence in which all breakdown voltage and current measurements are taken so as to not permanently alter the device for other measurements.

9.7.3 **Standard Evaluation Circuit (SEC**) (optional)

A Standard Evaluation Circuit (SEC) is a test specimen specially designed or a commercial product taken from production and used for verifying capability (totally or partly) and reliability in accordance with the Process Manual.

A manufacturer's SEC shall be used to demonstrate fabrication process reliability for the technology.

SECs are used in the qualification test programme to define capability.

For maintenance, the tests shall demonstrate the quality aspects and either all the limits of the capability or those limits of the capability used for the products delivered during the last period.

Two types of component may be used as a SEC:

Type I:

A component specially designed and manufactured to assess the design rules and the manufacturing process.

Type II:

A commercial product taken from production.

Generally it is not possible to cover all limits and all quality aspects of the capability with a single SEC. Either a single type or a combination of both types may be used and collectively they shall be adequate to assess the complete worst case design rules, the materials, manufacturing processes and the quality aspects. Where it is claimed that a diffused/ metallized element, or group of elements can demonstrate one or more limits, such element or group of elements shall be measurable separately without influence from other circuit elements.

The SEC shall be documented including the design methodology and the software tools used in the design, the functions it is to perform, its size in terms of utilized active device and simulations of its performance.

Every SEC shall have a detail specification which shall be written in accordance with the following requirements:

a) Complexity: The complexity of the SEC component shall contain, as a minimum, one half the number of active devices expected to be used in the largest circuit to be built on the qualified manufacturing line.

b) Functionality: The SEC shall contain fully functional circuits capable of being tested and screened in an identical manner to the qualified circuits.

c) Design: The SEC shall be used to stress minimum geometric and electrical design rules. The test conditions for the active devices and interconnects on the SEC shall be worst case conditions. The architecture of the SEC shall be designed so that failures can be easily diagnosed.

d) Fabrication: The SEC shall be processed on a wafer fabrication line, which is intended to be, or already is, a certified manufacturing line.

e) Packaging: The SEC shall be packaged in qualified packages according to the application fields.

9.8 Product verification

9.8.1 Test methods

Where applicable, verification tests on final product shall be in accordance with declared quality and reliability requirements. Test methods should be in accordance with, or correlate with IEC recognized standards (for example, IEC 60068).

9.8.2 New product introduction

The procedures which define the introduction and verification for each product shall be declared. This verification should include a formal acceptance of the products released from the qualified company to the customer, and may be obtained through one, or a combination, of the following:

– end of line testing;

– structural similarity with existing qualified products;

– wafer level testing, including wafer level reliability tests;

– product characterization and Cpk determination;

– yield analysis;

– in-line SPC.

10 Process characterization

10.1 Identification of process characteristics

Unless covered elsewhere in the TADD, applications for extension/amendment to technology approval shall include information relevant to newly introduced and/or changed process.

Process characterization is the extraction from the process of all the information required to define the process parameters for the CAD models and process design rules. It may be performed within the process design task or within the MMIC design facility or task or wholly or partly by a separate qualified facility.

Process characterization shall be performed on processes already developed when there is an introduction of a new process or a change to a current process and may be performed on the introduction of a new product or a change in product specification.

The objectives are to

– guarantee the quality of what is going out of the wafer fabrication or assembly facility,
– provide tools for the design of new MMICs.

In all cases, methods which demonstrate a relationship between process parameters, process outputs and characteristics shall be declared.

These methods shall include:

– A method for ensuring that the precision and accuracy of the measuring systems are sufficient to perform characterization and to reliably identify any out-to-control measurements.
– Identification of standards of measurements for capability and continuous improvement assessments.
– Application of statistical methods for determining parameter relationships, performing diagnostics, assessing potential capability using experimentation and stimulating continuous improvement.

10.2 Description of activities

The procedures for process characterization relating to the above shall be declared. Relevant flow charts and test vehicle information may be used to present or supplement this declaration.

The information shall detail parameters to be measured and clearly define the following:

- stages at which the measurements should be made;
- relationship with end product parameters;
- test vehicles and measurement methods to be used;
- rationale for
  - identification of critical process,
  - measurement parameter selection,
  - measurement system selection.

The parameters shall be specified within the allowable temperature range.

The activities for the following electrical physical and mechanical characterization shall be declared, together with any associated PCM and TCV descriptions.

10.2.1 Electrical

– PCM electrical parameter drift (parameters distribution statistical analysis temperature and voltage characterization).
– Determine acceptance limits for the wafer fabrication QC tests.
– Determine process engineering (or control) limits (for process stability determination).

10.2.2 Process spread

– Measurements shall be made of typical values and comprehensive studies shall be made on the characteristics of main circuits elements utilizing wafer batches with deliberately fabricated worst-case parameters.
– Simulations shall be made for input/output values of parameters and compared to these measurements.

10.2.3 Topology

- The following shall be determined, taking into account the equipment tolerances provided by the wafer fabrication:
  - rules on the same plane (spacing);
  - alignment rules and superposing rules (step coverage);
  - rules related to electrical problems (electrical guards) including worst case;
  - verification of these rules shall be performed using appropriate test vehicles.
- The general rules for DRC and ERC shall be defined.
- Verification of conformance shall be made following a new release of an application software and an introduction of a new algorithm for topology rules description. Traceability shall be maintained.
- Routing of blind (or complementary) layers may be calculated from known rules and documented (if applicable).
- Location and proximity rules related to temperature gradient shall be established. Protection rules and protection cell libraries shall be characterised in order to
  - establish the ESD limits for the technology,
  - determine the derating requirements and thermal behaviour in accordance with the established thermal coefficients.

10.2.4 Package

All certified packages shall be listed by package technology type. A manufacturer can qualify a group of packages within a family where a structural similarity plan exists and is validated by the TRB. For the qualification of assembly, process tests shall be performed on packages according to the whole process cycle.

These tests shall be defined in order to verify resistance to

– thermal constraint,
– mechanical constraint,
– solvents,
– humidity,
– any combination of the above.

10.3 Characterization procedures

The documents produced by the characterization task shall be sent to the internal or external design centre and shall cover all the design rules, viz.:

10.3.1 Topology rules

(i.e. geometric/layout rules).

10.3.2 Electrical rules

Detailed electrical rules

– exhaustive documentation giving technology limits,
– documentation describing simulation models (large- or small-signal models) and related parameters,
– attention is paid to technology spreads in parameters files (at 3 σ),
– a modelling of passive or active component library.

10.3.3 Package related thermal rules

These values may be obtained directly or indirectly by simulation or calculation. In this latter case, the method shall have been qualified by the SI, the manufacturer demonstrating a good correlation (approved by TRB) between actual measured values and calculated ones for at least one package of the same type. Any change made to the estimation method shall be qualified according to the same procedure.

10.3.4 Rules related to quality

Rules related to quality shall be documented (these may be included in the electrical rules) .

EXAMPLE: ESD (design rules for protection cells).

All of this information is an input to

– geometry verification (DRC),
– electrical rules verification (ERC),
– layout versus schematics verification (LVS).

Records relating to characteristics for delivered lots shall be maintained including:

– general characteristics of the process;
– intrinsic electrical rules (including maximum values and reliability rules (voltage and current limits etc.) related to the technology);
– simulations (including components library);
– worst case;
– DRC/ERC/LVS;
– protection cells.

11 Packaging and shipping

The procedures for packaging and shipment to ensure that the correct quantity of the correct product is delivered on time to the correct customer shall be declared.

11.1 Description of activities and flow charts

The activities for packaging and shipping shall be identified, supported by any relevant flow chart. Examples of activities include:

– environment and cleanliness of the area;
– ensuring compliance with customer order;
– protection against environmental change;
– protection against mechanical damage;
– protection against electrical damage;
– documentation/labelling.

For examples of a typical flow chart, see Figure 8.

11.2 Interfaces

11.2.1 Verification of customer requirements

The procedures for controlling the packing and shipping of product to meet customer requirements shall be declared.

11.2.2 Subcontracting

Packing and shipping may be subcontracted in accordance with 2.4.

11.3 Validity of release

The validity of release period shall be declared. Evidence shall be made available to assure that product released within this period conforms to the declared IECQ-CECC/customer/ application quality and reliability requirements.

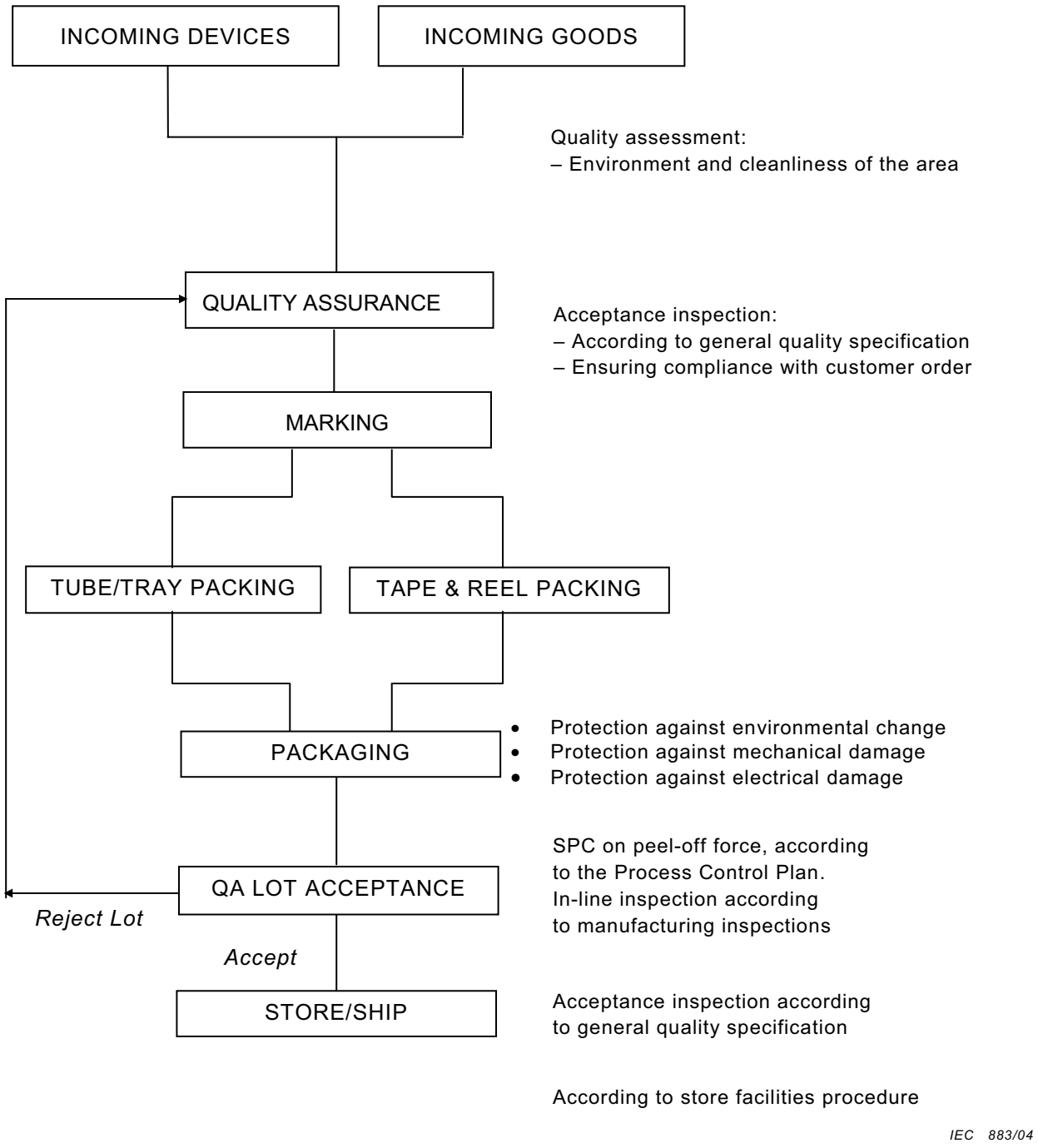


Figure 8 – Typical flow chart for packaging and shipping

12 Withdrawal of Technology Approval

Technology Approval shall be suspended if either:

– any part of the design or manufacturing process fails to meet the requirements of QC 001002-3, Clause 2, or QC 001002-3, Clause 6; or

– at the request of the Control Site; or

– where production through a main technical process or a declared critical process has disrupted such that re-qualification of the process would be required to re-start production.

Technology Approval shall be withdrawn if acceptable corrective action cannot be agreed, or at the request of the control site.

_____

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Q1 Please report on **ONE STANDARD** and **ONE STANDARD ONLY**. Enter the exact number of the standard: *(e.g. 60601-1-1)*

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Q2 Please tell us in what capacity(ies) you bought the standard *(tick all that apply).* I am the/a:

purchasing agent ❑
librarian ❑
researcher ❑
design engineer ❑
safety engineer ❑
testing engineer ❑
marketing specialist ❑
other.....

Q3 I work for/in/as a: *(tick all that apply)*

manufacturing ❑
consultant ❑
government ❑
test/certification facility ❑
public utility ❑
education ❑
military ❑
other.....

Q4 This standard will be used for: *(tick all that apply)*

general reference ❑
product research ❑
product design/development ❑
specifications ❑
tenders ❑
quality assessment ❑
certification ❑
technical documentation ❑
thesis ❑
manufacturing ❑
other.....

Q5 This standard meets my needs: *(tick one)*

not at all ❑
nearly ❑
fairly well ❑
exactly ❑

Q6 If you ticked NOT AT ALL in Question 5 the reason is: *(tick all that apply)*

standard is out of date ❑
standard is incomplete ❑
standard is too academic ❑
standard is too superficial ❑
title is misleading ❑
I made the wrong choice ❑
other .....

Q7 Please assess the standard in the following categories, using the numbers:
(1) unacceptable,
(2) below average,
(3) average,
(4) above average,
(5) exceptional,
(6) not applicable

timeliness.....
quality of writing.....
technical contents.....
logic of arrangement of contents .....
tables, charts, graphs, figures.....
other .....

Q8 I read/use the: *(tick one)*

French text only ❑
English text only ❑
both English and French texts ❑

Q9 Please share any comment on any aspect of the IEC that you would like us to know:

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