INTERNATIONAL STANDARD

IEC 60679-1

Third edition
2007-04

Quartz crystal controlled oscillators of assessed quality –

Part 1: Generic specification

Reference number
IEC 60679-1:2007(E)

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland
Email: inmail@iec.ch
Web: www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

- Catalogue of IEC publications: www.iec.ch/searchpub

The IEC on-line Catalogue enables you to search by a variety of criteria (reference number, text, technical committee,…). It also gives information on projects, withdrawn and replaced publications.

- IEC Just Published: www.iec.ch/online_news/justpub

Stay up to date on all new IEC publications. Just Published details twice a month all new publications released. Available on-line and also by email.

- Customer Service Centre: www.iec.ch/webstore/custserv

If you wish to give us your feedback on this publication or need further assistance, please visit the Customer Service Centre FAQ or contact us:

Email: csc@iec.ch
Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00

INTERNATIONAL STANDARD

IEC 60679-1

Third edition
2007-04

Quartz crystal controlled oscillators of assessed quality –

Part 1: Generic specification

Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE XC

For price, see current catalogue

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

QUARTZ CRYSTAL CONTROLLED OSCILLATORS OF ASSESSED QUALITY –

Part 1: Generic specification

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60679-1 has been prepared by IEC technical committee 49: Piezoelectric and dielectric devices for frequency control and selection.

This third edition cancels and replaces the second edition published in 1997 and its Amendments 1 (2002) and 2 (2003) and constitutes a technical revision. It represents a step in a revision of all parts of the IEC 60679 series to include the test requirements of the IECQ system. This edition is based on the relevant standards of that system.

The text of this standard is based on the following documents:

FDIS	Report on voting
49/769/FDIS	49/776/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

A list of all parts of the IEC 60679 series, published under the general title *Quartz crystal controlled oscillators of assessed quality,* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

QUARTZ CRYSTAL CONTROLLED OSCILLATORS OF ASSESSED QUALITY –

Part 1: Generic specification

1 Scope

This part of IEC 60679 specifies the methods of test and general requirements for quartz crystal controlled oscillators of assessed quality using either capability approval or qualification approval procedures.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60027 (all parts), *Letter symbols to be used in electrical technology*

IEC 60050-561, *International Electrotechnical Vocabulary (IEV) – Part 561: Piezoelectric devices for frequency control and selection*

IEC 60068-1:1988, *Environmental testing – Part 1: General and guidance*
Amendment 1 (1992)

IEC 60068-2-1, *Environmental testing – Part 2: Tests – Tests A: Cold*

IEC 60068-2-2, *Environmental testing – Part 2: Tests – Tests B: Dry heat*

IEC 60068-2-6, *Environmental testing – Part 2: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-7, *Environmental testing – Part 2: Tests – Test Ga and guidance: Acceleration, steady state*

IEC 60068-2-10, *Environmental testing – Part 2-10: Tests – Test J and guidance: Mould growth*

IEC 60068-2-13, *Environmental testing – Part 2: Tests – Test M: Low air pressure*

IEC 60068-2-14, *Environmental testing – Part 2: Tests – Test N: Change of temperature*

IEC 60068-2-17, *Environmental testing – Part 2: Tests – Test Q: Sealing*

IEC 60068-2-20, *Environmental testing – Part 2: Tests – Test T: Soldering*

IEC 60068-2-21, *Environmental testing – Part 2-21: Tests – Test U: Robustness of terminations and integral mounting devices*

IEC 60068-2-27, *Environmental testing – Part 2: Tests – Test Ea and guidance: Shock*

IEC 60068-2-29, *Environmental testing – Part 2: Tests – Test Eb and guidance: Bump*

IEC 60068-2-30, *Environmental testing – Part 2-30: Tests – Test Db: Damp heat, cyclic (12h + 12 h cycle)*

IEC 60068-2-32, *Environmental testing – Part 2: Tests – Test Ed: Free fall*

IEC 60068-2-45, *Environmental testing – Part 2: Tests – Test XA and guidance: Immersion in cleaning solvents*

IEC 60068-2-52, *Environmental testing – Part 2: Tests – Test Kb: Salt mist, cyclic (sodium chloride solution)*

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60068-2-64, *Environmental testing – Part 2: Test methods – Test Fh: Vibration, broad-band random (digital control) and guidance*

IEC 60068-2-78:2001, *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*

IEC 60469-1:1987, *Pulse techniques and apparatus – Part 1: Pulse terms and definitions*

IEC 60617-DB: 2001[1], *Graphical symbols for diagrams*

IEC 60679-5, *Quartz crystal controlled oscillators of assessed quality – Part 5: Sectional specification – Qualification approval*

IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test*

IECQ 01, *IEC Quality Assessment System for Electronic Components (IECQ) – Basic Rules*

IEC QC 001002-2:1998, *IEC Quality Assessment System for Electronic Components (IECQ) – Rules of Procedure – Part 2: Documentation*

IEC QC 001002-3:1998, *IEC Quality Assessment System for Electronic Components (IECQ) – Rules of Procedure – Part 3: Approval procedures*

ISO 1000, *SI units and recommendations for the use of their multiples and of certain other units*

ITU-T G.810, *Definitions and terminology for synchronization networks*

ITU-T G.811: *Timing characteristics of primary reference clocks*

ITU-T G.812, *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*

ITU-T G.813, *Timing characteristics of SDH equipment slave clocks (SEC)*

ITU-T G.825, *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)*

---

[1] "DB" refers to the IEC on-line database.

ANSI T1.101, *Synchronization Interface Standard*

ANSI T1.105.03, *Synchronous Optical Network (SONET) – Jitter and Wander at Network Equipment Interfaces*

ETSI EN 300 462 (all parts), *Transmission and Multiplexing (TM); Generic requirements for synchronization networks*

Telcordia GR-253, *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria*

- **Order of precedence**

Where any discrepancies occur for any reason, documents shall rank in the following order of precedence:

– detail specification;
– sectional specification;
– generic specification;
– any other international documents (for example of the IEC) to which reference is made.

The same order of precedence shall apply to equivalent national documents.

3 Terms, definitions and general information

3.1 General

Units, graphical symbols, letter symbols and terminology shall, wherever possible, be taken from the following standards:

IEC 60027
IEC 60050-561
IEC 60469-1
IEC 60617
ISO 1000

3.2 Definitions

For the purposes of this document, the following definitions apply.

3.2.1
simple packaged crystal oscillator
SPXO
crystal controlled oscillator having no means of temperature control or compensation, exhibiting a frequency/temperature characteristic determined substantially by the piezoelectric resonator employed

[IEV 561-04-01]

3.2.2
overtone crystal controlled oscillator
oscillator designed to operate with the controlling piezoelectric resonator functioning in a specified mechanical overtone order of vibration

[IEV 561-04-02]

3.2.3
crystal cut
orientation of the crystal element with respect to the crystallographic axes of the crystal

NOTE This definition is included as it may be desirable to specify the cut (and hence the general form of the frequency/temperature performance) of a crystal unit used in an oscillator application. The choice of the crystal cut will imply certain attributes of the oscillator which may not otherwise appear in the detail specification.

3.2.4
voltage controlled crystal oscillator
VCXO
crystal controlled oscillator, the frequency of which can be deviated or modulated according to a specified relation, by application of a control voltage

[IEV 561-04-03]

3.2.5
temperature compensated crystal oscillator
TCXO
crystal controlled oscillator whose frequency deviation due to temperature is reduced by means of a compensation system, incorporated in the device

[IEV 561-04-04]

3.2.6
oven controlled crystal oscillator
OCXO
crystal controlled oscillator in which at least the piezoelectric resonator is temperature controlled

[IEV 561-04-05]

NOTE This mode of operation ensures that the oscillator frequency will remain sensibly constant over the operating temperature range of the OCXO, therefore independent of the frequency/temperature characteristic of the crystal unit.

3.2.7
nominal frequency
frequency used to identify the crystal controlled oscillator

[IEV 561-04-06]

3.2.8
frequency tolerance
maximum permissible deviation of the oscillator frequency from a specified nominal value when operating under specified conditions

[IEV 561-04-07]

NOTE Frequency tolerances are often assigned separately to specified ambient effects, namely electrical, mechanical and environmental. When this approach is used, it is necessary to define the values of other operating parameters as well as the range of the specified variable, that is to say:

– deviation from the frequency at the specified reference temperature due to operation over the specified temperature range, other conditions remaining constant;

– deviation from the frequency at the specified supply voltage due to supply voltage changes over the specified range, other conditions remaining constant;

– deviation from the initial frequency due to ageing, other conditions remaining constant;

– deviation from the frequency with specified load conditions due to changes in load impedance over the specified range, other conditions remaining constant.

In some cases, an overall frequency tolerance may be specified, due to any/all combinations of operating parameters, during a specified lifetime.

3.2.9
frequency offset
frequency difference, positive or negative, which should be added to the specified nominal frequency of the oscillator, when adjusting the oscillator frequency under a particular set of operating conditions in order to minimize its deviation from nominal frequency over the specified range of operating conditions

[IEV 561-04-08]

EXAMPLE In order to minimize the frequency deviation from nominal over the entire temperature range, a frequency offset may be specified for adjustment at the reference temperature (see Figure 1).

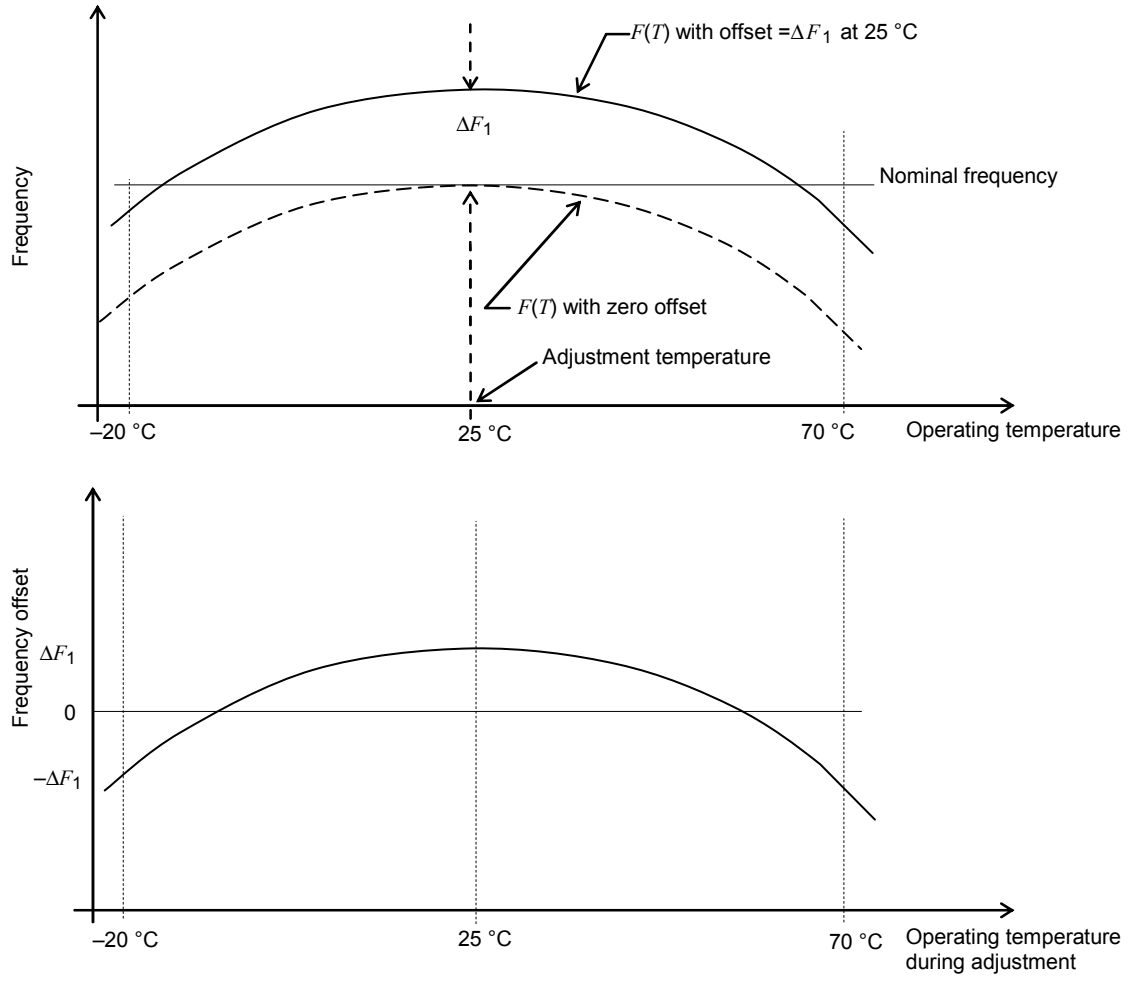


Figure 1 – Example of the use of frequency offset

3.2.10
adjustment frequency
frequency to which an oscillator must be adjusted, under a particular combination of operating conditions, in order to meet the frequency tolerance specification over the specified range of operating conditions, i.e. adjustment frequency = nominal frequency + frequency offset

[IEV 561-04-09]

3.2.11
frequency adjustment range
range over which the oscillator frequency may be varied by means of some variable element, for the purpose of:

a) setting the frequency to a particular value, or

b) to correct the oscillator frequency to a prescribed value after deviation due to ageing, or other changed conditions.

[IEV 561-04-10]

3.2.12
storage temperature range
minimum and maximum temperatures as measured on the enclosure at which the crystal controlled oscillator may be stored without deterioration or damage to its performance

3.2.13
operating temperature range
range of temperature over which the oscillator will function, maintaining frequency and other output signal characteristics within specified tolerances

[IEV 561-04-11]

3.2.14
operable temperature range
range of temperature over which the oscillator will continue to provide an output signal, though not necessarily within the specified tolerances of frequency, level, waveform, etc.

[IEV 561-04-12]

3.2.15
reference temperature
temperature at which certain oscillator performance parameters are measured, normally 25 °C ± 2 °C

3.2.16
reference point temperature
temperature measured at a specific reference point relative to the oscillator

3.2.17
thermal transient frequency stability
oscillator frequency time response when ambient temperature is changed from one specific temperature to another with a specific rate

3.2.18
stabilization time
time, measured from the initial application of power, required for a crystal controlled oscillator to stabilize its operation within specified limits

[IEV 561-04-13]

3.2.19
frequency/voltage coefficient
fractional change in output frequency resulting from an incremental change in supply voltage, other parameters remaining unchanged

[IEV 561-04-14]

NOTE In the case of OCXOs, a considerable time may elapse before the full effect of a supply voltage change is observed, as the temperature of the oven may drift gradually to a new value following the voltage perturbation.

3.2.20
frequency/load coefficient
fractional change in output frequency resulting from an incremental change in electrical load impedance, other parameters remaining unchanged

[IEV 561-04-15]

3.2.21
long-term frequency stability (frequency ageing)
relationship between oscillator frequency and time. This long-term frequency drift is caused by secular changes in the crystal unit and/or other elements of the oscillator circuit, and should be expressed as fractional change in mean frequency per specified time interval.

3.2.22
short-term frequency stability
random fluctuations of the frequency of an oscillator over short periods of time

[IEV 561-04-16]

3.2.23
Allan variance of fractional frequency fluctuation
unbiased estimate of the preferred definition in the time domain of the short-term stability characteristic of the oscillator output frequency:

$$\sigma_y{}^2(\tau) \cong \frac{1}{M-1}\sum_{k=1}^{M-1}\frac{(Y_{k+1}-Y_k)^2}{2}$$

where

Y_k are the average fractional frequency fluctuations obtained sequentially, with no systematic dead time between measurements;

τ is the sample time over which measurements is averaged;

M is the number of measurements.

The confidence of the estimate improves as M increases.

3.2.24
r.m.s. fractional frequency fluctuation
measure in the time domain of the short-term frequency stability of an oscillator, based on the statistical properties of a number of frequency measurements, each representing an average of the frequency over the specified sampling interval τ. The preferred measure of fractional frequency fluctuation is:

$$\frac{\Delta F}{F_0}(\tau)_{rms} = \left[\frac{1}{2(M-1)}\sum_{k=1}^{M-1}(Y_{k+1}-Y_k)^2\right]^{1/2} = \left[\sigma_y{}^2(\tau)\right]^{1/2}$$

3.2.25
phase noise
frequency-domain measure of the short-term frequency stability of an oscillator, normally expressed as the power spectral density of the phase fluctuations, Sφ(f), where the phase fluctuation function is $\varphi(t)=2\pi\ Ft-2\pi F_0 t$. The spectral density of phase fluctuation can be directly related to the spectral density of frequency fluctuation by

$$S_\varphi(f) = \left(\frac{F_0}{f}\right)^2 S_y(f) \quad \text{rad}^2/\text{Hz}$$

where

F is the oscillator frequency;

F_0 is the average oscillator frequency;

f is the Fourier frequency.

3.2.26
spectral purity
measure of frequency stability in the frequency domain usually represented as the signal side noise power spectrum expressed in decibels relative to total signal power, per hertz bandwidth. It includes non-deterministic noise power, harmonic distortion components and spurious single frequency interferences

3.2.27
incidental frequency modulation
optional measure of frequency stability in the frequency domain, best described in terms of the spectrum of the resultant base-band signal obtained by applying the oscillator signal to an ideal discriminator circuit of specified characteristics. If the detection bandwidth is adequately specified, the incidental frequency modulation may be expressed as a fractional proportion of the output frequency (for example 2×10^{-8} r.m.s. in a 10 kHz band)

3.2.28
amplitude modulation distortion
non-linear distortion in which the relative magnitudes of the spectral components of the modulating signal waveform are modified. It is also commonly known as frequency distortion, amplitude distortion and amplitude/ frequency distortion

3.2.29
linearity of frequency modulation deviation
measure of the transfer characteristic of a modulation system as compared to an ideal (straight line) function, usually expressed as an allowable non-linearity in per cent of the specified full range deviation. Modulation linearity can also be expressed in terms of the permissible distortion of base-band signals produced by the modulation device (for example, intermediation and harmonic distortion products not to exceed –40 dB relative to the total modulating signal power)

EXAMPLE: Figure 2 is a plot of the output frequency of a typical modulated oscillator specified to have a modulation characteristic of 133,3 Hz/V over a range of ± 3 V, with an allowed non-linearity of ± 5 %. Curve *D* is the actual characteristic compared with the ideal (curve *A*) and the limits (curves *B* and *C*).

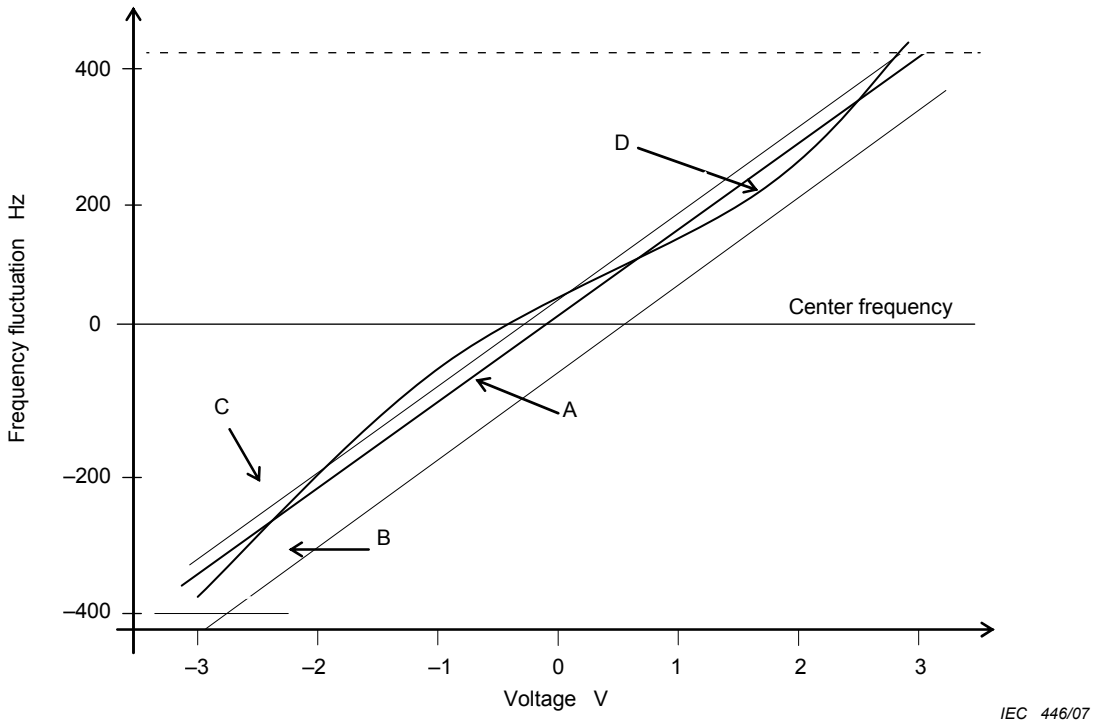


Figure 2 – Typical frequency fluctuation characteristics

3.2.30
harmonic distortion
non-linear distortion characterized by the generation of undesired spectral components harmonically related to the desired signal frequency. Each harmonic component is usually expressed as a power ratio (in decibels) relative to the output power of the desired signal

3.2.31
spurious oscillations
discrete frequency spectral components, non-harmonically related to the desired output frequency, appearing at the output terminal of an oscillator. These components may appear as symmetrical sidebands or as signal spectral components, depending upon the mode of generation. Spurious components in the output spectrum are usually expressed as a power ratio (in decibels) with respect to the output signal power

3.2.32
pulse duration
duration between pulse start time and pulse stop time (see Figure 3)

[IEC 60469-1, definition 3.3.2]

3.2.33
rise time
time interval required for the leading edge of a waveform to change between two defined levels. These levels may be two logic levels V_{OL} and V_{OH} or 10 % to 90 % of its maximum amplitude ($V_{HI} - V_{LO}$), or any other ratio defined in the detail specification (see Figure 3)

where

V_{OL} is the low level output voltage;

V_{OH} is the high level output voltage;

V_{HI} is the upper flat voltage of the pulse waveform;

V_{LO} is the low flat voltage of the pulse waveform.

3.2.34
decay (or fall) time
time interval required for the trailing edge of a waveform to change between two defined levels. These levels may be two logic levels V_{OH} and V_{OL} or 90 % to 10 % of its maximum amplitude ($V_{HI} - V_{LO}$), or any other ratio as defined in the detail specification (see Figure 3)

3.2.35
tri-state output
output stage which may be enabled or disabled by the application of an input control signal. In the disable mode, the output impedance of the gate is set to a high level permitting the application of test signals to following stages

3.2.36
symmetry (mark/space ratio or duty cycle)
ratio between the time (t_1), in which the output voltage is above a specified level, and the time (t_2), in which the output voltage is below the specified level, in percent of the duration of the full signal period. The specified level may be the arithmetic mean between levels V_{OL} and V_{OH}, or 50 % of the peak-to-peak amplitude (see Figure 3).

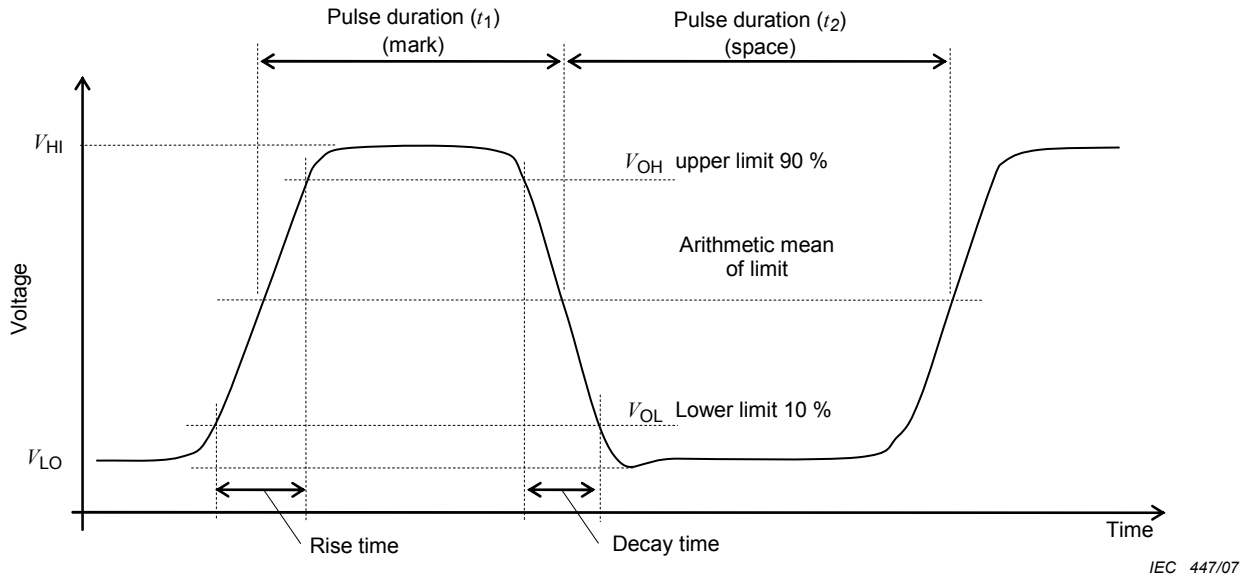


Figure 3 – Characteristics of an output waveform

The ratio is expressed as:

$$\frac{100\ t_1}{t_1 + t_2} : \frac{100\ t_2}{t_1 + t_2}$$

3.2.37
retrace characteristics
ability of an oscillator to return, after a specified time period, to a previously stabilized frequency, following a period in the energized condition

3.2.38
start-up time
time difference t_{SU} between the application of the supply voltage to the oscillator and the time when the r.f. output signal of desired frequency controlled by the quartz resonator fulfils specific conditions which are given below

a) Quasi-sinusoidal waveforms

The signal envelope is 90 % of the steady-state peak-to-peak amplitude (see Figure 20).

b) Pulse waveforms

The output pulse sequence is periodical near the steady-state frequency while its low level V_{LO} remains below V_{OL} and its high level V_{HI} exceeds V_{OH} permanently, where V_{OH} and V_{OL} are defined by the applicable logic family.

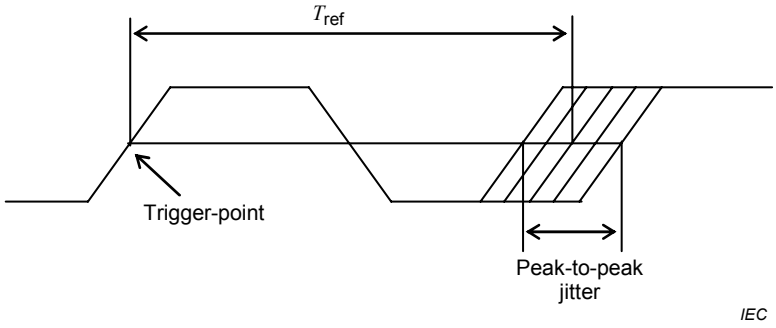
Precaution
The output signal may show spurious oscillations prior to the appearance of the steady-state signal.

3.2.39
phase jitter
short-term variation of the zero crossings of the oscillator output signal from their ideal position in time. The phase variation $\Delta\varphi$ with frequency components greater than or equal to 10 Hz. Variations slower than 10 Hz are called “wander”. Excessive jitter can increase the bit error rate (BER) of a communication signal by incorrectly transmitting a data-stream and can cause synchronization problems

The corresponding variation of the period length

$$\Delta T = \Delta\varphi / (2\pi f_c)$$

is called “period jitter” (f_c is the clock frequency).



Key
$T_{ref.}$ is the period of an ideal reference signal.

Figure 4 – Clock signal with phase jitter

The jitter amplitude is usually referred to the Unit Interval (UI) of one data bit-width (e.g. UI = 6,43 ns for 155,52 Mbit/s for STM-1/OC-3) or defined as absolute time variation (in nanoseconds, picoseconds or femtoseconds). It is quantified either as the peak-to-peak value, or as the r.m.s. value thereof.

“Higher confidence levels are required for some applications, so the peak-to-peak jitter can be specified as a larger range of σ in these cases.”

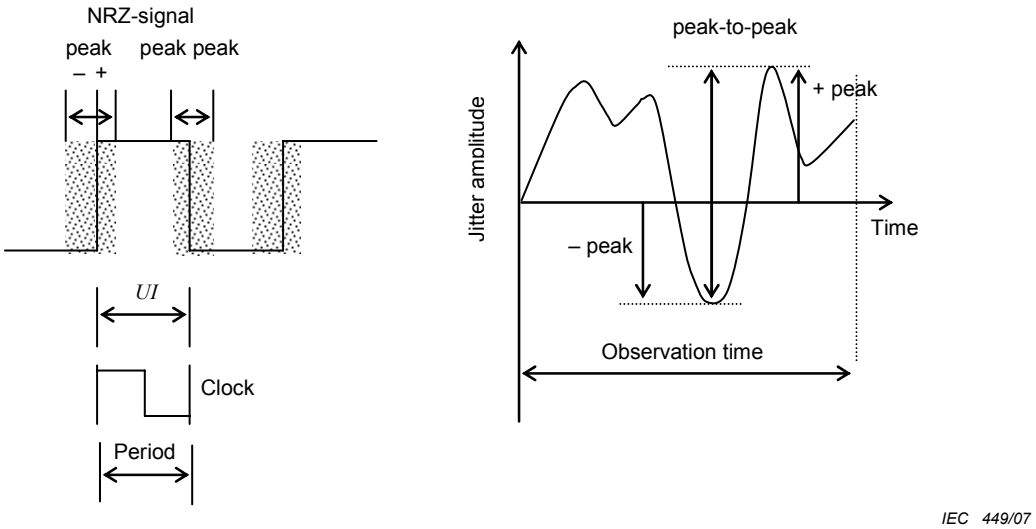


Figure 5 – Phase jitter measures

For random type jitter the r.m.s. value is defined as the standard deviation σ (sigma) of the underlying Gaussian distribution. The peak-to-peak jitter is then the range covered by 7σ (i.e. ±3,5σ), according to a confidence level of 99,95348 % (i.e. 465×10^{-6} tail).

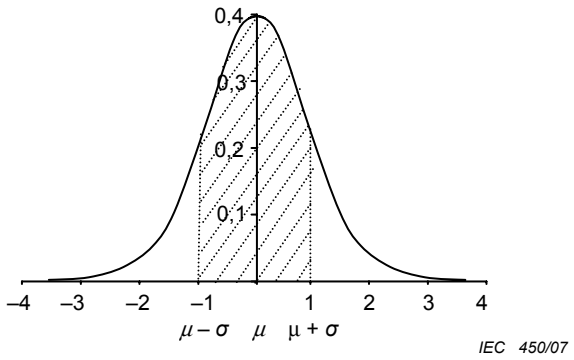


Figure 6 – Gaussian distribution of jitter

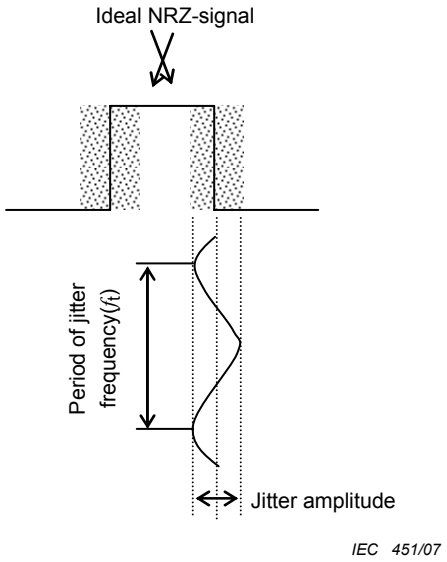


Figure 7 – Jitter amplitude and period of jitter frequency

In the case of subharmonics involved in the signal generation, phase jitter may contain non-random spectral components due to periodical change of the duty cycle. This causes a non-Gaussian distribution, i.e. the 7σ-rule for peak-to-peak values no longer applies. In such cases, only peak-to-peak values are meaningful. However, the determination of peak-to-peak values depends upon observation time. The recommended observation time for peak-to-peak jitter is 1 min. Longer times required when higher confidence is needed (i.e. when a larger range of σ is used to define peak-to-peak random jitter).

For the characterization of jitter, it is important to define the considered Fourier frequency range, i.e. the frequency components of the jitter itself. This is defined by the application (see standards ITU-T G.825, ANSI T1.105.03, Telcordia GR-253 and ETSI EN 300462).

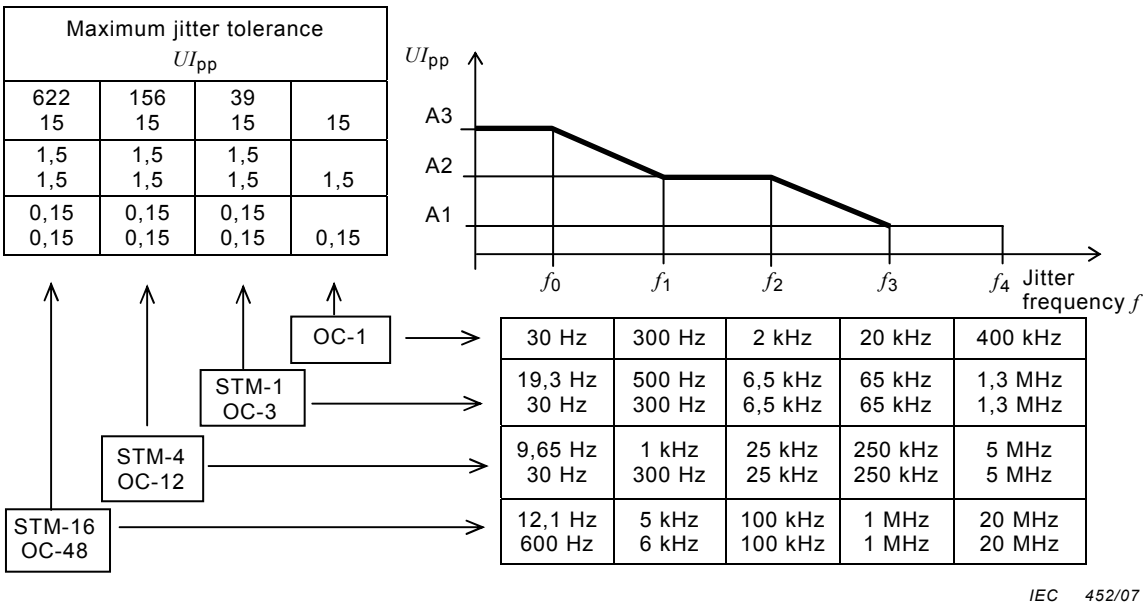


Figure 8 – Jitter tolerance according to ITU-T G.825, ANSI T1.105.03, Telcordia GR-253 and ETSI EN 300462

In connection with jitter and wander, the following three parameters are also used for clock characterization:

– TIE Time Interval Error (in nanoseconds or picoseconds);

– MTIE Maximum Time Interval Error (peak-to-peak TIE);

– TDEV Time deviation (r.m.s. value).

TIE is defined as the time deviation between the signal being measured and the reference clock, typically measured in nanoseconds.

MTIE is a measure that characterises frequency offsets. MTIE(τ) is defined as the largest peak-to-peak TIE in any observation interval of length τ (in seconds).

TDEV characterises the spectral content. TDEV(τ) is defined as the r.m.s. of filtered TIE, where the bandpass filter is centered on a frequency of 0,42/τ. It is calculated from the TIE samples for each point τi by the standard deviation $\sigma(\tau i)$ (see note).

NOTE For more details, refer to standards ITU-T G.810 to G.813, or ANSI T1.101 and T1.105.03, Telcordia GR-253 and ETSI EN 300462.

3.3 Preferred values for ratings and characteristics

Values should be preferably chosen from the following paragraphs, unless otherwise stated in the detail specification.

3.3.1 Climatic category (40/085/56)

For requirements where the operating temperature range of the quartz crystal controlled oscillator is greater than –40 °C to +85 °C, a climatic category consistent with the operating temperature range shall be specified.

3.3.2 Bump severity

(4 000 ± 10) bumps at 400 m/s^2 peak acceleration in each direction along three mutually perpendicular axes (see 5.6.6). Pulse duration: 6 ms.

3.3.3 Vibration severity

Sinusoidal

10 Hz to 55 Hz 0,75 mm displacement amplitude (peak value) 55 Hz to 500 kHz or 55 Hz to 2 000 Hz 100 m/s^2 acceleration amplitude (peak value)	30 min in each of three mutually perpendicular axes at 1 octave/min (see 5.6.7)
10 Hz to 55 Hz 1,5 mm displacement amplitude (peak value) 55 Hz to 2 000 Hz 200 m/s^2 acceleration amplitude (peak value)	30 min in each of three mutually perpendicular axes at 1 octave/min (see 5.6.7)

Random

(19,2 m/s^2)^2/Hz between 20 Hz and 2 000 Hz 196 m/s^2 acceleration or (48 m/s^2)^2/Hz between 20 Hz and 2 000 Hz 314 m/s^2 acceleration	30 min in each of three mutually perpendicular axes at 1 octave/min (see 5.6.7)

3.3.4 Shock severity

1 000 m/s^2 peak acceleration for 6 ms duration; three shocks in each direction along three mutually perpendicular axes (see 5.6.8), half-sine pulse, unless otherwise stated in the detail specification.

3.3.5 Leak rate

10^{-1} Pa cm^3/s (10^{-6} bar cm^3/s)

10^{-3} Pa cm^3/s (10^{-8} bar cm^3/s)

3.4 Marking

3.4.1 The quartz crystal controlled oscillator shall be clearly and durably marked (see 5.6.21) with items a) to g) below, and with as many of the remaining items as considered necessary:

a) type designation as defined in the detail specification;
b) nominal frequency in kilohertz or megahertz;
c) year and week of manufacture;
d) mark of conformity (unless a certificate of conformity is used);
e) factory identification code;
f) manufacturer's name or trade mark;
g) terminal identification;
h) designation of electrical connections;
j) power supply voltage and polarity (if applicable);
k) serial number (if applicable).

Where the available surface area of miniature quartz crystal controlled oscillators imposes practical limits in the amount of marking, instructions on the marking to be applied shall be given in the detail specification.

3.4.2 The primary packaging containing the quartz crystal controlled oscillator(s) shall be clearly marked with the information listed in 3.4.1 except item g) and electrostatic sensitive device (ESD) identification, where necessary.

4 Quality assessment procedures

Two methods are available for the approval of quartz crystal controlled oscillators of assessed quality. They are qualification approval and capability approval.

4.1 Primary stage of manufacture

The primary stage of manufacture for a quartz crystal controlled oscillator in accordance with 3.1.1.2 of IEC QC 001002-3 shall be as follows:

a) for oscillators incorporating a sealed crystal unit:
   – the assembly of the quartz crystal controlled oscillator;
b) for oscillators incorporating an unencapsulated crystal unit:
   – the final surface finishing of the crystal element in addition to the assembly of the oscillator.

NOTE The final surface finishing of the crystal element could be any of the following operations: lapping; polishing; etching; cleaning, in the case of polished plates.

4.2 Structurally similar components

The grouping of structurally similar crystal controlled oscillators for the purpose of qualification approval, capability approval and quality conformance inspection shall be prescribed in the relevant sectional specification.

4.3 Subcontracting

These procedures shall be in accordance with Annex B to Clause 2 of IEC QC 001002-3.

There shall be no subcontracting after the assembly of the crystal to the electronic circuit, except in the case of sealed crystal units, where the sealing of the final enclosure of the oscillator may be permitted.

4.4 Incorporated components

Where the final component contains components of a kind covered by a generic specification in the IEC series, these shall be produced using the normal IEC release procedures.

Where the contained components are not produced to an IEC detail specification, the approved manufacturer's chief inspector shall verify their quality by the use of

– a procurement specification covering all aspects necessary to ensure their satisfactory performance as part of the final product;
– an adequate approval test program maintaining a record of results;
– sufficient goods inward inspection procedures to ensure continued satisfactory performance of the final product.

4.5 Manufacturer’s approval

To obtain manufacturer's approval the manufacturer shall meet the requirements of 10.2 of IEC QC 001002.

4.6 Approval procedures

4.6.1 General

To qualify a quartz crystal controlled oscillator, either capability approval or qualification approval procedures may be used. These procedures conform to those stated in IECQ 01 and IEC QC 001002-3.

4.6.2 Capability approval

Capability approval is appropriate when structurally similar quartz crystal controlled oscillators based on common design rules, are fabricated by a group of common processes.

Under capability approval, detail specifications fall into the following three categories:

a) capability qualifying components (CQCs)

   A detail specification shall be prepared for each CQC as agreed with the NSI. It shall identify the purpose of the CQC and include all relevant stress levels and test limits;

b) standard catalogue items

   When a component covered by the capability approval procedure is intended to be offered as a standard catalogue item, a detail specification complying with the blank detail specification shall be written. Such specifications shall be registered by the IECQ;

c) custom built quartz controlled oscillators

   The contents of the detail specification shall be by agreement between the manufacturer and the customer in accordance with 6.6.1 of IEC QC 001002-3.

Further information on detail specifications is contained in the sectional specification IEC 60679-4.

The product and capability qualifying components (CQCs) are tested in combination and approval given to a manufacturing facility on the basis of validated design rules, processes and quality control procedures. Further information is given in 4.7 and in the sectional specification IEC 60679-4.

4.6.3 Qualification approval

Qualification approval is appropriate for components manufactured to a standard design and established production process and conforming to a published detail specification.

The program of tests defined in the detail specification for the appropriate assessment and severity revel applies directly to the quartz crystal controlled oscillator to be qualified, as prescribed in 4.8 and the sectional specification IEC 60679-5.

4.7 Procedures for capability approval

4.7.1 General

The procedures for capability approval shall be in accordance with 4.2 of IEC QC 001002-3.

4.7.2 Eligibility for capability approval

The manufacturer shall comply with the requirements of 4.2.1 of IEC QC 001002-3 and the primary stage of manufacture as defined in 4.1 of this generic specification.

4.7.3 Application for capability approval

In order to obtain capability approval the manufacturer shall apply the rules of procedure given in 4.2.4 of IEC QC 001002-3.

4.7.4 Granting of capability approval

Capability approval shall be granted when the procedures in accordance with 4.2.7 of IEC QC 001002-3 have been successfully completed.

4.7.5 Capability manual

The contents of the capability manual shall be in accordance with the requirements of the sectional specification.

The NSI shall treat the capability manual as a confidential document. The manufacturer may, if he so wishes, disclose part or all of it to a third party.

4.8 Procedures for qualification approval

4.8.1 General

The procedures for qualification approval shall be in accordance with IEC QC 001002-3.

4.8.2 Eligibility for qualification approval

The manufacturer shall comply with the requirements of 3.1.1 of IEC QC 001002-3 and the primary stage of manufacture as defined in 4.1 of this generic specification.

4.8.3 Application for qualification approval

In order to obtain qualification approval the manufacturer shall apply the procedures given in 3.1.3 of IEC QC 001002-3.

4.8.4 Granting of qualification approval

Qualification approval shall be granted when the procedures in accordance with 3.1.5 of IEC QC 001002-3 have been successfully completed.

4.8.5 Quality conformance inspection

The blank detail specification associated with the sectional specification shall prescribe the test schedule for quality conformance inspection.

4.9 Test procedures

The test procedures to be used shall be selected from this generic specification. If any required test is not included, then it shall be defined in the detail specification.

4.10 Screening requirements

Where screening is required by the customer for quartz crystal controlled oscillators, this shall be specified in the detail specification.

4.11 Rework and repair work

4.11.1 Rework

Rework is the rectification of processing errors and shall not be carried out if prohibited by the sectional specification. The sectional specification shall state if there is a restriction on the number of occasions that rework may take place on a specific component.

All rework shall be carried out prior to the formation of the inspection lot offered for inspection to the requirements of the detail specification.

Such rework procedures shall be fully described in the relevant documentation produced by the manufacturer and shall be carried out under the direct control of the chief inspector.

Subcontracting of rework is not permitted.

4.11.2 Repair work

Repair work is the correction of defects in a component after release to the customer.

Components that have been repaired can no longer be considered as representative of the manufacturer's production and may not be released under the IECQ system.

4.12 Certified test records

The requirements of Annex B of IEC QC 001002-2 shall apply. When certified test records (CTR) are prescribed in the sectional specification for qualification approval and are requested by the customer, the results of the specified tests shall be summarized.

4.13 Validity of release

Quartz crystal controlled oscillators held for a period exceeding two years following acceptance inspection shall be reinspected for the electrical tests detailed in 5.5.4 and 5.5.17, prior to release.

4.14 Release for delivery

Quartz crystal controlled oscillators shall be released in accordance with 4.3 of IEC QC 001002-3.

4.15 Unchecked parameters

Only those parameters of a component which have been specified in a detail specification and which were subject to testing, can be assumed to be within the specified limits. It should not be assumed that any parameter not specified will remain unchanged from one component to another. Should it be necessary for further parameters to be controlled, then a new, more extensive, detail specification should be used. The additional test method(s) shall be fully described and appropriate limits, AQLs and inspection levels specified.

5 Test and measurement procedures

5.1 General

The test and measurement procedures shall be carried out in accordance with the relevant detail specification.

5.2 Test and measurement conditions

5.2.1 Standard conditions for testing

Unless otherwise specified, all tests shall be carried out under the standard atmospheric conditions for testing as specified in 5.3 of IEC 60068-1.

Temperature	15 °C to 35 °C
Relative humidity	25 % to 75 %
Air pressure	86 kPa to 106 kPa (860 mbar to 1060 mbar)

In case of dispute, the referee conditions are the following:

Temperature	25 °C ± 2 °C
Relative humidity	48 % to 52 %
Air pressure	86 kPa to 106 kPa (860 mbar to 1060 mbar)

Before measurements are made, the quartz crystal controlled oscillators shall be stored at the measuring temperature for a time sufficient to allow the quartz crystal controlled oscillator to reach thermal equilibrium. Controlled recovery conditions and standard conditions for assisted drying are given in 5.4 and 5.5 of IEC 60068-1.

The ambient temperature during the measurements shall be recorded and stated in the test report.

5.2.2 Equilibrium conditions

All electrical tests shall be conducted under equilibrium conditions, unless otherwise specified.

When test conditions cause a significant change with time of the characteristic being measured, means of compensation for such effects shall be specified, for example the period of time that the oscillator shall be maintained at specified test conditions before making a measurement.

5.2.3 Air flow conditions for temperature tests

When devices are to be measured at temperatures other than 25 °C ± 2 °C, they shall be subjected to adequate forced air circulation to ensure close temperature control.

If heat loss due to forced air circulation affects the performance of the oscillator, still air conditions shall be simulated by enclosing the oscillator in a draught shield consisting of a thermally conducting box, having internal dimensions so that a 20 mm ± 5 mm clearance is maintained from all surfaces. The temperature at which measurements should be taken under these conditions is the reference point temperature on the surface of the draught shield.

If a draught shield is necessary, it shall be used for both high and low temperature tests.

5.2.4 Power supplies

DC power sources used in the testing of crystal controlled oscillators shall not have a ripple content large enough to effect the desired accuracy of measurement; a.c. power sources shall be transient free. When the ripple and/or the transient content of the power sources are critical to the measurement being performed, their effects shall be fully defined in the detail specification.

5.2.5 Precision of measurement

The limits given in the detail specification are true values. Measurement inaccuracies shall be taken into account when evaluating the results. Precautions should be taken to reduce measurement errors to a minimum.

5.2.6 Precautions

5.2.6.1 Measurements

The measurement circuits shown for specified electrical tests are the preferred circuits. Due allowance shall be made for any loading effects in cases where the measuring apparatus modifies the characteristics being examined.

5.2.6.2 Electrostatic sensitive devices

Where the component is identified as electrostatic sensitive, precautions shall be taken to prevent damage from electrostatic charge both before, during, and after test (see IEC 61000-4-2).

5.2.7 Alternative test methods

Measurements shall preferably be carried out using the methods specified. Any other method giving equivalent results may be used, except in case of dispute.

NOTE "Equivalent" means that the value of the characteristic established by such other methods falls within the specified limits when measured by the specified method.

5.3 Visual inspection

Unless otherwise specified, external visual examination shall be performed under normal factory lighting and visual conditions.

5.3.1 Visual test A

The quartz crystal controlled oscillator shall be visually examined to ensure that the condition, workmanship and finish are satisfactory. The marking shall be legible.

5.3.2 Visual test B

The quartz crystal controlled oscillator shall be visually examined under ×10 magnification. There shall be no cracks in the glass or damage to the terminations. Minute flaking around the further edge of a meniscus shall not be considered a crack.

5.3.3 Visual test C

The quartz crystal controlled oscillator shall be visually examined. There shall be no corrosion or other deterioration likely to impair satisfactory operation. The marking shall be legible.

5.4 Dimensions and gauging procedures

5.4.1 Dimensions - Test A

The dimensions, spacing, and alignment of the terminations shall be checked and shall comply with the specified values.

5.4.2 Dimensions - Test B

The dimensions shall be measured and shall comply with the specified values.

5.5 Electrical test procedures

5.5.1 Insulation resistance

A maximum voltage of 20 V, unless otherwise stated in the detail specification, shall be applied to the specified test points using the test circuit shown in Figure 9a. The resulting current shall be measured. It shall be less than the specified maximum value.

Alternatively, the resistance shall be directly measured with an ohmmeter (see Figure 9b). It shall be greater than the minimum specified.

Precautions shall be taken to ensure that measurements are made across the specified points with an applied voltage of the correct polarity and not exceeding the specified value. Failure to observe any of these conditions may result in damage to the device under test.

After the test, measurements shall be made to ensure that the oscillator is still functional.

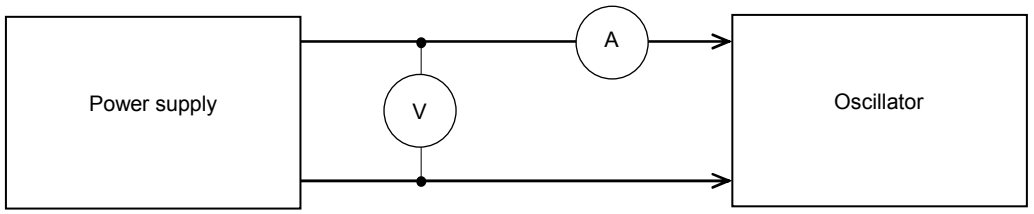


Figure 9a – Voltage-current method

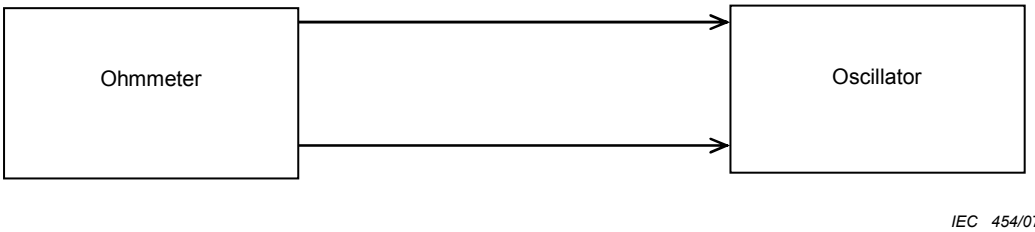


Figure 9b – Ohmmeter method

Figure 9 – Test circuits for insulation resistance measurements

5.5.2 Voltage proof

The specified voltage shall be applied only across the designated terminals, using the test circuit shown in Figure 10, after any specified preconditioning procedures have been applied. The source resistance and maximum permissible current flow shall be stated in the detail specification.

There shall be no arcing or other evidence of electrical breakdown.

After the test, measurements shall be made to ensure that the oscillator is still functional.

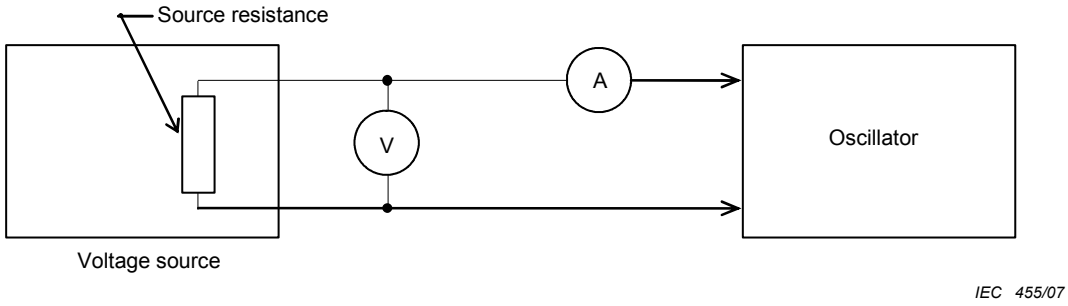


Figure 10 – Test circuit for voltage proof test

5.5.3 Input power

5.5.3.1 Oscillator input power

The oscillator shall be connected to the power supply and specified load as shown in Figure 11. The specified voltage shall be applied and allowed to stabilize for the specified time. Measurements of the voltage and current shall be made at the reference temperature, unless otherwise stated in the detail specification. The input power shall be calculated using these measurements.

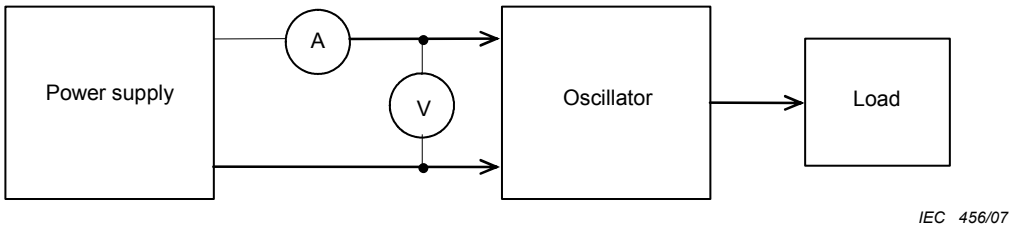


Figure 11 – Test circuit for oscillator input power measurement

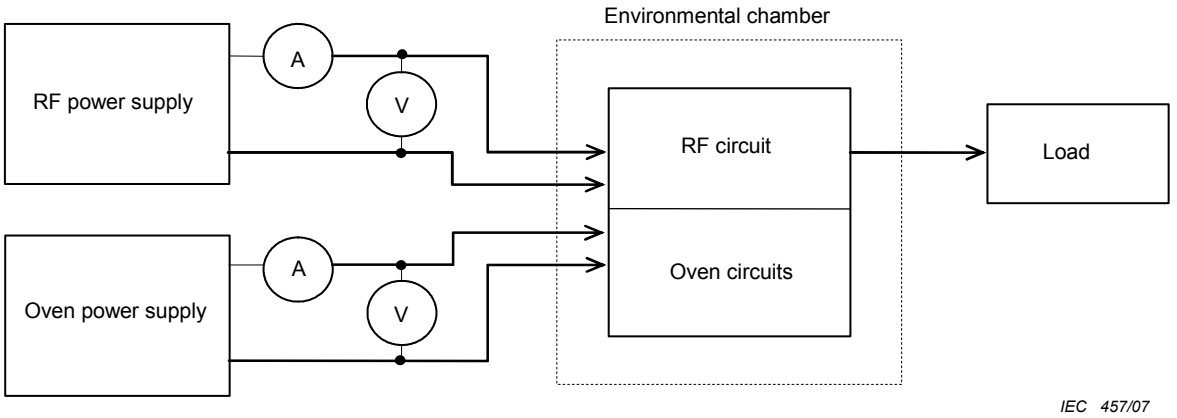
5.5.3.2 Oven and oscillator input power

The oscillator shall be connected to the test circuit (see note to Figure 12) and placed in the environmental chamber as shown in Figure 12. The load and supply voltage(s) shall be as specified in the detail specification. Where the input power to the oscillator will be affected by forced air circulation, still air conditions shall be simulated by enclosing the oscillator in a draught shield, as described in 5.2.3. Readings of voltage and current shall be taken at the specified temperatures as stated in the detail specification (usually at the minimum and maximum of the operating temperature range, as well as at the reference temperature).

The temperature will normally be taken as the reference point temperature on the surface of the draught shield, when used. If peak power is specified, the transient values of voltage and current shall be measured when the environmental chamber is adjusted to each of the specified temperatures. In this case, it may be necessary to attach a recording meter to the ammeter and/or voltmeter, so as to measure adequately the transient values.

The oscillator and oven shall be allowed to reach thermal equilibrium at the operating temperature, while unenergized, prior to any measurement of peak power. Should peak power be required, the environmental chamber shall have a thermal time constant significantly less than that of the oven-oscillator combination being measured.

The input power is calculated using the measured values of voltage and current.



NOTE The power to the oscillator may be supplied from the same power supply.

Figure 12 – Test circuit for oven and oscillator input power measurement

5.5.3.3 Oven input power

To measure the oven input power only, the test procedure described in 5.5.3.2 shall be used, except that the power supply to the oscillator shall be disconnected.

5.5.4 Output frequency

Output frequency measurements shall be made using either method 1 or method 2, according to the accuracy specified for the oscillator.

The following precautions shall be observed:

– the accuracy and resolution of the system shall always be an order better than that of the frequency to be determined;

– the oscillator shall be correctly loaded;

– the stability and accuracy of the system shall be verified by periodic checks of the frequency standard against an internationally recognized standard;

– for accurate measurements, it is essential that great care be taken to ensure that environmental conditions do not influence the results.

Method 1 – Measurement for accuracies less than or equal to 1×10^{-8}

The oscillator shall be connected, as shown in Figure 13, to the specified supply voltage and load. It shall be allowed to stabilize for the specified time under normal operating conditions.

The frequency shall then be measured on the frequency counter. The frequency may be determined either by direct frequency measurement or by period averageing. The time period of measurement will normally lie in the range of 0,1 s to 10 s. Period averageing will generally be used for the measurement of frequencies less than 5 MHz.

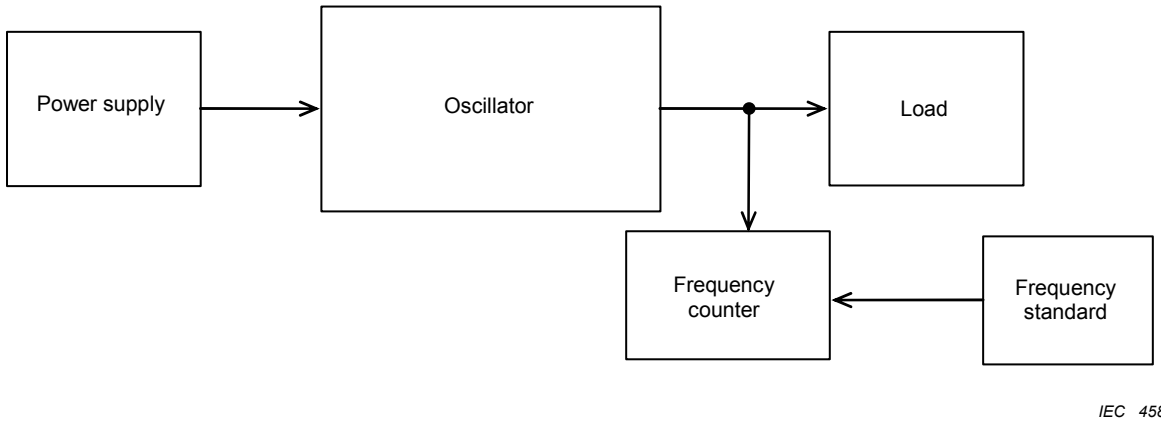


Figure 13 – Test circuit for measurement of output frequency, method 1

Method 2 – Measurement for accuracies greater than 1×10^{-8}

The oscillator shall be connected, as shown in Figure 14, to the specified supply voltage and load. It shall be allowed to stabilize for the specified time under normal operating conditions.

The frequency shall be measured on the frequency counter after multiplication to a frequency commensurate with the required accuracy. The time period will normally be in the range of 0,1 s to 10 s. For example a 2,5 MHz signal would need to be multiplied to 25 MHz to enable a measurement of frequency to be obtained to an accuracy better than 1×10^{-8} within 10 s.

Alternative methods include the use of a high speed counter in place of the frequency multiplier. It is also possible to use a system of phase comparison against a frequency synthesizer which is driven from a frequency standard, for accuracies of 1×10^{-10} or better.

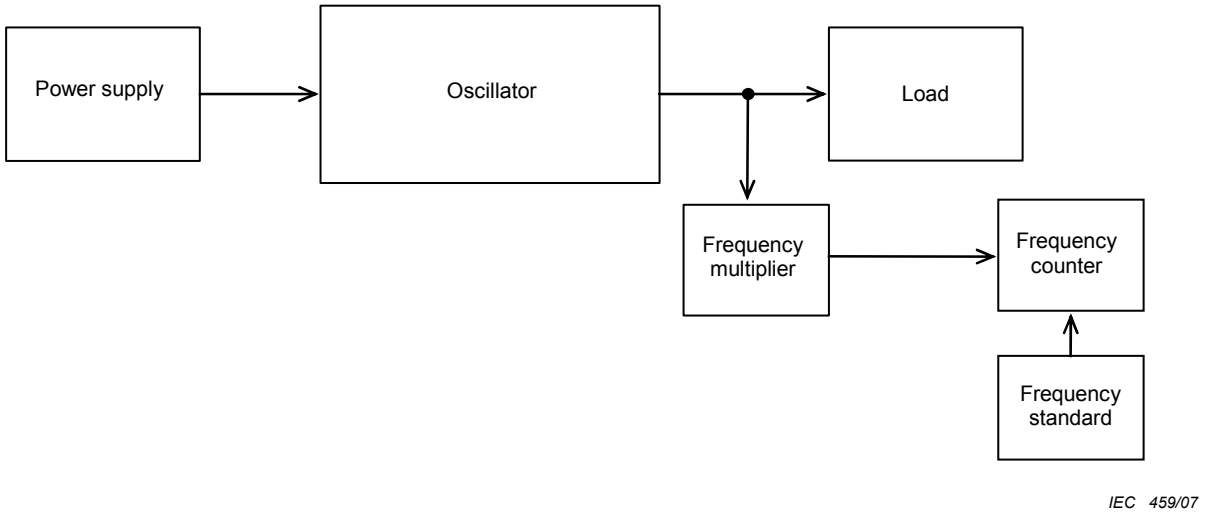


Figure 14 – Test circuit for measurement of output frequency, method 2

5.5.5 Frequency/temperature characteristics

5.5.5.1 Frequency at specified temperature(s)

The unenergized oscillator shall be placed in the environmental chamber and connected to the specified load using the test circuit shown in Figure 15. The specified supply voltage shall then be applied to the oscillator.

Where the input power to the oscillator will be affected by forced air circulation, still air conditions shall be simulated by enclosing the oscillator in a draught shield as described in 5.2.3.

The chamber shall be allowed to stabilize at the specified temperature and, when the oscillator has reached equilibrium (see 5.2.2), measurements of the frequency shall be made using the appropriate measurement method given in 5.5.4.

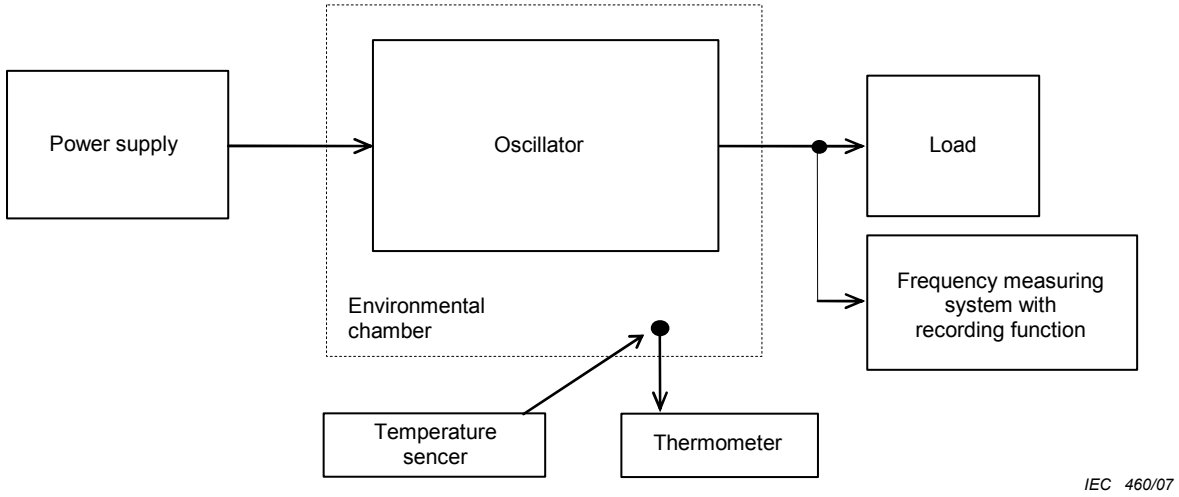


Figure 15 – Test circuit for measurement of frequency/temperature characteristics

5.5.5.2 Total frequency excursion

The unenergized oscillator shall be placed in the environmental chamber and connected to the specified load using the test circuit shown in Figure 15. The specified supply voltage shall then be applied to the oscillator.

Where the input power to the oscillator will be affected by forced air circulation, still air conditions shall be simulated by enclosing the oscillator in a draught shield as described in 5.2.3.

The chamber shall be allowed to stabilize at a temperature extreme and, when the oscillator has reached equilibrium (see 5.2.2), the frequency and temperature shall be recorded using the appropriate frequency measurement method given in 5.5.4.

The test chamber temperature shall be changed in incremental steps of 1,5 °C, ensuring that equilibrium is reached after each temperature step, or changed at a rate of 0,5 °C/min to the other extreme of temperature, unless otherwise specified in the detail specification.

Recordings of the frequency and temperature shall be made during the test.

If it is required by the detail specification to determine the reproducibility of the frequency/ temperature characteristics, the frequencies shall be recorded with temperature changes in both directions.

NOTE In some applications, it may be required to determine the reproducibility of the frequency/temperature characteristics as the temperature is first increased from minimum to maximum, then decreased from maximum to minimum. Differences in the characteristics obtained during increasing and decreasing temperatures are called retrace errors, or hysteresis, and are of particular importance when testing TCXO devices.

5.5.6 Frequency/load coefficient

Using a frequency measuring system as described in 5.5.4, measurements of the oscillator output frequency shall be made for the specified nominal load, minimum load and maximum load, all other operating parameters being maintained constant at their specified values. The load values shall then be calculated taking into account the effect of the measuring equipment connected to the output of the oscillator, which shall be included in the total load value.

5.5.7 Frequency/voltage coefficient

Using a frequency measuring system as described in 5.5.4, and maintaining all other operating parameters at their specified values, measurement of the oscillator frequency shall be made when the power supply voltage is adjusted to its specified nominal value, to its minimum value and to its maximum value. In all cases, the specified stabilization time shall be allowed between adjustment of supply voltage and measurement of frequency.

A transient frequency excursion may occur immediately after adjustment of the power supply voltage, particularly if the device under test is either an OCXO or TCXO type. When the magnitude of this transient excursion is of importance, recording type meters shall be used to record the frequency excursion. The maximum permissible deviations during the transient interval shall be separately specified.

When required, an environmental chamber shall be used to maintain the ambient temperature at its specified value during the performance of this test.

5.5.8 Frequency stability with thermal transient

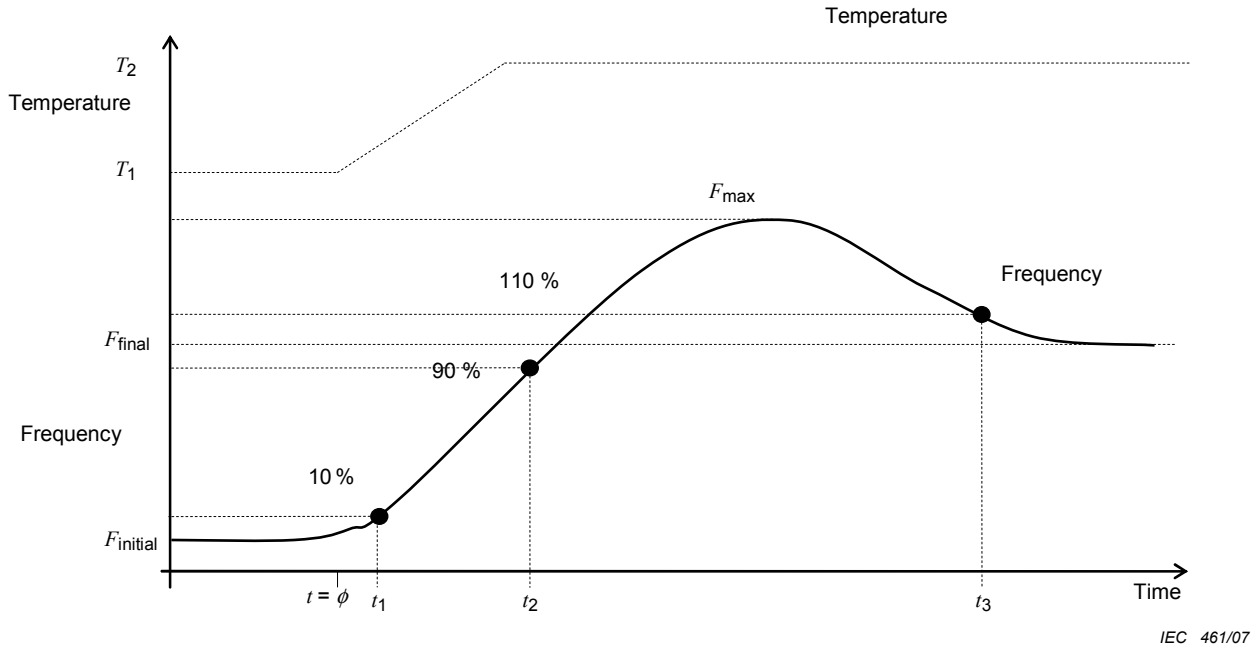
The unenergized oscillator shall be placed in the environmental chamber and connected to the specified load, using the test circuit shown in Figure 15. The specified voltage shall then be applied to the oscillator. The chamber shall be allowed to stabilize and the oscillator to reach equilibrium (see 5.2.2) at the specified initial temperature T_1. The oscillator output frequency shall be recorded.

The environmental chamber temperature shall then be changed at the specified rate to the final temperature T_2.

The oscillator output frequency and the environmental chamber temperature (as measured at the reference point) should be continuously recorded during and after this operation, resulting in a plot of both frequency change and temperature change similar to that in Figure 16, from which the thermal response time and the overshoot may be determined.

5.5.8.1 The overshoot of the transient excursion shall be specified in fractional parts of the nominal frequency (e.g. overshoot shall not exceed 2×10^{-7}):

$$\Delta F_{\text{os}} = \frac{F_{\text{max}} - F_{\text{final}}}{F_{\text{nomi}}}$$



t = Φ = end of stabilization time

t_1 = time for frequency to change 10 % of the steady-state increment

t_2 = time for frequency to change 90 % of the steady-state increment

t_3 = time for frequency to reach 110 % of the steady-state increment on the recovery form overshoot (in the case where overshoot is greater than 10 %)

Figure 16 – Thermal transient behaviour of typical oscillator

5.5.8.2 Unless otherwise specified, the thermal response time is the time interval between the instant the frequency has changed 10 % of the overall change and the instant the frequency has attained a value within 10 % (of the change) of its final frequency.

There are two possible cases, as shown by the sample recordings in Figure 16:

– when the overshoot is less than 10 %, the thermal response time is equal to $t_2 - t_1$ min;
– when the overshoot is equal or greater than 10 %, the thermal response time is equal to $t_3 - t_1$ min.

5.5.9 Oscillation start-up

The purpose is to determine the reliable start-up of the oscillation amplitude and to measure the start-up time.

Figure 17 depicts the generalized oscillator circuit.

The start-up characteristics of a real crystal oscillator depend on the following major factors.

Oscillator stage:

– noise factor of the active device;
– open loop gain (or excess negative resistance) of the oscillation sustaining stage;
– amplitude limiting of the active circuit;
– loaded Q (or effective bandwidth of the resonator);
– drive level dependency of the crystal resonance resistance.

Output stage:

– analog sinusoidal output;
– logic output.

Internal power lines:

– blocking capacitors;
– voltage regulators.

Supply voltage:

– rise time, soak time, off time;
– output impedance.

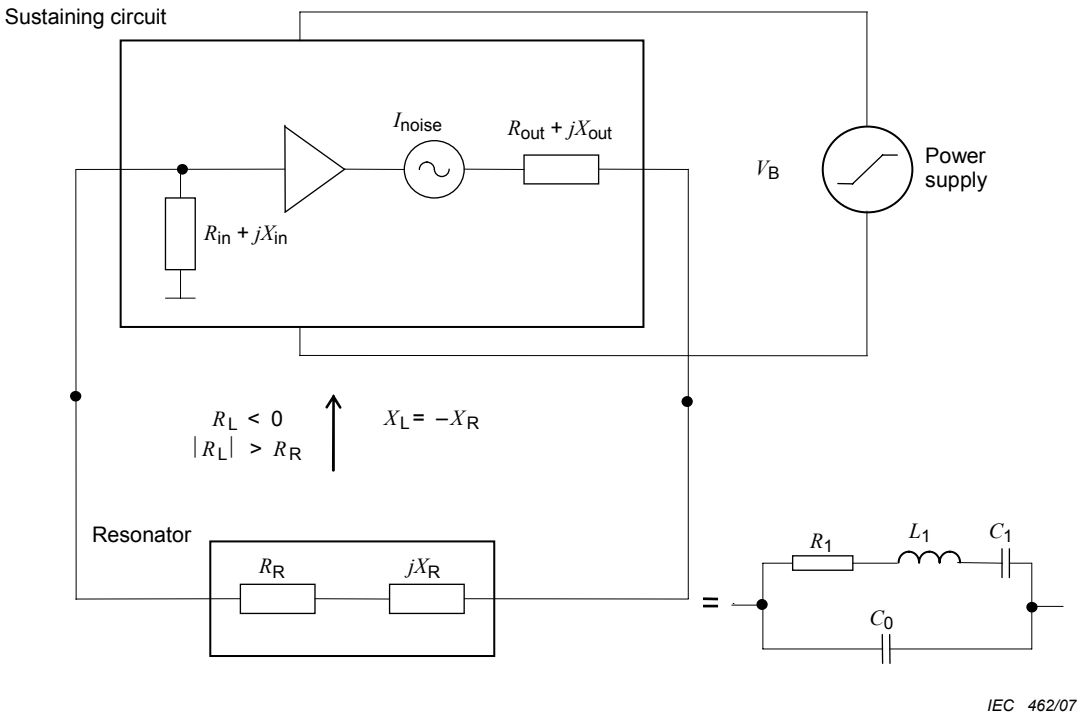


Figure 17 – Generalized oscillator circuit

5.5.9.1 Start-up behaviour

In order to determine whether the oscillation starts up reliably, the oscillator shall be connected to the test circuit for start-up behaviour shown in Figure 18.

The oscillator shall be connected to a programmable power supply. The r.f. output signal and the supply voltage are registered by an oscilloscope, the time scale of which is suitably set to display the whole start-up interval.

The supply voltage ramps linearly from zero to the nominal operating voltage. The ramp time t_{ramp} is chosen to be at least 100 to 1 000 times the specified or expected start-up time of the oscillator.

The oscillator shall show a regular and repeatable start-up behaviour within the time interval of the supply voltage ramp, as shown in Figure 19.

- **Specified conditions**

The following test conditions shall be stated in the detail specification:

– power supply voltage;
– load details;
– start-up time;
– in case of VCXO, d.c. control voltage.

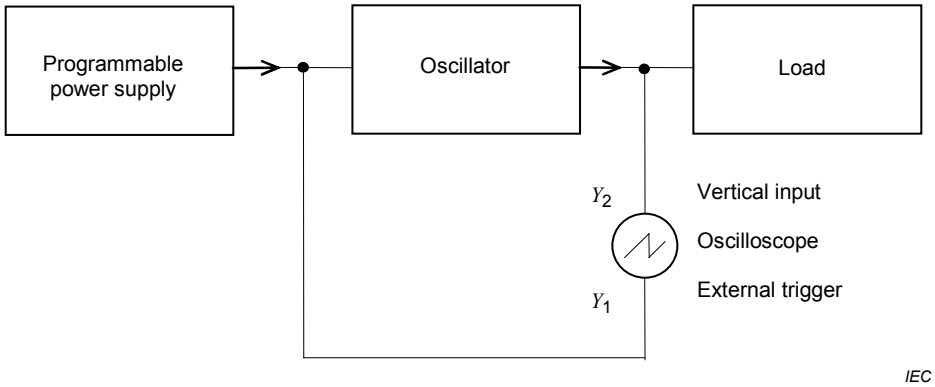


Figure 18 – Test circuit for start-up behaviour and start-up time measurement

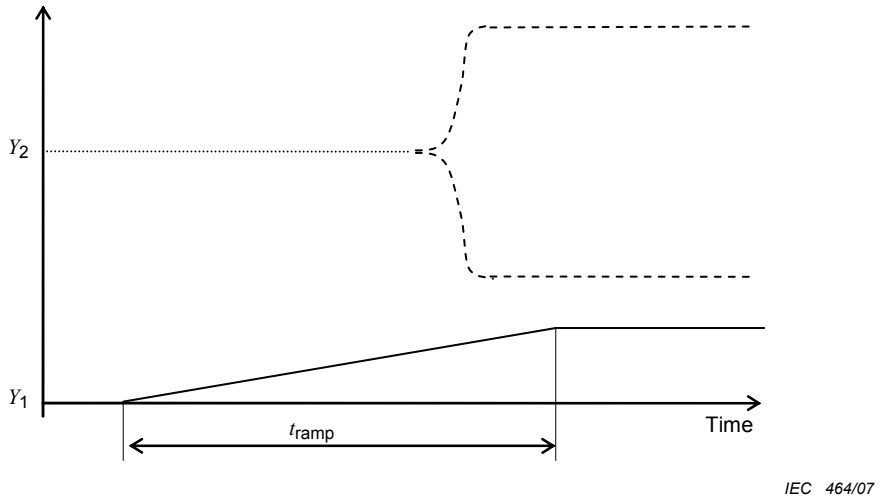


Figure 19 – Typical start-up behaviour with slow supply voltage ramp

5.5.9.2 Start-up time

In order to measure the start-up time of oscillation t_{SU} under specified conditions, the oscillator shall be connected to a programmable power supply (see Figure 18).

The r.f. output signal and the supply voltage shall be registered by an oscilloscope, the time scale of which is suitably set to display the whole start-up interval.

The supply voltage ramps up linearly from zero to the nominal operating voltage. The ramp time t_{ramp} is chosen to be less than one tenth of the specified or expected start-up time of the oscillator.

The start-up time t_{SU} is measured as the difference between the starting point of the d.c. ramp and the time when the r.f. output signal fulfils certain conditions which are given below:

a) quasi-sinusoidal waveforms

the signal envelope is 90 % of the steady-state peak-to-peak amplitude, unless otherwise specified;

b) pulse waveforms

the output pulse sequence is periodical near the steady-state frequency while its low level V_{LO} remains below V_{OL} and its high level V_{HI} exceeds V_{OH} permanently, where V_{OH} and V_{OL} are defined by the applicable logic family.

- **Precaution**

Logic output may show spurious oscillations prior to the appearance of the steady-state signal.

NOTE Make sure that the internal blocking capacitors of the oscillator are discharged before the start of the measurement.

An example is given in Figure 20.

The described procedure can be applied either as a single shot or as a periodical measurement. In the latter case, the following conditions shall be fulfilled (see Figure 21):

t_{ramp} as above;

t_{hold} ≥ 100 t_{SU};

t_{off} minimum length shall be chosen so that a further prolongation does not change the result for t_{SU}, for example t_{off} ≥ 100 t_{SU}.

During t_{off} the supply voltage terminal of the oscillator shall be short-circuited to ground in order to discharge internal blocking capacitors properly.

NOTE The factor 100 in formulae for t_{hold} and t_{off} can be reduced to smaller volumes, however, it should be verified that the measured start-up time is not changed, particularly for high Q resonators.

- **Precaution**

The power supply shall be able to deliver sufficient current to realize the specified voltage ramp at the oscillator supply voltage terminal. It shall be able to drain the discharge current of the oscillator during the t_{off} period.

Specified conditions

The following test conditions shall be stated in the detail specification:

– power supply voltage;
– load details;
– start-up time;
– in the case of VCXO: d.c. control voltage.

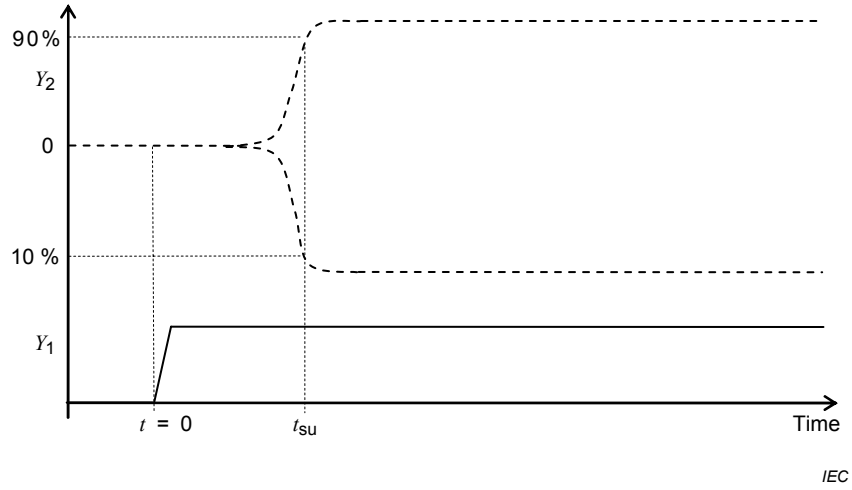


Figure 20 – Definition of start-up time

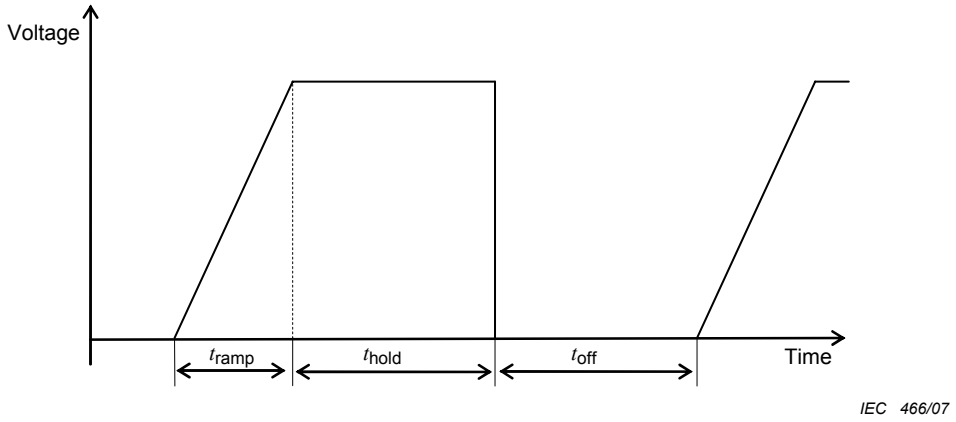


Figure 21 – Supply voltage waveform for periodical t_{SU} measurement

5.5.10 Stabilization time

The unenergized oscillator shall be placed in the environmental chamber and connected to the specified load using the test circuit shown in Figure 15. The frequency measurement used shall be as described in 5.5.4. The temperature of the chamber shall be adjusted to that specified in the detail specification. The oscillator shall then be energized and the output frequency registered on the recording meter as a function of time. The stabilization time t_s shall be the time taken for the oscillator output frequency to remain within a specified tolerance of its long-term value determined after a specified elapsed time (see Figure 22).

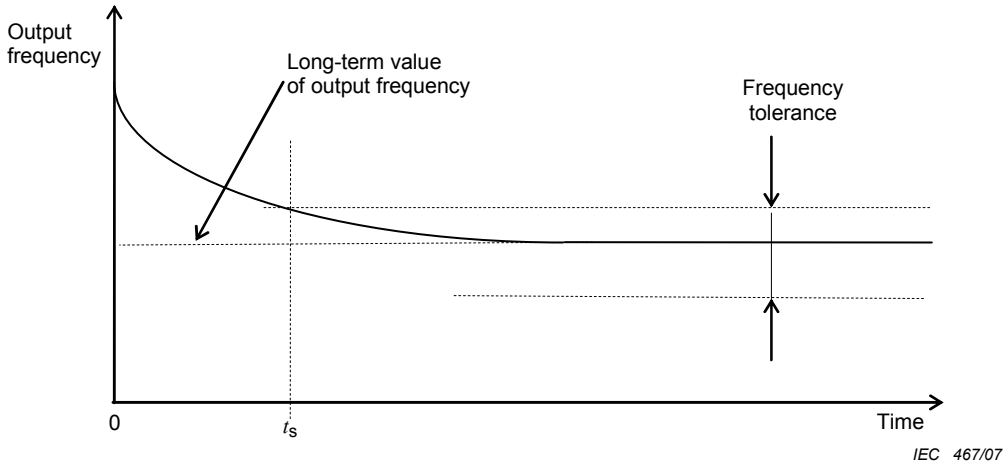


Figure 22 – Typical oscillator stabilization characteristic

5.5.11 Frequency adjustment range

The oscillator shall be connected as shown in 5.5.4 and, where necessary, to an appropriate control voltage. The oscillator shall be energized and allowed to stabilize for the specified time under normal operating conditions. The means by which the oscillator output frequency adjustment is made shall be adjusted to its maximum and minimum and the output frequency measured, unless otherwise stated in the detail specification.

5.5.12 Retrace characteristics

The unenergized oscillator shall be placed in the environmental chamber and connected to the specified load, using the test circuit shown in Figure 15. The chamber shall be maintained at a temperature in the range 20 °C to 30 °C, controlled within ±0,5 °C, unless otherwise stated in the detail specification. The oscillator shall be energized and all operating parameters adjusted to specified values, after which the frequency shall be measured as a function of time.

Following a specific period of operation (t_1, Figure 23, which shall exceed the stabilization time), the output frequency shall be recorded. The oscillator is then turned off, and allowed to assume the specified storage temperature for the specified time period t_2. At the end of the storage period, power is again applied, and frequency recorded as a function of time. The retrace time t_r is the time period following application of power required for the output frequency to return to within the specified tolerance of the value recorded before turn-off.

If the oscillator is stored (during period t_2) elsewhere than in the environmental chamber, adequate time shall be allowed for the oscillator to settle to the temperature specified for frequency measurement before any measurement of frequency takes place; this stabilization time (in an unenergized condition) should be taken as a part of the storage period t_2.

NOTE Provision is made for a separate specification of measurement temperature as, although the temperatures may be the same, the tolerance of the storage temperature may be considerably greater than that of the measurement temperature.

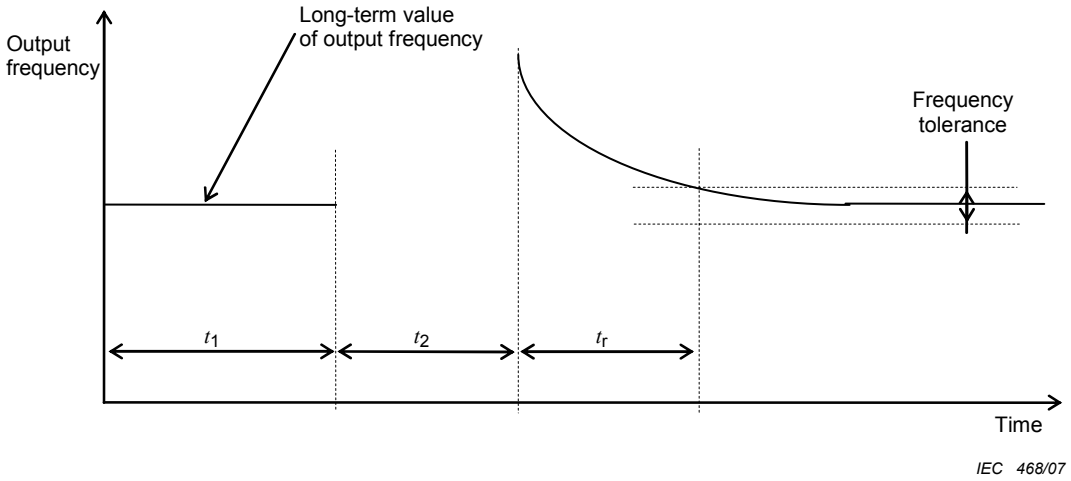


Figure 23 – Example of retrace characteristic

5.5.13 Oscillator output voltage (sinusoidal)

The oscillator shall be connected, as shown in Figure 24, to the specified supply voltage and load. It shall be allowed to stabilize for the specified period of time. The output voltage shall be measured across the load, and shall remain within the specified limits over the range of any frequency adjustment specified. Measurements shall be performed at the reference temperature, but may be carried out over the operating temperature range if required by the detail specification. Measurement shall be made with an r.f. voltmeter for r.m.s. voltages and an oscilloscope for peak-to-peak voltages.

In the case of quasi-sinusoidal waveforms, the measurement of output power shall always be performed by a direct-reading power meter or by means of a true r.m.s. reading voltmeter.

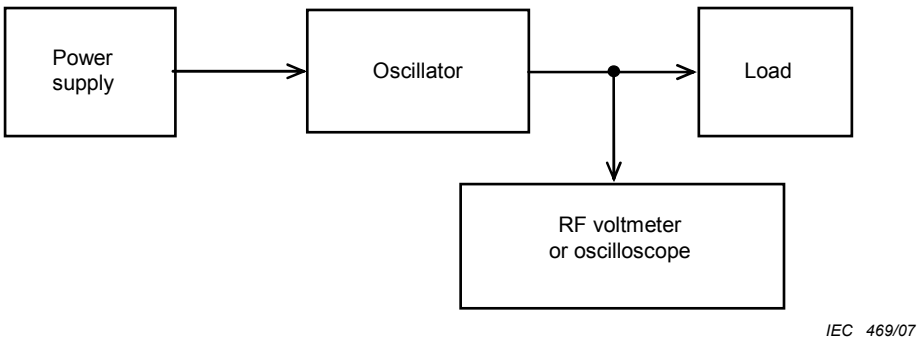


Figure 24 – Test circuit for the measurement of output voltage

5.5.14 Oscillator output voltage (pulse waveform)

The oscillator shall be connected, as shown in Figure 25, with the specified load (see Annex A for details of load circuits for logic drive).

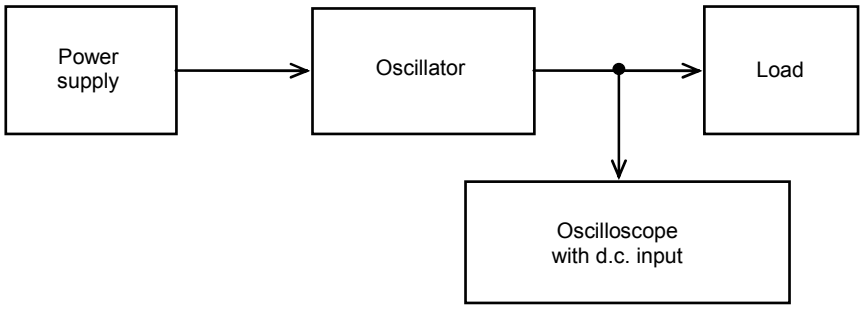


Figure 25 – Test circuit for the measurement of pulse outputs

The high and low level output voltages (see Figure 3) shall be measured on the oscilloscope, and shall be within the limits specified in the detail specification.

5.5.15 Oscillator output waveform (sinusoidal)

The oscillator shall be connected to the specified load, as shown in Figure 26.

The spectrum analyzer shall be adjusted to display a frequency range which embraces the appropriate harmonics of the oscillator. Typical quasi-sinusoidal waveforms are shown in Figure 27, and typical frequency spectra are shown in Figure 28.

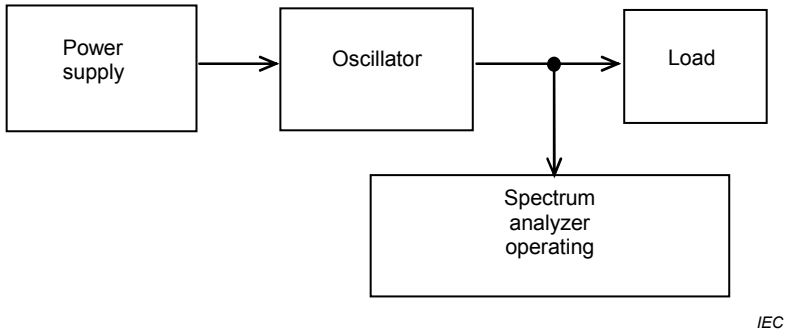


Figure 26 – Test circuit for harmonic distortion measurement

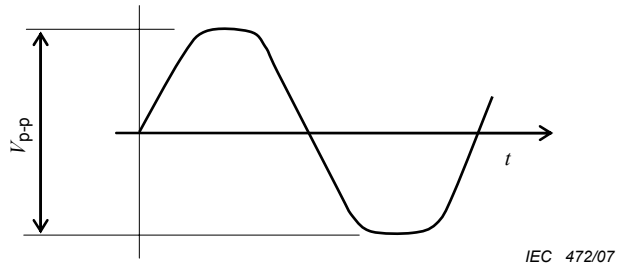


Figure 27a – Symmetrical

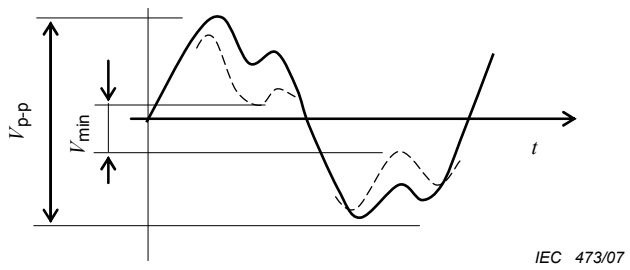


Figure 27b – Large odd harmonic content

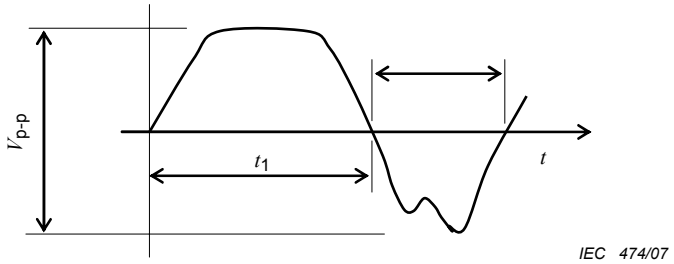


Figure 27c – Large even harmonic content

Figure 27 – Quasi-sinusoidal output waveforms

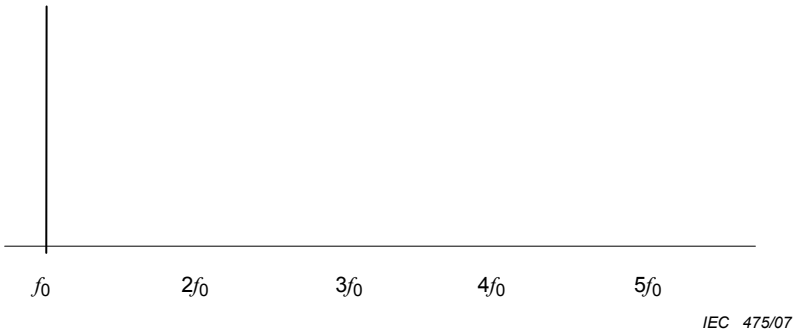


Figure 28a – Ideal spectrum

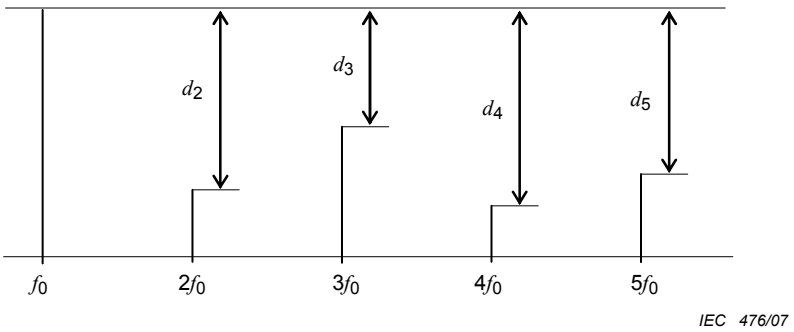


Figure 28b – Spectrum showing severe harmonic distortion

Figure 28 – Frequency spectrum for harmonic distortion

The spectra on the spectrum analyzer shall be measured, usually directly in decibels, as a power ratio with respect to the carrier power, expressed in decibels or, alternatively, the percentage distortion of the harmonic shall be calculated as follows:

$$D_x = \frac{100}{10^{d_x/20}}$$

where

D_x is the percentage of harmonic distortion;

d_x is the difference in level of fundamental and harmonic (in decibels) as measured on the spectrum analyzer;

x is the harmonic number.

When using this test method it shall be necessary to observe the following precautions:

– care shall be taken to ensure that the distortion is not produced in the input mixer of the spectrum analyzer;

– non-linear distortion (having the appearance of harmonic distortion) will be produced if the input mixer is over-loaded. This may be checked by placing an attenuator between the oscillator and the spectrum analyzer, and taking measurements at various power levels. The attenuator setting should not affect the percentage of harmonic distortion.

NOTE The total harmonic distortion may be obtained from a summation of the individual harmonically related responses.

$$D_{\text{total}} = 100\left[10^{\frac{d_2}{10}} + 10^{\frac{d_3}{10}} + \ldots + 10^{\frac{d_n}{10}}\right]^{-1/2}$$

5.5.16 Oscillator output waveform (pulse)

The oscillator shall be connected, as shown in Figure 25, and with the specified load (see Annex A for details of load circuits for logic drive).

5.5.16.1 Rise and decay times (see 3.2.33 and 3.2.34)

Measurements shall be made on both the rising and falling edges between the limits of the input voltage over which the operation of the particular logic family is guaranteed, for example, for TTL and CMOS logic families between V_{OH} min. and V_{OL} max. or at the 10 % and 90 % points with respect to the flat portion of the maximum amplitude level. Overshoot shall be disregarded in this measurement if its peak does not exceed the limits specified for the steady-state levels, or if the cause for the overshoot can be traced to inductances external to the oscillator and oscilloscope.

Where higher accuracies are required the following correction formula shall be used:

$$t_{\text{a}} = \sqrt{(t_{\text{i}})^2 - (t_{\text{s}})^2}$$

where

t_{i} is the measured rise or decay time;

t_{s} is the oscilloscope rise or decay time;

t_{a} is the actual time.

5.5.16.2 Pulse duration (see 3.2.32)

The pulse duration of the oscillator shall be measured with the oscilloscope when the rise and decay times are measured. Unless otherwise specified, measurements shall be made at the midpoint between V_{OL} max. and V_{OH} min. or at the 50 % level.

5.5.16.3 Symmetry (see 3.2.36)

When specified the symmetry of the waveform from the oscillator shall be determined when the rise and decay times are measured. Unless otherwise specified, measurements shall be made at the midpoint between V_{OL} max. and V_{OH} min. or at the 50 % level.

5.5.17 Oscillator output power (sinusoidal)

The test procedure shall be carried out as for 5.5.13, output voltage. The output power shall be calculated from the r.m.s. output voltage and the load impedance or, alternatively, it may be read directly from an appropriate power meter. In the case of quasi-sinusoidal waveforms, the measurement of output power shall always be performed by a direct-reading power meter or by means of a true r.m.s. reading voltmeter.

5.5.18 Oscillator output impedance (sinusoidal)

The oscillator shall be connected, as shown in Figure 24, except that the load shall be a precision (±1 % non-reactive) resistor R_L, equal to the specified load minus 10 %. The oscillator shall be energized and allowed to stabilize for the specified period of time after which the output voltage V_L shall be measured. The load shall then be replaced with a precision (±1 % non-reactive) resistor R_H, equal to the specified load plus 10 % and the output voltage V_H measured. The output impedance shall be calculated using the expression:

$$Z = \frac{R_L R_H (V_H - V_L)}{V_L R_H - V_H R_L}$$

NOTE This method is only valid if the output impedance of the oscillator is resistive, and it is not accurate when the output resistance is considerably lower than the load impedance.

5.5.19 Re-entrant isolation

The oscillator shall be connected to the test circuit, as shown in Figure 29. The ports between which the isolation is to be measured shall be shorted together. The level and frequency of the re-entrant signal, as specified, shall be set on the signal generator. Using the spectrum analyzer (or selective voltmeter), the output level of this signal shall be measured at the port to which the signal is not being applied (or at the specified port in the case of oscillators with multiple ports). The shorting link shall then be removed and the output level again measured.

The ratio of the two signals measured with and without the shorting link (usually expressed in decibels) is the re-entrant isolation between the appropriate ports at that frequency. This ratio shall be as stated in the detail specification.

When carrying out this test, the following precautions shall be observed:

– the loads presented to the oscillator are a combination of the output impedance of the signal generator, the input impedance of the spectrum analyzer (or selective voltmeter) and any externally applied loads;

– care shall be taken to prevent overloading of the spectrum analyzer (or selective voltmeter), as this will cause signal limiting and an apparent reduction in re-entrant isolation;

– if isolation is to be measured at a frequency which is a harmonic of the oscillator, then a pessimistic value of re-entrant isolation will be obtained. However, if the harmonic level is considerably lower than the isolation to be measured, a usable result can still be achieved. Where the harmonic content of the output signal is high, it is necessary to disable the oscillator (that is, to cause the device to cease oscillation while still remaining energized) before measurements can be made.

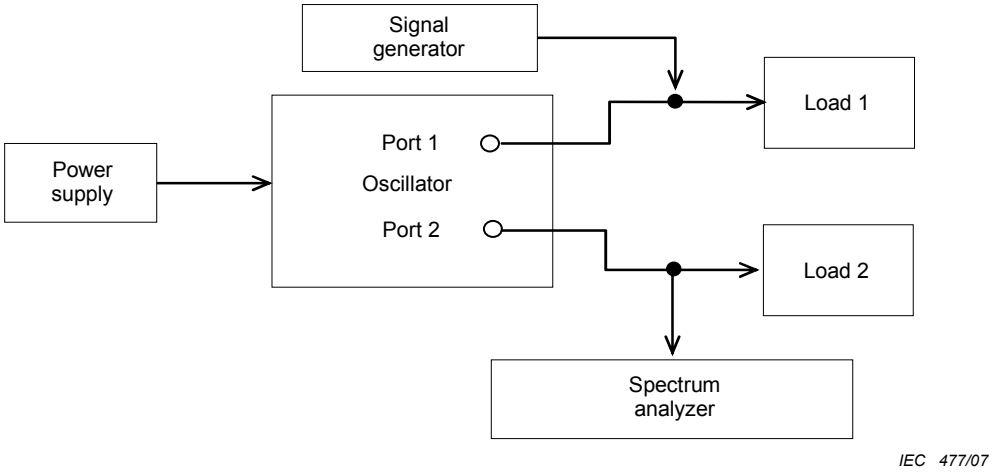


Figure 29 – Test circuit for the determination of isolation between output ports

5.5.20 Output suppression of gated oscillators

The oscillator shall be connected to the test circuit, as shown in Figure 30, and the tests carried out as follows.

The specified signal necessary to gate the ON output of the oscillator shall be applied, and the level of the output at its fundamental frequency and at any harmonic frequency or frequencies, as specified, shall be measured on the spectrum analyzer. The specified signal necessary to gate the OFF output of the oscillator shall then be applied and the new output level(s) measured.

The ratio of the ON and OFF output levels, usually expressed in decibels, is the output suppression at a particular frequency, and shall be as specified in the detail specification.

Care shall be taken to prevent overloading of the spectrum analyzer, as this will cause signal limiting and an apparent reduction in output suppression.

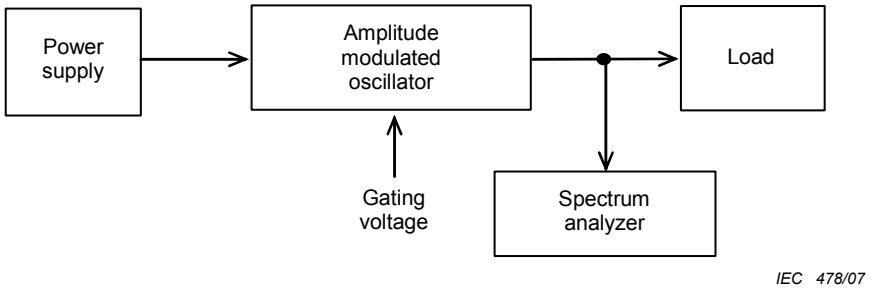


Figure 30 – Test circuit for measuring suppression of gated oscillators

5.5.21 Tri-state output characteristics

5.5.21.1 Tri-state disable mode output current

This test is used to determine the short-circuit output current drawn from an oscillator with a tri-state output when held in the disable mode.

The oscillator shall be connected as shown in Figure 31. With the enable/disable pin connected to the appropriate d.c. level via switch 1, that is to the specified supply voltage for oscillators designed for enable low, or to earth for those designed for enable high, the power to the oscillator shall be applied.

The enable/disable voltage levels shall be as specified in the detail specification. However, care shall be taken to ensure that the voltages applied to the enable/disable pin and the output pin cannot exceed the voltage applied to the oscillator.

The oscillator output is then switched, by switch 2, in turn between the supply voltage and earth, and the output current at each setting measured.

The maximum permissible output current in the disable mode, as specified in the detail specification, shall not be exceeded.

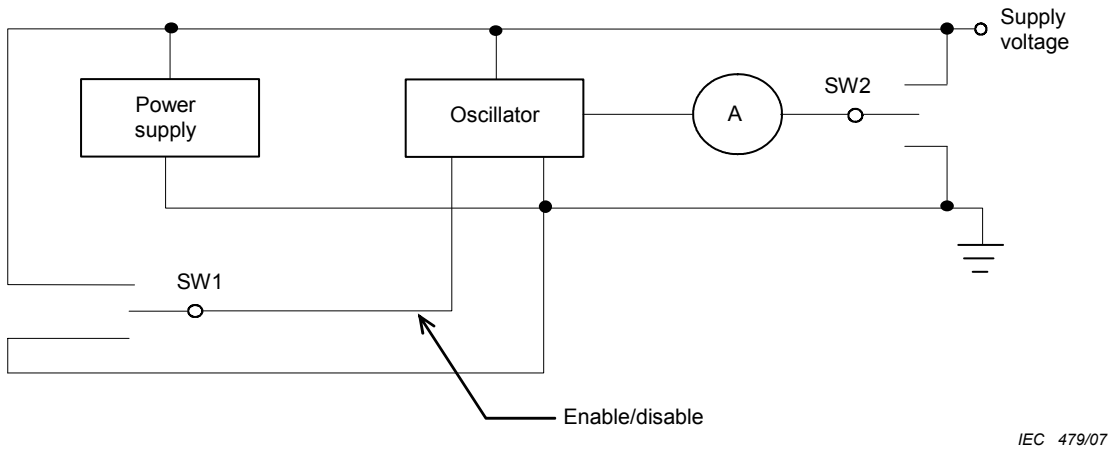


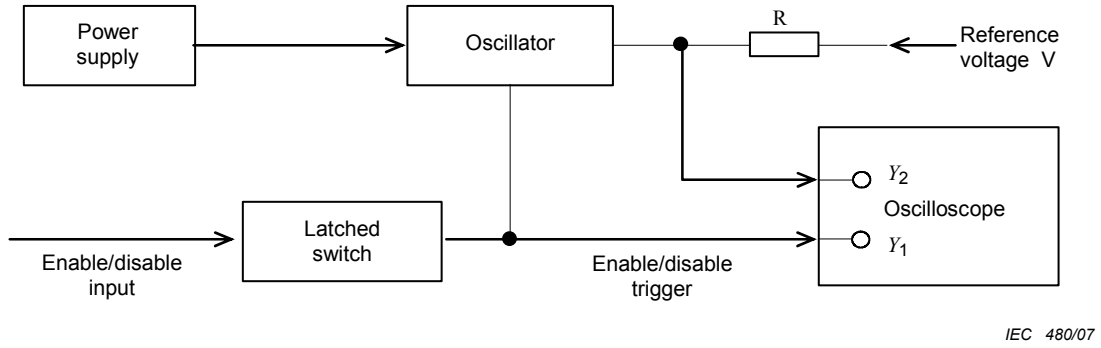
Figure 31 – Test circuit for tri-state disable mode output current

5.5.21.2 Output gating time

To measure the time taken for the oscillator output stage to switch between the enable and disable modes, the oscillator shall be connected as shown in Figure 32. The value of R shall be chosen so that the time constant formed by R and the oscilloscope input capacitance shall not affect the measurement accuracy.

The specified supply, reference, enable/disable voltages shall be applied to the oscillator, care being taken to ensure that the enable/disable voltages do not exceed the value of the supply voltage.

With an oscilloscope adjusted to trigger from either the enabling or disabling transition of the enable/disable input signal, as appropriate, and displaying the corresponding oscillator transition, together with the trigger transition, the gating time between the trigger transition and the time when the oscillator output stabilizes to the reference voltage shall be measured.



where

$V = \dfrac{(V_{OH} - V_{OL})}{2} + V_{OL}$ is the reference voltage;

V_{OL} is the oscillator low level output voltage;

V_{OH} is the oscillator high level output voltage.

Figure 32 – Test circuit for output gating time – tri-state

5.5.22 Amplitude modulation characteristics

5.5.22.1 Amplitude modulation index

Test A

This test procedure shall be used for a modulation index greater than 0,1 and less than 1,0. The oscillator shall be connected to the specified load, as shown in Figure 33, and the specified modulating signal applied. Measurements of x and y (see Figure 34) on the waveform shall be taken, and the modulation index (m) calculated from the expression:

$$m = \frac{y - x}{y + x}$$

The index obtained shall be as stated in the detail specification and the percentage modulation shall be 100 m %. This method of measurement shall not be used when *m* is less than 0,1 because of inherently low measurement accuracy.

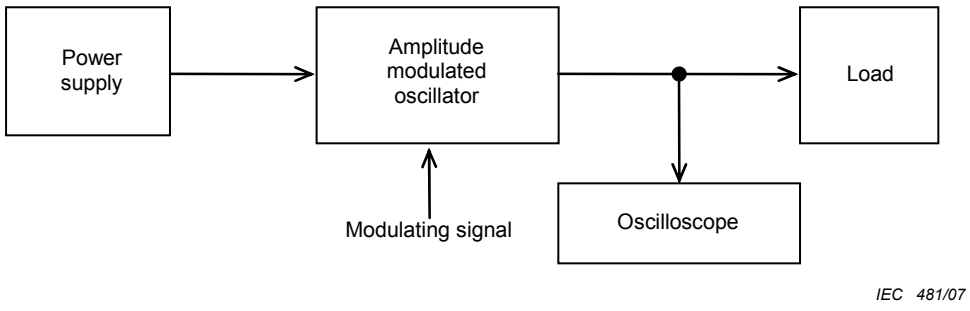
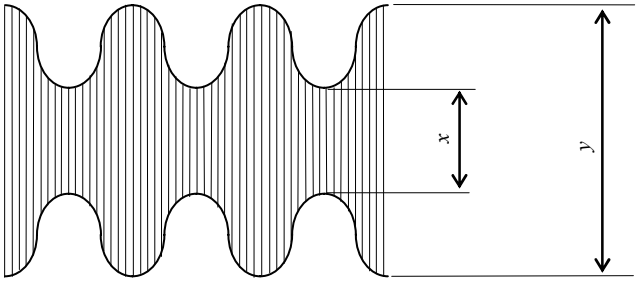


Figure 33 – Test circuit for modulation index measurement



IEC 482/07

Figure 34 – Modulation waveform for index calculation

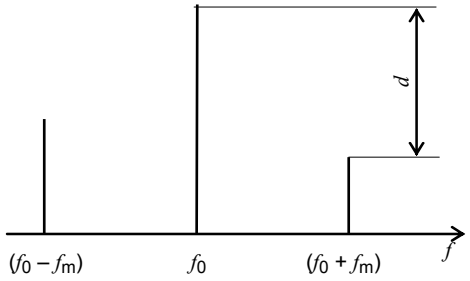
NOTE 1 The accuracy for this method is unaffected by the presence of frequency modulation.

NOTE 2 This method is valid for non-sinusoidal waveforms.

Test B

The test procedure shall be used for a modulation index less than 0,1.

The oscillator shall be connected to the specified load, as shown in Figure 33, except that the oscilloscope shall be replaced by a spectrum analyzer having an i.f. bandwidth sufficiently narrow to provide adequate discrimination between the oscillator output and its sideband signals. With the specified modulating signal applied to the oscillator, the spectrum analyzer shall be adjusted to present a display of the frequency spectrum in the region of the output frequency of the oscillator, using a logarithmic signal amplitude scale (see Figure 35).



IEC 483/07

f_0 is the oscillator output frequency;

f_m is the frequency of the modulating signal;

$f_0 - f_m$ is the lower sideband signal frequency;

$f_0 + f_m$ is the upper sideband signal frequency;

d is the difference between the oscillator output signal frequency (f_0) level and the level of either of the sideband signals, in decibels.

Figure 35 – Logarithmic signal amplitude scale

The modulation index (m) shall be calculated using the expression:

$$m = 10^{\frac{6-d}{20}} \quad (m < 0{,}1)$$

where d is the difference between the oscillator output signal frequency (f_0) level and the level of either of the sideband signals, in decibels.

The modulation index shall be as stated in the detail specification.

Care shall be taken to prevent overloading of the spectrum analyzer, causing signal limiting. This may be checked by placing an attenuator between the oscillator and the spectrum analyzer, and taking measurements at various power levels; the attenuator setting should not affect the value of *d* obtained.

NOTE 1 This method cannot readily be used if significant resultant frequency modulation is present (see 5.5.22.7), usually causing the two sideband signals to be unequal in amplitude. The effect of the resultant f.m. on the spectrum analyzer display may be reduced by choosing a high modulating signal frequency (frequency modulation index $\beta \propto \frac{1}{f_m}$).

NOTE 2 This method cannot readily be used if the modulation waveform is non-sinusoidal, whether because of harmonic content in the modulating signal or because of a.m. non-linear distortion (see 5.5.22.3).

5.5.22.2 Amplitude modulation sensitivity

The oscillator shall be connected to the specified road as shown in Figure 36. The signal generator providing a modulating signal at the specified frequency shall be connected to the external modulation terminal of the oscillator. Its output shall be set to the specified amplitude as measured by the oscilloscope or r.f. voltmeter. The modulation index of the output signal shall be measured as described in 5.5.22.1 (as appropriate).

In general, the amplitude modulation sensitivity is taken as the percentage modulation peak-to-peak voltage of the modulating signal and shall be as stated in the detail specification.

NOTE This method may be used to determine the immunity of an oscillator to power supply line ripple etc., by superimposing the modulating signal on the d.c. supply voltage.

5.5.22.3 Amplitude modulation distortion (non-linearity)

The oscillator shall be connected to the specified load as shown in Figure 36, except that the oscilloscope shall be replaced by a spectrum analyzer having an i.f. bandwidth sufficiently narrow to provide adequate discrimination between the oscillator output and its sideband signals.

A sinusoidal modulating signal at the specified frequency, and at a level such as to modulate the oscillator to the specified modulation index, shall be applied to the external modulation terminal of the oscillator; the spectrum analyzer shall be adjusted to present a display of the frequency spectrum in the region of the output frequency of the oscillator (see Figure 37).

The second, third, etc. harmonic distortion is usually expressed as d_2, d_3, etc. decibels, but may also be expressed as $\frac{100}{10^{\frac{d}{20}}}$ percentage distortion for each individual harmonic.

The distortion shall be within the limits stated in the detail specification.

When carrying out this test, the following precautions shall be observed:

– care shall be taken to prevent overloading of the spectrum analyzer, causing an apparent increase in modulation distortion. This may be checked by connecting an attenuator between the oscillator and the spectrum analyzer, and taking measurements at various power levels.

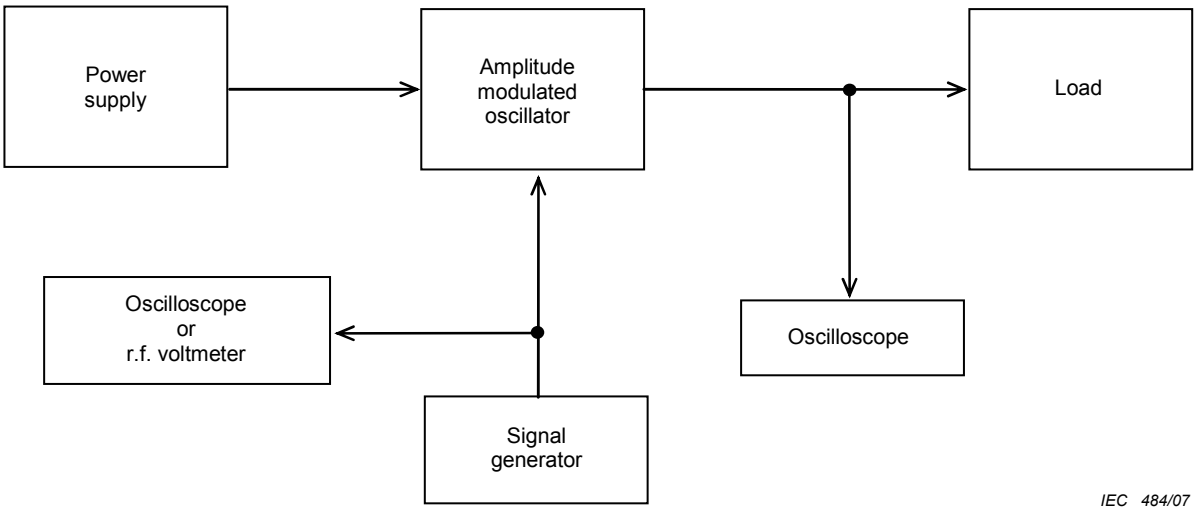
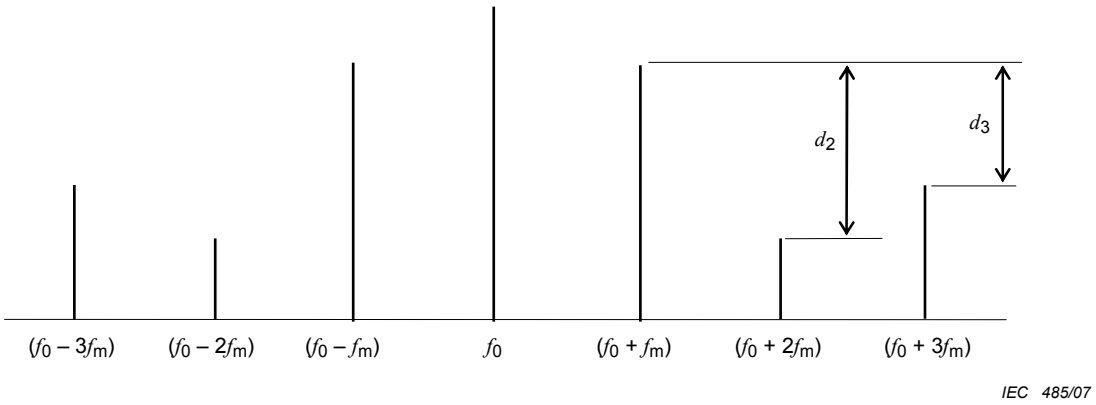


Figure 36 – Test circuit to determine amplitude modulation sensitivity



where

f_0 is the oscillator output frequency;

f_m is the frequency of modulating signal;

$(f_0 - f_m)$ is the lower sideband caused by the modulating signal;

$(f_0 - 2f_m)$ is the lower sideband caused by the second harmonic of the modulation signal;

$(f_0 - 3f_m)$ is the lower sideband caused by the third harmonic of the modulation signal.

Figure 37 – Frequency spectrum of amplitude modulation distortion

The attenuator setting should not affect the measurement of modulation distortion, that is the values of d_2, d_3, etc. If the harmonic content of the modulating signal is significant, the results obtained shall be corrected, or the modulating signal filtered so as to reduce its harmonic content.

NOTE Total modulation distortion may be assessed by detecting the output of the oscillator and measuring this signal with an appropriate distortion analyzer; this method measures the total sideband content of an amplitude modulated signal. The result may be obtained from the measurements made with a spectrum analyzer by summation of the sideband signals:

5.5.22.4 Amplitude modulation frequency response

The test procedure given in 5.5.22.2 with a sinusoidal modulating signal applied shall be used. The amplitude modulation sensitivity at a specified reference frequency shall be measured. Measurements shall then be taken at the other specified frequencies, giving the change in modulation sensitivity, usually expressed in decibels, which shall be within the limits stated in the detail specification.

$$\text{Total distortion} = \frac{100}{\sqrt{10^{\frac{d_2}{10}} + 10^{\frac{d_3}{10}} + \cdots}}$$

5.5.22.5 Pulse amplitude modulation

The oscillator shall be connected to the specified load and as shown in Figure 38.

A pulse generator, providing a modulating signal of specified waveform and repetition frequency, and which shall not be harmonically related to the oscillator frequency, shall be connected to the modulation input terminal of the oscillator.

Both this signal and the output waveform of the oscillator shall be displayed simultaneously on the oscilloscope, with the peak-to-peak amplitude of the output waveform adjusted to be twice that of the modulating signal, as shown in Figure 39.

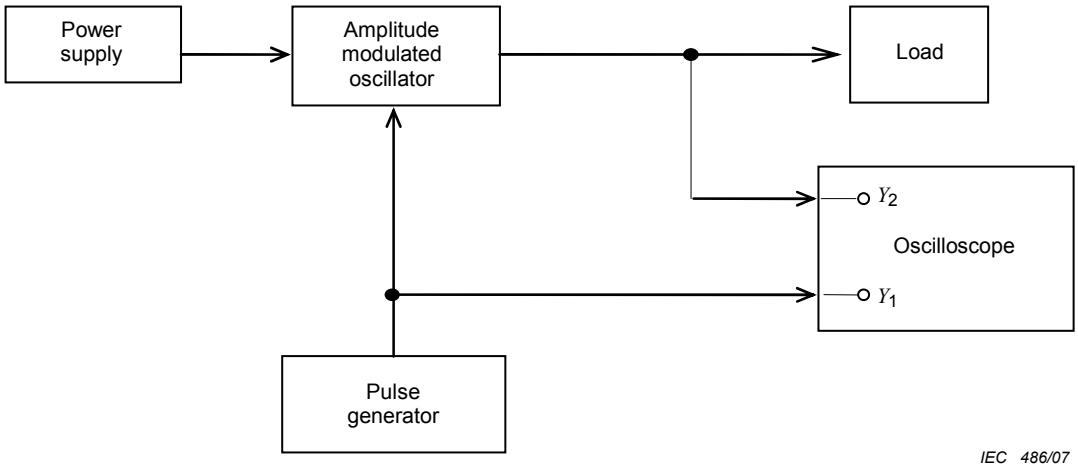


Figure 38 – Test circuit to determine pulse amplitude modulation

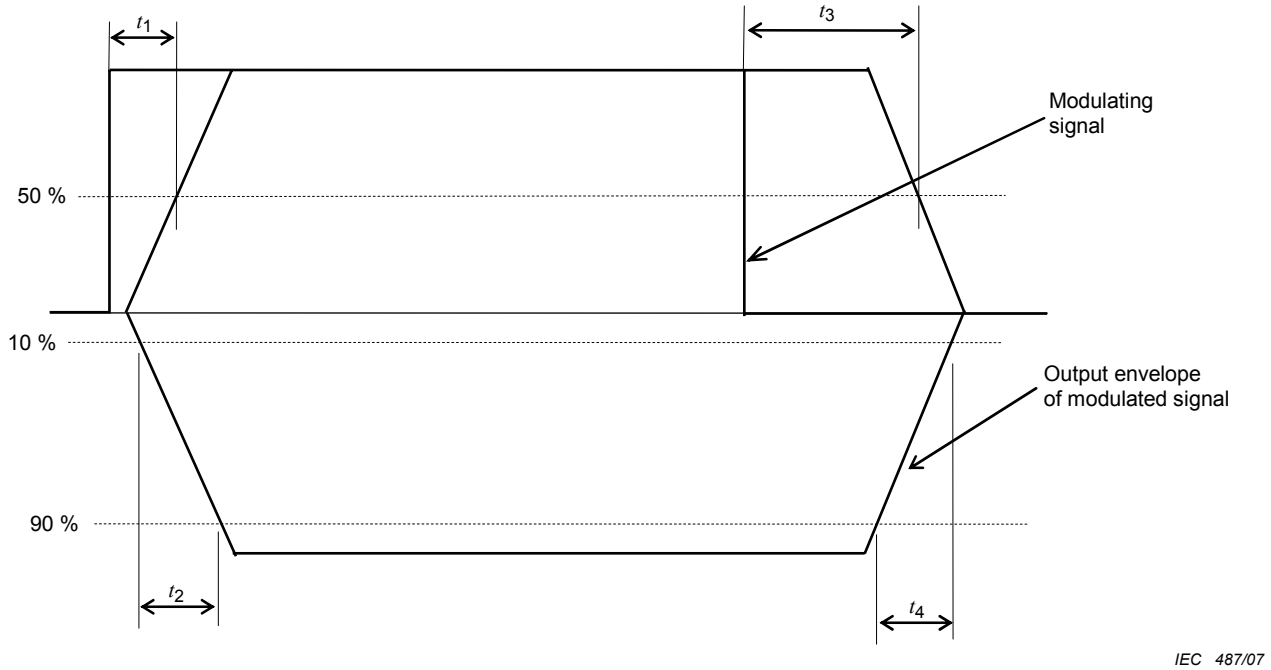


Figure 39 – Pulse modulation characteristic

The following parameters shall be determined and shall be as stated in the detail specification:

t_1 is the turn-on time, the time interval between the 50 % value of the modulating signal and the 50 % value of the output waveform, at the leading edge;

t_2 is the rise time, the time interval between the 10 % and 90 % values of the leading edge of the output waveform (assuming that the modulating signal rise time is negligible);

t_3 is the turn-off time, the time interval between the 50 % value of the modulating signal and the 50 % value of the output waveform, at the trailing edge;

t_4 is the decay time, the time interval between the 90 % and 10 % values of the trailing edge of the output waveform (assuming that the modulating signal fall time is negligible).

5.5.22.6 Amplitude modulation input impedance

A signal generator providing a modulating signal at the specified frequency shall be connected to the external modulation terminal of the oscillator and to a resistance box through a shielded transformer, as shown in Figure 40. The resistance box shall be non-reactive at the specified measurement frequency.

An oscilloscope (or suitable a.c. voltmeter) shall be connected so as to measure either the signal level across the resistance box (V_1) or the input level of the modulating signal to the oscillator (V_2).

The signal generator shall be adjusted so that the voltage level of the modulating signal at the input to the oscillator is at the specified level.

The modulation input impedance shall be calculated as:

$$Z = \frac{V_2}{V_1} R$$

and shall be as stated in the detail specification.

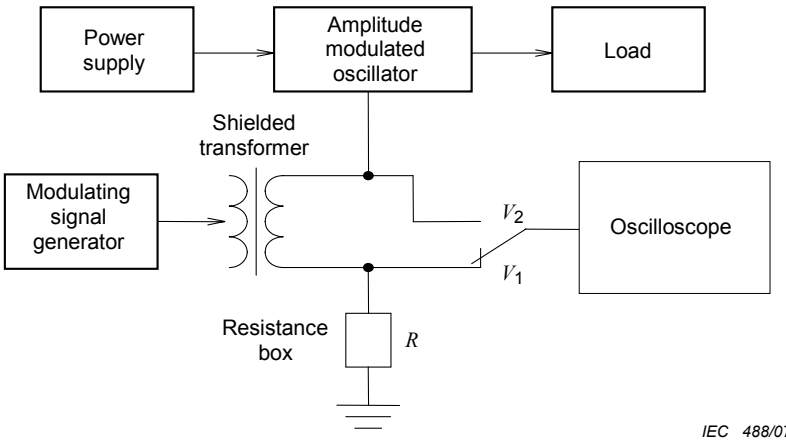


Figure 40 – Test circuit for the determination of modulation input impedance

5.5.22.7 Incidental frequency modulation on an amplitude modulation signal

The amplitude modulation shall be adjusted to the specified index, as described in 5.5.22.1. The resultant frequency modulation deviation shall then be measured, as described in 5.5.23.1. The magnitude of the deviation of the incidental frequency modulation of the amplitude modulated signal shall be within the limits stated in the detail specification. The limiting action of the frequency multiplier(s) will remove most of the amplitude modulation from the signal. However, care shall be taken to ensure that the residual a.m. is insufficient to affect the accuracy of the frequency modulation meter.

5.5.23 Frequency modulation characteristics

5.5.23.1 Frequency modulation deviation

- **Test A**

This test shall be used for a peak frequency deviation greater than 100 Hz.

The oscillator shall be connected to the specified load, as shown in Figure 41, with a modulating signal of specified frequency applied to its modulation input terminal.

The peak frequency deviation of the output signal shall be measured using an f.m. modulation (or deviation) meter, and shall be within the limits as stated in the detail specification.

When measuring very high frequency signals having a low peak frequency deviation, it may be necessary to use a local oscillator which is phase locked to a source having a low incidental f.m. content (for example a crystal oscillator), in order to reduce its f.m. noise deviation.

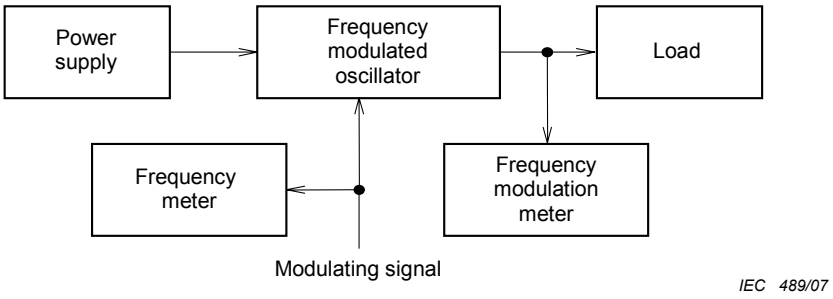


Figure 41 – Test circuit for the measurement of f.m. deviation

NOTE Frequency modulation index

$$\beta = \frac{\Delta f}{f_m}$$

where

Δf is the actual peak frequency deviation;

f_m is the frequency of the modulating signal.

- **Test B**

This test shall be used for a peak frequency deviation smaller than 100 Hz.

The oscillator shall be connected to the specified load, as shown in Figure 41, with the addition of a frequency multiplier before the f.m. modulation meter (see Note 2).

A modulating signal of specified frequency shall be applied to the modulation input terminal of the oscillator and the peak frequency of the output signal measured through the frequency multiplier using an f.m. modulation (or deviation) meter.

Hence

$$\Delta f = \frac{\Delta f_{\text{mult}}}{M}$$

where

Δf is the actual peak frequency deviation;

Δf_{mult} is the measured peak deviation;

M is multiplication factor.

The value obtained shall be within the limits stated in the detail specification.

When using this test method it shall be necessary to observe the following precautions:

– when measuring very high frequency signals having a low peak frequency deviation, it may be necessary to use a local oscillator which is phase locked to a source having a low incidental f.m. content (for example a crystal oscillator), in order to reduce its f.m. noise deviation;

– most oscillators are in some measure susceptible to ripple on the supply voltage; when measuring signals having a small frequency modulation index, great care shall be taken to ensure that supply voltage variations do not affect the measurement of peak frequency deviation.

NOTE 1 Frequency modulation index

$$\beta = \frac{\Delta f}{f_m}$$

where

Δf is the actual peak frequency deviation;

f_{m} is the frequency of the modulating signal.

NOTE 2 It may be necessary to use a mixer, before and/or after frequency multiplication, to down-convert the signal to bring it within the range of the frequency modulation meter.

5.5.23.2 Frequency modulation sensitivity

The oscillator shall be connected to the specified load, as shown in Figure 42. A signal generator providing a modulating signal at the specified frequency shall be connected to the modulation input terminal of the oscillator and its output set to the specified amplitude as measured by the oscilloscope or r.f. voltmeter. The specified modulation input level shall be such that the specified maximum permissible peak deviation of the oscillator is not exceeded. The peak frequency deviation of the output signal shall be measured as described in 5.5.23.1, tests A or B, as appropriate.

The frequency modulation sensitivity is defined as:

$$S_{\text{FM}} = \frac{\Delta f_{\text{p-p}}}{V_{\text{p-p}}}$$

where

$\Delta f_{\text{p-p}}$ is the peak-to-peak frequency deviation;

$V_{\text{p-p}}$ is the peak-to-peak modulating signal voltage.

Its value shall be within the limits stated in the detail specification.

NOTE This method may be used to determine the immunity of an oscillator to power supply line ripple, etc. by superimposing the modulating signal on the d.c. supply voltage.

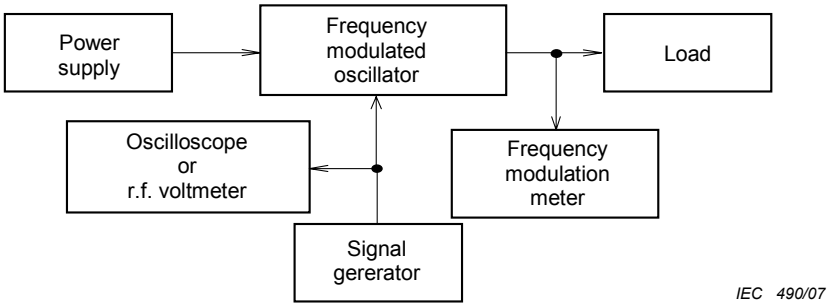


Figure 42 – Test circuit for the measurement of f.m. sensitivity

5.5.23.3 Frequency modulation distortion (non-linearity)

- **Test A (static test)**

The oscillator shall be connected to the specified load, as shown in Figure 43a, with a variable voltage d.c. power supply connected to the modulation input terminal. Measurements of the oscillator output frequency at the specified d.c. modulation voltages shall be made. A graph of output frequency against control voltage shall be plotted and hence the linearity of the frequency modulation deviation determined. This shall be within the limits stated in the detail specification.

- **Test B (dynamic test)**

The oscillator shall be connected to the specified load, as shown in Figure 43b.

A sinusoidal signal, at the specified frequency and at a voltage level such as to produce the specified modulation frequency deviation (see 5.5.23.1, tests A or B, as appropriate), shall be applied to the external modulation terminal of the oscillator.

The distortion of the output signal from the modulation detector (in modulation meter) shall be measured with a distortion meter. The distortion shall be within the limits stated in the detail specification.

When using this test method, it shall be necessary to observe the following precautions:

– if the harmonic content of the modulating signal is significant, the results obtained shall be corrected, or filtering may be added to the modulating signal to reduce the harmonic content;

– the distortion introduced by the detector of the modulation meter shall be low compared with that of the oscillator under test.

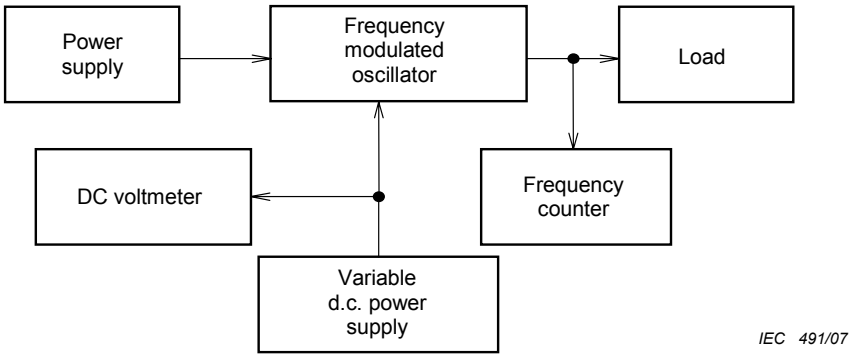


Figure 43a – Static test

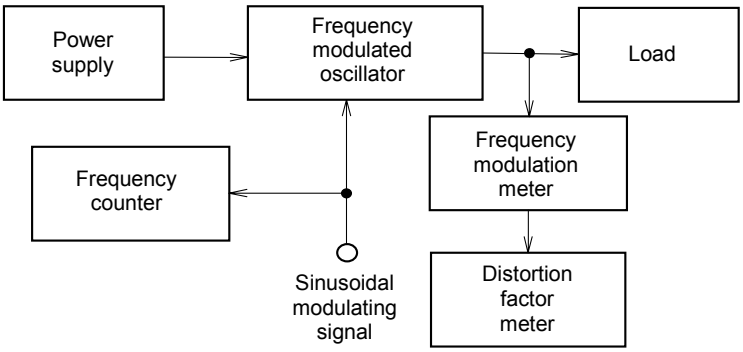


Figure 43b – Dynamic test

Figure 43 – Test circuit for the measurement of frequency modulation distortion

5.5.23.4 Frequency modulation frequency response

Using the procedures described in 5.5.23.2 with a sinusoidal modulating signal applied, the frequency modulation sensitivity at a specified reference frequency shall be measured. Measurements shall be made at other specified frequencies and the change in modulation sensitivity, usually expressed in decibels, determined. This change shall be within the limits stated in the detail specification.

5.5.23.5 Frequency modulation input impedance

This test shall be performed exactly as described in 5.5.22.6.

The resultant impedance shall be as specified in the detail specification.

5.5.24 Spurious response

The spurious response(s) shall be measured using the procedures exactly as described in 5.5.15, except that the measuring system shall be screened against any high level signals in the environment of the oscillator under test.

NOTE Spurious response(s) are, by definition, not harmonically related to the fundamental frequency and so it is difficult to differentiate between oscillator-generated spurious signals and those which may be picked up from the operating environment. This may be checked by removing the supply voltage from the oscillator.

5.5.25 Phase noise

5.5.25.1 General

Phase noise gives rise to a sideband distribution that consists of symmetrical pairs whose relative amplitude, compared to the carrier, is equal to half the peak phase deviation of that component in radians.

For the measurement of phase noise, synchronous signals are compared by means of a phase detector.

The output of the phase detector is the instantaneous voltage analog of the phase noise contribution. For the phase detector to be held to zero output, except for the phase noise contributions, it is essential that the oscillator under test (oscillator 2 in Figure 44) be kept in quadrature with the reference oscillator. This is achieved by using a d.c. amplifier to sense a zero phase detector output and hence drive the test oscillator to phase quadrature.

The output phase noise is monitored with a low frequency wave analyzer. The noise measured by the wave analyzer will be r.m.s. noise (it may be necessary to perform a conversion for average/r.m.s.) in both sidebands; this may be converted to a single-sideband phase noise by subtracting 6 dB.

Ideally, the reference oscillator (oscillator 1 in Figure 44) should have a very low noise contribution. It frequently occurs that both oscillators are of similar type; if this is so, it may be assumed that both oscillators have equal noise contributions, that is the signal-to-phase noise ratio will be degraded by 3 dB for similar oscillators. An appropriate allowance should be made when calculating the results.

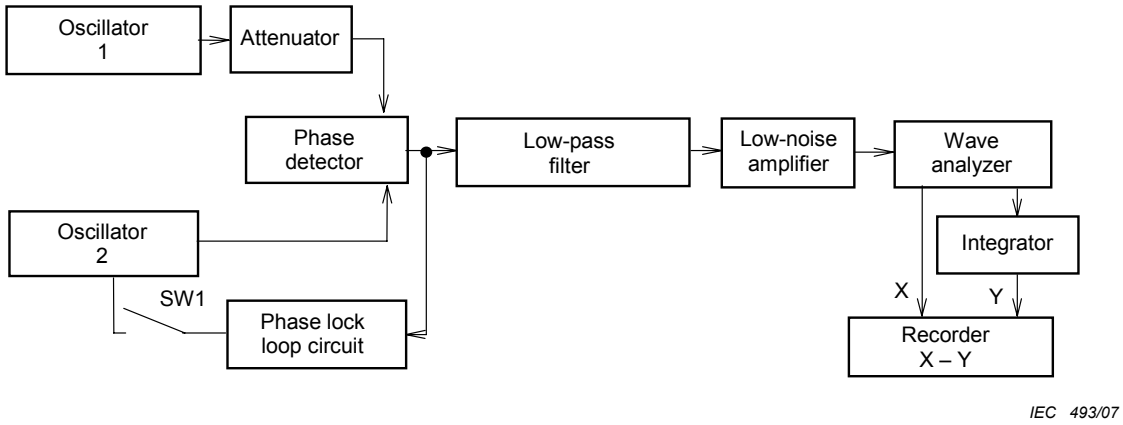


Figure 44 – Test circuit for the measurement of single-sideband phase noise

5.5.25.2 Procedure

The circuit shall be connected as shown in Figure 44. The feed-back loop from the phase detector shall be arranged such that oscillator 1 and oscillator 2 may be phase-locked in quadrature. The wave analyzer shall be set to the specified resolution bandwidth (frequency 1 Hz) and the integrator time constant to 1 s, unless otherwise stated in the detail specification.

Switch 1 shall be opened and a difference frequency will be established between oscillator 1 and oscillator 2. The wave analyzer shall be adjusted to the difference frequency and the scale of the X-Y recorder calibrated by means of the attenuator in the region –60 dB to –80 dB (high attenuation to prevent overloading of the low-noise amplifier).

Switch 1 shall then be closed. Oscillators 1 and 2 are phase locked in quadrature. The attenuator shall be set to –10 dB, unless otherwise stated in the detail specification, and the wave analyzer tracked in frequency over the specified range of offset frequencies over which the phase noise is to be measured.

5.5.25.3 Precautions

The response time of the frequency-control loop shall be very long compared with the period of the lowest sideband noise to be measured. For example, a 10 s response time (or 0,1 Hz cutoff frequency) would be indicated in order to measure phase noise sidebands at 1 Hz. Within the pass-band of the locking loop, the output signal is proportional to frequency noise; far outside the locking-loop pass-band, the output signal is proportional to phase noise, but in the transition region, the situation is somewhat complicated.

General precautions pertaining to the use of narrow-band tuned detectors shall be followed; in particular, the tuning rate (Hz/s) shall be small compared with the detector bandwidth (Hz) and the post-detector integration time shall be long compared with the inverse detector bandwidth.

For example, with a 10 Hz detector pass-band, the tuning (or slew) rate should be no greater than 1 Hz/s, and an integration time of at least 1 s should be used.

NOTE 1 The limit of resolution of this measurement system is determined by the minimum bandwidth of the wave analyzer. In this case, spectral components having a Fourier frequency lower than the analyzer bandwidth may not be measured.

NOTE 2 It is assumed that the noise contribution from the phase lock loop is small compared with the oscillator contribution. An alternative circuit arrangement is to manufacture the two oscillators with, for example, a 25 kHz frequency separation and then to examine (with the wave analyzer) the noise distribution around the 25 kHz output from a mixer, which should be used in place of the phase detector. In this arrangement, a band-pass filter (centered on the difference frequency) may be used instead of the low-pass filter. The disadvantage of this system is that it has an inherently lower stability and, in general, it will not be possible to use such low resolution bandwidths.

5.5.26 Phase noise – vibration

Using the procedure described in 5.5.25, the phase noise shall be measured with the oscillator operating whilst being subjected to vibration, as described in 5.6.7.2 (sinusoidal) or 5.6.7.4 (random).

The phase noise (vibration) shall be as specified in the detail specification.

5.5.27 Phase noise – acoustic

Using the procedure described in 5.5.25, the phase noise shall be measured with the oscillator operating whilst being subjected to acoustic noise, as required by 5.6.12.

5.5.28 Noise pedestal

5.5.28.1 General

The noise pedestal refers to the relative level of the oscillator frequency and the far-out noise level from the oscillator.

The graph in Figure 45 shows a typical spectrum as obtained from a crystal oscillator as displayed on a spectrum analyzer. Subclause 5.5.25 relates to the measurement of the noise contribution close to the oscillator frequency, while this test relates to the far-out contribution, usually expressed in decibels, below the oscillator frequency.

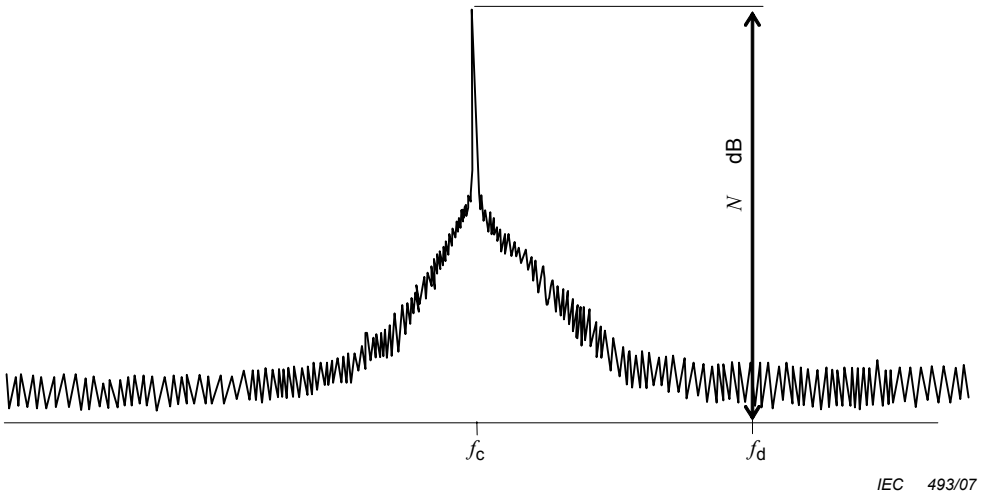


Figure 45 – Typical noise pedestal spectrum

5.5.28.2 Procedure

The oscillator shall be connected to the specified load and spectrum analyzer of specified resolution bandwidth, as shown in Figure 26.

From the output spectrum of the oscillator displayed on the spectrum analyzer, the noise pedestal shall be measured from the noise base line where it reaches asymptotic level, or at a specified frequency (f_d).

The measurement frequency (f_d) or separation from the oscillator frequency ($f_c - f_d$), if a specific frequency offset is relevant, shall be specified in the detail specification.

NOTE The mean level of the noise should be taken as the base line. This may be easily assessed if the spectrum analyzer incorporates a video filter which may be set for a long time constant, for example to a 10 Hz low-pass bandwidth.

5.5.28.3 Precautions

The following precautions shall be observed:

– care shall be taken to ensure that the noise contribution of the spectrum analyzer does not degrade the measurement of noise pedestal; this may be checked by changing the input attenuator setting of the spectrum analyzer. This should not change the value of N (see Figure 45), but rather reduce both the oscillator frequency level and the level of the far out noise. Spectrum analyzer noise will limit the applicability of this test to oscillators having a noise pedestal of about 70 dB to 90 dB (depending on the spectrum analyzer) or worse;

– should the noise pedestal be below the threshold level of the spectrum analyzer, the method described in 5.5.25 may be used to obtain an estimate of the noise pedestal; this is perfectly valid because, at low levels, the major contribution to the overall noise results from frequency or phase effects.

5.5.29 Spectral purity

5.5.29.1 General

Out-band noise refers to the relative level of the noise of frequencies far from the oscillator frequency, including discrete harmonic or spurious single frequency tones, to the level of the oscillator frequency.

Subclause 5.5.25 deals with the measurement of phase noise in the enhancement region near (within several bandwidths) the oscillator frequency, while this subclause refers to the flat additive noise region extending from several kilohertz to as much as several megahertz away from the oscillator frequency.

5.5.29.2 Procedure

The oscillator shall be connected as shown in Figure 26 and the spectrum analyzer adjusted to display the specified frequency range. The level of the noise pedestal may be determined directly from the spectrum analyzer display (in decibels), with appropriate correction for the analyzer bandwidth (that is 10 dB per decade bandwidth) in order to reduce the data to a 1 Hz basis.

5.5.29.3 Precautions

Care shall be taken to ensure that the noise contribution of the spectrum analyzer does not degrade the measurement. This may be checked by inserting a variable attenuator between the oscillator and the spectrum analyzer, and ensuring that both carrier and noise levels respond equally to attenuator setting.

In many cases, the signal-to-wideband noise ratio of crystal controlled oscillators will greatly exceed the dynamic range of available spectrum analyzers; in this case, it will be necessary to use a narrow-band elimination filter to attenuate the carrier to some known amount (that is 80 dB or 90 dB) in order to avoid saturation of the analyzer. Alternatively, some demodulation scheme may be used, such as the narrow-band phase locked loop of 5.5.25, to remove the carrier effectively.

NOTE Since the additive noise level from a crystal controlled oscillator may be comparable to the thermal noise generated by the load impedance itself, great care is recommended in the selection of any amplifier or signal processing equipment used in its measurement.

5.5.30 Incidental frequency modulation

The oscillator is connected as shown in Figure 46 and allowed to stabilize. The frequency discriminator shall provide a linear characteristic over a sufficiently wide band to prevent distortion of base-band spectral components in the specified frequency range. The incidental f.m. spectrum will be obtained directly on the X – Y recorder and shall be within the limits stated in the detail specification.

If it is specified to determine the total f.m. signal in a particular base-band region, a suitable band-pass filter and r.m.s. voltmeter may be substituted for the wave analyzer and X – Y recorder. In either case, it shall be necessary to determine the discriminator characteristic (volts/hertz deviation) in order to establish the calibration system.

It shall be necessary to take into consideration the following precaution.

The incidental f.m. of high-quality crystal controlled oscillators is commonly very small, especially at low base-band frequencies, requiring careful selection of low-noise discriminators and video amplifiers. Post-detection integration time and wave analyzer scanning rate shall be adjusted to be compatible with the wave analyzer bandwidth, in order to ensure accurate measurement of discrete f.m. tones, such as those produced by power supply ripple voltage, etc.

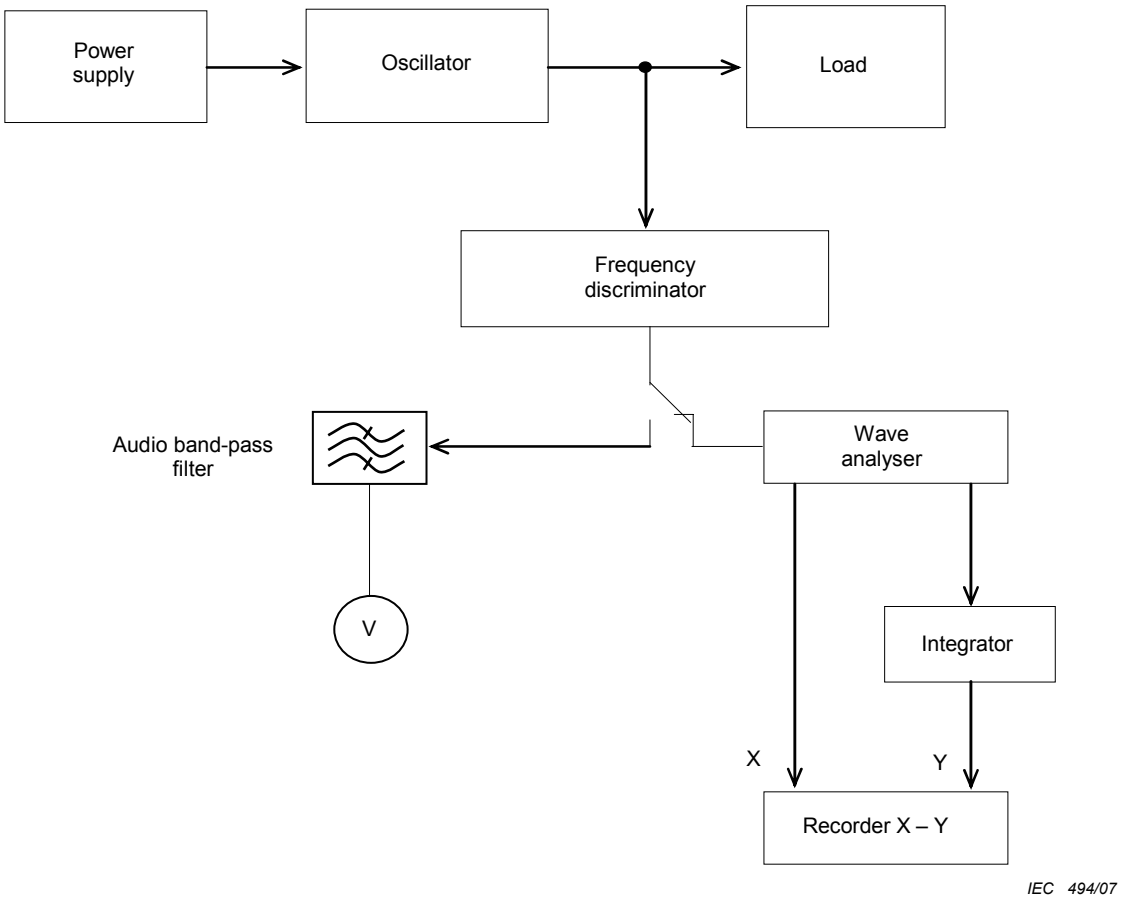


Figure 46 – Test circuit for the measurement of incidental frequency modulation

5.5.31 RMS fractional frequency fluctuations

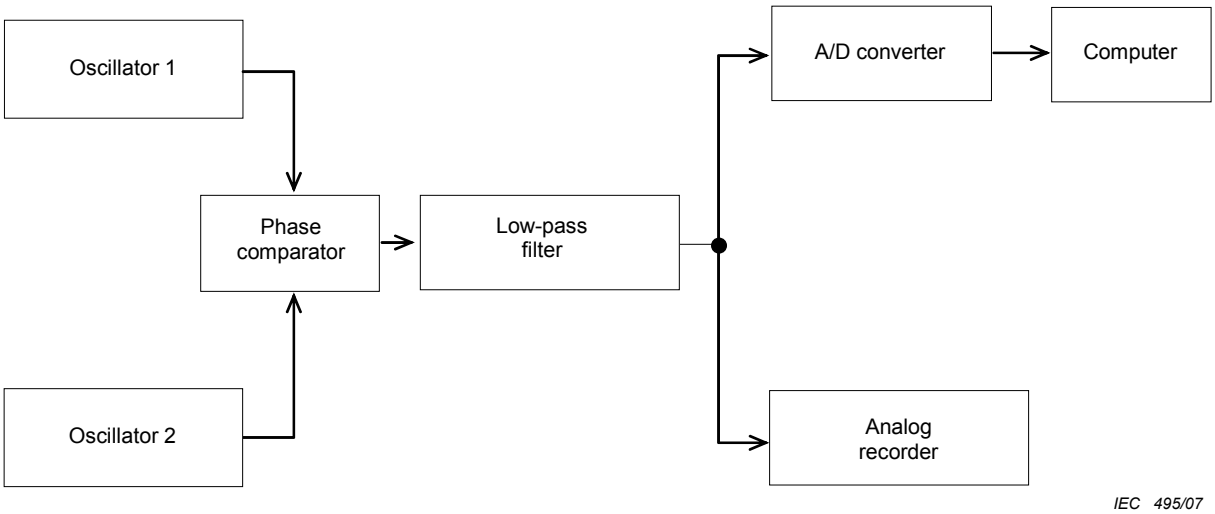
5.5.31.1 Procedure

In principle, time domain stability measurements are made with respect to a reference source having much better stability than the unit under test.

In general practice, however, comparisons are commonly made between two oscillators of similar design, and it is usually assumed that the probability densities and distribution functions of their random noise processes are nearly the same. Since the noise processes combine on a power basis, the fractional frequency fluctuations between the two similar oscillators shall be divided by $\sqrt{2}$ to arrive at an estimate of the fluctuation due to one of the oscillators alone. This is reflected in the formulae derived for each of the two methods.

- **Method 1** – Two oscillators having exactly the same mean frequency.

The two oscillators shall be connected as shown in Figure 47.



NOTE Phase comparators are often sensitive to both phase and amplitude deviations. In order to minimize sensitivity to amplitude, it is normal practice to use a double-balanced mixer as a quadrature detector.

Figure 47 – Test circuit for method 1

In the case of method 1, the phase comparator produces an analog signal which is directly proportional to the instantaneous phase fluctuations between the two oscillator signals (for Fourier frequencies below the cut-off of the low-pass filter). This signal may be examined by analog methods (such as continuous strip-chart recorder, r.m.s. voltmeter or spectrum analyzer), or it can be examined by time domain methods using a sampling type A/D converter with a controlled sample averageing time τ, and the repetitive sampled measurements stored for analysis by a computer. Using this method, there is no dead time introduced in the measurement system, and the r.m.s. fractional frequency fluctuation is:

$$\frac{\Delta F}{F_0}(\tau)_{\text{rms}} = \frac{1}{4\pi F_0 \tau}\left[\frac{1}{(M-1)}\sum_{k=1}^{M-1}\left[\left[\varphi(t_k+2\tau)-\varphi(t_k+\tau)\right]-\left[\varphi(t_k+\tau)-\varphi t_k\right]\right]^2\right]^{1/2}$$

where

M is the number of repetitive measurements;

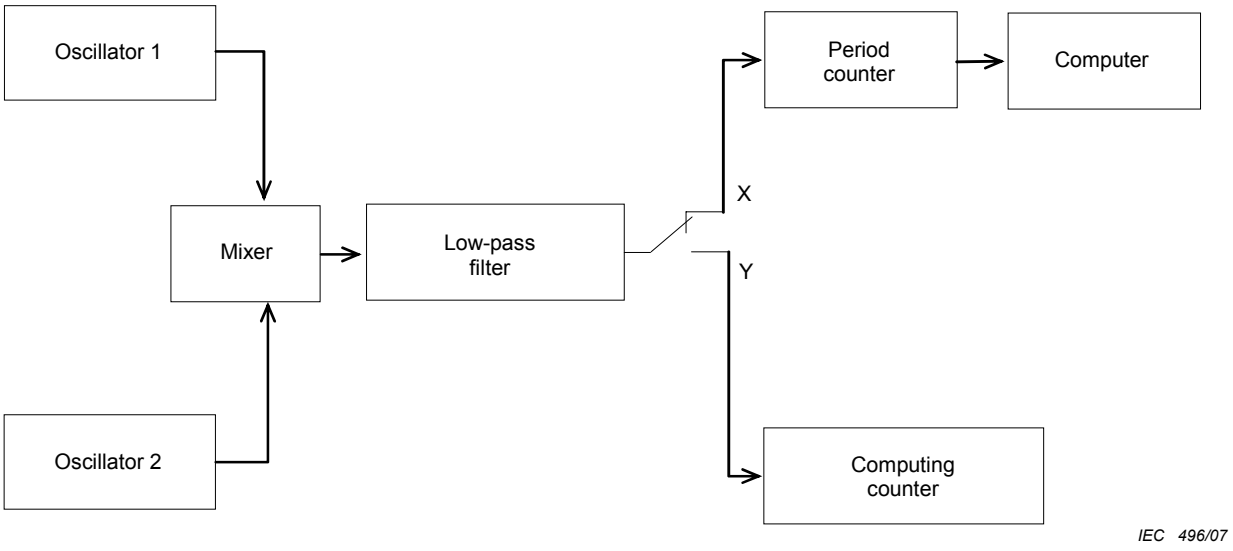
τ is the sample averageing time.

NOTE If, in fact, the reference oscillator used has much better stability than the unit under test, then all of the frequency fluctuations can be attributed to the unit under test and the equation above should be multiplied by $\sqrt{2}$.

- **Method 2** – Two oscillators having slightly different frequencies.

The two oscillators shall be connected as shown in Figure 48.

In this case, the two oscillators being compared are usually made to be essentially identical, except that one of the controlling crystals is adjusted to a slightly different frequency. Therefore, the output of the mixer will have a sinusoidal waveform whose frequency is the difference between the two oscillator frequencies. This is commonly chosen to be somewhere in the range from 100 Hz to 10 kHz. It is assumed that the small difference in crystal unit adjustment will not significantly influence the random noise characteristics of the oscillator.



NOTE Position X or Y may be used to obtain the Allan variance and deviation. X allows determination of the standard deviation as well.

Figure 48 – Test circuit for method 2

The specified number of measurements M of the period of the beat frequency is made, using the specified averageing time τ (τ should be an integral number of periods of the beat frequency). The interval between successive measurements T will usually be at least one period of the beat frequency longer than the sample averageing time τ and may be two or more periods greater depending upon the beat frequency and the recycling time of the counter-data acquisition system. The fractional frequency fluctuation is:

$$\frac{\Delta F}{F_0}(\tau)_{\text{rms}} = \frac{1}{\sqrt{B_2(r,\mu)}} \times \frac{1}{2F_0}\left[\frac{1}{(M-1)}\sum_{k=1}^{M-1}(F_{k+1}-F_k)^2\right]^{1/2}$$

where

τ is the sample averageing time;

$B_2(r,\mu)$ is the correction factor for dead time;

T is the sampling period;

$\gamma = \dfrac{T}{\tau}$ is the ratio of sampling period to sample averageing time;

F_k, F_{k+1} are the successive measurements of the beat frequency averaged for sample time τ, as described above.

NOTE As for method 1 above, if the reference oscillator has much better stability than the unit under test, all of the frequency fluctuations can be attributed to the unit under test and the value above should be multiplied by $\sqrt{2}$.

5.5.31.2 Modification of methods 1 and 2

Use of a crystal filter

In special instances (for example if only very short averageing times are of interest), a narrow-band crystal filter may be inserted between the reference oscillator and the mixer or phase comparator, as shown in Figure 49. For averageing times τ much less than the reciprocal of the filter bandwidth, this modification can remove the noise sidebands from the reference signal, so that only the frequency fluctuations of the unit under test will be observed. To be effective, however, the crystal filter itself shall be free from excess noise, protected from mechanical disturbances and maintained at constant temperature.

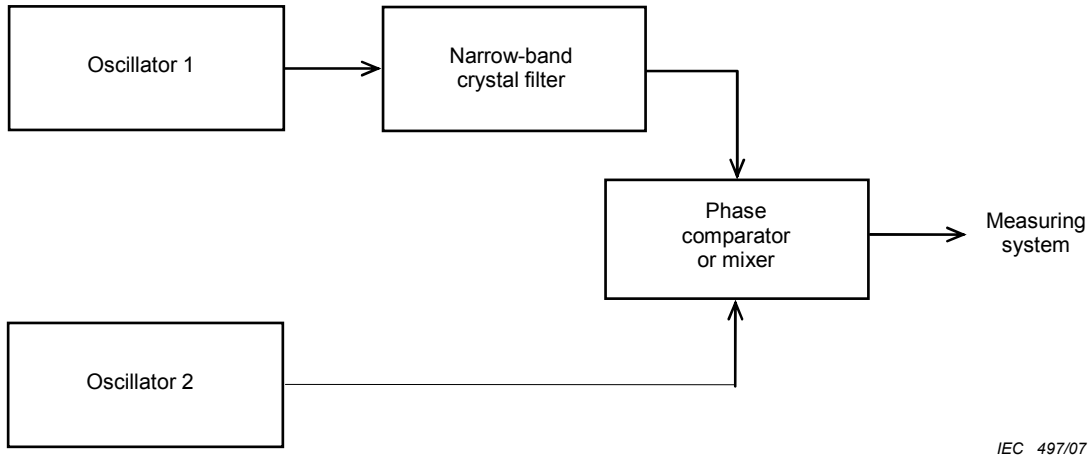


Figure 49 – Circuit modifications for methods 1 and 2

5.5.31.3 Precautions

The short-term frequency stability of an oscillator is a very sensitive measure of the spectral purity and, as such, should be performed under controlled conditions. For high orders of stability, screened enclosures should be used, the recording apparatus being outside the enclosure.

5.5.31.4 Results

The short-term frequency stability of an oscillator shall be given in graphical form. An example is given in Figure 50.

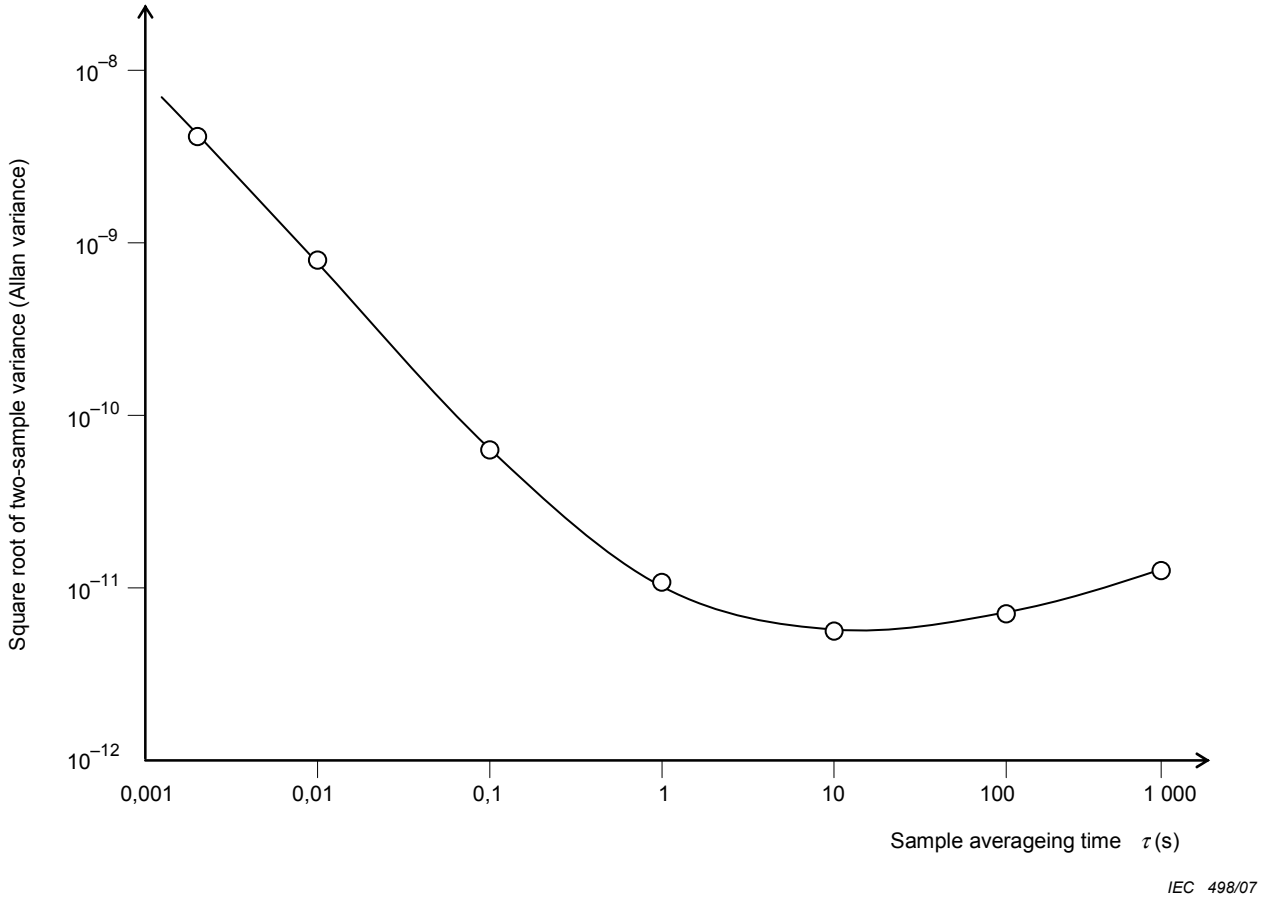
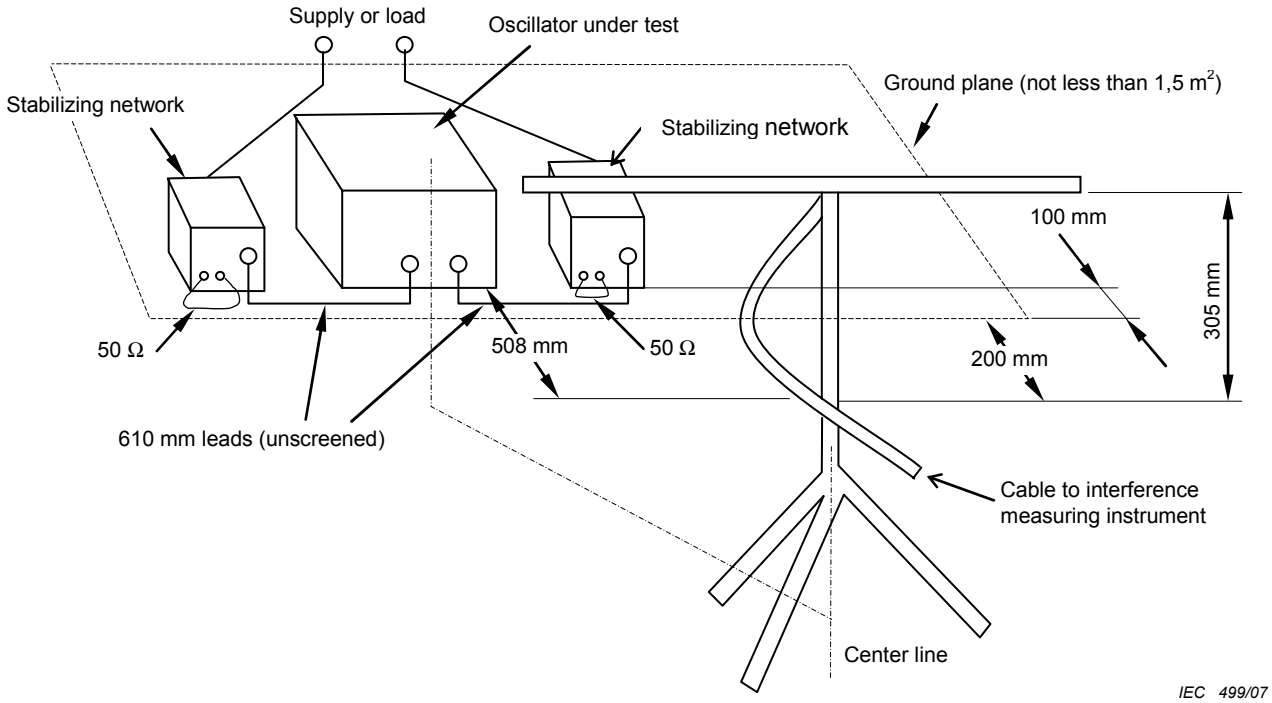


Figure 50 – Time-domain short-term frequency stability of a typical 5 MHz precision oscillator

5.5.32 Electromagnetic interference (radiated)

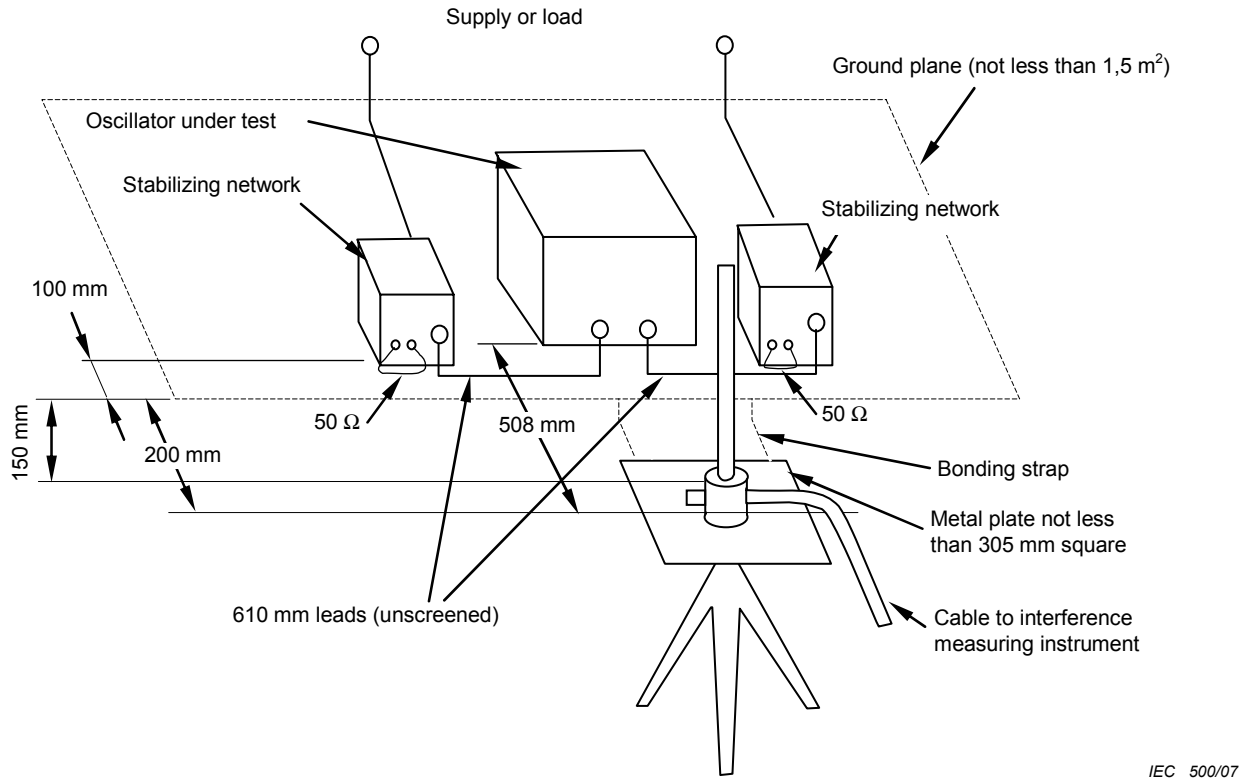
This method shall be used, unless otherwise specified by national regulations.

The test arrangements shall be as described in Figures 51a and 51b.



NOTE Stabilizing network to be bonded to the ground plane.

Figure 51a – Typical arrangement for radiated interference tests, 30 MHz and above



NOTE Stabilizing network to be bonded to the ground plane.

Figure 51b – Typical arrangement for radiated interference tests, below 30 MHz

Figure 51 – Radiated interference tests

5.5.32.1 Test conditions

For tests of radiated interference, it is essential that the test should be made in a screened room having dimensions not less than 2,4 m high, 2,1 m wide, and 4,6 m long.

Ideally, the tests for conducted interference should be made in a screened room having adequate filters in all incoming supply lines. If this is impracticable, precautions should be taken to ensure that the results are not affected by noise voltages and fields other than those due to the oscillator under test. This will involve the use of additional filters in the supply and/or load circuits.

The oscillator under test should be mounted on the ground plane. The ground plane shall be bonded to the screened room at points not more than 0,9 m apart, and at the ends of the ground plane.

The leads from the oscillator under test to the line impedance stabilizing network shall be 610 mm in length, and shall be screened or unscreened, as shown in the appropriate figure. The stabilizing networks in the lines not being measured shall be terminated by 50 Ω non-reactive resistors.

The impedance characteristics of the stabilizing network shall be within the limits of Figure 52. One practical method of attaining this impedance is shown in Figure 53.

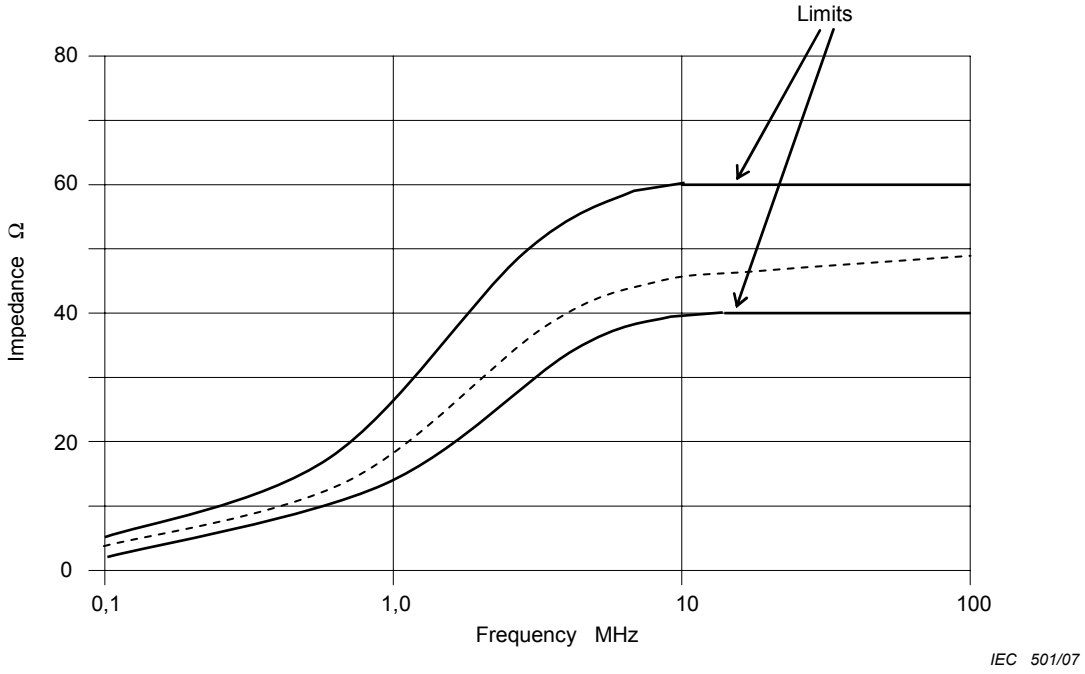
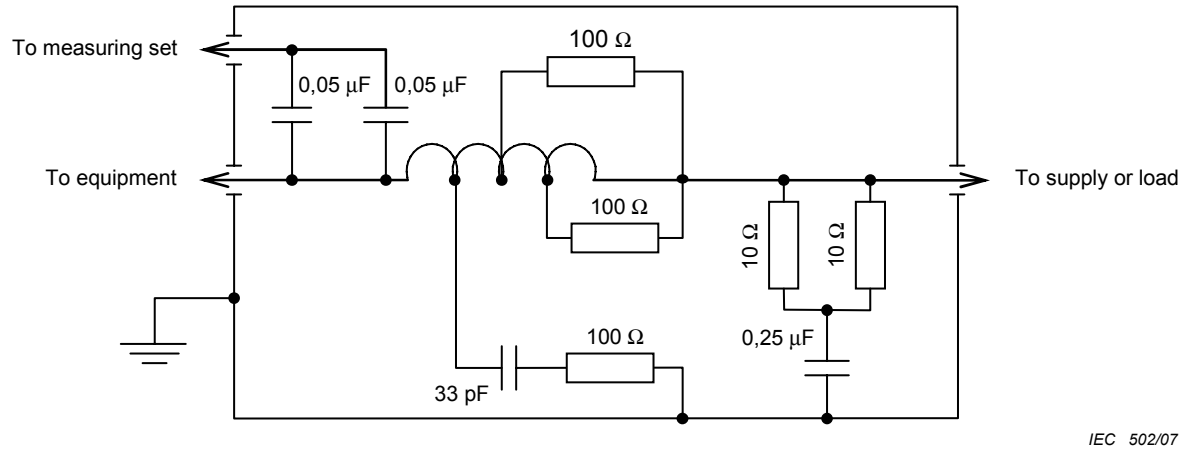


Figure 52 – Characteristics of line impedance of stabilizing network



Coil characteristics:

5 µH, 10 turns, 5,89 mm (0,232 in) 4 SWG[2)] wound on 51,0 mm (2 in) diameter former.

Figure 53 – Circuit diagram of line impedance of stabilizing network

5.5.32.2 Procedure

The oscillator shall be set up in a screened room and with a measuring system as described above.

The measurements shall be made under the load conditions producing the worst operating conditions from the point of view of radio interference.

A vertical rod aerial 1 016 mm ± 25 mm long shall be used at frequencies below 30 MHz. It shall be located at the point where maximum interference is obtained when it is moved along a line parallel to the front edge of the ground plane. At 30 MHz and above, a horizontal dipole aerial shall be used; over the frequency range 30 MHz to 50 MHz, a 50 MHz dipole shall be used and above 50 MHz a resonant dipole shall be used. It shall be placed parallel to the front edge of the ground plane. Its height shall be 305 mm ± 25 mm above the level of the ground plane and its center shall be adjacent to the geometrical center of the unit under test. The rod or the dipole aerial shall be located 508 mm from the nearest point on the surface of the oscillator under test. When the length of the dipole is less than of the test layout, it shall be moved parallel to the edge of the ground plane to the point of maximum response.

5.5.32.3 Measuring sets

Measuring sets having facilities for the measurement of peak values and having bandwidths within the limits shown in Table 1 are preferred for measurements specified in this standard. Measuring sets having other bandwidths are acceptable, provide suitable correlation factors are used.

Table 1 – Measuring sets bandwidth

Frequency range MHz	**Bandwidths limits,** at –6dB
0,05 to 0,15	200 Hz ± 100 Hz
0,15 to 30	9 kHz ± 1 kHz
30 to 300	150 kHz ± 50 kHz
300 to 1 000	150 kHz ± 50 kHz

2) British standard wire gauge.

All voltages measured shall be referred to 50 Ω.

If the input impedance of the measuring set differs from this value, a suitable matching network shall be used and the appropriate correction factor applied.

When a measuring set has a quasi-peak voltmeter only, it will need to be modified to read peak voltages.

As the impulse bandwidth of measuring sets normally differs from 1 kHz, and appropriate correction factor shall be applied on a linear basis.

In all cases, the measuring set shall be tuned for a maximum response to the interfering signal.

5.5.33 Phase jitter

Three basic methods are described:

a) measurement in the time domain by use of a digital real-time or sampling oscilloscope;

b) measurement in the data domain (BER test set);

c) measurement in the frequency domain:

   1) using a phase noise test set, or

   2) jitter and wander test set (see 5.5.34).

Method c)1) using a phase noise test set is the recommended measurement method because it allows sufficient accuracy for arbitrary oscillator output frequencies.

- In the measurement of phase jitter and wonder of an oscillator circuits, attention should be paid to relative measurement reproducibility.
- A user and a manufacturer should deepen understanding through discussion about relative measurement reproducibility.
- Measurement equipment (including software program) should be made clear between a manufacturer and a user through a contract.
- When phase jitter and wonder is calculated from phase noise, the range of frequency deviation should be made clear between a user and a manufacturer through a contract.

5.5.33.1 Measurement in the time domain

Digital real-time or sampling oscilloscopes with wide bandwidth, fast sampling rates, and large data memories are commercially available, in some cases with special jitter evaluation software.

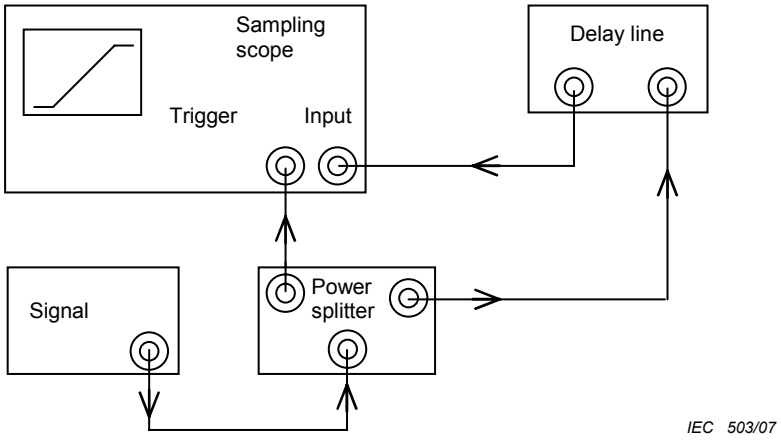


Figure 54 – Phase jitter measurement with sampling oscilloscope

The time variation of the edges of the clock signal relative to the trigger edge is displayed and stored over a large number (typically thousands) of cycles. Instrument software allows the determination of the peak-to-peak jitter value and a statistical evaluation of its distribution. The sampling oscilloscope method does not allow an accurate evaluation of the spectral content of the jitter. Also, jitter larger than one UI cannot be distinguished.

The measured jitter ($Jitter_{\text{meas}}$) value is worse than the jitter of the device under test ($Jitter_{\text{DUT}}$) due to the internal jitter of the instrument's clock ($Jitter_{\text{int}}$).

$$Jitter_{\text{DUT}} = \sqrt{(Jitter_{\text{meas}})^2 - (Jitter_{\text{int}})^2}$$

High stability/low noise crystal oscillators exhibit a significantly lower jitter than the instrument's clock jitter and trigger stability. Therefore, this technology is currently not suitable for accurate jitter measurement of such crystal oscillators.

5.5.33.2 Measurement in the data domain

BER test sets are used for measuring bit-error rate (BER) to characterise the overall system performance of a communication subsystem. It is difficult to deduct the contribution of the crystal oscillator jitter to the system BER. This method also does not yield quantitative jitter performance values for the crystal oscillator.

5.5.33.3 Measurement in the frequency domain

5.5.33.3.1 Phase noise test set

Jitter can be tested in the frequency domain using the well-established phase noise test method with a phase locked loop as described in 5.5.25.

For given SDH/SONET applications the Fourier frequency range ($f_{\text{min}} \ldots f_{\text{max}}$) may be selected as described in 3.2.39. If not specified in the relevant data sheet, the recommended Fourier frequency range is as given by f_3 to f_4 in Table 2.

Table 2 – Fourier frequency range for phase noise test

Oscillator output frequency	$f_0 = f_{\text{min}}$	f_3	$f_4 = f_{\text{max}}$
1 MHz to <10 MHz	10 Hz	10 kHz	100 kHz
10 MHz to <50 MHz	20 Hz	20 kHz	500 kHz
50 MHz to <200 MHz	100 Hz	50 kHz	1,5 MHz
200 MHz to <1 000 MHz	1,0 kHz	200 kHz	5,0 MHz
1000 MHz to <5 000 MHz	5,0 kHz	500 kHz	15 MHz
≥5 000 MHz	20 kHz	2 MHz	80 MHz

From Table 2 it can be seen that the most stringent requirement applies over the range f_3 to f_4.

Jitter performance over a frequency-band other than f_3 to f_4 may also be defined.

To compute the phase jitter, the phase noise data $L(f)$ have to be integrated in the considered frequency ranges and evaluated as follows:

Compute the spectral density of phase fluctuations $S_\varphi(f)$ from the single-sideband phase noise plot $10\log_{10} L(f)$

$$S_\varphi(f) = 2\,L(f)$$

Integrate $S\varphi(f)$ over the specified Fourier frequency range f_{min} to f_{max} to get the mean squared phase jitter in that bandwidth:

$$\left\langle \Delta\varphi^2(f) \right\rangle = \int_{f_{min}}^{f_{max}} S_\varphi(f)df$$

The mean square phase jitter can be approximated by stepwise integration over the specified Fourier frequency range f_{min} to f_{max} segmented by n, for example:

$$\left\langle \Delta\varphi^2(f) \right\rangle \approx \sum S_\varphi(f_i)\Delta f_i$$

where

$\Delta f_i = f_{i+1} - f_i \quad (i = 1 \ldots n-1)$

with

$f_1 = f_{min}$ and $f_n = f_{max}$

The square root of $\Delta\varphi(f)$ of the integral is the effective or r.m.s. phase jitter in radians. It can be converted into degrees, fractions of Unit Interval (UI), or time (in seconds) by multiplication with the following factor k:

	Degree[°]	Unit interval[UI]	Time [s]
k =	360/2π	1/(2π)	$1/(2\pi f_c)$

For random jitter, the peak-to-peak value is assumed to be 7 times the value computed above (see 3.2.39).

Accuracy:

A 1 dB error of the phase noise data 10 $\log_{10} L(f)$ over the full Fourier frequency range causes a jitter inaccuracy of approximately 10 %.

5.5.33.3.2 Communication analyzer

Commercially available communication analyzer may be used to measure jitter and wander of clock sources with the method described in ITU-T O.172. The working principle is similar to the phase noise measurement technique using the quadrature method. Softwares supplied with the test sets deliver directly all characteristic values for jitter and wander in numeric and graphical presentation.

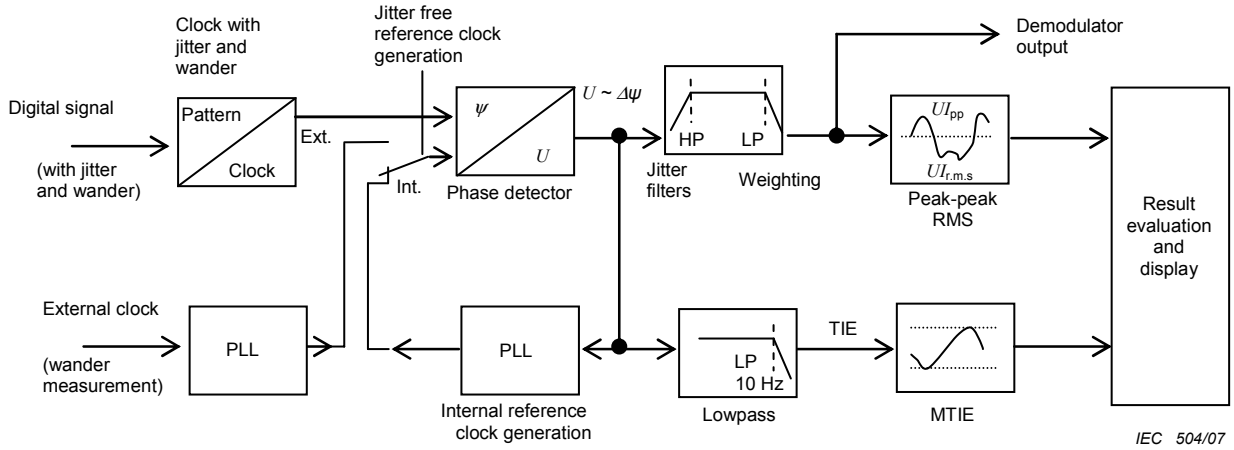


Figure 55 – Block diagram of a jitter and wander analyzer according to ITU-T O.172

The advantage of these systems over the phase noise test is that a measurement of both r.m.s. and peak-to-peak jitter is possible. The disadvantage is that these systems require an input signal (oscillator frequency) according to the standard data bit rates for optical communication systems (SONET, SDH), see Table 3.

Table 3 – Standard bit rates for various applications

SDH	SONET	Bit rate Mbit/s	Allowed oscillator frequencies
-	OC-1	51,84	25,92 MHz, 51,84 MHz
STM-1	OC-3	155,52	77,76 MHz, 155,52 MHz
STM-4	OC-12	622,08	311,04 MHz, 622,08 MHz
STM-16	OC-48	2488,32	1244,16 MHz, 2488,32 MHz
STM-64	OC-192	9953,28	4976,64 MHz, 9953,28 MHz

Oscillators with other output frequencies cannot be tested, which limits the area of application.

NOTE Other applications may have different requirements.

5.6 Mechanical and environmental test procedures

5.6.1 Robustness of terminations (destructive)

5.6.1.1 Tensile and thrust tests on terminations

The tests shall be performed in accordance with test Ua_1 (tensile) and test Ua_2 (thrust) of IEC 60068-2-21.

Unless otherwise stated in the detail specification, the values of tensile force shall be as given is Table 4 below and the values of thrust force shall be as given in Table 5 below.

Table 4 – Tensile force

Nominal cross-sectional area (1) mm^2	Corresponding diameter for circular-section wires mm	Force with tolerance of ±10 % N
$0,1 < s \leq 0,2$	$0,35 < d \leq 0,5$	5
$0,2 < s \leq 0,5$	$0,5 < d \leq 0,8$	10
$0,5 < s \leq 1,2$	$0,8 < d \leq 1,25$	20

(1) For circular-section wires, strips or pins :

the normal cross-sectional area is equal to the value calculated from the nominal dimension(s) given in the relevant specification.

For standard wires:

the nominal cross-sectional area is obtained by taking the sum of the cross-sectional areas of the individual strands of the conductor specified in the relevant specification.

Table 5 – Thrust force

Nominal cross-sectional area (1) mm²	**Corresponding diameter for circular-section wires** mm	**Force with tolerance of ±10 %** N
0,1 < s ≤ 0,2	0,35 < d ≤ 0,5	1
0,2 < s ≤ 0,5	0,5 < d ≤ 0,8	2
0,5 < s ≤ 1,2	0,8 < d ≤ 1,25	4
(1) For circular-section wires, strips or pins : the nominal cross-sectional area is equal to the value calculated from the nominal dimension(s) given in the relevant specification.		

5.6.1.2 Flexibility of wire terminations

The test shall be performed in accordance with test Ub (bending) of IEC 60068-2-21.

Unless otherwise stated in the detail specification, the load shall be so restricted that the bend starts 2,5 mm ±0,5 mm from the body of the crystal oscillator, the number of bends shall be three, and the loading mass and the values of bending force shall be as given in Table 6.

Table 6 – Bending force

Section modulus mm³	Diameter of corresponding round leads mm	Force with tolerance of ±10 % N
$4{,}2\times10^{-3} < Z_x \leq 1{,}2\times10^{-2}$	0,35 < d ≤ 0,5	2,5
$1{,}2\times10^{-2} < Z_x \leq 0{,}5\times10^{-1}$	0,5 < d ≤ 0,8	5
$0{,}5\times10^{-1} < Z_x \leq 1{,}9\times10^{-1}$	0,8 < d ≤ 1,25	10

NOTE 1 For round terminations, the section modulus is given by the following formula:

$$Z_x = \frac{\pi d^3}{32}$$

where

d is the lead diameter;

Z_x is the section modulus.

For strip terminations, the section modulus is given by the following formula:

$$Z_x = \frac{ba^2}{6}$$

where

a is the thickness of the rectangular strip perpendicular to bending axis;

b is the other dimension of the rectangular strip;

Z_x is the section modulus.

NOTE 2 The section modulus is defined in 3-21 of ISO 31-3 and the derivation of the above formulae can be found in standard textbooks on mechanical engineering.

5.6.1.3 Torque test on mounting studs

The test shall be performed in accordance with test Ud (torque) of IEC 60068-2-21.

Unless otherwise stated in the detail specification, the value of the torque force to be applied is given in Table 7.

Table 7 – Torque force

Nominal thread diameter mm	2,6	3,0	3,5	4,0	5,0	6,0
Torque Nm Severity 2	0,2	0,25	0,4	0,6	1,0	1,25

5.6.2 Sealing test (non-destructive)

5.6.2.1 Gross leak test

This test shall be performed in accordance with the procedure specified in test method 1 or 2 of test Qc of IEC 60068-2-17.

Method 1

The liquid shall be degassed water and the pressure of air above the water shall be reduced to 8,5 kPa (85 mbar) or less. It shall not be necessary to drain or remove the specimen from the water before breaking the vacuum.

Method 2

The liquid shall be maintained at 125 °C ± 5 °C. The immersion time shall be 30 s, unless otherwise specified in the relevant detail specification.

During the test there shall be no evidence of leakage of gas or air from the inside of the crystal oscillator. The continuous formation of bubbles shall be evidence of leakage.

5.6.2.2 Fine leak test

The test shall be performed in accordance with 6.4, test method 1 of test Qk of IEC 60068-2-17. Unless otherwise stated in the detail specification, the pressure in the pressure vessel shall be 200 kPa (2 bar).

The maximum leak rate shall not exceed the value specified in 3.3.5, unless otherwise stated in the detail specification.

5.6.3 Soldering (solderability and resistance to soldering heat) (destructive)

5.6.3.1 Solderability

- **Test A** (lead terminations)

This test shall be performed in accordance with method 1 of test Ta of IEC 60068-2-20. The terminations shall be examined for good tinning, as evidenced by free flowing of the solder with wetting of the terminations.

- **Test B** (surface mounted devices)

This test shall be performed in accordance with test Td of IEC 60068-2-58. The immersion time shall be 2 s ± 0,2 s at a temperature of 235 °C ± 5 °C, unless otherwise specified in the detail specification. The terminations shall be examined for good wetting of the terminations.

5.6.3.2 Resistance to soldering heat

- **Test A** (lead terminations)

This test shall be performed in accordance with method 1A of test Tb of IEC 60068-2-20. The immersion time shall be 5 s ± 1 s, unless otherwise specified in the detail specification. A screen of thermally insulating material shall be used to prevent the component being heated by direct radiation from the solder bath. It shall also allow the immersion of the terminations up to a point 2 mm from the emergence of the terminations from the body, unless otherwise specified in the detail specification.

- **Test B** (surface mounted devices)

This test shall be performed in accordance with test Td of IEC 60068-2-58. The immersion time shall be 10 s ± 1 s at, a temperature of 260 °C ± 5 °C, unless otherwise specified in the detail specification.

5.6.4 Rapid change of temperature: severe shock by liquid immersion (non-destructive)

The test shall be performed in accordance with test Nc of IEC 60068-2-14. The units shall be subjected to one cycle in a downward direction 98 °C ± 3 °C to 1 °C ± 1 °C for 5 s.

5.6.5 Rapid change of temperature: thermal shock in air (non-destructive)

The test shall be performed in accordance with test Na of IEC 60068-2-14.

For non-temperature-controlled crystal oscillators, the low and high test chamber temperatures shall be the extreme temperatures of the operating range stated in the detail specification. For temperature-controlled crystal oscillators, the low and high temperatures shall be –40 °C ± 3 °C and +85 °C ± 3 °C, respectively, unless otherwise stated in the detail specification.

The crystal oscillators shall be maintained at each extreme of temperature for 30 min, unless otherwise specified in the detail specification.

The crystal oscillators shall be subjected to 10 complete thermal cycles and then exposed to standard atmospheric conditions for recovery for not less than 2 h.

5.6.6 Bump (destructive)

The test shall be performed in accordance with test Eb of IEC 60068-2-29. The crystal oscillators shall be mounted or clamped as required by the detail specification. The three mutually perpendicular axes in which the bump is to be applied shall include:

– an axis parallel with the terminations;
– an axis parallel to the base of the crystal oscillator unit.

For surface mounted devices (SMD):

– an axis parallel with the terminal land plane;
– an axis perpendicular with the terminal land plane.

Unless otherwise specified, the combination of acceleration, duration and number of bumps shall be as specified in 3.3.2.

5.6.7 Vibration (destructive)

5.6.7.1 Vibration, sinusoidal (oscillator not operating)

The test shall be performed in accordance with test Fc of IEC 60068-2.6. The crystal oscillators shall be mounted or clamped as required by the detail specification. The three mutually perpendicular axes in which the acceleration is to be applied shall include:

– an axis parallel with the terminations;
– an axis parallel to the base of the crystal oscillator unit.

For surface mounted devices (SMD):

– an axis parallel with the terminal land plane;
– an axis perpendicular with the terminal land plane.

The detail specification shall state the acceleration spectral density (ASD), the frequency range and duration.

5.6.7.2 Vibration, sinusoidal (oscillator operating)

The test shall be as described in 5.6.7.1, except that, during the test, the oscillator shall be energized and electrical tests, as defined in the detail specification, shall be performed.

Unless otherwise stated, the combination of frequency range, vibration amplitude and duration of endurance for the above tests shall be as stated in 3.3.3.

5.6.7.3 Random vibration (oscillator not operating)

The test shall be performed in accordance with test Fdb of IEC 60068-2-64. The crystal oscillator shall be mounted or clamped as required by the detail specification. The three mutually perpendicular axes in which the acceleration is to be applied shall include:

– an axis parallel to the terminations;
– an axis parallel to the base of the crystal oscillator unit.

For surface mounted devices (SMD):

– an axis parallel with the terminal land plane;
– an axis perpendicular with the terminal land plane.

The detail specification shall state the acceleration spectral density (ASD), frequency range and duration.

5.6.7.4 Random vibration (oscillator operating)

The test shall be as described in 5.6.7.3 except that, during the test the oscillator shall be energized and electrical tests, as defined in the detail specification, shall be performed.

5.6.8 Shock (destructive)

The test shall be performed in accordance with test Ea of IEC 60068-2-27. The crystal oscillators shall be mounted or clamped as required by the detail specification. The three mutually perpendicular axes in which the shock is to be applied shall include:

– an axis parallel with the terminations;
– an axis parallel to the base of the crystal oscillator unit.

For surface mounted devices (SMD):

– an axis parallel with the terminal land plane;
– an axis perpendicular with the terminal land plane.

The degree of severity shall be as stated in 3.3.4, unless otherwise stated in the detail specification.

5.6.9 Free fall (destructive)

The test shall be performed in accordance with procedure 1 of test Ed of IEC 60068-2-32. The crystal oscillator shall be suspended by its terminations at a height of 1 000 mm. The number of falls shall be two, unless otherwise stated in the detail specification.

5.6.10 Acceleration, steady-state (non-destructive)

5.6.10.1 Acceleration, steady-state (oscillator not operating)

The test shall be performed in accordance with test Ga of IEC 60068-2-7. The crystal oscillators shall be mounted or clamped as required by the detail specification. The procedure and severity shall be as stated in the detail specification

5.6.10.2 Acceleration, steady-state (oscillator operating)

The test shall be as described in 5.6.10.1, except that, during the test, the oscillator shall be energized and electrical tests, as defined in the detail specification, shall be performed.

The procedure and severity shall be as stated in the detail specification.

5.6.11 Acceleration – 2 g tip over

To be agreed upon by the customer and the supplier.

5.6.12 Acceleration noise

To be agreed upon by the customer and the supplier.

5.6.13 Low air pressure (non-destructive)

This test shall be performed in accordance with test M of IEC 60068-2-13. The procedure and severity shall be as stated in the detail specification.

5.6.14 Dry heat (non-destructive)

This test shall be performed in accordance with test Ba of IEC 60068-2-2. The conditioning shall be carried out at the upper temperature indicated by the climatic category, for a duration of 16 h, unless otherwise stated in the detail specification.

5.6.15 Damp heat, cyclic (destructive)

This test shall be performed in accordance with test Db, variant 1, of IEC 60068-2-30, at severity b) and 55 °C for six cycles.

5.6.16 Cold (non-destructive)

This test shall be performed in accordance with test Aa of IEC 60068-2-1, at the lower temperature indicated by the climatic category, for a duration of 2 h, unless otherwise stated in the detail specification.

5.6.17 Climatic sequence (destructive)

The tests and measurements shall be performed in the following order:

– dry heat see 5.6.14;
– damp heat, cyclic see 5.6.15 (first cycle only);
– cold see 5.6.16;
– damp heat, cyclic see 5.6.15 (remaining five cycles).

In the climatic sequence, an interval of not more than three days is permitted between any of these tests, except between damp heat cyclic (first cycle) and cold tests.

In such a case, the cold test shall follow immediately after the recovery period specified for the damp heat test.

5.6.18 Damp heat, steady-state (destructive)

This test shall be performed in accordance with test Ca of IEC 60068-2-78, for 56 days, unless otherwise stated in the detail specification.

5.6.19 Salt mist, cyclic (destructive)

This test shall be performed in accordance with test Kb of IEC 60068-2-52. Severity 1 shall be used, unless otherwise stated in the detail specification.

5.6.20 Mould growth (non-destructive)

This test shall be performed in accordance with test J, variant 2, of IEC 60068-2-10.

WARNING – This test can constitute a health hazard, therefore special precautions should be observed (see Annex A of IEC 60068-2-10).

5.6.21 Immersion in cleaning solvent (non-destructive)

This test is applicable to superficial marking only. To establish the permanence of marking, this test shall be performed in accordance with method 1 of test XA of IEC 60068-2-45. The detail specification shall prescribe the solvent, the temperature of the solvent, the rubbing material and its dimensions, and the force to be used.

The marking shall be legible.

5.6.22 Radiation hardness

To be agreed upon by the customer and supplier.

5.7 Endurance test procedure

5.7.1 Ageing (non-destructive)

The oscillator units shall be maintained at a specified temperature for a continuous period of 30 days. During the period of the test, the control of temperature and the accuracy of frequency measurement shall be consistent with the accuracy of the maximum frequency variations specified. The oscillator units shall remain in the chamber throughout the duration of the test and shall be continually supplied with input power, unless otherwise specified.

The output frequency shall be measured at the end of the first 24 hours and at the end of the 30 days period. Additionally, at least four intermediate measurements shall be taken at intervals of not less than one day and not greater than five days. Measurements shall be carried out according to 5.5.4.

The performance requirements shall be expressed in terms of a maximum frequency change during the period of the test, or in terms of the slope of the frequency against time curve during the last five days of the test, based upon a minimum of three measurements.

Preferred conditions: SPXO and TCXO, the highest operating temperature specified; OCXO, +25 °C ± 2 °C.

5.7.2 Extended ageing (non-destructive)

This test shall be carried out in accordance with 5.7.1, except that the continuous periods shall be 1 000 h, 2 000 h or 8 000 h, as prescribed in the detail specification, and shall be used for information purposes only.

Measurements shall be carried out according to 5.5.4, except that they shall be made at 25 °C ± 2 °C or any other specified temperature.

5.7.3 Power consumption ageing

For sealed oven controlled quartz crystal oscillators the measurement of power consumption ageing rate shall be performed concurrently with the ageing test of 5.7.1.

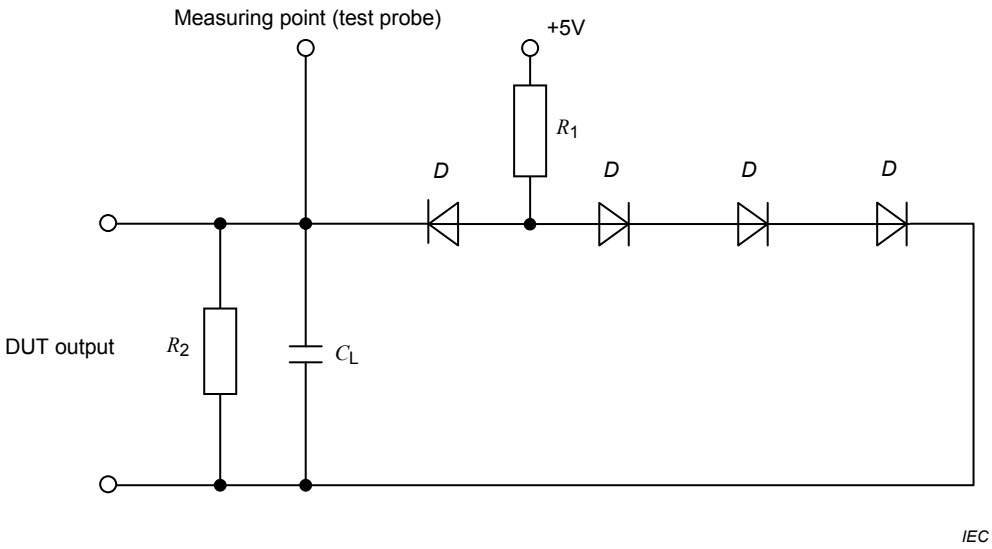
The test conditions and requirements of 5.7.1 shall apply.

Annex A
(normative)

Load circuit for logic drive

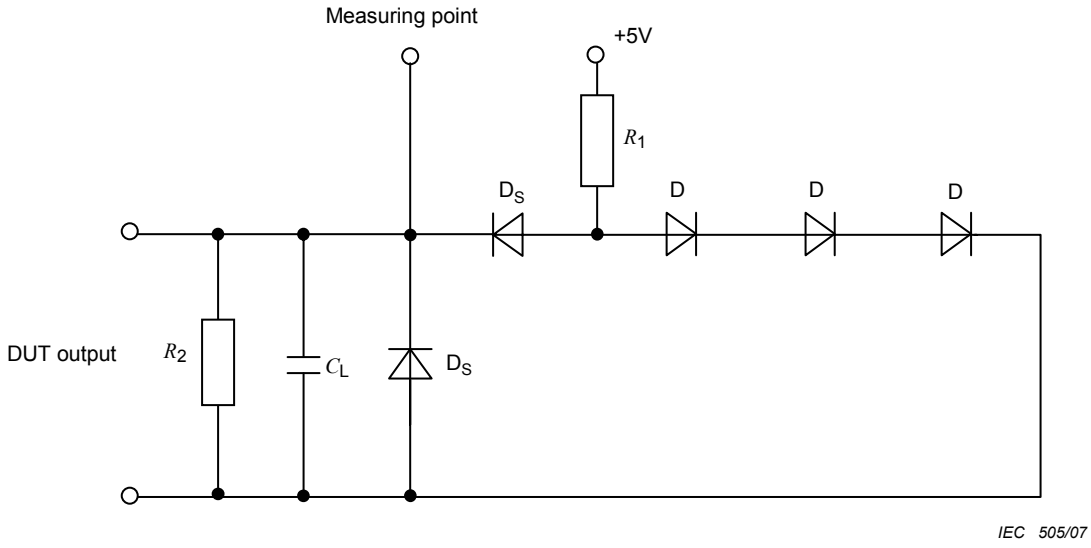
A.1 TTL and Schottky

The test fixture for oscillators designed with logic drive circuits shall simulate the load conditions which the oscillator is required to drive. Preferred test circuits for TTL and Schottky logic are shown in Figures A.1 and A.2, respectively.



NOTE Standard TTL (54/74 series)
High speed TTL (54/74 series)

Figure A.1 – Circuit for TTL



NOTE Schottky logic (54S/74S series)
Low power Schottky logic (54LS/74LS Series)

Figure A.2 – Circuit for Schottky logic

Key to Figures A.1 and A.2:

– diodes marked D shall be type 1N916 or 1N3064;

– diodes marked D_S shall be high speed Schottky type, for example 1S1993;

– values for R_1 and R_2 are dependent on the load requirement and may be calculated using the formulae:

$$R_1 = \frac{5 - (V_{OL} + V_D)}{n|I_{IL}|}$$

$$R_2 = \frac{V_{OH}}{n|I_{IH}|}$$

where

n is the number of gates;

V_{OL} is the oscillator low level output voltage;

I_{IL} is the low level input current per gate;

V_{OH} is the oscillator high level output voltage;

I_{IH} is the high level input current per gate;

V_D is the voltage drop across the diode.

NOTE V_D = 0,65 V for Figure A.1 and V_D = 0,45 V for figure A.2.

Values of these parameters for various TTL series for use in the above formulae are given in Table A.1.

Values for C_L are also given. It should be noted that C_L includes the probe and fixture capacitance.

The oscillator output voltage limit requirements using the test circuits of Figures A.1 and A.2 will normally be:

V_{OH}= 2,4 V min.

V_{OL}= 0,5 V max.

Table A.1 – Value to be using when calculating R_1 and R_2

TTL Series	74	54	74H	54H	74L	54L	74LS	54LS	74S	54S
V_{OH} (V)	2,4	2,4	2,4	2,4	2,4	2,4	2,7	2,7	2,7	2,7
V_{OL} (V)	0,4	0,4	0,4	0,4	0,3	0,3	0,4	0,4	0,5	0,5
I_{IH} (µA)	40	40	50	50	10	10	20	20	50	50
I_{IL} (mA)	–1,6	–1,6	–2,0	–2,0	–0,18	–0,18	–0,4	–0,4	–2,0	–2,0
C_L (pF)	15	15	25	25	50	50	15	15	15	15

The following information shall be specified in the detail specification:

R_1, R_2, C_L, V_{OH} and V_{OL}, together with the circuits to which reference is made.

NOTE Satisfactory operation in a particular circuit should not be considered as an assurance that a specific crystal oscillator will operate satisfactorily with all types of TTL logic.

A.2 CMOS

The test fixture for oscillators designed for CMOS logic circuits should simulate the load conditions which the oscillator is required to drive. The load circuit shall consist of a capacitance which shall be 10 pF times the number of gates being driven. The figure of 10 pF includes a 2,5 pF allowance for strays.

NOTE Satisfactory operation under these conditions should not be considered as an assurance that a specific crystal oscillator will operate in a satisfactory manner in any CMOS logic circuit.

A.3 ECL

Under consideration.

Annex B
(normative)

Latch-up test

B.1 Definition

B.1.1 Latch-up

A state in which a low-impedance path results from (and persists following) an input, output or supply overvoltage.

B.1.2 Test procedure

The latch-up test under static conditions subjects a device to greater stresses than it would encounter in normal operation and is even more severe than dynamic test methods using similar levels of current and voltage.

This test, if performed according to the procedures defined in this standard, is a necessary and sufficient method for the characterization of the latch-up susceptibility or immunity of quartz crystal controlled oscillators incorporating CMOS integrated circuits.

B.2 Test method

B.2.1 This test is destructive.

B.2.2 This test is applicable only to quartz crystal controlled oscillators containing CMOS integrated circuits.

B.2.3 This test shall be performed in accordance with IEC 60748-2.

B.2.4 This test is a recommended test procedure. It is not a specification. No test limits are given.

B.2.5 This test is performed for characterization and inspection purposes only. It is not a production test.

Annex C
(normative)

Electrostatic discharge sensitivity classification

C.1 Definition

C.1.1 Electrostatic discharge (ESD)

A transfer of electrostatic charge between two bodies having different electrostatic potentials.

C.1.2 Test procedure

This method establishes the procedure for classifying quartz crystal controlled oscillators, built with CMOS ICs, according to their susceptibility or immunity to damage or degradation caused by exposure to electrostatic discharge (ESD). This classification is used to specify appropriate packaging and handling requirements to provide classification data.

C.2 Test methods

C.2.1 This test is destructive.

C.2.2 Leaded quartz crystal controlled oscillators

For these oscillators, the Human Body Model (HBM) shall be used for the ESD test.

The test procedure is defined in IEC 60749-26.

The recommended maximum test voltage shall be 2 000 V.

Another maximum test voltage may be negotiated between supplier and customer.

C.2.3 SMD quartz crystal controlled oscillators

Since these crystal oscillators are usually assembled onto printed wiring boards (PWBs) by automated processes, the Machine Model (MM) shall be applied.

The test procedure is defined in IEC 60749-27.

The recommended maximum test voltage shall be 2 000 V.

Another maximum test voltage may be negotiated between supplier and customer.

C.2.4 The impact of ESD on oscillators in steady-state

Certain applications require that the output of an oscillator shall not be disrupted, even for a single cycle, if the oscillator enclosure is subjected to an ESD pulse.

A suitable test method is under consideration.

Bibliography

IEC 60122-1: 2002, *Quartz crystal units of assessed quality – Part 1: Generic specification*

IEC 60410:1973, *Sampling plans and procedures for inspection by attributes*

IEC 60679-2:1981, *Quartz crystal controlled oscillators – Part 2: Guide to the use of quartz crystal controlled oscillators*

IEC 60679-3:2001, *Quartz crystal controlled oscillators of assessed quality – Part 3: Standard outlines and lead connections*

IEC 60679-4, *Quartz crystal controlled oscillators of assessed qualify – Part 4: Sectional specification – Capability approval*

IEC 61000-4-3:2006, *Electromagnetic compatibility (EMC) – Part 4-3: Testing and measurement techniques – Radiated, radio-frequency, electromagnetic field immunity test*

IEC Guide 102:1996, *Electronic components – Specification structures for quality assessment (Qualification approval and capability approval)*

ISO 31-3:1992, *Quantities and units – Part 3: Mechanics* (withdrawn)

ITU-R TF 686:1994, *Glossary and definitions of time and frequency terms*

ITU-T O.172, *Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)*

IEEE 1139:1988, IEEE *standard definitions of physical quantities for fundamental frequency and time metrology*

ISBN 2-8318-9110-8

ICS 31.140

Typeset and printed by the IEC Central Office
GENEVA, SWITZERLAND