Gate Dielectric Integrity

MATERIAL, PROCESS, AND TOOL QUALIFICATION

Dinesh C. Gupta and
George A. Brown, editors

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Gate Dielectric Integrity: Material, Process, and Tool Qualification

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Foreword

The Conference on Gate Dielectric Integrity was held on January 25, 1999 in San Jose, California. ASTM Committee F-1 on Electronics sponsored the conference. The conference co-chairmen were Dinesh Gupta, of Mitsubishi Silicon America, and George Brown of Texas Instruments *(currently assigned to SEMATECH).*

The success of the conference is the result of both the hard work of many people in the industry who participated as coordinators, and the support of the Officers of Committee F-1. George Brown and Dinesh Gupta presided at the technical sessions and Howard Huff of SEMATECH joined Dinesh Gupta and George Brown in moderating the Panel discussions.

We are also thankful to all the presenters at the technical sessions who also joined as panel members. Many scientists from all over the world reviewed the manuscripts published in this book. Without their support, this publication would not have been possible. And finally, we acknowledge the hard work and efforts of the staff at ASTM in bringing the book to print.

Contents

A Note of Appreciation

The quality of the papers that appear in this publication reflects not only the obvious efforts of the authors, but also the unheralded, though essential, work of the reviewers. On behalf of ASTM, we acknowledge with appreciation their dedication to high professional standards and their contribution of time and effort.

Dinesh Gupta
George Brown

Overview

The papers in this volume were presented at the conference on Gate Dielectric Integrity (GDI) held in January 1999 in San Jose, California to describe the concepts and metrology of the Gate Dielectric Integrity and discuss its applications for the material and device process and tool qualification. ASTM Committee F-1 on Electronics sponsored the conference. In addition to the technical presentations, a panel discussion was also held at the conference. A summary of the panel discussion is provided in Appendix 2.

A wide variety of topics relating to the subject of GDI are presented in this publication. These topics include concepts, methods, protocols, and reliability assessment as related to dielectric integrity. The characterization of thin dielectrics, various GDI measurement techniques, and discussion of important effects on the characterization of GDI is also included.

The proceedings section is divided as follows:

- Concepts
- Thin Gate Dielectrics
- Characterization and Applications
- Standardization and Round Robins—included as Appendix 1

Integrity of thin dielectrics in MOS devices is a dominant factor in determining the overall reliability of microcircuits. Even though many factors influence the final performance of a circuit, device reliability, in general, starts with high quality of silicon material. Thus, gate dielectric integrity measurements are one amongst several most commonly used within so-called "Wafer Level Reliability Tests". The dielectric layer is put under stress until it fails. This failure occurs in two phases: 1) a wearout phase in which the external stress slowly degrades the oxide, and 2) a breakdown phase where certain physical parameters are exceeded and the dielectric undergoes a runaway current flow. This high current flow causes the dielectric, shortly after the electrical breakdown, to break down thermally and to be permanently damaged. Dielectric reliability may be evaluated by forcing either current or voltage, either with a fixed level or ramped (stepped) stress. MOS capacitors with polysilicon gates are customarily used as testing devices. Two stressing methods are used: 1) time-zero dielectric breakdown (TZDB), and 2) time-dependent dielectric breakdown (TDDB).

In TZDB testing, the test structure is checked for integrity by measuring the sample response after applying a constant, initial voltage or current. The stress, either voltage or current, is then increased in steps until a defined failure criterion occurs, or the applied stress reaches a specified limit. In TDDB testing, on the other hand, after a similar initial test, a constant stress level, either voltage or current, is applied until a pre-determined failure condition or upper time limit is reached.

Professor David Dumin of Clemson University explores several oxide reliability assessment attributes and associates them with oxide integrity. He discusses oxide wearout and breakdown in terms of trap generation inside the oxide and locally high current regions occurring during breakdown events. He also presents a technique to characterize electric breakdown distributions. The latter are important in determining yield and early failures of the devices.

John Suehle of National Institute of Standards and Technology discusses the oxide reliability and GDI characterization for thin gate dielectrics. The value of Q_{bd} in case of thin dielectrics and its dependence on device area and current density is discussed in his paper.

Alvin Strong of IBM Microelectronics describes the advantages and challenges of a voltage step stress technique for TDDB measurements on oxides in the range of 10 nm. He proposes the advantages as being: 1) sample homogenization, and 2) sample size minimization. "The challenge may be in the interpretation of the data obtained from this technique sometimes, but the benefits outweigh this disadvantage," he says.

Bersuker and Werking of SEMATECH propose a model that provides a physical explanation for the electric field and oxide thickness dependence of charge-to-breakdown measurements. They note that relatively lower damage in thinner oxides, as determined by the concentration of generated traps, may produce a greater effect on oxide leakage current. Therefore, gate leakage current may not directly represent oxide damage after heavy stress. In fact, they find that after heavy stress, leakage current is determined by the probability of trap assisted tunneling, while in lightly damaged oxides the density of generated traps controls leakage.

Gilbert Gruber and Robert Hillard of Solid State Measurements, Marshall Wilson and Jacek Lagowski of Semiconductor Diagnostics, and Mark Dexter, et al. of Texas Instruments describe various non-contact measurements of Gate Dielectric Integrity, and discuss some of the applications of these measurements. Gruber and Hillard stress the need for making the measurements rapidly and accurately, and present the use of Hg probe for GDI measurements. They discuss the application of this measurement in monitoring a variety of process induced defects. Wilson and Lagowski describe COCOS metrology which maps contact potential difference and surface photovoltage produced from the application of electric charge on the dielectric surface. They discuss various applications of this technique in the monitoring of process flows and contamination. Hasslinger and Dexter utilize measurements made on the Quantox tool to monitor oxidation furnaces routinely, and to solve the problem of contamination introduced during a high temperature device process. This contamination had resulted in parametric failures in LOCOS devices.

The paper by Michael Seacrist describes various applications of GDI measurements in silicon wafer manufacturing. "Silicon wafer related GDI sensitivity has driven silicon wafer suppliers to reduce and eliminate the vacancy-related defects," he says and discusses other wafer properties such as the smoothness and purity of the silicon surface, which influence thin dielectric GDI measurements. The paper by Grann et al. of Wacker Siltronic gives GOI measurements at different oxide thicknesses.

Miner et al. of Applied Materials discuss the process and equipment technologies for depositing thin gate dielectrics. They also discuss the differences in the reaction chemistry of deposition responsible for improvement in gate dielectric integrity. Murakami et al. from Mitsubishi Materials Silicon Corporation apply the high-resolution GDI measurements to study the defect level in various types of silicon wafers such as, Pure Silicon™, epitaxial silicon, hydrogen annealed bulk silicon, so-called low COP silicon, and conventional CZ silicon wafers. Using the TDDB technique, they show a correlation between grown-in crystalline defects and defects in the deposited oxide.

The papers by Dumin, Suehle, and most others give a broad bibliography on the topic of gate dielectric integrity. The articles published in the 1999 Symposium on VLSI Technology may also be interesting to readers.

Appendix 1 gives the interim results of two round robins on the gate dielectric integrity. These round robins are currently in progress. One of the round robins is being conducted in the USA under the joint auspices of JEDEC and ASTM Committees, and the other in Japan under the joint cooperation of JEIDA and SEMI Japan Committees. The U.S. round robin is based on three test procedures: voltage ramp test, current ramp test, and bounded current ramp test. On the other hand, the purpose of the Japan round robin is to standardize the characteristic evaluation of silicon wafer quality by oxide dielectric breakdown method.

Finally, appendix 2 gives a synopsis of panel discussions held at the conference. The Panel members were the presenters of the papers included in this volume.

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Concepts

D. J. Dumin[1]

Gate Oxide Reliability Assessment and Some Connections to Oxide Integrity

Reference: Dumin, D. J., **"Gate Oxide Reliability Assessment and Some Connections to Oxide Integrity,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification , ASTM STP 1382*, D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: Most characterizations of oxide reliability involve extrapolation of high voltage results to low voltage operation. Wearout at high voltages tends to be global while many reliability attributes, such as breakdown and stress-induced-leakage-currents (SILCs), tend to be local. This paper will explore several oxide reliability assessment attributes, including oxide breakdown, stress-induced-leakage-currents, and trap generation. These attributes will be described and an attempt will be made to associate them with oxide integrity.

Keywords: oxide reliability, oxide breakdown, trap generation, oxide integrity, reliability assessment, stress-induced-leakage-currents, SILCs, electric breakdowns, thermal breakdown, dielectric breakdown

Introduction

Since the invention of the metal-oxide-semiconductor (MOS) transistor in the 1960s the insulator of choice has been thermal silicon oxide. This material combines the highly desirable properties of an almost perfect insulator with the stable interface needed for reliable MOS operation, even in the presence of high electric fields [1], [2]. As with all insulators in electrical applications, it was early recognized that characterizing this material for quality, reliability, wearout, and breakdown was important.

It has been well documented that many of the local wearout/breakdown properties of the oxide and the oxide integrity are dominated by defects in the silicon substrate [3-7], by additions of impurities, intentional or inadvertent to the oxide [8-18], by surface roughness [19-26], and by anode material [27-28]. The differences in the surface roughness between the oxide-substrate interface and the oxide-gate interface has been used to explain the polarity dependence of breakdown [29-30]. The dominance of the cathode and the importance of the oxide field both contribute to the polarity dependence of breakdown and to the differences in breakdown distributions obtained with different gate materials [29-31].

Based on this general background, the following topics will be discussed. The wearout-breakdown process will be described, for both thick and thin oxides, where the details of the breakdown triggering mechanism are somewhat different. The importance of trap generation will be described in the context of correlating traps in the oxide with increased oxide leakage and with their role as a breakdown triggering mechanism. The use of stress-induced-leakage-currents (SILCs) will be briefly discussed as a characterization tool, particularly in thinner oxides where standard trap generation measurements are difficult to interpret. The differences between the electric breakdowns and the thermal breakdown will

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be described in some detail, with emphasis on the similarities and differences between these two breakdowns, and how the electric breakdowns can be used to describe oxide reliability and integrity. This paper will conclude with some suggestions for future work.

The Breakdown Process

In the 1960s and 1970s a description of the breakdown process was formulated [32-38]. The following description of the wearout-breakdown process is found in [38]:

"III. THE BREAKDOWN EVENT ... breakdown in thin-film capacitors as a multistage event consisting of (1) an initiating process followed by (2) instability and current runaway, (3) the voltage collapse and discharge of the electrostatic energy stored in the specimen and, (4) the establishment of a new low-voltage state. The discharge usually occurs in a filament and for capacitors with thin counter electrodes (<1000 A) nonshorting breakdowns may occur where the high localized currents and temperatures evaporate the electrode material around the breakdown channel, isolating the damaged area. For the nonshorting event two additional steps are required: (5) quenching of the hot breakdown channel and (6) recovery of the circuit via the series-resistor-sample-capacitor time constant"

Notice that this description of breakdown includes events that have become known as early-breakdowns, soft-breakdowns, quasi-breakdowns, and electric breakdowns [39-45]. This description of breakdown also leads to the concept of non-uniqueness of breakdown distributions [46]. The measurement of the breakdown event depends on the equipment used to make the measurements and the definition of what will be counted as a breakdown. That is, it is possible to count an electric breakdown as the breakdown event or it is possible to wait until thermal breakdown occurs. Even in the 1990s authors continue to redescribe this breakdown sequence, as if it were a new physical model, [47-51] in almost identical terms to that used in the 1960s and 1970s [32, 33, 38].

The wearout-breakdown process has been schematically shown in Figure 1. In this figure the wearout or weakening of the oxide has been shown as leading to the formation of an initial conducting path. When a conducting path forms between the cathode and anode, the electrical energy stored in the capacitor, $1/2\ CV^2$, discharges through this path, raising the local temperature, melting the materials, and leading either to an electric breakdown or a dielectric breakdown. In thicker oxides this conducting path is probably triggered by local avalanche processes in the oxide [52-55]. In thinner oxides the path is probably triggered by a local trap assisted tunneling or Bohr radius overlap between the traps generated by the high fields [56-61]. Optical techniques have been developed and used to confirm the local nature of multiple electrical breakdowns and of the final thermal, dielectric breakdown. [23, 25, 44, 46, 62-70]. Regardless of which process or processes lead to the generation of a local high current density region, it should be emphasized that the triggering of the breakdown is a thermal event and is caused by a local, high-temperature region.

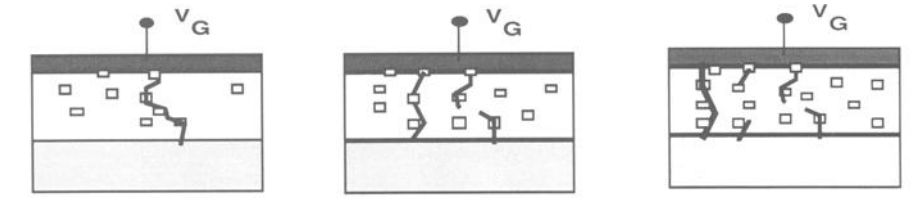


Figure 1 *The model of breakdown involving the formation, collapse, and re-formation of conducting paths between the cathode and anode.*

Trap Generation

Several techniques for measuring the trap densities or charge densities generated by the high voltages have been developed. One of the techniques that shows both good and bad features is shown in Figure 2. In this figure quasi-static capacitance-voltage (QSCV) characteristics of a 10 nm thick oxide have been shown before and after stressing at -9V until a fluence of over 1 C/cm^2 had passed through the oxide. The different C-V characteristics were recorded by changing the voltage at which the C-V measurement began. All of the measurements were begun at positive voltages, which was necessary because the substrate was p-type. The starting voltage polarity was opposite to the stress voltage polarity and partially tunnel discharged some of the stress generated traps, thus changing the measured flatband voltage [71-73]. If the flatband voltage had been used to determine the charges trapped in the oxide by the -9 V stress, then the amount and sign of the charges would have depended on the measurement conditions, resulting in an unacceptable technique for measuring oxide traps. However, the shape of the QSCV characteristics did not depend on the measurement sequence and could be used to determine the interface trap densities across the bandgap [74]. It can be seen from Figure 2 that the QSCV characteristics, and by inference, the interface trap densities, were all identical, regardless of the measurement sequence. Thus, measuring charge densities in the oxide after a stress can be meaningless. However, measuring interface trap densities results in a consistent and reproducible characterization of the interface damage caused by the high voltage stress.

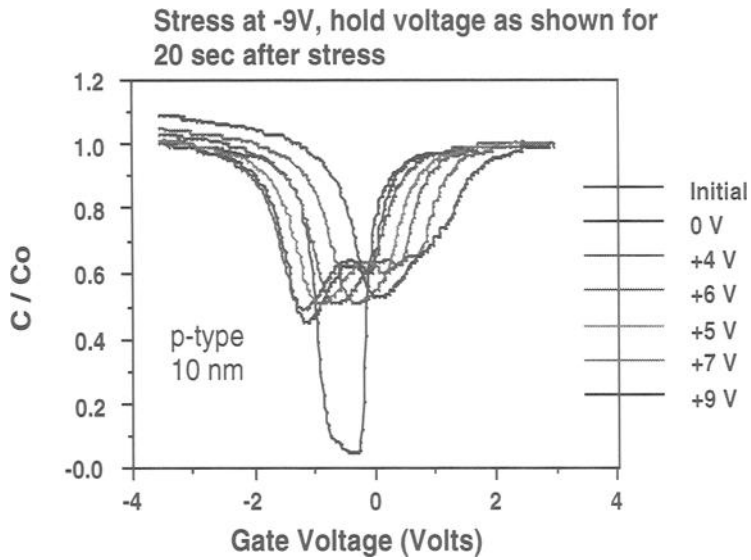


Figure 2 *Quasi-static C-V characteristics before and after identical stresses. The shape of the characteristics was independent of the small voltages applied after the stresses, while the flatband voltage shifts depended on how the measurement was made.*

The interface trap densities measured on 10 nm thick oxides have been plotted as a function of stress fluence in Figure 3 for oxides stressed at different voltages. At each of the target fluences the interface trap densities increased, in some cases as much as two orders of magnitude as the stress voltages were raise by 2 or 3 volts. Thus, the stress

voltage, or stress field, was more important in determining interface trap densities than was the fluence of electrons passing through the oxide. The fluence dependence of trap generation was sub-linear, with a fluence$^{(1/2)}$ dependence being a good fit to the data. Except for the anomalous positive charge (APC) portion of the trap generation, the sub-linear fluence dependence of trap generation is generally observed [75-77].

The importance of the sub-linear fluence dependence of trap generation can be realized by replotting the data of Figure 3 to show the interface trap generation rate in traps per fluence (electron) as shown in Figure 4. The trap generation is high at the start of the stress, falls as the stress progresses, and follows a fluence$^{-(1/2)}$ dependence, independent of stress polarity or substrate type. This fluence dependence of trap generation has lead to the concept that the traps are generated by the breaking of bonds in the oxide and the data shown in Figure 4 is actually a measure of the energy dispersion relationship for trap generation [77]. When the stress begins, the weakest bonds in the oxide are the first to be broken. As the stress continues it becomes more difficult to break a bond, since the weakest bonds have already been broken. The concept of using fabrication technology to increase bond strength and improve oxide reliability has been demonstrated [78]. The energy, bond-angle dispersion of the bridging oxygen bonds supports this model of bond breakage and trap generation [79]. High-voltage trap generation occurs in all oxides and is a global property of the oxide. As such, trap generation is probably not a very sensitive measure of oxide integrity, which is a more local phenomenon.

When the tunnel charge-discharge of the stress-generated traps is used to measure the bulk oxide trap density [80-84], similar fluence dependences are measured, as shown in Figure 5 [61]. The stress-generated bulk oxide trap densities were proportional to the fluence$^{(1/3)}$ and the trap generation rate was proportional to the fluence$^{-(2/3)}$. These different fluence dependences reflected the different coordination of interface trap densities (cm^{-2}) and bulk trap densities (cm^{-3}) and not some fundamental differences in the trap generation processes. The bulk trap generation rate dropped as the trap generation process continued. Trap densities of the order of mid-10^{19} / cm^3 occurred immediately prior to breakdown. These trap densities prior to breakdown are consistent with the model of breakdown being triggered by the generation of a local trap-assisted-tunneling current path in thinner oxides[60-63].

One of the problems that occurs when measuring either interface traps or bulk traps is the decrease in the measured trap densities as the oxides become thinner [85, 86]. While several authors have attributed this decrease in measured trap densities to decreases in trap generation, it is more likely due to the techniques used to measure the traps [86]. Traps within a tunneling distance, about 2 to 3 nm, of either interface tunnel charge and discharge in the first few seconds after the stress is removed. Most techniques for measuring trap densities are not able to account for these traps [86, 87]. Using conventional C-V or tunnel discharge measurements to measure the trap densities in oxides thinner than about 9 nm seriously underestimates the trap densities inside the oxides.

A recent study of the trap densities was made in oxides whose thicknesses were systematically varied between 5 nm and 13.5 nm [88]. The trap densities were measured as a function of stress field, stress fluence, and stress time. Typical trap density vs. electric field data taken on some of the 7 nm and 13.5 nm thick oxides have been shown in Figure 6. Similar data were taken on all of the other oxides. It was found that all of the trap density data, on all of the different thicknesses of oxides, for all stress fields, times, and fluences could be fit by one simple trap generation equation [88]. The trap density, N_T, was given by

$$N_T = N_0 \cdot \exp^{-(E_a / kT)} \cdot t^m = N_0 \cdot \exp^{-((\Delta H - \beta E_0) / kT)} \cdot t^m \qquad (1)$$

The constant, N_0, was found to be centered around $1.2 \cdot 10^{21}$ / cm^3, which is approximately the density of the bridging oxygen bonds in silicon oxide [79, 87]. Using the measured value of activation energy, E_a, of 0.2 ev, measured at 10 MV/cm [89], it is possible to determine ΔH, the enthalpy, as 0.32 ev. The constant, β, has the value of 0.012 cm/MV. The value of m was previously determined to be approximately 0.2 [90, 91].

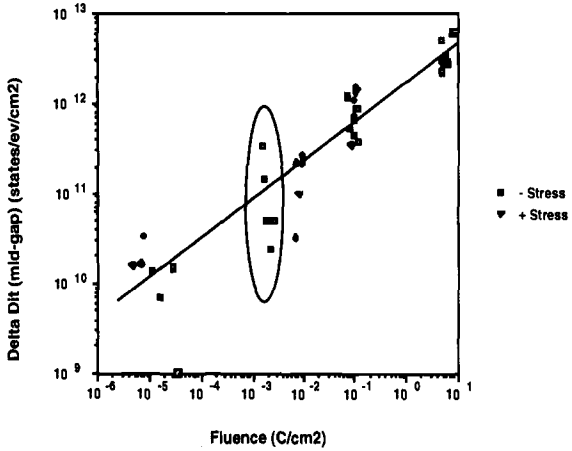


Figure 3 *Stress-generated interface trap densities as a function of stress fluence for 10 nm thick oxides stressed at different voltages. At each fluence level the different trap densities represent data taken at different oxide fields.*

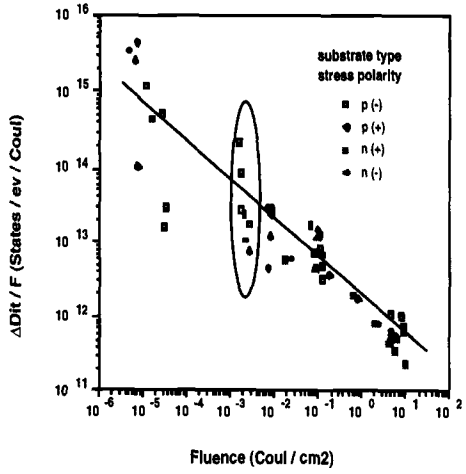


Figure 4 *The interface trap generation rate as a function of stress fluence showing thedrop in trap generation efficiency as the stress progresses.*

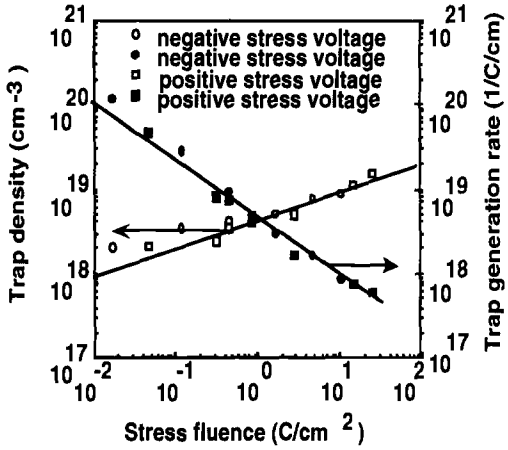


Figure 5 *Bulk oxide trap generation and trap generation rate as a function of stress fluence showing the fluence$^{(1/3)}$ and fluence$^{-(2/3)}$ dependences of the trap generation and trap generation rate, respectively.*

All of the constants in Eq. 1 have physical significance. The value N_0 indicates that the bridging oxygen bonds are the likely source of the traps, which may be oxygen vacancies [92], generated by the high fields [79, 92 - 95]. These traps are responsible for creating the conducting path between the cathode and anode that triggers breakdown in thin oxides [93, 96, 97]. The term ($\Delta H - \beta E_0$) is a field dependent activation energy. When ($\Delta H - \beta E_0$) = 0, there is no barrier to converting all of the bridging oxygen bonds to oxygen vacancies and the ultimate field strength of the oxide has been reached. The ultimate field strength of the oxide predicted by Eq. 1 is 27 MV/cm which is very close to the value of 30 MV/cm previously given [1]. The field acceleration factor, β, was found to be 0.012 cm/MV/ev, which predicts a factor of 10 increase in the trap density for every increase in field of 0.8 MV/cm. This field acceleration factor is very close to the factor of 10 increase in time-to-breakdown observed for every increase in field of 1 MV/cm [98, 99].

Using the measured values of N_0 and enthalpy, Eq. 1 can be written as

$$N_T = 1.2 \cdot 10^{21} \cdot \exp(-(0.32 + 0.012\, E_0) / kT) \cdot t^{0.2} \qquad (2)$$

This equation can be rearranged to predict the time-to-breakdown [100] by solving for time, and equating this time to the time-to-breakdown. The time-to-breakdown becomes

$$t = ttb = (N_T / N_0)^5 \cdot \exp(-(1.6 - 0.06\, E_0) / kT) \qquad (3)$$

The time-to-breakdown measured by long-time, low-field tests has yielded a ttb of

$$ttb = A_0 \exp((1.15 - 0.07\, E_0) / kT) \qquad (4)$$

which agrees quite well with the time-to-breakdown predicted based on trap generation data [93, 97, 101]. Notice that the activation energies of trap generation and breakdown are field dependent and are different from each other, something noted by others [102].

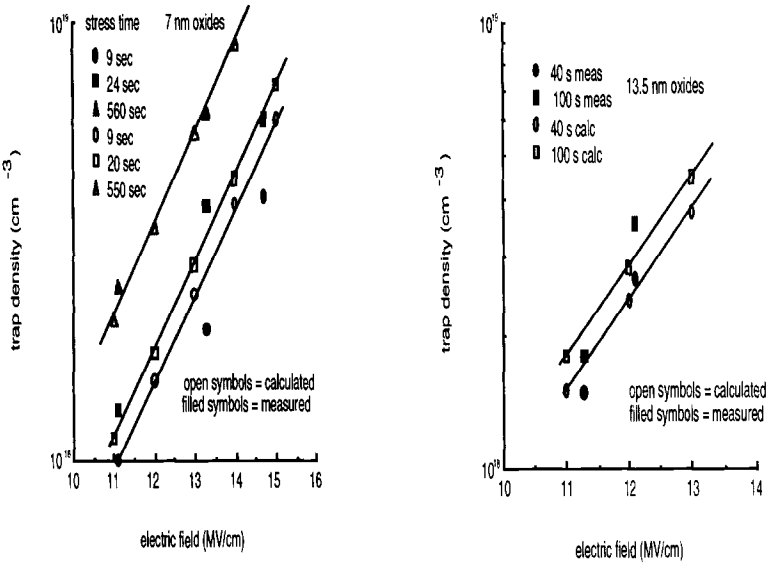


Figure 6 *Trap densities in 7 nm and 13.5 nm thick oxides as a function of stress field. The filled symbols represent the data and the open symbols represent the fit to the data described by Eq. 1.*

While most of the discussion of trap generation has focused on the traps being a precursor to dielectric breakdown, it should be noted that breakdown is not triggered by traps in the oxide. Breakdown is triggered by a locally high current density which leads to locally high Joule heating, thermal runaway, local melting and then, usually, evaporation of the melt, followed by multiple repetitions of this process until a stable short circuit is formed between the cathode and anode. It is possible to demonstrate that an oxide can breakdown without having a large density of stress generated traps by limiting the trap generation prior to the breakdown event. The QSCV characteristics shown in Figure 7 were taken on a 10 nm oxide grown on p-type silicon. The oxide was stressed with the surface in deep depletion, in the dark, where the current through the oxide was limited by the minority carriers (electrons) generated inside the depletion region of the semiconductor. The stress voltage that caused breakdown was +50 V and most of this voltage was dropped across the silicon depletion region. The QSCV characteristic has been shown before breakdown, after breakdown had occurred and the short circuit had been subsequently open-circuited using a technique similar to that previously described [32, 33, 37, 38], and after further stress at +45V. There were very few traps generated in the oxide, as can be seen by comparing the QSCV characteristics of Figure 7 with the QSCV characteristics of Figure 2. During all of these stresses the fluence through the oxide was less than 10^{-3} C/cm^2, very few traps were generated in the oxide because the oxide field was small, and yet the oxide broke down. The local breakdown region was probably caused by a high

local current density, triggered by local avalanching in the silicon.

In the above discussion concerning trap generation, it was assumed that the oxide field was the dominant trap generation mechanism. The details of trap generation are not yet completely known. It is still unclear if back-diffusion of holes generated in the silicon substrate or gate [75] or if hydrogen released at the anode [76] help catalyze the trap generation reaction. However, the hole back-diffusion will be very small at voltages below 5 V because the electrons arriving at the anode do not have sufficient energy to generate a hole capable of back-diffusing into the valance band of the oxide. This anode hole model also predicts trap generation proportional to the electron fluence, something not measured [75, 76, 77] and an infinite time-to-breakdown at zero electric field, a concept at odds with our understanding of entropy [96]. The liberation of hydrogen at the anode requires an electron energy greater than 2 ev and, thus, should not be important in circuits operating at voltages around 1.5 V.

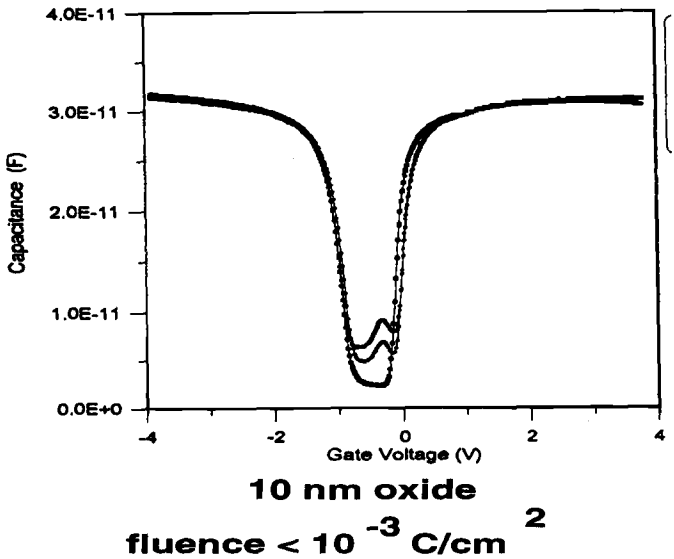


Figure 7 *QSCV characteristics taken on 10 nm thick oxides before breakdown, after breakdown and open-circuiting of the breakdown region, and after subsequent continued stress. The oxides were stressed in deep depletion where there was very little current through the oxide and relatively low fields across the oxide during the stress.*

Stress-Induced-Leakage-Currents (SILCs)

It has been known for some time that high voltage stresses lead to increased pretunneling currents, often called stress-induced-leakage-currents (SILCs) [103, 104]. These SILCs are directly proportional to the density of traps generated by the high voltage stresses [103, 104, 84, 105]. While these low-level leakage currents are generally not significant in logic circuit operation, they are a limiting factor in non-volatile memory operation because they reduce data retention time [106]. It is now recognized that SILCs are more complicated than just increases in the pretunneling currents. There are SILCs, often called type-B SILCs, that are associated with the minuscule conducting paths associated with electric breakdown regions [107-109]. These type-B SILCs lie, in magnitude, between the trap-assisted-tunneling currents caused by the traps and the high currents associated with the thermal breakdown region. Recently it has been found that the

trap-assisted-tunneling SILCs are composed of two terms, a dc term and a transient term [71, 72, 86, 110-119]. Both the field and thickness dependences of the two components are different [111, 112]. It should be noted that ionizing radiation produces SILC-like currents in an oxide [120-126]. However, these currents are not permanent and vanish once the less mobile holes have drifted or diffused out of the oxide. SILC-like currents can also be generated by incorporation of impurities into the oxide [8-10, 15], a property of the impurities that led to early non-volatile memories [9]. The impurity generated SILCs have the same dc-transient and dc components as stress-generated SILCs [10,15].

Measurement and Characterization of Breakdown

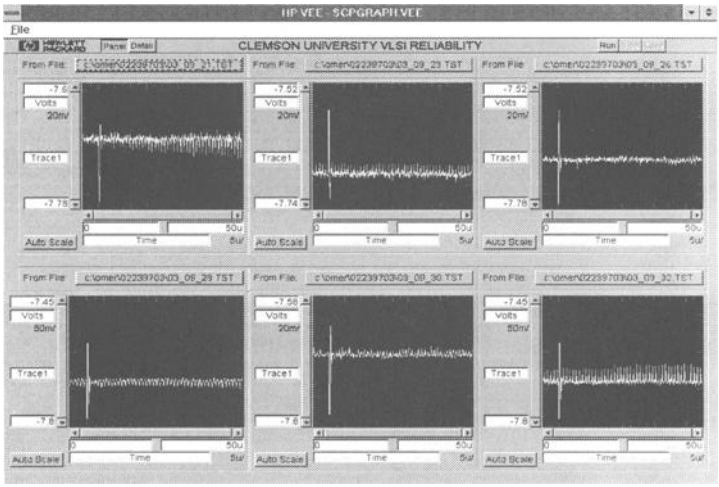
In light of the discussion above concerning the electrical/thermal nature of the breakdown events, a brief discussion of the measurement and characterization of breakdown is appropriate. The breakdown process involves both the electrical breakdowns and the thermal breakdown [32-38]. The importance of differentiating between the electrical breakdowns and the thermal breakdowns has been codified in a recent ASTM Standard dealing with ramped voltage breakdown measurements [127]. The electrical breakdowns have been discussed for constant current measurements [45, 128-131] and for constant voltage measurements [46, 132]. It has been shown that, while the breakdown voltage distributions of the electrical and thermal breakdowns are different, they produce parallel distributions [132, 133].

A series of measurements were undertaken to more clearly define details of the electrical and thermal breakdowns. The time-to-breakdown distributions for constant-voltage stressings of several oxides between 1.6 nm and 80 nm were determined. For each series of measurements, on a given thickness of oxide, the area of the capacitors was held fixed. During each measurement the current flowing through the oxide was measured using a HP 4140b pAmeter. A high speed storage oscilloscope, Tektronix TDS-520, was used to measure, record, and store the transient voltage across the oxide whenever an electric or thermal breakdown occurred. The surface of the gate on top of the oxide was optically observed to see when spots indicating a breakdown had occurred. Whenever an electrical breakdown produced the classic drop in voltage followed by a recharging of the oxide [32-38], the wave shape of the voltage across the oxide was recorded and stored in a large memory file. In thicker oxides a spot associated with the melting that accompanied an electrical breakdown appeared on the surface of the gate.

A few of the many typical waveshapes observed during one constant voltage stress test have been shown in Figure 8. The frequency of the electric breakdowns tended to increase as the stress time increased. The waveshapes of the individual electric breakdowns did not significantly change during the stress.

Several breakdown distributions measured on a small number of oxides have been plotted in Figure 9. The times of the first electric breakdowns have been plotted along with the times of the thermal breakdowns. These two distributions were relatively parallel, similar to the breakdown voltage distributions previously reported [133]. These two distributions were over an order of magnitude different in time-to-breakdown. These two distributions have been referred to as a time-dependent-electric-breakdown (TDEB) distribution and a time-dependent-dielectric-breakdown (TDDB) distribution, respectively. In Figure 9 two other breakdown distributions have also been recorded. For one of these distributions a low-impedance voltage source, VIZ WP-711, was used to produce the applied voltages. The VIZ WP-711 power supply was manufactured by VIZ Mfg. Co., Phila., PA, 19144 and had an internal impedance of approximately 10 ohms. The time-to-breakdown distribution measured when this power supply was used as the voltage source produced breakdown times very close to those measure by the TDEB distribution. For the other distribution, the HP 4140b pAmeter was used to supply the voltages to oxides, but an auxiliary external capacitor was placed across the oxide. The purpose of this additional capacitor was to store more capacitive energy and to make this energy available at the time

of an electric breakdown. The time-to-breakdown distribution measured when an external capacitor provided more capacitive stored energy, 1/2 CV^2, to the electric breakdown regions was also close to the TDEB distribution. Thus, the measured time-to-breakdown depended both on the measurement equipment and the definition of breakdown.



ALL ELECTRIC BREAKDOWN WAVESHAPES AND TIMES ARE RECORDED

Figure 8 *Waveshapes of electric breakdowns prior to thermal breakdown.*

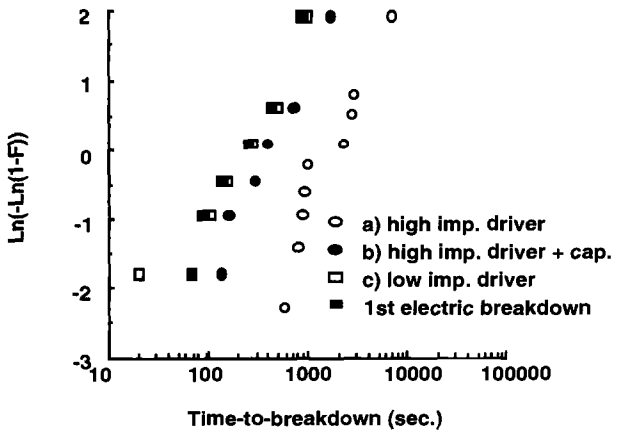


Figure 9 *Electric and thermal breakdown distributions obtained on identical oxides at the same stress fields. The explanation of the different distributions is given in the text.*

The explanation for the different breakdown distributions described in Figure 9 is inherent in the definitions of electrical and thermal breakdowns [32-38]. Every electric breakdown is a possible thermal breakdown. All that is needed to force an electric breakdown into becoming a thermal breakdown is to efficiently couple the electrical discharge of the capacitor during an electric breakdown into the formation of a large thermal melted region, a region sufficiently large that it will not open circuit during the subsequent discharge of the capacitor. Either a low impedance source, which could provide more total energy to the oxide during an electric breakdown event, or the use of an external capacitor to provide more energy during the electric breakdown could raise the local temperature to the point where a large, stable short circuit formed between the cathode and anode. The data shown in Figure 9 demonstrates different ways of coupling the energy of the electrical breakdown into the thermal breakdown and shows that breakdown distributions are not unique, but depend on the equipment and techniques used to measure them.

It is possible to use the electric breakdown distribution to simplify the measurement of the extrinsic portion of a breakdown distribution. It must be recognized that every electric breakdown is a possible thermal breakdown. Thus, if all of the times of the electric breakdowns are recorded, up to the final thermal breakdown, then a plot of the time-to-electric-breakdowns is, in reality, a plot of all of the possible times-to-thermal-breakdown. In Figure 10 the breakdown distribution obtained on 6 identical capacitors has been plotted. In this figure the open symbols are all of the electric breakdown times and the 6 filled symbols are the thermal breakdown times. As can be seen the electric breakdowns form the same "intrinsic" breakdown distribution that is found for the thermal breakdowns. However, the very large number of early electric breakdowns that were recorded also produced a plot of the "extrinsic" breakdown population. Usually, in order to obtain a multimodal breakdown distribution, particularly on modern high quality oxides where extrinsic breakdown is very unlikely, it is necessary to consume much time and break down hundreds of capacitors. The data shown in Figure 10 indicates a simple way of obtaining an "extrinsic" breakdown population using only a small number of devices. It is only necessary to record all of the times of the electric breakdowns and the thermal breakdowns on a small number of capacitors and then plot the total distribution. In Figure 11 similar electric/thermal breakdown distributions have been plotted for 3 nm thick oxides, showing the usefulness of this technique for producing breakdown distributions, even for very thin oxides. The concepts described above have been successfully applied to oxides as thin as 1.6 nm.

The electric breakdowns may be the cause of the overerase upsets in EEPROMs [134, 135]. This overerase upset has the following characteristics. During the erase of the EEPROM cell, Fowler-Nordheim tunneling currents flow through the oxide over the source. Some of the cells overerase and must be reprogrammed by a soft write. On every erase cycle, in general, different cells overerase, but occasionally the same cell overerases many times. In general, the number of cells that overerase increases as the number of write/erase cycles increases. It is proposed here that the cause of the overerase upset is electric breakdowns that occur locally during the high voltage erase operation. These overerase upsets have been shown schematically in Figure 12. These overerase upsets are not destructive and are self healing. They will produce a statistical distribution of over-erase upsets very similar to the statistical distribution of electric breakdowns.

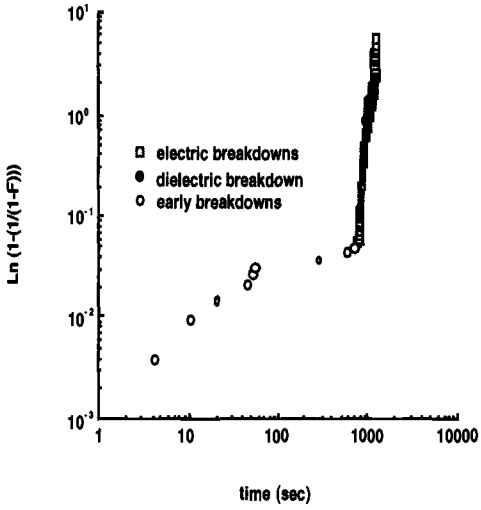


Figure 10 *The times of the electric and thermal breakdowns taken on 6 identical oxides, plotted as a breakdown distribution, showing an easy way to obtain both the "intrinsic" and "extrinsic" breakdown populations, using only a small number of oxides.*

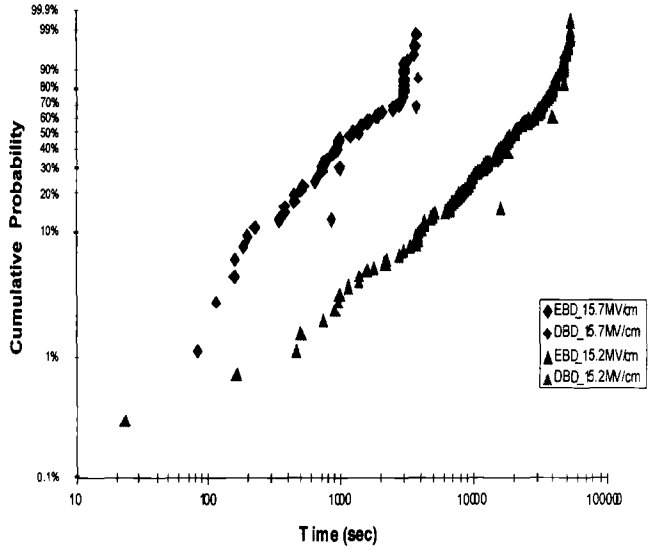
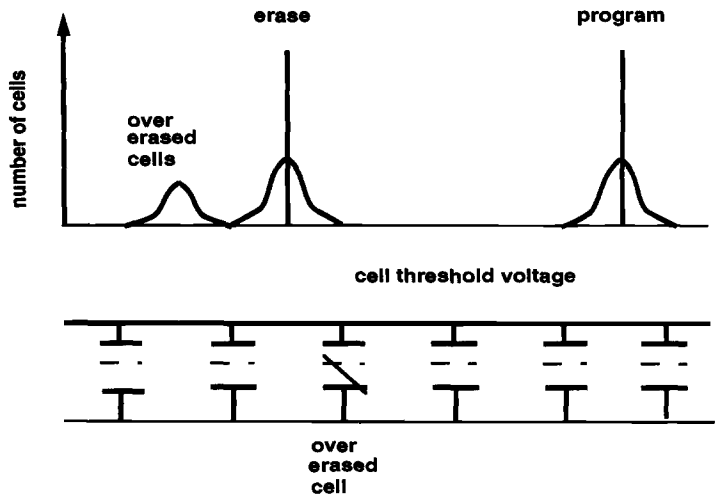


Figure 11 *Electric/thermal breakdown distributions obtained on 3 nm thick oxides at two different electric fields.*



SCHEMATIC DRAWING OF ONE CELL OVER ERASED

Figure 12 *A schematic sketch of the over-erase upset problem caused by source-side Fowler-Nordheim tunnel erase and electric breakdowns in the oxide in the vicinity of the source.*

Discussion and Conclusions

The field of oxide wearout and breakdown has been briefly discussed in terms of trap generation inside the oxide and locally high current regions occurring during breakdown events. There are, in general, many electrical breakdown events occurring prior to the thermal breakdown. The local breakdowns can be triggered by trap generation inside the thinner oxides and by avalanching in thicker oxides. However, these breakdowns can also be triggered by impurities or asperities, particularly at or near the cathode. These asperities are probably exceedingly important in determining oxide integrity. If the oxide is completely uniform and amorphous, then the incidence of early breakdowns or "extrinsic" breakdowns may be reduced, but early failures will still occur due to the statistics of the wearout/breakdown process.

Many of the processes occurring in oxides during high voltage stresses can be characterized by measuring the stress-generated trap densities. However, it should be recognized that conventional trap generation techniques severely underestimate the trap densities in very thin oxides. For thinner oxides, where tunnel charging and discharging of the traps near the interfaces underestimate the trap densities, SILCs are probably a better measure of trap generation. It is important to recognize that the SILCs contain both dc and transient components, and that these two components have different field and thickness dependencies.

Dielectric breakdown distributions, in spite of their near universal use, provide limited information concerning the physics of wearout and breakdown, since they are dominated by the thermal breakdown and are not a measure of the first breakdown in the oxide. The nonuniqueness of breakdown distributions is an area of oxide reliability that must be explored in greater detail in the future to insure that the measured breakdown data taken on large area capacitors at high voltages is applicable to small area devices operating at low voltages. More effort should be placed on measuring the transient electric breakdowns that occur prior to thermal breakdown, particularly for gate oxide integrity characterization.

The field, fluence, time, and thickness dependences of trap generation have been

measured and fitted to an Eyring equation. It was shown that the measured and calculated trap densities agreed quite well and the measured trap generation predicted the ultimate field strength of the oxides and the measured field and time dependences of breakdown distributions. The measured parameters found in the Eyring formulation point to the physical processes taking place inside the oxides during wearout. The traps are probably associated with the bridging oxygen atoms and are either oxygen vacancies or motion of the bridging oxygen atoms.

The most critical application where oxide wearout, trap generation, SILCs, and electric breakdowns are important is in the area of non-volatile memory production. The oxides in these devices not only sustain the highest operating fields of oxides in ICs but are most sensitive to oxide degradations. Methods of quickly and accurately characterizing oxide integrity in these devices are needed. It should be noted that a recent publication concerning EEPROM reliability indicated that dielectric breakdown is not observed in EEPROM devices because, while the applied field might be quite high, the total amount of capacitive energy is too small to trigger thermal breakdown [136].

Electric breakdowns are most important in determining yield and early failures. A technique has been presented that uses transient voltage measurements to characterize electric breakdown distributions. This technique has an advantage over other techniques for obtaining "extrinsic" breakdown populations, in that it requires recording many electric breakdowns on a small number of oxides. Oxide integrity can probably be characterized by measuring the electric breakdown distributions.

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Thin Gate Dielectrics

John S. Suehle[1]

Ultra-Thin Film Dielectric Reliability Characterization

Reference: Suehle, J. S., **"Ultra-Thin Film Dielectric Reliability Characterization,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382,* D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: The reliability of gate oxides is becoming a critical concern as oxide thickness is scaled below 4 nm in future technology. The breakdown detection algorithms in traditional reliability characterization techniques must be modified for sub-4 nm thick SiO_2 films that exhibit excessive tunneling currents and soft breakdown. It becomes essential to fully understand the physical mechanism(s) responsible for gate oxide wear-out and breakdown if reliability projections are based on the results of highly accelerated wafer-level GOI tests. Issues relating to the reliability testing of ultra-thin oxides are discussed with examples.

Keywords: silicon oxide, reliability, accelerated stress tests, gate oxide integrity, dielectric breakdown

INTRODUCTION

Continued scaling of gate dielectric thickness for advanced CMOS technologies raises serious reliability concerns for ultra-thin oxides. Excessive leakage current and soft breakdown exhibited by ultra-thin dielectrics present new challenges for reliability characterization.

Device breakdown detection becomes very difficult as oxides become thinner due to soft or quasi-breakdown modes. The failure criteria used in traditional reliability tests must be modified to allow for dependable and robust detection of breakdown. This paper discusses the difficulty in obtaining reliability parameters for ultra-thin SiO_2 films.

Specifically, Section II discusses corrections necessary for estimating the oxide electric field in ultra-thin films. Section III presents examples of soft breakdown in several common breakdown tests and discusses new breakdown detection algorithms. The validity of a common metric in reliability characterization, charge-to-breakdown, is discussed in Section IV.

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Section V discusses reliability projections based on the results of highly accelerated breakdown tests. Finally, conclusions are given in Section VI.

DETERMINATION OF BREAKDOWN ELECTRIC FIELD

Determining the correct oxide electric field can be difficult for ultra-thin films due to excessive leakage current, gate electrode depletion and quantum effects.

A dominant feature of ultra-thin dielectrics is the presence of excessive leakage current at lower electric fields. This leakage is due to quantum mechanical "direct" tunneling and can become significant and be in excess of several A/cm^2 near device breakdown [1]. Figure 1 shows the tunneling current characteristics for a 3 nm, 5 nm, and 10 nm thick SiO_2 film. Note that the low-field direct-tunneling current is substantial for the 3 nm thick oxide.

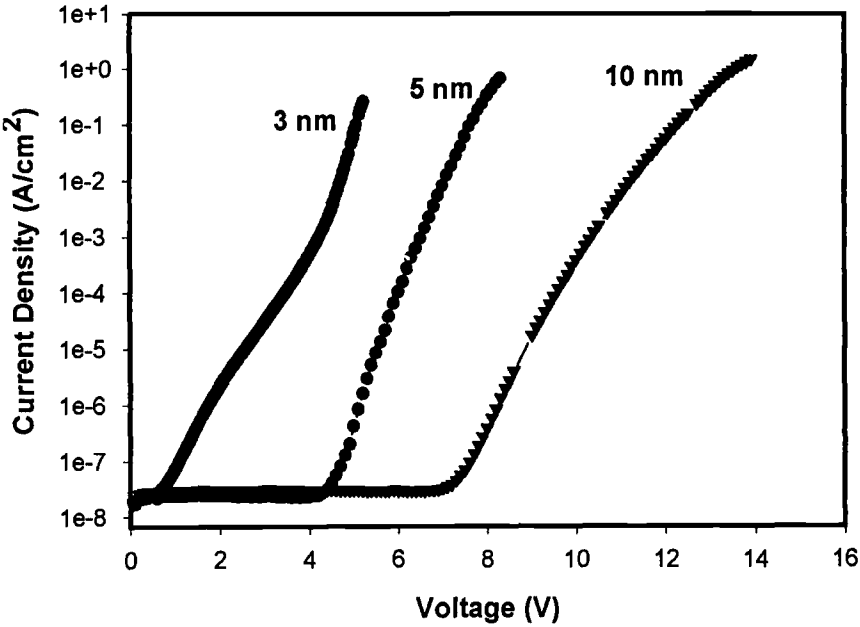

Figure 1- *Tunneling current versus voltage characteristics for a 3 nm, 5 nm, and 10 nm thick SiO_2 film. Note the substantial leakage current exhibited by the 3 nm film due to direct tunneling.*

Special care should be exercised when designing oxide test structures to reduce series resistance effects. The voltage drop across interconnects and gate electrodes due to excessive tunneling currents can be significant leading to an underestimation of gate electric field. Voltage drops can become large enough that the device breakdown voltage

is not achieved during the breakdown test. This is a particular concern for large-area test structures that can conduct significant levels of current before breakdown.

Other factors that can lead to incorrect estimates of oxide electric field include gate electrode depletion and quantum mechanical effects. The voltage applied across the gate can be divided into three components: the voltage drop across the gate-electrode depletion region, the gate oxide, and the quantum confinement region near the $Si\text{-}SiO_2$ interface. There is a variety of software codes and procedures available to estimate the oxide electric field when the above effects are significant and have been shown to yield similar results [2-4].

BREAKDOWN DETECTION IN GATE OXIDE INTEGRITY TESTS

Perhaps, the largest difficulty in conducting breakdown tests on ultra-thin oxides is the detection of the breakdown event. This event is usually described as a sudden decrease in voltage in the case of a constant-current test or a sudden increase in current in the case of a constant-voltage test. "Soft" or "quasi" breakdown modes are frequently observed when testing oxides thinner than 5 nm. This is illustrated in Fig. 2 which shows the voltage versus time characteristics for a 3, 10, and 20 nm oxide subjected to the Joint Electron Device Engineering Council (JEDEC) bounded current ramp test. Note that there are sudden and abrupt decreases in the gate voltage for the 10 nm and 20 nm thick films. However, the 3 nm thick film exhibits only a slight decrease in voltage. It is not clear where the actual breakdown occurred.

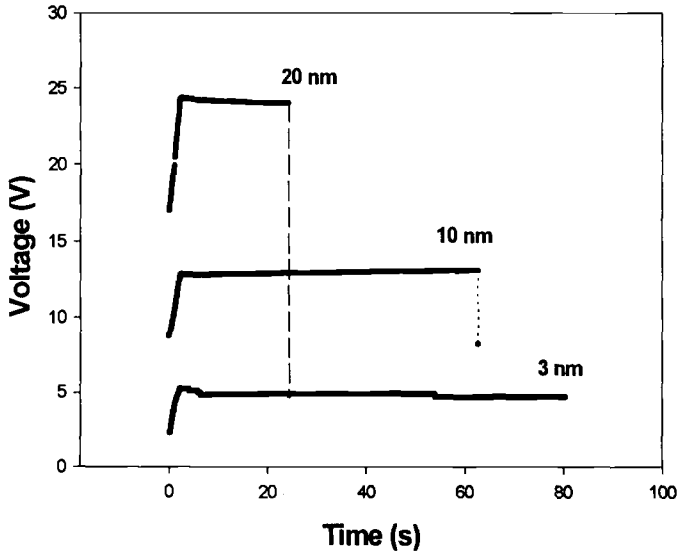

Figure 2- *Voltage versus time characteristics for a 3 nm, 10 nm, and 20 nm thick oxide subjected to a bounded-current ramp test. The current is ramped*

and held at 0 .25 A/cm^2. Breakdown is easily detected in the 10 nm and 20 nm thick films. The 3 nm thick film shows only a slight decrease in voltage making breakdown detection difficult. The device area is 5 x 10^{-4} cm^2.

Similar soft breakdown behavior is observed in constant-voltage tests illustrated in Fig. 3. The figure shows current versus time characteristics for a 3, 5, and 10 nm thick oxide subjected to a constant electric field of 13 MV/cm. The sudden increase in current is clearly observed for the 10 nm thick sample. However, breakdown is observed as a

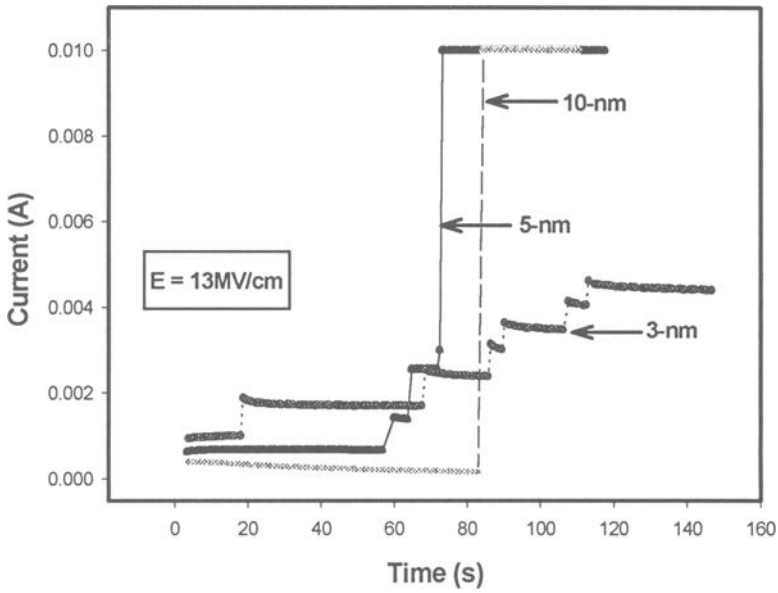

Figure 3- *Current versus time characteristics for a 3 nm, 5 nm, and 10 nm thick oxide subjected to a constant electric field of 13 MV/cm. Device breakdown exhibited by a sharp increase in current is clearly observed for the 10 nm thick sample. The 5 nm and 3 nm thick samples only show a series of small steps in current. The device area is 5 x 10^{-4} cm^2.*

series of small steps in current for the thinner films. JEDEC and American Society for Testing and Materials (ASTM) recently modified the voltage ramp test to utilize a change in slope as the breakdown criterion [5]. Earlier versions used an absolute current change or percent current change as the breakdown criterion. The ramp test is illustrated in Fig. 4 for three different oxide thicknesses. Breakdown is clearly observed for the 5 nm and 10 nm thick samples and can easily be detected by existing breakdown criteria. Note that breakdown is not evident in the 3 nm thick sample.

Figure 5 shows the slope ratio ($\Delta I(n)/\Delta V(n)$)/($\Delta I(n-1)/\Delta V(n-1)$) versus ramp voltage for the 3 nm sample. Note that a 3X increase in slope would be adequate to detect breakdown in this case.

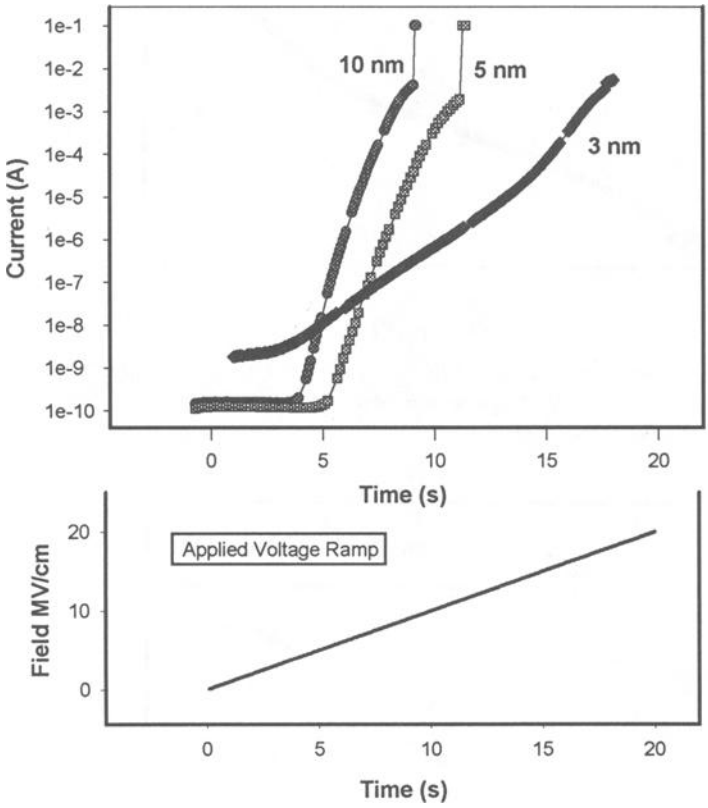

Figure 4- *Current versus voltage characteristics for a 3 nm, 5 nm, and 10 nm thick oxide subjected to the JEDEC/ASTM ramped voltage breakdown test. Breakdown in the 3 nm sample cannot be observed and requires a new criterion for detection.*

The process of evaluating the reliability of ultra-thin oxides on large area test structures is a particular concern. The structures can conduct significant current levels approaching the capabilities of the test system before failure. Breakdown detection can be difficult in this case since the difference between the current at breakdown and the tunneling current can be very difficult to detect. This is illustrated in Fig.6 which shows a figure identical to Fig.5, but the device has a larger area of 1×10^{-2} cm^2. In this case a 3X change in slope is not adequate to detect breakdown. Even if the change in slope ratio is reduced it is not clear where breakdown occurred.

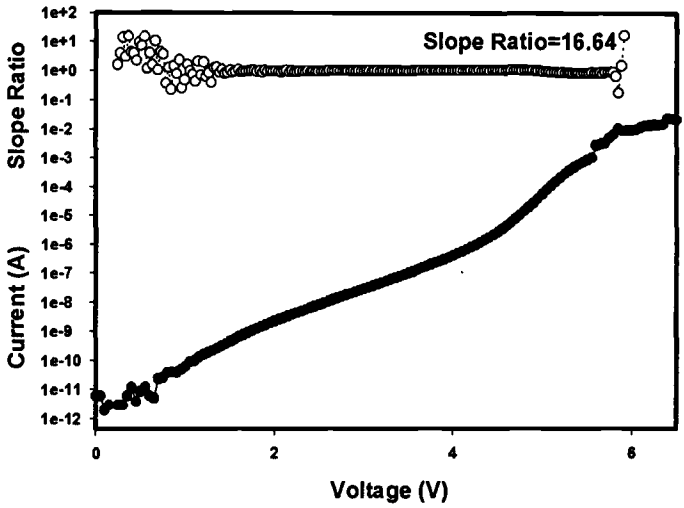

Figure 5- *Slope change ratio versus ramp voltage for a 3 nm thick oxide. Note that a 3X change in the slope would be adequate to detect breakdown. The device area is 5 x 10^{-4} cm^2.*

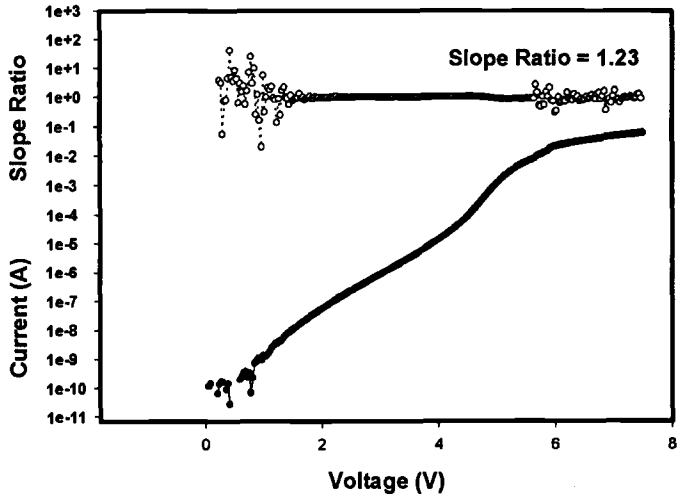

Figure 6- *Slope change ratio versus ramp voltage for a 3 nm thick oxide similar to Fig.5. In this case the device area is 1 x 10^{-2} cm^2. Note that a 3X change in the slope never occurs during the test.*

Figure 7 illustrates the effect a larger device area has on detecting failure during a bounded-current ramp test. The test is the JEDEC standard current-ramp test with a holding current of 0.25 A/cm. The bottom figure shows the voltage versus time characteristic for a 3 nm oxide with a 5 x 10^{-4} cm^2 area. Note that breakdown can be detected by the JEDEC failure criterion of 10% to 15% decrease in voltage.

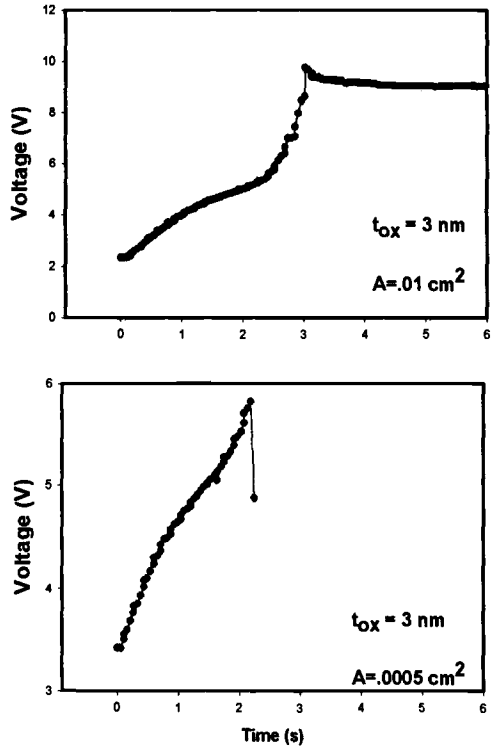

Figure 7- *Voltage versus time characteristic for the JEDEC J-RAMP test performed on a 3 nm oxide having an area of 1 x 10^{-2} cm^2 (Top) and an area of 5 x 10^{-4} cm^2 (Bottom). Breakdown is detected when the voltage across the oxide drops by 15%. Note that there is no voltage drop for the larger area device shown in the top figure.*

The top figure depicts the same oxide with an area of 1 x 10^{-2} cm^2. Note that there does not appear to be an abrupt drop voltage during the test. "Soft" or "quasi" breakdown has been explained as charge trapping and de-trapping in a physically damaged region near the Si-SiO_2 interface [6] or multiple tunneling paths caused by electron traps [7]. Another explanation is that the energy stored on the gate of an ultra-thin oxide (CV^2) is not large enough to cause a thermal destructive breakdown [8].

Recent studies have shown that soft breakdown is usually accompanied by current or voltage noise [9,10]. In fact, oxides thinner than 2.6 nm only exhibit noise when breakdown occurs [10]. Post-breakdown noise can increase by 5 orders of magnitude while pre and post current-voltage characteristics are nearly identical [11]. The monitoring of voltage or current noise to detect breakdown has been suggested as a new breakdown criterion in reliability tests [11,12]. This technique has been shown to be easily implemented in an automated testing environment [12]. Such a technique could possibly be used to detect breakdown in the examples shown in Figs. 6 and 7b.

It has been shown that soft breakdown in ultra-thin gate oxides does not immediately cause device failure (an increase in a metal-oxide-semiconductor field-effect transistor, MOSFET, offstate current) and is dependent on channel length and width [13].

THE VALIDITY OF CHARGE-TO-BREAKDOWN

Charge-to-breakdown (Q_{bd}) is one of the most common metrics used to monitor the integrity and reliability of thin-gate oxides. Q_{bd} can be obtained from any constant or ramped voltage/current breakdown test by integrating the current flowing through the dielectric until it fails. This procedure is illustrated in Fig. 8.

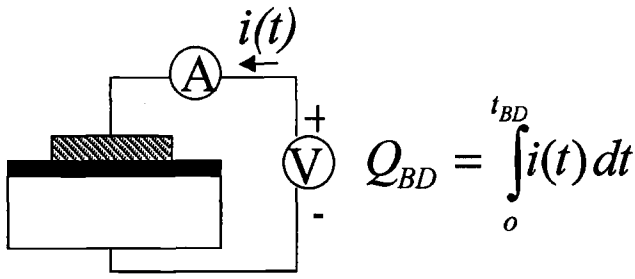

Figure 8- *Schematic of oxide breakdown test illustrating the calculation of charge-to-breakdown.*

Larger values of Q_{bd} are assumed to indicate more reliable and higher integrity dielectrics. Special care must be used when interpreting this value for ultra-thin dielectrics. It has been reported that Q_{bd} exhibits a dependence on stress current density [14,15]. This dependence on current density is observed to become greater as the oxide thickness is decreased [16]. Figure 9 shows that the value of Q_{bd} becomes smaller for thinner oxides when the stress current density is large (the right side region of the plot). However, this trend is the opposite for smaller stress current densities (the left side region of the plot). The value of Q_{bd} is independent of oxide thickness for moderate current densities (the center of the plot).

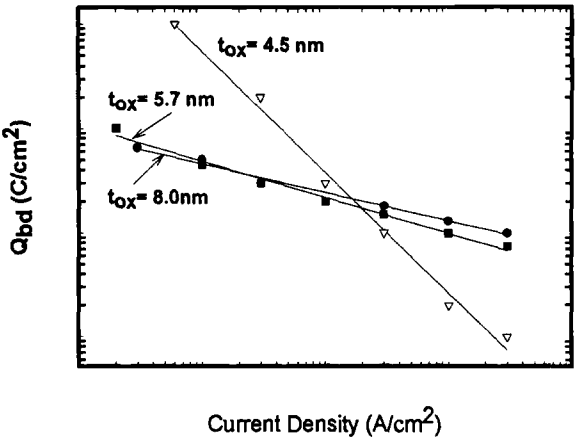

Figure 9- *Data from ref. 16 illustrating the increasing dependence of Q_{bd} on stress current density as oxide thickness is decreased.*

It has been observed that the value of Q_{bd} exhibits a dependence on test structure area. Q_{bd} decreases as the gate area increases. This dependence results from the localization of the breakdown spot and the statistical distribution of the location of this spot over the oxide gate area. Larger gate areas have a greater probability of including a breakdown spot. It has been recently reported that this dependence becomes greater as the gate oxide thickness is reduced [17]. This behavior is shown in Fig 10. Note that the value of Q_{bd} can vary up to three orders of magnitude depending on the test structure area for the 4.3 nm thick sample.

The variation of Q_{bd} with area is much less for the thicker films. The slope of the lines plotted in Fig. 10 is directly related to the dispersion of the failure distribution (or the shape parameter beta in a Weibull plot). Thinner oxides are reported to exhibit a larger beta in their Weibull distributions resulting in a larger variation with area [17, 18].

RELIABILITY EVALUATION

The primary motivation for performing accelerated breakdown tests is to monitor gate oxide integrity and quality and to ultimately obtain information that can be used to estimate product reliability in the field. Short-duration constant-current or voltage tests are usually used to obtain acceleration parameters to extrapolate oxide life under use conditions. Recent studies have questioned the use of constant current tests to evaluate ultra-thin oxides. Wu et al. [13] have shown that Q_{bd} or T_{bd} increases with decreasing oxide thickness under constant-current conditions and that the opposite trend occurs under constant-voltage conditions. It has been explained that a lower voltage is required to sustain the same current density in ultra-thin oxides due to the thickness dependence of direct tunneling currents.

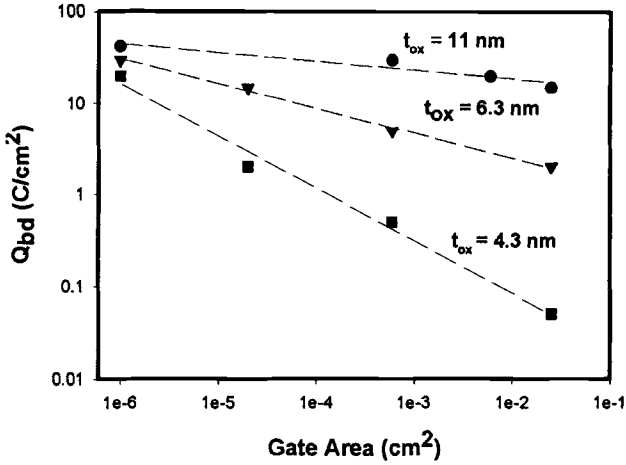

Figure 10- *Data reported in ref. 17 showing the area dependence of Q_{bd} for three different oxide thicknesses. Note that the thinnest oxide exhibits the largest variation of Q_{bd} with area.*

This lower voltage results in a lower electric field or a lower electron energy leading to a smaller defect generation rate. Nigam et al. [17] have also shown that constant current stressing can lead to an incorrect reliability assessment for ultra-thin dielectrics. Their example illustrates that using a constant-current stress (same current density) to evaluate the reliability between two different processes indicated each process had a similar charge-to-breakdown value. Constant-voltage tests revealed that there was a significant difference between the charge-to-breakdown values. It is generally believed that the results from accelerated constant-voltage tests are more accurate when assessing the reliability of thin films since devices operate in this mode during normal use conditions. Also, it has been shown that the $\log(Q_{bd})$ for ultra-thin dielectrics exhibits a linear dependence on gate voltage [19]. This observation suggests an "E" model [20] for breakdown, which predicts that the defect generation is electric field driven or related to the energy of the tunneling electrons, depending on the assumed physical mechanism.

It has been demonstrated that long-term time-dependent dielectric breakdown (TDDB) acceleration parameters can be extracted from any ramped voltage- or current-breakdown test by assuming that oxide damage is cumulative and irreversible during the test and the oxide electric field governs the defect generation [21]. Figure 11 illustrates the technique for a constant current breakdown test performed on a 9 nm oxide. The voltage-versus-time curve is recorded during the breakdown test. The curve can be divided into many smaller stress intervals and each interval removes a small percentage of the total life of the oxide as shown in the figure. The contributions from all of the intervals must add to unity when the device breaks down. Two parameters are required to construct the $\log(t_{50})$ vs. E curve used to extrapolate device life. These parameters are extracted from two distinct voltage-versus-time curves.

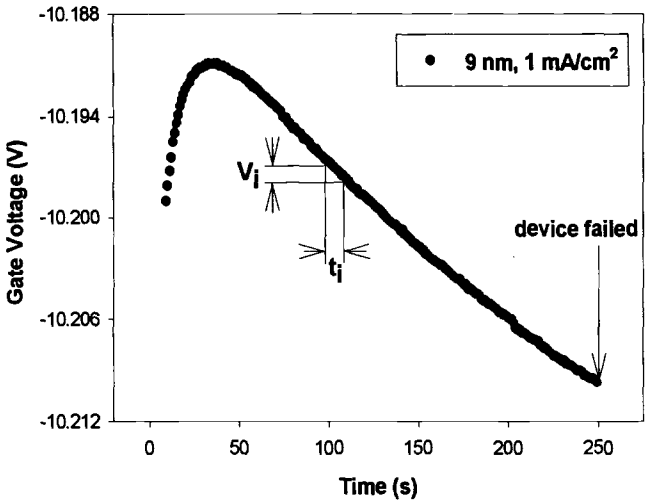

Figure 11- *Voltage-versus-time curve obtained during an accelerated constant current breakdown test for a 9 nm thick SiO_2 film. The figure illustrates the voltage-time integration technique for extracting long-term acceleration parameters from highly accelerated breakdown tests from ref. 21.*

The extracted $\log(t_{50})$ vs. E curve is shown with the actual curve determined from long-term time-dependent dielectric breakdown tests shown in Fig. 12. The agreement is excellent illustrating that the gate voltage or the oxide electric field governs the wear-out and eventual breakdown of thin dielectrics in the 3 nm to 9 nm thickness range.

CONCLUSIONS

The characterization of oxide reliability and integrity becomes more challenging as oxide thickness is scaled down. Soft breakdown modes dominate device failure and make breakdown detection very difficult. Failure detection algorithms in accelerated breakdown tests must be modified for ultra-thin dielectrics. Films thinner than 3 nm may require current or voltage noise detection techniques to detect breakdown.

Special care must be exercised when using charge-to-breakdown as a measure of device reliability. The value of Q_{bd} is a function of device area and current density. These dependencies become stronger as the oxide thickness is scaled down.

Constant-voltage tests are preferred when characterizing wear-out and time-dependent dielectric breakdown of ultra-thin dielectrics. This is due to the observation that defect generation is proportional to the gate voltage, and constant voltage is a more realistic stress condition.

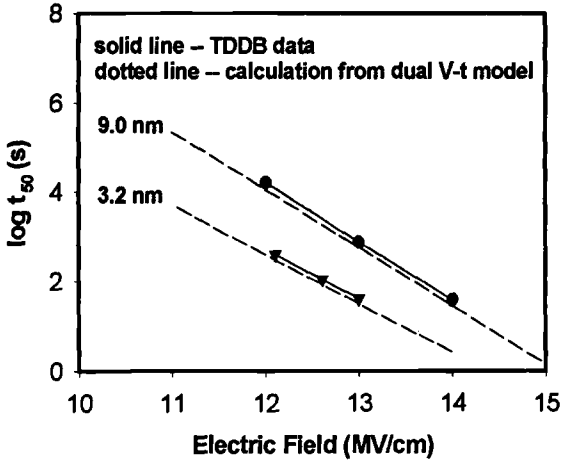

Figure 12- *Extracted log(t_{50}) vs. E curve using the technique in ref. 21 and compared to the actual curve obtained from time-dependent dielectric breakdown measurements.*

The log(t_{bd}) is observed to be linearly dependent on the oxide electric field, which is an important consideration when extrapolating device lifetime at use electric fields from accelerated stress conditions.

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Alvin Strong[1]

Voltage Step Stress for 10 nm Oxides

Reference Block: Strong, A., **"Voltage Step Stress for 10 nm Oxides,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382, D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.*

Abstract: The advantages and challenges of a voltage step stress technique using time dependent dielectric breakdown (TDDB) as the metric are discussed for oxides in the range of 10 nm. A brief comparison is given between life stress and step stress results for oxides on the order of 10 nm. Reference is made to a more complete comparison between life stress and step stress as well as to some of the literature in which step stress changed the outcome of the life stress. Some of the challenges for thinner oxides are discussed, especially oxides of thickness less than 5 nm. An example of the step stress analysis technique is discussed on a point-by-point basis.

Keywords: step stress, gate oxide, semiconductor, TDDB

Advantages

There are two main advantages to using a step stress technique. The first advantage is a theoretical advantage. Step stressing offers the most complete and perfect sample homogenization scheme possible. That is, all of the hardware from each process lot and wafer are equally represented in all of the stress cells. Each stress cell is assumed to be uniformly at a single set of conditions. Thus any lot or wafer dependence is equally represented in each stress cell, so that conclusions are not influenced by wafer or lot distribution inequalities in a given stress cell.

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The second advantage is a practical advantage. Step stressing requires fewer samples for the same number of fails. The largest sample in a constant voltage stress would be in the lowest voltage cell. The second lowest cell would have the next largest sample, etc. In the step stress case, only the sample of the lowest condition cell is required since it will be stepped to all of the higher voltages. This does require a somewhat longer time; however, the lowest cell also requires the longest time step.

Additional Considerations

Although we have achieved excellent agreement between constant life stress and step stress results [*1*], others have reported that in some cases, a low early constant stress, has caused the following higher stress to predict a longer TDDB life than if only the higher stress were used [*2*]. The two experiments were not identical and no attempt has been made to understand the two sets of results. The difference may be in the details of the voltage conditions used, the time on stress, or the oxide quality. In any case, the reader needs to be aware of that body of work as well.

We have step stress experience only for relatively thick oxides of 10 nm and thicker. The methodology must be verified again if the technique is to be considered for significantly thinner oxides. For oxides thinner than 5 nm, Stressed Induced Leakage Currents are of concern and this phenomenon must also be considered in the analysis.

Even for oxides of 10 nm and thicker, the data is more difficult to interpret than simple life stress data. However, with care, it can be interpreted and the benefits outweigh this disadvantage.

Experimental Results

A large sample of approximately 2000 chips were used in this experiment for a 13.5 nm oxide. A voltage screen of 5 volts was used to screen time-zero fails. The constant life stress was done at 8.5 volts for about 3000 sec. The step stress conditions were as follows: 6.5 volts for 1800 sec, 7.5 volts for 1200 sec, and 8.5 volts for 600 sec. The results are shown in Figure 1. The step stress modeling has already been done and only the modeled step stress data and the constant voltage data are plotted in Figure 1. Excellent agreement is shown between the step stress and the constant stress especially for the longer times. Larger sample sizes usually yield results that are easier to interpret.

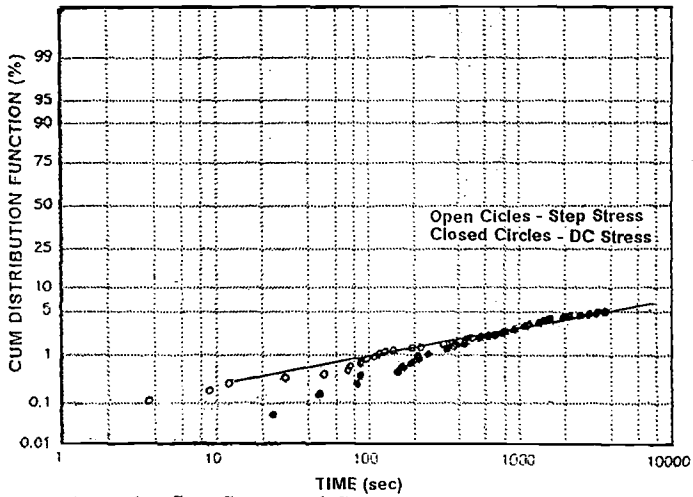

Figure 1 – *Step Stress and Constant Life Stress Comparison*

Step Stress Analysis Technique

A simulation will be used to provide an example to explain the analysis technique. This simulation is based on typical distributions but does not represent any single set of results and is meant only as an instruction vehicle.

The first step is to design the step stress voltages in such a way that there is reasonable separation between failure distributions for of the voltage steps. The experimental design will be checked during the analysis.

After the data is taken, plot cumulative fails versus time on a Weibull chart for each voltage step. Assume that the beginning of each voltage step starts at "zero" time, so that the plot at this point is no different than if a number of constant life stresses were done and plotted.

Although in principle, this technique can be used either for the extrinsic or intrinsic dielectric breakdown regions, it is most useful for the extrinsic region since large sample sizes are required to accurately predict dielectric behavior in this region. If a large range of voltages, or a long time is used, both the extrinsic region and a part of the intrinsic region may emerge. Obviously in this case the regions must be separated and only one region treated at a time.

Acceleration may be calculated using the model of choice. The example here assumes an "E" model, for which T_{acc}=exp (r ΔE), where T_{acc} is time acceleration between two conditions, r is the acceleration factor between those two conditions, and ΔE is the electric field difference between the two conditions.

The fails are shown in Figure 2 for all three cells. A sample size of 300, and a stress time of 2000 seconds for the lower two cells was assumed. The fields during the stress were assumed to be 4 MV/cm, 5.5 MV/cm, and 7 MV/cm. The decade in which the first fails occur depends on the sample size and the time resolution of the measuring system.

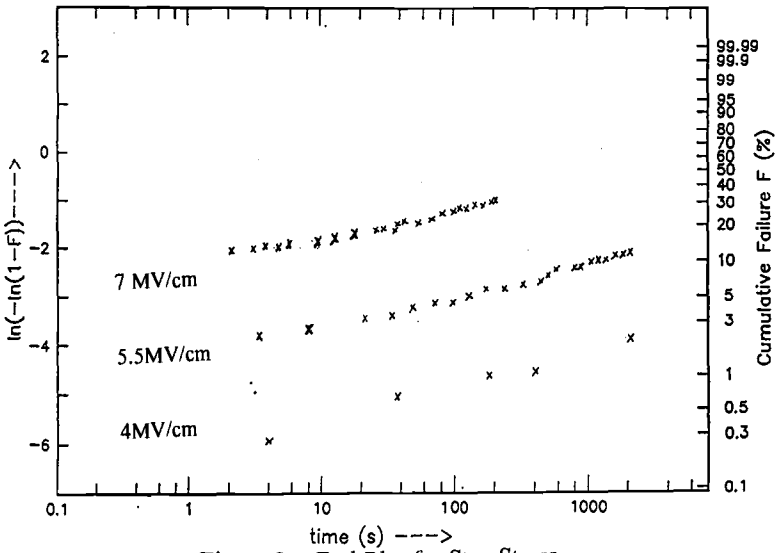

Figure 2 – *Fail Plot for Step Stress*

The curve fitting program should force the slopes of the lines for the different stresses to be equal in the case of the "E" model. The part of the curve which is used to determine the slope of the line is that portion for the longer stress times. In addition, the lowest voltage curve typically has a limited number of fails so it does not necessarily accurately reflect the slope. The fitted lines for the plots are shown in Figure 3.

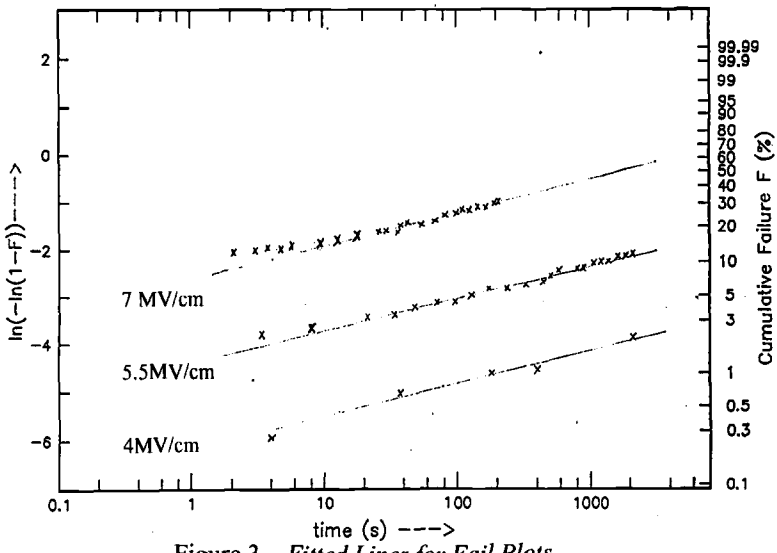

Figure 3 – *Fitted Lines for Fail Plots*

Again to emphasize the point, the line is fitted to the last 1 to 1.5 decades of the data. T_{acc} is measured as the difference between each of the cumulative distribution function (cdf) lines. Since they are parallel, it does not matter what value of cdf is used for the calculation. The result is shown in Figure 4. The acceleration, T_{acc}, is 403 in both cases. The acceleration factor r is then calculated from $r = \{\ln(T_{acc})\} / \Delta E = \{\ln(403)\} / 1.5 = 4$ cm/MV.

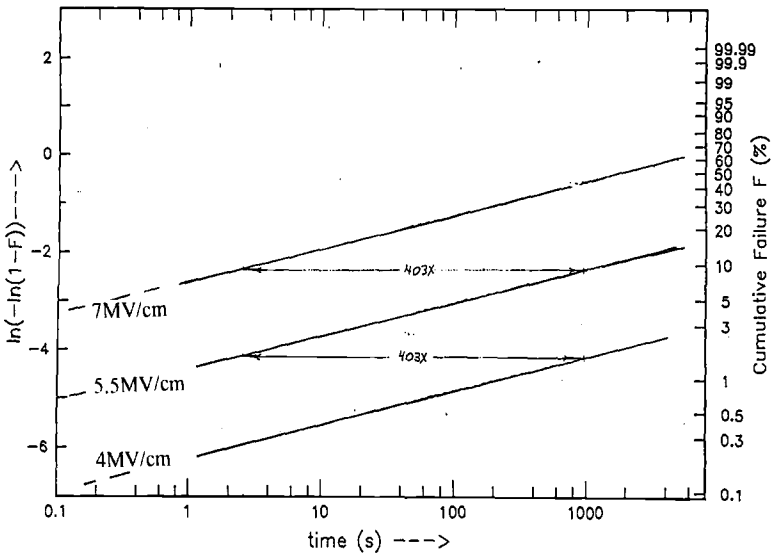

Figure 4 – *Accelerations Shown for Step Stress*

In most cases this completes the analysis of the step stress.

If the data is limited, with only a few early fails, and the early fail points are crucial for the determination of the slope, then it may be necessary to iterate once to refine the acceleration calculation.

In the case above, all points are incorrect by the total stress time of the previous stress divided by the acceleration, ie 2000 sec / 403 = 4.96 sec. For those points before 10 sec, a 5 sec time adder makes a large difference in the position of the point, and for those points before 40 sec, it makes some difference. These corrections are shown in Figure 5. If the slope of the lines were to change with these corrections, a new slope through the points should be drawn and the calculations redone.

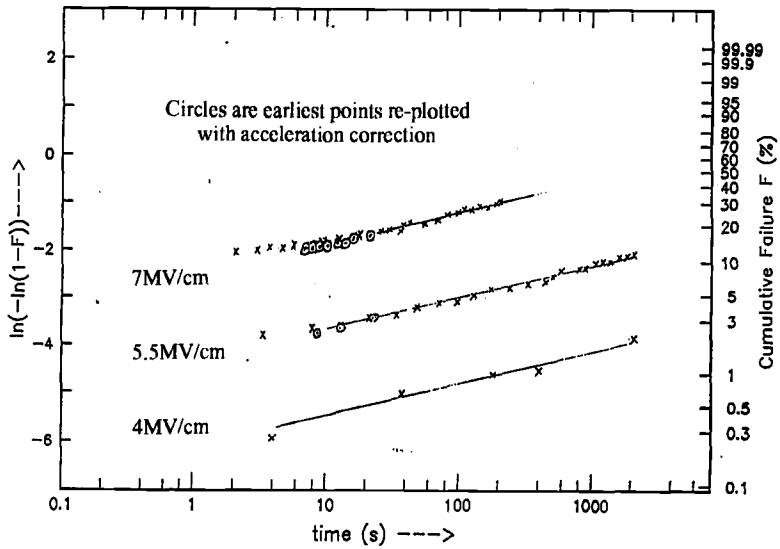

Figure 5 – *Step Stress Plotting Point Correction*

Summary

The real advantages of step stressing include sample size minimization and homogenization. With some care in the final data analysis, these advantages may be realized. The technique must be verified for use on oxides below 5-10 nm.

Acknowledgment

The author gratefully acknowledges R. Vollertsen for generating the simulation.

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Gennadi Bersuker[1] and James Werking[1]

Localized Charging Damage in Thin Oxides

Reference: Bersuker, G., and Werking, J., **"Localized Charging Damage in Thin Oxides,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382,* D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: In the proposed model, breaking of the oxide chemical bonds is assumed to result from the combined effect of electric field and electron fluence in the oxide during electrical stress. Collision between the injected electron and oxide atoms may excite the bond to an unstable electronic state that can lead to the formation of a structural defect. Electric field polarizes, and thus weakens the defect bonds causing bond breakdown. The model describes charge–to-breakdown dependence on electric field, temperature and oxide thickness. The difference in positive and negative gate bias charge-to-breakdown data is attributed to the presence of the structural strained layer at the Si/SiO2 interface. This approach is used for analysis of the effects of process induced charging stress on transistor parameters. It is shown that leakage current may increase or decrease with oxide thickness depending on the magnitude of the stress induced charging damage.

Keywords: charge-to-breakdown, trap generation, stress induced leakage current, plasma damage, antenna transistors, thin oxide damage, oxide breakdown model

Introduction

Scaled devices require thinner gate oxides, and it is therefore important to estimate how such scaling may affect oxide susceptibility to process-induced charging stress. Changes in the oxide electrical parameters are a manifestation of some stress-induced physical changes in the oxide structure - formation of oxide traps. It is generally assumed that these physical changes involve chemical bond breaking in the oxide. Therefore, the bond breaking process is of primary interest for understanding the effects of stress on the oxide electrical properties.

The temperature and electric field dependence of oxide electrical breakdown indicates that bond breaking most likely occurs on weaker bonds associated with defects in the SiO_2 structure, in particular oxygen vacancies. These defects may exist in the oxide prior to the electrical stress, or be created during the stress. In the proposed model, breakdown precursor defects are considered to be created by collisions of injected electrons with oxide atoms. It is shown that the stress induced defect formation process is responsible charge-to-breakdown dependence on oxide thickness. This approach

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describes the physical mechanisms of the bond breaking process; including the effect of electric field, temperature and electron collision probability. The model is used to explain positive and negative bias charge-to-breakdown data, as well as to understand process-induced charging damage effects on transistor parameters.

Localized Model for Bond Breakdown Process

In the proposed model we assume that whatever the nature of the oxide traps induced by electrical stress, the trap generation is triggered by the breakdown of chemical bonds. In general, oxide under electrical stress experiences influence of both an electric field and electron fluence. During electrical stress bond breakdown may be considered as a two step process – bond excitation by a collision with an injected electron and subsequent bond breaking assisted by temperature and electric field. Collisions of the injected electrons with oxide atoms may result in the formation of the structural defect in the oxide while polarization of the weak defect bonds by the electric field leads to the bond breakdown. These effects are discussed in more detail below.

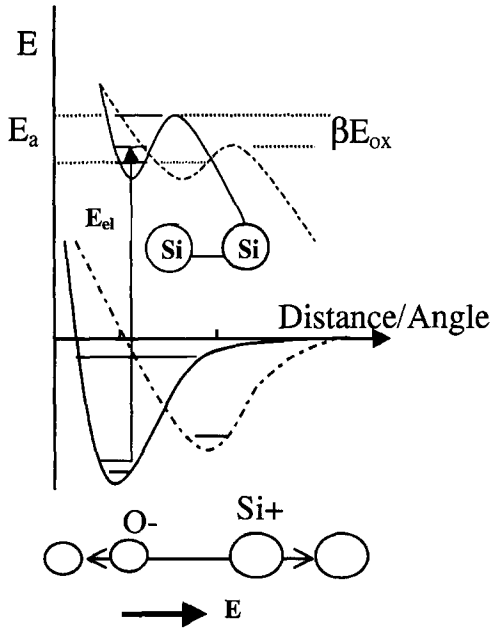

Figure 1 - *Dependence of the bond energy on the bond length with (broken line) and without (solid line) applied electric field for different local structural configurations.*

In order to consider electric field effects on oxide susceptibility to charging stress, we first briefly discuss energy properties of the individual bonds. Dependence of the bond

energy on the bond length (or angle) is presented qualitatively in (Fig. 1). In the ground electronic state, the minimum of the bond energy defines the equilibrium distance between the atoms in a regular SiO_2 structure. Raising the temperature leads to population of excited vibrational states in the energy well, and increases the amplitude of their atomic vibrations. If the crystal temperature is increased to such values that the energy states near the top of the well are populated, the atom displacements become so large that bonds start to break. This manifests itself in crystal melting. Thus, bond breaking probability P can be described by the Boltzmann expression: $P = \exp(-E_a/kT)$ where E_a is the bond activation energy for the given electronic state (ground or excited) corresponding to the particular local atomic configuration in SiO_2.

Electric field applied to the dielectric shifts the positions of the positively and negatively charged ions in opposite directions, thus increasing the interatomic distance in the bond. Changes in the bond length translate into a shift in the position of the minimum of the potential energy curve (Fig. 1) and makes the energy minimum more shallow. This means that the bond energy is decreased. In the case of a simple ionic bond, in the harmonic oscillator approximation, the change in the bond energy, ΔE, is equal to $\Delta E = q \times E_{ox} \equiv \beta E_{ox}$, where q is the effective ion charge, x is the change in the interatomic distance, and E_{ox} is the electric field acting along the bond. Detailed analysis of polarization effects on SiO_2 is done in [*1*] where it is shown that the local electrical field acting on the bond might be significantly stronger than the applied field. Thus, the probability of bond breakdown in the presence of electric field takes the following form:

$$P_E = e^{-(E_a - \beta E_{ox})/kT} \tag{1}$$

To discuss the effect of electron fluence on the bond breaking process we first note that even at low temperatures there is non-zero probability of "spontaneous " bond breaking due to excitation of a valence electron (by light, γ-radiation, etc.) from the bonding to an anti-bonding orbital. Collisions with the electrons injected during electrical stress play similar role. Electrostatic interaction with the injected electron can excite the electron resided on the bond that destabilizes the bond atomic configuration. This instability may lead to creation of a structural defect. For instance, excitation to the unstable electronic state of the Si-O-Si bond can cause oxygen departure and subsequent formation of Si-Si bond. The energy required for the defect formation varies depending on the local stress conditions and generally does not exceed 4.5 eV. In the case of Si-O-Si bond, this energy weakens with the deviation of the Si-O-Si angle from 144°.

As was mentioned above, the oxygen vacancies which seem to be a likely breakdown precursor can be formed due to electron collisions during electrical stress as well as prior to the stress, for instance at the oxide growth stage. The oxygen vacancies created during electrical stress are characterized by much longer Si-Si distances (3.1 A vs.2.5 A), and correspondingly lower bond energies than the vacancies resulting from the synthesis process [*2*]. The fact that the activation energies estimated from electric field

dependence of the time to dielectric breakdown [*1, 2*] is lower than theoretical estimates (1.15 eV and 1.8 eV, respectively) indicates the importance of the electron-oxide collision process for the understanding of the oxide breakdown.

When the oxide thickness is significantly larger than the electron mean free path in the oxide t_0, each injected electron may experience multiple collisions with oxide atoms. When oxide thickness approaches the electron mean free path value, the electron-oxide collision probability reduces. Thus, in the case of thin oxides, when an injected electron may experience a single collision at most, a collision probability for an electron traveling distance t in the oxide can be written as follows (analogously to the absorption coefficient):

$$N = 1 - \exp(-st) \tag{2}$$

where s is the electron collision probability per unit traveling distance in SiO_2. The parameter s is a function of the oxide density, crystal structure irregularities, presence of charge centers, etc. Then, the probability of the electronic transition to the defect state is proportional to the probability of an electron-bond collision at a distance t, dN/dt, and electron kinetic energy $E_{el} = E_{ox}$ t (since higher electron impact energy allows for such transitions to occur on stronger bonds thus increasing a number of bonds which can be affected by the given electron).

The total probability for an electron to break a bond in a single collision can be expressed as a multiple of the probabilities of the transition to the defect state and breakdown of this defect bond assisted by temperature and electric field, P_E in Eq. (1):

$$P(t) \propto P_E \cdot E_{el} \cdot \frac{dN}{dt} = P_E \cdot E_{ox} t \cdot s e^{-st} \tag{3}$$

Here electrons are assumed to be moving in a ballistic regime, and we neglect the probability of a spontaneous bond breaking at room temperature. Integrating over the total oxide thickness t_{ox} one obtains the probability of bond breaking per one injected electron passing through the oxide:

$$P = \frac{1}{s} E_{ox} \left[1 - (1 + st_{ox}) e^{-st_{ox}}\right] \cdot e^{-(E_a - \beta E_{ox})} \tag{4}$$

A number of broken bonds per unit area, D, can be described by the following expression

$$D = Q \cdot P \tag{5}$$

where Q is the total electron fluence per unit area passed through the oxide, and P is the probability of the bond breaking in a single collision.

Oxide breakdown occurs when the local trap density D/t_{ox} exceeds some characteristic critical value D_c. The moment of breakdown defines a charge-to-breakdown value, $Q = Q_{bd}$ in Eq. (4). Taking into account the approximately linear dependence of critical trap density D_c on oxide thickness in thin oxides 25 Å < t_{ox} < 80 Å [*4, 5*], $D_c = D_{c0}$ t_{ox} (D_{c0} is the critical concentration in the very thin oxide $t_{ox} < t_0$), from Eqs. (1-5) one can obtain the following dependence of the charge-to-breakdown Q_{bd} on the electric field and oxide thickness:

$$Q_{bd} = A\frac{e^{-(\beta E_{ox}-E_a)/kT}}{E_{ox}}\cdot\frac{D_0 s t_{ox}^2}{1-(1+st_{ox})\exp(-st_{ox})} \qquad (6)$$

where A is a dimensional constant of proportionality. Here for simplicity we neglected dependence of critical trap density on electric field [*6*]. In the tunneling oxides, D_c is independent from the oxide thickness that leads to the replacement of the term t_{ox}^2 in the Eq.(6) denominator with t_{ox}.

One can see from Eq. (6) that both electric field and electron fluence contribute to the trap generation process. Electric field causes polarization and subsequent weakening of the chemical bonds (described by the term $\exp(-\beta E_{ox})$ in Eq. (6)) in agreement with the E_{ox} model experimentally confirmed recently [*7*]. Additional $1/E_{ox}$ electric field dependence originated from the effect of electron acceleration by the electric field (that increases the probability of creation of defect bonds during electron-oxide collisions) leads to the Q_{bd} singularity at very low E_{ox}. This singularity reflects the fact that we neglected the presence of the breakdown precursor defects in the oxide. Accounting for these defects adds a term cP_E to Eq.(5) where c is the concentration of the pre-existing breakdown precursor defects per unit area, and P_E is from Eq.(1). Then, the condition under which the density of collision-assisted broken bonds dominates the one of generated on pre-existing defects only takes the form: $c_0 < D_c/P_E$ where $c_0 \equiv c/t_{ox}$ is the density of the pre-existing defects in the oxide. As one can see, relative share of the bonds broken only by the electric field (without collisions) increases with field and temperature and depends on oxide thickness ($D_c \propto t_{ox}$) and quality determined by c_0 value.

Eq.(4) can be modified if formation of a breakdown precursor defect requires some minimum energy E_{th}. In order to create a defect an incident electron should be accelerated to a threshold energy $E_{ox}\, t_{th} = E_{th}$. . In this case, bond breaking probability P takes the form:

$$P = \frac{1}{s}E_{ox}\left[1-\{1+(st_{ox}-t_{th})\}e^{-s(t_{ox}-t_{th})}\right]\cdot e^{-st_{th}}\cdot e^{-(E_a-\beta E_{ox})} \qquad (4')$$

To analyze thicker oxides, $t_{ox} > t_0$, Eq. (6) can be simplified by completely neglecting the probability of collisions when the distance electrons travel in the oxide is less than the electron mean free path t_0. Then, Eq. (2) transforms into $N \approx 1 - \exp[s(t - t_0)]$, and Eq. (6) takes the form

$$Q_{bd} \approx \frac{2}{3} \cdot \frac{D_0}{sE_{ox}} \cdot e^{-(\beta E_{ox} - E_a)/kT} \cdot \frac{t_{ox}}{t_{ox} - t_0} \qquad (7)$$

Here we assumed that $st_{ox} << 1$. Eq. (7) is valid for the oxide thickness in the range $t_0 < t_{ox} < (2\ t_0/s)^{1/2}$. As follows from Eq. (7), in the given oxide thickness range fewer traps are generated in thinner oxides under the constant current stress (E_{ox} is determined by the current density and independent from the oxide thickness) due to both lower collision probability and electron impact energy.

In order to verify the above $Q_{bd}(t_{ox})$ dependence, we compared oxide thickness t_{ox} calculated with Eq. (7) to the nominal thickness that was measured both optically and electrically. Charge-to-breakdown (hard breakdown) measurements were done on 20x20 um^2 n+ poly NFET capacitors under positive and negative gate bias at 0.5 A/cm^2 constant current stress (Fig. 2).

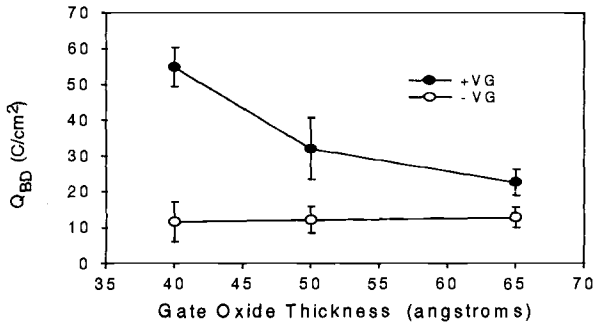

Figure 2 - *Constant current charge-to-breakdown vs. oxide thickness. Error bars correspond to ±1 standard deviation*

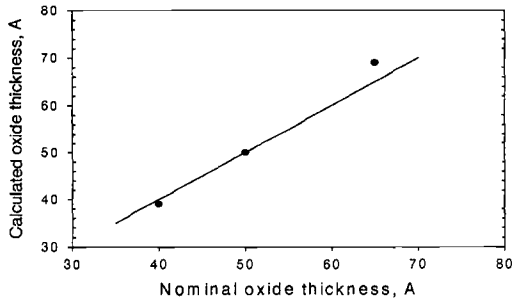

Figure 3 - *Gate oxide thickness calculated with Eq. (8) vs. nominal thickness.*

Using positive bias Q_{bd} data and ratios of Q_{bd} in Eq. (7) for different t_{ox} , we found that the best fit of the calculated oxide thickness to the nominal ones (Fig. 3) can be obtained with $t_0 \cong 30$ Å.

Substrate and Gate Injection Charge-to-Breakdown

So far, the oxide physical characteristics have been assumed to remain constant across the oxide. However, it has been well established that stress at the SiO_2/Si interface results in a structural "strained" layer in SiO_2 [*8,9,10*]. The strained layer is characterized by higher than bulk oxide density (2.4 g/cm^3) and high compressive stress. These lead to increase in the probability of breaking for the bonds weakened by the stress in the strained layer:

$$P_E = e^{-(E_a - \beta E_{ox} - E_{str})/kT} \tag{8}$$

where E_{str} is an average energy of the stress that affects an individual bond.

The existence of the strained layer breaks the symmetry between the positive and negative gate bias injection in the oxides thicker than the electron mean free path. Indeed, in the case of substrate electron injection the mean free path $t_0 \cong 30$ Å covers significant portion of the strained layer, so that E_{str} are expected to be very close to the bulk oxide ones E_{str_sub} (Fig. 4).

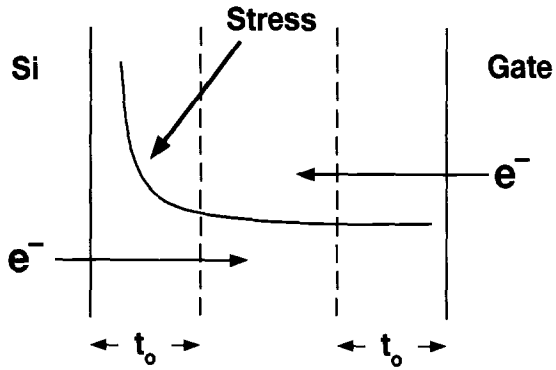

Figure 4 - *Schematics of substrate and gate electron injections vs. distribution of stress in oxides.*

On the other hand, for gate injection, the mean free path distance covers oxide outside the structural strained layer. Therefore, to a great extent, E_{str} in Eq. (8), which represent average of $E_{str}(t)$ over the oxide thickness t_{ox} outside the mean free path distance, is

determined by the structural strained layer properties, and is much greater than in the substrate injection case. Subsequently, in the latter case, Q_{bd} values are greater for all oxide thickness.

In addition, in the gate injection case, E_{str_gate} parameter may exhibit strong oxide thickness dependence: the thinner the oxide, the greater the share of the structural strained layer in the total oxide thickness, and therefore average E_{str_gate} value is higher. Based on the expected behavior of the E_{str_gate} parameter in the gate injection case in the extremely thin and thick oxides, we may propose the following dependence of the E_{str_gate} on oxide thickness: $E_{str\_gate} \approx E_{str\_sub} \cdot t_{ox}/ t_{ox}\text{-}t_0$, where the average value of the stress energy in the substrate injection case, E_{str_sub}, is assumed to be independent from the oxide thickness. Substituting the above E_{str_gate} dependence in Eq. (8), we obtain the following relation between the charge-to-breakdown for gate, Q_{bdg}, and substrate, Q_{bds}, injections valid for oxide thickness $t_{ox} > t_0$:

$$Q_{bds} / Q_{bdg} = e^{-(E_{str\_sub} - E_{str\_gate})/kT} \approx 1 + \frac{E_{str\_sub}}{kT} \cdot \frac{t_0}{t_{ox} - t_0} \qquad (9)$$

We calculated the oxide thickness t_{ox} in Eq. (9) using Q_{bd} values in (Fig. 2) and t_0 = 30 Å. Comparison of the calculated thickness to the nominal ones is presented in (Fig. 5). The fit was obtained with $E_{str\_sub}/kT \cong 1$ that leads to an estimate $E_{str\_sub} \cong 0.026$ eV. Note that other oxide properties, like interface roughness that was not discussed here may also contribute to Q_{bd} values.

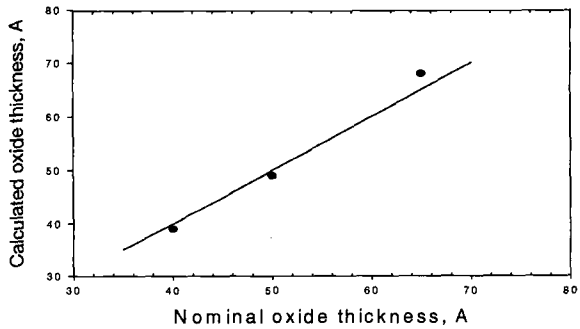

Figure 5 - *Gate oxide thickness calculated with Eq. (9) vs. nominal oxide thickness.*

Process Induced Damage

The trap generation model discussed above was applied to the process induced charging damage evaluation using test structures that contain transistors with attached charge collecting antennas at different wafer processing levels. Charging stress level in the established process is relatively low, and stress generated trap density is usually significantly smaller than required to cause oxide breakdown. The sensitivity of transistor parameters to gate oxide characteristics allows for measurement of relatively low damage that may not show up in device yield.

We analyzed charging damage effects in 0.35 um LDD NMOS transistors with 65 Å, 50 Å, and 40 Å gate oxides (similar effects were observed in the identically processed lot with 65 Å, 55 Å and 45 Å gate oxide splits). Splits for each oxide thickness contain 4 wafers, with 17 die per wafer tested. Poly, metal-1 or full flow charge collecting antennas are attached to transistor gates, with antenna-to-gate ratios (AR) up to 90 K:1. Fowler-Nordheim (F-N) stress, 1 nA/um^2 for 2 sec, was used to reveal latent damage.

The charge damage effect (CDE) induced by processing is measured as a difference in a transistor parameter T shift due to F-N stress between an antenna transistor and a reference transistor at the same die location:

$$\Delta T = \left[T_{stress}(antenna) - T_{no\_stress}(antenna)\right] - \left[T_{stress}(reference) - T_{no\_stress}(reference)\right] \tag{10}$$

Reference devices are protected from charging damage during processing by poly-level fuses between drain, source, gate, and substrate (when fuses are blown the gate oxide is not under stress).

In the case of thin oxide, gate leakage current I_g seems to be a very sensitive damage parameter; it exhibits strong antenna effect in most types of antenna modules even before F-N stress. In metal-1 antenna transistors, I_g increases with antenna size (Fig. 6) and decreases with oxide thickness (Fig. 7). The same trends are observed in CDE of I_g, after the F-N stress (Fig. 8). Transconductance G_m and threshold voltage V_t do not show antenna effect before F-N stress. CDE in G_m and V_t is greater for thicker oxide, especially in devices with edge intensive antennas (Fig. 9). The fact that I_g is reduced after the F-N stress (Fig. 6) indicates that hole-type traps were created in the oxide during metal-1 processing. This conclusion is supported by V_t data (Fig. 9) that show negative shift of V_t with respect to reference transistors after F-N stress, such shift being accompanied by increase of G_m. Devices with poly area antennas show positive CDE of V_t (Fig.10) and no effect in I_g, suggesting that electron-type traps were primarily generated during poly processing.

For tested transistor parameters in metal-1 and poly antenna modules, thicker gate oxides demonstrate greater susceptibility to charging stress (Figs. 6-10) (see [*11*]), in agreement with the model prediction for thicker oxides, Eq. 7. On the other hand, in the

full flow modules that include contact antennas (having up to 39,000 contacts) in addition to area antennas, thinner oxides show higher gate leakage (Fig. 11) (similar results were reported in [*12*]).

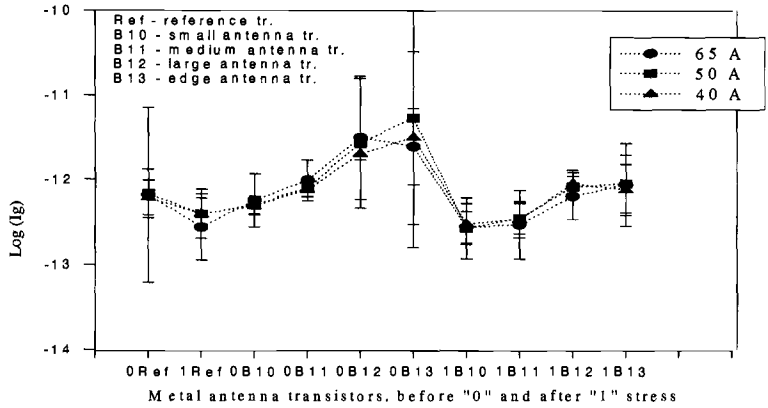

Figure 6 - *Pre- and post-stress gate leakage current for reference and metal-1 antenna transistors. Error bars correspond to ±1 standard deviation. In the x axis, 0 and 1 in front of the transistor type correspond to the data before and after the F-N stress.*

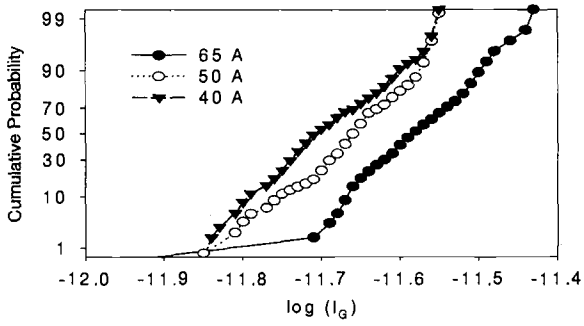

Figure 7 - *Pre-stress gate leakage current of metal-1 large antenna transistors.*

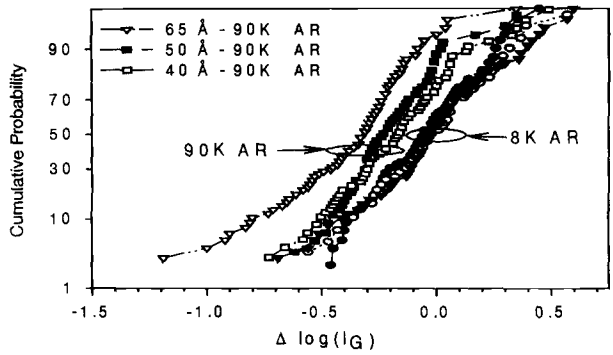

Figure 8 - *Charge damage effect, calculated with Eq. (11), in gate leakage current of metal-1 antenna transistors.*

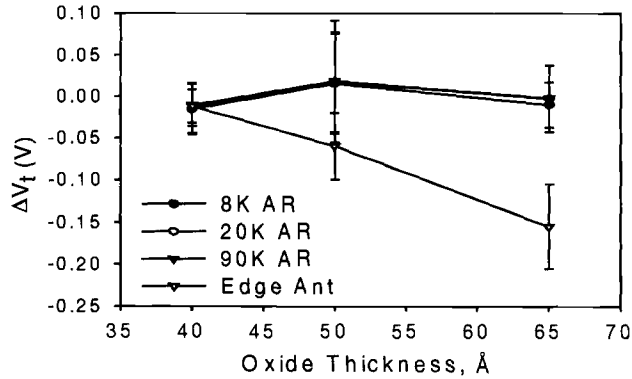

Figure 9 - *Charge damage effect in threshold voltage of metal-1 antenna transistors.*

For tested transistor parameters in metal-1 and poly antenna modules, thicker gate oxides demonstrate greater susceptibility to charging stress (Figs. 6-10) (see [*11*]), in agreement with the model prediction for thicker oxides, Eq. 7. On the other hand, in the full flow modules that include contact antennas (having up to 39,000 contacts) in addition to area antennas, thinner oxides show higher gate leakage (Fig. 11) (similar results were reported in [*12*]).

In this module, gate oxides in antenna transistors are very leaky due to heavy charging damage during processing, as follows from the dependence of I_g on antenna sizes. V_t and G_m show no antenna effect before F-N stress (no data available after the stress due to very high damage in transistors).

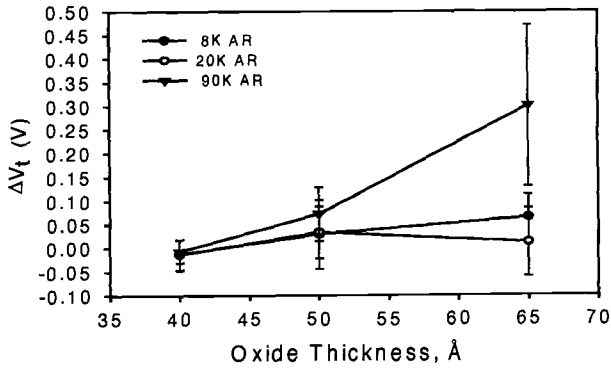

Figure 10 - *Charge damage effect in threshold voltage of poly antenna transistors.*

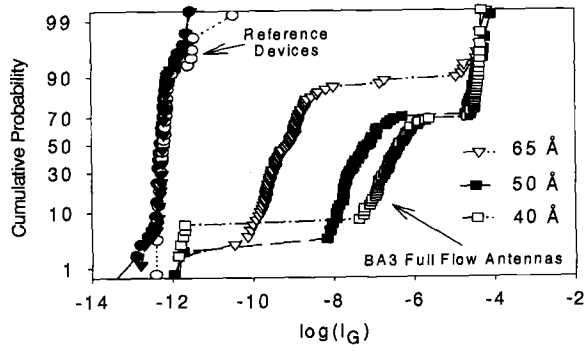

Figure 11 - *Gate leakage current of reference and full flow large antenna transistors.*

Thus, two groups of devices, with lower (metal-1, poly modules) and higher (full flow module) charging damage, demonstrate opposite trends: when total damage is low, thinner oxides show less charge damage effect, however, they seem to be more susceptible to stress in the case of higher damage.

Stress Induced Leakage Current

In order to explain data in the heavily damaged full flow module that seemingly contradicts our model, we need to discuss a leakage current mechanism. Trap assisted

tunneling current is proportional to the density of traps $D_0 = D/t_{ox}$ which can accept electrons and to the probability of electron tunneling from the substrate to these traps W (for simplicity, we assume that in the ultra thin oxides, tunneling via one trap only is required for each electron):

$$j_{TA} = j_0 \cdot D_0 \cdot W \tag{12}$$

where j_0 is the coefficient of proportionality.

In the quasi-classical approximation, electron tunneling probability P can be written as follows: $W \propto \exp\{-\int\sqrt{[E(t)-E_0]}dt\} \approx \exp\{-E_b^{1/2}(\alpha + \beta t)\}$, where E_b and E_0 are the energy barrier at the Si/SiO_2 interface and the initial electron energy, respectively. α and β are coefficients that depend on the electron and barrier energies and on the trap location between the oxide interfaces. In particular, if a trap is in the middle of the SiO_2 layer, $\beta = 1/2$.

As oxide thickness increases, trap assisted tunneling current j_{TA} reduces due to exponential decline of tunneling probability W. However, j_{TA} may also increase with oxide thickness because of increase in the trap density $D_d \propto t_{ox}$ within the approximation used in Eq. (7). (In a general case of Eq. (6), trap density increases with the oxide thickness in a more complex way; note that $t_{ox}s<<1$). To determine dependence of the trap assisted tunneling current on the oxide thickness, we estimated an oxide thickness t_{max} at which trap assisted current is maximum.

Graphical results of these calculations are presented in (Fig. 12). As follows from the equation $dj_{TA}/dt_{ox} = 0$, $t_{max} \propto \gamma/D_0$ decreases with the increase of the trap density D_0, and the parameter γ is a function of E_b, β, and t_0. The value of t_{max} with respect to the oxide thickness under consideration tells us whether leakage current should increase or decrease with oxide thickness. When the trap density D_0 is small, t_{max} may be greater than the maximum thickness of the oxides under consideration, and therefore one observes increase of leakage current as oxide thickness increases (broken line in (Fig. 12)), as we see in metal-1 and poly modules. Decline of current in thinner oxides is due to insufficient number of traps which assist tunneling current, and we term this case damage controlled leakage.

When damage increases (D_0 increases) as in the case of full flow module, t_{max} decreases and may correspond to oxide thickness that is smaller than the minimum thickness of the oxides in our experiment. In such case that can be termed tunneling controlled leakage, one observes decrease of leakage current when oxide thickness increases (solid line in (Fig. 12)), due to smaller tunneling probability W in thicker oxides.

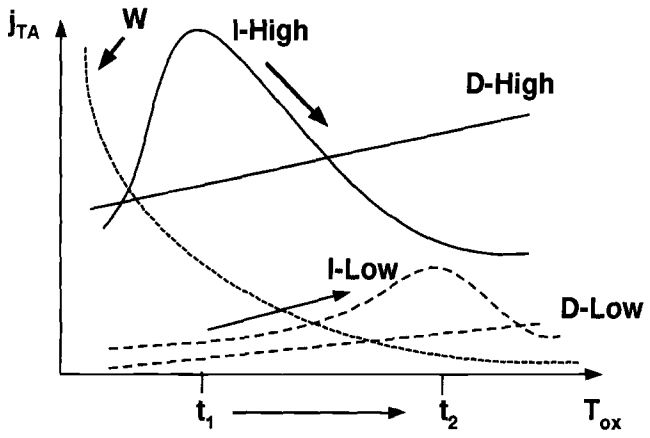

Figure 12 - *Leakage current vs. oxide thickness in the cases of high, D-high, and low, D-low, damage.*

Summary

The proposed model provides a physical explanation for the electric field and oxide thickness dependence of Q_{bd}. It is shown that both electric field and electron fluence contribute to the trap generation process through weakening of the oxide chemical bonds and collisions of injected electrons with oxide atoms, respectively. According to the model, electron-oxide collisions responsible for the creation of the breakdown precursor defects lead to the Q_{bd} oxide thickness dependence. Effectiveness of the defect creation process is proportional to the electron impact energy that results in $1/E_{OX}$ factor in the electric field dependence of Q_{bd}. Experimentally observed $\exp(-E_{OX})$ dependence originates from polarization of the oxide chemical bonds in the applied electric field.

Thinner oxides are less susceptible to charging stress (under identical stress conditions) since both the probability of collisions of injected electrons with oxide atoms and electron impact energy decrease with oxide thickness. However, relatively lower damage in thinner oxides (determined as a concentration of generated traps) may produce a greater effect on oxide quality, in particular on oxide leakage current. Gate leakage current does not directly represent oxide damage after heavy stress. It is found that after heavy stress, leakage current is determined by the probability of trap assisted tunneling, while in lightly damaged oxides the density of generated traps controls leakage.

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Characterization and Applications

Gilbert A. Gruber[1] and Robert J. Hillard[2]

Characterization of Gate Dielectrics with Mercury Gate MOS Current-Voltage Measurements

Reference: Gruber, G. A., and Hillard, R. J., **"Characterization of Gate Dielectrics with Mercury Gate MOS Current-Voltage Measurements,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382,* D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: MOS device performance and reliability depend strongly on the quality of the gate dielectric. Metallic contamination, stoichiometry, interface properties, and substrate quality all have an influence. Gate Oxide Integrity (GOI) measurements are frequently used for monitoring oxide quality and reliability. Conventionally, testing the integrity of these gate dielectrics requires the use of prefabricated polysilicon or metal gate MOS capacitors (MOSCAPs). However, this involves short loop processing that is time-consuming and can itself affect the gate oxide quality. Therefore, a method that can monitor these factors rapidly and accurately for both production and process development is highly desirable. In this paper, a mercury gate is presented for Gate Oxide Integrity (GOI) measurements. This mercury gate is formed using a highly repeatable mercury probe Capacitance-Voltage/Charge-Voltage/Current-Voltage (CV/QV/IV) system. Several applications are discussed that show how these measurements may be used in monitoring a variety of process-induced defects. An example of the application of mercury gate Metal-Oxide-Semiconductor Current-Voltage (MOS IV) measurements for ultra-thin (less than 10 nm) oxide development is also presented.

Keywords: mercury probe, mercury gate, gate dielectric, plasma damage, surface cleaning, metal contamination, ultra-thin oxide

Introduction

The quality of the gate oxide in an Metal-Oxide-Semiconductor (MOS) device is affected by many different defects. These defects include metallic contamination, electron and hole traps, particles, and oxide stoichiometry [*1*]. Gate oxide integrity (GOI) measurements are useful for monitoring oxide quality and reliability. Traditionally, GOI measurements have been made on MOS structures fabricated with metal or polysilicon gates. The problem with these fabricated gates is that they take time, are expensive to

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fabricate, and can interrupt production. Use of an alternate gate electrode that does not require fab processing for GOI measurements is highly desirable. This paper demonstrates the use of a mercury gate for GOI measurements used to characterize dielectric quality; it also shows that mercury gate GOI measurements are sensitive enough to be used for furnace control, monitoring of process-induced damage on flat capacitors, and for advanced gate dielectric development.

Experimental

A highly repeatable mercury probe described previously [*2*] was used for the GOI measurements in this study. Nominal gate areas are determined by the size of the mercury capillary used to form the gate. In this study, capillaries with diameters of 0.5- to 4.0-mm were used. For the thicker oxides measured in this work, a mercury gate approximately 4.0-mm in diameter was used to monitor defect densities as low as 0.1-cm^{-2} and is some cases a 1.0-mm capillary was used. For ultra-thin gate oxide characterization, where thickness, leakage, and trapping are critical parameters, a mercury gate of approximately 0.5-mm diameter was used. The area repeatability of all gate areas was better than 0.1%, one-sigma. The current-voltage (IV) measurements were made using a Keithley 236/237 Source Measure Unit (SMU). Data collection and analysis were performed using the PROCAP software used in the CV/QV/IV systems produced by Solid State Measurements, Inc.

Physics of Mercury Gate IV Measurements

Mercury gate GOI measurements are just as sensitive to a variety of defects and to advanced gate properties as conventional polysilicon or prefabricated metal gate measurements but the absolute value of the mercury gate GOI parameters, such as Charge-to-Breakdown (Q_{BD}) and Field-to-Breakdown (F_{BD}), are significantly different than those obtained with polysilicon gates. This is especially true for the case of gate injection – where the gate is at negative bias. The reasons for this difference are explained by considering basic transport mechanisms. First, there is a significant difference in work function between mercury and polysilicon gates as shown in Table 1

Table 1 – *Ideal Barrier Heights*

Gate Material	Work Function (eV)	$E_C - E_F$ (eV)	Ideal ϕ_B (eV)
Aluminum	4.25	N/A	3.35
Mercury	4.50	N/A	3.60
n+ Polysilicon	4.05	N/A	3.15
Si Substrate	N/A	0.1	3.25

[3]. The higher work function of the mercury results in a higher injection barrier height. Therefore, a mercury gate has lower and slightly higher F_{BD} values than a polysilicon gate on the same dielectric film. Generally, a change of about 60 meV in barrier height will result in a order-of-magnitude change in current. For the case of substrate injection where the gate is under a positive bias, the GOI parameters will differ only slightly from the polysilicon gate values because the barrier height depends on the silicon substrate properties and not on the gate material. Second, on more aged surfaces an interfacial layer can exist between the mercury gate and the dielectric surface. This layer is composed of organics, inorganics, water, or combinations of these impurities and can induce an increase in the effective barrier height. However, even though the absolute values of parameters measured on polysilicon and mercury gates are different the sensitivity to changes in these parameters is nearly the same as shown in the examples below.

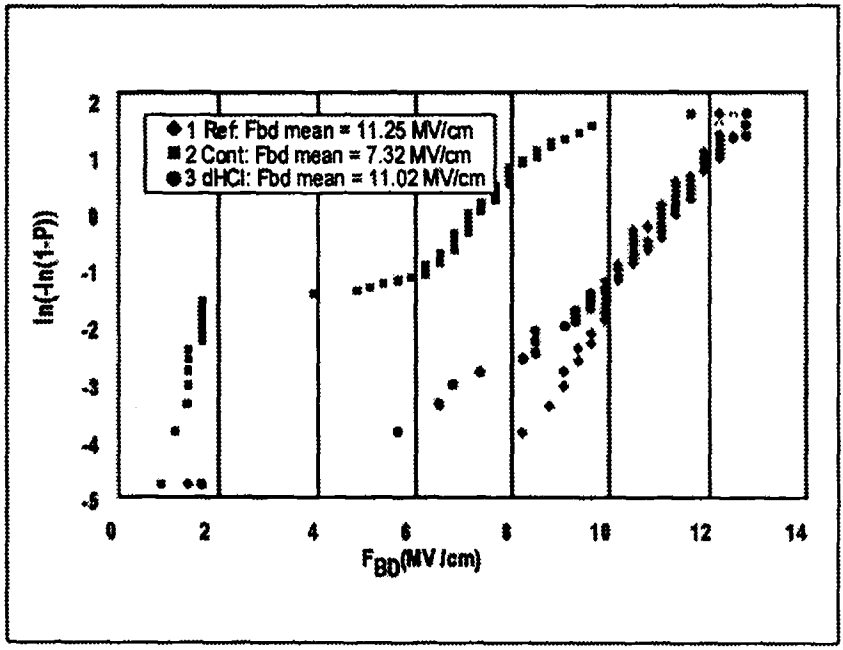

Figure 1 – *Effects of Iron Contamination: Weibull Plots of F_{BD} Showing the Effects of Iron on Quality of Oxide*

Furnace Control

Thermally grown silicon dioxide films are the most common dielectric materials now in use. The quality of the oxide is highly dependent on cleanliness in the furnace

where these films are grown and on the condition of the silicon surface prior to oxide growth. Factors such as metallic contamination, particles, gas leaks, surface precleans, etc., can all contribute to the degradation of these oxides as shown by GOI measurements.

The sensitivity of mercury gate F_{BD} measurements to iron contamination is demonstrated in the Weibull plots shown in Figure 1. In this case, three p-type wafers all oxidized to ~50-nm after various treatments were studied: first, a control wafer (1), second, a wafer that was contaminated with iron by ion implantation and given no further treatment (2) and, third, an iron contaminated wafer similar to 2, that was given an HCl based surface treatment (3). Stepped voltage IV measurement maps were made with the 4-mm diameter gate to obtain field-to-breakdown, F_{BD} , values. The iron-contaminated sample, 2, shows a shift of approximately 4 MV/cm in the F_{BD} value at the 50-percentile level and a distinct defect-related knee in the Weibull plot. Although the F_{bd} value at the 50- percentile level of the surface-treated iron-contaminated wafer, 3, is close to that of the control wafer, some iron contamination obviously still remains after the clean, as indicated by the tail in the Weibull plot.

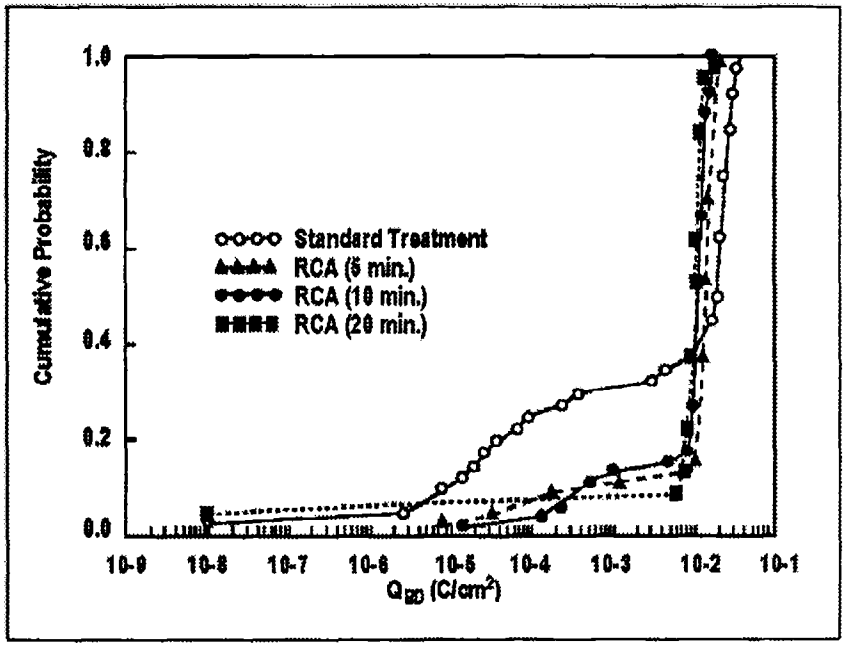

Figure 2 – *Effects of Oxide Pretreatment: Cumulative Probability Plots of Q_{BD} for Various RCA Cleaning Times*

The sensitivity of the mercury gate GOI measurement to preoxidation surface treatments with RCA cleans is shown in Figure 2. Here a 1.0-mm mercury gate was used to measure charge-to-breakdown, Q_{BD}, by the stepped current method. Maps of Q_{BD} were made on a series of n-type wafers that had been cleaned for different lengths of time prior to oxidation. An oxide thickness of approximately 12-nm was then grown on the wafers. As the surface treatment time is increased from the very short Standard Treatment to as long as 20 min., the defect density indicated by the knee in the Q_{BD} probability plot improves. This is probably due to a decrease in both particle density with the RCA-1 clean and metal contamination with the RCA-2 clean as the cleaning time is increased.

Plasma Damage

Process-induced plasma damage occurs in gate dielectrics as the result of process charging and can cause physical damage or excessively high tunneling currents. The problem with process-induced charging is that generally only a small amount of charge is actually placed on the wafer surface. However, because the ratio of passive to active

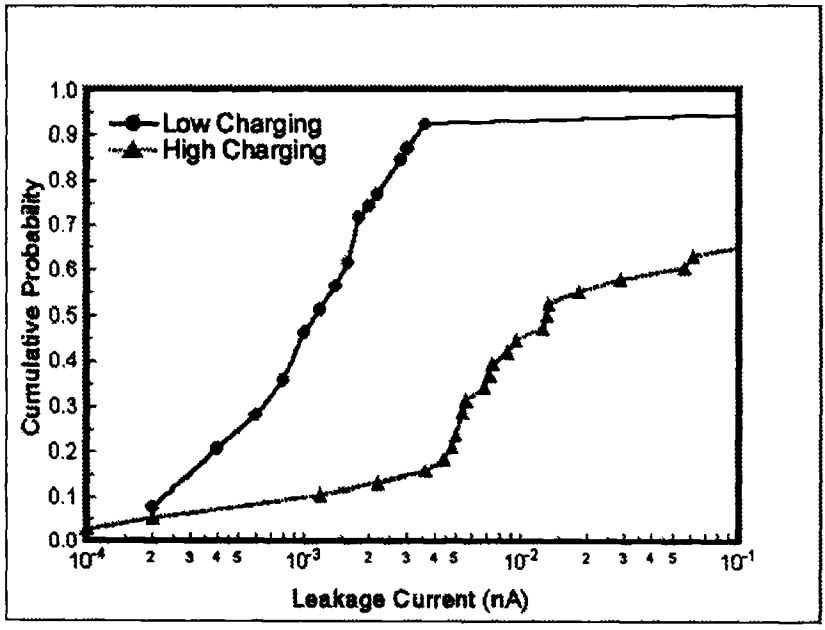

Figure 3 – *Leakage Current Cumulative Probability for Polysilicon Gate Antenna Structure Comparing the Effects of High and Low Oxide Charging*

oxide (antenna ratio) is large, a significantly higher electric field is placed on the active gate oxide. This results in damage and reduced reliability of these active gate oxides. Conventionally, special antenna structures are required to monitor these charging effects. However, these antenna structures are costly and time consuming to prepare. Therefore it would be very useful if the same sensitivity to plasma damage could be obtained using a typical MOS flat capacitor. In this study, p-type wafers each with 200-nm of thermal oxide were used as substrates for the deposition of 30- to 40-nm of PECVD oxide. Half of these substrate wafers had polysilicon antenna structures over the thermal oxide for the antenna charge measurements; a sister set of wafers with no antenna structures was used for the mercury gate measurements. Oxides were deposited at two different power settings to obtain a set of wafers having oxides deposited at low power with low charging and wafers having oxides deposited at high power with high charging.

Figure 3 shows the effects of low and high charging on typical polysilicon gate antenna structures. The generally higher leakage currents and distinct knee in the cumulative probability plot of the high charging plot indicate a much higher plasma induced damage in this gate oxide than is seen with the low charging plot. In general, flat capacitors cannot detect process-charging effects. But, it has been found that the rate-of-

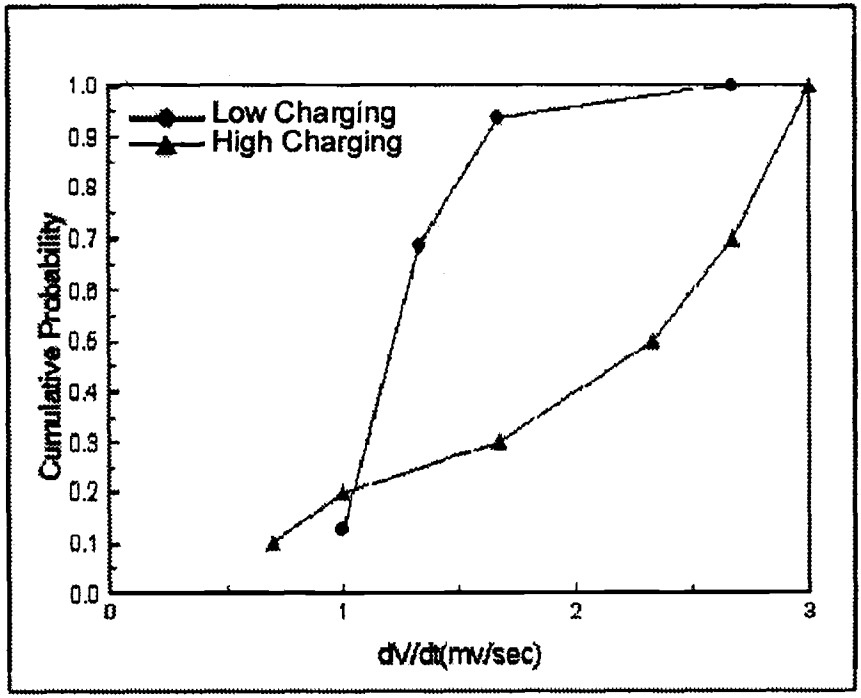

Figure 4 – *Constant Current dV/dt Cumulative Probability for Mercury Gate Flat Capacitor Comparing the Effects of High and Low Oxide Charging*

change in measured voltage with application of a low constant current can be sensitive enough to monitor these effects using a flat mercury capacitor [*4*]. The plots of a 10-nA constant current dV/dt made on mercury gate flat capacitors in Figure 4 show the same sensitivity to low and high charging as the polysilicon gate antenna structures.

Advanced Gate Dielectric Development

The National Technology Roadmap for Semiconductors (NTRS) estimates that an Equivalent Oxide Thickness (EOT) of 1.5- to 2.5-nm will be required for geometries with line widths below 0.15-μm. The potential problems when using silicon dioxide at these line widths are boron penetration from the polysilicon through the gate oxide, direct tunneling leakage currents, and oxide reliability. Much work has been done recently to

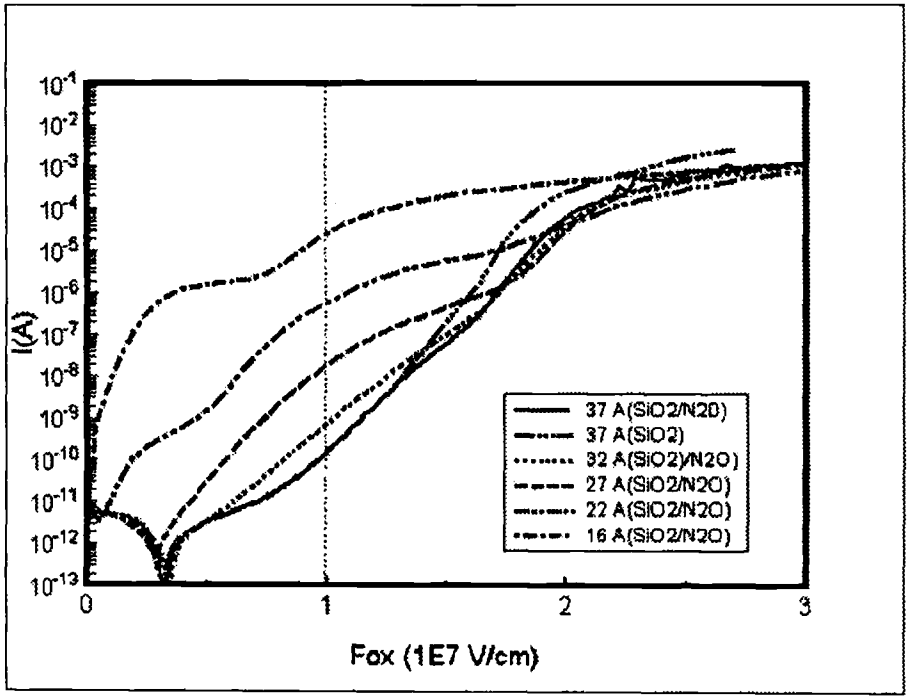

Figure 5 – *Current vs. F_{ox} for Various Ultra -Thin Oxide and Nitrided Oxides as Measured by Mercury Gate MOS IV*

improve the reliability of these ultra-thin oxides and reduce boron penetration by using nitrided oxides. However, the problem of excessively high tunneling still exists. Currently, work is being done using high k dielectrics such as tantalum pentoxide, silicon nitride, and aluminum oxide to replace silicon dioxide. The problem with these materials

is that they have much higher bulk and interface trap densities than thermally grown silicon dioxide.

As an example of the sensitivity of mercury GOI to the development of these advanced gate dielectric materials, Figure 5 shows the results of five site maps done on nitrided oxides with thicknesses ranging from 1.6- to 3.7-nm on p-type substrates. The overlap of the plots at each site for each sample is an indication of the repeatability of these measurements and the uniformity of the film properties. Several other key features are seen in the data. First, the vertical line at $1x10^7$ V/cm shows the high sensitivity to the dielectric thickness. Second, for mercury gates, a sensitivity of 0.35-nm /decade, which is very close to the 0.25-nm/decade reported for polysilicon gates, has been determined from a plot of current vs. thickness obtained at $1x10^7$ V/cm. Third, it is also very clear from the plots of the two 3.7-nm thickness films that there is a definite improvement in the quality of the thermal oxide when it is nitrided with an anneal in N_2O as indicated by the improved F_{BD} of the nitrided film. Fourth, according to Weir [*5*] the noise seen at the high current end of these plots is an indication that breakdown has occurred. Soft breakdown in ultra-thin dielectrics is difficult to detect. However, Weir claims that one method for detecting soft breakdown is to monitor this noise in the IV data, which increases immediately following breakdown. This figure thus illustrates the sensitivity of mercury gate IV measurements to the critical parameters of gate dielectrics and their usefulness as a tool in the development of new gate dielectric materials.

Conclusion

The sensitivity and usefulness of the mercury gate GOI measurements to defects in gate oxides and other dielectric materials have been demonstrated. Although the absolute levels of GOI parameters like F_{BD}, and, differ significantly from the conventional polysilicon gate values, the mercury gate measurements are just as sensitive to changes in the quality of dielectric materials. The sensitivity of mercury gate GOI measurements to metal contamination and surface cleaning makes this measurement ideal for monitoring oxidation furnace quality. The sensitivity of the flat mercury MOS capacitor to changes in dV/dt at constant current indicates that this measurement can be used to monitor plasma damage without the need for fabricating costly antenna structures. Also, the unique ability of the highly repeatable mercury contact for monitoring the quality of ultra-thin dielectrics and the effects of oxide nitridation make mercury gate GOI measurements a useful tool in the development of advanced gate dielectric materials for 0.15-nm geometries and below.

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COCOS (Corona Oxide Characterization of Semiconductor) Metrology: Physical Principles and Applications

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Reference: Wilson, M., Lagowski, J., Savtchouk, A., Jastrzebski, L., and D'Amico, J., **"COCOS (Corona Oxide Characterization of Semiconductor) Metrology: Physical Principles and Applications,"** *Gate Dielectric Integrity: Material, Process and Tool Qualification, ASTM STP 1382*, D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: During the past five years great progress has been made in CV replacement metrology which utilizes precise dosing of electric charge on dielectric surfaces achieved with a corona discharge in air. This charge produces controlled changes of electric field in the dielectric film and in the space charge region of semiconductor substrate. The response of the dielectric and semiconductor is monitored in a non-contact manner using three measurements: the contact potential difference (CPD) in the dark, CPD under strong illumination, and the small signal ac-surface photovoltage (ac-SPV). In COCOS metrology these measurements are performed as a function of the corona charge placed on the whole wafer. A near equipotential, whole wafer surface is maintained while the semiconductor space charge is transferred from accumulation – through flat band – to deep inversion. Data analysis based on electrostatic equations and charge neutrality gives a total set of electrical parameters, equivalent to those obtained in MOS-CV metrology, characterizing the space charge, the semiconductor-dielectric interface and the dielectric film. The equipotential condition is crucial for reducing charge transport along the surface without creating guard-rings. Using a blanket of corona charge placed over the wafer surface and whole wafer mapping of CPD and SPV, the COCOS metrology enables one to obtain whole wafer maps of almost all parameters. Examples are given, illustrating COCOS application to Si/SiO_2, with an emphasis on thin gate oxide reliability.

Keywords: COCOS, corona, interface traps, stress induced leakage current, iron contamination, contact potential difference

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Physical Principles of COCOS

Whole Wafer Corona Charging

The COCOS[3] method combines two key elements: whole wafer corona charging and contact potential difference (CPD) measurement [*1*]. Historically, the use of corona charging and subsequent CPD measurement to investigate oxidized Si wafers was introduced in 1968 by Williams and Willis at the RCA Laboratories in Princeton, New Jersey [*2*]. However, Williams and Willis used a needle-type corona electrode to deposit charge on only a small surface site. As a result, this was a slow one-site-at-a-time measurement. This method of corona charging was used until the development of the SDI whole wafer corona charging method [*3*]. As shown in Figure 1, the whole wafer corona charging is realized by depositing a blanket of corona charge across the surface of the oxidized wafer using a corona wire moving parallel to the wafer surface.

Ions generated by the corona discharge in air do not cause damage to the oxide because at atmospheric pressures their mean free path of about 10^{-5} cm is very short as compared to the 1 cm distance the ion has to travel to from the wire to the wafer surface. Therefore the ions reach the SiO_2 surface with very low kinetic energy. For positive polarity, the dominant ionic specie is of the type $(H_2O)_nH^+$, while for negative polarity CO_3^- is the dominant ion [*4*]. These ions are thermally stable on the oxide surface up to temperatures of about 250°C, but can be easily removed by rinsing with deionized water.

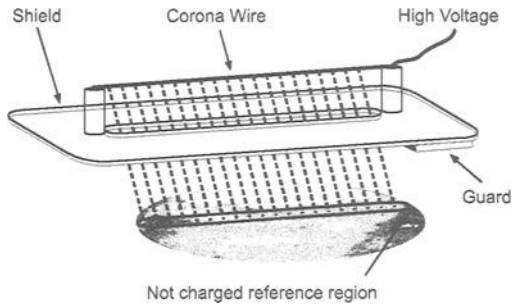


Figure 1 – *COCOS whole wafer corona charging method.*

[3] The acronym COCOS, standing for "CORONA-OXIDE-CHARACTERIZATION OF SEMICONDUCTOR," was introduced in 1997. COCOS™ is a trademark for corresponding tools manufactured by Semiconductor Diagnostics, Inc.

Contact Potential Difference (CPD) Measurement

Figure 2 is a schematic of the contact potential difference probe that is used in the COCOS method. The probe assembly is placed approximately 1 mm above the wafer surface. A vibrating fork directly below a steady reference electrode modulates the probe to wafer capacitance and generates an AC current signal that is monitored. This AC signal is directly proportional to the contact potential difference (V_{CPD}):

$$J = V_{CPD} \frac{dC}{dt} \tag{1}$$

where C is the capacitance between the probe and the wafer periodically varied by the vibrating fork and J is the generated AC current.

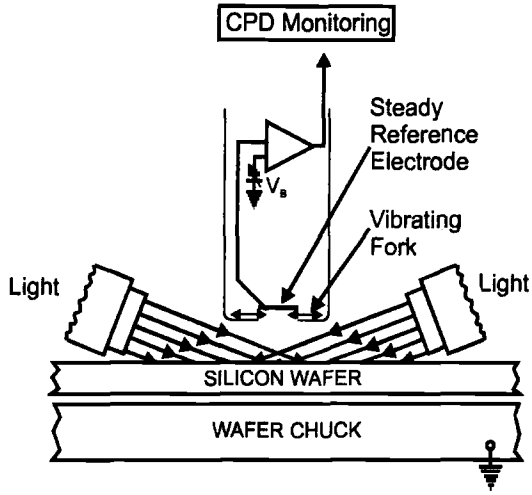


Figure 2 – *CPD probe setup enabling measurement in the dark and under illumination.*

The change of the contact potential difference (ΔV_{CPD}) caused by an increment of corona charge is equal to the change in the voltage drop across the oxide (ΔV_{OX}) plus the change in the surface barrier (ΔV_{SB}) (voltage drop across the space charge region):

$$\Delta V_{CPD} = \Delta V_{OX} + \Delta V_{SB} \tag{2}$$

Strong illumination of the Si underneath the CPD probe flattens the surface barrier giving approximately $V_{SB} \approx 0$. Illumination does not effect V_{OX}. Accordingly, CPD

measurements in the dark and under illumination are used to determine ΔV_{SB} induced by corona charge:

$$\Delta V_{CPD}^{dark} - \Delta V_{CPD}^{ill} = \Delta V_{SB} \tag{3}$$

Knowing changes in the surface barrier due to corona deposition, the corresponding changes in the oxide voltage are determined from eqn. 2 as:

$$\Delta V_{OX} = \Delta V_{CPD}^{dark} - \Delta V_{SB} \tag{4}$$

or

$$\Delta V_{OX} = \Delta V_{CPD}^{ill} \tag{5}$$

COCOS Experimental Setup

Figure 3 illustrates the combination of the two key COCOS elements in the experimental setup used in the COCOS method. A blanket of corona charge is placed on the surface of the oxidized wafer and the effect of this corona deposition upon the oxide and silicon is monitored using the CPD measurement in the dark and under illumination. The two key elements work together to provide information about the oxide, the Si/SiO_2 interface and the near surface silicon.

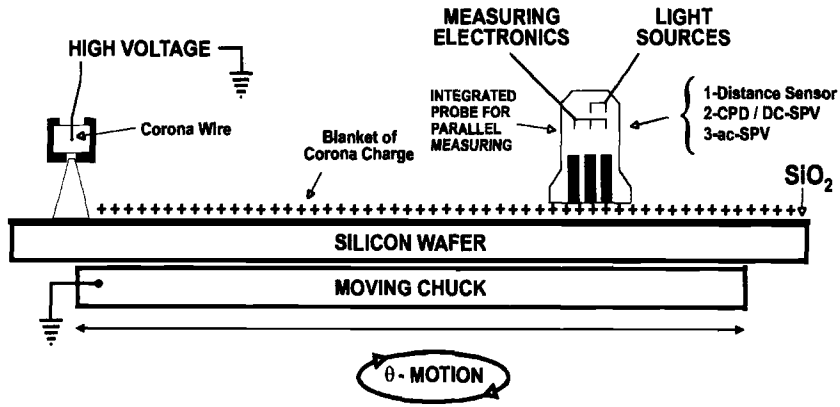
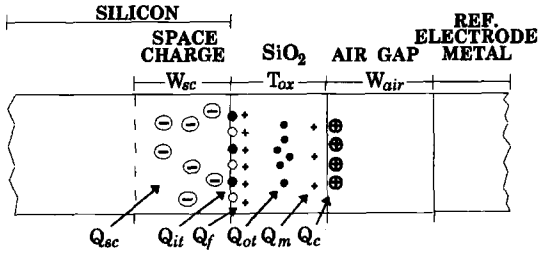


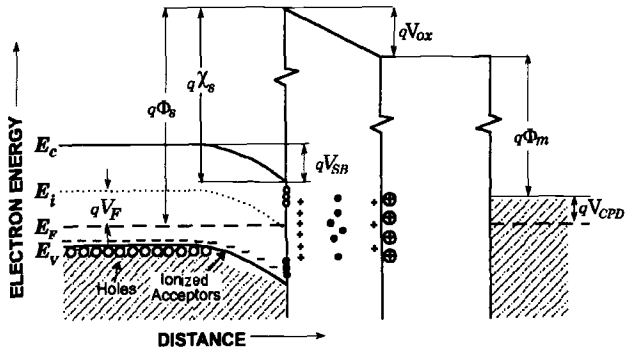
Figure 3 – *COCOS experimental setup schematic.*

Figure 4 illustrates an energy band diagram of the Si/SiO_2 system with a CPD reference electrode. In this diagram it is shown that the net effective oxide charge, Q_{OX}, including the deposited corona charge, must be imaged in the space charge region in order to fulfill the condition of electrical neutrality:

$$Q_{OX} = Q_{it} + Q_f + Q_{ot} + Q_m + Q_c = -Q_{sc} \tag{6}$$



Q_{sc} Space Charge
Q_{it} Interface Trap Charge
Q_f Oxide Fixed Charge
Q_{ot} Oxide Trapped Charge
Q_m Mobile Ionic Charge
Q_c Corona Charge



$$V_{CPD} = \Phi^{\circ}_{ms} + V_{SB} + V_{ox}$$

$$\Phi^{\circ}_{ms} = \Phi_m - (\chi_s + \frac{E_g}{2} + V_F)$$

E_c Conduction Band Energy
E_i Intrinsic Energy
E_F Fermi Energy
E_V Valence Band Energy
$q\Phi_s$ Semiconductor Work Function
$q\Phi_m$ Work Function of Ref. Electrode
$q\chi_s$ Semiconductor Electron Affinity
V_F Bulk Fermi Potential
V_{SB} Semiconductor Surface Barrier
V_{ox} Oxide Voltage

Figure 4 – *Si/SiO$_2$ energy band diagram with a CPD reference electrode.*

Therefore, a quantum of corona charge, ΔQ_c, deposited on the surface of the oxidized silicon can be imaged in the space charge region, ΔQ_{sc}, but can also be imaged in any oxide traps that can exchange charge with the bulk silicon, i.e., interface traps ΔQ_{it}.

$$\Delta Q_c = -(\Delta Q_{sc} + \Delta Q_{it}) \tag{7}$$

The surface space charge, Q_{sc}, can be determined from the surface barrier, V_{SB}:

$$Q_{sc} = \pm \frac{\sqrt{2}\varepsilon_s kT}{qL_D} F\left(V_{SB}, \frac{n_0}{p_0}\right) \tag{8}$$

and

$$F\left(V_{SB}, \frac{n_0}{p_0}\right) = \pm\left[(e^{-\beta V_{SB}} + \beta V_{SB} - 1) + \frac{n_0}{p_0}(e^{\beta V_{SB}} - \beta V_{SB} - 1)\right]^{1/2} \quad (9)$$

where F is the space charge function which relates the surface barrier to the net value of the surface charge [5,6], L_D is the extrinsic Debye length for holes, $L_D = [\varepsilon_s/qp_0\beta]^{1/2}$, n_0 and p_0 are the concentrations of free electrons and holes respectively, in the semiconductor bulk, $\beta=q/kT$, q is the elementary charge, kT is the thermal energy and $K_s\varepsilon_0=\varepsilon_s$ is the permittivity of the semiconductor.

The interface trap charge, ΔQ_{it}, corresponding to a given quantum of corona charge is determined from the following relation:

$$|\Delta Q_{it}| = |\Delta Q_c| - |\Delta Q_{sc}| \quad (10)$$

The density of interface traps, D_{it}, be calculated as the ratio $\Delta Q_{it}/\Delta V_{SB}$, where ΔV_{SB} is the change in the surface barrier due to the deposited quantum of corona charge. A D_{it} spectrum can then be obtained by plotting D_{it} versus V_{SB}.

The corona charge deposited on the surface of the oxide changes the electric field in the oxide in accordance with Gauss's law:

$$\Delta E_{OX} = \frac{\Delta Q_c}{\varepsilon_0 \varepsilon_{OX}} \quad (11)$$

where ΔE_{OX} is the change in the electric field across the oxide and $\varepsilon_0\varepsilon_{OX}$ is the permittivity of the oxide.

A corresponding change of the voltage drop across the oxide with a thickness T_{OX} is:

$$\Delta V_{OX} = T_{OX}\Delta E_{OX} = \frac{\Delta Q_c}{C_{OX}} \quad (12)$$

where C_{OX} is the capacitance of the oxide:

$$C_{OX} = \frac{\Delta Q_c}{\Delta V_{OX}} \quad (13)$$

MOS-CV and COCOS Comparison

A comparison highlighting the differences and similarities between the MOS-CV and COCOS techniques is shown in Figure 5. The MOS technique uses a gate such as

polysilicon or metal deposited on the surface of the oxide and an electrical back contact to the semiconductor substrate. A bias voltage is applied to the gate in order to change the electric field in the oxide and in the semiconductor space charge region. The response to this gate bias is monitored by measuring capacitance-voltage, C-V, and current-voltage, I-V, characteristics. The overall procedure including the fabrication of capacitors is costly and time-consuming. It is also a destructive one. COCOS does not require preparation of a gate or a back contact. It is non-destructive and permits reusing of measured wafers. A comparison of the variables and parameters involved in the two techniques is shown in Table 1. From zero band bending up to the deep inversion threshold, COCOS has an advantage in determining the flat band voltage without knowing the doping level or dielectric capacitance and in determining the interface trapped charge and surface barrier. For ultra thin oxides, COCOS revealed advantages in accumulation over MOS due to much lower leakage in the high field range resulting from a suppression of direct tunneling. This aspect is important for accurate C_{OX} determination.

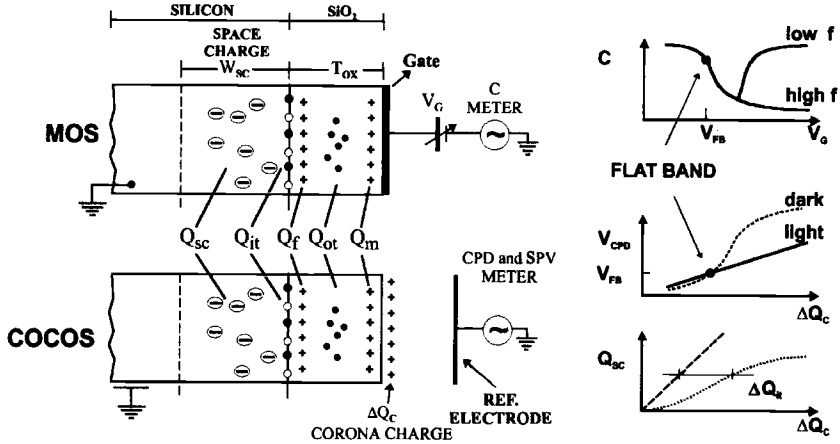


Figure 5 – *COCOS and MOS-CV schematic comparison.*

Table 1 – *COCOS and MOS-CV variable and parameter comparison.*

	Independent Variable	Oxide Field Change	Measured Quantity	Method Voltage	Flatband
MOS[a]	V_G	$\Delta E_{ox} = f(V_G)$	C vs V_G	C-V	$V_{FB} = V_G$
COCOS[b]	ΔQ_C	$\Delta E_{ox} = \frac{1}{\varepsilon_0 \varepsilon_{ox}} \Delta Q_C$	V_{CPD}^{Dark} vs ΔQ_C V_{CPD}^{Light} vs ΔQ_C	V-Q	$V_{FB} = V_{CPD}^{Dark} - V_{CPD}^{Light}$
			Q_{SC} vs ΔQ_C	Q-Q	

(a) Complicated relationships in depletion to deep inversion; difficult to separate ΔV_{OX} and ΔV_{SB},
(b) explicit relationships and easy separation of ΔV_{OX} and V_{SB}.

In Figure 5 to the right of the COCOS schematic are two plots illustrating typical experimental results obtained from a COCOS measurement. The upper plot shows V_{CPD} plotted versus the corona charging increment. There is curve of V_{CPD} in the dark and one of V_{CPD} under illumination. The difference between these two curves is the surface barrier (V_{SB}). When the V_{CPD} in the dark equals V_{CPD} under illumination, V_{SB}~0 and the COCOS flat band (V_{FB}) condition is achieved.

Interface Trap Spectrometry/Water Flask Analogy

The plot in the bottom right of Figure 5 shows Q_{SC}, calculated from V_{SB}, plotted against the corona charging increment, ΔQ_C. This Q-Q plot is used for COCOS measurement of interface traps. The one-to-one line in this plot represents the ideal case in which there are no interface traps and all of the corona charge deposited on the surface of the oxide is imaged in the space charge region. Any deviation from this line, illustrated by the other curve in the plot, is due to trapping by interface states. The difference between these two curves is the interface trapped charge, ΔQ_{it}.

A water flask analogy was developed to help in the understanding of interface trap spectrometry in the COCOS method. Figure 6 illustrates the water analogy. Water being poured into the container is analogous to electrons induced in the space charge region by positive corona deposited on the oxide surface of p-type Si. The height of the water, h, in the container is analogous to the surface barrier, V_{SB}. The flasks on the side of the container represent discrete interface traps. In the ideal case with no flasks (no interface traps present), the height of the water in the container would linearly increase with every dose of water.

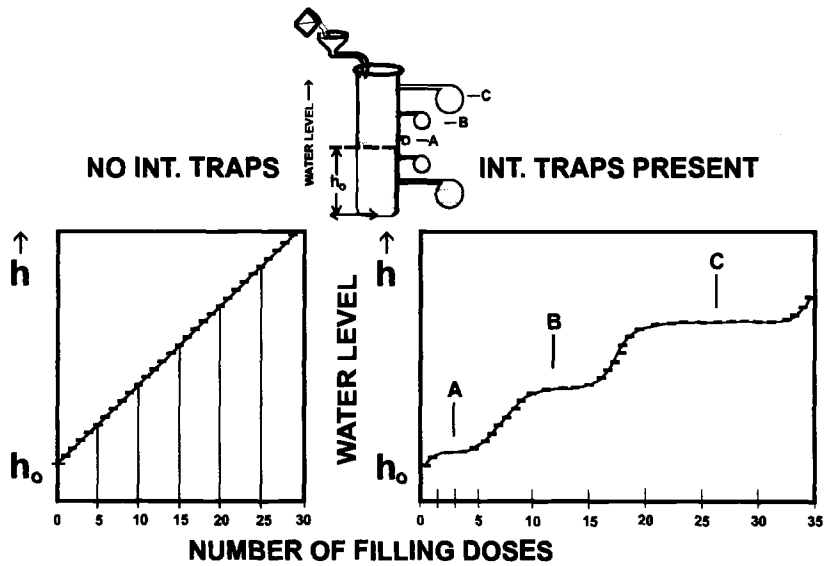


Figure 6 – *Water flask analogy with discrete interface traps.*

However, with flasks present (discrete interface traps present), the water level would stop rising until the flask is filled. Likewise, the surface barrier would be pinned at a discrete interface trap until that trap is filled by corona charge induced electrons in the space charge region. The flasks (or traps) give rise to the ledges labeled A, B and C shown in the water height versus filling dose plot in Figure 6. Similar ledges due to discrete interface traps appear in the ΔV_{SB} versus ΔQ_C plots and in the corresponding Q-Q plots (ΔQ_{SC} versus ΔQ_C). These ledges create corresponding peaks in a D_{it} spectrum. Figure 7 illustrates a different water/interface trap analogy with a continuous distribution of interface states represented by the small tubes on the side of the container. This case corresponds to the typical U-shaped distribution of interface states across the band gap.

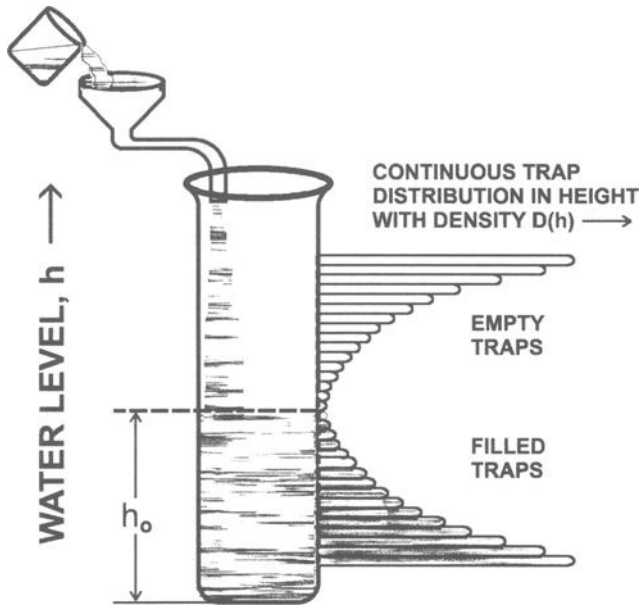


Figure 7 – *Water flask analogy with a continuous interface state distribution.*

Applications of COCOS

A historically important stepping stone in the development of the COCOS methodology was the introduction of the whole wafer corona charging method used in the mapping of sodium contamination in oxides [*1,3,7,8*]. Sodium contamination mapping and many other applications of the COCOS method in an industrial setting will be discussed in an article to be published shortly [*9*]. Present work discusses applications of the COCOS method that deal with the issues of gate dielectric reliability: wearout and stress-induced leakage current (SILC). Wear-out and SILC have become very important

issues as the thickness of gate oxides have been scaled down to <100Å [*10-14*]. The COCOS technique can monitor aspects of wearout and SILC in a non-contact manner. This avoids the inherent difficulties associated with the measurement of thin oxides by the MOS-CV technique [*15*].

Corona Stress

COCOS methodology summarized in Table 1 uses low electric fields in the oxide (below 1 MV/cm), which create negligible room temperature leakage. Larger electric fields are used in COCOS measurements of dielectric wearout and SILC. Weinberg et al implemented, for the first time, corona charging to investigate SiO_2 films on Si at very high fields [*16,17*]. With increasing corona charge, an electric field in an oxide increases and for sufficiently high corona charge tunneling of electrons (or holes) from the semiconductor to the oxide conduction (or valence) band takes place. Such Fowler-Nordheim, F-N, tunneling induced by positive corona charging is illustrated in Figure 8. Once the tunneling takes place the charge build-up on the oxide stops when the F-N current density, $J_{F\text{-}N}$, reaches the corona ionic current density, J_{Corona}. At this stage prolonged corona charging produces stress leading to oxide wearout and SILC. After corona charging is terminated the surface charge decays due to residual $J_{F\text{-}N}$ current and/or SILC depending on the stress fluence. In COCOS stress experiments the fluence is controlled by stress time and by the magnitude of corona current density.

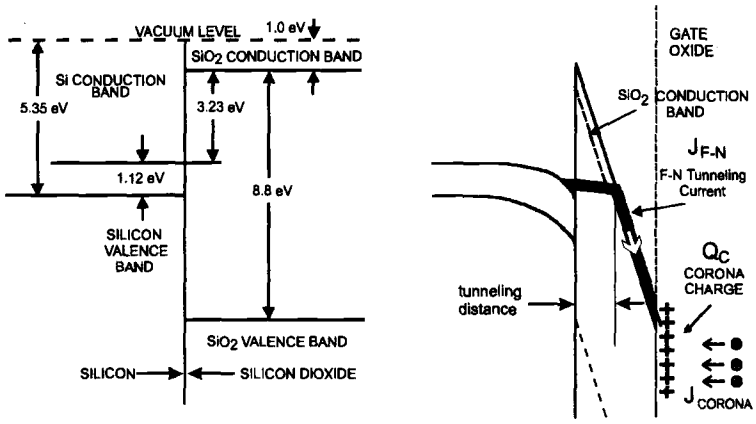


Figure 8 – *Energy band diagram of the Si/SiO_2 system without any oxide charge and with corona leading to Fowler-Nordheim tunneling.*

Stressed-induced Interface Traps and Flat-band Shift

Dumin [*10*] made a very important general statement regarding wearout: "During the wearout phase, defects or traps are generated inside the oxides [*18*], and at the oxide interfaces [*19*] by the voltages applied across the oxides and/or the currents flowing through the oxides." The COCOS method can be used to apply voltage across oxides and induce corresponding currents. In addition COCOS provides a means for monitoring the traps, thus enabling the study of wearout phenomenon.

Stress-induced creation of interface traps is demonstrated in Figure 9 by D_{it} spectra before and after corona stressing for a 50Å oxide. The D_{it} spectrum before stress shows a typical U-shaped distribution with a minimum value of about $7x10^{10}$ $qcm^{-2}eV^{-1}$. However, the spectrum after stress shows almost two orders of magnitude increase in the interface trap density. Table 2 summarizes the effect of corona stress upon D_{it}, flat-band voltage and the effective charge, Q_{eff}, measured with COCOS at the same wafer site. Notice the large negative shift in the flat-band voltage, indicating the large increase in the positive oxide charge.

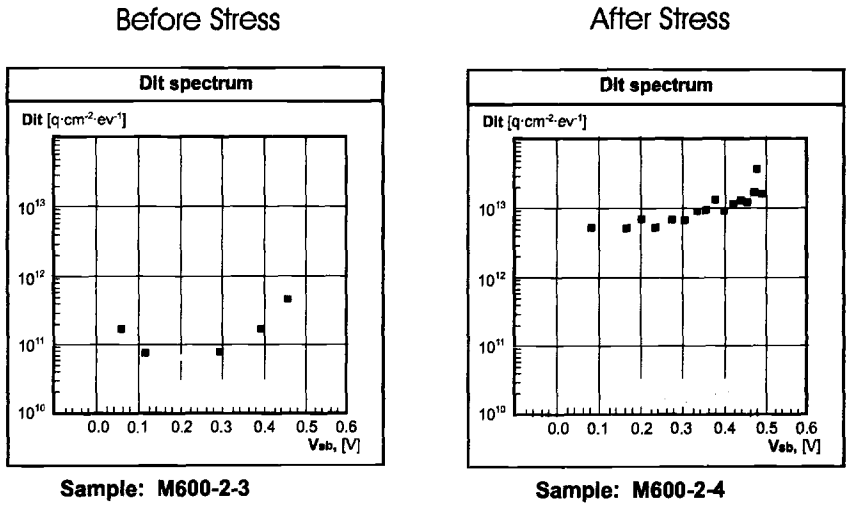


Figure 9 – *Interface trap spectra of a 50Å oxide before and after corona stress.*

Table 2 – *Summary of interface trap density, flat-band voltage and effective charge values before and after corona stress.*

	D_{IT} [$cm^{-2}eV^{-1}$]	V_{FB} [V]	Q_{eff} [q/cm^2] = $-V_{FB}C_{OX}$
Before Stress	$6.6x10^{10}$	-0.09	$9.9x10^{11}$
After Stress	$4.7x10^{12}$	-0.46	$5.1x10^{12}$

COCOS I-V Method

Using the COCOS method it is possible to obtain I-V curves without fabrication of MOS capacitors. In COCOS I-V, the voltage equals the contact potential difference, V_{CPD}, while the current is monitored by CPD measurement of the corona charge dissipation due to electron or hole transport across the oxide. The current density is:

$$J = \frac{dQ_c}{dt} \tag{14}$$

The technique of CPD monitoring of corona charge decay on thin films has been extensively used to investigate resistivity and high field effects in polymer films [*20*]. The COCOS I-V methodology is a modification of this technique with the intent to investigate very thin gate dielectrics.

Using the COCOS I-V technique we have investigated SILC phenomenon in thin gate oxides below 100Å. The COCOS I-V data in this work is actually presented as corresponding current density versus electric field in the oxide. The curves in Figure 10 were obtained for an 85Å oxide stressed at room temperature with various fluences of positive corona. Notice that the curve at the lowest fluence follows theoretical Fowler-Nordheim tunneling, while subsequent larger fluence stress results in significant current at lower electric fields, i.e. SILC.

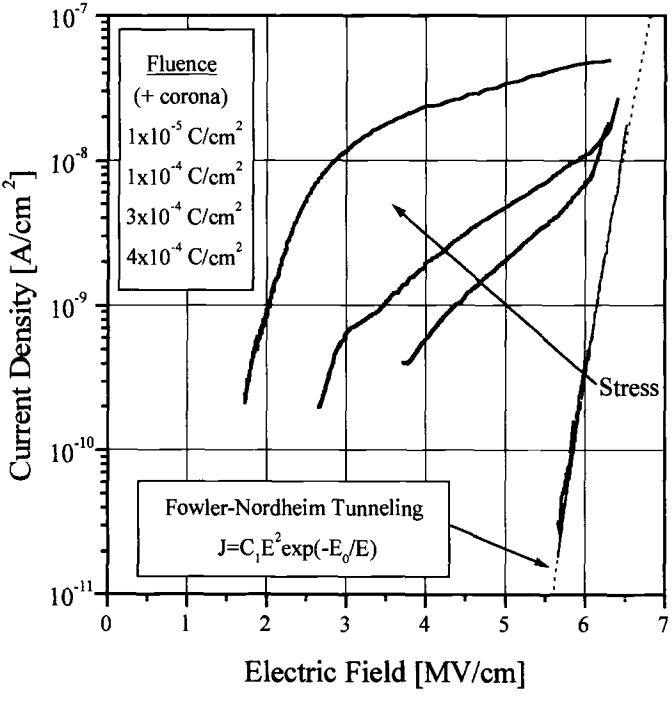


Figure 10 – *Current as a function of oxide field for an 85Å oxide after corona stress.*

The effect of corona stress on leakage for a 35Å oxide is shown in Figure 11. The slope of the lowest fluence curve is substantially smaller than that of the F-N tunneling shown in Figure 10. This indicates a different mechanism such as direct tunneling consistent with the behavior of very thin oxides. Once again notice the shift in the COCOS current characteristics to higher currents and lower fields due to SILC.

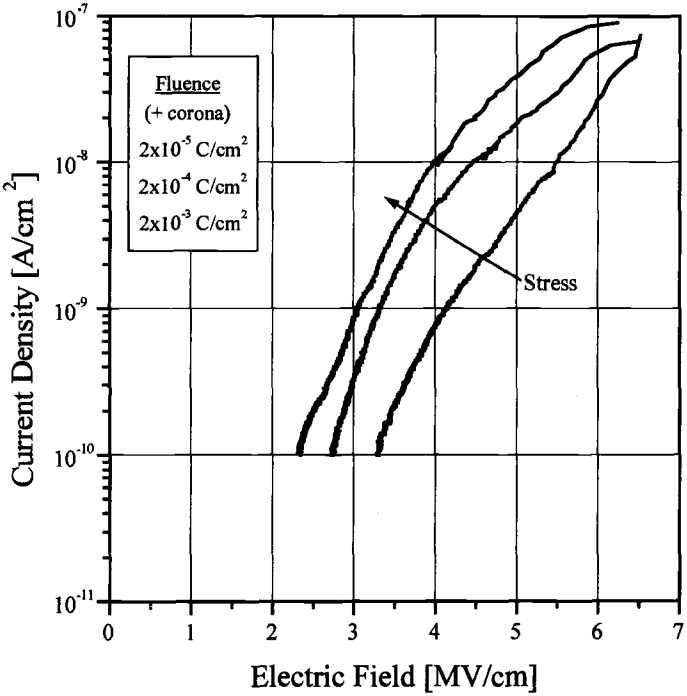


Figure 11 – *Current as a function of the oxide field for a 35Å oxide after corona stress.*

Effect of Iron Contamination on SILC

The effect of iron contamination upon SILC in thin gate oxides was also investigated using the COCOS I-V technique. Silicon wafers were contaminated with iron at two different levels: $5x10^{10}$ and $5x10^{11}$ atoms/cm^3. The wafers were then thermally oxidized to 70Å. The curves in Figure 12 were measured for each wafer after stressing with three fluence levels. It is seen that at the lowest fluence the curves are nearly identical in spite of different iron contamination levels. At the highest fluence the higher iron contaminated wafer shows a definite shift to higher currents as compared to the wafer with the lower iron level. This clearly demonstrates significant SILC enhancement by iron contamination. Details of this study will be published in a separate publication [*21*].

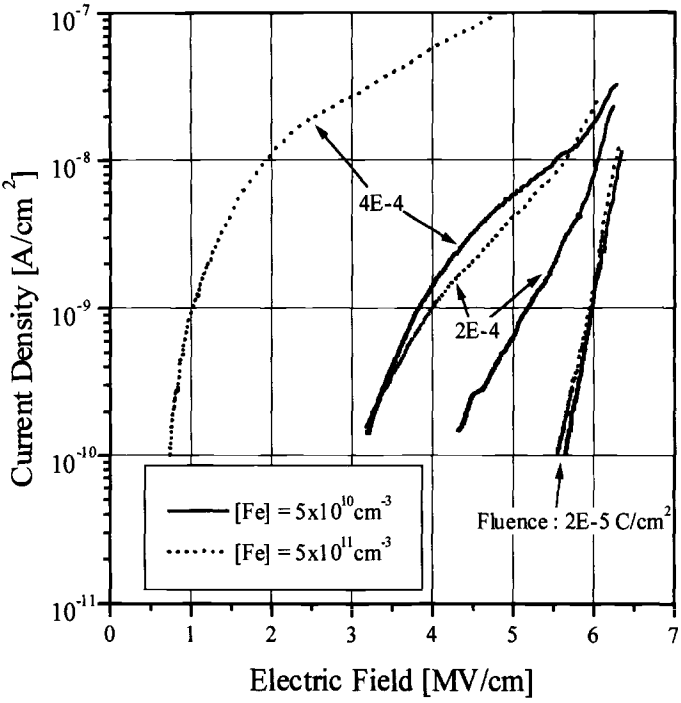


Figure 12 – *Effect of iron contamination on SILC in 70Å oxides.*

SILC Mapping

The COCOS technique can also be used to map the magnitude of SILC similar to V_{CPD} mapping of soft-breakdown discussed in earlier work [*22*]. Figure 13 illustrates a map of oxide field that has been dubbed the "SILC Cross". The SILC cross was generated by first charging the entire wafer at a low fluence to the onset of Fowler-Nordheim tunneling. The area of the cross was then charged with a much higher fluence, creating defects in the oxide and causing SILC in this area. The damaged oxide in the area of the cross can no longer hold as much charge on the surface as the surrounding area due to SILC. As shown in Figure 13, this results in a lower oxide voltage (i.e., lower V_{CPD} and also lower oxide field) in the area of the cross. Figure 14 shows the correspondence between two areas of the SILC cross map and their position on COCOS I-V curves. This example illustrates that the COCOS methodology can be used to monitor SILC by mapping of V_{CPD} after corona stress.

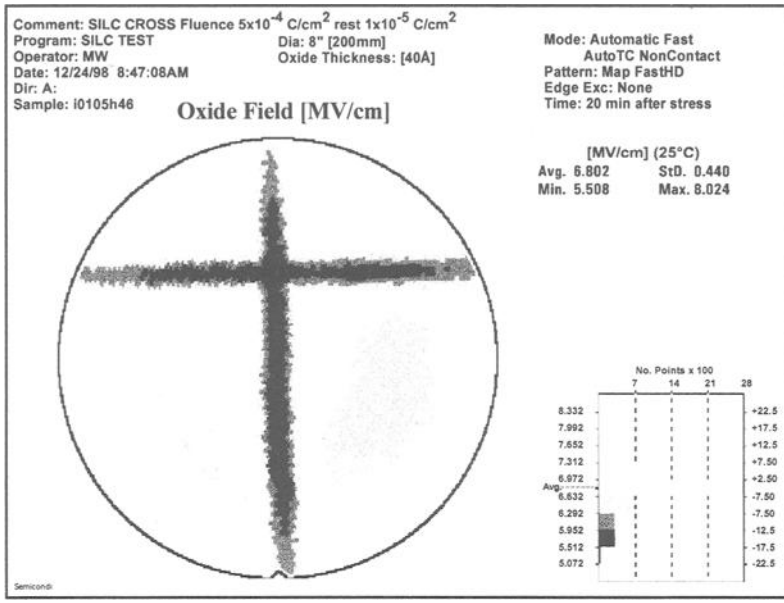


Figure 13 – *"SILC Cross" oxide field map.*

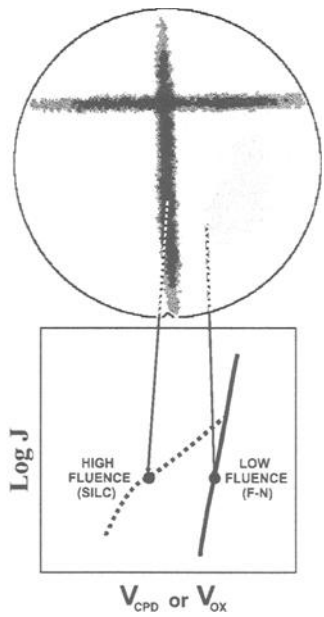


Figure 14 – *"SILC Cross" map and corresponding positions on COCOS I-V curves.*

Conclusions

COCOS is a non-contact, no preparation replacement for MOS-CV/IV technology. It can be used to monitor reliability issues in thin gate oxides such as wear-out manifested by stress-induced interface traps and flat-band shift. Using corona stress and the COCOS I-V technique, SILC in thin oxides can be investigated with fast turnaround times. New COCOS generated data indicate that iron contamination at the level of $5x10^{11}$ atoms/cm^3 is detrimental to SILC in 70Å gate oxides. It is also demonstrated that whole wafer corona charging combined with fast V_{CPD} mapping provides a means for mapping of SILC distribution.

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Application of Quantox Measurements to Identify Phosphorus Contamination in Silicon Wafers

Reference: Dexter, M. A., Hasslinger, K. M., Fritz, J. R., and Ullo, C. A., **"Application of Quantox Measurements to Identify Phosphorus Contamination in Silicon Wafers,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382,* D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: During a three-year period, MOS fab experienced a 0.3% parametric failure rate on LOCOS devices. The observed failure mode is high N- and low P-channel current leakage. Only wafer number five of a lot was affected. This selective (believed) phosphorus contamination was appropriately named the "Phantom Wafer Failure". MOS fab implemented routine monitoring on all oxidation furnaces using the Keithley Quantox characterization tool in December 1997. Flatband voltage and mobile ion concentration were monitored using this tool. It was only after implementing this monitoring that the fab was able to identify the source of the phosphorus contamination. This report illustrates using the Keithley Quantox to identify the source of this phosphorus contamination.

Keywords: quantox, corona oxide semiconductor, cos, phosphorus contamination, furnace monitoring

Introduction

Quantox tool implementation replaces metal or poly-Si gate MOSCAP C-V for oxide characterization measurements. This provides fast feedback since Quantox uses a contactless measurement method immediately following oxidation. Compare this to MOSCAP CV, which requires ~ 1 week of process and test time. An additional, somewhat unanticipated benefit is that the contactless test method is more sensitive to furnace variations compared to MOS-C testing. Enhanced sensitivity arises since post-oxidation processing no longer obscures or convolves the oxide properties with those of: poly-Si or metal dep, poly doping, gate etch, or sinter anneal. The primary Quantox parameters monitored in the MOS fab are mobile ion concentration (Qm) and flat band voltage (Vfb).

See figure 1 for system schematic.

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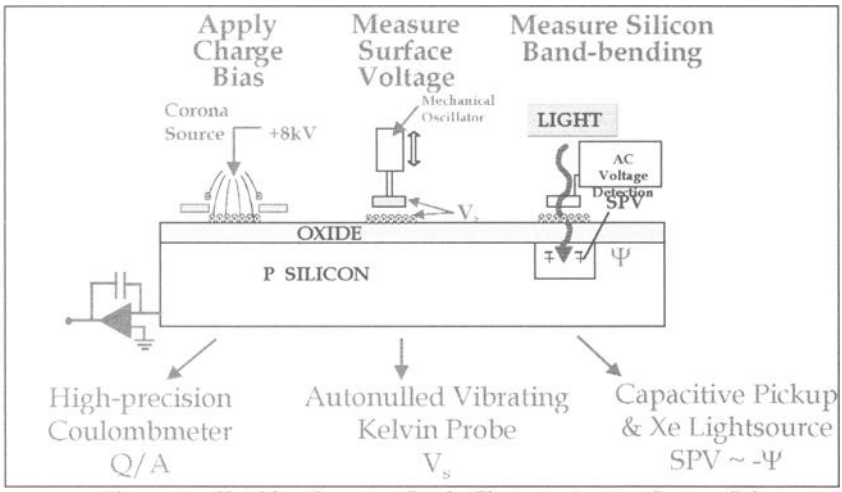


Figure 1 – *Keithley Quantox Oxide Characterization System Schematic*

Quantox Principle of Operation

The Quantox technique is referred to as corona oxide semiconductor (COS) and is analogous with the metal-oxide-semiconductor (MOS) system. COS uses deposited corona charge to bias the capacitor rather than an physical contact (via deposited gate material). In the former case, controlled charge deposition (from the corona source) controls the bias, permitting a complete sweep from inversion to accumulation. The COS system functions as a low frequency C-V plotter because the system remains in thermal equilibrium throughout the measurement, i.e., minority carriers and interface traps are able to follow the slow changes in corona charge. Much of the parameter extraction derives from the charge-surface voltage-surface photovoltage data (Q-V-SPV). The reader is referred to references [1-3] for a thorough description of the technique.

Flatband Voltage Determination (Vfb)

Flat band voltage (Vfb) is determined by first depositing charge and measuring both surface photovoltage and surface potential until a null photovoltage is detected. At this point the flatband condition has been reached.

Mobile Ion Concentration Determination (Qm)

The delta surface voltage before and after annealing under a low electric field is proportional to the mobile ion concentration (Qm). Details of the biasing and heating sequence are in the aforementioned references.

Interface Trap Density and Other Parameters

Additional Quantox measurement capabilities include: electrical dielectric thickness, interface trap density (D_{it}), total charge (Q_{TOT}), near surface doping , and generation or

recombination lifetime. Many parameters are extracted from the Q-V-SPV curve and are wholly analogous to the same parameters measured via the traditional MOS-C technique. Figure 2 shows an example of the measured Q-V and Q-SPV curves from which Dit, Tox and Vfb are determined.

In routine furnace control *of the fab*, only VFB and Qm were monitored. It was in this routine monitoring that *the fab* observed significant shifts in VFB for several "tank drive process" furnaces. Tank drive furnaces are used to perform a high temperature diffusion and activation of implanted phosphorus and boron that form P and N-well structures.

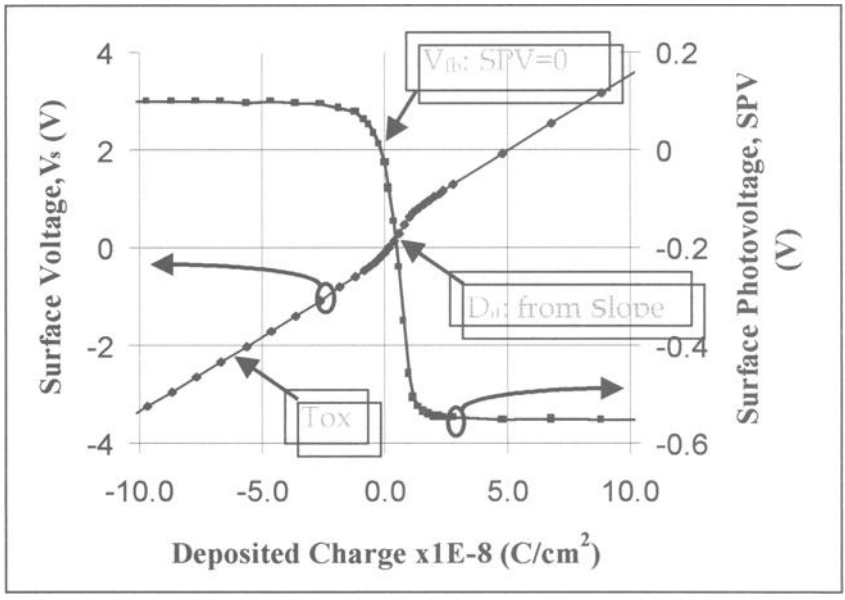


Figure 2 – *Quantox Q-V and SPV-Q Measurement Curves.*

Monitor Implementation

Quantox measurements were performed on the same oxide structure for all samples tested. The starting substrate was P <100> CZ silicon, 8-10 ohm-cm with low bulk oxygen concentration. Oxidation of these samples was performed in a vertical furnace using a special wet oxidation recipe. The oxide thickness target was 1000A. Following oxidation, the samples were measured using MCLT followed by Quantox testing. Three sites were tested per wafer with Qm, Vfb, Dit and generation lifetime being measured. Initial testing established target Vfb values at –1.0 V. Figure 3 summarizes the flatband voltage behavior for two sets of furnaces in the fab.

The figure also contrasts stable flatband voltage behavior (-1.0 ± 0.1V) of thin oxide furnaces with the unstable behavior of tank drive furnaces, which show larger, erratic Vfb. The shift in Vfb could be related to factors such as high interface trap density, leaky

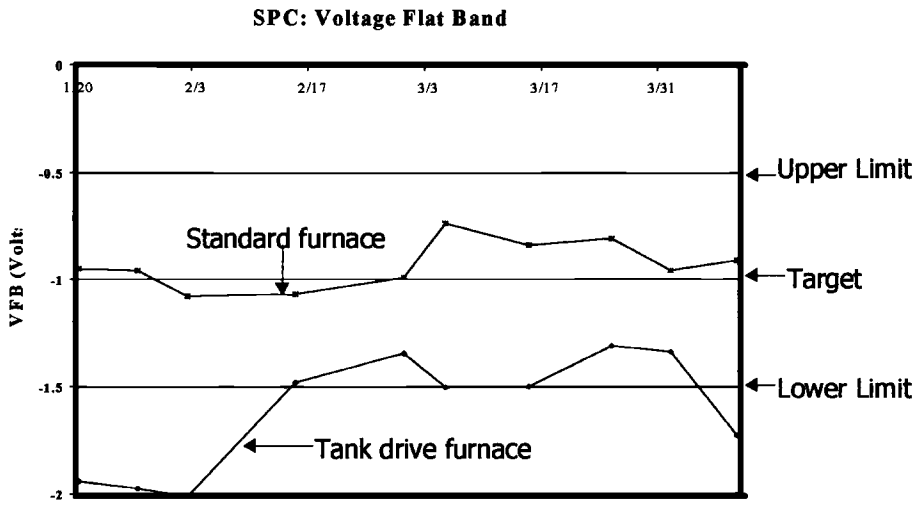


Figure 3 - *Process control flat band voltage for oxidation furnaces: Thin oxide versus tank drive furnaces.*

oxides, or high fixed charge. Analysis of additional measurements on the Quantox helped to clearly identify the source of this behavior.

Tank drive furnace data was compared to other oxidation furnaces, revealing a few additional discrepancies. For example, surface doping is typically 1.1E15 cm-3 for all oxidation furnaces but for tank drive furnaces, an error stating bad doping number (and a value of 1E18 cm-3) was reported. This was consistent with an N-type contamination signature because of the nature of the Quantox surface doping measurement. Doping is measured by first forming a field induced junction. This defines the area of the test region and isolates it by suppressing lateral diffusion. Then, the test site is pulsed into deep depletion and both the voltage change across the depletion region and the applied charge are measured. These values are used to calculate doping. The bad doping density numbers were consistent with N-type contamination because the Quantox couldn't form a depletion region due to the high minority carrier (N-type) concentration in the guard ring region. In other words, given a surface N-skin, while Quantox is attempting to bias a p-Si surface into depletion (by depositing positive charge) the surrounding guard ring region immediately supplies minority carriers (which collapses the junction).

Discussion of Tank Drive Monitor Results

Surface photovoltage measurements revealed a pattern of higher magnitude, negative SPV in the center compared to the edge of the wafer as shown in Figure 4. (the tool has the capability to map surface photo voltage across the wafer). The result is a picture

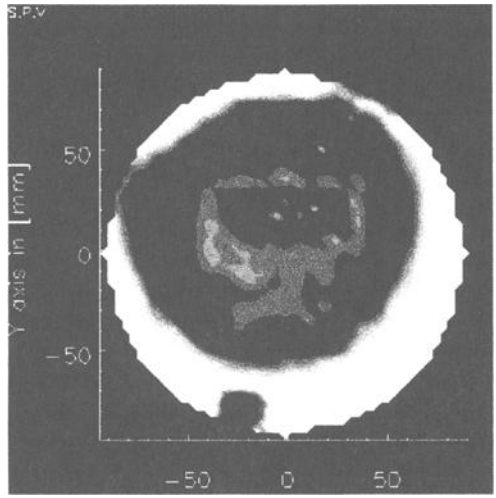
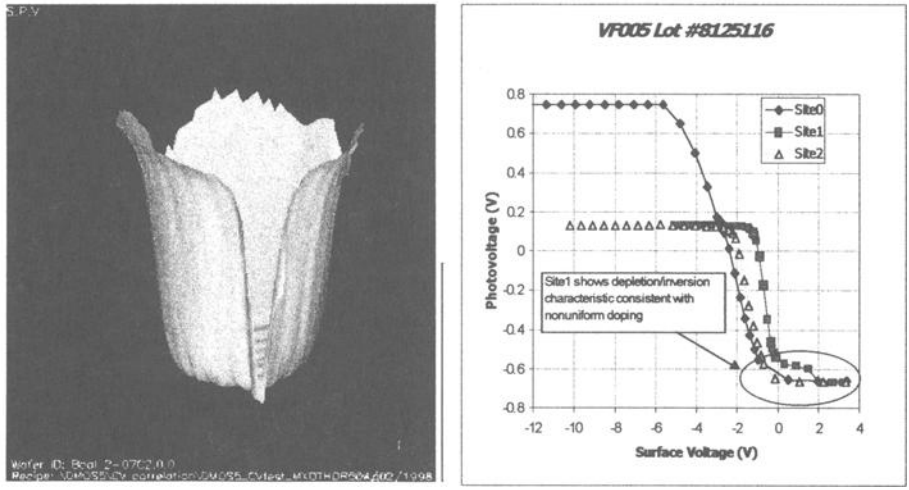


Figure 4 – *Surface Photovoltage Map on Tank Drive Wafer*



(a) (b)

Figure 5 - *(a) SPV 3D map of Phosphorus Contamination. (b) V-SPV curve on a tank drive furnace. Note the abnormally large swing in surface photovoltage for site #0.*

of the silicon band bending which would be influenced by n-type contamination. The 3D SPV map is shown in Figure 5a.

Surface doping and flatband voltage measurements were then repeated on additional center and edge sites. The Vfb results formed a pattern which ranged from aberrant in the center region of the wafer, to good or normal edge readings. Additionally, the V-SPV curve on a few sites had a distinctive "kink" and larger than normal range (see Figure 5b). In all cases, abnormal flatband voltage and doping data were observed in the center sites (shaded region of Figure 4). The larger than normal SPV range for the V-SPV sweep is highly suggestive of the presence of a junction, i.e., an n-type surface contamination.

These data contributed to the hypothesis that we were seeing the effects of phosphorus contamination. Armed with the electrical signature of phosphorus contamination, physical characterization via SIMS analysis was performed. The results showed an obvious phosphorus level difference between the center and edge sites on the wafer as seen in Figure 6.

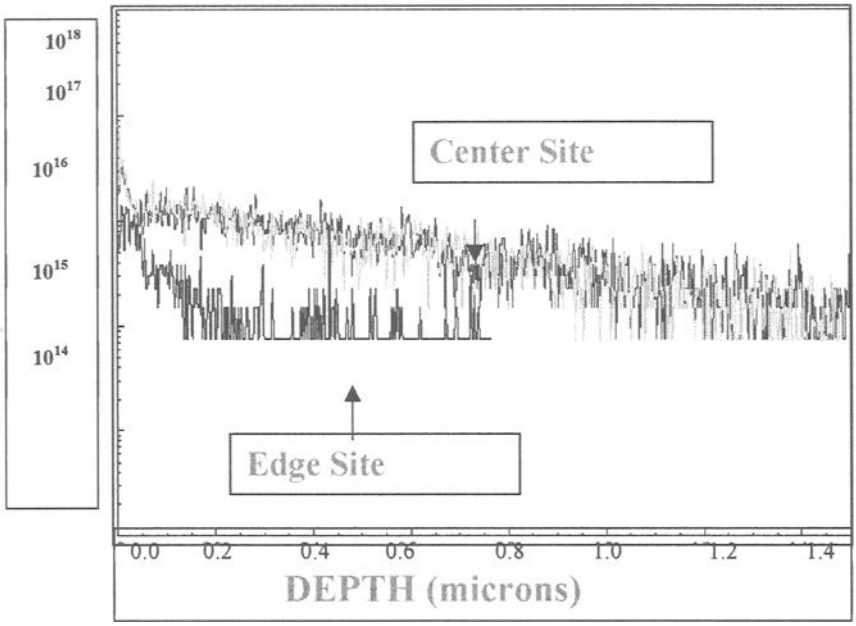


Figure 6 - *SIMS Analysis of Suspected Phophorus Contaminated Wafer. The phosphorus profile confirms that there is about an order of magnitude higher P level in the center of the wafer compared to the edge.*

Corrective Action and Link to Phantom Wafer Fails

Once the high Vfb and doping was attributed to phosphorus contamination, the next step was to identify the root cause. Also, given that the parametric failure occurred on wafer number five, which is typically the only wafer in the lot underneath a dummy wafer,

attention was focused on the furnace dummy wafers. Furnace dummies from all types of furnaces - even phosphorus furnaces - were selected for a special test oxidation run. In this test, pilot wafers were stacked beneath furnace dummies. A new wafer for Quantox analysis was placed directly beneath each furnace dummy wafer. The wafers were oxidized in a tank drive furnace with the weekly monitor recipe and then analyzed using Quantox and SIMS.

The results on the Quantox showed that the phosphorus contamination signature was achieved on the wafer directly underneath the phosphorus furnace dummy wafer. There was not much of a difference between samples under other types of furnace dummies. The phosphorus contamination signature was expected on the tank drive wafer but no flatband voltage shift was observed. Given that the contamination problem had always been intermittent, this was not too surprising. The change in Vfb and surface doping influenced by the surrounding furnace wafers is shown in Figures 7-8.

SIMS analysis on the wafers beneath the Phosphorus furnace dummy physically confirmed the Phosphorus contamination. Also, the same signature of shifted center and normal edge flatband voltages was observed. These findings supported the theory that the root cause is Phosphorus contaminated furnace dummies in tank drive furnaces. These furnace dummies cross contaminate the production wafer directly beneath the dummy wafer. Due to the furnace loading configuration of these furnaces the wafer in slot 5 of our cassette is loaded directly underneath a dummy wafer.

Dummy Wafer Control

Dummy Wafer Clean/Change - The final step was follow-up corrective action. The initial approach was to determine if exchanging old furnace dummies with brand new dummies would resolve the problem. Therefore one furnace was selected for dummy wafer change out. Another furnace was selected for dummy wafer cleaning as a more cost effective solution. We then ran the weekly oxidation test and measured the Quantox wafers. The results showed improved Vfb and surface doping in both furnaces except one test in the cleaned dummy furnace. This one test showed the bad signature of low Vfb and 1e18 surface doping. See Figure 9.

Dummy Clean Plus Oxidation – Additional dummy wafer preparation was attempted since dummy wafer contamination was still observed (indirectly via Vfb) shortly after dummy wafer cleaning. The cleaning procedure was modified to include a preprocess oxide growth step once the wafers were reintroduced to the furnace. This dummy wafer preparation was only partially successful. The contamination signature was still observed eventually.

Nitride Coated Dummy Wafers – Finally, nitride coated dummy wafers were used in the tank drive furnaces. The thought being that autodoping of both pilot and product wafers could be prevented by using a silicon nitride barrier. However, as before, this method was only partially successful.

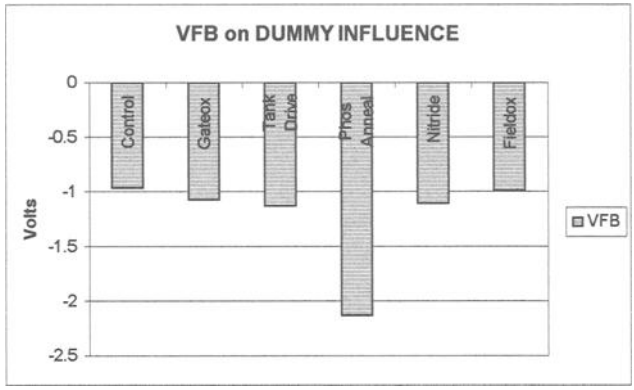


Figure 7 - *Furnace Dummy affect on Vfb*

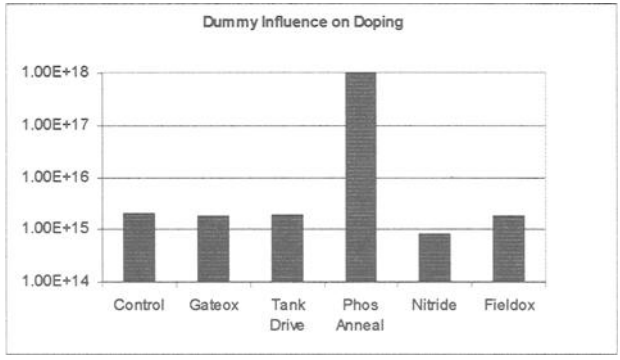


Figure 8 - *Furnace Dummy affect on Surface Doping*

Summary of Dummy Wafer Preparation Efforts

Having linked the so-called Phantom Wafer Fails to dummy wafers, several methods were attempted to eliminate the problem. Frequent change out of old dummies with new ones was not a cost effective solution. At the same time, all efforts at cleaning or sealing the dummy wafers eventually resulted in a return to the phosphorus contaminating state. The problem of dummy wafer effect on product proved difficult to resolve and in fact has not been. Resolved as shown in Figure 10.

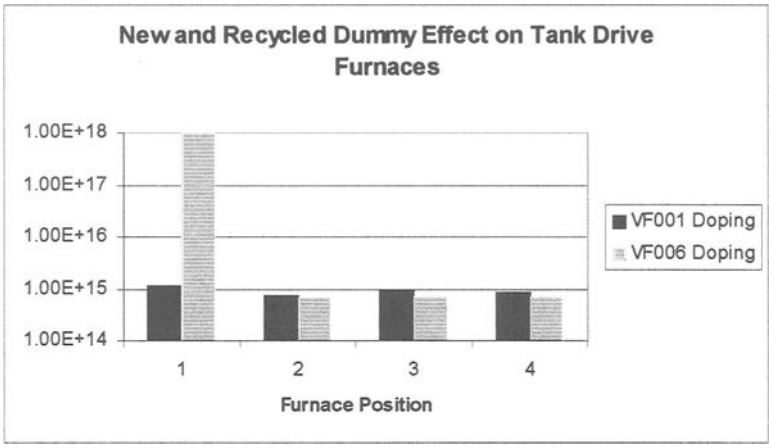


Figure 9 - *New and Cleaned Dummy effect on Surface Doping*

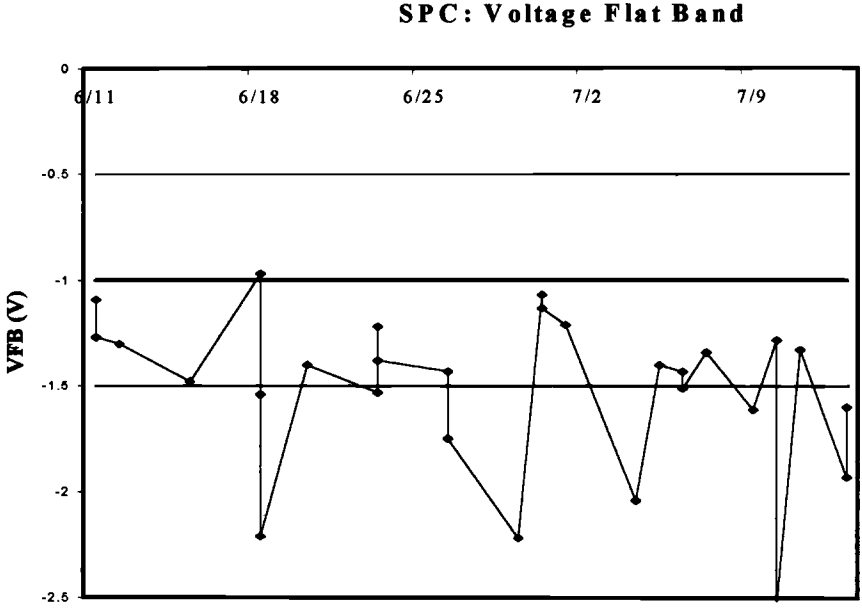


Figure 10 - *Summary of Wafer Changeout Efforts. Following each observed failure, some corrective action ,e.g., cleaning the furnace, changing the dummies, etc. was taken. Flatband voltage drift was still commonly observed for this group of furnaces.*

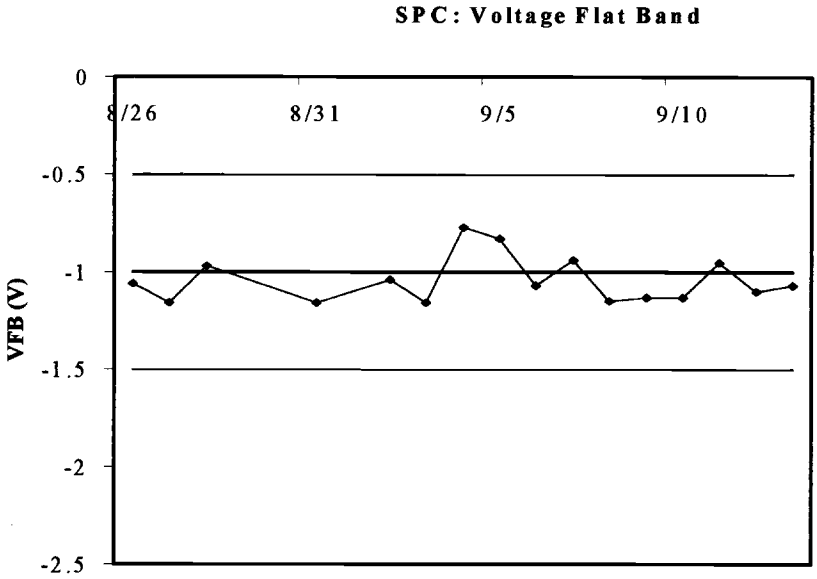


Figure 11 – *Tank Drive Furnace Flatband Voltage Following Corrective Action. Note the immediate improvement following implementation of modified furnace loading.*

Furnace Loading Effects

There is an alternative to normal furnace loading which places a dummy load above one wafer in each lot. The thermal load can be supplied by another product wafer rather than a dummy wafer. In this mode of furnace operation, the top position in the furnace would still be exposed to a non-production wafer. This potential problem was resolved by placing a monitor wafer in position above the topmost product wafer position within the furnace. This monitor wafer is changed out more frequently than the dummy wafers and is better controlled. The resulting flatband chart for the tank drive furnaces is shown in Figure 11. Although improvement was expected, the magnitude of the improvement was surprising. Immediate improvement in flatband voltage standard deviation and target values are apparent. This result further confirmed that dummy wafers were in fact the root cause of the observed erratic flatband voltage.

In addition, there was a measurable drop in Phantom Wafer fails at parametric which coincided with the introduction of modified furnace loading. The lessons learned from fab's tank drive furnace experience have been fanned out to other furnaces.

Conclusion

The source of a long-time cross-contamination problem was identified using the Quantox tool for furnace monitoring. A Vfb shift and bad doping number on the Quantox led to identifying the root cause of Phosphorus contamination. SIMS confirmed higher

phosphorus concentration. These results confirm the value of such a tool for rapid feedback and routine furnace monitoring.

By using the Quantox, we were made aware of a problem with our furnace processing and were able to verify the corrective action. Valuable insight was gained into a contamination source which had not been properly accounted for. The fact that we were unable to develop a reliable, inexpensive dummy wafer cleaning procedure was not at all expected. We therefore conclude that dummy wafers are an uncontrolled source of process variation and care must be taken to minimize their impact on product. One cannot assume that they are mere passive thermal loads. An alternate furnace loading method was eventually implemented in order to resolve the problem.

Acknowledgments

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Special thanks to George Brown, Texas Instruments, Inc for helpful insights provided.

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Michael R. Seacrist[1]

Application of Gate Oxide Integrity Measurements in Silicon Wafer Manufacturing

Reference: Seacrist, M. R., **"Application of Gate Oxide Integrity Measurements in Silicon Wafer Manufacturing,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382*, D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: The contribution of silicon starting material to device yield potential via gate oxide breakdown performance has grown in importance with the continually increasing levels of device gate area. Gate oxide integrity (GOI) testing is applied in silicon wafer manufacturing to determine the material-related capacitor defect density. GOI testing is used as a research tool and as part of a standard test set for evaluating and qualifying process changes from crystal pulling through final wafer cleaning. GOI measurements are also used to monitor finished wafer product quality. Other parallel material measurements are made for comparison and examined for correlation with GOI. Applications and results of GOI measurements in silicon wafer manufacturing are reviewed.

Keywords: silicon, oxide breakdown, gate oxide integrity, crystal originated pits or particles (COPs)

Introduction

The influence of silicon wafers on GOI has become a topic of intense interest in recent device generations. Advanced devices with sufficiently large gate oxide capacitor area can exhibit sensitivity to the starting material-related GOI defect density depending upon the defect characteristics of the wafer and the oxide thickness used in the application. The awareness of the silicon-related GOI defect density is reflected in the challenging GOI defect density goals for starting material in the 1997 National Technology Roadmap for Semiconductors [*1*]. The GOI influence of polished wafer starting material is strongly related to the density of vacancy-related point defect agglomerates from crystal growth [*2*]. The vacancy-related agglomerates intersecting the wafer surface are partially detected and not accurately separated from particles in laser light scattering surface inspection as light scattering events. These light scatterers are commonly referred to as crystal originated pits or particles (COPs) [*3*]. The vacancy-related agglomerates can also be detected as flow pattern defects (FPDs) in decorative etching. Polished wafers with fewer or no vacancy-related point defect agglomerates, and epitaxial wafers with a complete absence of these defects have low GOI defect

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densities. Example data are presented later.

The aim of GOI measurements in silicon materials fabrication is to determine the material-related GOI defect density and identify the processes that have an influence. GOI testing has been used extensively as a research tool to measure responses to changes in the crystal pulling process. The influence of the wafering, polishing, and cleaning processes on GOI must also be taken into account in order to understand clearly the signals from crystal growth related defects. GOI testing is applied throughout the silicon manufacturing process to test new processes, and process and equipment changes. The GOI test is commonly applied after thermal simulations of IC fabrication processes to determine responses to oxygen precipitation. GOI sampling is also performed to monitor the finished product. GOI testing is done in conjunction with the measurement of other material parameters such as local light scatterers, micro-defects, metallics, surface roughness, and others.

Capacitor Fabrication, Testing, and Data Analysis

Simple polysilicon gate MOS capacitors are fabricated using the following process flow:

Capacitor Fabrication

Gate Oxidation – 200 angstroms nominal thickness
Polysilicon Deposition – 4000 angstroms nominal thickness
Polysilicon Doping – POCl3 furnace doping
Capacitor Pattern – varying capacitor areas
Polysilicon Etch
Backside Contact – oxide removed and backside metal deposited if needed for lower resistance contact

This simple capacitor process flow forms planar gate oxide capacitors. MOS capacitors of varying areas are fabricated. The focus of this GOI testing is to determine the material related GOI defect density so large area capacitors are tested. The capacitor areas are typically in the 0.1-0.4 cm^2 range. On a 200mm wafer approximately 150 capacitors are tested in a pattern that covers most of the wafer. The capacitor area and the number of capacitors tested, along with the capacitor preparation influence, ultimately determines the defect density resolution for the material. Using Poisson's statistics, Figure 1 shows the calculated relationship between the capacitor area and defect density resolution for varying levels of population defectivity.

The defect background added by the capacitor preparation process is monitored by adding epitaxial wafers to a GOI test batch. Epitaxial wafers are not subject to the GOI influences of crystal point defect agglomerates or the potential polishing-related surface effects as on polished wafers. Figure 2 illustrates the use of epitaxial wafers used as preparation monitors by comparing GOI yields in a sequence of evaluations of conventional vacancy-rich polished wafers. The epitaxial wafers essentially provide a "perfect" GOI reference from which to identify preparation induced defects.

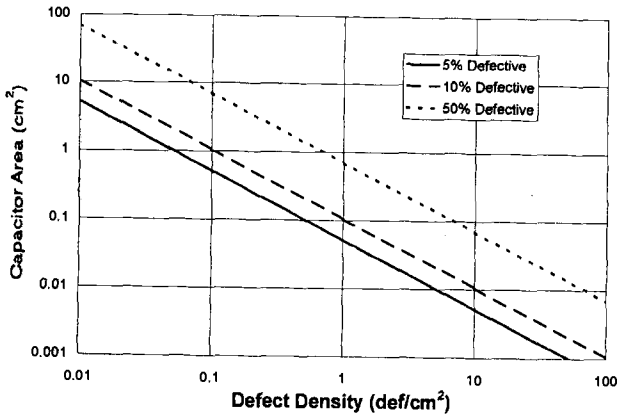

Figure 1 – *Capacitor area and defect density resolution.*

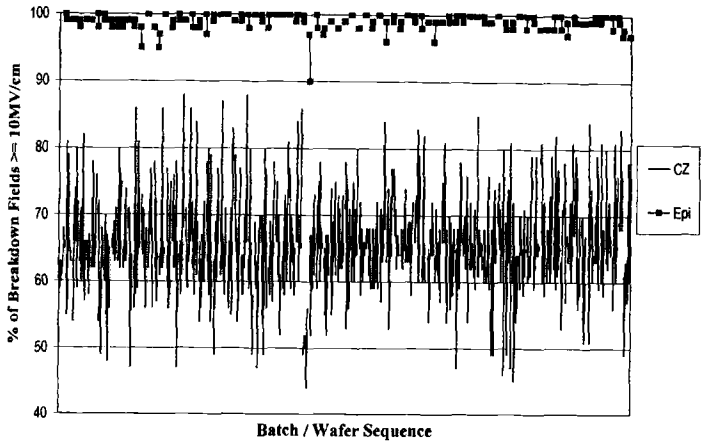

Figure 2 – *Monitoring capacitor preparation influence with epitaxial wafers.*

The primary electrical test is a voltage ramp test. The linear ramp rate is nominally set at 0.5 V/sec. Judgement of the breakdown condition is set at either a fixed current density limit (soft breakdown) or at the destructive breakdown point. The purpose of the test is to resolve the low to medium electric field failures caused by crystal point defect agglomerates. These defects have not been observed to exhibit time dependent breakdown behavior so the time dependent dielectric breakdown tests (TDDB, QBD) are not commonly applied. They may be necessary when the focus of material-related GOI testing shifts from micro-defects to other phenomena.

The current-voltage characteristic is recorded during the ramped voltage test and is compared against the expected Fowler-Nordheim (FN) tunneling current characteristic for the oxide thickness under test. Shifts in the current-voltage characteristic from the expected tunneling current are indicative of surface characteristics that are not micro-defect related. A current-voltage characteristic consistent with expected FN tunneling is a condition that must be met in order to attach significance to the distribution of oxide breakdown fields.

Data analysis methods are aimed at determining the capacitor defect density as a function of field or stress level, and separating different modes of oxide breakdown. Distributions of breakdown fields are transformed into Weibull plots and defect density estimates using Poisson's statistics:

$$Y(E) = e^{-(A*D(E))} \quad (1)$$

where Y(E) is the yield at some defined electric field level, A is the capacitor area, and D(E) is the capacitor defect density at some defined electric field. The applications of these statistical methods for GOI data analysis are described in detail elsewhere [*4*].

An example wafer output from the ramped voltage test is shown in Figure 3 for a vacancy-rich polished wafer. The wafer was tested with a soft breakdown current density limit of 1 ma/cm^2. The plot shows the typical elements examined in a ramped voltage test (clockwise from top-left): 1) breakdown field map, 2) tunneling current scatterplot showing the last prior to reaching the current density limit versus the solid line showing the predicted Fowler-Nordheim tunneling, 3) histogram and cumulative failure plot of the breakdown fields, and 4) a Weibull plot of the breakdown fields.

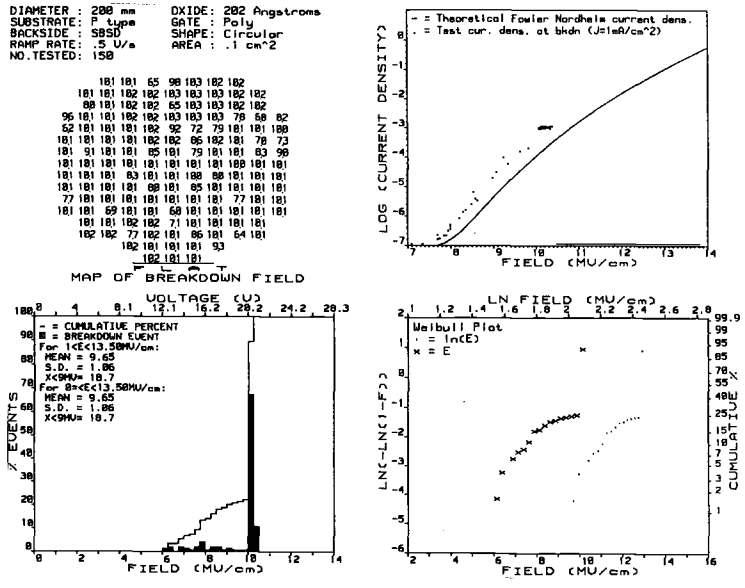

Figure 3 – *Ramped voltage test output showing field map, J-E plot, and statistics.*

The influence of the oxide thickness on oxide defect density has been reported previously [5]. A gate oxide thickness of 200 angstroms is used to ensure that the test is sensitive to the material defects while remaining in a technically relevant oxide thickness range. Tests continue in order to determine the impact of oxide thickness on oxide defect densities for crystals grown under conditions that result in varying levels of vacancy-related defect agglomerates. Recent comparisons of oxide defect density between 200 and 50 angstrom gate oxides for wafers from the same crystals are reported in the next section, and will show that 200 angstrom oxide is sensitive to the vacancy-related defects while 50 angstrom oxide is not.

Applications of GOI Measurements

Crystal Growth

As discussed earlier, the influence of crystal growth related point defect agglomerates has been the main area of GOI research. A review of these point defect phenomena during crystal growth is covered elsewhere [6]. GOI defect densities have been correlated with the presence of vacancy-related defects detected as COPs. Many of the COPs are too small to be detected at the current size threshold of laser inspection systems. Repeated SC1 cleans enlarge the COP related light scatterers to the point where they can be detected and better separated from particles in laser surface inspection. Experiments to relate GOI with 200 angstrom gate oxide and COP levels have been performed using CZ wafers grown and annealed under various conditions to achieve varying COP densities. Figure 4 shows the correlation between capacitor defect density and light scatterers from the initial polished wafer laser inspection. Figure 5 shows the correlation between capacitor defect density and laser inspection after the polished wafers were processed through four extended SC1 cleaning cycles. Note the excellent correlation between the number of COPs and the capacitor defect density with the enlargement of the COPs after the additional SC1 cleaning cycles. Correlations have also been established between GOI and vacancy-related flow pattern defects highlighted by decorative etching.

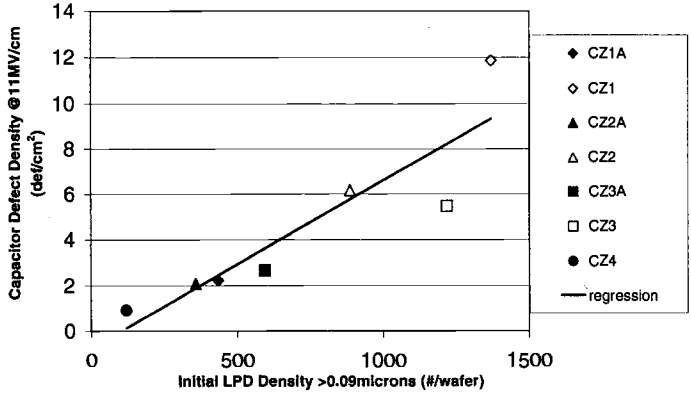

Figure 4 – *Capacitor defect density compared against initial light scatterer level.*

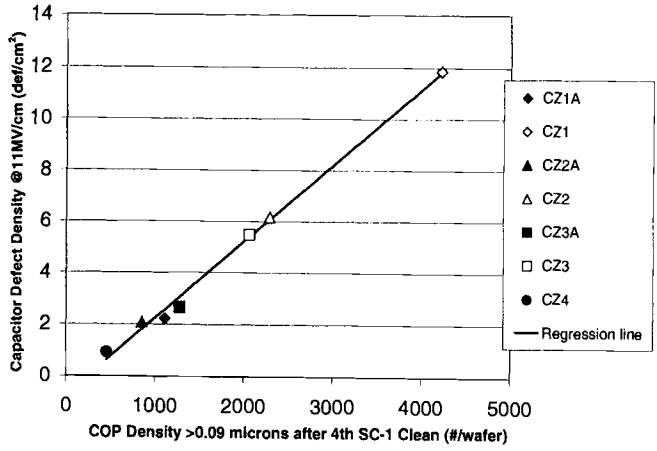

Figure 5 – *Capacitor defect density compared against light scatterers detected after four extended SC1 cleans.*

Depending on the crystal growth conditions a wafer can be completely of the vacancy point defect type, the interstitial point defect type, or contain both. Interstitial defects do not limit the GOI yield but can create junction leakage related yield issues in device fabrication. Oxide breakdown maps an effectively highlight the presence of a within wafer pattern when there is a point defect boundary between vacancies and interstitials. The oxide breakdown pattern corresponds well with COP patterns detected by light scattering after extended SC1 cleans.

GOI comparisons of wafers made with different crystal pulling processes are made routinely. An example of such a comparison is shown in Figure 6 for a 200 angstrom GOI test. Capacitor defect densities were calculated from the distribution of breakdown fields. The varying COP levels in the CZ materials were achieved by varying the crystal pulling and cooling rates. Epitaxial wafer results are also plotted for comparison in Figures 6 and 7. Note the strong sensitivity of capacitor defect density to the COP level for the 200 angstrom gate oxide. The epitaxial wafer and the CZ wafer with no COPs exhibit essentially the same performance. Wafers from the same set of crystals were also tested at an oxide thickness of 50 angstroms and the resulting defect density plot is shown in Figure 6. The 50 angstrom gate oxide did not exhibit a measurable sensitivity to the varying COP levels. The capacitor defect density resolution is estimated to be approximately 0.2 defects/cm^2 for the number and area of capacitors tested for both oxide thicknesses. These results are consistent with other reports of similar experiments [*7*]. Models have been proposed to explain the decreasing vacancy-defect sensitivity of thinner gate oxide [*8*].

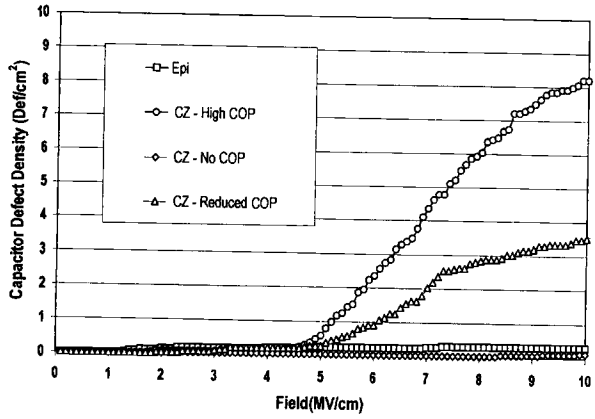

Figure 6 – *Capacitor defect density comparison for varying COP levels with 200A oxide.*

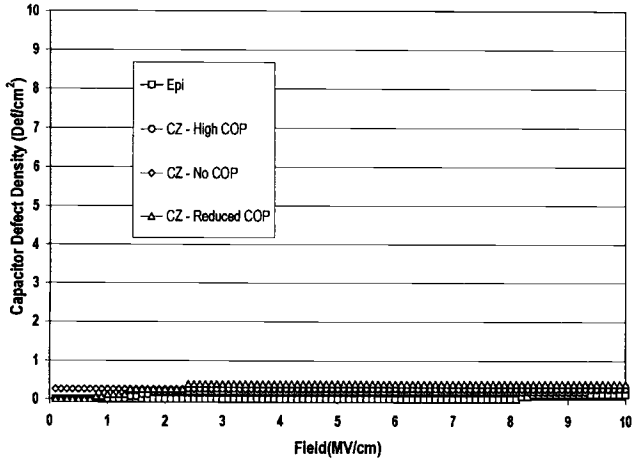

Figure 7 – *Capacitor defect density comparison for varying COP levels with 50A oxide.*

Wafer Processing

The influences of the wafering, polishing, and final cleaning processes on GOI have not been studied as extensively and are not as well understood as the crystal contribution. The wafer processing has been developed such that no GOI influence is normally detected above the crystal limited background in the 200 angstrom ramped voltage test. When crystal related defects are sufficiently reduced, the GOI influences related to other characteristics of the wafer may be found. Factors such as surface microroughness and metals do not have degrading effects on GOI within normal bounds of modern silicon material. Conditions can be forced by intentional contamination or intentional roughening of the surface that will degrade GOI.

By processing epitaxial wafers, expected to have very low GOI defect densities, through wafer processes such as polishing and cleaning the GOI degradation from those processes can be monitored. The characteristics of these processes have been developed so that there is typically no GOI degradation associated with them. Monitoring the GOI influence of these processes, though, can help to identify upset conditions that degrade GOI. GOI tests are part of the standard set of tests used to qualify changes in the wafer processes.

An example of the surface influence on GOI is illustrated in an example of epitaxial wafers that had experienced degradation haze while stored in a wafer cassette. The haze was determined by laser surface inspection. The GOI response for wafers tested with the hazed surface condition showed a shift in the current-voltage behavior with the onset of tunneling current at a much lower voltage for the same oxide thickness. Oxide thickness was measured to be normal both optically and electrically. Because of the shift in the current-voltage characteristics the breakdown fields judged at the soft breakdown current density limit appeared to have shifted in the associated breakdown field distributions. By re-cleaning a separate set of wafers from the same batch with the identical surface haze condition and then performing the GOI test, it was demonstrated that the surface condition causing the shifted current-voltage behavior was easily removed, and the current-voltage curves and the breakdown field distributions returned to normal. This type of removable surface influence does not represent a true GOI defect and does not influence the gate oxide performance in IC fabrication. These type of surface influences highlight the importance of first examining the current-voltage characteristic against expected tunneling current behavior before attaching significance to the distribution of breakdown fields.

Product Monitor

GOI testing is not typically applied to qualify wafer shipments. Other material parameters are measured to determine the suitability of wafers for shipment. GOI testing is applied routinely to a sampling of product wafers in order to monitor performance and identify any upset conditions relative to an established GOI performance baseline that may not be captured by other material measurements.

Designing GOI Experiments

GOI experiments are routinely conducted to test process responses. In order to avoid uncertainties that will make interpretation of results difficult, these experiments must be carefully designed. Comparative tests are necessary to accurately measure the GOI influence of a process change. When testing a process change, such as polishing slurry A versus slurry B, the test wafers must be from the same crystal and crystal position. They ideally have been processed in the same batch through all prior and subsequent process steps, and then evaluated in the same GOI test batch. The potential GOI signals can be further amplified by using an epitaxial or other similar "perfect" GOI type wafer. This enables the test to have maximum sensitivity to any degrading effects of the variables being tested, and to minimize the noise from other factors that influence GOI and may not be completely homogeneous within the test wafer set.

GOI Challenges

Silicon wafer-related GOI sensitivity has driven silicon wafer suppliers to develop wafers with lower and with zero vacancy-related defects. New crystal processes have been developed that completely suppress the formation of GOI degrading point defect agglomerates resulting in CZ wafers that have GOI performance equivalent to epitaxial wafers. Recent data, including results reported here, question the sensitivity of thinner gate oxides to the vacancy-related defects. A more complete understanding of thin gate oxide material sensitivities and a physical model that describes the influence of COPs on oxides must be developed. Beyond the crystal-related defects there are also challenges to understand the degree to which other wafer properties such as the smoothness and purity of the surface will influence thin oxide GOI.

Additional challenges include measuring wafer GOI performance against industry roadmap goals. Detection limit capabilities as a function of capacitor size and number of capacitors / wafers tested have to be assessed. Ultra-thin oxide capacitor preparation and testing may also be a challenge to silicon wafer suppliers.

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Silicon Substrate Related Gate Oxide Integrity at Different Oxide Thicknesses

Reference: Grann, E. D., Huber, A., Grabmeier, J., Hölzl, R., and Wahlich, R., **"Silicon Substrate Related Gate Oxide Integrity at Different Oxide Thicknesses,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382*, D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: Gate oxide integrity (GOI) testing is a valuable tool for the characterization, development and optimization of tailor-made silicon (Si) substrates for the integrated circuits industry. Different Si substrates with various numbers of grown-in defects have been evaluated using charge-to-breakdown measurements. Yield and defect density analyses are studied for oxide thicknesses in the range from 40 nm down to 5 nm. The sensitivity and impact of grown-in defects, here predominantly crystal-originated particles (COPs), for different material groups on gate oxide reliability are shown in detail. In addition, results are presented on gate oxide degradation due to intentional metallic (Ni, Cu, Fe) contamination of various wafer types.

Keywords: gate oxide integrity, silicon, crystal originated particles (COPs), metallic contamination, nickel (Ni), iron (Fe), copper (Cu), oxide thickness

Introduction

Gate oxide integrity (GOI) testing is a powerful technique for material and process characterization for both integrated circuits manufacturers and Silicon (Si) substrate suppliers. Crystal and surface properties reflect themselves in the reliability of gate oxides. It is known that grown-in defects such as voids in bulk Si delineated as crystal-originated particles (COPs) after prolonged SC1 cleaning ($NH_4OH/H_2O_2/H_2O$) negatively affect the gate oxide breakdown behavior. Gate oxide failures yield valuable information for the optimization of crystal growth parameters and the related role of defect structures. Furthermore, the dependence of GOI on the thermal history of an ingot, process technology (e.g. gate dielectrics, gate materials, cleaning), and the transition from vacancy-rich to interstitial-rich material are key issues to increase integrated circuit (IC) performance and device yield [*1*].

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This paper examines the use of gate oxide integrity measurements as a method of monitoring substrate related defects and developing advanced Si crystals. Wafers were selected from ingots which had been grown with different cooling rates, thereby varying the size, number, and distribution of the crystal-originated particles (COPs) present in the wafer [*2*]. By also changing the thicknesses of the gate oxides, it is possible to study the sensitivity of GOI to substrate defects.

Insidious heavy metal contaminants, such as iron, nickel and copper can detrimentally affect the performance of devices fabricated on silicon wafers [*3,4*]. The effect of iron, nickel and copper contamination on the gate oxide integrity for different substrates and different gate oxide thicknesses was investigated.

Experiments

All of the samples used in this study were boron-doped p-type wafers with a (100) orientation. Three basic types of wafers were used: polished 200 mm Czochralski grown (CZ) and 150 mm float zone grown (FZ) substrates, and 200 mm epitaxial p/p+ wafers.

Additionally, contamination experiments were performed on 150 mm FZ and 150 mm p/p+ epitaxial wafers. These wafers were intentionally contaminated with Ni, Cu and Fe in the range of 6×10^{11} at/cm^2 to 2×10^{12} at/cm^2 by a well defined spin-coating method. As a reference, a blank solution was spun on a control wafer. After contamination, a drive-in step thermal cycle was done in an argon atmosphere at 800°C for 30 min for the Ni and Cu wafers and at 1000°C for 30 min for the Fe wafers. The cooling rate was about 50°C/min. in all cases. Each test group was run in a separate thermal cycle to minimize cross contamination effects. After a modified RCA clean, metal oxide semiconductor (MOS) capacitors were fabricated with an oxide thickness of 25 nm.

In a further contamination experiment, polished 200mm CZ wafers were spin-contaminated with 5×10^{12} at/cm^2 Ni. Afterwards these wafers were subjected for several hours to a thermal cycle which simulated a typical CMOS process. Again, the wafers underwent a modified RCA clean and MOS capacitors were fabricated. In this case, however, the MOS capacitors had oxide thicknesses of 17 nm, 7.5 nm and 5 nm.

The MOS capacitors used in all of the measurements were prepared and measured in the same way. Oxides were grown on the sample wafers to the desired thickness using a dry oxidation process. The 8 mm^2 gate areas were made of phosphorus doped poly-silicon. The gate oxide integrity measurements were performed by testing 100 capacitors on each wafer using the gate injection mode.

A current density was gradually stepped from J = 1 μA/cm^2 (electric field E < 5 MV/cm) to monitor early breakdowns, up to a maximum value (E > 12 MV/cm) to detect intrinsic gate oxide failures. Breakdown is defined to occur when the monitored voltage dropped by more than a preset amount between successive measurements. The total charge density to breakdown Q_{bd} is determined by the time integral of the injected current density. Assuming a Poisson distribution of defects, the wafer's defect density at a particular charge density, $D(Q_{bd})$, is calculated using the following equation [*5*]

$$D(Q_{bd}) = -\frac{\ln(1-\frac{N_{failed}}{N_{total}})}{A_{gate}} \qquad (1)$$

where N_{failed} is the number of capacitors which failed below the specified Qbd value, N_{total} is the total number of capacitors tested, and A_{gate} the gate area. Typically, for defect density calculations, $Q_{bd} = 0.1$ C/cm^2. In addition, a yield is calculated by simply determining the percentage of capacitors which fail below a specified Q_{bd} value. For yield calculations, a Q_{bd} of 5×10^{-4} C/cm^2 is used. This lower Q_{bd} value for the yield calculation corresponds well to failures below 10MV/cm extracted from time zero dielectric breakdown (TZDB) measurements.

Results and Discussion

Wafers from CZ grown ingots with different, decreasing, cooling rates, denoted by CZ1 to CZ4, and wafers from a very slowly pulled and therefore interstitial-rich ingot, labeled CZ5, are compared with epitaxial and FZ wafers for an oxide thickness of 25 nm. Ingot CZ1 was the fastest cooling, while ingots CZ2, CZ3, and CZ4 all cooled for monotonically longer times. The yield and defect density results are summarized in Figure 1a and 1b, respectively. The wafer yields increased with cooling time; from CZ1 with a nearly 30% yield to CZ3 and CZ4 with yields around 65%. Wafers from CZ5, the FZ ingot, and the epitaxial wafers all showed yield values around 99%. The defect densities $D(Q_{bd} = 0.1$ C/cm$^2)$ correlated well with the yield data. The CZ5, FZ, and epitaxial wafers all had defect densities below 0.5 cm^{-2}; wafers from CZ1 had the highest defect density of around 17 cm^{-2} while CZ2, CZ3, and CZ4 were all about 6 cm^{-2} to 10 cm^{-2}. The COP density evaluated by light point defect (LPD) measurements (> 0.12μm) after 4 h SC1 treatment correlates well with the GOI defect density $D(Q_{bd})$ calculated at $Q_{bd} = 5 \times 10^{-4}$ C/cm^2. The COP densities of FZ and epitaxial wafers are about two orders of magnitude lower than CZ4. This suggests that it is the very low COP density that is responsible for the high yield in FZ and epitaxial wafers as well as in the interstitial rich material CZ5. Simulations taking into account the thermal history and the intrinsic point defect spectrum confirm the important role of the COP density for GOI [6]. In Figure 2, the COP density distribution is plotted as a function of the void size for CZ1 to CZ4. The detection limit for COPs in a LPD counter after SC1 treatment is approximately 0.12μm, as indicated in Figure 2. A four-hour SC1 treatment can reveal COPs so small that even those present in CZ1 can be measured. The integral of the COP density distribution over the different void sizes is comparable to the measured COP density. With increasing ingot cooling rates, the COP density distribution shifts to smaller void sizes with increasing peak values. The high COP density therefore results in a low yield and a high defect density.

The Weibull distributions for GOI measurements made on capacitors with different oxide thicknesses on CZ3 are shown in Figure 3. For oxide thicknesses between 5 nm and 25 nm the cumulative percentage of failures at $Q_{bd} = 0.1$ C/cm^2 are nearly constant, indicating that these samples have the same defect densities. The strong increase in the slope of the curve for the 40 nm thick gate oxide between 0.01 C/cm^2 and

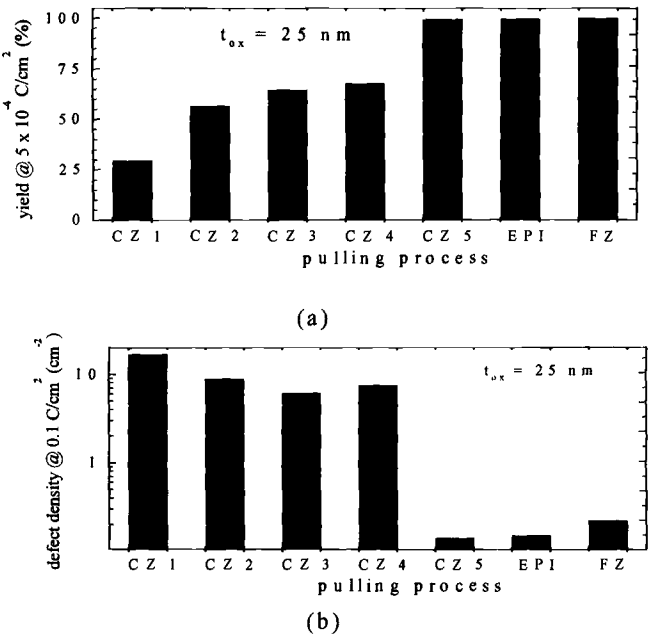

Figure 1 - *(a) Comparison of different wafer yields at Q_{bd} = 5 x 10^{-4} C/cm^2, (b) Comparison of different wafer defect densities at Q_{bd} = 0.1 C/cm^2.*

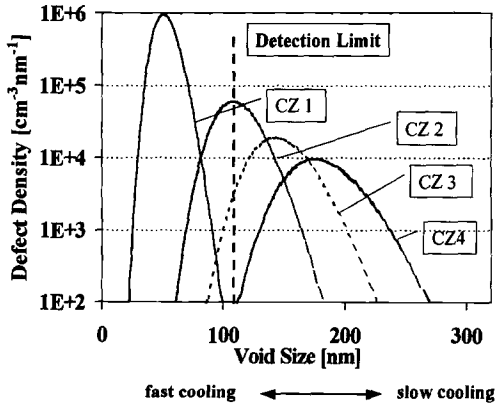

Figure 2 - *COP defect density as a function of void size for differently cooled crystals* [6].

0.1 C/cm^2 is not fully understood. The sharp increase in the slope of the Weibull plots around 1 x 10^{-6} C/cm^2 is due to gate oxide failures caused by COPs.

For a gate oxide thickness less than 7.5 nm, the influence of COPs on oxide breakdown is significantly reduced. This may be due to local thinning of the gate oxide at the COP site that is more pronounced for thick gate oxides, leading to fewer COP failures in capacitors with thinner gate oxides [*7,8*]. Figure 4 shows the same oxide series for epitaxial wafers. Evidently, nearly no COP failures are observed around Q_{bd} = 1 x 10^{-6} C/cm^2 leading to a high yield and low defect densities.

The sharp increases in the slope in both Figure 3 and Figure 4 beyond Q_{bd} = 0.1 C/cm^2 indicate intrinsic gate oxide failures. The Q_{bd} value where 90 % of the capacitors have failed has been taken as a measure of the intrinsic oxide strength. The results are summarized in Figure 5, where the 90 % Q_{bd} value is plotted as a function of oxide thickness. Starting at an oxide thickness of 5 nm, the Q_{bd} values first increase, reaching a maximum at 12.5 nm, and then decrease. Both CZ and epitaxial material show the same behavior and peak position. This effect can be explained in the following way: as gate oxide thickness increases, the influence of roughness at both the phosphorus doped poly-silicon/SiO_2 and the SiO_2/Si interfaces decreases, resulting in higher intrinsic Q_{bd} values. It is believed that the Si surface properties and not the Si bulk play the dominant role for thin oxides (< 10 nm). The decrease of Q_{bd} in Figure 5 for thicker oxides can be explained by the incorporation of more and more Si into the oxide during the gate oxidation, leading to a weaker intrinsic oxide [*9*]. Both effects may lead to a peak in the Q_{bd} value for a certain oxide thickness.

The remainder of our experiments involved the influence of metallic contamination on GOI. In the first experiment, we studied the influence of iron, nickel and copper on the gate oxide integrity using a gate oxide thickness of 25 nm. The FZ wafers had no external gettering on the wafer backside in order to fully evaluate the effect of the contamination. Furthermore, the oxygen content was less than 2 x 10^{16} at/cm^3 and should thus not contribute to any internal gettering effects. The results are presented in Figure 6. Our experiments revealed that iron is by far the most serious contamination metal affecting GOI yield. Nickel affects GOI less than iron but is still highly detrimental, whereas Cu contamination is much less critical for GOI. After removing carefully poly-crystalline Si and the gate oxide from the wafers and etching them for 2 minutes in a Wright etchant, Ni haze was found under the GOI structure. We therefore suggest that it is these nickel silicides that mainly degrade GOI yield [*4*].

The impact of iron and nickel contamination on gate oxide breakdown for 150mm p/p+ epitaxial wafers is shown in Figure 7. The p/p+ epitaxial wafers can getter metal impurities due to the heavily boron doped (10-15 mΩcm) silicon substrate and mechanical backside damage. Iron and nickel contamination affects the GOI yield on these wafers much less than on the FZ wafers with no gettering sites. GOI measurements are thus a sensitive technique to examine different gettering mechanisms in silicon wafers. The small influence of the metal contamination compared to virgin wafers near the intrinsic breakdown is not due to metal silicide formations under the GOI structure because, after removing the polycrystalline Si and oxide layers, we did not find any metal haze after preferential etching.

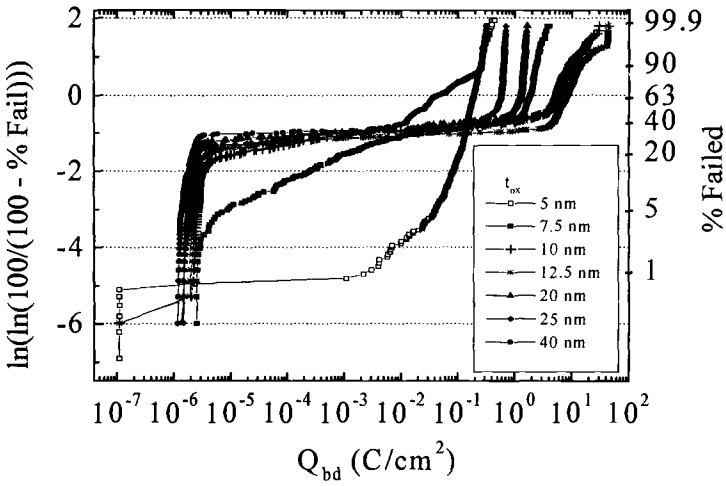

Figure 3- *Weibull distributions for different oxides grown on polished wafers.*

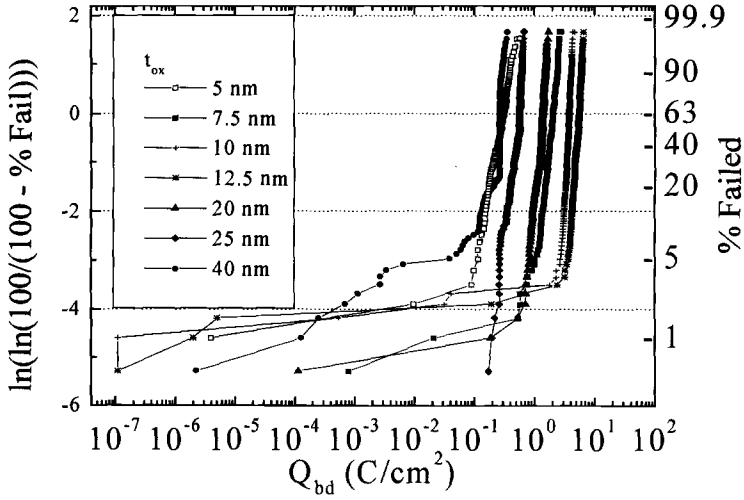

Figure 4- *Weibull distributions for different oxides grown on p/p+ epitaxial wafers.*

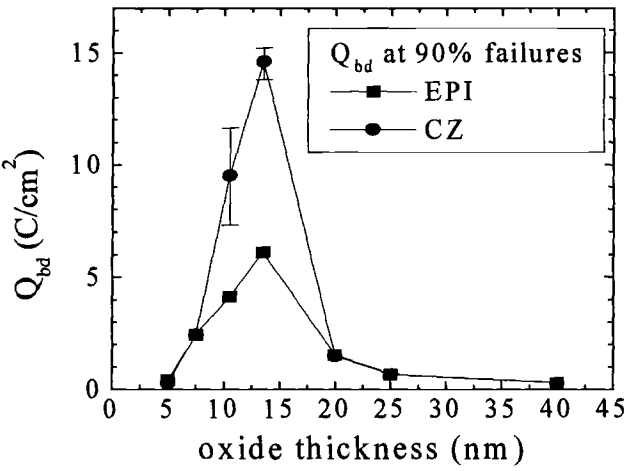

Figure 5- *Intrinsic oxide strength as a function of oxide thickness.*

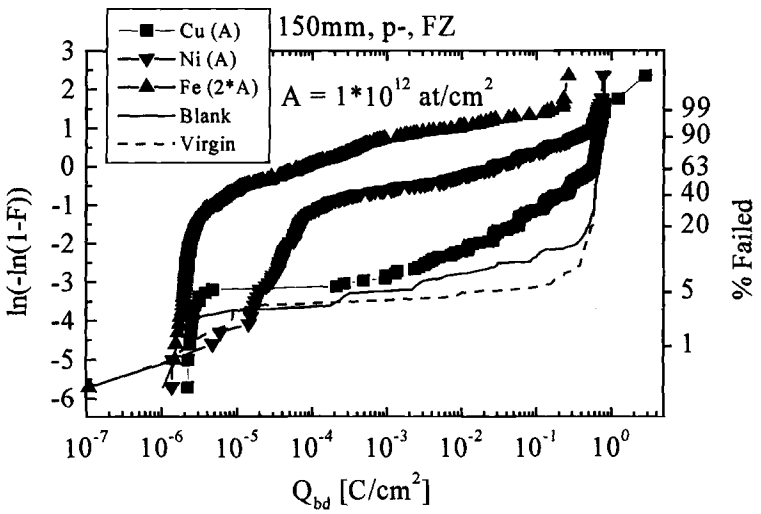

Figure 6 – *The effects of copper, nickel, and iron contamination on the GOI performance of float zone wafers.*

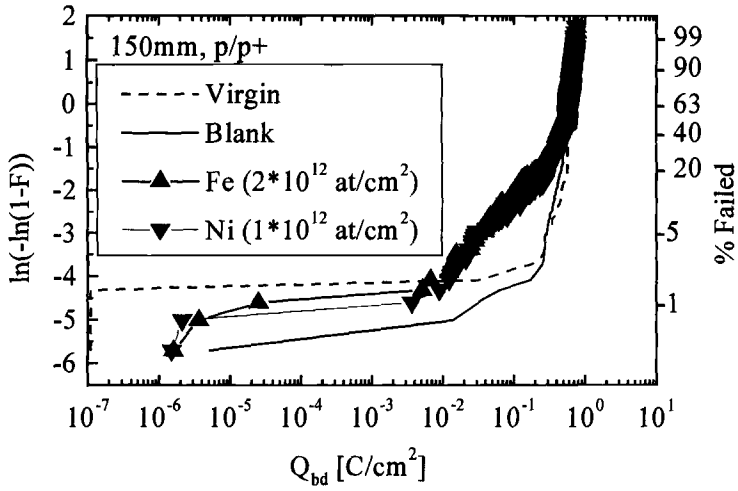

Figure 7 – *The effect of nickel and iron contamination the GOI performance of p/p+ epitaxial wafers.*

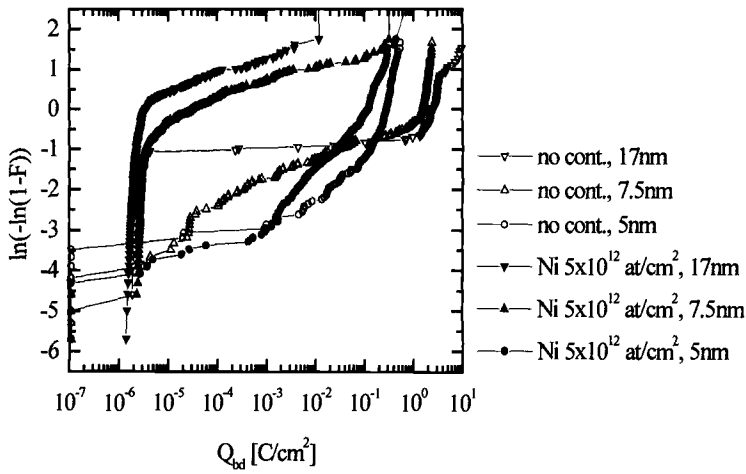

Figure 8 - The effect of nickel contamination on the GOI performance of polished CZ wafers at different oxide thicknesses.

In a second set of experiments, MOS capacitors with different gate oxide thicknesses were fabricated on Ni contaminated (5 x 10^{12} atoms/cm^2) 200 mm CZ wafers. The results are shown in Figure 8. Note that F is the cumulative percentage of failures, N_{failed}/N_{total}. The nickel contamination strongly affects the GOI behavior at an oxide thickness of 17 nm. Reducing the oxide thickness leads to a reduction in the influence of COPs and also of the Ni contamination. At 5 nm the contamination is far less critical than at 17 nm. This suggests that ultra-thin gate oxides are much less sensitive to COP failures and Ni contamination. For 5 nm gate oxides pre-breakdowns start to occur for Q_{bd} values below 1 x 10^{-6} C/cm^2. These might also partially be a result of the whole furnace process itself and be even more evident for gate oxides thinner than 5 nm. Furthermore, it was reported that so-called A-mode failures strongly increase below 7 nm [*10*].

Conclusions

It has been demonstrated that the COP density in Si crystals is a crucial factor for the gate oxide integrity. In the gate oxide thickness range of 40 nm down to 5 nm, the negative impact of COPs on the electrical breakdown at Q_{bd} = 5 x 10^{-4} C/cm^2 strongly decreased. This can be qualitatively explained by the interplay of interfacial and bulk properties contributing to the intrinsic oxide quality.

Contamination studies showed that the gettering efficiency in the Si substrate also determines the influence of metals onto gate oxide reliability. Investigations of intentionally contaminated CZ material with thick and thin oxides enabled us to distinguish between contamination and COP-related breakdown.

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Single-Wafer Gate Dielectric Technologies for Sub-0.18 μm Applications

Reference: Miner, G., Xing, G., Yokota, Y., Jaggi, A., Sanchez, E., Chen, C., Lopes, D., **"Single-Wafer Gate Dielectric Technologies for Sub-0.18 μm Applications,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382,* D.C. Gupta and G.A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA 2000.

Abstract: The continued aggressive scaling of device dimensions presents serious challenges in transistor design and process integration. In particular for the gate dielectric, the reduction in equivalent oxide thickness challenges the limits of current process and equipment technologies. Single-wafer oxidation technologies are fundamentally different from their batch furnace counterparts and can address these challenges. The differences in single-wafer reaction chemistry are responsible for significant improvements in gate dielectric integrity. Rapid thermal processing also makes possible high levels of nitrogen incorporation, while maintaining this reliability improvement. These improvements will be increasingly important for the next several device generations.

Keywords: gate dielectrics, single-wafer, wet oxidation, nitrided oxides

Introduction

The advancement of device capability and speed requires the continued aggressive scaling of the gate dielectric. Table 1 shows the 1997 Semiconductor Industry Association (SIA) targets for gate dielectric equivalent oxide thickness equivalent oxide thickness as a function of time and device technology generation. Also shown are the advanced equivalent oxide thickness requirements driven by the most advanced device manufacturers which tend to lead the SIA roadmap by a full generation.

Table 1.- *SIA Gate Dielectric Roadmap*

Calendar	1997	1999	2001	2003	2006
Technology (μm)	0.25	0.18	0.15	0.13	0.10
Eq. Oxide Thick (nm)	4.0-5.0	3.0-4.0	2.0-3.0	2.0-3.0	1.5-2.0
Advanced Eq. Oxide Thick (nm)	3.0-4.0	2.5-3.5	2.0-3.0	1.5-2.5	< 1.5

[1]Thermal Processing Organization, Applied Materials, 2727 Augustine Drive, Santa Clara, CA 95054

This roadmap presents difficult challenges to gate dielectric performance, most significantly for reliability and tunneling leakage. Recent research has shown fundamental reliability may limit SiO_2-based dielectrics to 2.6±0.15 nm, as shown in Figure 1 [1]. This indicates a new or fundamentally more reliable dielectric will be required, otherwise the scaling targets for gate thickness and operating voltage may not be met. This projection was based on oxides grown in a conventional furnace, and was independent of oxidation ambient for O_2, N_2O and NO gases. However, we will show that growth conditions in a single wafer processing chamber differ from batch furnaces and produce consistently more reliable oxides for the same thickness. This will extend use of SiO_2 below the 26 nm limit.

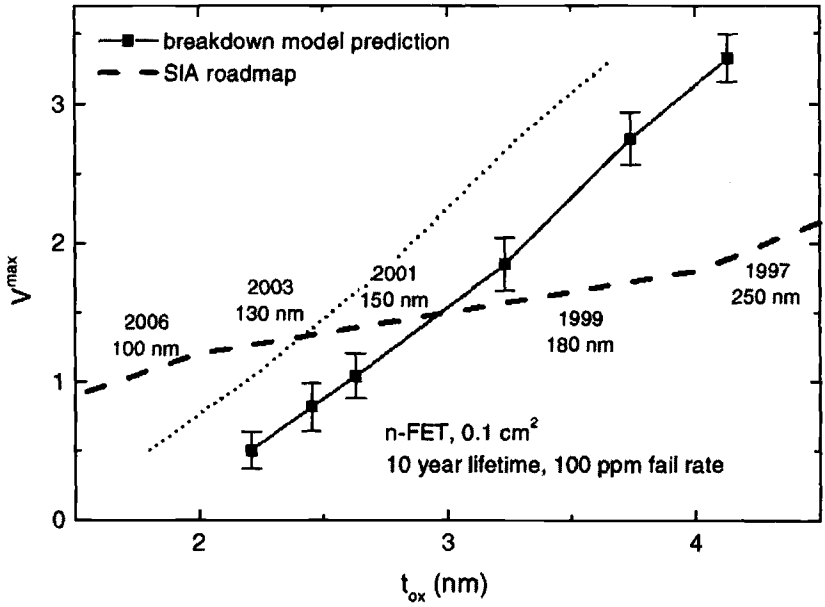

Figure 1-*Reliability Limits of SiO_2*

Leakage is also a limiting factor in gate dielectric scaling. Figure 2 shows gate leakage as a function of thickness [1]. Based on a maximum tolerable leakage current of 1 A/cm^2, the minimum thickness is 21 nm, again indicating scaling limits will be reached at the 0.13 μm technology node.

Again, single wafer oxidation can extend SiO_2. Recent work has demonstrated reduced leakage for films grown by a unique single-wafer oxidation process called *In-Situ* Steam Generation (ISSG) [2]. This novel process will be described in detail.

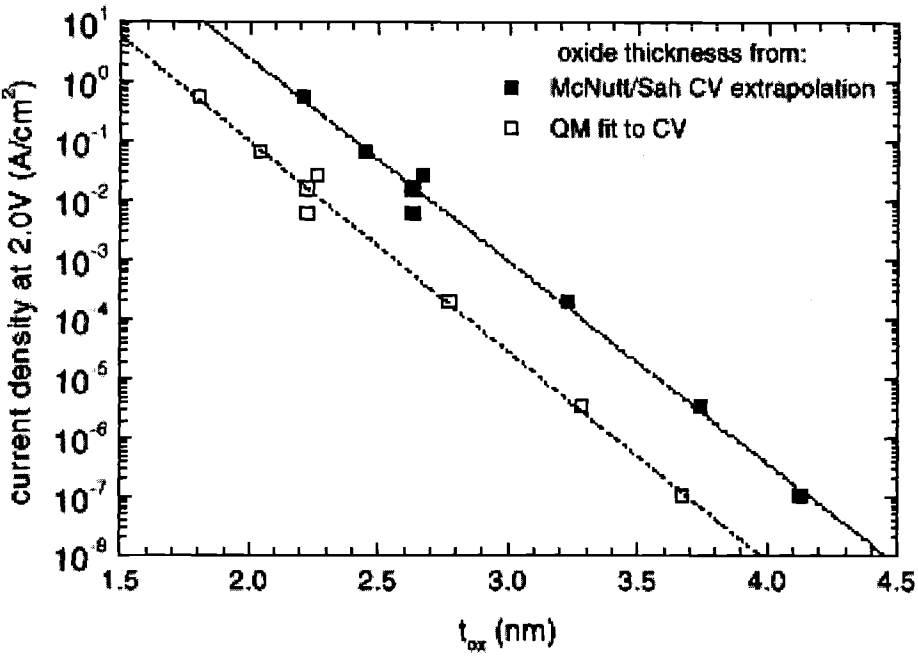

Figure 2 - *Gate Leakage versus Thickness*

Finally, single-wafer technologies offer improvements in ultra-thin film process control and flexibility for integration of multiple process steps to address more advanced dielectric solutions. This is useful in engineering nitrogen profiles in SiO_2, as well as creating stacked or graded dielectrics with higher dielectric constant materials such as silicon nitride.

This paper will focus primarily on 0.18 - 0.13 μm gate dielectric solutions in the 25-35 nm range processed in the Applied Materials RTP Centura™.

In-Situ Steam Generation (ISSG)

In-Situ Steam Generation (ISSG) is a unique process for performing steam oxidation. Typically batch furnaces use an external pyrogenic torch to produce steam. In the external torch configuration, H_2 and O_2 are combusted at atmospheric pressure in proximity to a hot element or in a hot-wall reaction chamber which ignites the reaction, producing H_2O. The resulting steam is then introduced into the hot-wall furnace tube to oxidize the wafers.

ISSG is a low pressure process whereby the H_2 and O_2 are introduced to the process chamber directly, without precombustion. Figure 3 shows a cross section of the cold-wall RTP Centura™. Process gas flows across a rotating wafer heated by tungsten-halogen lamps. The hot wafer is the ignition source and the reaction between H_2 and O_2 occurs at the wafer surface. The process is kept at low pressures, near 10 Torr, to ensure safety.

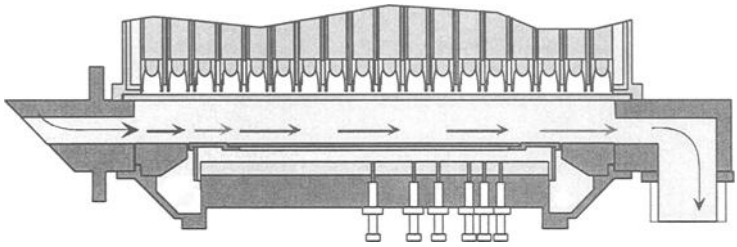

Figure 3 - *Gas Flow in RTP Centura*

The primary gas reactions in this low pressure process are [3]:

$$H_2 + O_2 \rightarrow 2OH \quad (1)$$
$$H_2 + OH \rightarrow H_2O + H \quad (2)$$
$$O_2 + H \rightarrow OH + O \quad (3)$$
$$H_2 + O \rightarrow OH + H \quad (4)$$

Using a model of the RTP Centura including temperature and gas flow dynamics, the primary species at the wafer are found to be O_2, H_2, H_2O and O. Figure 4 shows the H_2O and O components as a function of position as the gas moves across the chamber and is rapidly heated by the wafer. The reaction rates of each of these species with the silicon substrate are not known, however we would expect the atomic oxygen to be highly reactive and we believe it to be responsible for some of the unusual reaction kinetics observed.

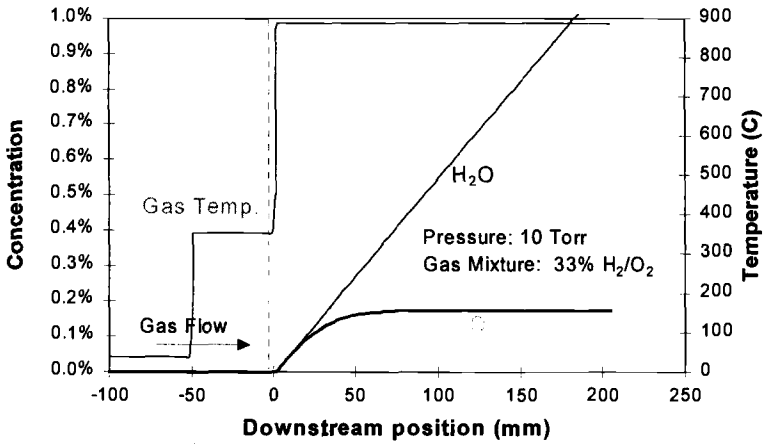

Figure 4. - *Model of H_2/O_2 Reaction Across Wafer*

Figure 5 shows the oxide thickness grown during a fixed thermal cycle of 1050 °C, 60 seconds. Oxidation rates typically show a square root dependence on pressure. This is true for pressures from atmospheric pressure down to 50 Torr (data not shown). However, near 10 Torr the growth rate suddenly rises to nearly twice the atmospheric dry growth rate. We believe that this anomalous high growth rate is caused by the atomic oxygen. At pressures above 20 Torr the mean free path is reduced, leading to more rapid recombination from O to O_2, and the high growth rate disappears.

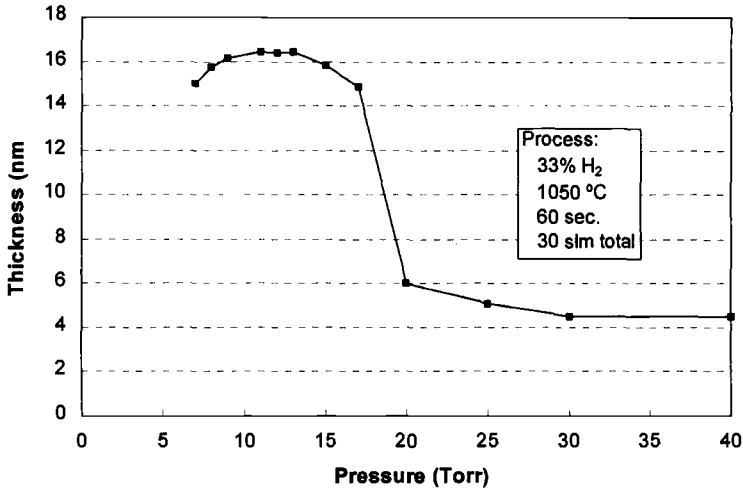

Figure 5 - *Pressure Dependence of ISSG Growth*

In addition to the differences in reaction chemistry and growth kinetics, ISSG produces fundamentally different film properties compared to conventional dry and wet oxides. When etched in a dilute HF solution, ISSG oxides have 10% lower etch rate than dry oxides grown at the same temperature.

This difference in bulk material or bonding structure also improves electrical performance. ISSG gate oxides have consistently yielded significantly enhanced reliability over batch furnace oxides. Figures 6 compares ISSG gate oxide reliability to furnace oxides, both wet and dry, from several independent experiments.

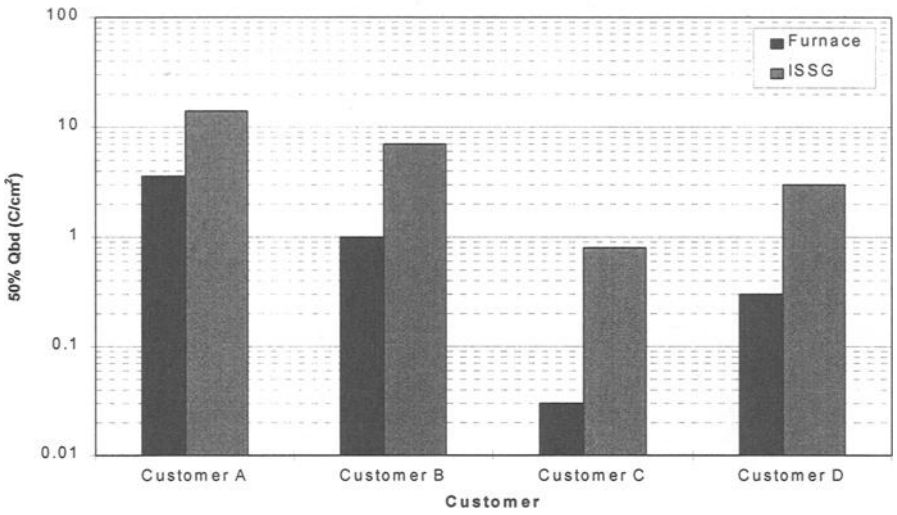

Figure 6 - *Q_{bd} Comparison Between Furnace & ISSG*

Consistent improvement in reliability of roughly an order of magnitude has been demonstrated in multiple tests comparing ISSG with furnace dry and wet oxides as well as RTP dry oxides.

N_2O Oxidation

Oxidation using N_2O has been done in both batch and single-wafer systems, and again the single-wafer process is fundamentally different.

At high temperatures, N_2O decomposes. The primary reactions are:

$$N_2O \rightarrow N_2 + O \quad (1)$$
$$N_2O + O \rightarrow 2NO \quad (2)$$
$$O + O \rightarrow O_2 \quad (3)$$
$$N_2O + O \rightarrow N_2 + O_2 \quad (4)$$

At oxidation temperatures the N_2O decomposition occurs quickly such that in a batch system by the time the gas has reached the wafers, the ambient is composed of primarily N_2, O_2, and NO.

In a single-wafer chamber, such as the RTP Centura, the decomposition occurs at or near the wafer surface, and therefore the atomic oxygen created in reaction 1 plays an important role [4-6]. The resulting differences include improved reliability, reduced surface nitrogen incorporation, and improved wafer-to-wafer repeatability.

Figure 7 shows a distinct improvement in charge-to-breakdown of oxides grown in N_2O when compared to both RTO and furnace oxides [7]. This result has been verified in several experiments.

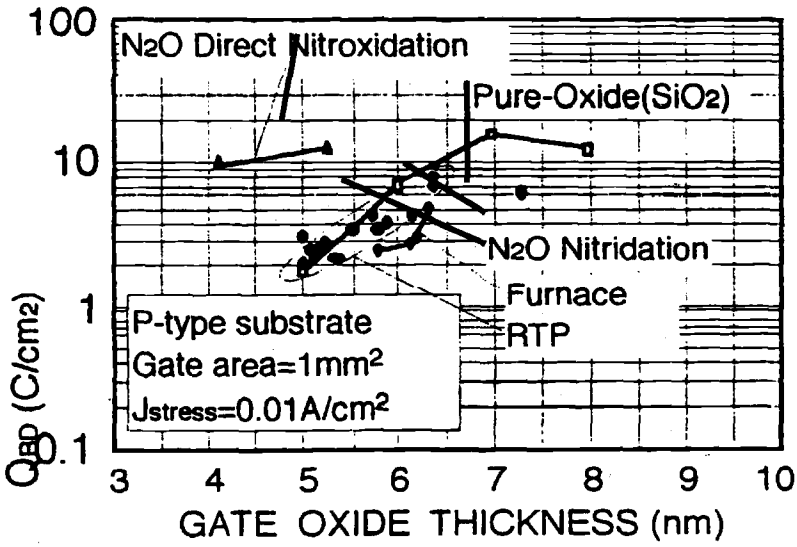

Figure 7 - *Charge-to-Breakdown of N_2O-Grown Oxide*

N_2O oxides have been shown to inhibit boron penetration from p+ polysilicon gates. In a recent demonstration N_2O was found to be a more effective barrier to boron penetration than an NO annealed oxide despite having a lower peak nitrogen concentration [7]. The nitrogen profiles in Figure 8a show a typical broad profile for the N_2O-grown sample versus the NO-annealed sample. Figure 8b shows the flatband voltage change in the capacitance-voltage curves resulting from different levels of boron penetration after a thermal anneal.

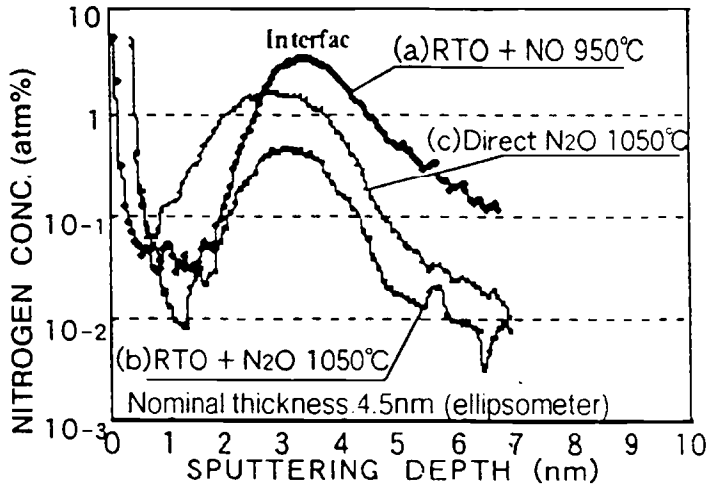

Figure 8a.- *SIMS Nitrogen Profiles*

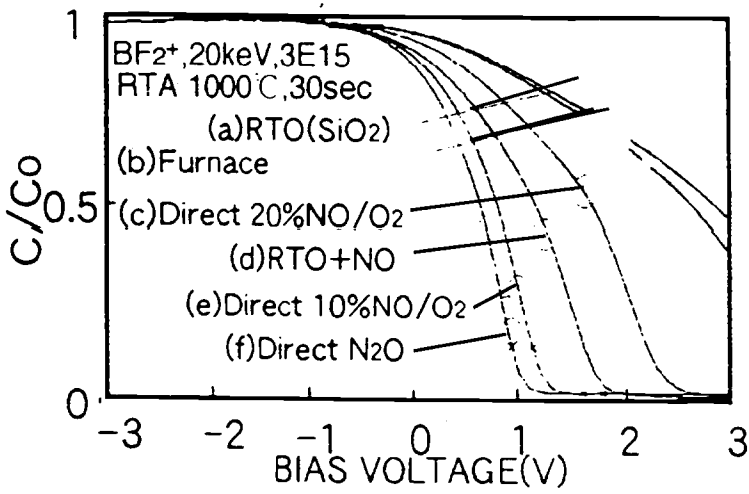

Figure 8b.- *V_{fb} Shift Caused by Boron Penetration*

Higher nitrogen concentrations with still broad profiles and high reliability can be achieved by reoxidizing NO-grown oxides using either N_2O or ISSG. Figure 9 shows two such profiles.

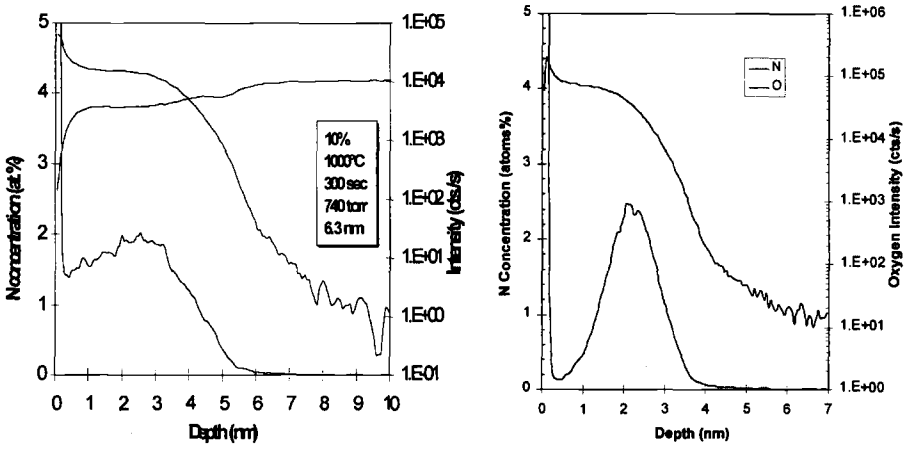

Figure 9 - *SIMS Profiles of N_2O and ISSG Reoxidized NO-Grown Oxides*

Conclusions

The unique thermal environment of a single-wafer chamber enables new process technologies for gate dielectrics. ISSG and N_2O oxidation both generate atomic oxygen during the reaction/decomposition which significantly enhances gate dielectric integrity.

These capabilities will enable the extension of SiO_2-based gate dielectrics for next generation devices as well as providing a reliable base oxide for stacks including higher dielectric constant materials.

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High Resolution Gate Oxide Integrity (GOI) Measurement in Near-Perfect Silicon

Reference: Murakami, Y., Yamazaki, T., Itou, W., and Shingyouji, T. **"High Resolution Gate Oxide Integrity (GOI) Measurement in Near-Perfect Silicon,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382*, D. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: Gate Oxide Integrity (GOI) measurements are performed for various types of silicon wafers: Pure Silicon™, Epitaxial, Hydrogen Annealed, Low COP CZ, and Conventional CZ wafers. A clear dependence of GOI parameters is observed with Time Zero Dielectric Breakdown (TZDB) and Time Dependent Dielectric Breakdown (TDDB) measurements. Using multisource measurement units can perform high resolution GOI measurements. Time Dependent Dielectric Breakdown (TDDB) measurements on 5300 MOS capacitors on a 200 mm wafer have been made successfully with this technique. High resolution GOI measurements, in particular, make clear the correlation between grown-in defects and oxide defects in CZ wafers. It is also demonstrated that this technique is highly suitable for the evaluation of various types of near-perfect silicon, which inherently has no defects.

Keywords: GOI, TZDB, TDDB, High resolution, grown-in defects, R-OSF

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Introduction

Gate oxide integrity is one of the most critical concerns for sub-micron CMOS devices, and it is most important as a quality issue of silicon wafer materials. It is now widely known that grown-in defects incorporated during CZ crystal growth affect seriously the GOI [*1-7*]. These grown-in defects are measured with various characterization techniques (SC1cleaning [*8, 9*], Secco etching [*10*], Laser Scattering Tomography [*11, 12*]), and are called by different names (Crystal Originated Particle (COP), Flow Pattern Defect (FPD), and Laser Scattering Tomography Defect (LSTD)).

As the importance of grown-in defects on GOI is widely accepted, many efforts have been given to decrease the grown-in defects by applying various techniques. It is known that epitaxial layers grown on CZ silicon have no grown-in defects [*13*], annealing of CZ wafers under non-oxidized ambient, in particular, hydrogen decrease drastically the grown-in defects at the surface layers [*14*]. And as an ultimate method to make perfect silicon, optimization of the ratio of growth-velocity (V) and temperature gradient (G): V/G is intensively investigated [*15, 16*].

In this paper, we evaluate these various near perfect silicon crystals by using GOI measurement. Both TZDB and TDDB measurement are applied. We have applied in particular high resolution TDDB measurement to see the exact correlation of the distribution of grown-in defects and GOI characteristics.

Experimental

We have measured five kinds of Silicon wafers: Pure Silicon™[*15*](Perfect Silicon), p/p+ epitaxial, Hydrogen Annealed, Low-COP CZ, Conventional CZ. The specifications of the wafers are shown in Table 1. Oxygen concentrations are specified in Old ATSM.

Figure 1 shows the CMOS simulation procedure, which depends on the kind of devices and the manufacturer. Figure 2 shows the process sequences of making MOS capacitor for GOI measurements. After CMOS simulation and removal of sacrifice oxide, gate oxide with the thickness of 9nm or 25nm were grown by pyrogenic oxidation. Figure 3 shows the mask pattern for poly-silicon electrode. We have two kinds of mask patterns: (a) Conventional, which size is 20mm^2 for TZDB and 4mm^2 for TDDB, and the coverage is 14% and 3% respectively. (b) High resolution, which

size is $4mm^2$ and the coverage are 79 %.

Multi Source Measurement Unit (SMU) is used in the measuring systems. Pascal-based programming, which have various special procedures, make it possible to measure TZDB, TDDB characteristics. Data analysis was performed using commercially available spread-sheet-based software. Figures 4 and 5 shows the measurement protocol of TZDB and TDDB measurement respectively. These are basically comparable to the E-Ramp and J-Ramp method described in [*17*] .

Step delay time of the TZDB measurement is 0.1 second, and voltage step corresponds to 0.1MV/cm increment of applied electric field. The judgement current of breakdown in the TZDB measurement is set to not too high current: $10^{-4}A/cm^2$ (20μA for $20mm^2$ gate area) to avoid the measurement error due to the fact that some capacitors have relatively high resistive paths after the breakdown. However, the defect-related breakdown field increases with the decrease of oxide thickness, the separation of intrinsic mode (C-mode) and defect-related mode (B-mode) is difficult in case of thin oxide [*18*]. We continued to increase the voltage until the current reach 1mA which is 50 times larger than the judgement current of TZDB measurement, after the current exceeded the judgement current (20μA) at 1st run TZDB measurement. MOS capacitors containing defects break by 1mA current during 1st run, these are detected as A-mode (initially short mode) at 2nd run TZDB measurement. By using the 2nd run TZDB measurement, we can detect defect-related mode even in relatively thin oxide.

Final stress of the TDDB measurement is $1A/cm^2$. In high resolution measurement, we used 4 probes and 4 SMU at the same time in this experiment. Alternatively, the combination of multi SMU (up to 200 channels) and probe card (20pins) make the throughput of the measurement at least 20 times faster than conventional measurement.

Table 1-Sample Specification

Sample Name	Sample Specification
Pure Si	Resistivity 8～12Ωcm, Oi～22ppma (Old ASTM), Particle 8/W (>0.10μm)
Epitaxial	P/P+, 11μm, Resistivity of epilayer 8～12Ωcm, Resitivity of substrate 0.01～0.02Ωcm, Particle 3/W (>0.13μm)
Hydrogen Annealed	Resistivity 9～13Ωcm, Oi～23ppma (Old ASTM), H_2 annealing, 1200℃, 1hrs, Particle 5/W (>0.13μm)
Low COP CZ	Resistivity 8～12Ωcm, Oi～18ppma (Old ASTM), Particle 35/W (>0.10μm)
Conventional CZ	Resistivity 8～12Ωcm, Oi～26ppma (Old ASTM), Particle 465/W (>0.10μm)

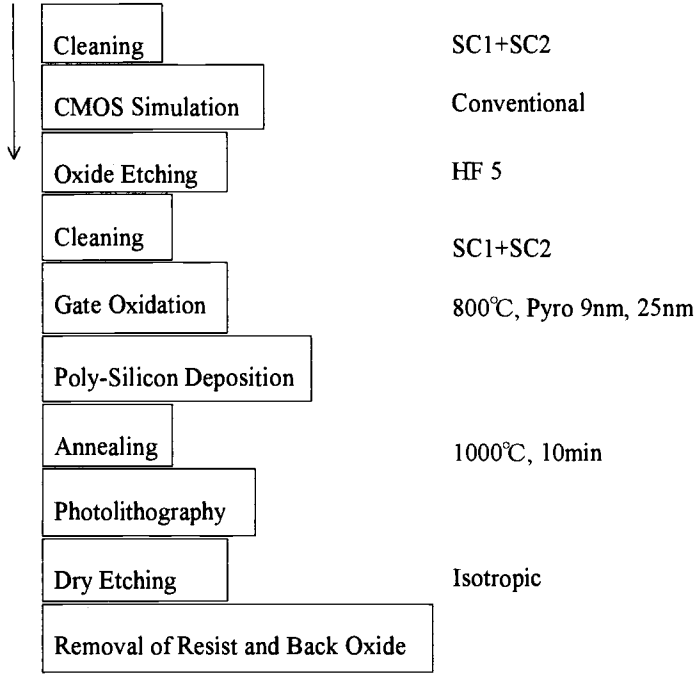

Figure 1. MOS capacitor preparation processes

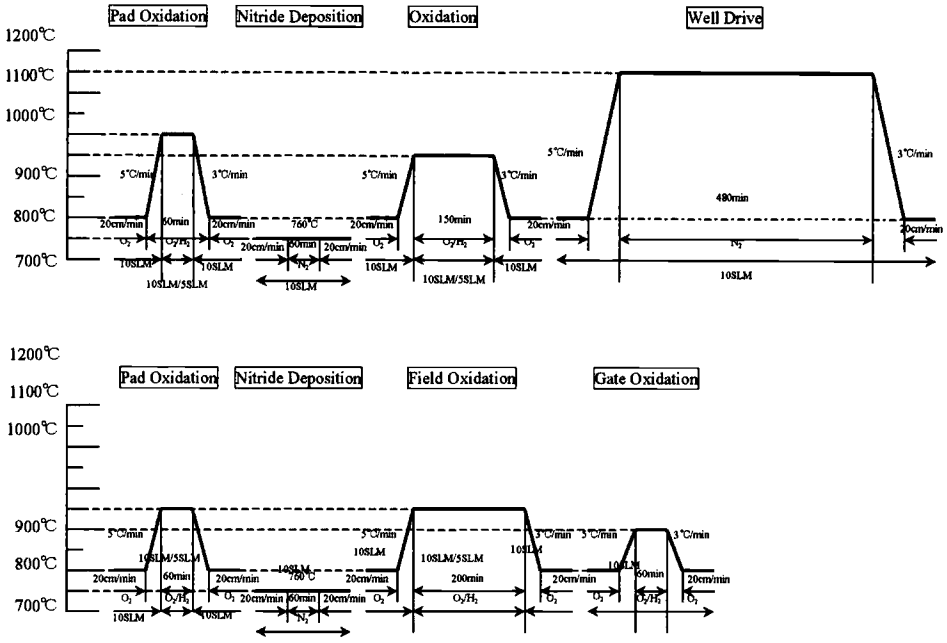

Figure 2. CMOS simulation processes

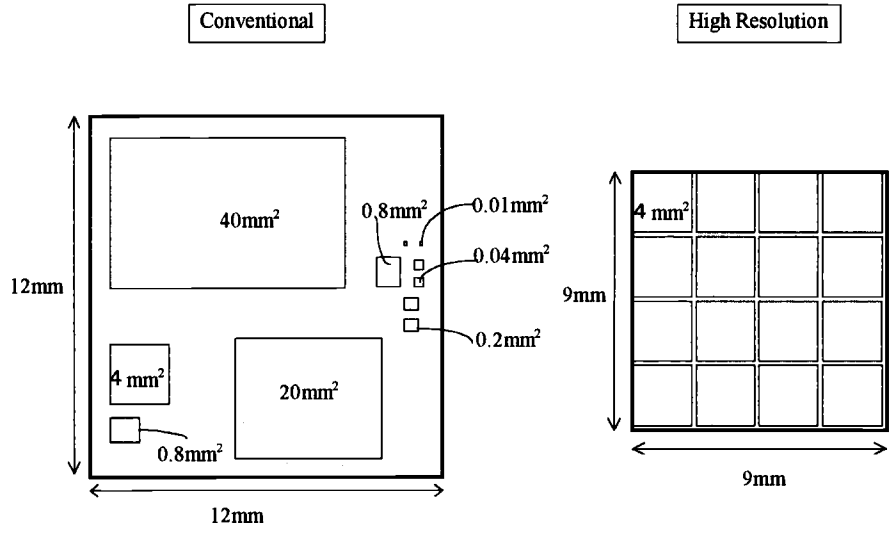

Figure 3. Poly-silicon mask patterns

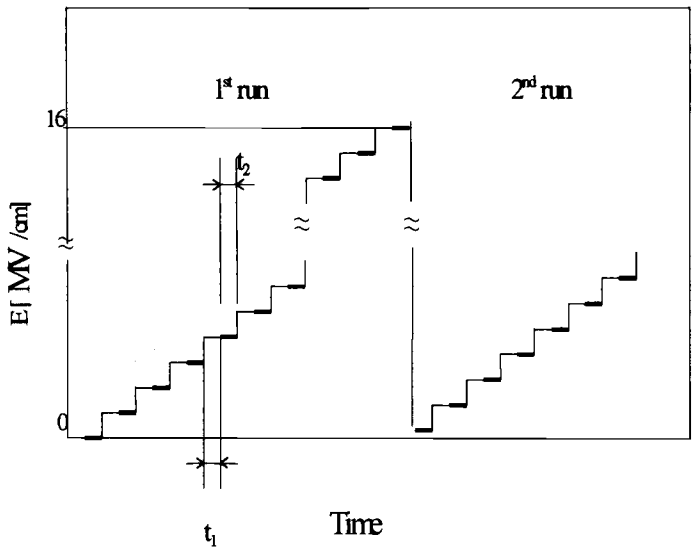

Figure 4. Measuring protocol of Time Zero Dielectric Breakdown(TZDB) measurement. Step delay time is 0.1 sec. Voltage step corresponds to 0.1MV/cm increment of E-field.

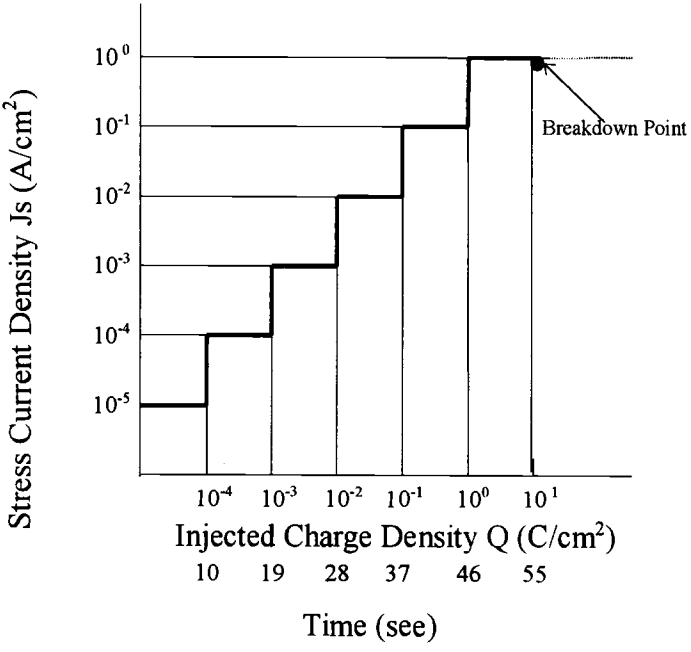

Figure 5. Measuring protocol of Time Dependent Dielectric Breakdown(TDDB) measurement

Results and Discussion

Conventional GOI Measurement

Figure 6 shows the GOI results of conventional TZDB measurement. We show here the GOI of two different oxide thicknesses (9 nm, 25 nm). Since grown-in defects are bulk-related defects, probability of containing defects in thicker oxide must be larger and the thicker oxide shows worse GOI characteristics. Pure Silicon, Epitaxial and hydrogen annealed wafers have the best GOI. Low COP wafers shows poor GOI compared to conventional CZ. In 9 nm oxide, no oxide defects are detected in all wafers, because of the reason already described. Figure 7 shows the results of TZDB 2nd-run measurement. In the hydrogen annealed wafer, oxide defects are observed. Furthermore, even in 9 nm oxide, oxide defects are observed except Pure Silicon and Epitaxial wafers.

Figure 8 shows the GOI results of the Step Current TDDB measurement. As is expected from the TZDB results, Pure and Epitaxial wafers have the best results. Defects in the hydrogen annealed wafer are observed more clearly than the TZDB measurement even in 9 nm oxide. Low COP CZ is still bad in TDDB. It is speculated that the Low COP crystals were grown under relatively fast-cooling condition compared to the condition in conventional crystals, therefore, the size of COPs in the Low COP crystals is smaller but the number of grown-in defects is larger than those in conventional crystals.

High Resolution GOI Measurement

Figure 9 shows the results of high resolution TDDB measurement. 5300 points are measured, which needs 30 times longer to measure, but in this experiment, 4 points are measured at the same time. Measuring time is around 20 hours. If we applied the probe card system, which is under preparation, measuring time become 4 hrs for one wafer.

Figure 10 shows the spatial correlation between grown-in defects which are measured with OPP (Optical Precipitates Profiler) technique and oxide defects with GOI measurement. OPP is commercially available defect analyzer which measures the phase shift of scattered light caused by the crystal defects (grown-in defects are detected here). There are two discrepancies between OPP defect density and oxide defect density. One of the discrepancy is that there is a big difference in GOI defect

density of Low COP and Conventional CZ, even though no big difference is observed in OPP defect density. Another discrepancy is the amazing features of the ring-shaped region which have relatively high density oxide defects in Low COP and Conventional CZ. In the OPP measurement, defect density is monotonous function of radius, but oxide defect distribution has a peak at the rather peripheral region. It is well known that GOI is poor inside the OSF ring, and it is also poor on the OSF ring after the heat treatment to induce OSF [*19, 20*]. Although some OSFs and precipitates were observed in the Conventional CZ wafer, no OSF and precipitates were observed in Low COP wafers. Measured defects here by OPP measurement must be not oxygen precipitates but mainly grown-in defects. We have found that even without OSF or precipitates that are optically detectable, GOI is poor on the OSF ring. Physical origin of these discrepancies are not well understood yet, but we speculate that OSF nuclei (small oxygen precipitates [*21*]) or smaller size of grown-in defects which are not detected with current OPP measurement technique must be important in GOI characteristics.

We have some oxide defects even in pure and epitaxial wafers as shown in Figure 11. We cannot exclude the effect of the preparation process of MOS capacitor at current measurement. But, this high-resolution TDDB measurement must be powerful tool to see the perfection of silicon wafers in the era of Perfect Silicon that will come soon.

Conclusions

We have developed high-resolution gate oxide integrity measurement procedures. By using this TDDB technique, we have taken the precise correlation between grown-in defects and oxide defects distribution. We find that GOI is poor not only inside the OSF ring but also on the OSF ring. We speculated that this is due to OSF-nuclei or small grown-in defects that are not detected with current measurement techniques. Furthermore, this technique is very suitable for the evaluation of various types of near-perfect silicon, which have basically no grown-in defects.

Acknowledgment

We would like to acknowledge Mr. Muroi, Mr. Koya, and Dr. Furuya for the defect observations. We would like to thank Mr. Gupta Dinesh for his suggestions

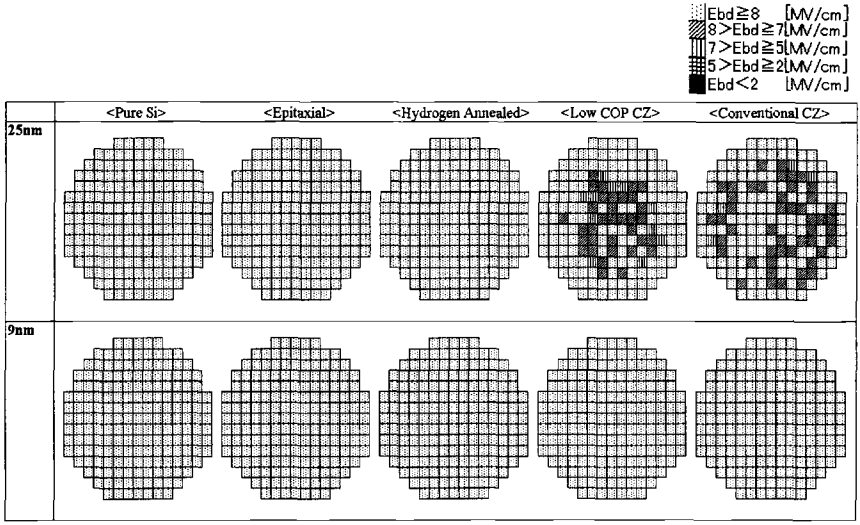

Figure 6 Results of Conventional TZDB measurement of various near perfect silicon. After CMOS Simulation, 850℃ Pyro oxidation Tox=9nm, 25nm, Poly-Si gate electrode 20mm^2, Judgement Current 1×10^{-4}A/cm^2

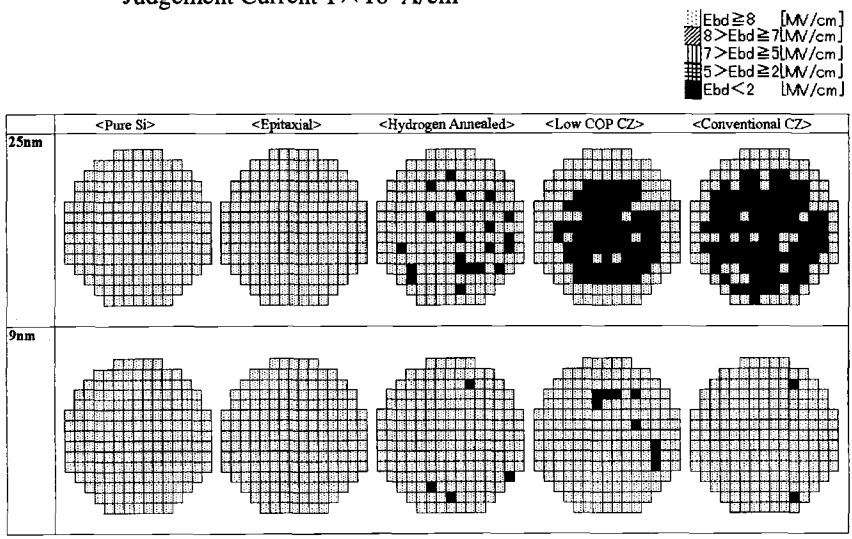

Figure 7 Results of Conventional TZDB 2nd-run measurement of various near perfect silicon. After CMOS Simulation, 850℃ Pyro oxidation Tox=9nm, 25nm, Poly-Si gate electrode 20mm^2, Judgement Current 1×10^{-4}A/cm^2

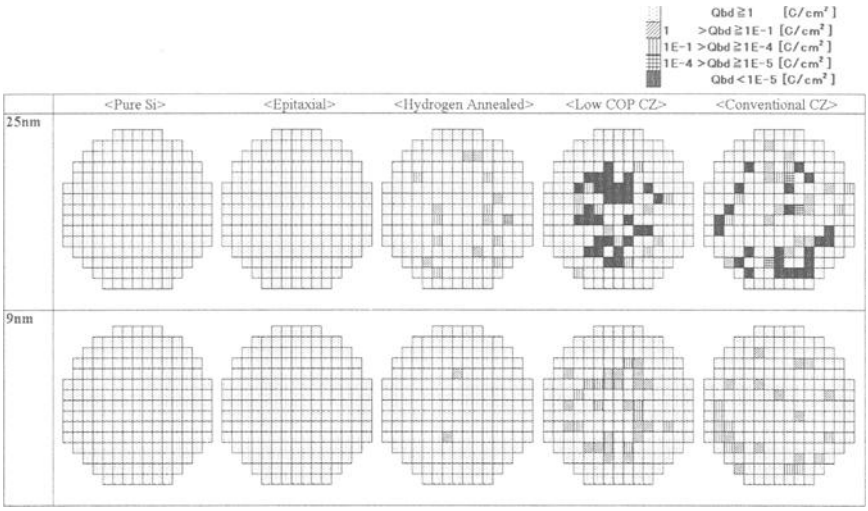

Figure 8 Results of Conventional TDDB measurement of various near perfect silicon. After CMOS Simulation, 850℃ Pyro oxidation Tox=9nm, 25nm, Poly-Si gate electrode 20mm^2, Judgement Current 1×10^{-4}A/cm^2

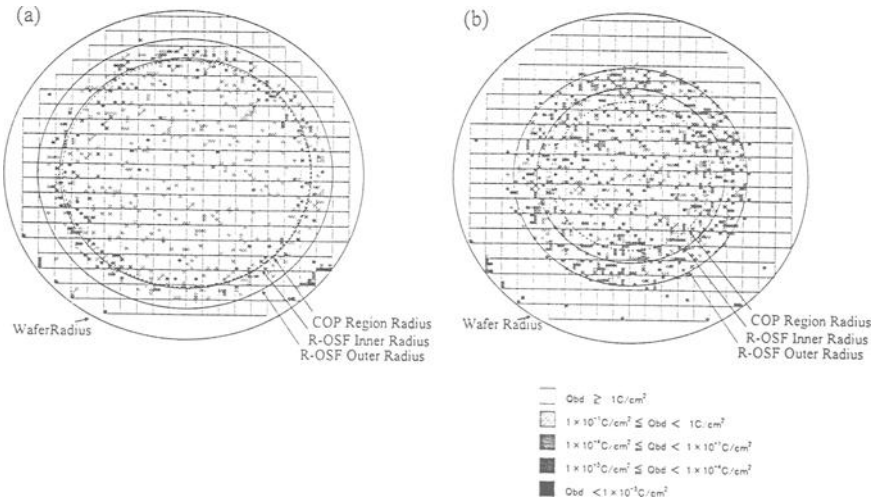

Figure 9 Results of high resolution TDDB measurement of various near perfect silicon. After CMOS Simulation, 850℃ Pyro oxidation Tox=9nm, Poly-Si gate electrode 20mm^2
(a) Conventional CZ wafer (b) Low COP CZ wafer

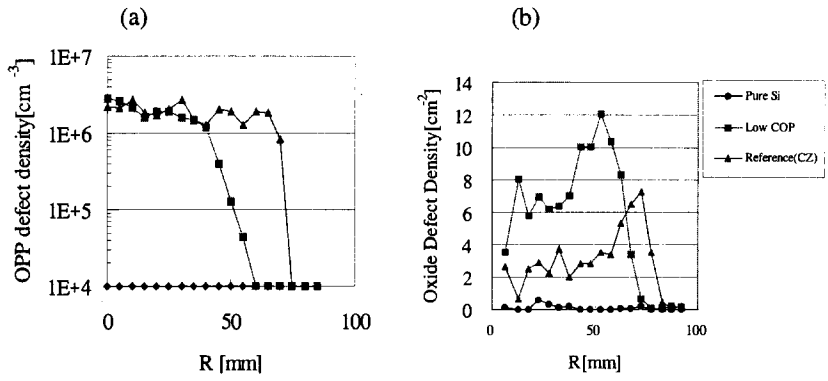

Figure 10. Correlation between GOI and grown-in defects

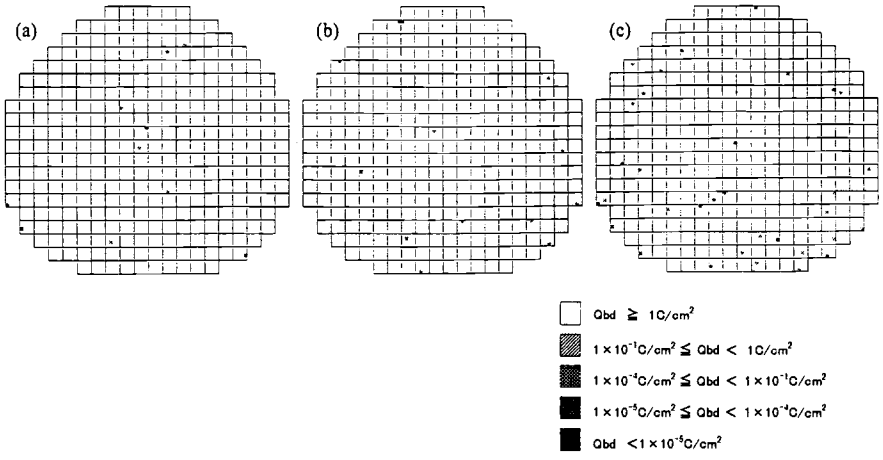

Figure 11 Results of high resolution TDDB measurement of various near perfect silicon. After CMOS Simulation, 800℃ Pyro oxidation Tox=9nm, Poly-Si gate electrode 20mm^2
(a) Pure Si (b) Epitaxial (c) Hydrogen annealed

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Qualification of Epi Layers and Interface Properties by an Improved μ-PCD Technique

Reference: Pavelka, T., **"Qualification of Epi Layers and Interface Properties by an Improved μ-PCD Technique,"** *Gate Dielectric Integrity: Material, Process, and Tool Qualification, ASTM STP 1382*, D. C. Gupta and G. A. Brown, Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

Abstract: The microwave photoconductive decay (μ-PCD) and the surface photovoltage (SPV) techniques are proved to be powerful methods in the qualification of semiconductor bulk materials. They are applied best for standard wafers with homogeneous material quality. However, both methods have their limitations when measuring epitaxial layer (epi) wafers or silicon on insulator (SOI) structures. In its conventional realization the SPV measurement is limited by the active layer thickness. On the other hand an epi layer grown on highly doped substrate typically does not generate high enough signal in a μ-PCD measurement.

The aim of the present work is the introduction of a new, improved microwave photoconductive decay technique with sensitivity exceeding that of the conventional techniques by orders of magnitude. It is shown that such a method is not only able to provide material quality in case of epi and SOI structures but can help also in the qualification of interface properties.

Data are presented to show the above statement including maps of contamination distributions in epi structures.

Keywords: silicon, epitaxial wafer, carrier lifetime, surface/interface recombination velocity

The recombination properties in silicon show a high sensitivity to the presence of contamination or structural defects. The surface photovoltage (SPV) and the microwave photoconductive decay (μ-PCD) techniques are widely used to detect contamination in the industrial practice. The major advantages of these techniques are their noncontact and nondestructive nature. Furthermore, they are also capable of performing high-speed, high-resolution mapping of whole wafers.

However, they have serious limitations when applied to layer structures like epi or SOI wafers. They are essentially unable to resolve variations as a function of spatial depth.

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This limitation is basically due to the fact that generated carriers diffuse out of the volume of interest.

Junction techniques like Deep Level Transient Spectroscopy (DLTS) [*1*] have the advantage that their investigated volume is limited to the space charge region of a Schottky diode or a pn junction. In such a case information characteristic of a thin layer can be obtained. In addition to its high sensitivity (detection limits down to $10^9/cm^3$ or even below) DLTS is also capable of the identification of the impurity in question. However, this technique has its serious limitations. Being a contact technique it requires sample preparation like evaporation of a Schottky contact. The actual measurement is performed as a function of temperature therefore the measurement cycle time extends to hours.

The room temperature photoluminescence (PL) technique recently has been introduced for the investigation of carrier lifetime in epi layers. This approach does not require contact to the wafer and is insensitive to the wafer surface [*2*]. Nevertheless, this technique does not have the capability of producing high speed, high resolution whole wafer map of contamination. Therefore theμ-PCD technique still can have its role in the qualification of epi layers.

Problems of the μ-PCD Technique Applied in Epi Qualifications

A μ-PCD measuring sequence consists of two steps: generation of carriers by a high intensity laser pulse, and then the detection of the recombination process by microwave reflection. With the application of short wavelength laser excitation (with short enough penetration depth in silicon) the carrier generation can be limited to the near-surface region, i.e., to the epi layer. For example, a 532 nm wavelength green laser pulse generates carriers in a depth extended not far beyond 1 μm. However, carriers immediately start to diffuse after generation therefore spreading out of the volume where they originally have been generated. Depending on the actual structure they even can reach the bulk material within some ns time. Even if the detecting microwave signal penetration is limited to the epi layer by the application of high frequency microwaves, carrier recombination can take place in the entire wafer thickness and the measured time constant will be determined by the whole volume regardless of which section is monitored in the measurement [*3*].

A further complication is that in p/p^+ or in n/n^+ structures the heavily doped substrate has high absorption and only a small proportion of the microwave intensity is reflected from the wafer. As a consequence, in a conventional μ-PCD apparatus a p/p^+ or n/n^+ wafer does not typically generate any detectable signal. To overcome this problem sometimes special test wafers with low-doped substrates are produced for the evaluation of the epi-growth process. Apart from the complications that instead of real product wafers, test structures with different material properties have to be used, one has to consider the problem of carriers spreading out of the epi to the bulk region. In such a case the measured 'effective' lifetime is determined by the following processes: bulk recombination, recombination in the epi layer, interface recombination between the bulk and epi layer, surface recombination on top of the epi and diffusion of carriers between

different regions. From a single measured time constant it is practically impossible to separate the contribution of the above components. Moreover the measured value typically is dominated by bulk lifetime having only minor contribution from the epi region.

In a p/p^+ or n/n^+ wafer there is a potential barrier between the epi with standard resistivity and the highly doped bulk. This barrier will prevent carrier diffusion to some extent, i.e., excess carriers are confined to the epi layer. As a consequence, bulk contribution is decreased considerably so these structures are preferable for epi characterization once the sensitivity problem is overcome.

The Role of Surface Recombination in Epi Investigations

The major goal of the μ-PCD measurement is the determination of the net bulk/epi lifetime characteristic of material quality. For that purpose bulk/epi recombination should be distinguished from surface related processes. In case of a bare silicon wafer, however, surface recombination is typically very fast and therefore dominates the measured lifetime. More specifically, there is a two-step process: carriers diffuse from the bulk/epi to the surface, then surface recombination takes place.

In case of a typical epi thickness, the characteristic time of carrier diffusion to the surface is in the range of some ns. Therefore the expression for the measured effective lifetime is simplified to the following form:

$$\frac{1}{\tau_{measured}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}}$$

where

$$\tau_{surface} = \frac{d}{2S}$$

d = layer thickness
S = surface recombination velocity
(For the case of simplicity it has been supposed that surface/interface recombination velocity on both surfaces are equal.)

We have to note here that the surface due to the small thickness of an epi layer plays a much more important role in epi lifetime measurements than in case of homogeneous bulk wafers. Surface recombination velocity actually puts a limit to the highest measurable lifetime in an epi layer. (see Figure 1).

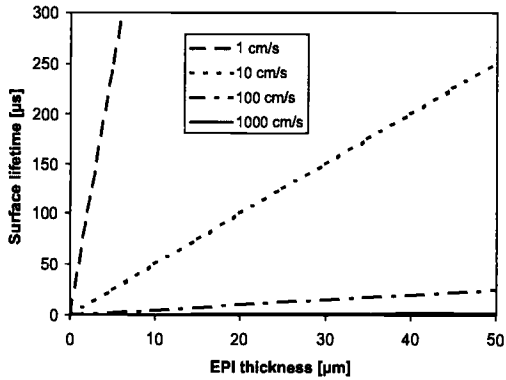

Figure 1.- The longest measurable lifetime in an epi layer in case of different surface recombination velocities

We can actually conclude that an efficient reduction or at least a proper control of surface recombination is a key for epi lifetime measurements. Even if surface recombination is not eliminated completely, it should be kept constant over the entire wafer surface with a known value. In such a case it can be accounted for finally leading to the subtraction of net epi lifetimes.

Also with a constant contribution from surface recombination wafer to wafer variation of epi lifetime could be monitored even if the measured 'effective' value is strongly influenced or limited by surface recombination. A further possibility is that a change in the epi lifetime can be investigated as a result of a given process like heat treatment or Fe-B pair dissociation due to illumination. If the surface contribution is not influenced by the treatment, then this component drops out of comparisons and the net change can be analyzed in itself. As an example, iron concentration determination easily is performed even with insufficient but constant surface passivation.

Oxide/Corona Passivation

A good quality thermal oxide is typically a satisfactory surface passivation for standard bulk wafer measurements. Oxidized wafers therefore are measured by the µ-PCD technique without any sample preparation. However, as mentioned above the investigation of epi layers put a much tighter limit to the tolerable surface recombination velocity. It was shown that the application of corona charge on thermal oxide can improve the passivation efficiency and even surface recombination velocities down or below 1 cm/s could be achieved [*4*].

While in standard bulk wafers both (front and back) surfaces should be passivated due to the fact that carriers usually reach the back surface as well by diffusion, in a p/p^+ or n/n^+ epi structure the potential barrier prevents carriers from reaching the backside of the

sample. As a consequence, a top surface passivation is sufficient for the investigation of these structures. The effect of the deposited charge on the measured effective lifetime in case of p/p^+ and n/n^+ oxidized wafers is shown in Figures 2.a. and 2.b.

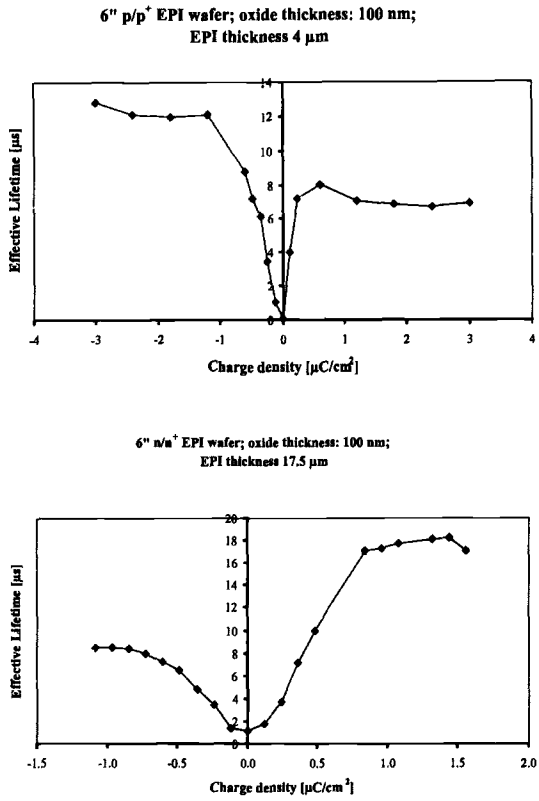

Figure 2.a. and 2.b. – Effective lifetime in oxidized epi wafers as a function of charge deposited on the oxide. Highest passivation efficiency is reached by accumulation is both cases: negative charge on p and positive charge on n material.

It is seen that the best passivation (i.e., longest effective lifetime) is achieved when the semiconductor surface is driven to accumulation. This probably is due to the fact that in accumulation minority carriers are repulsed from the surface preventing them from recombining there. Finally, passivation efficiency, of course, depends on the oxide-silicon interface. Even in complete accumulation there is still some surface recombination taking place.

It should be emphasized that even an incomplete but homogeneous interface/surface recombination velocity makes possible wafer to wafer or region to region comparisons.

Chemical Surface Passivation on Bare Wafers

There are cases when measurements are required on non-oxidized wafers, especially when the effect of high temperature thermal oxidation should be eliminated. For the above purpose an alternate form of lattice termination, namely the chemical passivation of the surface has been introduced. With the introduction of iodine containing solution surface recombination velocities comparable to a good quality thermal oxide could be reached [*5, 6*].

Improved μ-PCD Technique

A standard μ-PCD apparatus with a 905 nm infrared and a 532 nm green laser excitation source and a 10 GHz reflectometer was used for the investigation of epi characteristics. The antenna design was modified to confine microwave into the volume of interest. The details of the actual arrangement are to be published elsewhere. The result of the above improvement is a signal level typically 2-3 orders of magnitude higher than that from a conventional equipment. As a consequence, practically all p/p^+ and n/n^+ epi structures with standard epi thickness and resistivity on substrate with any doping can be investigated. High resolution (0.5 mm) lifetime maps of whole epi wafers are recorded with a speed of 30 ms/point. Such a measurement of a p/p^+ as-received oxidized epi wafer is shown in Figure 3.a.

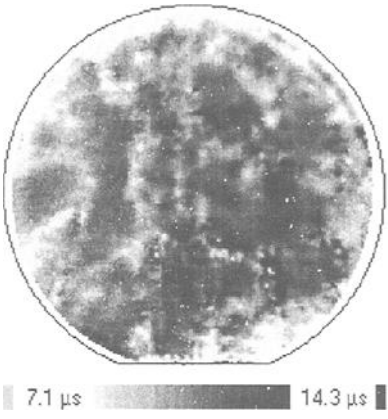

Figure 3.a. - Lifetime map of an p/p^+ as-received epi wafer (epi thickness 6.3 μm, epi resistivity 13 Ωcm, substrate resistivity 0.15 Ωcm)

Figure 3.b. - Lifetime map of the wafer from Fig. 3.a. after the deposition of 500 μC/cm² negative charge.

In case of a typical thermal-oxide, the interface state density and oxide charge shows an inhomogeneous distribution which is reflected in the actual measurement. After the deposition of negative charge on the entire wafer surface (about 500 $\mu C/cm^2$) the semiconductor surface is pushed to accumulation, surface recombination velocity is reduced and charge density is homogenized. As a consequence, the measured lifetime is increased and by the elimination of interface recombination velocity variations a structure from the material is made visible on the recorded map (Figure 3.b.). A ring-like pattern is clearly resolved by the measurement even if the relative lifetime variations between neighboring rings are in the range of some percent.

The above pattern probably is originated from crystal growth and appears in the map probably due to a minor influence from the bulk material. It will be shown later that the measured value has a stronger contribution from the epi layer. A similar map recorded on an n/n^+ structure can be seen in Figure 4. Not like the above p/p^+ wafer which had a homogeneous epi quality the present map shows a large variation in the epi characteristics having a low lifetime feature originated from the epi process close to the flat region. (In this case for maximum surface passivation a positive corona charge was applied to reach accumulation.)

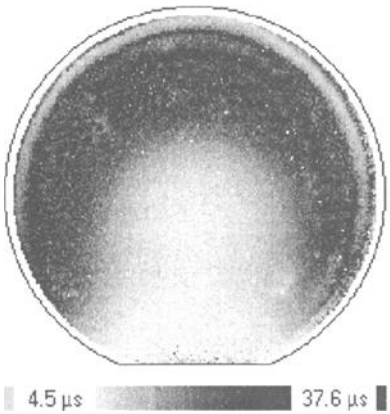

Figure 4. - Lifetime map of an n/n+ epi wafer (epi thickness 17.5 µm, epi resistivity 0.59Ωcm, substrate resistivity 0.015 Ωcm) after the deposition of 500 $\mu C/cm^2$ positive charge.

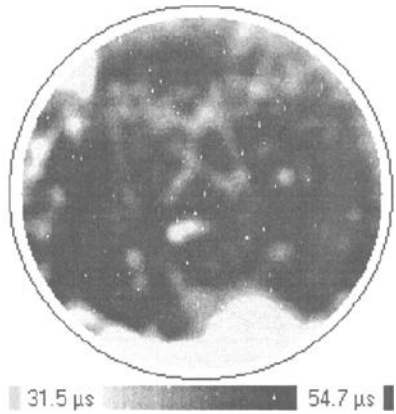

Figure 5. - Lifetime map of a p/p+ epi wafer with chemical surface passivation with an epi thickness of 8µm.

To eliminate the contribution from high temperature oxidation processes on epi quality bare wafers are measured with chemical surface passivation. (A solution containing iodine is spread over the surface.) Proper application of this technique may lead to a recombination velocity comparable to that of a charged thermal oxide. High resolution map of a p/p^+ epi wafer with iodine passivation is seen in Figure 5. It is important to note that in an 8 µm epi layer effective lifetime exceeding 50 µs could be reached. With the

application of a simultaneous bias light the passivation efficiency even can be improved further, this way giving a possibility of measuring net epi lifetimes without the need of further calculation [7].

Contamination Concentration Determination in Epi Layers

Iron is a well-known contaminant in silicon wafers. In p/p^+ type silicon iron is present in the form of Fe-B pairs. It is common knowledge that Fe-B pairs can be dissociated by annealing or illumination and such treatments result in iron interstitials separated from B dopants [*8*].

In the present study a high intensity halogen lamp was used for Fe-B separation. Such treatment was applied to an iron contaminated sample for the demonstration of the practicality of this technique.

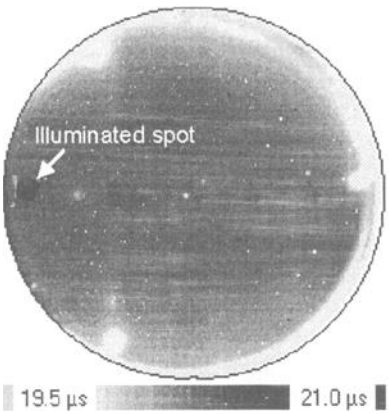

Figure 6. - Fe-B pair dissociation due to a halogen lamp spot illumination in a bare silicon wafer.

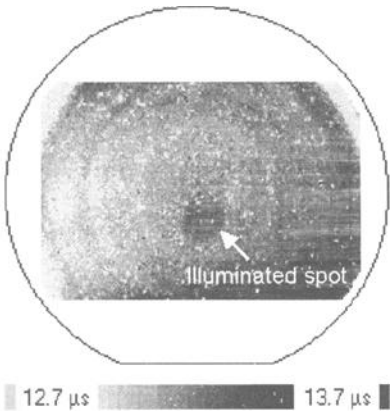

Figure 7. - Fe-B pair dissociation due to a halogen lamp spot illumination in the p/p+ epi wafer from Figure 3.a. and 3.b

Figure 6 shows a high resolution lifetime of a standard bulk wafer without any surface passivation. Even if the measured value is essentially surface recombination limited effective lifetime, the illuminated spot with its increased value is distinguished on the map. Supposing that the surface contribution is not modified by the illumination, it actually drops out of the comparison of the measured value before and after treatment finally making possible the determination of iron concentration in the given material. In the present wafer iron concentration of $2.2 \times 10^{10}/cm^3$ was determined with the help of the following expression:

$$N_{Fe} = C \cdot \left(\frac{1}{\tau^{before}_{measured}} - \frac{1}{\tau^{after}_{measured}} \right)$$

where

N_{Fe} = iron concentration
C = constant
$\tau_{before\ measured}$ = lifetime measured before illumination
$\tau_{after\ measured}$ = lifetime measured after illumination

The same experiment was performed on the p/p^+ epi wafer already shown in Figures 3.a. and 3.b.

In the present case only a square-shaped window around the illuminated spot has been scanned. As in the bulk wafer case an increased lifetime spot due to illumination is seen clearly on the map. This is a clear indication that this wafer has iron contamination. One still has to prove that iron contamination was not detected in the highly doped bulk but in the 13 Ωcm epi layer. For this purpose further measurements should be performed. In this case not only the Fe-B dissociation process but also the subsequent association of Fe-B pairs were followed at room temperature (see Figure 8). It has been proven by Zoth and Bergholz [8] that the Fe-B association time constant basically is determined by the B concentration, i.e., by the doping of the material in question. According to their data in a material with 0.015 cm resistivity the association should take place in much less than an hour, while in a layer with 13 Ωcm resistivity the association time should extend to about 13 hours. In fact the measured characteristic time for the association is in agreement with the expectations for the epi layer with 13 Ωcm resistivity. Therefore it is concluded that both the iron association and the dissociation process took place in the epi layer and such an experiment is a straightforward way of detecting iron in epi structures.

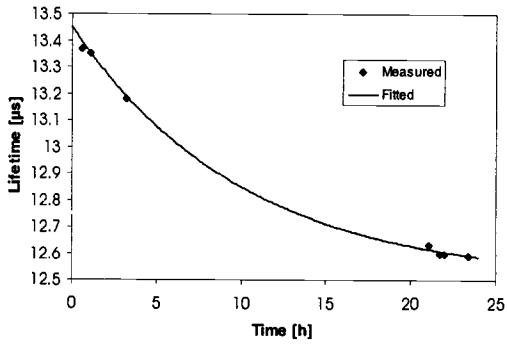

Figure 8. - Fe-B pairing (association) in the epi layer of a p/p^+ wafer from Figure 3.a. and 3.b.

Conclusion

It was shown that a modified μ-PCD technique with improved sensitivity is capable of measuring p/p^+ and n/n^+ epi structures. If the epi surface is passivated properly, the measured lifetime variation is characteristic of the epi quality. It was also demonstrated that iron contamination is easily detected in p epi layers with the above approach.

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Standardization and Round Robins

Appendix 1

Interim Reports of Two Inter-Laboratory Round Robins on Gate Oxide Integrity, One Conducted by ASTM Committee F-1 and JEDEC Committee, And the Other Conducted by JEIDA Committee and SEMI, Japan

The two round robins, one conducted by ASTM Committee F-1 and IEEE-JEDEC Committee, and the other conducted by JEIDA Committee and SEMI in Japan are entirely different in their scopes. The ASTM/JEDEC round is being conducted in the USA to test gate oxide integrity with three test procedures, namely the voltage ramp, the current ramp and the bounded current ramp methods. The voltage ramp method is considered useful in determining changes in a given device process, and is supported by the ASTM Standard Test Method F1771-97[1]. The current ramp and bonded current ramp tests are supported by test methods published by JEDEC Committee[2]. John Suehle of NIST discusses the details of this round robin below.

The charge-to breakdown evaluation of a silicon wafer is widely used in determining the wafer quality for device yields and reliability. The purpose of the second round robin conducted by JEIDA Committee and SEMI Japan is to establish 1) the correlation between sample preparation conditions, measurement conditions, and 2) to compare the results of the oxide breakdown measurements performed on the multi-laboratory basis. Upon obtaining suitable conditions, it is anticipated that a method of measurement of silicon wafer quality in terms of oxide breakdown will emerge. This method will be useful by both the silicon producers as well as users who fabricate devices on the silicon wafers. Kikuo Yamabe of the University of Tsukuba discusses this round robin and provides initial results.

Both round robins are expected to be completed in the year 2000.

..... Dinesh C. Gupta, Co-Editor

Round Robin on GOI Test Methods Conducted by ASTM/JEDEC: Interim Report[3]

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The purpose of the inter-laboratory round robin is to evaluate the joint ASTM/JEDEC voltage ramp test procedure for ultra-thin oxides having a thickness down to 3 nm. The round–robin will also evaluate modifications made to the breakdown criteria used in the JEDEC current ramp and the bounded current ramp test. The failure (breakdown)

[1] ASTM Book of Standards, Volume 10.05. The test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F1.06 Section F on Metrology for Process Control, George Brown, Chairman.

[2] EIA/JEDEC Standard 35-1.

[3] Round Robin conducted by John Suehle of NIST and George Brown of SEMATECH (Texas Instruments Assignee).

criterion for the voltage ramp test was changed from an increase of 10 times in the measured current to a factor of 3 in the current-voltage slope change. The failure criterion for the current ramp was changed from a 15% drop in the measured voltage to a 5% drop in the measured voltage. The results from the round robin will be used to assess the robustness of the three breakdown tests when performed on different sets of equipment and to determine if any of the test parameters need to be modified

Texas Instruments, Inc supplied twenty wafers. The wafers were processed such that there were four sets of wafers having SiO_2 grown to a thickness of 20, 10, 5, and 3 nm. Sixteen wafers were patterned with round capacitor test structures with 4 different areas and four wafers were not patterned for Hg probing. Each participating laboratory is instructed to perform 3 tests: ASTM/JEDEC Voltage Ramp test, JEDEC Current Ramp test, and the JEDEC Bounded Current Ramp test.

Eleven laboratories have agreed to participate in the round-robin experiment. NIST serves as the reference laboratory. Three laboratories have completed the tests and three are currently conducting the experiment. Initial results indicate that the tests are robust and yield quantitatively similar reliability parameters even when performed on different test equipment. The round robin is expected to be completed in the year 2000.

Standardization of Silicon Wafer Evaluation by Oxide Breakdown---Results of first Round Robin conducted in Japan

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Higher operation speed and better reliability is required in modern silicon ULSI's and better yields and high reliability are necessary in order to ensure high device performance. It is known that the silicon substrate quality as measured by the defect density strongly influences the quality of silicon dioxide film. Further, it is known that 1) surface metallic contamination and 2) oxygen precipitates and voids influence the breakdown defect densities of thermally grown SiO_2 films deposited on silicon wafers. The voids are aggregates of the atomic vacancies in the silicon substrate[4-6]. The hydrogen-annealed silicon wafers or epitaxial silicon wafers generally have lower densities of oxygen precipitates and voids near the surface and, thus provide low oxide breakdown defect density. Both of these materials are, however, costlier than the CZ wafers. The evaluation of the silicon wafers by dielectric breakdown of thermally grown silicon oxide on silicon substrates is very sensitive and practical, but the results are affected by the sample preparation and measurement conditions. In the first round robin, the conditions of sample preparation and measurements employed by participants was checked.

[4] Yamabe, K., Taniguchi, K. and Matsushita, Y., Thickness dependence of dielectric breakdown failure of thermal SiO_2 films", *Proc. IRPS '83, IEEE*, 1983, pp. 148-190.

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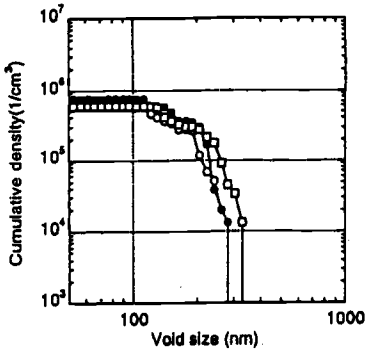

Fig.1. Grown-in defect density distribution by OPP.

The participants of the first round robin are 7 companies, MEMC Japan Ltd., Komatsu Electronic Metals Co. Ltd., Shin-Etsu Handotai Co. Ltd., Nippon Steel Corp., Toshiba Ceramics Co. Ltd., Wacker Chemicals East Asia Ltd., and Mitsubishi Material Silicon Co.

Samples were cut from one phosphorus-doped Czochralski-grown P-type (100)-oriented silicon crystal ingot with a resistivity 9-11 Ω. Cm and were identically processed. The interstitial oxygen concentration was $8\text{-}9\times10^{17}cm^{-3}$ (JEIDA standard). Three wafers were selected from the lot and the grown-in defect density distributions were determined by Optical Precipitate Profiler (OPP) measurements. It was confirmed that the total defect density was $6\text{-}8\times10^{5}$ cm^{-3} in all wafers chosen (Fig. 1).

Fabrication of MOS capacitors:
Two wafers were provided to each participant who fabricated MOS capacitors using the following method. Each company cleaned the wafers by their own cleaning method, deposited silicon oxide of 10 and 25 nm at 900°C in an atmosphere of pure dry oxygen, and deposited phosphorus-doped polysilicon films of 200-400 nm thickness and with a sheet resistance of less than 50 Ω/□ by LPCVD method. Lithography and either a chemical dry etching or wet etching technique and the company's own photomask was used to form the electrode pattern. The sizes of the capacitors' gate areas were 1 and 10 mm^2. Back surface contact was not employed.

Evaluation of dielectric breakdown[4, 5]
TZDB (Time zero dielectric breakdown) measurement condition: The gate field of the MOS capacitor was allowed to increase in steps of 0.25 MV/cm until the leakage current of the gate oxide exceeded the pre-determined dielectric breakdown current of 1 μA. The gate field at this time was made to be the dielectric breakdown electric field. The gate field was applied in the direction of the gate electron injection. No compensation was made for the flat band voltage Approximately 100 capacitors were measured for each condition, and histograms were drawn for three breakdown modes as follows:
A-mode - $E_{BD} \leqq$ 1MV/cm, B-mode - 1 MV/cm $< E_{BD} \leqq$ 8MV/cm, and C-mode - E_{BD} >8 MV/cm.

Results and discussion

Fig. 2 shows typical breakdown mode ratios and their average value. Each ratio was calculated for MOS capacitors fabricated by company B and measured by 7 participants. The gate oxide thickness was 25 nm and capacitor area was 10mm^2. Wafer #F1 measured by company F had lower B mode failure fraction by about 15 % in comparison to the

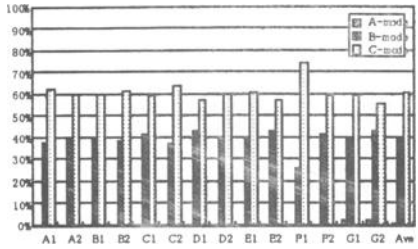

Fig.2. Oxide breakdown mode ratios measured by 7 companies.
Company B fabricated the MOS capacitors.

measurements made by other companies. This result could be explained, because the company F made an error in the measurement. Accordingly, the data of #F1 was excluded from the average calculation. Assuming that the oxide breakdown defects have the Poisson distribution, the oxide defect density, α_{ox}, may be calculated from the failure fractions in Fig.2, using equation 1.

$$\alpha_{ox} = - \ln (1-F)/S \qquad (1)$$

Where, S is the capacitor gate area, and F is the failure fraction for each oxide breakdown mode.

In Fig.3, the average defect densities for the MOS capacitors fabricated by 7 participants are shown. The defect density are low for companies B and D, high for companies E, F and G and in between these for companies A and B. The average density of the B mode defect is 5.8cm^{-2} with a dispersion of $\pm$ 1 cm^{-2}. The average A mode defect density is lower than 0.1cm^{-2}. The average oxide thickness is about 24.9nm. Assuming that the silicon thickness converted to the silicon dioxide is 0.44 times the oxide thickness, the converted silicon thickness is 11.0 nm. Considering the low A mode defect density, it is reasonable to presume that the B mode oxide defect can be mainly due to defects in silicon substrate. Therefore we can estimate that the defect density in the silicon substrate

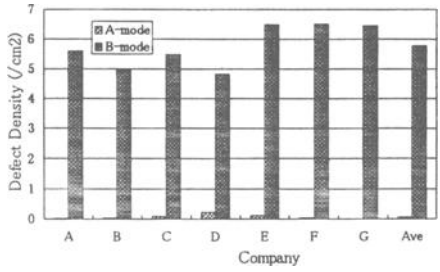

Fig. 3. Oxide breakdown mode ratios measured by 7 participants. MOS capacitors were fabricated by company B.

is $(5.3 \pm 0.9)\times10^{6}cm^{-3}$. As shown in Fig.1, the dispersion of the COP (Crystal Originated Pits) density of the silicon crystal ingot is $6\text{-}8\times10^{5}cm^{-3}$, which is about tenth of the electrically measured defect density described above. This difference may be explained as follows: First, the minute defects, which cannot be measured by the OPP technique, may become origins of the B-mode oxide defects. Secondly, there may be some defect origins during wafer process such as surface contamination after cleaning treatment and diffusion of phosphorus atoms near the polysilicon gate electrode at the oxide interface. However, considering that the dispersion of the B mode defect densities among the 7 fabricating companies is at most $\pm$ $1cm^{-2}$, the second reason can be omitted. The lower detection limit for defect diameter by OPP measurement is about 100nm. In Fig.1, the increasing trend with decreasing defect diameter is not perfectly saturated at 100nm. Defects of diameter less than 100nm, of course, exist in silicon. And it is hard to consider that the dielectric breakdown of 25nm oxide is not sensitive to defects in silicon with diameters of the order of ten nanometers. This explanation allows one to believe that the sensitivity of defect measurement by OPP method is lower than the defect evaluation by dielectric breakdown of the thermally grown silicon dioxide on silicon substrate. For the gate area of 1 mm^2, the measured capacitor number of 100 is too small to estimate the exact defect density.

Fig.4 shows defect densities of the 10nm oxides. Compared to defect densities in 25nm oxides, the defect densities of 10nm oxides are remarkably lower except for the company, D. Due to their fabrication process, companies D and F had higher defect densities.

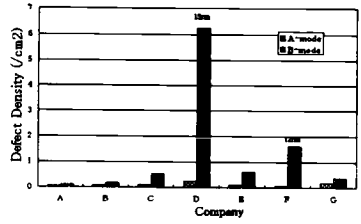

Fig. 4. A- and B-mode oxide defect densities for MOS capacitors fabricated by each participant. Oxide thickness is 10 nm.

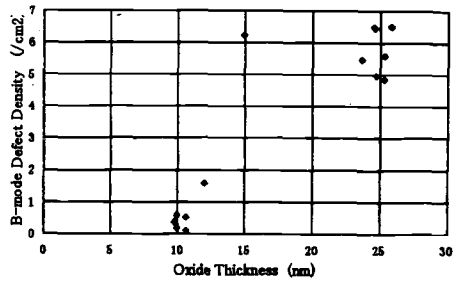

Fig. 5. B-mode oxide defect densities as a function of oxide thickness.

In Fig.5, the oxide defect density is plotted as a function of silicon oxide thickness. The defects are distributed uniformly with a density, ρ_{si}, in the vicinity of the silicon surface and become dielectric breakdown defects upon incorporation in the oxide by thermal oxidation. Assuming that all B mode defects come from defects in silicon substrate, α_{ox} of the B mode is given by

$$\alpha_{ox} = \rho_{si}\, T_{ox}/0.44 \qquad (2)$$

The B mode defect density should be in proportion to the oxide thickness, T_{ox}. However, in Fig.5, the oxide defect density steeply increases when oxide is thicker than 10nm, as explained by inverse relationship of oxide breakdown field and oxide thickness. Since the B mode failure fraction is too low, the same measurement for dielectric breakdown of the two oxides, 10nm and 20nm, is not suitable for the evaluation of defects in silicon wafers. In case of 10nm oxide, another evaluation method such as a time dependent dielectric breakdown (TDDB) is proposed.

Oxide thickness

The error in the value of oxide thickness affects the oxide breakdown mode ratio. The influence is especially large for oxides thinner than 20nm.

The leakage current of silicon oxide film depends upon the electric field across the oxide and, is controlled by the. Fowler-Nordheim (FN) tunneling mechanism. The leakage current in different oxide thickness will be equal if the series resistances in the oxides, coming from the silicon substrate, polysilicon electrode and wiring etc., are equal. Therefore, if the same measuring system is used, a variation in oxide thickness may be calculated from the gate voltage distribution that gives equal leakage currents for the capacitors with equal gate areas. From the current-voltage characteristics, gate voltages were obtained for a leakage current of 1×10^{-6} A/mm^2. Oxide thickness was measured on the test wafer by ellipsometric measurement. Figures 6(a) and 6(b) show the correlation between gate voltage and the oxide thickness for 25nm and 10nm oxides. In fig. 6(a), all data points are within a region enclosed between +10% and -10% lines, while in fig. 6(b), only one data point is below the -10% line. This indicates that the leakage current of the

oxide deposited by this company is higher than that of the leakage currents of oxides from other companies. A round robin for the oxide thickness measurement is planned among the seven companies.

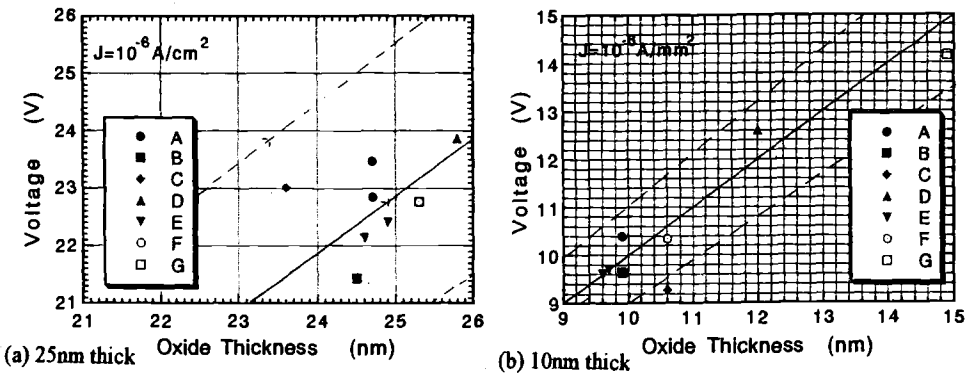

Fig. 6. Critical gate voltage vs. oxide thickness measured by ellisiometry. The critical gate voltage is a voltage at which the gate oxide leakage current reaches 10-6 A/cm2 of MOS capacitors with oxides of (a) 25 nm thick and (b) 10 nm thick

Conclusion

This round robin consisted of sample preparation and measurement of oxide breakdown by seven companies in the process of evaluating silicon substrate quality by gate oxide integrity. It is anticipated that following a second round robin, the standard test method for GOI measurement can be recommended in the year 2000

Panel Discussion

Appendix 2

Panel Discussions – A Synopsis

Dinesh Gupta and Howard Huff wrote the material presented in this appendix. It is based on their material and feedback from Dave Dumin, Gennadi Bersuker, Yoshio Murakami, and John Suehle. This material, however, did not go through the review process and is presented for information only.

The Panel members included G.Bersuker, SEMATECH; M.Dexter, Texas Instruments; D.J.Dumin, Clemson University; E.D.Grann, Wacker Siltronic; G.Gruber, Solid State Measurements; G.Miner, Applied Materials; Y.Murakami, Mitsubishi Materials Silicon Corporation; T.Pavelka, Semilab Rt; M.Seacrist, MEMC Electronic Materials; A. Strong, IBM; J.S.Suehle, NIST; and M.Wilson, Semiconductor Diagnostics.

Gate dielectric integrity (GDI) was described to be one of the most critical parameter of CMOS devices. Certain grown-in defects incorporated during crystal growth impact the integrity of the gate dielectric films. Thus, GDI has frequently been used to classify the quality of silicon wafers. These measurements have led silicon suppliers to develop crystal growing processes, which suppress the formation of point defect agglomerates, thus reducing or eliminating vacancy-related defects. GDI performance in wafers using these technologies can approach epitaxial wafer equivalence. It is, however, not well understood how much other wafer properties such as microroughness, surface contamination etc. will influence thin dielectric GDI. Continued scaling of gate dielectric thickness for smaller technology nodes raises reliability concerns for ultra-thin dielectrics because excessive leakage current and soft breakdown present new challenges.

Many methods are used to introduce the stress during measurement. These methods include constant voltage, constant current, and VRAMP or JRAMP (step or bounded). The ramped current and constant current measurements of Q_{bd} can only be correlated if test conditions are properly taken into account.

The results for thicker oxides (>10 nm) measured under constant voltage and. constant current stress are closely related. For thinner oxides ($\leq$ 3 nm, for example, where direct tunneling becomes more important) however, Q_{bd} measured by a constant current stress (CCS) is very sensitive to the stress conditions, and tends to lose its significance as a metric.

Published literature has shown that even for thicker oxides, Q_{bd} cannot be directly correlated with dielectric lifetime determined by device testing, but can be useful as a rapid process control method for determining dielectric defect density. Data is available

in the literature, however, which shows that if extrinsic defect density is the desired parameter, ramp test duration could be decreased from 25 sec down to one sec with no loss of resolution. Q_{bd} is not a predictor of dielectric lifetime, but it can be used to identify defective dielectrics.

The detection of the breakdown event during the breakdown test becomes quite difficult, especially in ultra-thin dielectric films. The event is noted in terms of a sudden decrease of current in the constant current method. According to one panel member, "soft- or quasi-breakdown may occur during testing of oxides thinner than 5 nm. Leakage was also a limiting factor in dielectric scaling. It was mentioned that the minimum thickness is 2.4 nm based on a defect generation model with a tolerable leakage current of 1 A/cm^2 was identified from reliability consideration [1].

The calculation of defect density is based on a Poisson distribution using the following relationship

$$Y = \exp(-AD), \qquad (1)$$

Where:
Y = yield of good units in terms of defined criterion,
A = area of sample, cm^2, and
D = defect density, defects/cm^2

The yield may be represented by *(1-F)* as follows:

$$1\text{-}F = \exp(-kt^n) \qquad (2)$$

Where, *k* and *n* are constants, characteristic of the transformation of a good to a bad device, *F* ($\neq$1) is the fraction of devices that fail, and *t* is the time. Equation (3) is used to convert the cumulative percentages to Weibull format (where *ln* is the natural log operator):

$$\ln\{-\ln(1\text{-}F)\} = +\ln k + n \ln t \qquad (3).$$

The Weibull distribution is often used to present Q_{bd} results. According to one panel member, "the CCS method is preferable from a material characterization point-of-view because CCS is not too sensitive to the variation in the oxide thickness." However, constant voltage stress (CVS) is preferred for thinner oxides. Electrode polarity has a large effect on Time Dependent Dielectric Breakdown (TDDB), at least for CCS measurements and oxides greater than about 5 nm. Improved TDDB is often achieved when carrier injection is from the substrate rather than from the electrode. The effect of grown-in crystalline defects on hard breakdown decreases with the decrease in dielectric film thickness. The temperature at which the wafers are annealed after poly deposition (for activation of the dopant in the poly) is important, e.g., TDDB of an MOS capacitor annealed at 1000°C is much better than that of the MOS capacitor annealed at 900°C. A wet, rather than a dry, oxidation has been noted to improve Q_{bd} (see Figure1). Finally, the effect of COPs on gate dielectric integrity decreases with the decrease in the oxide

thickness. Indications suggest that the effect of metal impurities be also reduced with decreasing oxide thickness [2], although this topic is still an open question with data reported for both possible outcomes.

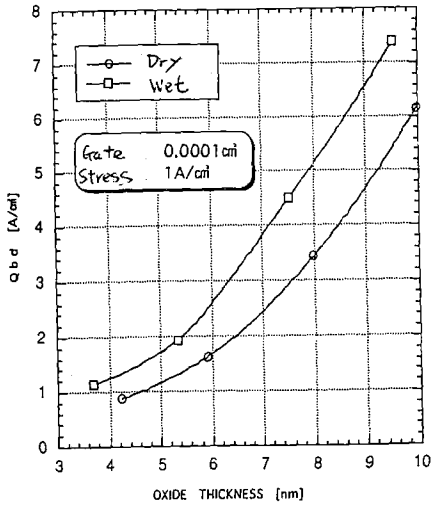

Fig.1. Qbd vs. oxide thickness for wet and dry oxidation. (The figure was supplied by Y.Murakami, Mitsubishi Materials Silicon Corporation).

As described elsewhere in this publication, the oxide wearout and breakdown field can be understood in terms of trap generation inside the oxide and locally high current regions occurring during the breakdown event. Both electric field and electron current contribute to the trap generation process through weakening of the oxide chemical bonds. Many effects occurring in oxides during high voltage stresses can be characterized by measuring the stress-generated trap densities, which are related to the stress-induced-leakage-current (SILC).

The literature [3-5] published on oxides and oxide breakdown mechanisms subsequent to this conference are included here for the interested reader.

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