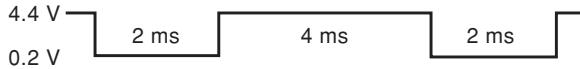


# ANSWERS TO SELECTED PROBLEMS

## CHAPTER 1

- 1-1. (a) and (e) are digital; (b), (c) and (d) are analog  
1-3. (a) 25 (b) 9.5625 (c) 1241.6875  
1-5. 000, 001, 010, 011, 100, 101, 110, 111  
1-7. 1023  
1-9. Nine bits  
1-11.



- 1-13. (a)  $2^N - 1 = 15$  and  $N = 4$ ; therefore, four lines are required for parallel transmission. (b) Only one line is required for serial transmission.

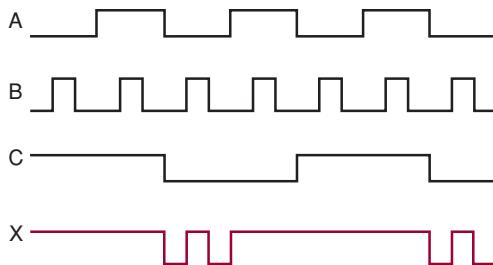
## CHAPTER 2

- 2-1. (a) 22 (c) 2313 (e) 255 (g) 983  
2-2. (a) 100101 (c) 10111101 (e) 1001101  
(g) 11001101 (i) 11111111  
2-3. (a) 255  
2-4. (a) 1859 (c) 14333 (e) 357 (g) 2047  
2-5. (a) 3B (c) 397 (e) 303 (g) 10000  
2-6. (a) 11101000011 (c) 1101111111101  
(e) 101100101 (g) 011111111111  
2-7. (a) 16 (c) 909 (e) FF (g) 3D7  
2-9.  $2133_{10} = 855_{16} = 100001010101_2$   
2-11. (a) 146 (c) 14,333 (e) 15 (g) 704  
2-12. (a) 4B (c) 800 (e) 1C4D (g) 6413

- 2-15. (a) 16 (c) 909 (e) FF (g) 3D7  
2-16. (a) 10010010 (c) 001101111111101 (e) 1111  
(g) 1011000000  
2-17. 280, 281, 282, 283, 284, 285, 286, 287, 288,  
289, 28A, 28B, 28C, 28D, 28E, 28F, 290, 291, 292,  
293, 294, 295, 296, 297, 298, 299, 29A, 29B, 29C, 29D,  
29E, 29F, 2A0  
2-19. (a) 01000111 (c) 000110000111 (e) 00010011  
(g) 10001001011000100111  
2-21. (a) 9752 (c) 695 (e) 492  
2-22. (a) 64 (b) FFFFFFFF (c) 999,999  
2-25. 78, A0, BD, A0, 33, AA, F9  
2-26. (a) BEN SMITH  
2-27. (a) 101110100 (parity bit on the left)  
(c) 11000100010000100 (e) 0000101100101  
2-28. (a) No single-bit error (b) Single-bit error  
(c) Double error (d) No single-bit error  
2-30. (a) 10110001001 (b) 11111111 (c) 209  
(d) 59,943 (e) 9C1 (f) 010100010001 (g) 565  
(h) 10DC (i) 1961 (j) 15,900 (k) 640 (l) 952B  
(m) 100001100101 (n) 947 (o) 10001100101  
(p) 101100110100 (q) 1001010 (r) 01011000 (BCD)  
2-31. (a) 100101 (b) 00110111 (c) 25 (d) 0110011  
0110111 (e) 45  
2-32. (a) Hex (b) 2 (c) Digit (d) Gray (e) Parity;  
single-bit errors (f) ASCII (g) Hex (h) byte  
2-33. (a) 1000  
2-34. (a) 0110  
2-35. (a) 777A (c) 1000 (e) A00  
2-36. (a) 7778 (c) OFFE (e) 9FE  
2-37. (a) 1,048,576 (b) Five (c) 000FF  
2-39. Eight

## CHAPTER 3

3-1.



3-3. x will be a constant HIGH.

3-6. (a) x is HIGH only when A, B, and C are all HIGH.

3-7. Change the OR gate to an AND gate.

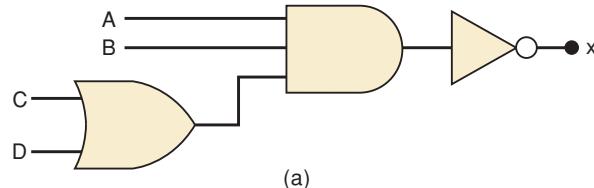
3-8. OUT is always LOW.

3-12. (a)  $x = (\overline{A} + \overline{B})BC$ . x is HIGH only when ABC = 111

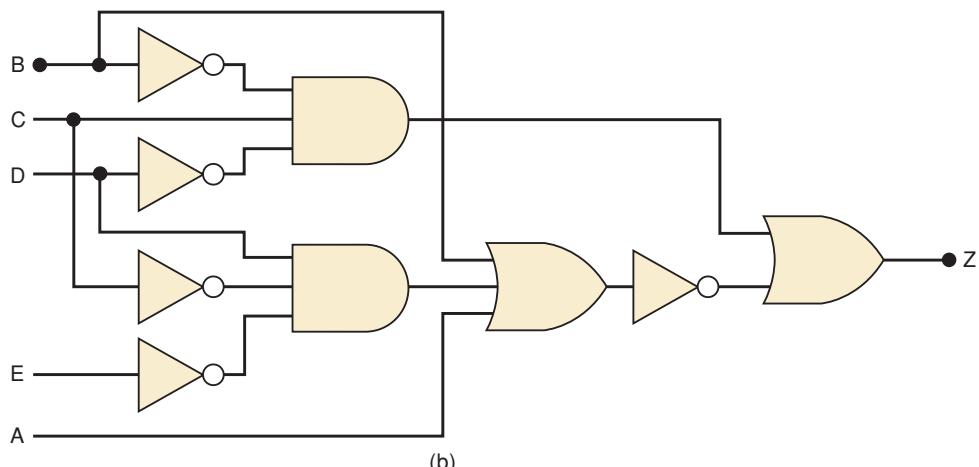
3-13. X is HIGH for all cases where E = 1 except for EDCBA = 10101, 10110, and 10111.

3-14. (a)  $x = D \cdot (\overline{AB} + \overline{C}) + E$ 

3-16.

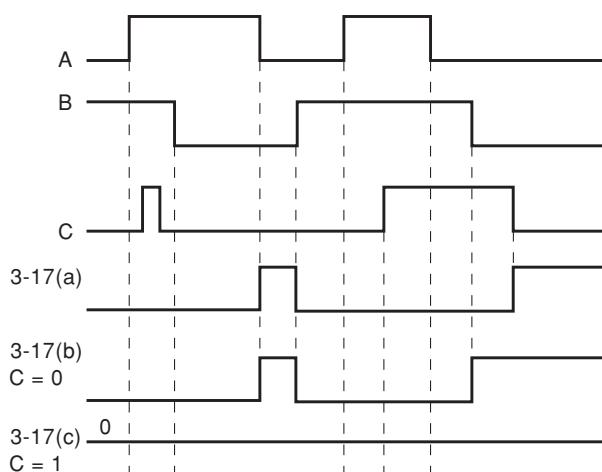


(a)



(b)

3-17.-3-18.

3-19.  $x = (\overline{A} + \overline{B}) \cdot (\overline{B} + \overline{C})$  $x = 0$  only when  $A = B = 0, C = 1$ .

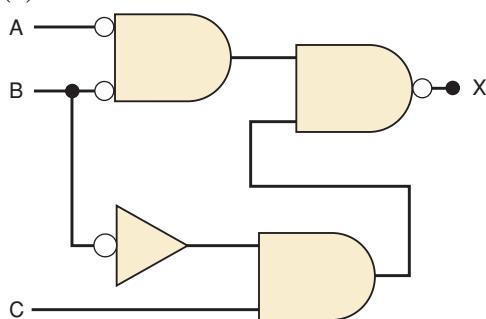
3-23. (a) 1 (b) A (c) 0 (d) C (e) 0 (f) D

(g) D (h) 1 (i) G (j) y

3-24. (a)  $M\bar{P}\bar{N} + \bar{M}\bar{P}N$ 3-26. (a)  $A + \bar{B} + C$  (c)  $\bar{A} + \bar{B} + CD$  (e)  $A + B$ (g)  $\bar{A} + B + \bar{C} + \bar{D}$ 3-27.  $A + B + \bar{C}$ 3-32. (a)  $W = 1$  when  $T = 1$  and either  $P = 1$  or  $R = 0$ .

3-33. (a) NOR (b) AND (c) NAND

3-35. (a)

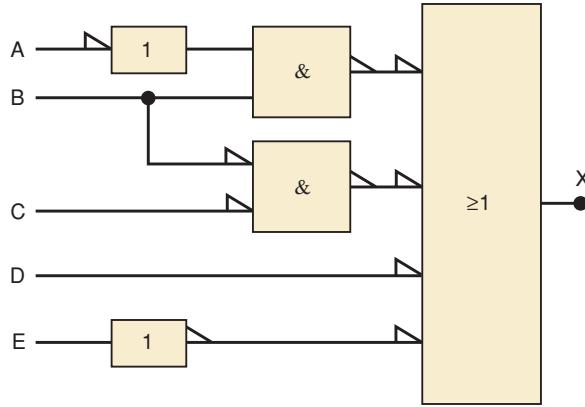


3-38. X will go HIGH when  $E = 1$ , or  $D = 0$ , or  $B = C = 0$ , or when  $B = 1$  and  $A = 0$ .

3-39. (a) HIGH (b) LOW

3-41.  $\overline{\text{LIGHT}} = 0$  when  $A = B = 0$  or  $A = B = 1$ .

3-42. (a)



3-43. (a) False (b) True (c) False (d) True  
(e) False (f) False (g) True (h) False (i) True  
(j) True

3-45. AHDL and VHDL solutions are on the enclosed CD.

3-47. Put INVERTERS on the  $A_7, A_5, A_4, A_2$  inputs to the 74HC30.

3-49. Requires six 2-input NAND gates.

## CHAPTER 4

4-1. (a)  $\overline{CA} + CB$  (b)  $\overline{QR} + Q\overline{R}$  (c)  $C + \overline{A}$  (d)  $\overline{R}\overline{S}\overline{T}$

(e)  $BC + \overline{B}(\overline{C} + A)$

(f)  $BC + \overline{B}(\overline{C} + A)$  or  $BC + \overline{B}\overline{C} + AC$

(g)  $\overline{D} + A\overline{B}\overline{C} + \overline{ABC}$

(h)  $x = ABC + ABD + ABD + \overline{B}\overline{C}\overline{D}$

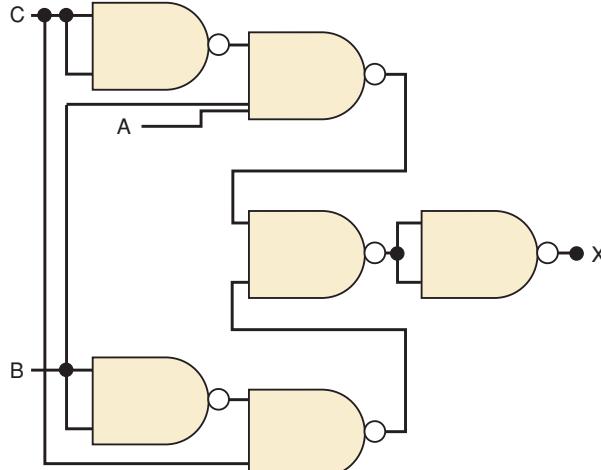
4-3.  $MN + Q$

4-4. One solution:  $\bar{x} = \overline{BC} + ABC$ . Another:

$x = \overline{AB} + \overline{B}\overline{C} + BC$ . Another:  $BC + \overline{B}\overline{C} + \overline{AC}$

4-7.  $x = \overline{A}_3(A_2 + A_1A_0)$

4-9.



4-11. (a)  $x = \overline{A}\overline{C} + \overline{B}C + ACD$

$\overline{C}\overline{D}$	$\overline{C}D$	$CD$	$C\overline{D}$
$\overline{A}\overline{B}$	1 1	1 1	
$\overline{A}B$	1 1		
$A\overline{B}$			1
$AB$			
$A\overline{B}$		1 1	

4-14. (a)  $x = BC + \overline{B}\overline{C} + AC$ ; or  $x = BC + \overline{B}\overline{C} + A\overline{B}$

(c) One possible looping:

$x = \overline{ABD} + ABC + ABD + \overline{B}\overline{C}\overline{D}$ ; another one is:

$x = ABC + ABD + ACD + B\overline{C}D$

4-15.  $x = \overline{A}_3A_2 + \overline{A}_3A_1A_0$

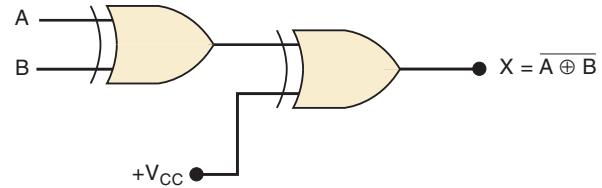
4-16. (a) Best solution:  $x = \overline{B}\overline{C} + AD$

4-17.  $x = \overline{S}_1\overline{S}_2 + \overline{S}_1\overline{S}_3 + \overline{S}_3\overline{S}_4 + \overline{S}_2\overline{S}_3 + \overline{S}_2\overline{S}_4$

4-18.  $z = \overline{BC} + \overline{ABD}$

4-21.  $A = 0, B = C = 1$

4-23. One possibility is shown below.



4-24. Four XNORs feeding an AND gate

4-26. Four outputs where  $z_3$  is the MSB

$z_3 = y_1y_0x_1x_0$

$z_2 = y_1x_1(y_0 + \overline{x}_0)$

$z_1 = y_0x_1(y_1 + \overline{x}_0) + y_1x_0(y_0 + \overline{x}_1)$

$z_0 = y_0x_0$

4-28.  $x = AB(\overline{C} \oplus D)$

4-30.  $N-S = \overline{CD}(A + B) + AB(\overline{C} + \overline{D})$ ;  $E-W = \overline{N}-\overline{S}$

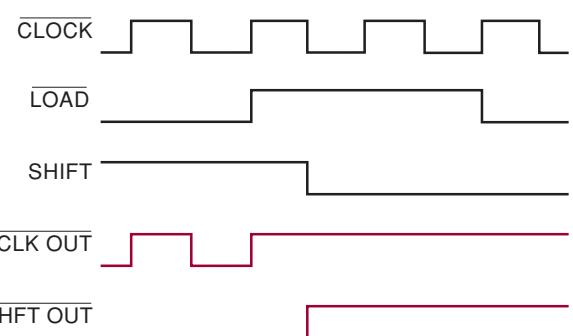
4-33. (a) No (b) No

4-35.  $x = A + BCD$

4-38.  $z = x_1x_0y_1y_0 + x_1\overline{x}_0y_1\overline{y}_0 + \overline{x}_1x_0\overline{y}_1y_0 + \overline{x}_1\overline{x}_0\overline{y}_1\overline{y}_0$

No pairs, quads, or octets

4-40. (a) Indeterminate (b) 1.4–1.8 V (c) See below.



4-43. Possible faults: faulty  $V_{CC}$  or ground on Z2; Z2-1 or Z2-2 open internally or externally; Z2-3 internally open

4-44. Yes: (c), (e), (f). No: (a), (b), (d), (g).

4-46. Z2-6 and Z2-11 shorted together

4-48. Most likely faults:

faulty ground or  $V_{CC}$  on Z1;

Z1 plugged in backwards;

Z1 internally damaged

4-49. Possible faults:

Z2-13 shorted to  $V_{CC}$ ;

Z2-8 shorted to  $V_{CC}$ ;

broken connection to Z2-13;

Z2-3, Z2-6, Z2-9, or Z2-10 shorted to ground

4-50. (a) T, (b) T, (c) F, (d) F, (e) T

4-54. Boolean equation; truth table; schematic diagram

4-56. (a) AHDL: gadgets[7..0] :OUTPUT;  
VHDL: gadgets :OUT BIT\_VECTOR  
(7 DOWNTO 0);

4-57. (a) AHDL: H"98" B"10011000" 152  
VHDL: X"98" B"10011000" 152

4-58. AHDL: outbits[3] = inbits[1];  
outbits[2] = inbits[3];  
outbits[1] = inbits[0];  
outbits[0] = inbits[2];  
VHDL: outbits(3) <= inbits(1);  
outbits(2) <= inbits(3);  
outbits(1) <= inbits(0);  
outbits(0) <= inbits(2);

4-60.

BEGIN

```
IF digital_value[] < 10 THEN
    z = VCC; --output a 1
ELSE z = GND; --output a 0
END IF;
```

END;

4-62.

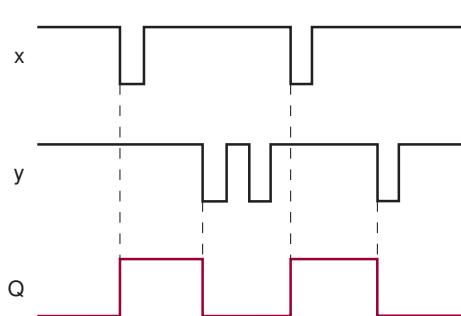
```
PROCESS (digital_value)
BEGIN
    IF (digital_value < 10) THEN
        z <= '1';
    ELSE
        z <= '0';
    END IF;
END PROCESS
```

4-65. S=!P#Q&R

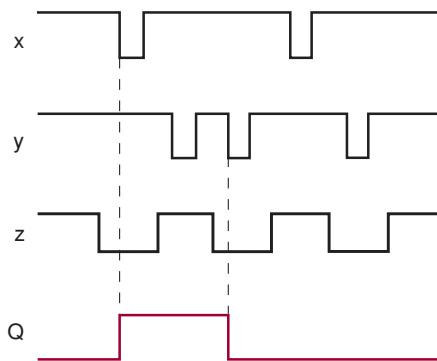
4-68. (a) 00 to EF

## CHAPTER 5

5-1.



5-3.



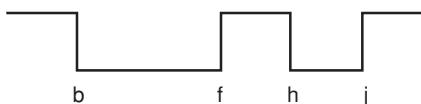
5-6. Z1-4 stuck HIGH

5-9. Assume  $Q = 0$  initially.

For PGT FF:  $Q$  will go HIGH on first PGT of CLK.

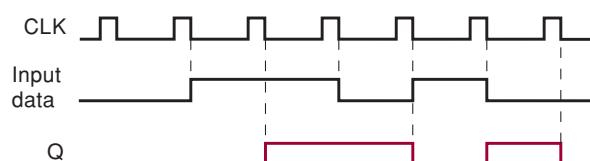
For NGT FF:  $Q$  will go HIGH on first NGT of CLK, LOW on second NGT, and HIGH again on fourth NGT.

5-11.



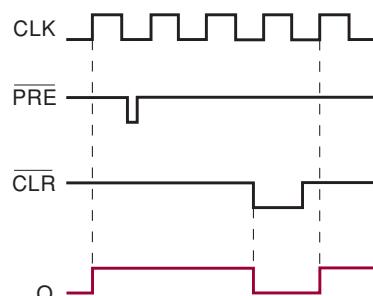
5-12. (a) 5-kHz square wave

5-14.



5-16. 500-Hz square wave

5-21.



5-23. (a) 200 ns (b) 7474; 74C74

5-25. Connect A to J,  $\overline{A}$  to K.

5-27. (a) Connect X to J,  $\overline{X}$  to K. (b) Use arrangement of Figure 5-41.

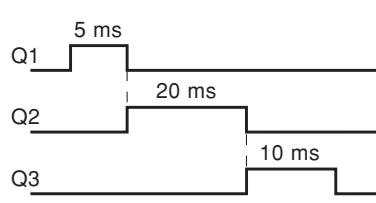
5-29. Connect  $X_0$  to D input of  $X_2$ .

5-30. (a) 101;011;000

5-33. (a) 10 (b) 1953 Hz (c) 1024 (d) 12

5-36. Put INVERTERS on  $A_8$ ,  $A_{11}$ , and  $A_{14}$ .

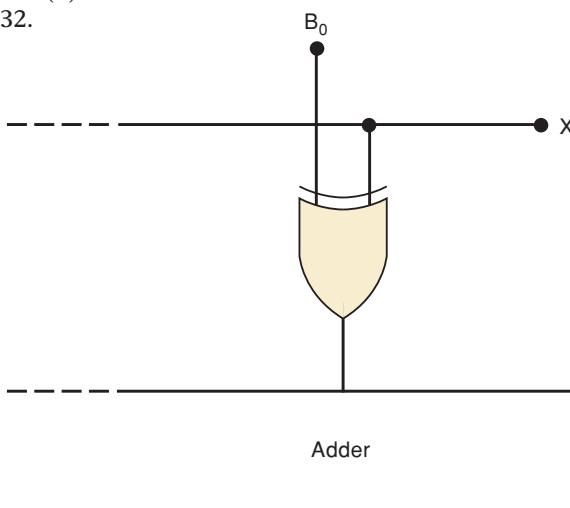
5-41.



- 5-43. (a)  $A_1$  or  $A_2$  must be LOW when a PGT occurs at  $B$ .  
 5-45. One possibility is  $R = 1 \text{ k}\Omega$  and  $C = 80 \text{ nF}$ .  
 5-50. (a) No (b) Yes  
 5-51. (a) Yes  
 5-53. (a) No (b) No  
 5-55. (a) No (b) No (c) Yes  
 5-56. (a) NAND and NOR latch (b) J-K (c) D latch  
 (d) D flip-flop  
 5-59. See Prob5\_59.tdf and prob5\_59.vhd on the enclosed CD.  
 5-61. See Prob5\_61.tdf and prob5\_61.vhd on the enclosed CD.  
 5-66. (a) See Prob5\_66a.tdf on the enclosed CD.  
 (b) See Prob5\_66b.vhd on the enclosed CD.

**CHAPTER 6**

- 6-1. (a) 10101 (b) 10010 (c) 1111.0101  
 6-2. (a) 00100000 (including sign bit) (b) 11110010  
 (c) 00111111 (d) 10011000 (e) 01111111  
 (f) 10000001 (g) 01011001 (h) 11001001  
 6-3. (a) +13 (b) -3 (c) +123 (d) -103  
 (e) +127  
 6-5.  $-16_{10}$  to  $15_{10}$   
 6-6. (a) 01001001; 10110111 (b) 11110100; 00001100  
 6-7. 0 to 1023; -512 to +511  
 6-9. (a) 00001111 (b) 11111101 (c) 11111011  
 (d) 10000000 (e) 00000001  
 6-11. (a) 100011 (b) 1111001  
 6-12. (a) 11 (b) 111  
 6-13. (a) 10010111 (BCD) (b) 10010101 (BCD)  
 (c) 010100100111 (BCD)  
 6-14. (a) 6E24 (b) 100D (c) 18AB  
 6-15. (a) 0EFE (b) 229 (c) 02A6  
 6-17. (a) 119 (b) +119  
 6-19. SUM =  $A \oplus B$ ; CARRY =  $AB$   
 6-21.  $[A] = 1111$ , or  $[A] = 000$  (if  $C_0 = 1$ )  
 6-25.  $C_3 = A_2B_2 + (A_2 + B_2)\{A_1B_1 + (A_1 + B_1)[A_0B_0 + A_0C_0 + B_0C_0]\}$   
 6-27. (a) SUM = 0111  
 6-32.



6-33.

[F]	$C_{N+4}$	OVR
(a) 1001	0	1

- 6-35. (a) 00001100  
 6-37. (a) 0001 (b) 1010  
 6-39. (a) 1111 (b) HIGH (c) No change (d) HIGH  
 6-41. (a) 00000100 (b) 10111111  
 6-43. (a) 0 (b) 1 (c) 0010110  
 6-44. **AHDL**  
 $z[6..0] = a[7..1];$   
 $z[7] = a[0];$   
**VHDL**  
 $z(6..0) <= a(7..1);$   
 $z(7) <= a(0);$   
 6-47. AHDL: ovr <= c[4] \$ c[3];  
 VHDL: ovr <= c(4) XOR c(3);  
 6-48. See Prob6\_48.tdf and Prob6\_48.vhd on the enclosed CD.  
 6-53. Use D flip-flops. Connect  $(S_3 + S_2 + S_1 + S_0)$  to the  $D$  input of the 0 FF;  $C_4$  to the  $D$  input of the carry FF; and  $S_3$  to the  $D$  input of the sign FF.  
 6-54. 000000001001001; 111111110101110

**CHAPTER 7**

Note: Solutions to some problems in Chapter 7 are provided in a document file (*Chapter 7 solutions.doc*) on the enclosed CD. Please see this file as indicated below.

- 7-1. (a) 250 kHz; 50% (b) Same as (a) (c) 1 MHz  
 (d) 32  
 7-3.  $10000_2$   
 7-5. 1000 and 0000 states never occur  
 7-7. (a) See schematic on CD. (b) 33 MHz  
 7-9. Frequency at  $D = 100$  Hz (see diagram on CD)  
 7-11. Replace four-input NAND with a three-input NAND driving all FF CLRs whose inputs are Q5, Q4, and Q1  
 7-13. See diagram on CD.  
 7-15. Counter switches states between 000 and 111 on each clock pulse  
 7-17. See timing on CD.  
 7-19. See timing on CD.  
 7-21. (a) 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, & repeat (b) MOD-12  
 (c) Frequency at QD (MSB) is 1/12 of CLDK frequency  
 (d) 33.3%  
 7-23. (a) see timing on CD (b) MOD-10  
 (c) 10 down to 1 (d) Can produce MOD-10, but not same sequence  
 7-25. (a), (b) See diagrams on CD.  
 7-27. See diagrams on CD.  
 7-29.

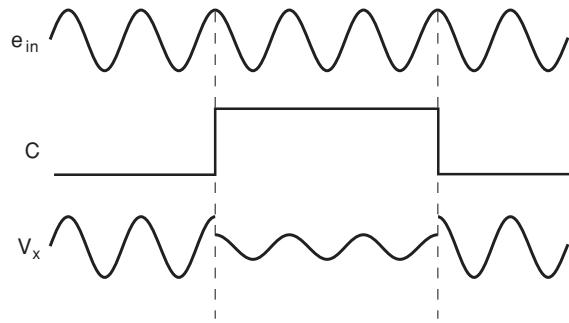
Output:	QA	QB	QC	QD	RCO
Frequency:	3 MHz	1.5 MHz	750 kHz	375 kHz	375 kHz
Duty cycle:	50%	50%	50%	50%	6.25%

- 7-31. Frequency at  $f_{out1} = 500$  kHz, at  $f_{out2} = 100$  kHz  
 7-33.  $12M/8 = 1.5M$     $1.5M/10 = 150k$     $1.5M/15 = 100k$    See diagram on CD  
 7-35. See gate symbols on CD.  
 7-37. See simulation on CD.  
 7-39. See simulation on CD.  
 7-41. See diagram on CD.  
 7-43. (a)  $J_A = B \bar{C}$ ,  $K_A = 1$ ,  $J_B = C A + \bar{C} \bar{A}$ ,  
 $K_B = 1$ ,  $J_C = B \bar{A}$ ,  $K_C = B + A$   
 (b)  $J_A = B \bar{C}$ ,  $K_A = 1$ ,  $J_B = K_B = 1$ ,  $J_C = K_C = B$   
 7-45.  $J_A = K_A = 1$ ,  $J_B = C A + D \bar{A}$ ,  $K_B = A$ ,  $J_C = D \bar{A}$ ,  
 $K_C = B \bar{A}$ ,  $J_D = \bar{C} B \bar{A}$ ,  $K_D = \bar{A}$   
 7-47.  $D_A = \bar{A}$ ,  $D_B = B A + \bar{B} \bar{A}$ ,  $D_C = C A +$   
 $C B + \bar{C} \bar{B} \bar{A}$   
 7-49. See HDL files on CD. mod13\_ahdl mod13\_vhdl  
 7-51. See HDL files on CD. gray\_ahdl gray\_vhdl  
 7-53. See HDL files on CD. divide\_by50\_ahdl  
 divide\_by50\_vhdl  
 7-55. See HDL files on CD. mod256\_ahdl  
 mod256\_vhdl  
 7-57. See HDL files on CD. mod16\_ahdl mod16\_vhdl  
 7-59. See diagram on CD.  
 7-61. See HDL files on CD. mod10\_ahdl mod5\_ahdl  
 mod50\_vhdl mod10\_vhdl mod5\_vhdl  
 7-63. See HDL files on CD.  
 wash\_mach\_delux wash\_mach\_delux  
 7-65. See table on CD.  
 7-67. Eight clock pulses are needed to serially load a  
 74166, since there are eight FFs in the chip.  
 7-69. See timing on CD.  
 7-71. See answer on CD.  
 7-73. See diagram on CD.  
 7-75. See diagram on CD.  
 7-77. Output of 3-in AND or J, K inputs to FF D  
 shorted to ground, FF D output shorted to ground,  
 CLK input on FF D open, B input to NAND is open  
 7-79. See HDL files on CD. siso8\_ahdl siso8\_vhdl  
 7-81. See HDL files on CD. piso8\_ahdl piso8\_vhdl  
 7-83. See simulation on CD.  
 7-85. See HDL files on CD. johnson\_ahdl  
 johnson\_vhdl  
 7-87. See simulation on CD.  
 7-89. (a) Parallel   (b) Binary   (c) MOD-8 down  
 (d) MOD-10, BCD, decade   (e) Asynchronous, ripple  
 (f) Ring   (g) Johnson   (h) All   (i) Presettable  
 (j) Up/down   (k) Asynchronous, ripple   (l) MOD-10,  
 BCD, decade   (m) Synchronous, parallel

## CHAPTER 8

- 8-1. (a) A; B   (b) A   (c) A  
 8-2. (a) 39.4 mW, 18.5 ns   (b) 65.6 mW, 7.0 ns  
 8-3. (a) 0.9 V  
 8-4. (a)  $I_{IH}$    (b)  $I_{CCCL}$    (c)  $t_{PHL}$    (d)  $V_{NH}$   
 (e) Surface-mount   (f) Current sinking   (g) Fan-out  
 (h) Totem-pole   (i) Sinking transistor   (j) 4.75 to  
 5.25 V   (k) 2.5 V; 2.0 V   (l) 0.8 V; 0.5 V  
 (m) Sourcing  
 8-5. (a) 0.7 V; 0.3 V   (b) 0.5 V; 0.4 V   (c) 0.5 V; 0.3 V  
 8-6. (b) AND, NAND   (c) Unconnected inputs

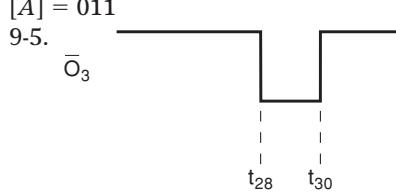
- 8-7. (a) 40   (b) 33  
 8-8. (a)  $20 \mu A/0.4$  mA  
 8-9. (a) 30/15   (b) 24 mA  
 8-11. Fan-out is not exceeded in either case.  
 8-13. 60 ns; 38 ns  
 8-14. (a)  $2 \text{ k}\Omega$   
 8-15. (b)  $4.7\text{-k}\Omega$  resistor is too large.  
 8-19. a, c, e, f, g, h  
 8-21. 12.6 mW  
 8-27. AB + CD + FG  
 8-29. (a) 5 V   (b)  $R_S = 110 \Omega$  for LED current of 20 mA  
 8-30. (a) 12 V   (b) 40 mA  
 8-33. Ring counter  
 8-36. 1.22 V; 0 V  
 8-37.



- 8-38. -1 and -2  
 8-39. (a) 74HCT   (b) Converts logic voltages  
 (c) CMOS cannot sink TTL current.   (d) False  
 8-41. (a) None  
 8-44. Fan-out of 74HC00 is exceeded; disconnect pin 3  
 of 7402 and tie it to ground.  
 8-46.  $R_2 = 1.5 \text{ k}\Omega$ ,  $R_1 = 18 \text{ k}\Omega$   
 8-49. (b) is a possible fault.  
 8-50. 0 V to -11.25 V and back up to -6 V

## CHAPTER 9

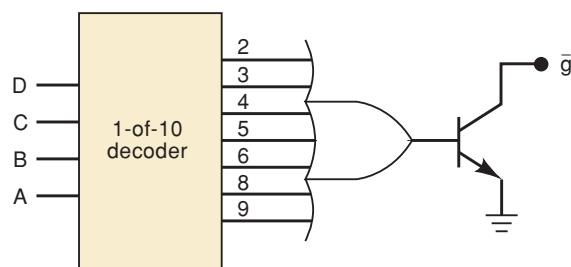
- 9-1. (a) All HIGH   (b)  $\bar{O}_0 = \text{LOW}$   
 9-2. Six inputs, 64 outputs  
 9-3. (a)  $E_3E_2E_1 = 100$ ; [A] = 110   (b)  $E_3E_2E_1 = 100$ ;  
 [A] = 011



- 9-7. Enabled when D = 0

- 9-10. Resistors are  $250 \Omega$ .

- 9-12.



9-13. (a), (b) Encoder (c), (d), (e) Decoder

9-17. The fourth key actuation would be entered into the MSD register.

9-18. Choice (b)

9-20. (a) Yes (b) No (c) No

9-21.  $A_2$  bus line is open between Z2 and Z3.

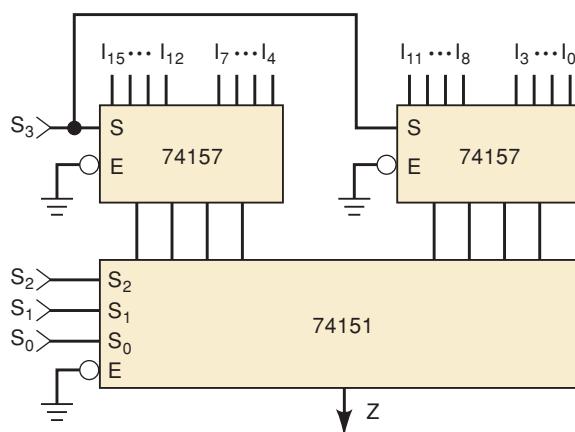
9-23.  $g$  segment or decoder output transistor would burn out.

9-25. Decoder outputs:  $a$  and  $b$  are shorted together.

9-26. Connection 'f' from decoder/driver to XOR gate is open.

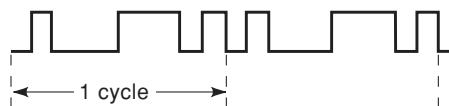
9-29. A 4-to-1 MUX

9-31.



9-32. (b) The total number of connections in the circuit using MUXes is 63, not including  $V_{CC}$  and GND, and not including the connections to counter clock inputs. The total number for the circuit using separate decoder/drivers is 66.

9-33.



9-35.

<b>A</b>	<b>B</b>	<b>C</b>	
0	0	0	$0 \Rightarrow l_0$
0	0	1	$0 \Rightarrow l_1$
0	1	0	$0 \Rightarrow l_2$
0	1	1	$1 \Rightarrow l_3$
1	0	0	$0 \Rightarrow l_4$
1	0	1	$1 \Rightarrow l_5$
1	1	0	$1 \Rightarrow l_6$
1	1	1	$1 \Rightarrow l_7$

9-37. Z = HIGH for DCBA = 0010, 0100, 1001, 1010.

9-39. (a) Encoder, MUX (b) MUX, DEMUX

(c) MUX (d) Encoder (e) Decoder, DEMUX

(f) DEMUX (g) MUX

9-41. Each DEMUX output goes LOW, one at a time in sequence.

9-43. Five lines

9-46. (a) Sequencing stops after actuator 3 is activated.

9-47. Probable fault is short to ground at MSB of tens MUX.

9-48.  $Q_0$  and  $Q_1$  are probably reversed.

9-49. Inputs 6 and 7 of MUX are probably shorted together.

9-50.  $S_1$  stuck LOW

9-53. Use three 74HC85s

9-55.  $A_0$  and  $B_0$  are probably reversed.

9-57.  $\overline{OE}_C = 0$ ,  $\overline{IE}_C = 1$ ;  $\overline{OE}_B = \overline{OE}_A = 1$ ;  $\overline{IE}_B = \overline{IE}_A = 0$ ; apply a clock pulse.

9-61. (a) At  $t_3$ , each register holds 1001.

9-63. (a) 57FA (b) 5000 to 57FF (c) 9000 to 97FF (d) no

9-65. See Prob9\_65.tdf and Prob9\_65.vhd on the enclosed CD.

## CHAPTER 10

10-1. (d) 20 Hz (e) Only one LED will be lit at any time.

10-2. 24

10-3. Four states = four steps \*  $15^\circ/\text{step} = 60^\circ$  of rotation

10-5. Three state transitions \*  $15^\circ/\text{step} = 45^\circ$  of rotation

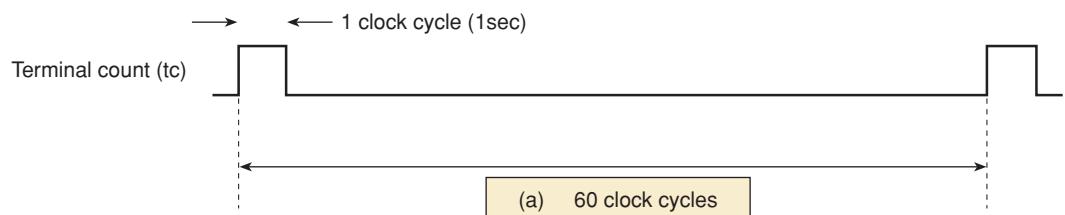
10-10. 1111

10-12. (a) 1011

10-13. No

10-15. The data go away (hi-Z) before the DAV goes LOW. The hi-Z state is latched.

10-16.



10-17.  $60 \text{ cycles/sec} * 60 \text{ sec/min} * 60 \text{ min/hr} * 24 \text{ hr/day} = 5,184,000 \text{ cycles/day}$ . This takes a long time to generate a simulation file.

10-18. When the set input is active, bypass the prescaler and feed the 60-Hz clock directly into the units of seconds counter.

10-22. See Prob10\_22.tdf and Prob10\_22.vhd on the enclosed CD.

## CHAPTER 11

11-1. (f), (g) False

11-3. LSB = 20 mV

11-5. Approximately 5 mV

11-7. 14.3 percent, 0.286 V

11-9. 250.06 rpm

11-11. The eight MSBs: PORT[7..0]  $\Rightarrow$  DAC[9..2]

11-13.  $800 \Omega$ ; no

11-15. Uses fewer different  $R$  values

11-17. (a) Seven

11-19. 242.5 mV is not within specifications.

11-21. Bit 1 of DAC is open or stuck HIGH.

11-22. Bits 0 and 1 are reversed.

11-24. (a) 10010111

11-27. (a) 1.2 mV (b) 2.7 mV

11-28. (a) 0111110110

11-31. Reconstructed waveform frequency is 3.33 kHz.

11-32. (a) 5 kHz (b) 9.9 kHz

11-33. Digital ramp:  $a, d, e, f, h$ . SAC:  $b, c, d, e, g, h$

11-36.  $80 \mu\text{s}$

11-38. 2.276 V

11-40. (a) 00000000 (b) 500 mV (c) 510 mV

(d) 255 mV (e) 01101110 (f)  $0.2^\circ\text{F}$ ; 2 mV

11-45. Switch is stuck closed; switch is stuck open, or capacitor is shorted.

11-47. (a) Address is EAxx.

11-52. False: a, e, g; True: b, c, d, f, h

## CHAPTER 12

12-1. 16,384; 32; 524,288

12-3.  $64\text{K} \times 4$

12-7. (a) Hi-Z (b) 11101101

12-9. (a) 16,384 (b) Four (c) Two 1-of-128 decoders

12-11. 120 ns

12-15. The following transistors will have open source connections:  $Q_0, Q_2, Q_5, Q_6, Q_7, Q_9, Q_{15}$ .

12-17. (a) Erases all memory locations to hold  $\text{FF}_{16}$

(b) Writes  $3C_{16}$  into address  $2300_{16}$

12-19. Hex data: 5E, BA, 05, 2F, 99, FB, 00, ED, 3C, FF, B8, C7, 27, EA, 52, 5B

12-20. (a) 25.6 kHz (b) Adjust  $V_{\text{ref}}$

12-22. (a)  $[B] = 40$  (hex);  $[C] = 80$  (hex) (b)  $[B] = 55$  (hex);  $[C] = AA$  (hex) (c) 15,360 Hz (d) 28.6 MHz (e) 27.9 kHz

12-24. (a) 100 ns (b) 30 ns (c) 10 million (d) 20 ns (e) 30 ns (f) 40 ns (g) 10 million

12-30. Every  $7.8 \mu\text{s}$

12-31. (a) 4096 columns, 1024 rows (b) 2048 (c) It would double.

12-34. Add four more PROMs (PROM-4 through PROM-7) to the circuit. Connect their data outputs and address inputs to data and address bus, respectively. Connect  $AB_{13}$  to  $C$  input of decoder, and connect decoder outputs 4 through 7 to  $CS$  inputs of PROMs 4 through 7, respectively.

12-38. F000–F3FF; F400–F7FF; F800–FBFF; FC00–FFFF

12-40.  $B$  input of decoder is open or stuck HIGH.

12-42. Only RAM modules 1 and 3 are getting tested.

12-43. The RAM chip with data outputs 4 through 7 in module 2 is not functioning properly.

12-44. RAM module 3, output 7 is open or stuck HIGH.

12-46. Checksum = 11101010.

## CHAPTER 13

13-2. The necessary speed of operation for the circuit, cost of manufacturing, system power consumption, system size, amount of time available to design the product, etc.

13-4. Speed of operation

13-6. Advantages: highest speed and smallest die area; Disadvantages: design/development time and expense

13-8. SRAM-based PLDs must be configured (programmed) upon power-up.

13-10. In a PLD programmer or in-system (via JTAG interface)

13-12. pin 1—GCLR<sub>n</sub> (Global Clear)

pin 2—OE2/GCLK2 (Output Enable 2/Global Clock 2)

pin 83—GCLK1 (Global Clock 1)

pin 84—OE1 (Output Enable 1)

13-14. Logic cell in MAX7000S is AND/OR circuit versus look-up table in FLEX10K; EEPROM (MAX7000S) and SRAM (FLEX10K); MAX7000S is nonvolatile; FLEX10K has greater logic resources.