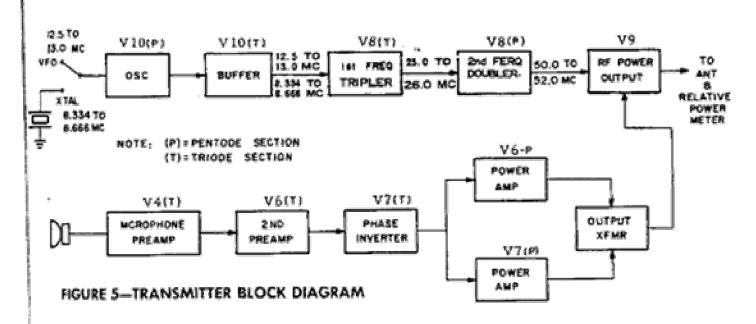
The output of the first mixer V2 is fed to the grid of the pentode portion of the 2nd mixer (V3). The triode portion of V3 is a 6.2 Mc crystal oscillator. The output of the 6.2 Mc crystal oscillator is fed to the grid of the pentode portion of the 2nd mixer V3 where it combines with the 5745 Kc signal fed from the 1st mixer V2. The output of the 2nd mixer V3 is tuned to 455 Kc which is the second intermediate frequency.

The output of the 2nd mixer stage V3 is fed through two stages of IF amplification (V4 and V5) and then to a 1N60 diode detector. The 1N60 diode detector rectifies the IF signal to produce the audio signal and the AVC voltage.

After filtering the AVC voltage is applied to both 455 Kc IF amplifiers, the second mixer, and the Nuvistor RF amplifier to provide automatic volume control.

After filtering the audio signal is fed through a self-adjusting automatic noise limiter to the YOL control. From the volume control the signal is fed to the input of the first audio amplifier V7. After amplification the audio signal is fed to the grid of the triode section of the phase inverter (V6). The phase inverter processes the audio signal and feeds it to the grids of the pentode sections of two tubes (V6 and V7) which operate as push-pull power amplifiers. The output of the push-pull power amplifier is fed to the primary of the output transformer (T5).

The secondary of the output transformer (T5) has two windings. One winding is used to drive the receiver speaker. The second winding is used to modulate the transmitter when relay K3 is in the proper position.



TEAMSMITTER

Refer to the transmitter block diagram Figure 5 while reading the following. If greater detail seesired at any point, refer to the schematic diagram.

The transmitter signal is generated in the pentode section of the oscillator/buffer stage V10. The oscillator may be either crystal-controlled or used as a VFO. The triode section of the scillator/buffer stage V10 is a buffer amplifier used to isolate the oscillator from undesirable flects which might be caused by the loading of the following circuitry. The output of the buffer implifier V10 is fed to the input of the first frequency doubler/tripler stage, triode section of V8.