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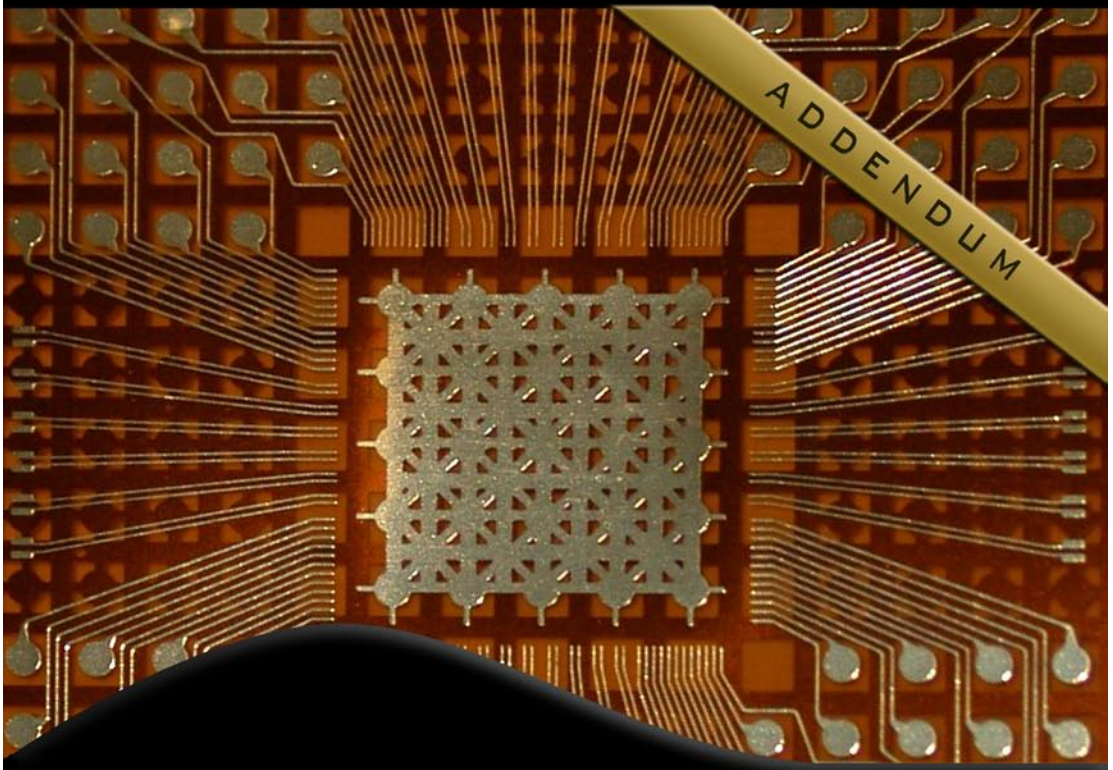

FLEXIBLE CIRCUIT TECHNOLOGY

JOSEPH FJELSTAD

Flexible Circuit Technology

Third Edition

ADDENDUM

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Flexible Circuit Technology

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INTRODUCTION

Welcome to this new revision of the Third Edition of Flexible Circuit Technology. This revision marks an important turning point for this text as it now includes chapter sections by some of the world's top experts with experience in flexible circuit technology, including: Top-tier GE electronics miniaturization researcher William (Bill) Burdick; Kevin Durocher, GE Process Development Engineer; reliability expert Werner Engelmaier (known around the globe as "Mr. Reliability"); and world-renowned soldering guru Bob Willis. It also includes a section on solderless assembly of flexible circuit technology based on the rapidly evolving Occam process concept, which embraces simplification and minimalism.

This revision is, thus, another (hopefully) timely update for the reader and an important expansion over earlier work to keep pace with the rapid changes in this important enabling technology. Even as these words are being written, it is clear that there will soon be need for a fourth edition to capture all of the technological improvements that have come to light even as the revision process was ongoing.

With the last point in mind, the reader of this book is invited to participate in that effort (which will begin shortly) by sharing his or her knowledge with other readers. As evidenced by the outstanding contributions that have been made by my esteemed colleagues to this expanded effort, future editions will be the work of increasing numbers of contributors. Thus, if the reader has any unique materials, processes or structures that he or she would like to bring to the attention of other readers of this text, it is hoped that those individuals will consider sharing their advances with the readers of the next edition of this book. Thank you in advance.

Kindest Regards,
Joseph Fjelstad
May 2008

ABOUT THE AUTHOR

Werner Engelmaier has over 43 years of experience in electronic packaging and interconnection technology. Known as "Mr. Reliability," he is the president of Engelmaier Associates, L.C., a firm providing consulting services on reliability, quality aspects of electronic packaging and interconnection technology. Prior to that, he was a Distinguished Technical Staff at Bell Labs for 24 years.

He authored over 180 technical publications and has been awarded a number of patents. Werner has conducted many tutorial workshops and has contributed to numerous task forces, specifications, standards, and design guides. He is chairman of the IPC Product Reliability Main Committee.

Mr. Engelmaier has been the recipient of many honors and awards, including R&D 100 Awards in 1978 and 1981; the Bell Labs Distinguished Technical Staff Award in 1986; the IEPS Electronic Packaging Achievement Award in 1987; and the IPC President's Award in 1988. He was inducted into the IPC Hall of Fame in 2003 and is a Fellow of IMAPS.

Born in Vienna, Austria, Mr. Engelmaier holds Mechanical Engineering degrees from TGM in Vienna, from USC, and from MIT.

Chapter 1

Flex Circuit Design Guide for Static and Dynamic Flexing

By Werner Engelmaier

Introduction

Flexible circuits by their very nature have an inherent ability to flexurally deform. This permits the roll-to-roll manufacturing processes for large volume production. In roll-to-roll processing the rolls around which the flex circuits are transported typically have 3-to-4 inch radii. The numerous traversals around processing rolls, even though each traversal contributes to the cumulative fatigue damage, do not come close to exhausting the ductility of the copper conductors.

Designers have exploited the inherent flexibility to design flex circuits to be flexurally deformed during assembly, adjustment, and repair procedures, to have complex three-dimensional final geometries, and to sustain multiple flexural cycles during functional life. Flexural deformation imposes strains,

which are inversely proportional to the bend radius, on the materials in the flex circuits. The applied strains are directly proportional to the flex circuit thickness and are largest at the outer surfaces.

The bend radii imposed by the designers are typically considerably smaller than those of the processing rolls. This makes it necessary for the designer to understand the flexibility limitations of the flex circuit and to take these limitations into consideration not only for the final product geometry and functional life, but also for all prior assembly, adjustment, and repair procedures to avoid yield problems and functional life failures.

The items that need attention in the design phase can conveniently be divided into three groups:

1) conductor layout
2) flex circuit stack up
3) material selection

The factors influencing these design considerations from a flexibility viewpoint are:

1) assembly, adjustment and repair procedures
2) final circuit geometry
3) number of flexures during functional life

From the foregoing it should be clear that these design considerations are necessary only in bend regions of flex circuits where the circuits will be flexurally deformed. However, many of the points raised here should be carried out as a matter of good design practice whether or not the flex circuits contain bend regions.

Strain vs. Ductility

Determination of Strain

The bending of flex circuit causes deformation, strain, and stresses in the circuit materials. The strains and stresses are functionally related for each material via the stress-strain diagram. The forces necessary to cause flexural deformation are small; the flexural deformation is determined by the imposed bend geometry. Thus, the amount of induced strain is the parameter of interest. Ductility, D_f, is the ability of a material to deform plastically before

fracture occurs, and is defined as the strain at fracture, $\varepsilon_{fracture}$:

$$D_f \equiv \varepsilon_{fracture} \quad [1]$$

Usually, ductility is determined as the elongation or the reduction of area caused by a tension test. Ductility of metallic foils and flex circuit conductors cannot however be determined with a tension test because of the cross-sectional and gage length aspect ratios of the test samples, and a fatigue ductility test is used, such as ASTM E 796 [Ref. 1]or IPC TM-650, TM 2.4.2.1 [Ref. 2]. In principle at least, the ductility values determined by these various methods should be identical. Uniaxial strain relates to the dimensions before and after deformation by:

$$\varepsilon = \frac{L - L_0}{L_0} \quad [2]$$

where ε = strain (x 100, %),
L = length after deformation,
L_0 = original length.

In flexure, the strain is not uniform but has a linear distribution from a maximum compressive strain _c,max, on the concave surface to a maximum tensile strain _t,max, on the convex surface. This strain distribution is illustrated in Figure 1. As can be seen in Figure 1, the strain is zero at the neutral surface and increases proportionally with the distance from the neutral surface.

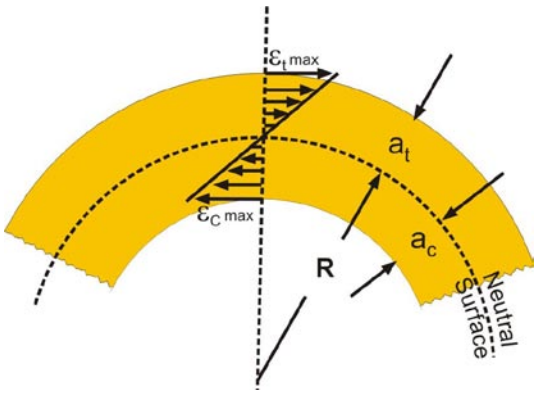

Fig. 1: Strain Distribution in a Bent Beam

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[1] "Standard Test Method for Ductility Testing of Metallic Foil," ASTM E 796, Annual Book of ASTM Standards, ASTM, Philadelphia, PA, 1981.

[2] "Flexural Fatigue and Ductility, Foil," Test Method 2.4.2.1, IPC Test Methods Manual IPC TM-650, The Institute for Interconnecting and Packaging Electronic Circuits, Lincolnwood, IL, August 1980

The strains can be calculated by the following simple relationship:

$$\varepsilon = \frac{y}{R} \quad [3]$$

where y = distance from the neutral surface,
R = radius of curvature of the neutral surface.

Thus, the maximum tensile and compressive strains are at

$$\varepsilon_{t,\max} = \frac{a_t}{R} \quad \text{and} \quad \varepsilon_{c,\max} = \frac{a_c}{R} \quad [4, 5]$$

where $\varepsilon_{t,\max}$ = tensile strain at the convex surface,
a_t = distance of the convex surface from the neutral surface,
$\varepsilon_{c,\max}$ = compressive strain at the concave surface,
a_c = distance of the convex surface from the neutral surface.

In Figure 1 and Equations 4 and 5, two items are presumed known: a) the location of the neutral surface, and b) the radius of curvature of the neutral surface. For symmetric beams bent over circular mandrels these parameters are easily located: a) the neutral surface lies in the center of the beam, and b) the radius of curvature of the neutral surface is the sum of the mandrel radius and half the beam thickness. Flex circuits can be designed either as single-sided, double-sided or multi-layered circuits. Assuming that the conductor patterns on both circuit sides are essentially identical and follow the other layout recommendations, double-sided and multi-layered flex circuits are symmetric beams [Note that in bending into the predominantly plastic regime, such as folding, shifts in the location of the neutral surface can occur due to 1) the different plastic behavior of materials in tensile and compressive loading and 2) the different plastic behavior of the component materials in the case of asymmetric beams] and the maximum tensile and compressive strains are of equal magnitude (but of opposite sign) and can be determined from:

$$\varepsilon_{\max} = \varepsilon_{t,\max} = -\varepsilon_{c,\max} = \frac{\frac{t}{2}}{\rho_{\min} + \frac{t}{2}} \quad [6]$$

where ε_{max} = maximum strain at the conductor,
t = flex circuit thickness,
ρ_{min} = minimum radius of curvature on the concave side of the bent flex circuit.

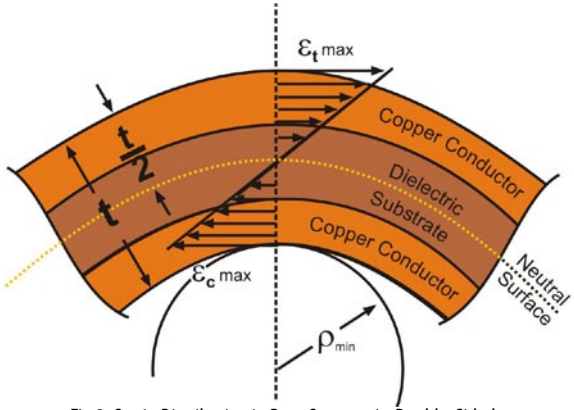

Fig 2: Strain Distribution in Bent Symmetric, Double-Sided Flexible Printed Circuit Wiring

Figure 2 illustrates the relationship expressed in Equation 6, which states that the strain increases with increasing flex circuit thickness and decreasing radius of curvature.

It should be noted that the flex circuit bend geometry shown in Figure 2 is not circular. Flex circuits may be bent without the benefit of a forming mandrel. The resulting bend geometries are non-circular and have a minimum radius of curvature at the bend apex which is significantly smaller than the radius resulting from a circular bend in the same space.

This implies that for tight geometries for which the flex circuit conductors will have to be deformed into the plastic regime, the use of a forming mandrel is recommended.

In the case of a flex circuit with the conductor in the center between two dielectric layers, Equation 6 changes to:

$$\varepsilon_{max} = \varepsilon_{t,max} = -\varepsilon_{c,max} = \frac{\frac{t_{Cu}}{2}}{\rho_{min} + \frac{t}{2}} \qquad [7]$$

where ε_{max} = maximum strain at the conductor,
t_{Cu} = conductor thickness,
t = flex circuit thickness,
ρ_{min} = minimum radius of curvature on the concave side of the bent flex circuit.

For asymmetric beams, such as single-sided flex circuits, the neutral surface is not located in the center of the beam. For static equilibrium, the forces on the beam section must sum to zero, thus

$$\int_A \sigma dA = 0 \qquad [8]$$

where σ = stress distribution in the beam section and,
A = beam section area.

The locus of balance of tensile and compressive forces is the neutral surface and can be calculated using Equations 3 and 8 and the stress strain relationships of the materials in the beam.

For single-sided flex circuits for which the criterion

$$\left(\frac{t}{t_{Cu}} - 1\right)^2 \frac{E_S}{E_{Cu}} \leq 0.1 \qquad [9]$$

where t_{Cu} = conductor thickness,
E_S = modulus of elasticity of flex circuit dielectric,
E_{Cu} = modulus of elasticity of copper conductor.

is satisfied, the center of the copper conductors is a close approximation of the neutral surface location. Therefore,

$$a \cong \frac{t_{Cu}}{2} \qquad [10]$$

where a = location of neutral surface of flex circuit from the flex circuit conductor surface (see Figure 3).

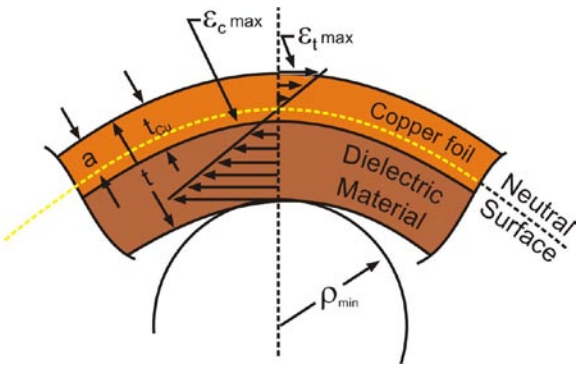

Fig. 3 Strain Distribution in Bent Single-Sided Flexible Printed Circuit Wiring

The location of the neutral surface for flex circuit designs that do not meet the criteria in Equation 10 can be calculated under the assumption of totally elastic bending. This assumption allows calculation of the neutral surface subject to the cautions regarding plastic deformations.

Using the concept of equivalent homogeneous cross sections with the modulii of elasticity (see Table I) and the thickness of the various flex circuit component layers, location of the neutral surface is

$$a = \frac{\sum_i E_i t_i a_i}{\sum_i E_i t_i} \qquad [11]$$

where E_i = modulus of elasticity of material in the flex circuit component layer under consideration,
t_i = centroid location of the flex circuit component layer under consideration from the FPW conductor surface,
a_i = thickness of the FPW component layer under consideration.

Table I. Typical Mechanical Properties of Some Flexible Printed Materials.

Material	Modulus of Elasticity $Ex10^{-6}$ psi	Tensile Strength $s_u x10^{-3}$ psi	Fracture Elongation e, %	Fracture Ductility* D_f, %
Epoxy Polyester	0.20	7.6	20.0	N/A
Epoxy-Polyester-Glass	0.47	15.0	0.3	N/A
Kapton	0.40	34.0	82.0	N/A
ED Vendor Copper				
Standard	12.0	41.0	3 - 18	5-25
Annealed	12.0	34.0	10 - 25	15-50
ED Copper Overplating	12.0	41.0	12 - 30	60 - 90
Rolled Annealed Copper	17.0	27.0	15 - 35	50 - 150
Flex Circuits,				
Vendor Copper only	12.0	41.0	—	5 - 25
Overplated	12.0	58.0	—	7 - 60
Solder (60/40 Sn/Pb)	3.3	7.6	21.0	—
Covercoat	0.043	1.0	30.0	—
Mylar	0.55	25.0	120.0	—

* The ductility of FPW, copper-clad flexible laminate, and copper foil can be determined using the IPC Test Methods 3.4.3.1, 2.4.3.2 and 2.4.2.1 of IPC-TM-650, respectively.

With the location of the neutral surface determined either from Equation 10 or 11 as appropriate, the maximum strains in the conductor are then

$$\varepsilon_{t,\max} = \frac{a}{\rho_{\min} + t - a} \quad [12]$$

and

$$\varepsilon_{c,\max} = \frac{a - t_{Cu}}{\rho_{\min} + t - a} \quad [13]$$

for the bend direction shown in Figure 3 and

$$\varepsilon_{t,\max} = \frac{t_{Cu} - a}{\rho_{\min} + a} \quad [14]$$

and

$$\varepsilon_{c,\max} = \frac{-a}{\rho_{\min} + a} \quad [15]$$

for a bend in the opposite direction.

Determination of Allowable Strain Range

As mentioned earlier, repeated cyclic flexing causes cumulative fatigue damage which can lead to failure due to ductility exhaustion even though the strains imposed during each individual flexure are much smaller than the available ductility. It can be argued that any bending can be viewed as at least a partial flexure fatigue cycle, thus allowing a unified approach for single bends and multiple flexures.

For cyclic fatigue, the cumulative fatigue damage depends on the applied strain range, $\Delta\varepsilon_{max}$, which is the strain amplitude between the reversal points in the bending cycle. Thus:

$$\Delta\varepsilon_{\max} = \varepsilon_{+\text{Reversal}} - \varepsilon_{-\text{Reversal}} \quad [16]$$

where $\varepsilon_{+\text{Reversal}}$ and $\varepsilon_{-\text{Reversal}}$ have to be determined for the extreme reversal positions during the flex cycle using Equations 6 through 15 as appropriate. It should be emphasized here that except for fully reversed cyclic bending, where the strains at the reversal points are of equal magnitude but opposite signs, the values for ρ_{min} will be different at the two reversal positions. In fact, the strains at both reversal positions can be tensile strains if the cycling does not come back to the original flat, zero strain flexible printed wiring position.

From fatigue concepts, the relationship between the fatigue life, the material properties, and the strain range causing failure is [Ref. 3]

$$\Delta\varepsilon = N_f^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{0.178\log\frac{10^5}{N_f}} \qquad [17]$$

where $\Delta\varepsilon$ = cyclic strain range

N_f = flex life in mean cycles-to-failure

D_f = ductility of the conductor material

S_u = ultimate tensile strength of the conductor material

E = modulus of elasticity of the conductor material

In Equation 16 the first term is the Coffin-Manson relationship between the applied plastic strains and fatigue failure and the second term represents the fatigue contribution of the elastic strains. Figure 4 gives a graphical representation of Equation 16 for copper electrodeposited without brighteners at a ductility of D_f = 30%. The contributions due to the applied plastic and elastic strain ranges are shown separately in Figure 4.

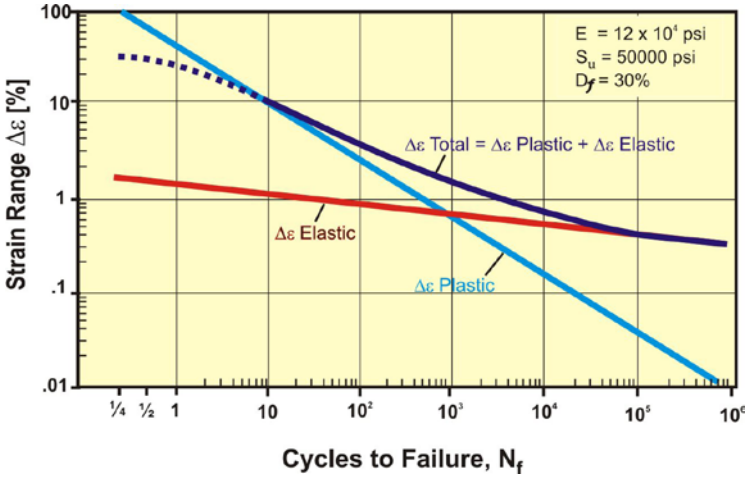

Figure 4. Strain Range-Fatigue Life Curve for Electrodeposited Copper

Equation 16 has been demonstrated to closely describe the strain range-fatigue life behavior of a wide variety of metals over the whole range of fatigue lives with the exception of extremely low cycle fatigue (N_f < 20 cycles-to-failure). At extremely low-cycle fatigue, deviations from the Coffin-Manson

[3] Engelmaier, W., "Results of IPC Copper Foil Ductility Round Robin Study," IPC-TR-484, The Institute for Interconnecting and Packaging Electronic Circuits Lincolnwood IL April 1986

relationship occur due to the increasingly more significant effects of strain hardening, susceptibility to crack initiation at non-homogeneities, neutral surface shifts, and pre-straining caused by the initial bend. These deviations can collectively be described by the empirical relationship

$$\Delta\varepsilon = \frac{N_f^{0.4} D_f^{0.75}}{N_f + C} + 0.9 \frac{S_u}{E} \left[\frac{\exp(D_f)}{0.36} \right]^{0.178 \log \frac{10^5}{N_f}} \quad [18]$$

where C = extreme low-cycle fatigue parameter,
and = 0.5 for electrodeposited copper.

These deviations described by Equation 18 are shown in Figure 4 by the dashed curves.

Low-cycle fatigue, where the strains applied during bending are primarily in the plastic strain range, is the regime for fatigue lives of less than 500 cycles-to-failure. For situations where only a small number of flex cycles (N_f < 20 cycles-to-failure) is employed, Equation 18 can conveniently be simplified by neglecting the contribution from the elastic strain range. Therefore, for small numbers of flexures, the allowable strain range for copper foil can be approximated by:

$$\Delta\varepsilon = \frac{N_f^{0.4} D_f^{0.75}}{N_f + 0.5} \quad \text{for } N_f \leq 20, \quad [19]$$

where a single bend into a final geometry is counted as a quarter fatigue cycle (N_f = 1/4).

Applied Strain versus Available Ductility

In order to avoid failures due to conductor fractures, the allowable strain range (Eq. 19) has to exceed the maximum applied strain range, such that

$$\Delta\varepsilon_{max} < \frac{N^{0.4} D_f^{0.75}}{N + 0.5} \quad [20]$$

where N = estimated number of flexures.

Unfortunately, due to the statistical nature of both the applied strains and the available ductilities (see 3.0), reality is not a simple as might be concluded from equation 20.

Statistical Nature of Strain and Ductility

Distribution of Applied Strain

Primarily because of deviations in the minimum bend radii from the design radius resulting from bending without forming mandrels, the strains that a bent flex circuit will be subjected to will in practice have a distribution rather than a fixed value. Since, typically, the design radius of a flex circuit bend is the largest radius that will fit into the available space, the distribution of actual radii of curvature is typically a skewed distribution of radii less than the design radius. This follows since the bend geometry is usually assumed to be circular, when in fact, it is not and cannot be. Figure 5 shows the distribution of actual radii of curvature for a design with a nominal design radius of 125 mils and a forming fixture mandrel radius of 125 mils.

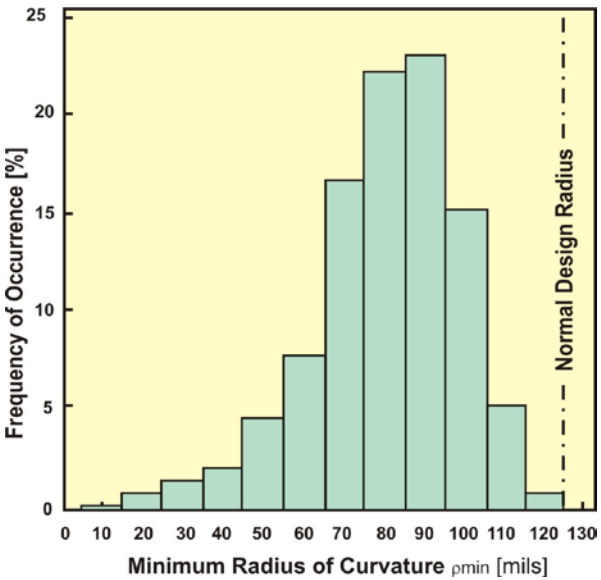

Fig. 5 Observed Minimum Radius of Curvature Distribution for Formed FPW with a Nominal Design Radius of 125 mils.

Superimposed upon the strain distribution resulting from the bend radii variation is another strain distribution due to the deviation in the flex circuit thickness form nominal. Furthermore, some design features can cause localized strain concentrations, which can significantly increase the maximum applied strains.

Distribution of Available Ductility

Ductility, by its very nature, is a statistical materials property since failure of the 'weakest link' causes failure of the whole. Wrought foil will have less of distribution than will plated foil.

Ductility distributions are readily determined using the test methods described in References 1 and 2.

Conductor irregularities, such as nicks, pinholes and etching defects, reduce the available ductility depending on their size as illustrated here:

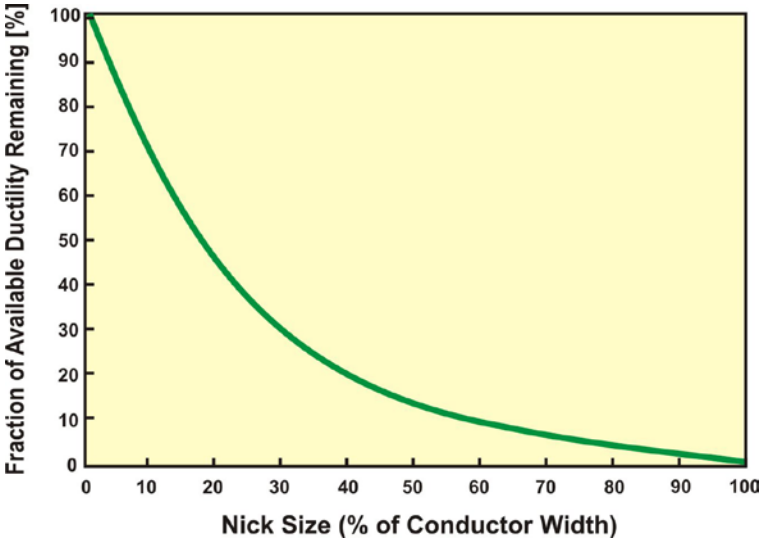

Figure 6. Reduction in Available Ductility Due to Conductor Defects.

Applied Strain Distribution versus Available Ductility Distribution

As discussed earlier, to avoid conductor fractures, the available ductility has to be large enough to satisfy the strain criterion in equation 20. With the distributions of applied strains and available ductility described previously, it is clear that it might be prudent to apply a safety (read uncertainty) factor to avoid failures.

ABOUT THE AUTHORS

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Kevin Durocher joined the General Electric Corporate Research and Development Electronic Systems and Technology Lab in 1984 and has been actively involved in several advanced electronic packaging, semiconductor development, and MEMS programs. He is currently a process development engineer on programs for various GE businesses that utilize thin film passives, optical devices, and high resolution flex circuits. Mr. Durocher has coauthored eight papers in the area of electronic thin films and has a total of 31 issued U.S. patents.

Bill Burdick is an electrical engineer with GE Corporate Research and Development's Electronic Manufacturing and Materials Laboratory where, since 1984, he has contributed to the design and development of advanced electronic packaging technology and led both military and commercial electronic packaging development programs for GE and its customers. Over the past five years, his technical role has expanded to include the definition of and leadership in advanced technology development for high-performance, highly reliable electronic assemblies and systems.

Bill's most recent technical investigations, research, and work have been in the area of high-density electronic packaging and interconnect technology development for medical diagnostic imaging systems including magnetic resonance, digital mammography, computed tomography, and ultrasound. Currently, he is leading a cross-functional engineering team in the development of highly manufacturable and reliable MR receiver coils. As well, he is contributing to the development of electronic packaging solutions for Photovoltaic systems. Prior to his work in MR receiver coil technology development, Bill led and served as principal investigator of a cross-functional GE team that invented, designed, developed, and evaluated electronic packaging and interconnect technology for the detector used in GE's LightSpeed Volume CT imaging system. Over the past 15 years, Bill also contributed to performance, quality, and reliability improvements for electronic packaging for digital X-ray and ultrasound imaging systems.

Bill has published numerous technical articles and has filed over 35 U.S. Patents. He has served on the International Test Conference Session Review and as IMAPS Known Good Die Session Chair.

Chapter 2

Process Challenges and System Applications in Flex

By Kevin M. Durocher and William E. Burdick, GE Research

The ability to produce large-area, fine-pitch flexible interconnect is driven by a number of elements. Those elements are comprised of materials, processes, facilities, equipment, design, and engineering support. The demand for thin, fine-pitch flexible interconnect requires unique considerations that are not possible with traditional printed circuit board (PCB) technologies. Fine feature requirements, over large areas, must have clean process facilities and tooling. Most PCB facilities have limited clean-room capabilities and are often restricted to Class 10,000 in the pattern transfer area. Fine-pitch interconnect processing of structures with less than 100µm pitch requires clean process areas—i.e., Class 100-1,000–to be able to produce interconnect with acceptable yield. The clean-room facilities must also be augmented with tooling, processes, and operator controls for low-defect densities.

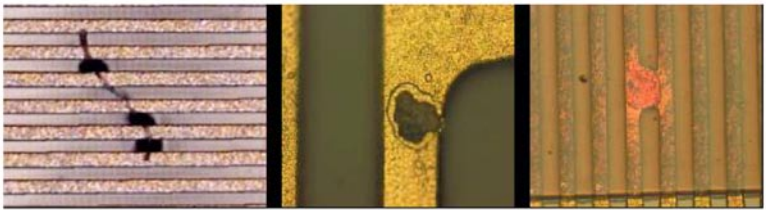


Figure 1: Examples of Flexible Printed Circuit Defects

As shown in Figure 1, defects found on flexible interconnect can include trapped fibers, hole in trace, and conductor-to-conductor shorts. These defects are the result of particles generated from process materials or the process environment, including tooling, operators, and the process facility.

Many manufacturers have designed clean process tools that contain the work and protect it from an unclean facility.

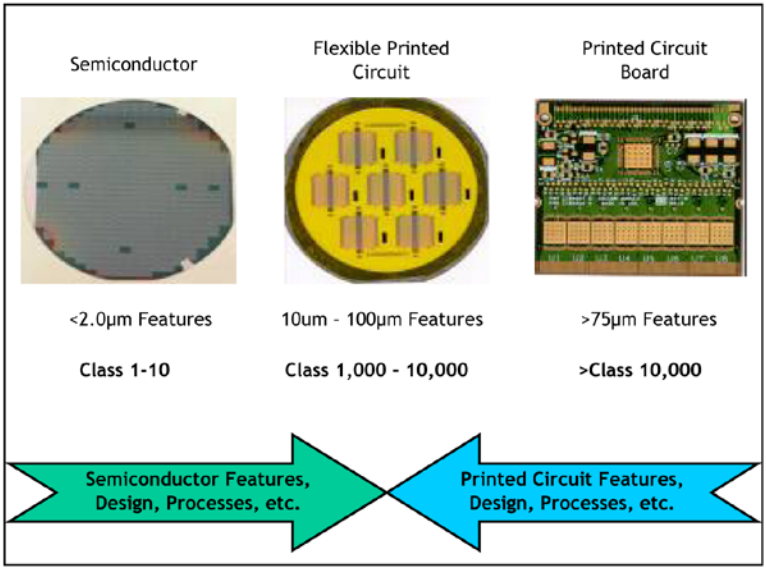


Figure 2: Semiconductor, Flex, and PCB Comparison

As shown in Figure 2, flexible printed circuits, with respect to features and process environments, are at the intersection of their semiconductor and printed circuit board equivalents. Fine-pitch flexible interconnect resides at the intersection; tooling, facilities, and expertise from the semiconductor industry are more closely coupled to fine pitch.

In addition to requiring clean space and controlled defect densities, fine-pitch interconnect involves thin dielectric materials (<50µm) that are difficult to handle. Traditional panel processing requires special handling to prevent material movement through processing. In reel-to-reel or web-based processing it is possible to tension the thin polymer substrate to control dimensional stability of the web. Temporary bonding of thin substrate materials has been developed by a number of companies, but the cost of generating the temporary substrate and the size limitations can be expensive while the release process utilized can be difficult to control and reproduce. Controlling substrate material movement during processing is critical for multilayer metal processing where registration is a key factor. The ability to register microvias to metal landing pads and the accompanying cover pads can limit manufacturing capabilities. Via pad size drives most vendor capabilities and, ultimately, dictates the routing densities that can be realized between the pads or restrictions.

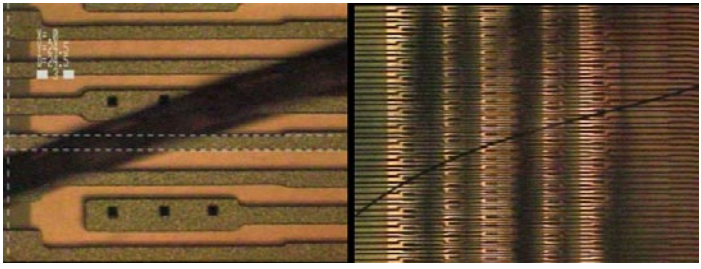


Figure 3: Defects in Two-Metal-Layer Flex

A flex circuit with trace line widths of 25µm, 25µm diameter vias, and a core of 25µm-thick polyimide is shown in Figure 3. On the surface of that flex, a ~75µm-diameter human hair is visible. The presence of foreign objects of this size and smaller illustrates the need for clean processing facilities and tools and proper garmenting and particle controls.

GE Research has developed a method to tension thin-core polymer substrate materials and process them with conventional wafer-based semiconductor tools. This method allows for fine-pitch feature processing and enables the manufacturing source to process the material as they would traditional silicon-based semiconductors. Maintaining a consistent tension of the thin substrate material through processing allows for improved

layer-to-layer registration, the ability to print and etch smaller features, and the use of advanced tooling. Some of the advanced tooling used at GE includes centrifuge, spin coaters, UV steppers, high-pressure scrub, metal sputter tools, and assembly equipment. The ability to pattern fine pitch and control layer-to-layer registration makes it possible to achieve fine pitch in multilayer constructions (6-8 metal layers).

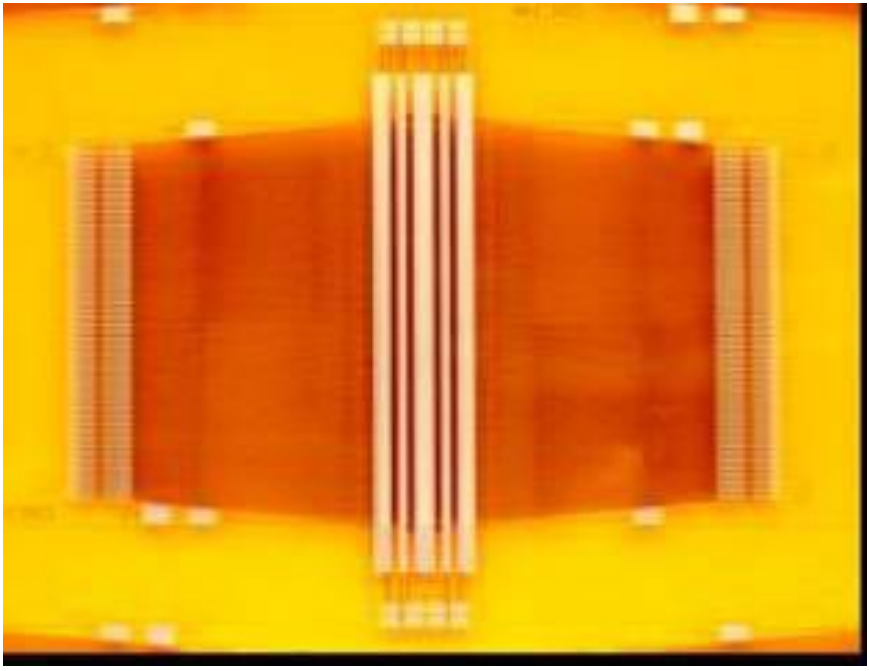


Figure 4: Ultrasound Flex Circuit

The use of flexible printed circuits has become prevalent in diagnostic imaging systems; in particular, the flex shown in Figure 4 is utilized in an ultrasound probe. The circuit shown has features of 4µm-thick copper, 25µm-thick polyimide, conductor pitch of 50µm, and 25µm-diameter laser-drilled vias.

Test Element Groups (TEGs) or process monitor coupons are critical components in the fabrication of reliable, high-quality flexible interconnect. TEGs are routinely used for standard process control (SPC), certification of compliance (COC), and reliability or qualification testing. A number of standards can be used for interconnect compliance, such as IPC, JDEC,

ASTM, etc. TEGs can be utilized as in-process monitors, for post-fabrication validation, and as reliability screening coupons.

In-process monitoring examples include resistivity or Kelvin test structures to insure metal thickness after plating operations. Four-point probe resistivity measurements can be performed, prior to pattern and etch operations, to measure uniformity of metal deposits. Other in-process coupon examples include lithographic resolution structures (critical dimension measurement vehicles), impedance coupons, elongation/ductility coupons, flexural endurance coupons, and via interconnect strings.

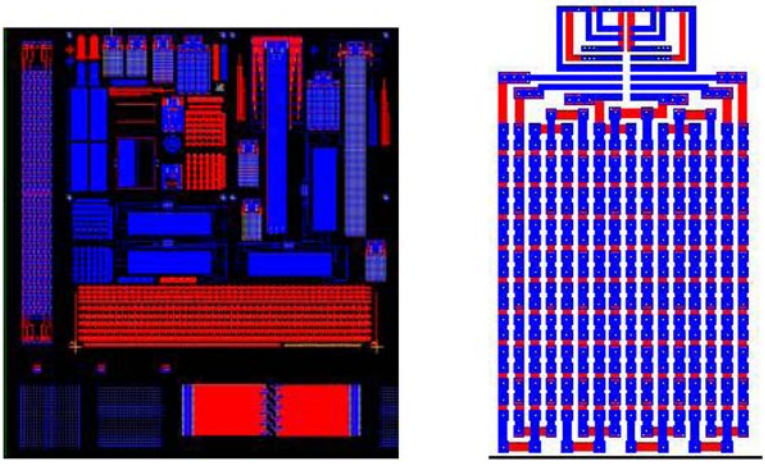


Figure 5: Test Element Group Design, Via String Coupon

Via string coupons allow the manufacturer to test an array of vias (200-500) on the device panel for a measure of via integrity during and after circuit fabrication. Via integrity can be measured by passing current through the via structure to insure that sidewall metal coverage is adequate for the circuit operation environment. The via string can combine all metal layers and metal layer pairs to aid in troubleshooting process fabrication issues (via drilling, via cleaning, via metallization). This coupon allows for circuit troubleshooting and, if performed in-process, can save process time and costs by identifying issues early in a process cycle. Specific via string designs allow for accurate measurements of metal contact resistance.

Examples of post-fabrication test coupons include strip line structures

for high-frequency calibration, assembly monitors (reflow/float coupons), elongation or flexural endurance test structures, and via strings. Many coupon designs are available for reliability tests, such as: via string monitors for thermal cycle, isolation resistance tests, flexure test structures, solder float coupons, and electro-migration testing.

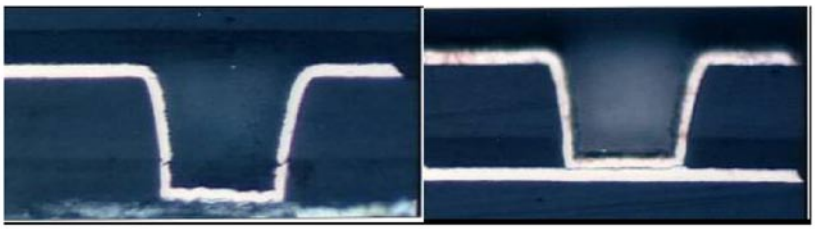


Figure 6a: Via Defect

Figure 6b: Via Defect

Common via defects are shown in Figures 6a and 6b. In the former, a crack in the via sidewall resulted from stress during laser processing. In the latter, a layer of contaminant is present, at the bottom of the via, due to incomplete laser plasma processing.

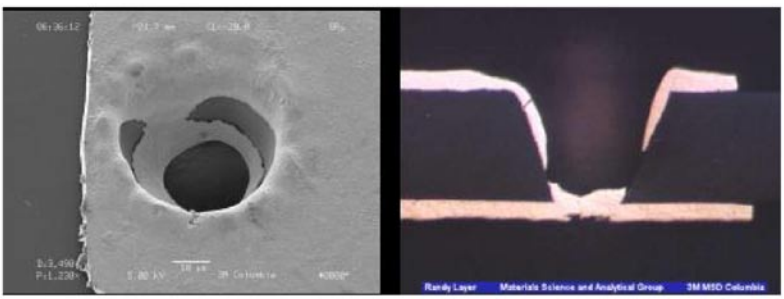


Figure 7: SEM and Cross-sectional Images of Incomplete Via Plating

Another common via defect is shown in Figure 7. This defect resulted from the stress generated by passing current through interconnects. The via defect was attributed to incomplete plating of the via during copper electro-plating.

In-situ via process monitoring allows for testing of via integrity after patterning of metal pairs in a traditional sequential interconnect buildup process. Via test structures can be stressed by passing current through the string to identify incomplete via plating and metal sidewall coverage issues

(as shown in figure 7). The images shown in Figures 6a, 6b, and 7 illustrate multiple via process issues (cracking of interconnect at polyimide/adhesive joint, incomplete via drilling/cleaning, and incomplete metal sidewall coverage in the via barrel). The design of the test vehicle or TEG structure also allows for automated probing of flexible interconnect, whether it be resistivity mapping or DC resistance measurements.

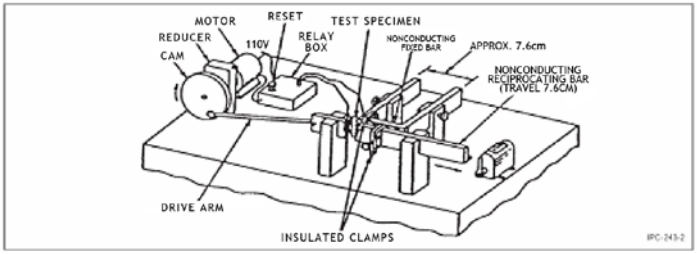


Figure 8: Flexural Endurance Tester per IPC

The test standard 2.4.3 from IPC TM-650 is a method to measure flexural endurance of etched flexible printed wiring circuit patterns. The standard describes the tooling, test coupon, and method for testing. Resistivity is monitored in this test, as changes in the material due to cracks, and delamination due to material flexure, will result in the loss of electrical connectivity.

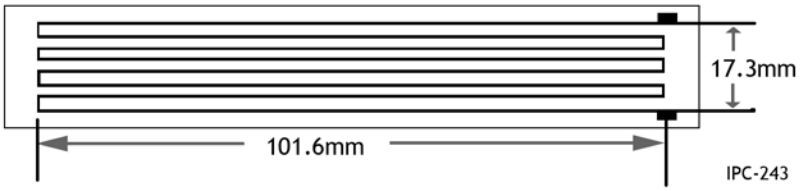


Figure 9: Flexural Endurance Test Pattern

GE Research has developed a version of the flexural endurance test based on the IPC standard. Added features to the tester include:

- **Automated resistivity monitor with threshold**
- **Multiple circuit load (4–up)**
- **Pogo-pin quick connection**
- **Variable-speed motor**
- **Fine-pitch pattern (25mm traces)**
- **Automated data logger**

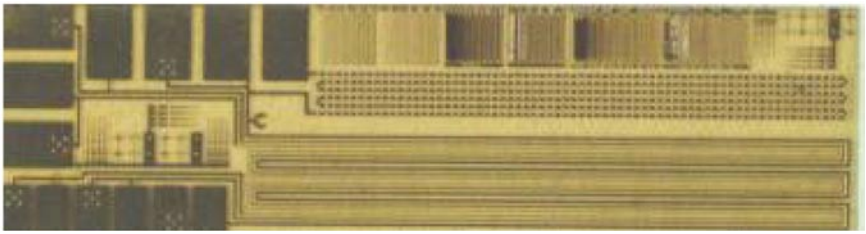


Figure 10: GE Fine-Pitch Flexural Endurance Coupon (array of trace pitch, 1-metal-layer vs. 2-metal-layer design)

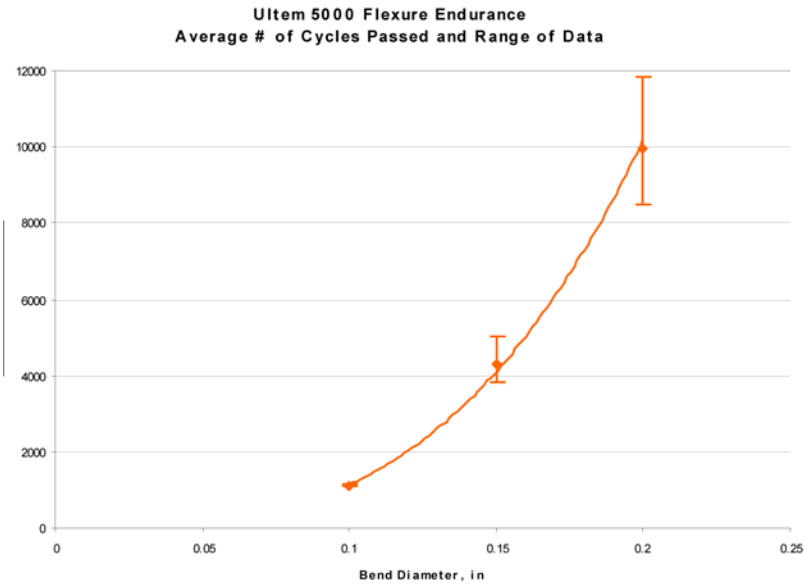


Figure 11: Example of Data Output from GE Research Flexural Endurance Tester (Ultem polyimide film characterization)

GE Research has also developed a number of TEG monitor cells that are assembled as blocks in a library for use on multiple platforms (RF, DC, analog, PWB, thin core, silicon, etc). The TEG blocks can be assembled in the field area of the panel to aid in process monitoring, second-level assembly, and reliability screening. GE Research has also developed specific tooling to aid in the characterization of thin-core flexible interconnect materials. Examples of the tools include elongation test stands, flexural endurance systems, and automated electrical testing platforms. The TEG monitors are regularly used in healthcare, military, and commercial flex-circuit fabrication. These monitors are often used as screening tools for vendor capability demonstrations.

Electrical performance, and the corresponding electrical functional testing, is also a critical aspect in flexible printed circuits. Procedures for functional testing are application–specific, but generally, basic function including impedance characterization is tested. Often, users overlook characterization of surface isolation resistance because its adverse impact on electrical performance in low-signal amplitude (microvolts, microamps) applications is not considered or because of the difficulties in obtaining valid data at low-signal amplitudes, especially in the environments required for isolation resistance testing.

Leakage currents, due to the presence of ions on the surface or within the layers of a flex circuit, occur in the presence of a voltage source and moisture. Most flex (and PCB) circuit manufacturers perform surface isolation resistance testing at the circuit level; i.e., total ion content is extracted from the entire circuit. This test method assumes a uniform distribution of ions; accordingly, it can lead to undetected risk for leakage currents, due to undetected high, local concentrations of surface or embedded ions. For example, given a total ion content limit of $5\mu g/in_2$, a 2" x 2" flex circuit would pass surface isolation resistance testing if the total ion content measured was 20µg. Clearly, if that 20µg was a single piece of sodium located in a very small area on the flex circuit, its potential to cause leakage current would be significantly greater than if that same 20µg of sodium was configured as a uniform layer on the entire flex circuit surface. The conclusion: Surface isolation resistance testing does not provide sufficient resolution to identify potential risk of leakage currents in flex circuits.

To understand the risk of leakage current and its adverse impact on system function, it is necessary to perform leakage current testing. In its simplest form, the leakage current test would be structured to allow for testing of the flex after twenty-four hours' exposure to ambient environment. The flex would then be placed in a humidity chamber (100%RH) for twenty-four hours. The flex would be removed, and leakage current testing would be repeated; due to the potential for moisture evaporation once outside the humidity chamber, leakage testing of the flex circuit should be completed in one hour, in ambient environment. Ideally, testing should take place in the humidity chamber, but the equipment, facility, and process challenges of in-situ testing may require non-ideal test methods.

Unfortunately, there is no industry standard or generic test limit for leakage current in flex circuits. The user must analyze the data to characterize and compare leakage current values for both ambient and high-humidity conditions with the application-and-use environment. If individual or specific lots of flex circuits show deviation from the norm, then those circuits are suspect and should be subjected to further testing and analysis. That analysis can include destructive testing, e.g., sectioning suspect circuits and subjecting those sections to ion chromatography to measure ion content locally.

System-Based Flex Applications

The demand for thin, lightweight, high-density interconnect continues unabated. Similarly, application strategies for satisfying the ever-changing and ever-growing demand for high-density interconnect continue to change. Since their inception, flexible printed circuits have evolved into a cornerstone technology of high-density interconnect. Flex has become a fundamental interconnect technology, from its first application in tape automated bonding (TAB) and corresponding simple, point-to-point configurations to the fine-pitch, multilayer designs that are commonplace in today's mobile electronic products. However, the approaches in using flex to satisfy the demands of high-performance, highly reliable systems with high volumetric density I/O are still evolving.

Following a familiar path of technology development, the use of flex has changed from first-level to second-level interconnect applications; more recently, the role of flex has been expanded to include system-level interconnect. At each point in its changing role in applications, flex technology has been modified to meet the application demands. For example, to meet the demands of die-to-die interconnect, the single-layer, via-less, point-to-point circuits found in 1970s TAB packaging sprouted additional layers. The transformation to multilayer interconnect required the development of new features such as vias for interconnecting layers; new materials such as adhesives to bond dielectric and conductor layers; and new processes and equipment for manufacturing the resulting incarnation of flexible printed circuits. As device I/O increased beyond the capabilities of existing multilayer technology, the trace and space features of flex were

reduced. Over the past twenty years, feature sizes in flex such as conductor geometry, via diameter, dielectric thickness, etc., have been improved significantly. These improvements positioned flex for its now-dominant position in portable consumer, display, and medical electronics interconnect applications.

As witnessed over the past ten years, the reduction in interconnect feature size has slowed. At the same time, device I/O counts have increased as semiconductor features have decreased, according to Moore's Law. This disparity in interconnect and semiconductor feature size has created an interconnect "brick wall" that demonstrates the need for advancing the capabilities of interconnect systems. As shown in Figure 12, semiconductor device minimum feature size (and rate of decrease in feature size) far exceeds the equivalent in flex and PCB technologies. The corresponding gap in interconnect capability has and will limit advances in semiconductor applications until advances in volumetric I/O density, form factor, weight, flexibility, etc., are implemented in flex. In the meantime, flex must be utilized as an integral part of the interconnect system.

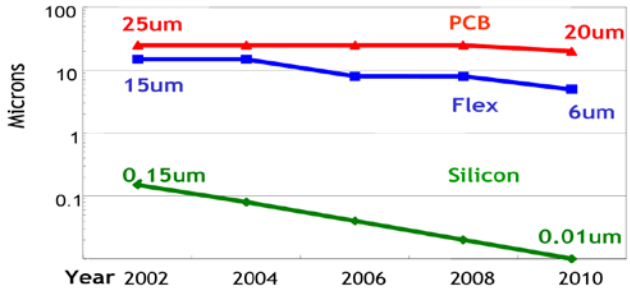


Figure 12: Silicon, Flex and PCB Minimum Feature Comparison

Although the complexity of electronic systems has increased over the past ten years, the challenges in interconnect systems have been minimized due to the functional partitioning of electronic systems into key subsystems: encoding/decoding, processing, display, and power. Typically, flex is utilized for interconnection within a subsystem as well as for system interconnect.

Figure 13: Apple MacBook Air (Image courtesy of iFixit)

Figure 13: Apple MacBook Air (Image courtesy of iFixit)

As shown in Figure 13, laptop computers include examples of these types of interconnect.

Figure 14: 4 x 1Mbit DRAM MCM

As well, flex is utilized in advanced packaging products such as the thin memory module shown in Figure 14 and the 3D Multichip Module shown in Figure 15. (Note that the four-device memory module has the same dimensions, including thickness, as a postage stamp.)

Further, these products show that there exists a hierarchy of packaging and interconnect technologies to satisfy electronic system requirements. In particular, because there is no need for flexure and there is no significant disadvantage in weight, the major interconnect technology in today's portable electronics systems is still PCB. Flex is relied upon to satisfy the need for thin, conformal, and flexible interconnect as well as to serve as the substrate of choice for attaching many (if not most) flip-chip and chip-scale packages. Flex and PCB have similar performance and reliability; cost can

differ significantly, depending on the application. However, as every early-technology adopter knows, higher costs are expected and well tolerated at the early stage in new and/or advanced product introduction.

As electronics miniaturization has continued, the use of flex in electronics systems has flourished. Rigid substrates, common in the first multichip module technologies, have been replaced with flexible printed circuits and either integrated or chip-on-flex.

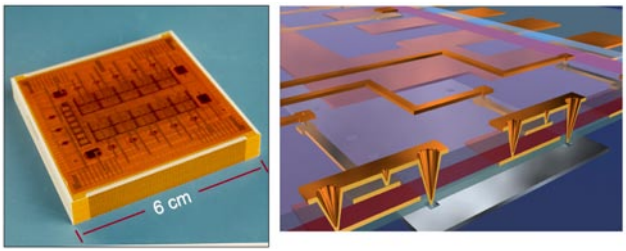


Figure 15: GE High-Density Interconnect

Likewise, the use of flex as a substrate for electronic systems utilizing chip-sized and chip-scale packages has increased dramatically. However, during the period that flex has supplanted PCB as a substrate and increased its share as an interconnect technology, direct chip attach has been developed to circumvent the lack of high-density interconnect. For example, the earliest displays utilized in electronic systems included display electronics mounted on PCBs. These PCBs were attached to the display by means of a standard connector. Over time, PCBs with standard connectors were replaced by flexible cables, constructed using one to a few metal and dielectric layers, with standard and novel connectors. As the size of displays shrank to meet the demands of portable electronics, chip-on-glass technology was perfected. Directly attaching the electronics to the display I/O reduced the system I/O demands to a quantity compatible with flex capability. This is a key point to consider in the application of flexible interconnect.

The primary challenge in today's flex technology is its I/O capability, as determined by minimum feature sizes. For example, in single-metal-layer (1ML) flex, trace and space widths as small as 10-microns have been produced using commercial processes, materials, etc. Even finer features have been produced, as shown in Figure 16, a transfer lithography process comprised of 4-micron-pitch (one-micron trace, three-micron space), flex configuration. Similarly, feature sizes in two-metal-layer (2ML) flex, the lion's share of commercial flex production, have been reduced to twenty-five microns. But minimum trace and space geometries do not tell the entire

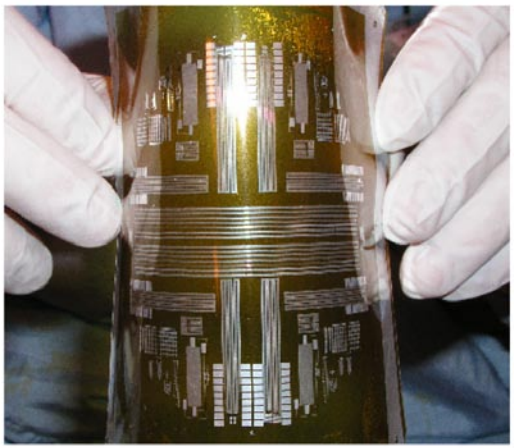


Figure 116: 4µm-Pitch Flexible Printed Circuit (Transfer Lithography)

story of I/O capability for flexible printed circuits.

There are many questions to pose when assessing the capabilities of potential flex suppliers; perhaps the most critical is, what are the supplier's minimum via land pad dimensions? The dimensions of the via land pad highlight the alignment capability of the flex supplier's processes and dictate the minimum pitch of the flex interconnect. Consequently, not all 2ML flexes with twenty-five micron features have equal interconnect density. Moreover, even though feature sizes are decreasing, I/O capability in flex is not increasing or, at a minimum, is not increasing at the same rate. Accordingly, second-level assembly continues to move closer and closer to the device.

As witnessed in chip-sized and chip-scale packages, by adapting an existing technology to a novel configuration, the unmet needs for very fine pitch, high volumetric I/O packages effected the reduction in use or elimination of standard electronic packages. Plastic encapsulated lead frames and multilayer ceramic packages have been replaced by plastic encapsulated flex interconnected bare die or, in many cases, by bare die. Similarly, the increasing use of direct chip attach results, in part, from the inability of flex interconnect to meet the constant demand for higher pixel counts in displays. In this case, package interconnect by means of wirebonds with millimeters of length and flex interconnect of tens to hundreds of millimeters in length has been replaced by stud bumps (of tens of microns in diameter, produced using the same wirebonding equipment and materials) and the complete elimination of the flex interconnect. Electronic packaging technologists and applications engineers are currently developing similar system-based solutions and applications by revisions, enhancements, etc., to existing interconnect technologies in order to meet the never-ending

demand for greater interconnect density and capability. However, even though its features continue to lag behind those of semiconductors, flex has and always will play a significant role in the optimization of system design.

To explore the shift from component-based to system-based design and its impact on flex technology and applications, it is useful to examine the recent development of a high-performance X-ray detector for GE Health Care's LightSpeed VCT CT system, a state-of-the-art computed tomography system whose image quality is dependent on many subsystems, especially the X-ray detector.

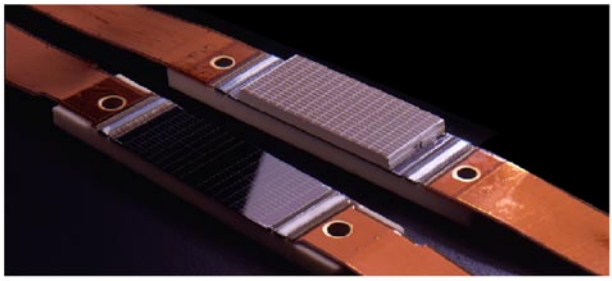


Figure 17: 4-Slice CT Detector Modules

As shown in Figure 17, CT X-ray detectors have been fabricated using many of the technologies and processes common to hybrid circuits, such as ceramic substrates, wirebonds, etc. The detector (16 x 16 photodiode array) and flex interconnect are attached to the ceramic substrate and the photodiode array interconnected to the flex by wirebonds. This approach, including flex circuits, satisfied detector designs from the inception of CT systems. However, manufacturers of CT systems, in their response to constant market demands for both larger detector array size (to capture large-image volumes per imaging sequence) and finer resolution (by decreasing the size of pixels while increasing the quantity of pixels) soon became limited by the package configuration and interconnect technology. Throughout the development of CT systems, designers had simply added signal layers and/or decreased the feature sizes of the flex interconnect to meet the demands for higher image resolution of patient coverage. Designers at GE realized that the interconnect demands of CT detectors were about to overtake, the capabilities of commercial flex interconnect. As a result, a significant development effort was begun to create an ultra-high-density flexible interconnect to take the place of the existing commercially-available flex circuits that were a mainstay of CT detector systems. After much brainstorming and development of conceptual

designs, it was determined that this advanced commercial flex technology would not be available until long after the desired product launch date for GE's next CT system.

Given the constraints of existing commercially-available flex technology, GE's CT detector design team reassessed the interconnect requirements for their next-generation detector. As was customary for each new product introduction, the new detector had to provide twice as many pixels as its predecessor. And, to realize the "Holy Grail" of imaging the heart in a single breath hold, the imaging area had to double. (Prior to LightSpeed VCT, imaging area increased but never by anything as great as a factor of two.) It was quickly realized that existing flex technology could satisfy the product demands, but only if the diode I/O configuration was changed to an area array. By transforming the I/O configuration from the traditional linear array to an area array, the need for ultra-high-density (four metal layers with a less than 50-micron pitch) flex vanished. GE Research's electronic packaging and IC designers teamed to develop a revolutionary new detector design, as shown in Figure 18, comprised of a photodiode array with backside I/O, in an area array configuration, and multiple flexes (six metal layers with 400-micron pitch), and analog-to-digital converters located in very close proximity to the detector. This approach eliminated the interconnect choke point that resulted from escaping diode signals at the periphery of the diode package. Consequently, the need for more complex and costly interconnect was eliminated. However, the total amount of flex circuit area increased, but not at a significant cost to the detector system. The GE CT detector team had not only found a solution to their product development challenges, but they had resolved the challenge of commercial availability of fine-featured flex by transforming the detector configuration through reliance on semiconductor features. As described previously, the improvement in feature capabilities

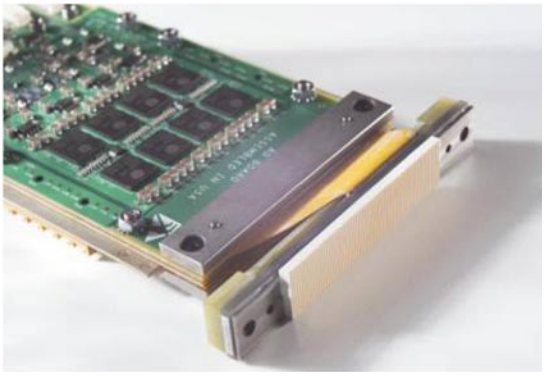


Figure 18: GE LightSpeed VCT Detector Module

in semiconductors far outpaces the equivalent in flexible printed circuits. Optimal packaging solutions are more readily available when all system components are included in a system-level packaging and interconnect design approach. Those who desire to implement flexible interconnect solutions in existing and future electronics packaging applications must embrace these principles.

Another example worthy of study is a novel solution developed for an RF Low Noise Amplifier (LNA). As shown in Figure 19, a conventional PCB with through-hole and SMT technology was used for packaging a very-high-performance (0.5db noise figure) low noise amplifier for an MR imaging application. In this application, rejection of common mode currents is required. Accordingly, as shown in Figure 20, a balun is needed. As in all diagnostic imaging systems, there is an insatiable demand for greater pixel quantities and densities. With the corresponding increase in volumetric I/O density, due to fixed package volumes, the electronic systems (including packaging and interconnect) must decrease in size. The designers were asked to reduce the size of the existing LNA by at least a factor of four, in area. However, the designers recognized that reducing the area by a factor of four would satisfy only the next product; future products would require area reduction of 10X or more. Accordingly, to avoid a series of minor changes, a major design change was required.

Figure 19: LNA

Figure 20: Balun

Reducing component size and optimization of circuit size were considered and rejected because that combination of design changes would satisfy only the near-term goal of a 4X area reduction. Replacing the PCB with a multilayer fine-pitch flex would have effected another 1X improvement in area reduction, albeit at an overall cost increase. It quickly became clear that a redesign of the LNA alone was not going to satisfy the long-term goal of a 10X reduction in area.

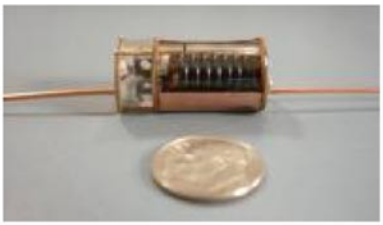


Figure 21: LNA-Balun

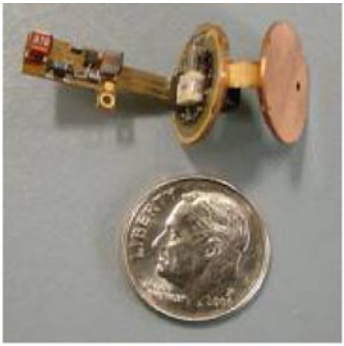


Figure 22: LNA-Balun Flex Assembly

As shown in Figure 21, a novel system-based solution, LNA-Balun, was developed. As shown in Figure 22, a folded, 2ML flex with 50-micron features was used to replace the single-sided four-layer PCB. Through-hole components were eliminated. And, the flex was designed to fit inside the balun. By considering the LNA-balun system as the design space and relying on commercially available materials, technologies, assembly processes, etc., the designers were able to eliminate the entire volume of the LNA, as used in the existing product. Further, designers utilized flex where its salient features were applicable, acting on the principle that there is no technology that can or should be applied universally.

Flex Integration

To achieve an optimal interconnect and packaging design, it is important to utilize flex only when flex best satisfies application and other needs. Flex is a good choice when the primary need is for flexible, conformal, thin, lightweight, etc. Flex is also a good choice for applications requiring comparatively high I/O density, low cost, or performance advantages that cannot be achieved in PCB constructions. Flex can be utilized in many applications other than the aforementioned “good choices”; however, the user is strongly encouraged to consider cables, PCB, and other suitable interconnect technologies or else risk unnecessary design complexity, reliability risk, system connector challenges, higher cost, etc. As in conventional electrical design, interconnect must be partitioned according to product specifications including performance, reliability, cost, et al.

Interconnect partitioning, intentional or otherwise, can be found in the hierarchy of interconnects that is in almost any electronic system. For example, although personal computers include state-of-the-art semiconductors and their corresponding nanometer feature sizes, the power for those semiconductors is supplied through cables that are constructed using 18-gauge or larger conductors. Likewise, packaging designers need to partition the interconnect chain to satisfy system specifications, requirements, etc., using "just enough technology."

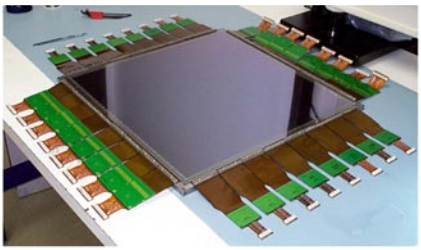


Figure 23: GE Digital X-Ray Detector Assembly

As shown in Figure 23, a digital X-ray detector is comprised of an amorphous silicon detector panel and digital amplification and processing electronics. The pitch of the electronic devices that detect the converted X-ray signal can be as small as 100 microns. Their corresponding I/O are configured in a 150-micron-pitch linear array, along each of the four edges of the panel. The choice in detector panel I/O pitch is limited by the I/O capability of high-performance, highly reliable, flexible printed circuits. Flex was chosen because it is flexible, a requirement for packaging a digital X-ray detector in the same form factor as the film canister used in conventional X-ray imaging, and for ease of manufacturing; in particular, the ease with which the flex can be connected to the 150-micron-pitch detector panel I/O using anisotropic conductive film (ACF) was a significant factor in the use of flex interconnect.

The flex that interconnects the detector panel and signal processing electronics is a 2ML, 150-micron pitch design. One end of the flex is bonded to the panel; the other end is bonded, using ACF, to a multilayer PCB. Multiple ASICs (in bare die form) are attached, in a linear array, on the PCB; the ASICs are wirebonded to the PCB. The ASICs amplify and convert the analog signals produced by the detector panel and route those signals through a connector to a second flexible printed circuit that connects to the system electronics. The second flex, because of multiplexing of the digitized signals, requires fewer signal conductors; thus, it is a low-density 2ML flex (signal plus shield layer).

The next logical step in packaging optimization for this type of electronic system would be the integration of the ASICs and ancillary electronics into the flex. This integration step, if done properly, would replace the PCB with flex, reduce the number of interconnects, and reduce detector panel manufacturing steps, without increasing the cost of the flex-PCB-flex system, as above.

Printed Electronics

Interconnect technology is expanding to include printed systems. As detailed in the iNEMI Organic and Printed Electronics Roadmap, shown in Figure 24, there is a bounty of printed electronics technologies, such as "drop on demand," Xerography, micropen, et al. It is not within the scope of this chapter to detail the principles, advantages, benefits, etc., of each technology; rather, it's important for electronic packaging and interconnect designers to understand the salient features of printed electronics and digital fabrication technologies as well as the similarities and differences among conventional printed circuit technologies and processes.

		Lateral Resolution (µm)	Average Dry Thickness (µm)	Benefits	Critical Processing Parameters
Contact	Gravure	>15	0.8 – 8.0	• Hardware and functional inks are commercially available • Low-cost, high speed parallel processing • Demonstrated repeatability	• Particle size and distribution in ink • Solvent evaporation rate • Rheological properties • Substrate surface energy • Imprint load • Printing speed
	Flexo	>20	0.8 – 2.5		
	Offset	>15	0.5 – 2.0		
Non-Contact	Inkjet	>50	0.3 – 10.0	• CAD data driven: "on-the-fly," maskless changes; adaptable to error • Conformal and 3D printing • Multiple materials	• Particle size in ink • Solvent compatibility • Rheological properties • Substrate • Jetting distance • Environment
	Micro Dispensing (SUBSTRATE)	>50	5.0 – 100.0		

GE Proprietary

Figure 24: Comparison of Printed Circuit Methods

Digital fabrication can be viewed as the creation of electro-optical-mechanical-thermal systems by means of either parallel or sequential additive processes, as controlled by a digital device. As with any technology,

the designer should consider and take advantage of the technology's features before applying it. In the case of digital fabrication, those features include adaptive, additive, roll-to-roll processes and the ability to fabricate on curved, conformal, curvilinear surfaces. An example of a circuit printed on a curved surface is shown in Figure 25.

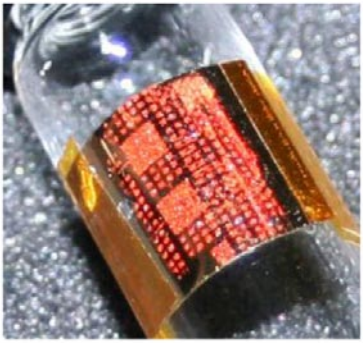


Figure 25: Printed Circuit on Curved Surface (Image courtesy of Alejandro Briseno/Stanford University)

Most often, digital fabrication is accomplished in a roll-to-roll process, but panel-based digital fabrication is also possible. The revolutionary aspect of digital fabrication, as compared to conventional printed circuits, is the ability to simultaneously create electronic and/or optical devices, electrical interconnects, mechanical structures, and thermal management systems. For example, using conventional technology and processes, a television remote control is produced by packaging and assembling tens to hundreds of electronic devices onto PCBs and subsequently assembling the PCBs, interconnect, LED, touchpad, etc., within a plastic housing. Digital fabrication would allow the entire system to be fabricated, layer-by-layer, in a fashion similar to that of stereolithography apparatus (SLA). Applying digital fabrication requires a transformation in thinking by electronic system designers: digital fabrication provides for the 2D and 3D design and fabrication of systems that are not limited to electrical interconnect and passive devices.

In digital fabrication, materials with the necessary electrical, mechanical, thermal, and optical properties to form the desired devices, systems, etc., are deposited onto a substrate. Polymer and plastic are the most common substrate materials, due to their compatibility with low-cost, high-throughput processing. However, rigid substrates can be used as well. The materials used in forming electronic devices and interconnect are, typically, conductive inks and dielectrics. Any material, however, that can be dispensed by the dispensing system ("print head" plus material control) can be used. The materials used in forming mechanical and thermal structures, likewise, are defined by the application and limited by the capabilities of the "print head"

and material control system. To date, biological, organic, optical, and many types of functional materials have been printed.

Given that devices and structures are being "built-up," layer-by-layer, there are key differences in the resulting device and feature attributes. For example, vias can be formed as filled or partially filled and can be conductive and/or nonconductive, electrically and/or thermally. Unlike conventional printed circuit technology and processes, digital fabrication can be used to produce vias of any geometry. Similarly, individual traces can be of any geometry and can be produced to effect sidewalls with attributes to support application needs. Conductors produced using conventional printed circuit technology have sidewalls that are tapered or orthogonal. Digital fabrication could be used to produce conductors with irregular sidewall features, as related to specific performance or mechanical applications. Furthermore, in digital fabrication, mechanical, thermal, and other features could be included in the construction of conductors.

Currently, the primary applications for printed electronics are OLEDs, as shown in Figure 26, and RFID. Photovoltaics are also an application for printed electronics, but this field is immature compared to OLEDs and RFID.

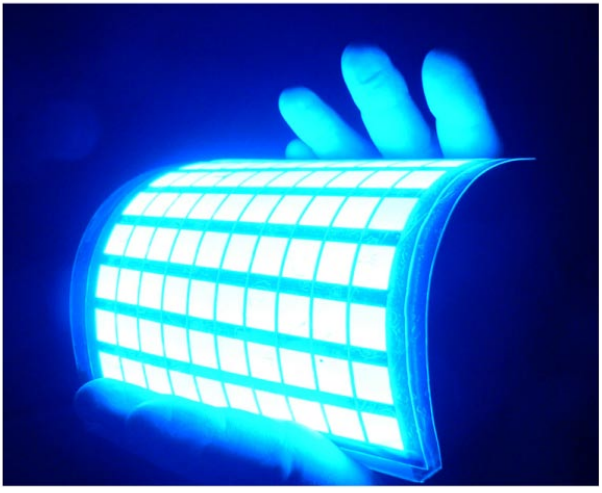


Figure 26: Printed OLED Array

Transistors that operate in the tens of megahertz have been printed; recently, researchers at the University of Illinois (Rogers et al.) announced that they had printed silicon circuits on plastic that operate at switching speeds of 500 megahertz. As shown in Figure 27, there are demands for printed, stable, high-speed digital and high-fidelity analog devices; however, materials to produce devices other than low-speed, simple ones are lacking. Accordingly, other than novel devices produced in laboratories, printed electronics have not been used

to produce the basic "building-block" high-speed digital or analog devices (e.g., FPGAs and operational amplifiers, respectively). These components are fundamental to systems comprised of analog devices.

Similarly, with respect to printing electrical interconnects, digital fabrication is in its infancy. Plated vias, a staple of the layer-to-layer interconnect found in conventional printed circuit technology, are nonexistent or crudely implemented in digital fabrication. Moreover, the electrical performance and reliability of vias and conductors are either not known or, with respect to characterization, known incompletely. It will be interesting to observe if and when the creation and maintenance of electronic and interconnect standards are realized.

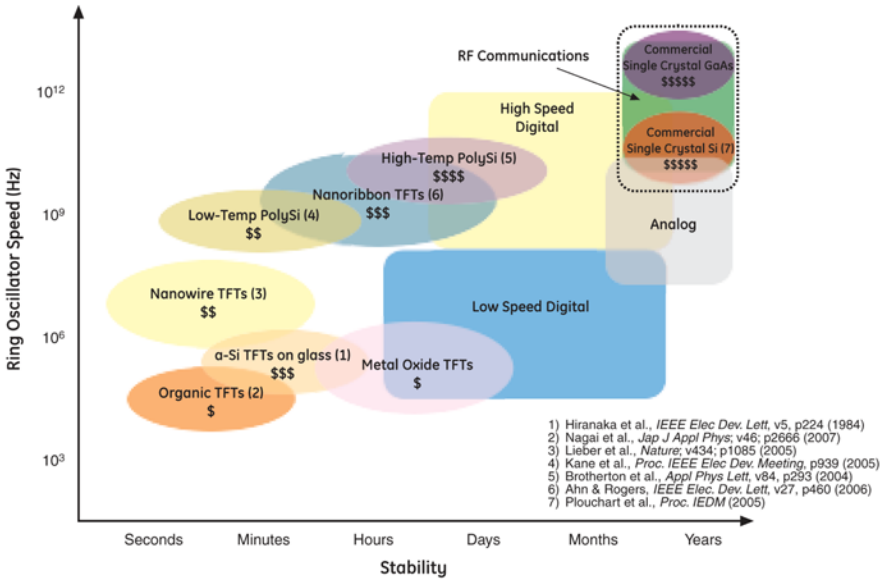


Figure 27: Device Speed and Stability Specifications

ABOUT THE AUTHOR

Bob Willis currently operates a training and consultancy business based in England. He is the Technical Manager of the SMART Group and a member of the technical committee. Although a specialist for companies implementing Surface Mount Technology, Bob provides training and consultancy in most areas of electronic manufacture, in the last 10 years focusing on lead-free manufacture, which has earned him the SOLDERTEC/Tin Technology Global Lead-Free Award for his contribution to the industry. He has worked with the GEC Technical Directorate as Surface Mount Coordinator for both Marconi and GEC; prior to that, he was Senior Process Control Engineer with Marconi Communication Systems, where he had worked since his apprenticeship. Following his time with GEC, he became Technical Director of an electronics contract manufacturing company, where he formed a successful training and consultancy division.

Over the past few years, Bob has travelled in the United States, Japan, China, New Zealand, Australia, South Africa and the Far East looking at areas of electronics consulting and lecturing on electronic assembly. He was presented with the Paul Eisler award by the IMF (Institute of Metal Finishing) for the best technical paper during their technical programmes.

Bob was Chairman of the SMART Group, European Surface Mount Trade Association, from 1990-94 and has been elected Honorary President for life. He currently holds the position of SMART Group Technical Manager and also works on BSI Standards Working Parties. He is a Fellow of the Institute of Circuit Technology, an NVQ Assessor, Member of the Institute of Quality Assurance and Society of Environmental Test Engineers. Bob currently writes regular features for AMT Ireland, Asian Electronics Engineer and Circuits Assembly (the US magazine).

Chapter 3

Flexible Circuit Assembly

(A rework of Chapter 7) by Bob Willis

INTRODUCTION

Flexible circuits offer some unique challenges to the assembly process. The assembly materials and processes for populating and interconnecting components to a flexible circuit range are essentially identical to those used for standard rigid boards, but there are some twists required, as will be shown. The assembly processes range from very simple methods, such as manual component insertion and hand soldering (which requires little or no fixturing), to fully automated methods, which normally require specially developed, design-specific and dedicated fixtures.

How, then, does one choose an assembly process and method for flex circuits? To begin appropriately, it is necessary to consider a number of important factors: What is the flex circuit base material? What types of

components will be used? How many assemblies will be built? These and other important questions must be addressed before one can adequately make the proper decisions regarding assembly. These seemingly simple matters can greatly influence the assembly choice. For example, it is commonly assumed that polyester circuits cannot be used in applications where soldering is required. The reason for this assumption is that polyester films have a low melt point and will be grossly distorted by the tin-lead soldering process. However, when properly fixtured, soldering can be used for joining components to polyester. A number of major OEMs have been doing just that for many years. They have developed methods that provide proper shielding of the body of the polyester circuit in process. The distortion of the material can be localized to areas adjacent to the point of connection. With the advent of the well-meant but misguided legislation mandating the use of lead-free solders, there will be significant challenges ahead, as lead-free solders have a roughly 30-40ºC higher melting temperature than traditional tin-lead solders. Sadly, it appears that traditional tin-lead solders are actually more environmentally friendly, so the law does double damage. One alternative is to use lower-temperature solders, or conductive adhesives can also be employed. The important thing is that manufacturers not limit themselves in their thinking and that they be open to alternative solutions. Following is a brief review of the key elements of flex circuit assembly.

Assembly Overview

As was indicated earlier, the assembly process for flex circuits follows a path similar to rigid boards but with some important points of departure. It is, thus, of value to understand the traditional flow of assembly as a point of common reference.

There are but a few simple elements associated with and required for assembly: interconnecting substrates (e.g., PCBs or flex circuits), components (e.g., ICs, discrete components and connectors) and a method for joining them. The challenge comes in bringing these elements together in a cost-effective and highly reliable way. This normally means that a high degree of automation and capital expenditure is required. A simple flow diagram of the assembly process, illustrating how and when the various elements are brought together to create an assembly, is provided in Figure 7-1.

A brief examination of the assembly process based on the flow diagram is provided.

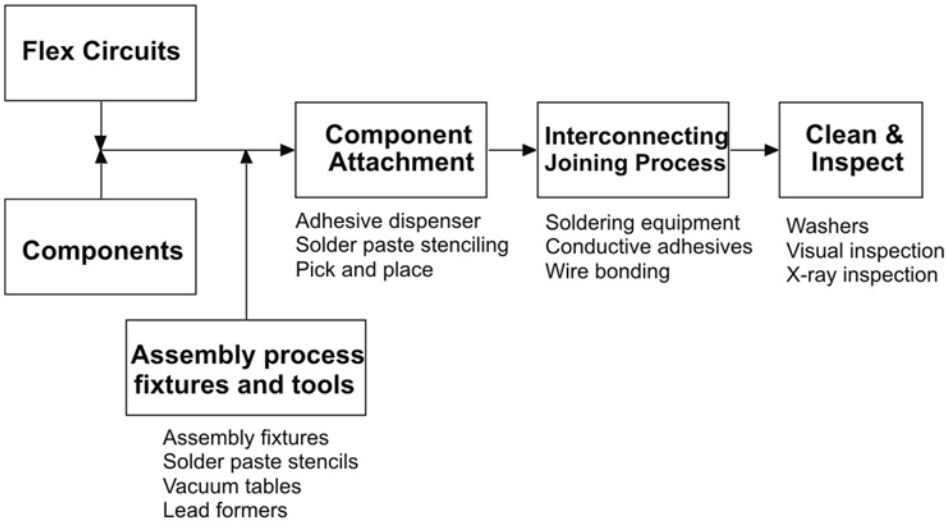


Figure 7-1 Simplified flow diagram for flex circuit assembly

Flex Circuit & Component Preparation

As the principle elements of a flex circuit assembly, the flex circuit and the components should be properly prepared. One thing that most plastic components and flex circuits have in common is that they take up moisture. This means that they must be protected from humid environments. Otherwise, they must be pre-baked to prevent explosive outgassing of trapped moisture and the creation of defective conditions such as cracked components or blistering and delamination of the coverlayer. With the more recent introduction and use of photoimagable liquid masks rather than a traditional coverlayer, the problems of moisture and baking have been reduced but not eliminated.

If baking of the flexible circuits is required, then a typical temperature would be above 100ºC to dry out the circuits. The upper temperature may be 110-125ºC; it's all dependent on the time when the circuits reach temperature. Plain flexibles have very little mass; flexi-rigid boards will have more mass and require more time to dry out. To minimize the temperature and time so as not to impact the solderability of the surface coating, the moisture content levels need to be established.

For component preparation, it has been suggested that the optimum component lead angle for leaded surface-mounted components is 60º +/– 5º. That angle can be opened up to 45-65ºfor existing designs where the component body has been reduced in width. The purpose of the 55º to 65º lead angle is to provide added strain relief in x, y, and z axis during thermal cycling beyond what the flex circuit can offer intrinsically. To achieve high reliability, the heel fillet of the solder joint should be adequate. Component lead angles greater than 65-70º improve the chances of this. While component lead co-planarity is important to good assembly, one shouldn't force leads into co-planarity by using a thermode or other method to drive component leads into the solder. It is better to reform the leads off line. In practice, there are few issues with the components, provided the design of the footprint is correct, the terminations are solderable, and they all meet the minimum requirements of the soldering process—i.e., they can stand up to convection, vapour phase reflow and rework temperatures for tin-lead or lead-free alloys. Typical reflow temperatures for tin-lead are 210-225ºC; for lead-free they will be 230-250ºC. If parts are to be subjected to wave solder on the base of the board, then the tin-lead can be between 240-250ºC and lead-free 255-270ºC.

Assembly Process Fixtures and Tools

A range of fixtures and tools is required for normal assembly. The requirements of these elements will vary with the assembly process chosen. For example, through-hole assembly fixtures for wave soldering are quite different from those required for surface mount assembly. A brief discussion of each process is warranted.

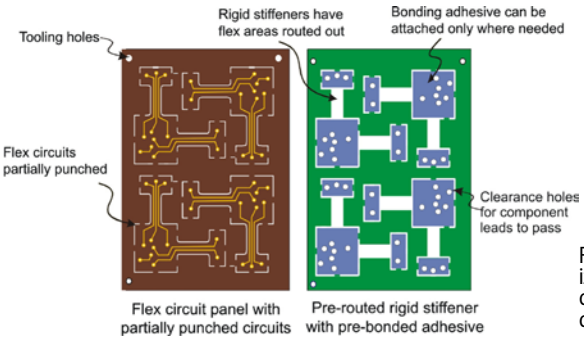


Figure 7-2. Mass application of stiffeners in panelized form facilitates both stiffener application and component assembly. When bonded together, the circuit can be processed much like a rigid board.

Wave or Selective Solder Fixturing

Wave solder fixtures are designed to carry the flex assembly over a molten solder wave while keeping the flex circuit and components stable. There are several possible solutions to this problem. For example, the flex circuits can be left attached to the stiffener assembly in panel form as illustrated in Figure 7-2. This method is relatively common. It can be a cost-effective solution, provided there are not an excessive number of defective parts in the panel and the use of the stiffener is beneficial at other stages during assembly and test.

Another possible method for fixturing flex circuits for wave solder is illustrated in Figure 7-3. Here, either individual holes are drilled or much larger openings are provided in a carrier plate that allows the component leads and plated through holes to be properly accessed by the solder wave. There are design rules available from many solder pallet/fixture manufacturers for both wave and selective soldering. Basically, the thickness of the material between the wave and the flexible should be the minimum to support the flexible and to make sure that the pallet does not flex during soldering. The thicker the material, the more it will displace the wave during contact, requiring larger clearances. The flexible must be held flat in the pallet and not allowed to rise, as this will lead to flux and solder getting under the flex and onto the pallet, leading to a manual cleaning step each time a pallet is processed.

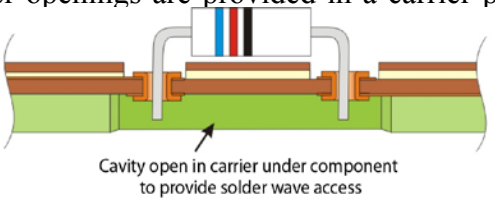
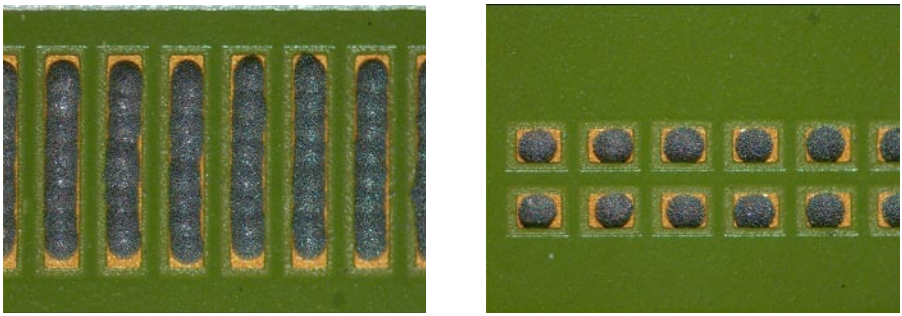


Figure 7-3. Fixtures for wave soldering should support the flex circuit through the wave while providing access to the leads and through holes of the flex circuit. The edges of the pallet wall should be chamfered as much as possible to allow the solder to flow in and out from the aperture. Ideally, the gap between the lead and the edge of the pallet on the trailing edge should be larger to aid solder drainage.

Surface Mount Fixturing/Tooling

Surface mount assembly of flexible circuits is extremely difficult without proper tooling and fixturing. There are a number of different tools and fixtures required. A solder paste stencil is the most common way to apply solder paste on the surface mount lands. There are no real changes in stencil design or aperture modifications for flexible circuits as the surface is basically rigid when printed. Stencil thicknesses used are generally in

line with rigid board technology: 0.005-6″ thick, produced by laser or electroforming nickel. A new solder paste jetting technology is an option for New Product Introduction NPI and small- to medium-production runs, thus eliminating the stencil requirements. Development over the last couple of years with different paste suppliers makes it a valued option.



Examples of solder jetting being used on a circuit board for fine pitch and 0201 chip components. The circular pattern of the round jetting patterns is just visible in the surface of the paste. The images were taken from a board process on a Mydata MY500. (Courtesy of Bob Willis)

Normally, a vacuum system is used to hold the circuit flat during the screen printing of solder paste. Direct vacuum fixturing on reel-to-reel lines is used for special applications but less so solder paste printing. Reel-to-reel assembly is illustrated in Figure 7.8 later in this chapter. This is frequently used in combination with special fixtures such as described earlier. The individual fixtures or pallets can be made from a variety of materials such as glass epoxy or anodized aluminum. The fixture provides a stable base for processing, thus allowing more common soldering process profiles to be run. An example of a fixture for surface mounting a flex circuit can be seen in Figure 7-4.

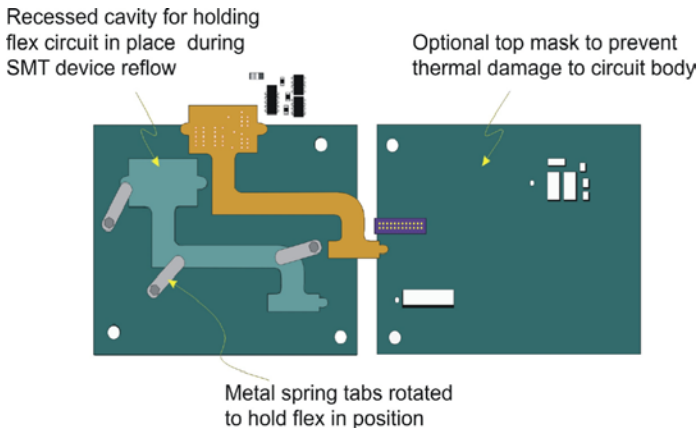
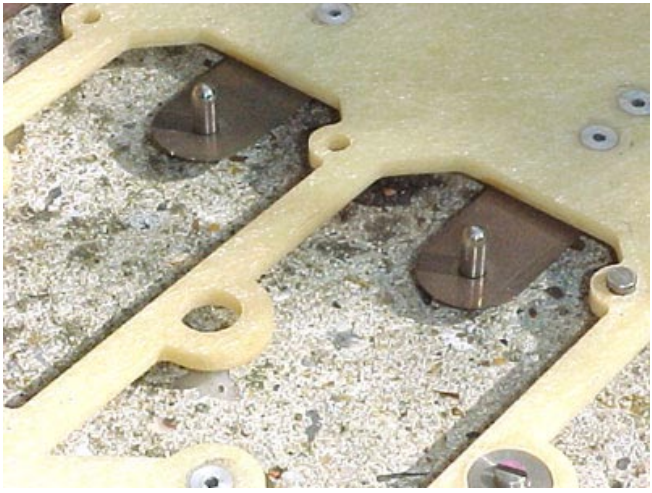
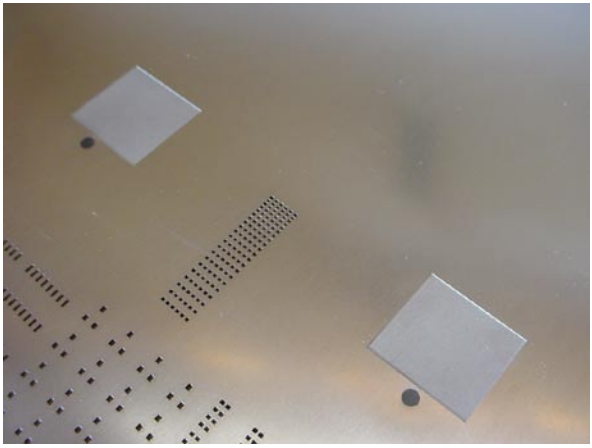


Figure 7-4. The fixture for surface mount on flex serves to keep the circuit flat and supported during the reflow operation. A top mask can be employed to prevent thermal damage to the bulk of the circuit. This facilitates the soldering of lower melt temperature base materials when they are economically preferred.

Retracting tooling pins can be used on thin rigid and flexible circuits to locate the images for assembly but retract when required. One example is shown above. These pins may be necessary when printing solder paste with a stencil. (Photo courtesy of Bob Willis)





The base of this solder paste stencil foil has been designed to allow for minimum pin protrusion during the printing process. (Photo courtesy of Bob Willis)

Figure 7-5. Example of a carrier for flexible circuit assembly. Thermal relief areas on the base of the pallet have been machined directly under the active circuits to improve delta T during reflow. Also consider drain holes under the flex if using vapour phase reflow or if cleaning is being considered. (Photo courtesy of Bob Willis)

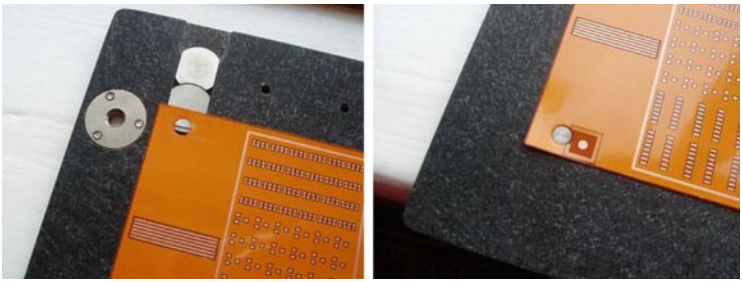
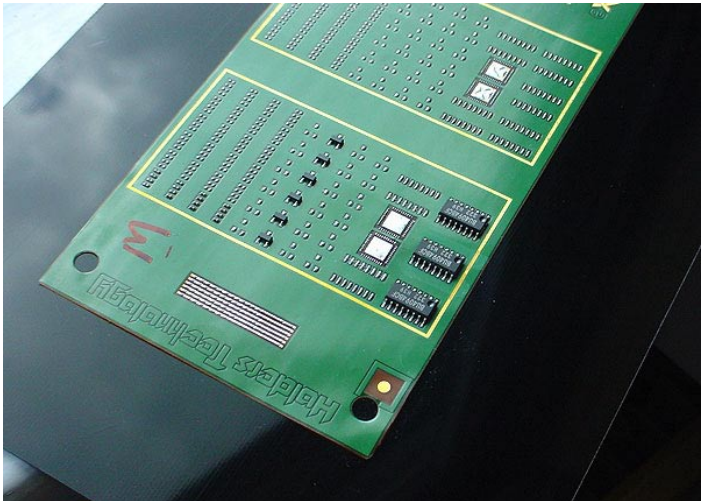


Figure 7-6. Zero standoff pins serve for aligning and holding the flex circuit to the fixture. Any minor protrusion of the pin above the surface of the flex would need to be considered in the solder paste stencil design. (Photos courtesy of Bob Willis)

Use of sticky pallets is a fairly recent trend in the Far East and has not seen use in other parts of the world. The material will stand up to high temperatures associated with lead-free assembly and can be used multiple times before cleaning. Although recommended for 500 process cycles prior to cleaning, pallets produced from these materials have been used in high volume. As with traditional pallets, fiducial alignment marks on the flexible circuit are used during printing and component placement to overcome any error on the fixturing. The pallet can be used through the complete assembly process.

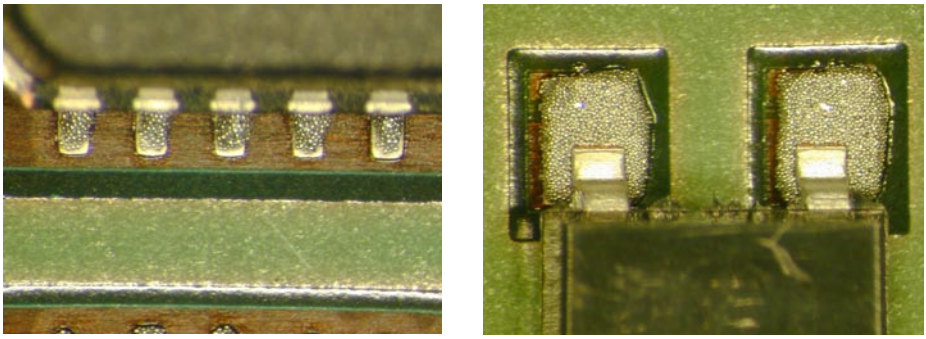


Example of a sticky pallet with a flexible circuit assembly in position. Normally, the sheet of material would have some tooling holes to make automatic placement of the flexible circuits possible in production. (Photo courtesy of Bob Willis)

Component Placement

Placement of components onto a flexible circuit board is best performed automatically, though manual placement can be used for prototype or low-volume production depending on complexity. The efficacy of modern automated equipment and manufacturing management

practices continues to reduce the low-volume crossover point. Component density is another factor requiring consideration, for as component densities increase, manual placement becomes more difficult. As the carrier pallet supports the flexible through each stage in the process, there are no issues during placement: The machine just sees the circuit as a rigid board for assembly.



Examples of components placed onto solder paste prior to reflow; the two examples show a row of terminations on a Land Grid Array and SOT23 package. (Photo courtesy of Bob Willis)

Nonconductive, high-temperature adhesives are useful in holding components in place while the soldering operation takes place. Only small dots of adhesive are required for wave soldering applications. They can be applied by point dispensing, stenciling or pin transfer. SMT adhesive would normally be used only when the components are to be reflow-soldered; it has in the past been used when conducting simultaneous double-sided reflow.

In the case of wave soldering, care needs to be taken over the selection of the adhesive and the polyimide cover layer, as often the adhesion forces can be lower after curing. Trials should be considered using the flexible substrate of choice and adhesive. Shear force measurements of components like SOT23 will be in excess of 600-800grams.

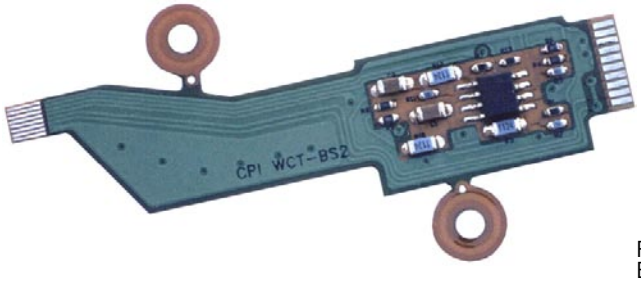


Figure 7-7
Example of a flex circuit SMT assembly
(Courtesy Interconnect Systems, Inc.)

Interconnecting and Joining Processes

There are several process options available for making electrical interconnection between the component and the flex circuit. The choice of joining method is linked hierarchically—firstly to the electrical performance and reliability expectations of the finished product and secondly to the materials used in making the flex circuit. Following are some of the most common methods in use.

Conductive Adhesive Attach

Conductive adhesives are a popular method of assembling components to certain types of PCBs. The adhesives normally consist of UV- or thermally-cured epoxies, which are filled with silver particles. The material can be stenciled or dispensed point by point onto the selected component lands prior to assembly. However, care needs to be taken over the application of these circuits, as any dynamic flexing may still require the component and joints to be supported, often with another material.

Solder Joining

Tin-lead-based solder has long been the most common method for interconnecting components to flex circuits. Of the many different types of tin-lead solder available, Eutectic Sn63Pb37 solder (M.P. 183ºC) is perhaps the most commonly used solder. Other solders are of value for flex circuit assembly, especially where lower melting-point base materials, such as polyester, are used in the flex circuit construction. Indium-tin solder (In52Sn48 [M.P. 117ºC]) and bismuth-tin solder (Bi57Sn43 [M.P. 138ºC]) have both been employed for such purposes.

More recently, the tin-silver-copper family of lead-free solder alloys has been used with melting points between 217ºC and 221ºC, suitable only with polyimide flexible materials.

In a reflow process, the solder is melted using a reflow oven. IR, forced air convention and vapor phase are all candidate processes. Care should be taken in profiling any flex circuit assembly process because of their much lower thermal mass. Examples of assembly profiles for a flex circuit assembly using lead-free solder can be seen in Figure 7-8.

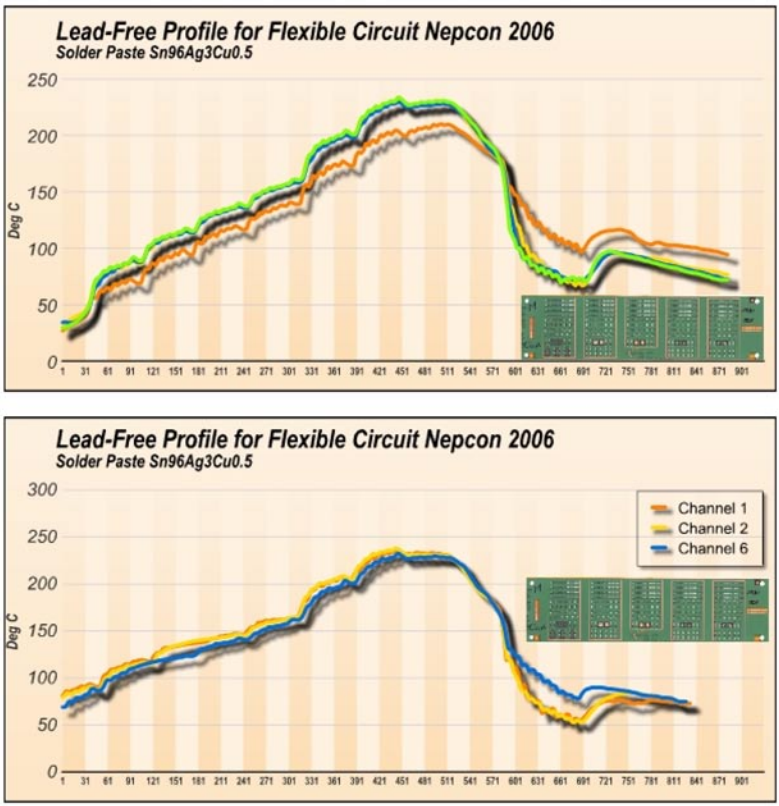


Figure 7-8: Two lead-free soldering profiles for a flex circuit assembly on a process carrier using a KIC profiler. The first profile shows a larger delta T between selected terminations on the circuit. After modification to the carrier and reduction of the thermal mass, the second profile shows a more acceptable reflow profile. (Courtesy of Bob Willis)

Reflow Soldering

There are three methods used for reflow soldering of flexible circuits and surface mount components. They are:

- **Hot plate – conduction**
- **Vapor phase reflow**
- **Convection**

Hot plate reflow

Hot plate reflow is probably one of the oldest processes, often referred to as brown or black belt reflow, where circuits are reflowed by conduction. A linked chain conveyor would drag pallets holding the flexible circuits over a

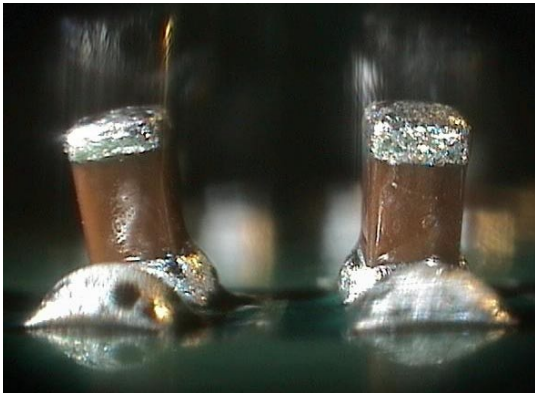
series of heated plates at different temperatures to achieve reflow. A profile could be defined by individually setting the hot plates—not an ideal control, but cost-effective in the early days of SMT.

A simple and quite elegant manual soldering process for a few small surface-mount non-fine pitch packages on polyimide flexibles would be a static hot plate. Positioned on either side of the hot plate would be a preparation plate and a cooling plate. Operators would place a solder-leveled circuit on a hot plate after first fluxing the pads with a liquid flux. The surface mount components would be placed manually on the pads and then the circuit slid onto the hot plate; when reflow of the joints had taken place, the circuit would be moved from the hot plate to the cooling plate. Often, operators would flux and move the circuit onto the hot plate, then start to place the components to increase throughput.

Vapour phase soldering

Vapour phase soldering (VPS), also referred to as condensation soldering, has been around in the industry for many years and was one of the only two serious options during the early introduction of surface mount technology. The first reflow system used by many engineers for SMT was VPS, as they preferred the simplicity of the process and process set-up over the problems of accurate loading, board belt positioning, profiling and overheating flux residues on infrared IR. The introduction of convection reflow, which is still the most significant part of the marketplace, was like VPS without the fluid when compared to IR reflow.

A well-designed board worked very well and gave high soldering yields. A poor design, particularly on passive components, would amplify the number of lifted and tombstoned components. All vapour phase systems can show a difference in component lift due to the fundamental nature of the process—fluid on a surface. As the vapour condenses on the surface of the board and turns to liquid, component movement can occur. Is this a reason to dismiss VPS? No—it's often just an excuse to stick with the poor design. A recent lead-free trial comparing VPS with convection showed an increased number of lifting defects with VPS. If you only looked at the total PPM levels, you might say that VPS was the cause, but the defects were all on one



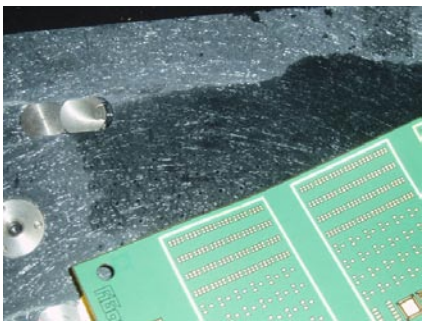
component size; hence the need for good documentation during design reviews and NPI at contract assembly companies.

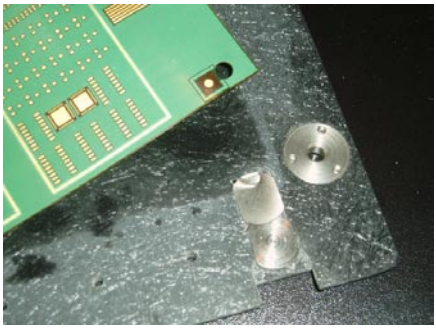
Example of 0402 tombstone capacitors on a flexible circuit prior to modification of the design rules on the circuit. (Photo courtesy of Bob Willis)

In the original batch vapour phase system, the primary fluid was boiled and generated a vapour layer. In order to contain this vapour within the size constraints of the holding tank, it was necessary to cover the vapour to prevent it escaping; this was done with a secondary fluid that also produced a vapour layer boiling at a lower temperature. The condensing coils used cold water running through them at a very low flow rate to recondense the vapour; the fluid then circulated back through filters. Above the primary coil, another coil was used to reduce the loss of the secondary blanket of vapour sitting on top of the primary fluid.

In operation, a basket loaded with assembled boards would simply be lowered through the secondary layer and into the primary. After the work had reached reflow temperature, the basket would be raised. On the way up, it was allowed to dwell in the secondary basket in order to contain primary vapour and fluid. Ideally, the board or basket would be very slightly angled to allow condensed fluid to run off. The basket would then be raised out of the machine and allowed to cool. Prior to this operation, the assembled boards did have to go through a preheating operation to reduce the possibility of thermal shock to the volatile material in the solder paste. This was normally conducted using a separate oven. Today, this is all incorporated into the VPS systems to control more tightly the profile of the board assemblies. Only one fluid is selected, boiling at either 230ºC or 240ºC. The option of using a vacuum on some systems allows for further reduction of voiding in joints.

There are still differences in the delta T on the board surface and under components in VPS, but it is very small at the peak temperatures, provided time is allowed for the profiles to converge. The initial temperature rise through preheat does have recordable differences, just as in convection, but can be smaller depending on the machine design. Through good design and process control, the amount of fluid loss can be very small, and recent surveys of users show an extremely economic and flexible process for lead-free.





Using support pallets with vapor phase soldering requires modification to prevent the fluid being retained under the circuit. Holes placed under the circuit will reduce dragout of the fluid. (Photos courtesy of Bob Willis)

Convection reflow

Convection reflow is the most common reflow soldering process in the industry; machines have been used successfully for reflow of tin-lead or, more recently, of lead-free for many years. Both air and nitrogen systems have proven to be very successful when correctly set up and maintained. Basically, a reflow oven consists of multiple heating zones with a mesh conveyor for small-volume or pin conveyor for inline high-volume transportation of the product through the zones. Each zone temperature is set to achieve a temperature rise on the assembly prior to final reflow of the solder paste to form the interconnection between the component termination and the flexible circuit pads. Generally, the higher the convection rates in the zones, the further reduced the delta T across the surface of the assembly. Controlling the zone temperatures, convection rates and conveyor speeds allows an engineer to define a process profile.

Preheat

When the printed board loaded with components first enters the reflow oven, it is at ambient temperature around 18-20ºC. Initially, the preheat section will increase the temperature of the assembly. The rate of temperature rise will depend on the oven settings and the thermal demand of the board and pallet. Some component suppliers limit the component specifications to a rise temperature of 3-4º per second.

During preheat, any volatile material in the paste can be driven off, and the initial cleaning action of the flux contained in the paste can be started. Some materials do not activate until they reach substantially higher temperatures. During preheat, every effort is made not to create too much of a temperature differential on the board surface as it may be difficult for this to be overcome during the soak period. A temperature rise in the initial preheat zone can be between 80-150ºC.

Soak

The soak period allows all temperatures on the surface of the board to normalise. It is inevitable that, during preheat, some termination areas on the surface of the board will heat up more quickly than others. Today, with the greater sophistication of reflow technology, the surface of the board can see limited temperature variations, but at the component termination interface the temperatures will vary. As a guide, under a plastic ball grid array, the differential temperature can be 10-15ºC. Under a through-hole connector body, the temperature difference can be 15-20ºC higher than the surface of the circuit board; hence the need for effective profiling.

Reflow

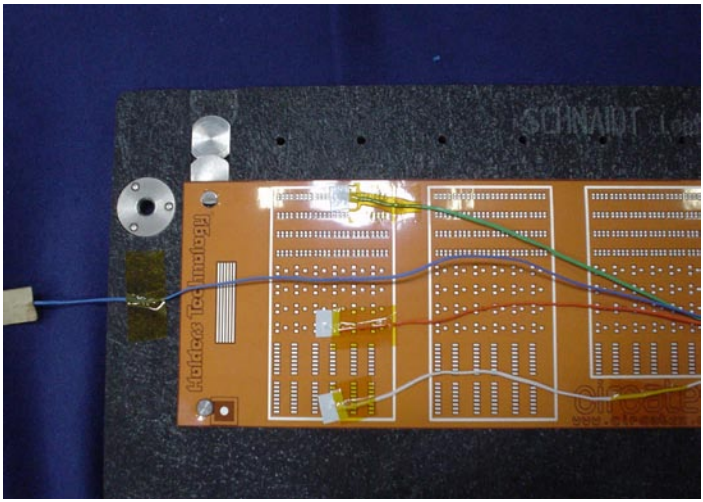
The reflow zone is where the board temperature moves over the liquid temperature of the solder paste. The paste is normally 63/37 or 62/2/36, the first reflowing at 183ºC and the second silver loaded alloy becoming liquid at 179ºC; in the case of lead-free tin-silver-copper, 217-221ºC.

The aim of the reflow zone is to allow reflow in the shortest time possible to produce reliable joints—normally within 30 seconds. This is usually dependent on the temperature differential of the board entering the reflow zone. If the assembly temperature is less than, say, 140ºC and there is a 20ºC differential, all joints will not make reflow temperature.

Cooling

When all the solder joints have been formed and the board moves out of the heating zones, the board will begin to cool naturally and the solder will solidify. To speed up cooling, blowers are used as standard, blowing ambient air. In recent years, air has been replaced by nitrogen, and refrigeration systems have been introduced to speed up the cooling cycle.

Some engineers suggest that you cannot conduct reflow reliably in a reflow oven of fewer than five zones, but this is not true. Provided the board assembly can be reflowed with the minimal differential temperature across the board, not subjecting the components to a thermal shock outside their specification and having the joints in a liquid state for a period of less than 30 seconds, any number of zones is acceptable. The only limiting factor of short 5-zone reflow ovens is the throughput speed and the cooling.



Profiling a flexible on a pallet may require a combination of thermocouple attachment techniques. The use of high-temperature solder is the preferred technique, but aluminum tape can be very beneficial on flexibles. The pallet was set up for profiling with an air probe for the KIC system. (Photo Courtesy of Bob Willis)

Nitrogen

The use of nitrogen has become popular over the last few years, particularly when using low-residue solder pastes and copper OSP coated circuit boards. The use of lead-free has also forced some companies into using nitrogen to improve the process window. The nitrogen is being used to displace the oxygen and open up the process window during reflow soldering. Oxygen levels in reflow soldering at or below 1000 ppm have been shown to improve soldering performance and prove economically viable if copper

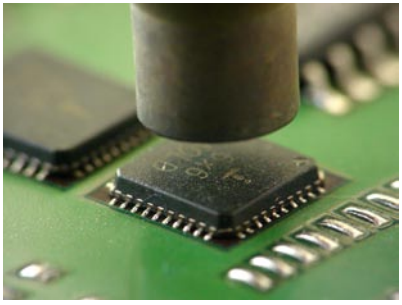
boards are being used. The use of copper boards coated with an organic solderable protector (OSP) is cheaper than gold or lead-free solder levelled, and the saving can offset the use of nitrogen. Hence the quality and process improvements obtained with the use of nitrogen are free, or nearly free.

Profiling

Profiling rigid boards or flexibles is essential to guarantee that peak temperatures for components are not being compromised and that the soldering process is in line with paste suppliers' recommendations. Some engineers have said that profiling is not required with VPS, but just look at the profiles in this chapter for different pallet designs. Although the difference in delta T in convection reflow is higher, VPS soldering will see an impact from the mass of the pallet.

Rework on Flexible Circuits

Rework of surface mount solder joints on flexible circuits should not be more challenging than on their conventional counterparts; hot air, infrared or contact heating tools can be very effective with tin-lead or lead-free, and, again, it is dependent on the materials used to produce the flexible. Consideration needs to be taken of the moisture content on circuits with a coverlayer. It has often been considered that copper pads can be easily lifted on flexible during rework, but just as with conventional boards, if the solder is in a liquid state, then no force is applied to the surface—only heat. Well-trained staff can rework boards without damage; it's a matter of making sure that the skills are learnt and that management provide the time for staff to perfect the theory into practical experience.



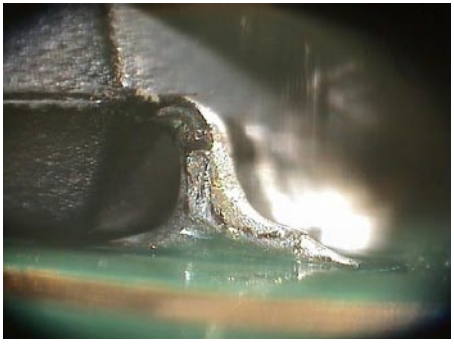
Example of the Land Grid Array (LGA) package being reworked on a polyimide flexible circuit with a hot air tool.

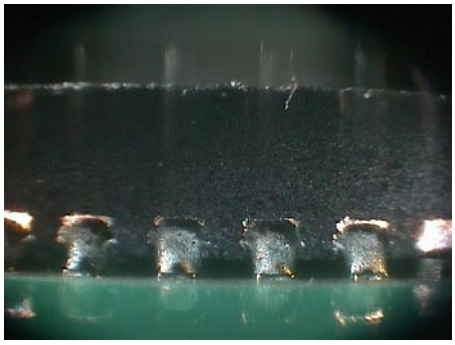
A chip capacitor is being removed, using a set of hot tweezers.
(Photos Courtesy of Bob Willis)

Solder Joint Inspection

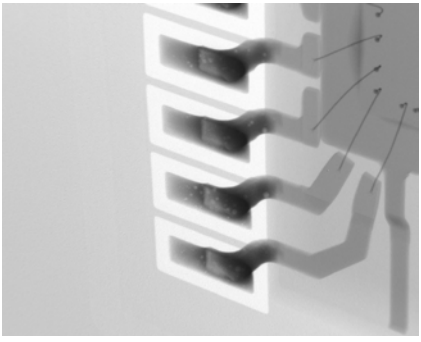
Inspection of solder joints can be conducted manually or automatically using automatic optical or x-ray inspection equipment. Inspection criteria in IPC 610 or, where required, other industry criteria for flip chip, through-hole reflow, underfill and land grid arrays, can apply. In the case of automatic inspection, the same pallets can be used for the assembly stages, providing an ideal support.

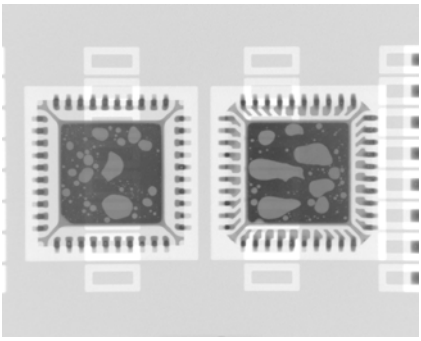
As a flexible circuit can be semi-rigid or fully flexible, the full range of defects related to normal reflow or wave soldering will still apply in manufacture. As flexible circuits can lift and float if not properly fixtured for assembly, it is more likely to see examples of the open joints rather than short circuits, so consider the type of possible defects when defining inspection procedures.





These examples show typical lead-free solder joints on a flexible circuit after assembly and soldering.
Examples of a gull wing lead on an SOIC and LGA terminations were captured with an ERSA Scope. (Photos Courtesy of Bob Willis)





X-ray images of gull wing and LGA terminations assembled with tin-silver-copper
were inspected and captured in real time on a DAGE system. (Courtesy of Bob Willis)

Reel-to-Reel Assembly

There have been several efforts to assemble flexible circuits using reel-to-reel (or roll-to-roll) assembly methods. Conceptually, the approach is very attractive, especially for flexible circuits processed in a reel-to-reel. One concern for such assembly is that if there is need for a line shutdown, a significant amount of product may be at risk, and reworking in web form is somewhat problematic. Still, it remains an appealing approach for certain types of high-volume products that are small and have few components. Examples of such products include smart card assemblies and RFID devices, which, typically, have only one or two components. Such devices can be assembled using more traditional soldering methods, conductive adhesives or wire bonding technology. Sheldahl and Phillips Corp. co-developed a piece of equipment in the 1990s wherein the reflow oven was placed on rails, allowing it to be moved back and forth over the web in case of a web shutdown, and thus allowing the operator to prevent local overheating by moving the oven back and forth over the web to prevent hot spots.

An example of a prospective piece of reel-to-reel assembly equipment is shown in Figure 7-9.

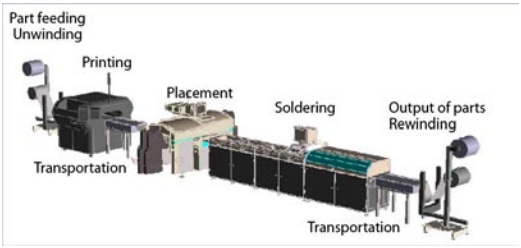


Figure 7-9 A prospective piece of equipment for reel-to-reel assembly of flexible circuits. (Source: Siemens L&A)

Wire Bonding

Wire bonding is a very useful interconnection technology, long employed in IC die assembly when interconnecting the chip to a leadframe or package. The technology has also been employed successfully in direct assembly of IC chips to flex circuits. Wire bonding is performed by one of two major methods: thermosonic bonding and ultrasonic or wedge bonding. The choice of wire bonding process is highly influenced by the materials used and reliability requirements of the finished product. For example, wedge

bonding with aluminum wire can be performed at room temperature and is thus a good choice when lower-temperature laminate materials are used. In contrast, thermosonic bonding of gold wire requires a heat bonding stage that is commonly operated at 150º C. Of these two primary methods, thermosonic offers greater versatility in terms of design and termination placement as the second bond can be made at any angle after the first bond is complete. Wedge bonding is much more constrained and more directional.

As an interconnection technology, wire bonding also offers some unique design advantages owing to its allowing the assembly process to provide jumpers proximate to the die, if desired. Correct selection of the surface coatings, and maintaining that surface for bonding, are extremely important.

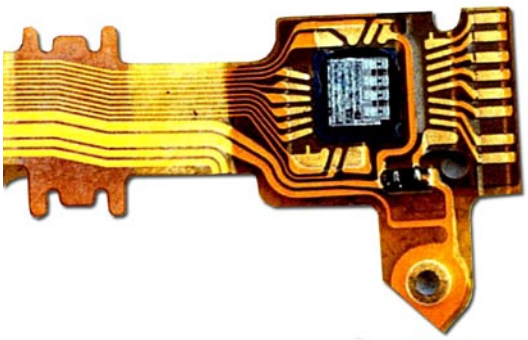


Figure 7-10 Example of a chip-on-flex assembly in which the IC chip is wire-bonded directly to the flex circuit. (Courtesy Interconnect Systems, Inc.)

SUMMARY

Assembly of flexible circuits requires special knowledge, special tooling and a great deal of care. This chapter has attempted to highlight some of the most important points and experiences from manufacture. A great number of excellent books have been published on the subject of component assembly and soldering technology, and, while they are not specific to flexibles, they may also be of value.

“The future is unknowable beyond the undeniable fact that it will be different from today, for change is the only universal constant.”

Joseph Fjelstad

Chapter 4

Solderless Assembly Processes for Flexible Circuit

By Joseph Fjelstad, Verdant Electronics

Introduction

Flexible circuits have proven themselves as a method of choice for an increasing number of electronic product designs. The reasons have been recounted in this text and others elsewhere many times. Included among benefits are design freedom, light weight, reduced size and improved electrical performance, just to name a few. While flexible circuits continue to be used to make simple electrical connections, as they have since their inception, they have been increasingly used to make much more complex electronic assemblies, especially for handheld electronic products such as cell phones, PDAs and the like. Such assemblies routinely involve the placement and interconnection of surface-mount devices using solder. In fact, it was observed by researchers in the nascent surface-mount industry that flexible circuits offered a more reliable platform for surface mount.

This was because the flexible substrate had a low modulus of elasticity, thus reducing strain on solder joints during the thermal excursions associated with use.

This was an important observation for the industry, as it not only offered a pathway to making reliable surface-mount interconnections but also reinforced the concept that interconnection compliance—either from the substrate or the leads—was a vital concern. This is not to say that reliable interconnections could not be otherwise achieved. In fact, faced with the daunting task of having to address the concerns of assembly that came with components and substrates having significant mismatches in terms of coefficients of thermal expansion (CTE), other researchers, most notably at IBM, proved that the use of an underfill between the component and the substrate could also protect the solder joint interconnections.

Tin-lead solder has been the primary method for connecting electronic components to printed circuits of nearly every type since near the time of the electronics industry's inception. Over the last sixty years, solder has proven itself a viable and valuable assembly method. In addition, over that time span, the industry developed a deep understanding of the solder technology that was hard-won over years of practice. However, as of July 2006, the European Union banned the use of lead in electronic solder, based on the misguided assumption that lead in electronic solder represented a real risk to human health, an assumption that has yet to be proven by the scientific method.

This new era of lead-free solder has resulted in a host of new problems for the electronics industry, many of which had not been experienced when elemental lead was included in the solder alloy. Electronics assembly technology literature is replete with articles and papers citing the problems or challenges of lead-free assembly and proposing new or improved solutions or investigative tools, which might better serve to unearth the problems of lead-free soldering.

Because of the European Parliament's sanction of lead in electronic assembly, there is presently an ongoing global effort to create lead-free electronic products. The lead sanction has created a challenge of significant

proportions for the electronics manufacturing industry in terms of meeting the cost and reliability demands of OEMs. For example, the production of lead-free electronics requires the exposure of electronic circuits and components to much higher temperatures (e.g. 30°C-40°C) than are required for printed circuit assemblies with traditional tin-lead solder. Moreover, due to the greater complexity of modern electronic assemblies with two-sided assembly and stacked components, such exposures might not take place just once but several times.

Unfortunately, as is well known by reliability engineers, exposure of electronics to higher temperatures degrades component reliability. These negative effects are not limited to integrated circuits alone. The damaging effects of the higher lead-free solder temperatures on optoelectronic components and certain types of discrete components such as larger capacitors have also been identified as concerns. Moreover, the use of excess energy not only degrades reliability and shortens IC life: It also wastes energy. There are, in addition, other types of concerns. For example, the increasingly extensive use of tin plating as a termination finish is reopening the door to a problem once solved—specifically, the problem of tin whiskers. With component lead pitch shrinking to below 0.5mm and tin whiskers capable of growing to lengths of 10mm-12 mm, concerns about the recurrence of whisker risk are justifiably elevated. Finally, it is a simple fact of life that global sourcing and supply-chain expansion has greatly increased distance between electronic product designers and their suppliers. The result is a reduction in vital resources and support for domestic technology development in many developed nations in Europe and North America, which could result in supply-line vulnerability in troubled times.

In this environment, a new approach to manufacturing all types of electronic assemblies, including flexible circuits, without the use of solder, (i.e. solder-free) is now in development. The new process has come to be known as the Occam Process, so named to honor the 14th-century English philosopher and logician William of Occam, whose rigorous thinking and arguments in favor of finding the simplest possible solution served as the inspiration and catalyst for the new approach.

Solderless Assembly Process Basics

Given the rather extensive list of challenges and concerns just reviewed, a new method for fabricating circuit assemblies has been disclosed that sidesteps all of the problems created by the lead-free solder directive. The new method is, in the most basic sense, a reverse of standard assembly in that the electronic components are placed first and *then* provided with interconnections by plating up the circuit patterns and making connection to the component terminals. There is, however, one important twist: The new approach does not employ solder. With this simple change, the process does not subject the PCB or the components of the electronic assembly to the temperatures of 250°C-270°C required to assemble with SAC alloys, which have become de facto standards for assembly. There is also no real concern about moisture sensitivity, as components will not be exposed to soldering temperatures. In addition, concerns about flux removal from tiny spaces beneath components and between their leads are obviated because flux is not used. Moreover, because the fully tested and burned-in components used in the assembly are completely encapsulated, the concerns of mechanical shock and thermal cycling reliability of connections are vastly diminished. As a final point of interest, in 1999, Agilent Technologies engineer Stig Oresjo conducted a major study of solder-joint defects on printed-circuit boards. The study included 15 companies and more than one billion solder joints, and the author concluded that "although companies claimed defect levels in the range of 75 to 150 defects per million opportunities (DPMO), the reality was five to ten times that high." An IPC presentation from the proceedings of a test conference having a slide reporting on the study offered the following defect distribution results:

1) 41% Solder Opens
2) 20% Shorts
3) 20% Solder Quality
4) 8% Placement
5) 8% Electrical
6) 3% Other

From this, it is evident that 80% of the problems of electronics assembly are related to soldering (90% if the 8% for placement is included). The 8% electrical problems, though not specific, may be at least in part the result of solder temperatures; thus, any effort to eliminate solder does arguably have merit.

While there are certain approaches to creating solderless assembly that can be used with traditional circuit boards, the more attractive assembly approaches at this time do not require a separately fabricated printed circuit board. This fact allows the manufacturer to bypass completely issues related to certification and qualification of vendors and other RoHS-related concerns in supply chain management, which is now often global in scope and includes inventory and storage management, preparation, certification and design modification.

Solderless Assembly Process Detail

To better understand the solderless assembly process and its many benefits, a good comprehension of traditional electronics manufacturing is of value. Currently, the standard practice for the manufacture of a conventional electronic assembly includes the following familiar steps. Using surface mount technology as a model, first, a schematic and components list is created and a PCB is designed, fabricated, tested and delivered to the assembler. The assembler stencils solder paste onto the component interconnection lands located on the PCB, and the components are then accurately placed on the board and temporarily held in place by the paste until the solder paste is reflowed at soldering temperatures. The reflow process creates a permanent interconnection between the component leads and the PCB terminations. The method just described is a process that works, but it is not perfect: Shorts and opens are often found on the electronic assembly and, on occasion, components are damaged by the temperature of assembly. In fact, rework and repair are considered part of the normal manufacturing regimen and are often factored into the cost.

In contrast, the solderless assembly process is fundamentally a reverse order interconnection process. The process uses, for the most part, mature, low-risk, industry-familiar core processing technologies in a proven sequence. A key element and artifact of the process is that the electronic components are interconnected to one another by copper plating after they are assembled into their final positions, and solder is completely avoided. The basic steps of this process embodiment are illustrated below.

Detailing the new process approach step-by-step, one finds that the components are first placed onto any one of several bases. These could

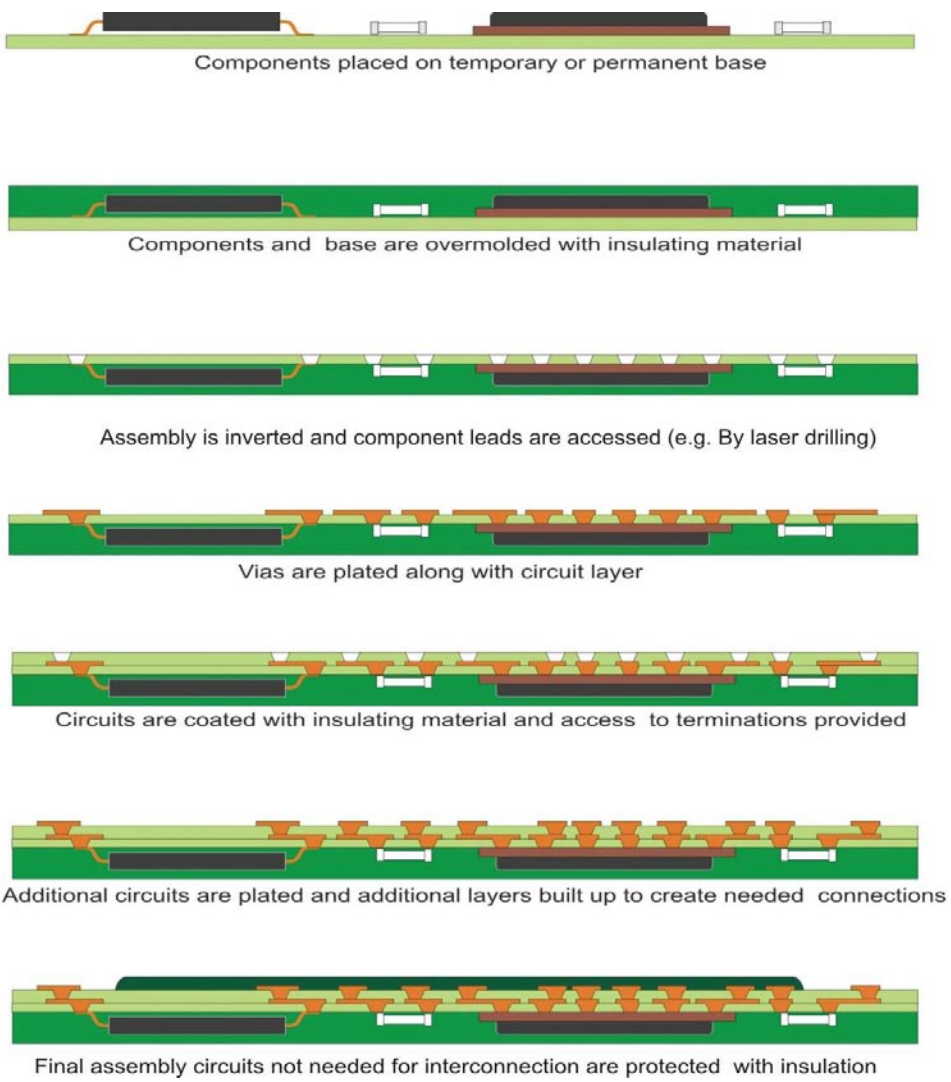
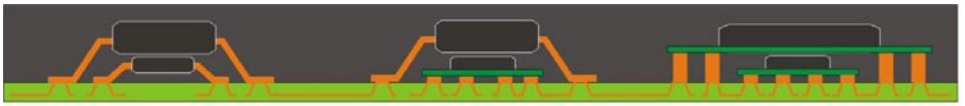


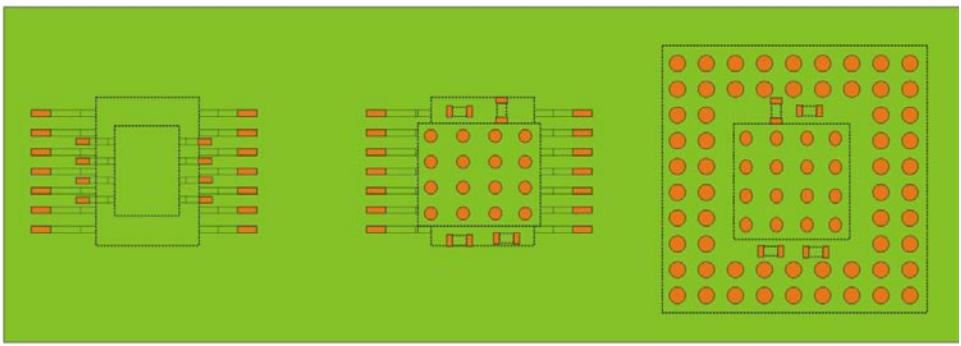
Figure 1: The basic Occam process manufacturing steps.

include, but are not limited to, a removable tacky film on a temporary base or a permanent base that uses a permanent adhesive. In either of these cases, the base temporarily immobilizes the components until the structure is encapsulated. At this point, the entire array of tested and burned-in components has become a monolithic assembly, with all components now permanently locked into a predetermined place. The bottom surfaces of component terminations can then be exposed by removing the temporary base and film or by making holes in the permanent base using a suitable method such as mechanical abrasion or laser ablation. An interesting benefit of the

technology is that it allows for components to be assembled in an overlapped manner, which is not possible in traditional circuit manufacturing.



Placement of IC components directly on top of one another or small discrete devices (not visible) can greatly increase component packaging density



Component contact view of cross section above show land patterns for packaged IC components and discrete devices.

Figure 2: The Occam process allows for components to be stacked one above. another when possible and desired for even higher density designs..

All the connections to the component terminations are then created by a conductive circuit creation (e.g., copper plating) step, which makes the interconnections to the exposed surfaces of the terminations arrayed across the encapsulated module's surface. Circuit patterns can be created at this point and additional layers of insulation and circuits added as necessary until all required connections are made. The interconnections can even be redesigned as needed up to the moment they are made, and no high-aspect-ratio via drilling is required. Methods similar to this have seen use in the creation of multichip modules and packages that were destined for soldering in the past. As noted earlier, it is also possible to interconnect the assembly by the co-lamination of circuit layers to the encapsulated component assembly block.

Just such methods have been developed and used by Matsushita and Toshiba for the production of multilayer circuits in recent years.

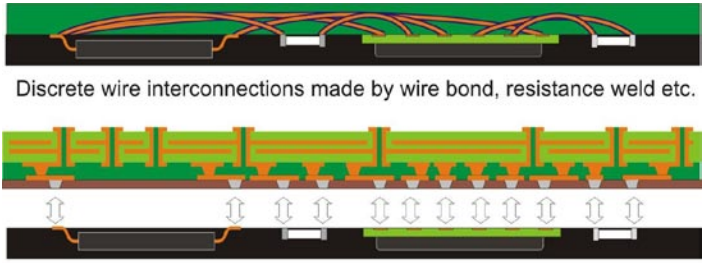


Figure 3: Once the components are secured in place, interconnection can be made in a number of different ways such as discrete wiring and lamination with programmed or anisotropic bond layers. Direct writing techniques (not shown) are also possible.

Assemblies of this type are expected to be low in cost and readily adaptable to the integration of thermal enhancements such as internal head spreaders or even heat pipes, as well as EMI shielding, embedded electrical and optical components, and more.

The final circuit layer can be connected to whatever user interfaces, displays and power connections are required for operation by means of any suitable interconnections or connectors. The assembly can be coated with a conformal or rigid protective insulator layer. Moreover, when two layers of components are required, they can be stacked and joined back-to-back with a central support, which could include various heat spreader constructions such as were described earlier. More advanced structures are then possible, and stacking and interconnection of assemblies from one side to the other can be accomplished by interconnection pins inside the assembly, either individually or in groups and arrays. Edge connections can be created that will allow for stair-stepped interconnections. The potential of these structures appears to be limited more by imagination than physics. If desired, interconnection between sides can be augmented by various connector structures or flex circuits as well, as shown in Figure 4. While it is not possible within the limits of this section to provide images of all of the potential thermal management

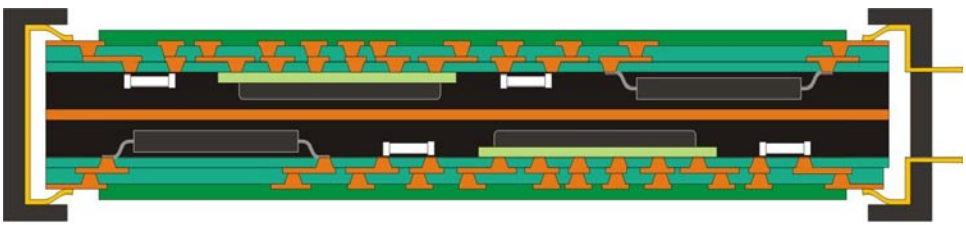
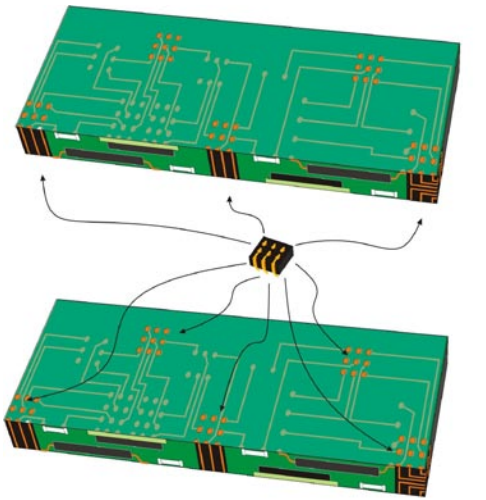


Figure 4: Components can be embedded in both face-up and face-down manner and attached to a central heat spreader, as shown. Connections from side to side can be made with connectors, as shown, or with through-hole "via plugs" that can be placed where needed on the assembly.another when possible and desired for even higher density designs.

solutions, optical interconnect alternatives, EMI and ESD protection methods, connectors, second-side, and odd-form enhancements that are achievable, it is expected that there will be many such offerings making their appearances as the technology moves into more complex applications.



Low profile connectors such as above make connections between assemblies. They can be discrete as shown or in sheet form. A layer of material with cutouts for connectors and their alignment can be provided.

Figure 5: Assemblies can be connected in stacked or in edge-card manner depending on the needs of the design. another when possible and desired for even higher density designs.

Repeated here for emphasis is the fact that because the Occam process does not involve exposing the assembly to the high temperature needed for reflow soldering of lead-free solder, component moisture sensitivity level is essentially obviated as a concern. (Note: The moisture sensitivity level, or MSL, is a measure of the risk of component damage due to absorbed moisture in the package during soldering, devised by JEDEC or the Joint Electronic Device Council.) Moreover, while traditional tin-lead solder processing's maximum temperature is around 220°C, SAC alloys approach 260°C and the vapor pressure of water more than doubles over this 40°C temperature change, and component damage due to explosive outgassing of absorbed moisture in the package during soldering is an increased concern; but when no soldering is required, all such concerns are obviated.

All components can be treated as if they were MSL-1, which means that they do not require dry storage, special handling or accurate hold-time recordkeeping in normal environments. The process also allows use of components that are not capable of withstanding lead-free soldering temperatures (aluminum electrolytic capacitors, optoelectronic devices, some connector types, etc.). Moreover, and also repeated here for emphasis, is the fact that because no high-temperature soldering is required, heat spreaders, heat sinks or even heat pipes can be embedded directly into or made an integral part of the assembly.

Design and Routing Advantages of Solderless Assembly Structures

As has already been stated, the solderless assembly process is not completely different from standard assembly; only the order of manufacture is reversed. Like a standard printed wiring board, the interconnect structure still must be designed and fabricated. However, with the Occam process, several design constraints are relaxed. For example, there is no need for large component pads or lands for soldering; thus, simplified routing for area array is possible, as can be seen in Figure 6.

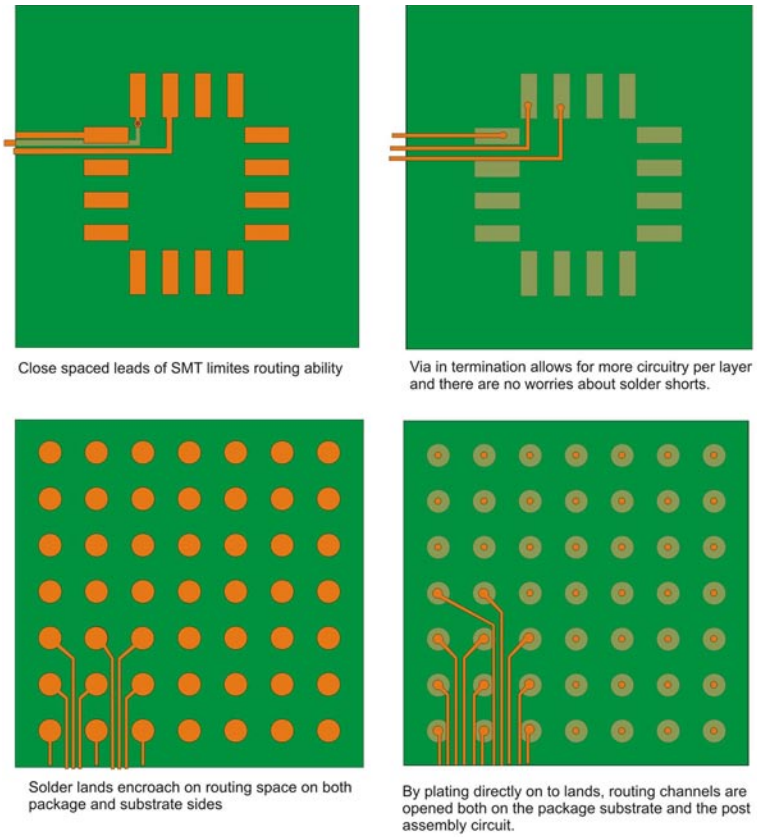


Figure 6: Routing advantages are possible for both peripheral and area array packages. Moreover, because there is no need for reflow and cleaning, the Occam process allows for edge-to-edge tiling of BGAs to create shorter path interconnections with reduced energy use and higher performance..

This feature allows a higher circuit density as well as a potential reduction in the number of layers required for the design. Moreover, there is no need for drilling high-aspect-ratio vias all the way through the assembly, as special structures have been anticipated to address the need when faced.

The new approach to design and manufacture is also amenable to implementation using the interconnected mesh power system (IMPS) design approach developed at the University of Arkansas by Professor Len Schaper and his colleagues in the 1990s. In the design process with IMPS, a design starts with a grid of power and ground conductors that are three times the width of a minimum width signal conductor and separated by the minimum space. Signal conductors are then routed through the spaces of the mesh, with the power and ground narrowed to accommodate them. While IMPS structures were originally designed with IC chip modules in mind, the concepts are applicable to higher-level interconnections as well. Hewlett-Packard, for example, worked on a similar concept called Power Mesh. It was developed for the coarser features that are found on standard PCBs, and the Power Mesh structures use full metal ground planes. [i]

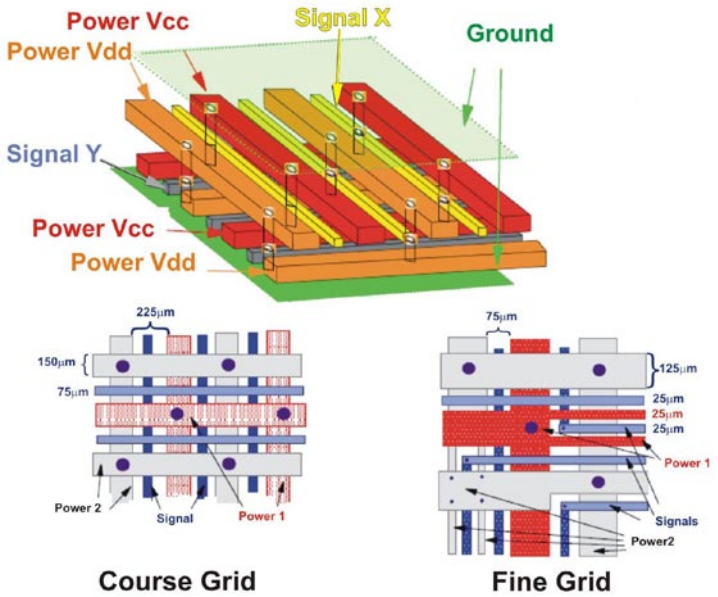


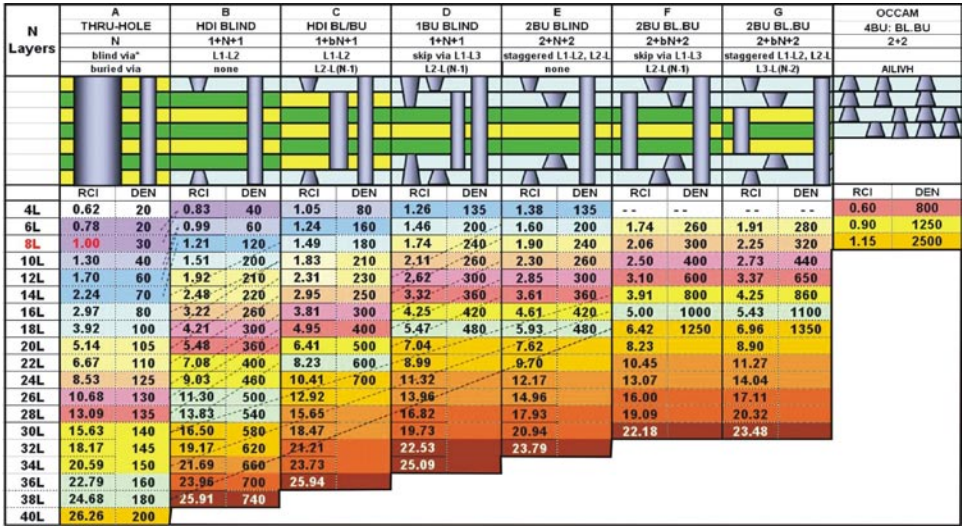
Figure 7: The Occam process is well suited to designing with the IMPS approach developed at the University of Arkansas, or the similar Power Grid concept developed at HP, which employs full metal grounds. Significant layer reductions can be achieved. With Power Mesh, multilayer routing efficiency for each layer approaches 95%. (Image courtesy of Happy Holden, Mentor Graphics)

The mesh is never broken or disconnected. All of the signal conductors are coplanar transmission lines referenced to both power and ground, and the reference is preserved when the signal goes from X to Y. Crosstalk is very low, because there is always an AC ground conductor between every pair of signal conductors. The initial mesh establishes the allowed signal tracks. Any EDA router can be used to lay out the signal wiring in the channels.

A design rule check is used to impose minimum clearance on the power and ground to narrow traces as required. The general design method has been shown capable of significant layer reductions compared to traditional design approaches (e.g. from 8 layers down to 4 layers or even 2 layers), while offering lower noise and lower crosstalk, based on measurements. [ii] These innovative wiring architectures can replace as many layers of conventional through-hole wiring. When coupled with Occam type processing to create a direct HDI interconnection to component terminations without the need for soldering, the combination could well support requirements for I/O connections up into the hundreds of I/O per cm. [iii] An analysis of relative cost of various multilayer circuit constructions and the I/O density capability is provided in Figure 8 and reveals that, when compared to a standard 8-layer plated-through-hole construction having a relative cost of 1.0 and I/O density of 30 pins per square inch (~6 pins per cm2), an Occam buildup structure is capable of replacing up to a 14~18-layer board with perhaps a 4 - 8 layer board while providing 2500 I/O (~400 I/O per cm2) and maintaining a relative cost of 1.15. [iv]

Solderless Assembly Review

The nontraditional approach to electronics manufacturing that has been described portends the elimination of solder from the electronics assembly



N Layers	A THRU-HOLE N blind via* buried via		B HDI BLIND 1+N+1 L1-L2 none		C HDI BL/BU 1+bN+1 L1-L2 L2-L(N-1)		D 1BU BLIND 1+N+1 skip via L1-L3 L2-L(N-1)		E 2BU BLIND 2+N+2 staggered L1-L2, L2-L none		F 2BU BL.BU 2+bN+2 skip via L1-L3 L2-L(N-1)		G 2BU BL.BU 2+bN+2 staggered L1-L2, L2-L L3-L(N-2)		OCCAM 4BU: BL.BU 2+2 AILIVH	
	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.62	20	0.83	40	1.05	80	1.26	135	1.38	135	--	--	--	--	0.60	800
6L	0.78	20	0.99	60	1.24	160	1.46	200	1.60	200	1.74	260	1.91	280	0.90	1250
8L	1.00	30	1.21	120	1.49	180	1.74	240	1.90	240	2.06	300	2.25	320	1.15	2500
10L	1.30	40	1.51	200	1.83	210	2.11	260	2.30	260	2.50	400	2.73	440		
12L	1.70	60	1.92	210	2.31	230	2.62	300	2.85	300	3.10	600	3.37	650		
14L	2.24	70	2.48	220	2.95	250	3.32	360	3.61	360	3.91	800	4.25	860		
16L	2.97	80	3.22	260	3.81	300	4.25	420	4.61	420	5.00	1000	5.43	1100		
18L	3.92	100	4.21	300	4.95	400	5.47	480	5.93	480	6.42	1250	6.96	1350		
20L	5.14	105	5.48	360	6.41	500	7.04		7.62		8.23		8.90			
22L	6.67	110	7.08	400	8.23	600	8.99		9.70		10.45		11.27			
24L	8.53	125	9.03	480	10.41	700	11.32		12.17		13.07		14.04			
26L	10.68	130	11.30	500	12.92		13.96		14.96		16.00		17.11			
28L	13.09	135	13.83	540	15.65		16.82		17.93		19.09		20.32			
30L	15.63	140	16.50	580	18.47		19.73		20.94		22.18		23.48			
32L	18.17	145	19.17	620	21.21		22.53		23.79							
34L	20.59	150	21.69	660	23.73		25.09									
36L	22.79	160	23.96	700	25.94											
38L	24.68	180	25.91	740												
40L	26.26	200														

Figure 8: A spreadsheet analysis of relative cost of various multilayer circuit constructions and the I/O density capability reveals that, when compared to a standard 8-layer plated-through-hole construction having a relative cost of 1.0 and I/O density of 30 pins per square inch, an Occam buildup structure is capable of replacing up to a 14~18-layer board while providing 2500 I/O and maintaining a relative cost of 1.15. (Data and graphic courtesy of Happy Holden, Mentor Graphics)

process. The idea of eliminating solder is not completely new, however. Previously proposed means to do so, such as the use of conductive adhesives, have not been accepted by the market for various cost-performance and reliability reasons.

Lead-free, though well intentioned, is, according to a recent EPA study[v], less environmentally friendly than tin-lead solder technology and is causing the electronic manufacturing industry to spend billions of dollars unnecessarily on new equipment and towards the development of new materials and methods to meet the EU's RoHS requirements in the process. Realizing this dire situation, a number of household-name companies from around the globe are beginning to develop processes and to manufacture prototypes using solderless assembly and interconnection methods. Forward-looking PCB manufacturers and EMS assemblers are on the path to learning more about each other's processes and how to adapt and integrate each other's technologies into their own manufacturing processes.

In the end, the elimination of—or, rather, the integration of the printed circuit board manufacture directly into assembly—avoids many of the less obvious costs such as supply-chain management (vendor qualification, lead-times, incoming QC, etc.), testing, inventory management, protective storage, bake-out and handling. Also, because the interconnection is not created until after assembly, the design can be modified as needed with no necessity for drills, fills and jumper wires. Finally, it is anticipated that the finished product will be totally encapsulated with a tough and properly CTE-matched epoxy or other material and, thus, will be quite rugged because the solder joint (which is the most commonly identified failing element of failure, rework and repair) is eliminated.

Flex Circuit Assemblies without Solder

While most of the attention on the solderless assembly process in this chapter has been focused on the manufacture of replacements for traditional rigid printed circuits, the technology can also be applied to flexible substrates, accessing the many important attributes and capabilities that flexible circuits commonly offer the user while adding to them the benefits of solder elimination. One of the significant potential benefits is the opening up of the opportunity to use a wider range of new materials. For example,

polyester materials have some very attractive properties and significant cost advantages over flex materials such as polyimide. Polyester is very low in moisture uptake, making it a more stable dielectric for controlled impedance applications, and it is also a reasonably tough film suited to dynamic flexing; however, one of the things that has held this useful polymer back is the fact that it cannot be easily soldered with tin-lead solder, and it is essentially impossible to solder with higher temperature lead-free solders, as the material will shrink and distort like a potato chip. With the Occam process, temperatures in the range of soldering are never experienced, and thus the expanded use prospects for polyester are greatly improved. There are other advantages, but for the sake of brevity, let's take a look at at a couple of prospective processes for creating solderless (or solder-free) flex circuit assemblies.

One of the cardinal rules of flex circuit assembly is to support the components. This requirement normally implies the need for a stiffener beneath the components. When building Occam process flexible circuits, the manufacturer still needs to stiffen the components but from the top by means of an encapsulation rather than from the bottom, as is the custom. The basic process for an all-SMT assembly is: 1) place components securely in place, e.g., adhesively bond them to the flex film; 2) encapsulate the components,

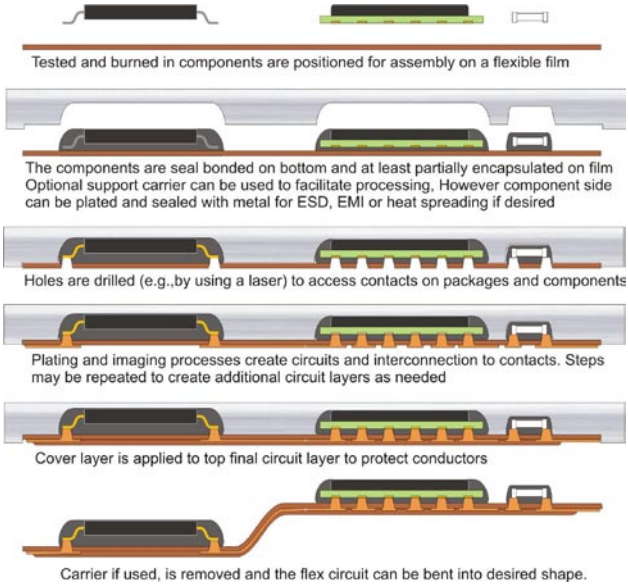


Figure 9: The Occam process applied to flexible circuits offers some unique design and assembly possibilities.

leaving the areas designed to be flexible open; 3) place assembly on optional carrier; 4) access component terminations using a laser or chemical milling process; 5) copperplate blind via connections to the component contacts, and plate and etch circuit patterns; and 6) apply cover layer.

Monolithic Solderless Flexible Circuit Assembly

An alternative approach to creating solderless flexible circuit assemblies is to bond a piece of flexible film or cast a thin flexible film onto components that are embedded in a precast structure. Access to the component leads is accomplished by use of any suitable controlled-depth feature-access process such as laser, plasma, chemical milling or similar method. A significant benefit of these types of structures is that they obviate the need for stiffeners for component support, as they are embedded in and integral with the assembly. However, perhaps even more interesting is that it appears feasible that the encapsulation of the components and film could be produced in a single step by using a suitable injection-moldable thermoplastic material, thus creating a monolithic flexible circuit assembly as shown in Figure 10.

Such approaches, when fully developed, could significantly simplify the fabrication process by providing a uniform base onto which the user can build up the circuits to complete the assembly. The graphic provided in Figure 10 illustrates the fundamental elements of the process for creating a monolithic flexible circuit assembly. Though abbreviated, the process steps shown are representative of processing possibilities

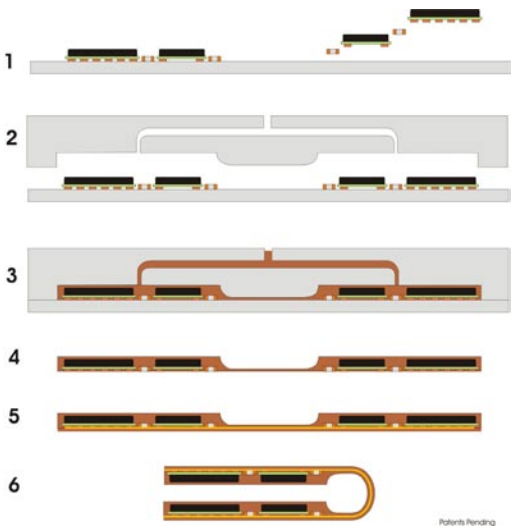


Figure 10: Injection molding allows for monolithic assembly and the integration of component stiffener and flexible interconnections according to the following plan: 1) Place components in mold; 2) Clamp mold; 3) Injection mold components in situ including strain reliefs; 4) Remove from mold; 5) Form metal circuits and coat with insulator material; 6) Form to desired shape.

Summary

In summary, the continuing challenge of making lead-free solder work has given rise to a whole new method of circuit assembly and fabrication that could eliminate solder altogether. The improved approach to assembly offered by the Occam process gives the OEM a new choice for producing products that should prove a highly reliable and cost-effective approach to electronic assembly. An added and important benefit is that the product built using the process will not only comply with RoHS requirements but will actually be far more environmentally friendly than solder-assembled products.

Full qualification of both the process and product is underway in several locations around the globe. Military product developers have been profoundly impacted by the industry's move to lead-free electronics and are showing very high levels of interest. Although they are exempt from legislated lead-free requirements, military product developers are finding themselves increasingly unable to procure components with the tin-lead solder finishes that they know are reliable, and it is for this reason that a number of major military product suppliers and their customers are moving quickly to explore solderless assembly as a way around the growing problem.

The future is unknowable beyond the undeniable fact that it will be different from today, for change is the only universal constant. If widely adopted, the Occam process just described, and/or prospective variations on it, will facilitate the manufacture of high-functionality electronics that are at once mechanically robust, highly reliable and environmentally friendly. What remains to be seen is how quickly the process can deliver on those promises. Given the rising tide of global interest, it could be relatively soon.

In conclusion, solderless flexible circuit assembly technology offers significant potential for the future. It will broaden the range of material options and significantly expand the horizon of electronic interconnection design. Once interconnection technologists and product designers begin to climb this new technology "tree" open-mindedly, they will find branches that take them to many new types of processes, methods and structures that they would not have anticipated or seen before they began the climb. The few examples described here are not likely to be the end but only the beginning of this new and evolving realm of electronic assembly without solder.

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[i] Holden, H. "A Design Technology Innovation-The Power Mesh Architecture for PCBs." *The Board Authority-CircuiTree*, Vol. 2, Number 4, Dec 2000, pp-42

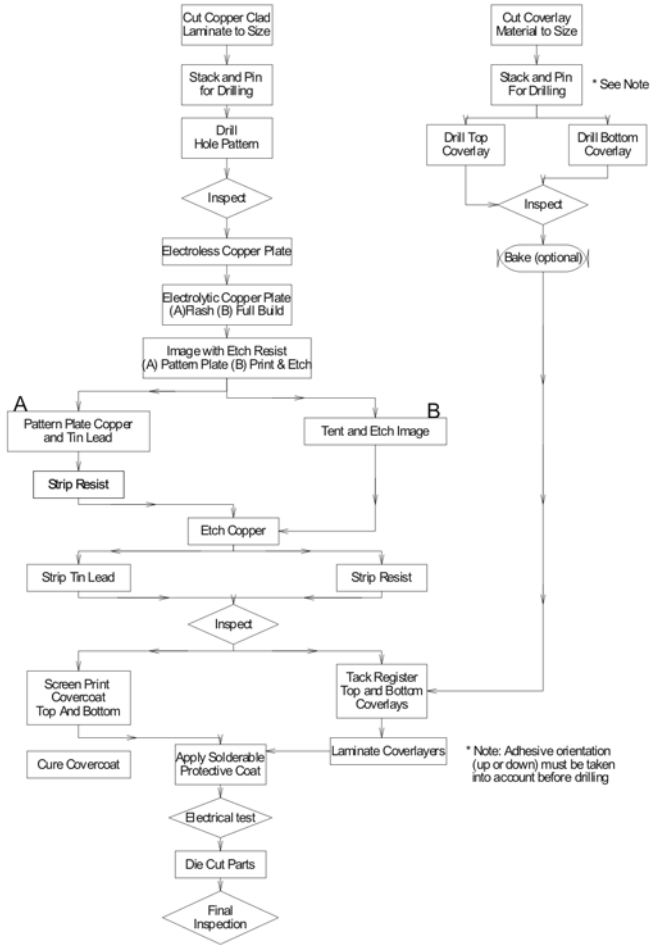
[ii] W. Schaper, M. D. Glover, and M. Kabumoto, "Comparison of the Interconnected Mesh Power System (IMPS) and Buried Stripline Interconnect Topologies." Proc. 2001 Int'l Conference on High Density Interconnect and System Packaging, 2001, pp. 58-63

[iii] Holden, H. "Will 3D ICs Replace PCBs?" *CircuiTree Magazine*, Nov 2007, pp. 38-40

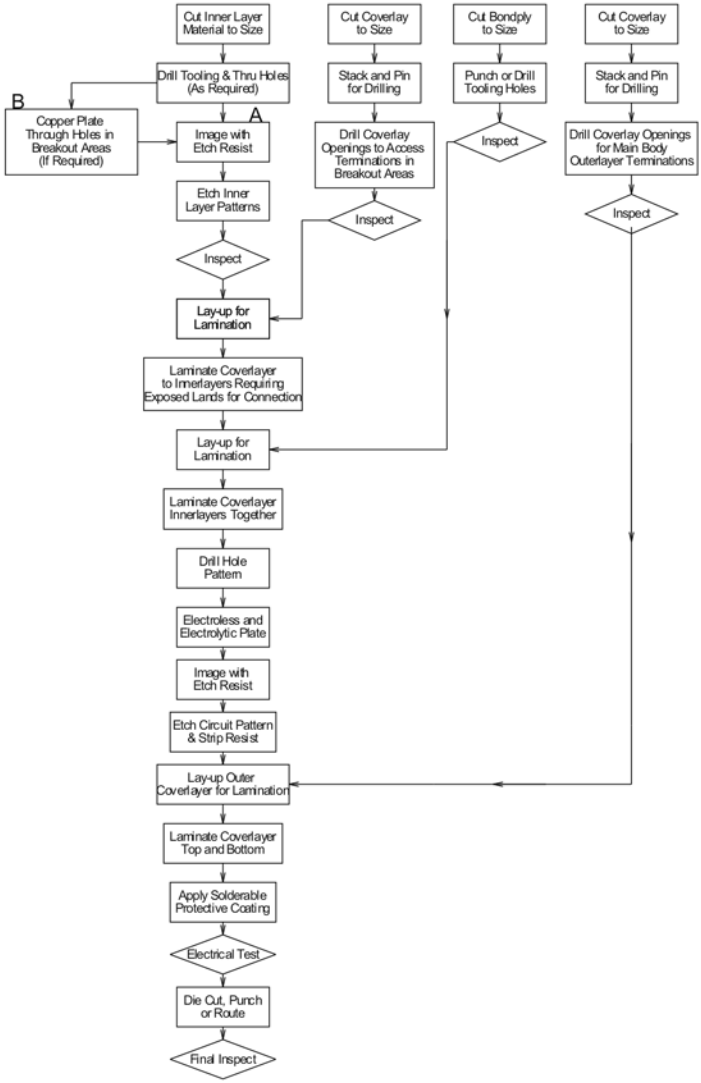
[iv] Holden, H. Proceedings, First International Occam Process Conference, San Jose, CA, October 16, 2007

[v] http://www.epa.gov/opptintr/dfe/pubs/solder/lca/index.htm

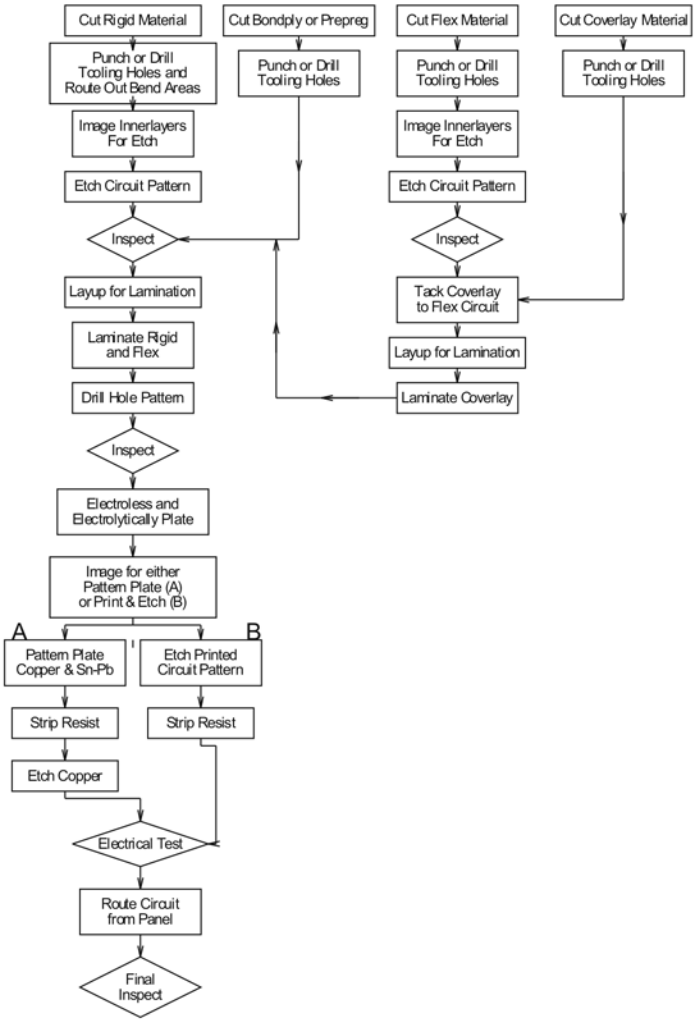
Double-Sided Flex Manufacture

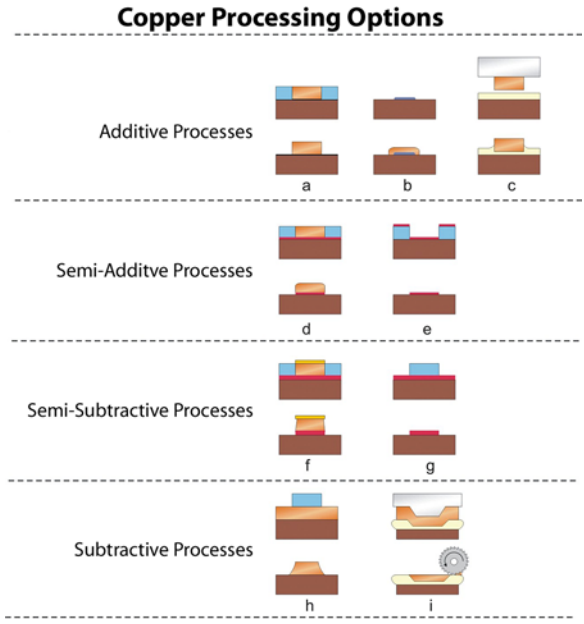


Multilayer Flex Manufacture



Rigid-Flex Manufacture




Copper Processing Options
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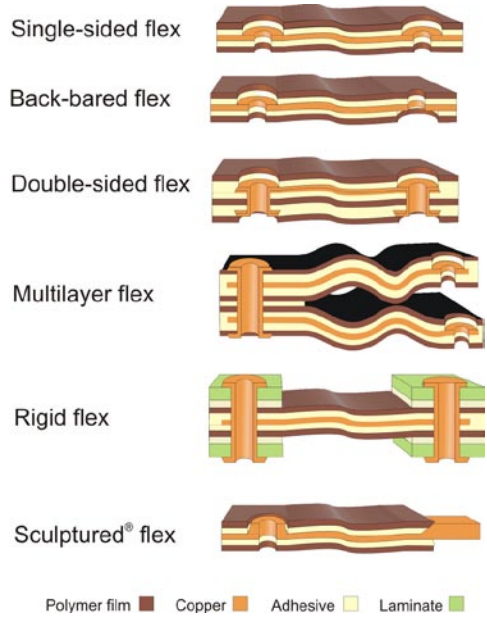
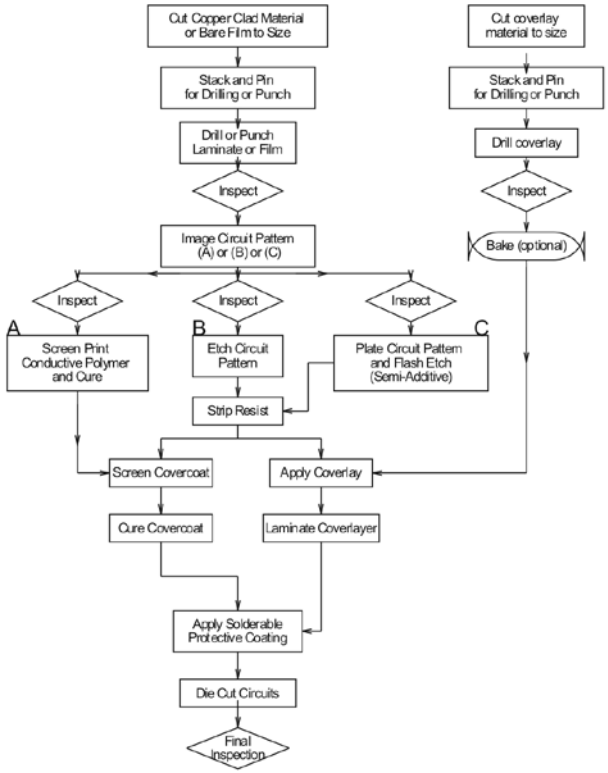

Single-sided flex
Back-bared flex
Double-sided flex
Multilayer flex
Rigid flex
Sculptured® flex
Polymer film
Copper
Adhesive
Laminate

Photo Courtesy of Flexible Circuit Technologies

Single Layer Flex Manufacture



About this book

This is an addendum to the third edition of *Flexible Circuit Technology* which has become one of the most popular texts available on the subject as a result of its simple approach to tackling this important and highly enabling electronic interconnection technology. The book was written to provide a bridge of understanding by offering a clearly defined set of steps which take the reader from basic concepts to a more detailed review of the various technology and materials that must be brought together to create these modern wonders of electronic interconnection wizardry. The book opens with an overview and brief history and then proceeds to describe the basic structures and some of the myriad applications and steps that the prospective user can take to engage in flexible circuit design and use. Materials used for flex circuits are reviewed next, followed by a comprehensive review of established flex circuit design practices and an overview of manufacturing process. The final chapters of the original book are devoted to issues related to test, inspection and a review of the important industry specifications used to help communicate needs between vendor and user. To purchase or download the third edition visit: www.flexiblecircuittechnology.com.

About the Author

Joseph Fjelstad, founder of Verdant Electronics, is a 35-year veteran of the electronics inter-connection industry and international authority, author, columnist, lecturer and innovator with more than 150 issued and pending US patents in the field. He is co-founder and CEO of SiliconPipe, a leader in high speed interconnection architecture design, much of it, not surprisingly, based on flexible circuit technology. Prior to founding SiliconPipe, he was with IC package technology developer Tessera Technologies, where he was appointed the company's first fellow.

Fjelstad and his innovations have been recipients of many industry awards and accolades, but he is most proud of the accomplishments of his children and grandchildren.

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