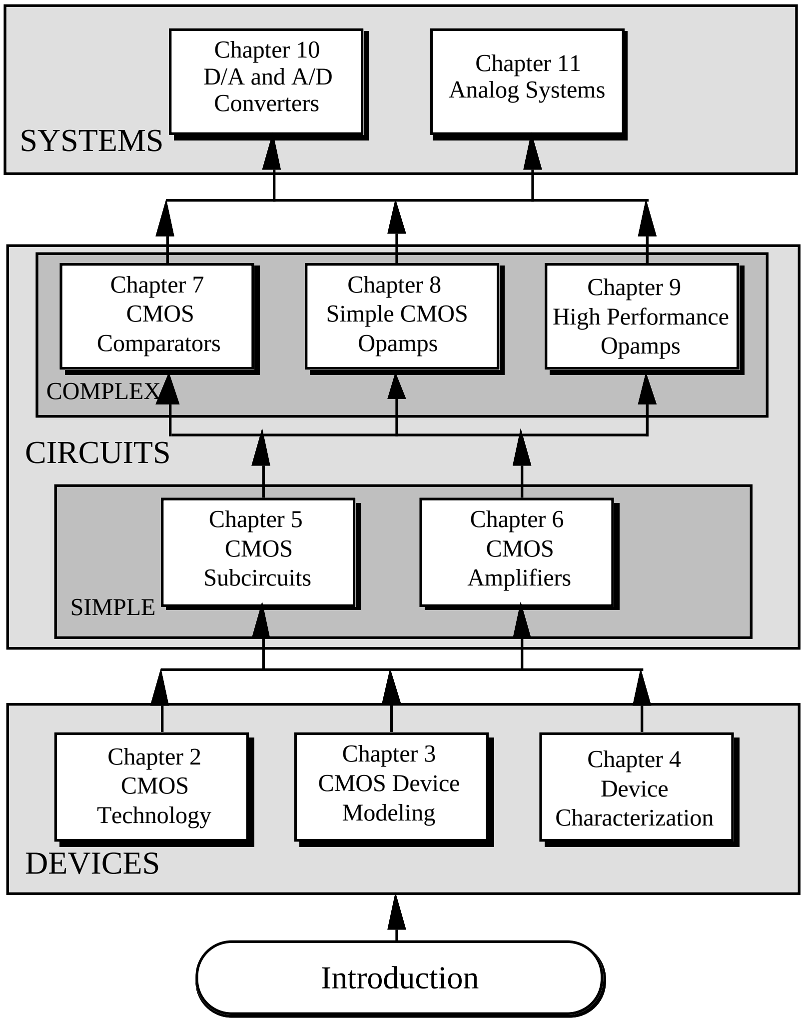
I. INTRODUCTION

Contents

Organization



I.1 - INTRODUCTION

GLOBAL OBJECTIVES

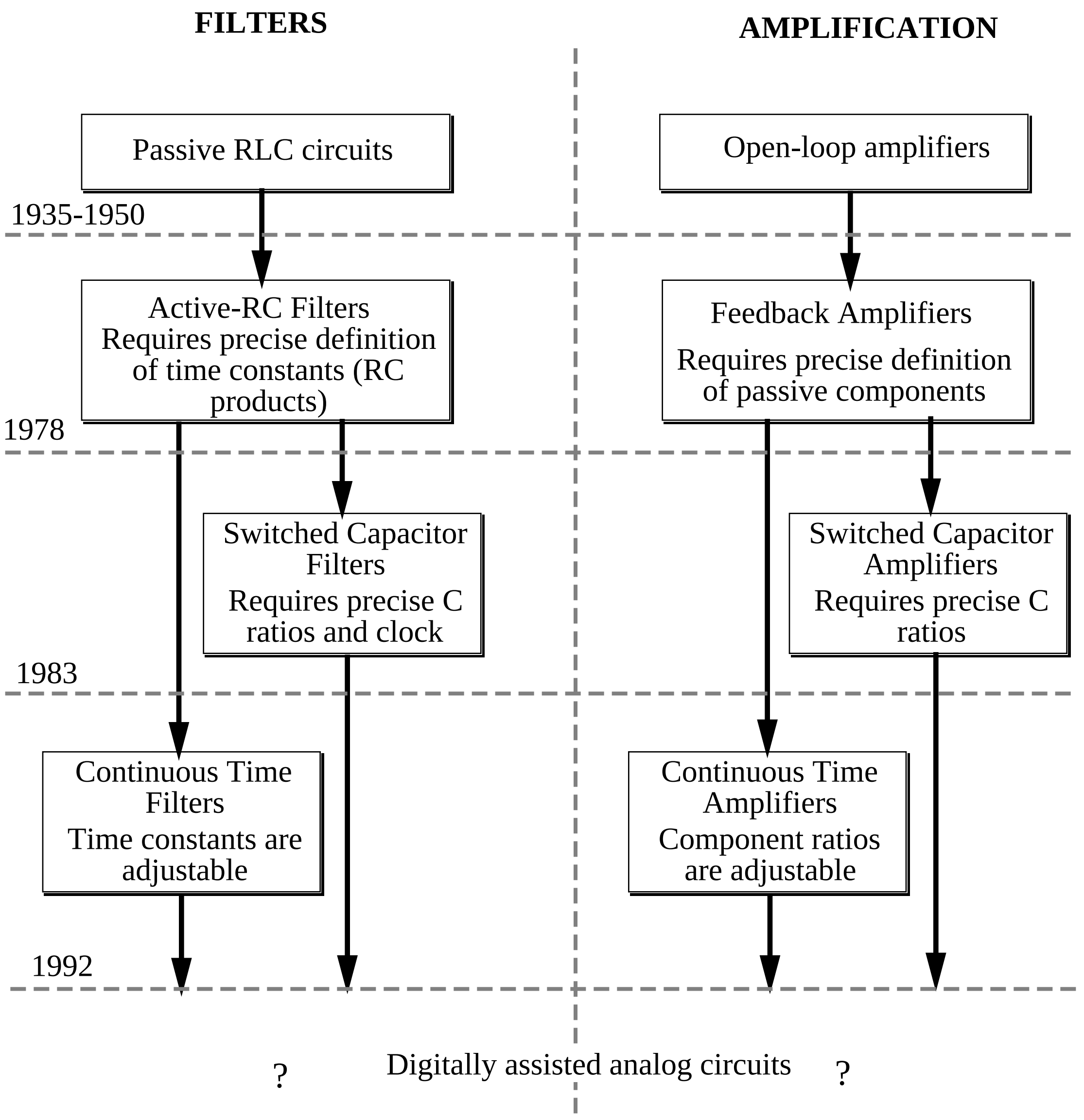
- Teach the analysis, modeling, simulation, and design of analog circuits implemented in CMOS technology.
- Emphasis will be on the design methodology and a hierarchical approach to the subject.

SPECIFIC OBJECTIVES

1. Present an overall, uniform viewpoint of CMOS analog circuit design.
2. Achieve an understanding of analog circuit design.
    - Hand calculations using simple models
    - Emphasis on insight
    - Simulation to provide second-order design resolution
3. Present a hierarchical approach.
    - Sub-blocks → Blocks → Circuits → Systems
4. Examples to illustrate the concepts.

I.2 ANALOG INTEGRATED CIRCUIT DESIGN

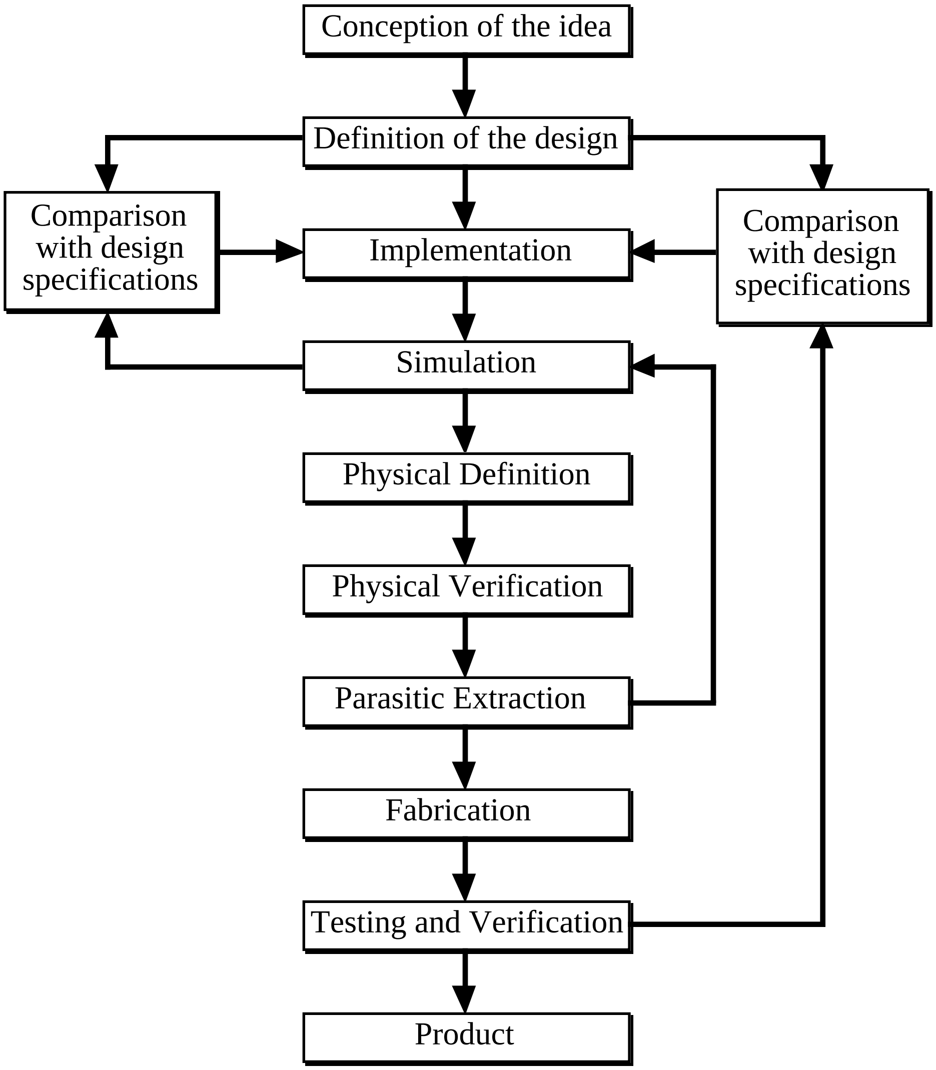
ANALOG DESIGN TECHNIQUES VERSUS TIME



DISCRETE VS. INTEGRATED ANALOG CIRCUIT DESIGN

Activity/Item	Discrete	Integrated
Component Accuracy	Well known	Poor absolute accuracies
Breadboarding?	Yes	No (kit parts)
Fabrication	Independent	Very Dependent
Physical Implementation	PC layout	Layout, verification, and extraction
Parasitics	Not Important	Must be included in the design
Simulation	Model parameters well known	Model parameters vary widely
Testing	Generally complete testing is possible	Must be considered before the design
CAD	Schematic capture, simulation, PC board layout	Schematic capture, simulation, extraction, LVS, layout and routing
Components	All possible	Active devices, capacitors, and resistors

THE ANALOG IC DESIGN PROCESS

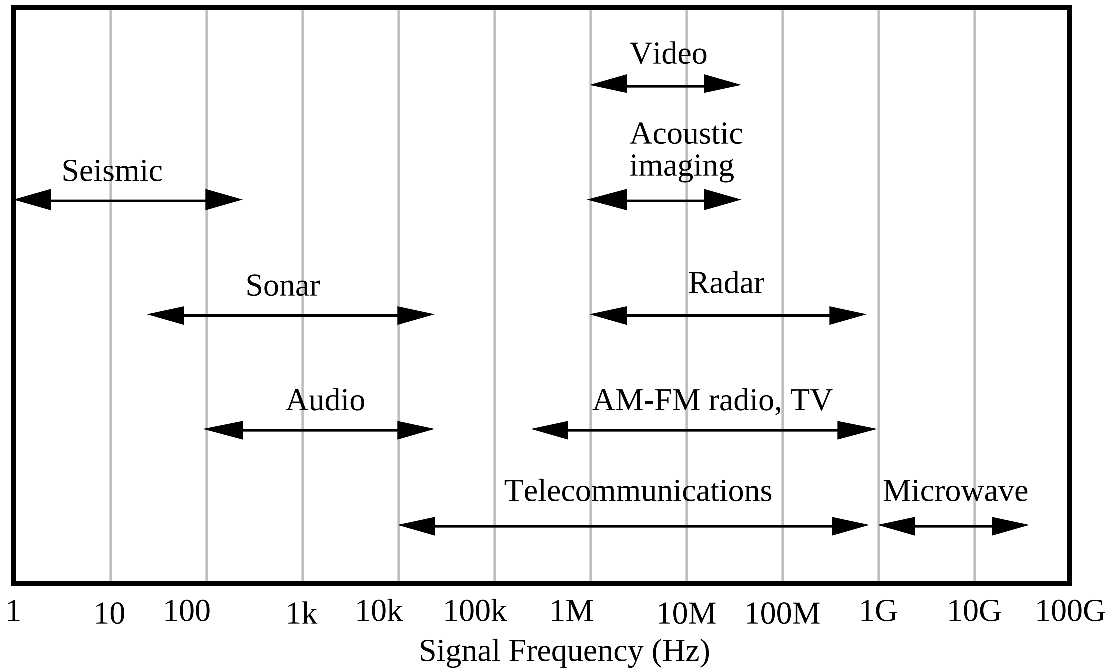


COMPARISON OF ANALOG AND DIGITAL CIRCUITS

Analog Circuits	Digital Circuits
Signals are continuous in amplitude and can be continuous or discrete in time	Signal are discontinuous in amplitude and time - binary signals have two amplitude states
Designed at the circuit level	Designed at the systems level
Components must have a continuum of values	Component have fixed values
Customized	Standard
CAD tools are difficult to apply	CAD tools have been extremely successful
Requires precision modeling	Timing models only
Performance optimized	Programmable by software
Irregular block	Regular blocks
Difficult to route automatically	Easy to route automatically
Dynamic range limited by power supplies and noise (and linearity)	Dynamic range unlimited

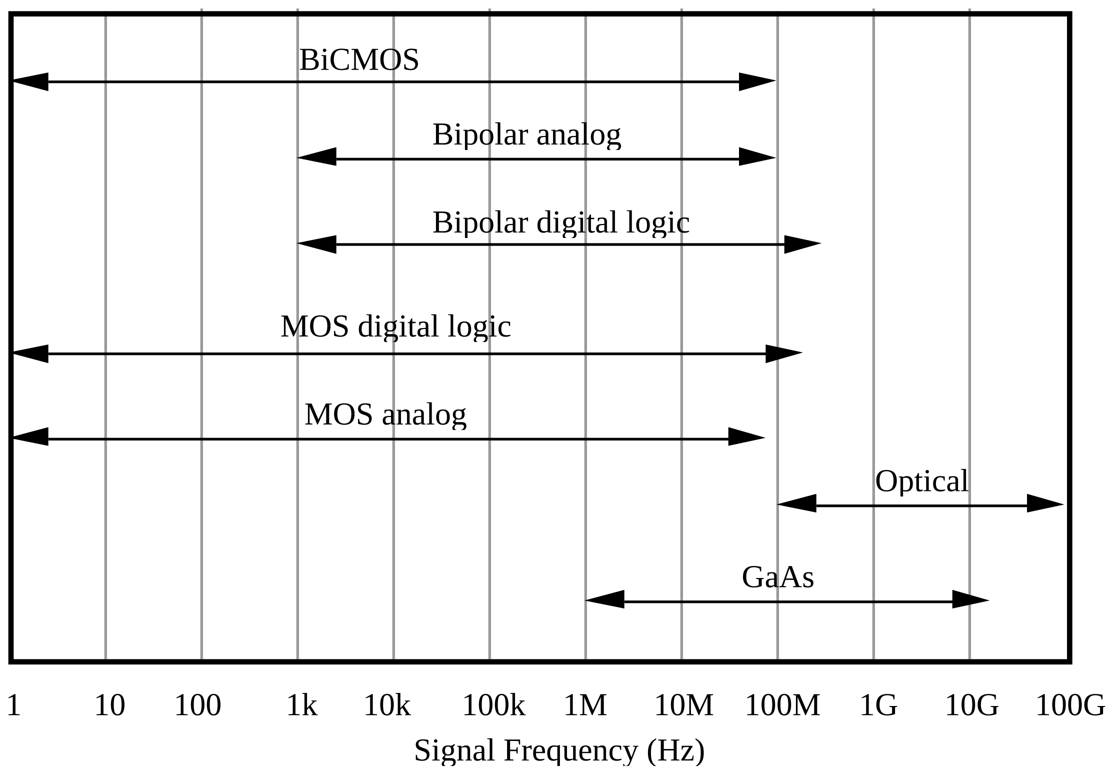
I.3 TECHNOLOGY OVERVIEW

BANDWIDTHS OF SIGNALS USED IN SIGNAL PROCESSING APPLICATIONS



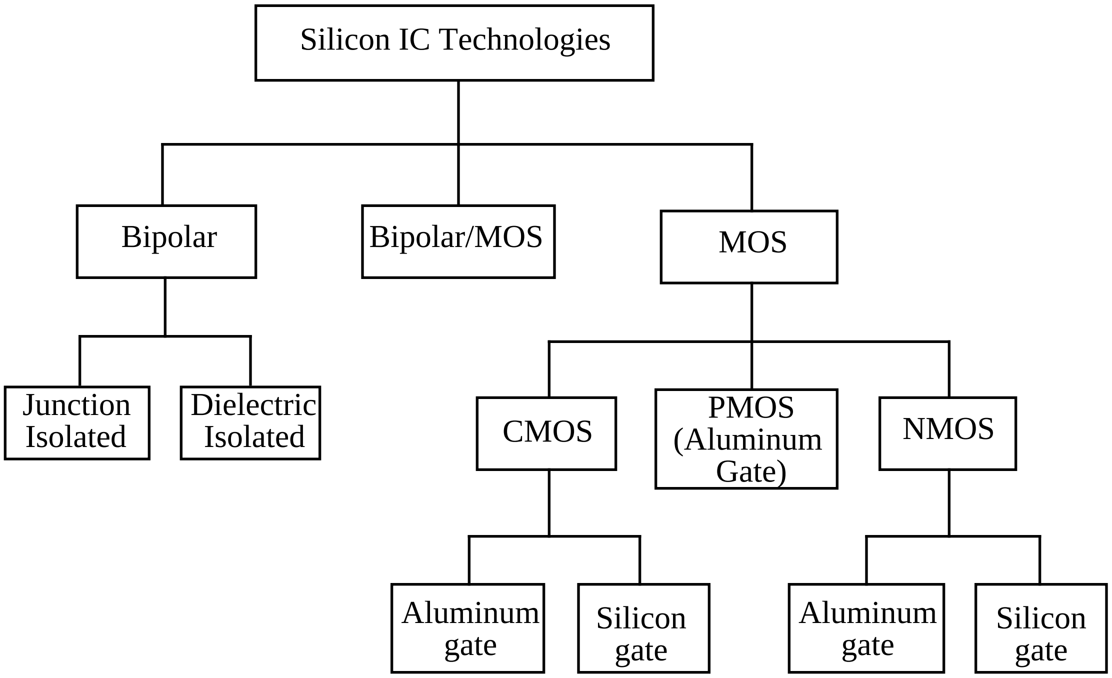
Signal frequency used in signal processing applications.

BANDWIDTHS THAT CAN BE PROCESSED BY PRESENT-DAY TECHNOLOGIES



Frequencies that can be processed by present-day technologies.

CLASSIFICATION OF SILICON TECHNOLOGY



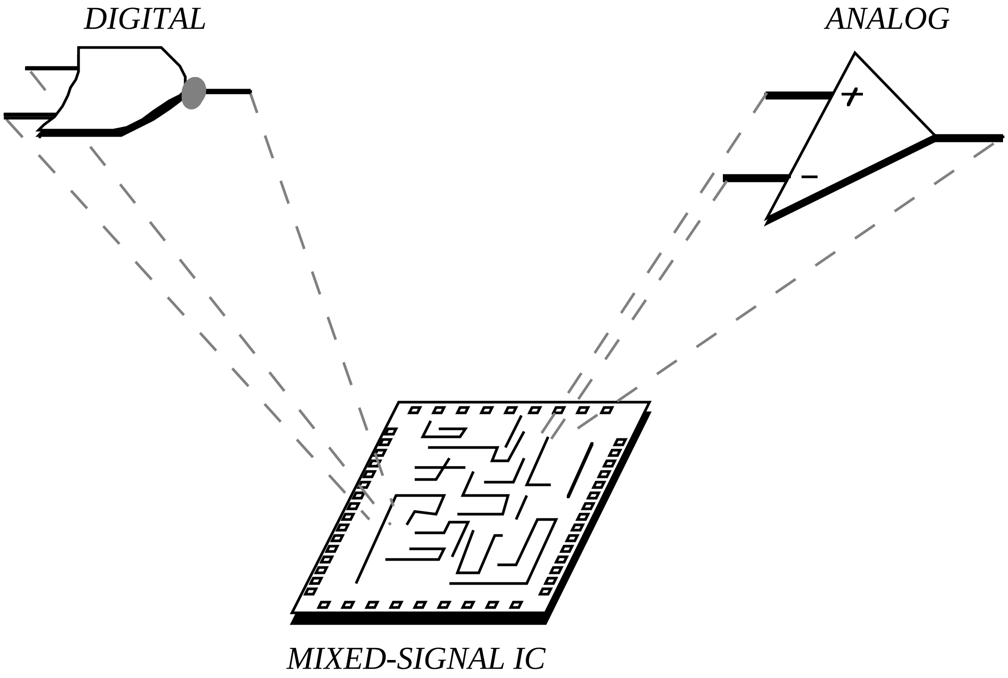
BIPOLAR VS. MOS TRANSISTORS

CATEGORY	BIPOLAR	CMOS
Turn-on Voltage	0.5-0.6 V	0.8-1 V
Saturation Voltage	0.2-0.3 V	0.2-0.8 V
g_m at 100µA	4 mS	0.4 mS (W=10L)
Analog Switch Implementation	Offsets, asymmetric	Good
Power Dissipation	Moderate to high	Low but can be large
Speed	Faster	Fast
Compatible Capacitors	Voltage dependent	Good
AC Performance Dependence	DC variables only	DC variables and geometry
Number of Terminals	3	4
Noise (1/f)	Good	Poor
Noise Thermal	OK	OK
Offset Voltage	< 1 mV	5-10 mV

WHY CMOS???

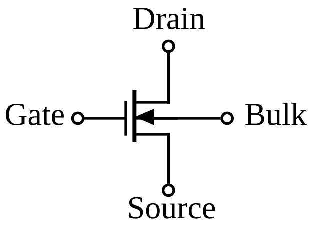
CMOS is nearly ideal for mixed-signal designs:

- Dense digital logic
- High-performance analog

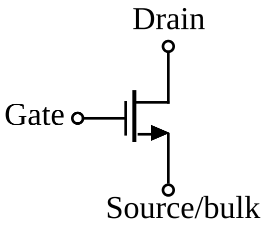


I.4 NOTATION

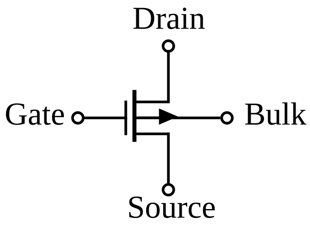
SYMBOLS FOR TRANSISTORS



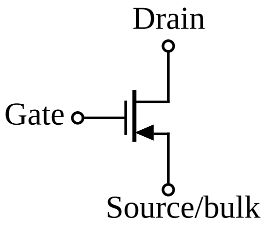
n-channel, enhancement, $V_{BS} \neq 0$



n-channel, enhancement, bulk at most negative supply



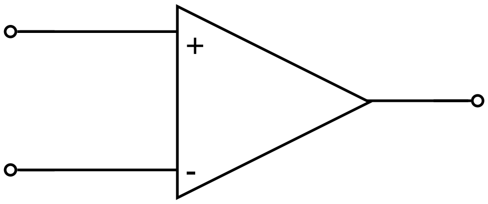
p-channel, enhancement, $V_{BS} \neq 0$

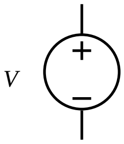


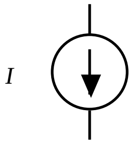
p-channel, enhancement, bulk at most positive supply

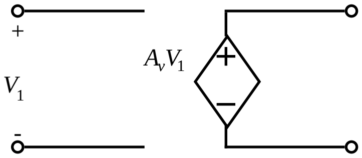
SYMBOLS FOR CIRCUIT ELEMENTS

Operational Amplifier/Amplifier/OTA

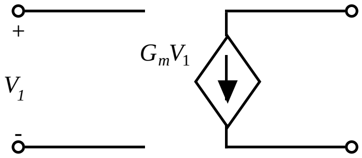




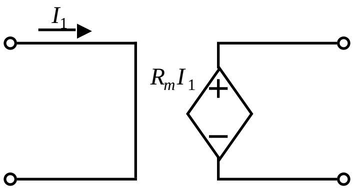




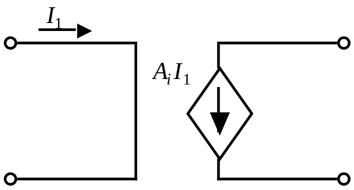
VCVS



VCCS

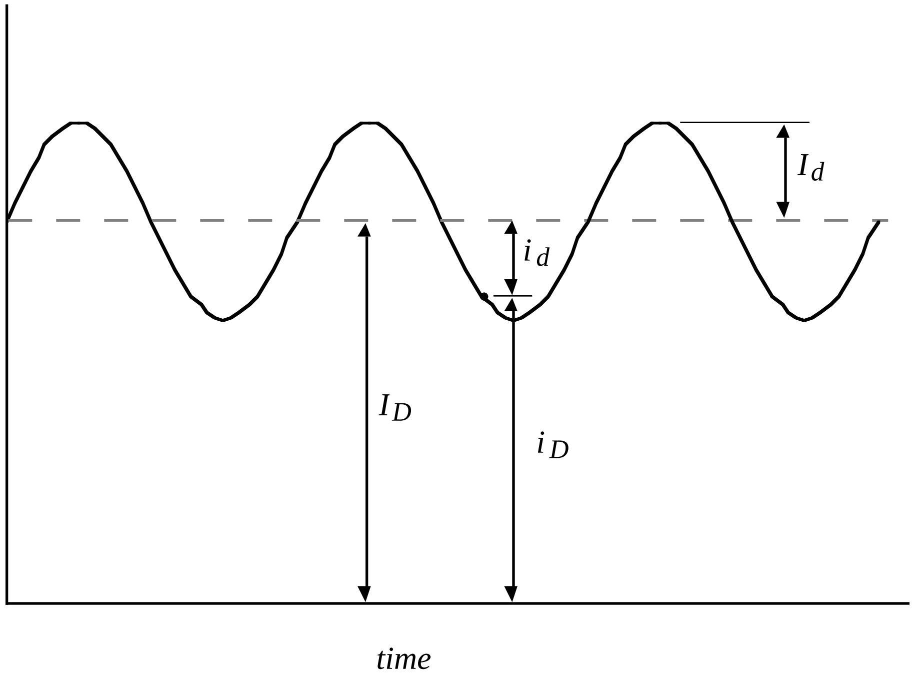


CCVS



CCCS

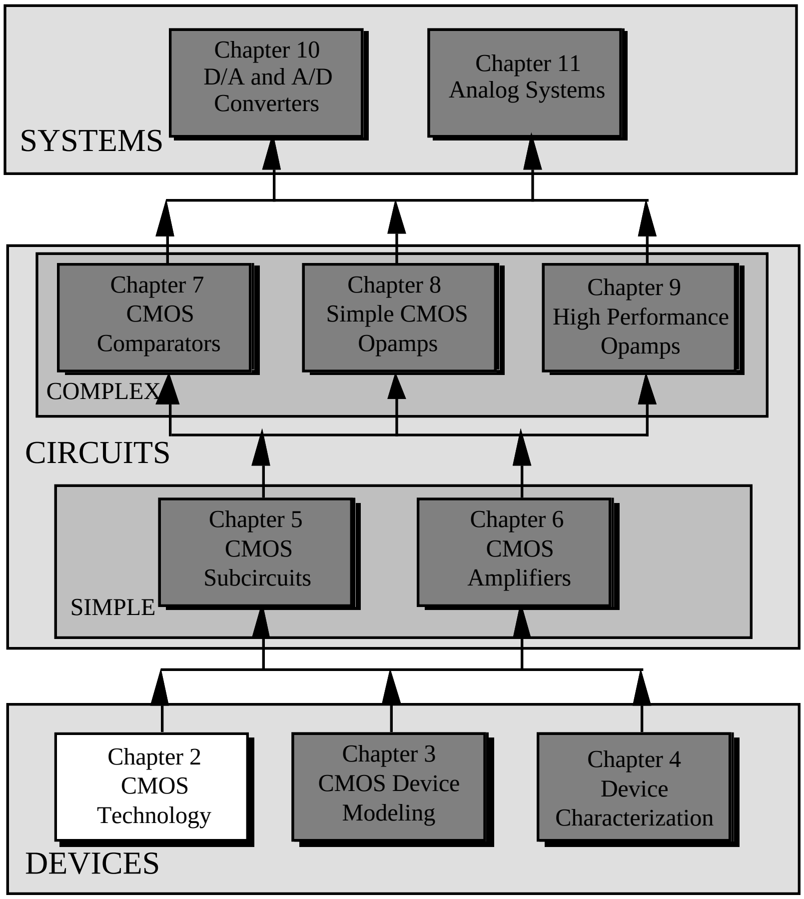
Notation for signals



II. CMOS TECHNOLOGY

Contents

Perspective



OBJECTIVE

- Provide an understanding of CMOS technology sufficient to enhance circuit design.
- Characterize passive components compatible with basic technologies.
- Provide a background for modeling at the circuit level.
- Understand the limits and constraints introduced by technology.

II.1 - BASIC FABRICATION PROCESSES

BASIC FABRTICATION PROCESSES

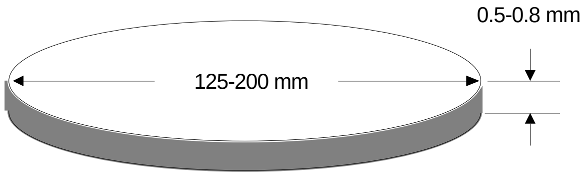
Basic Steps

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching

Photolithography

Means by which the above steps are applied to selected areas of the silicon wafer.

Silicon wafer

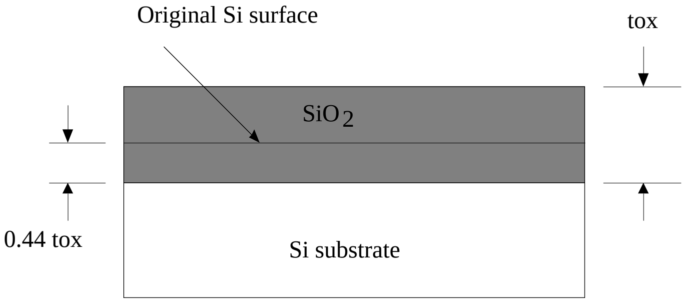


n-type: 3-5 Ω-cm

p-type: 14-16 Ω-cm

Oxidation

The process of growing a layer of silicon dioxide (SiO_2)on the surface of a silicon wafer.

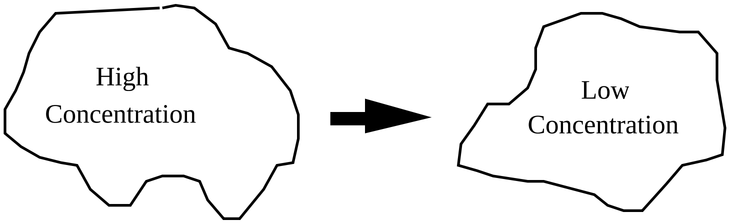


Uses:

- Provide isolation between two layers
- Protect underlying material from contamination
- Very thin oxides (100 to 1000 Å) are grown using dry-oxidation techniques. Thicker oxides (>1000 Å) are grown using wet oxidation techniques.

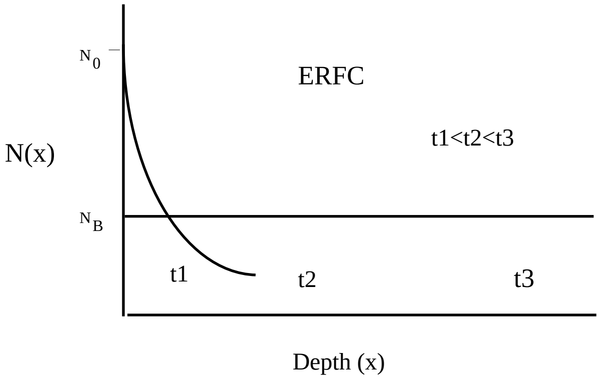
Diffusion

Movement of impurity atoms at the surface of the silicon into the bulk of the silicon - from higher concentration to lower concentration.

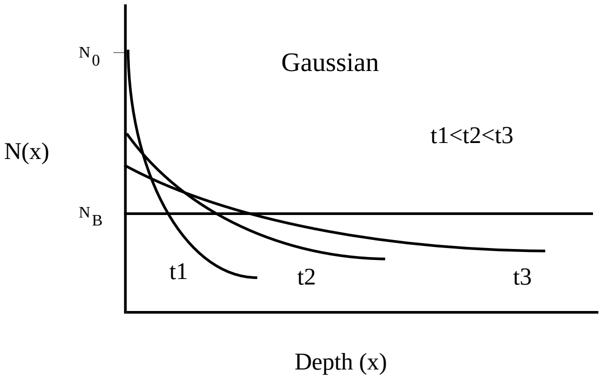


Diffusion typically done at high temperatures: 800 to 1400 °C.

Infinite-source diffusion:

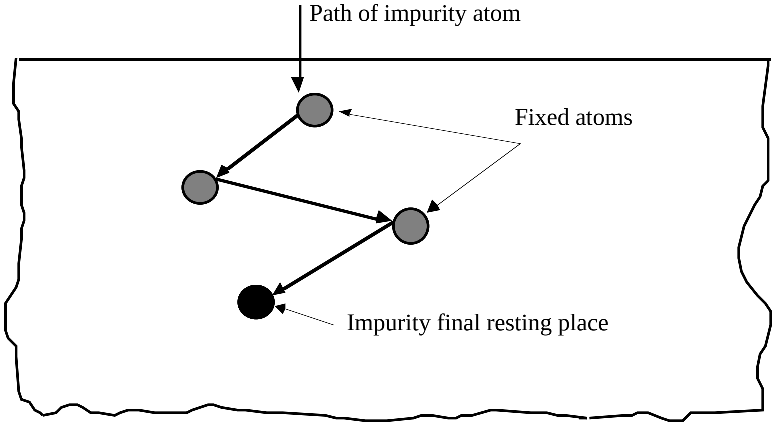


Finite-source diffusion:

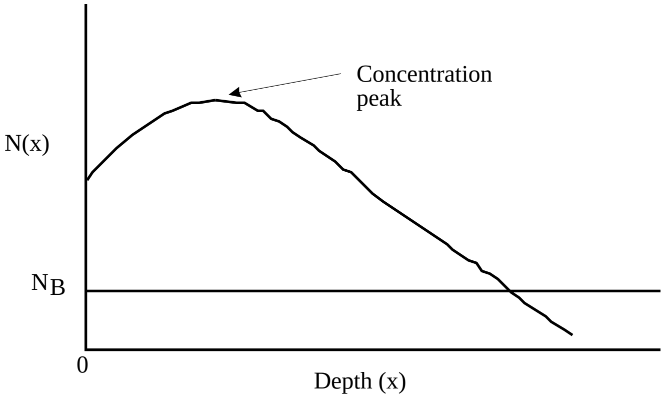


Ion Implantation

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target.



- Anneal required to activate the impurity atoms and repair physical damage to the crystal lattice. This step is done at 500 to 800 °C.
- Lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Unique doping provile available with buried concentration peak.



Deposition

Deposition is the means by which various materials are deposited on the silicon wafer.

Examples:

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Polysilicon

There are various ways to deposit a meterial on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

Materials deposited using these techniques cover the entire wafer.

Etching

Etching is the process of selectively removing a layer of material.

When etching is performed, the etchant may remove portions or all of:

- the desired material
- the underlying layer
- the masking layer

Important considerations:

- Anisotropy of the etch

$$A = 1 - \frac{\text{lateral etch rate}}{\text{vertical etch rate}}$$

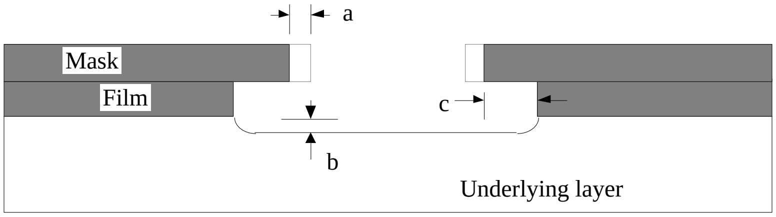
- Selectivity of the etch (film toomask, and film to substrate)

$$S_{\text{film-mask}} = \frac{\text{film etch rate}}{\text{mask etch rate}}$$

Desire perfect anisotropy (A=1) and invinite selectivity.

There are basically two types of etches:

- Wet etch, uses chemicals
- Dry etch, uses chemically active ionized gasses.



Photolithography

Components

- Photoresist material
- Photomask
- Material to be patterned (e.g., SiO_2)

Positive photoresist-

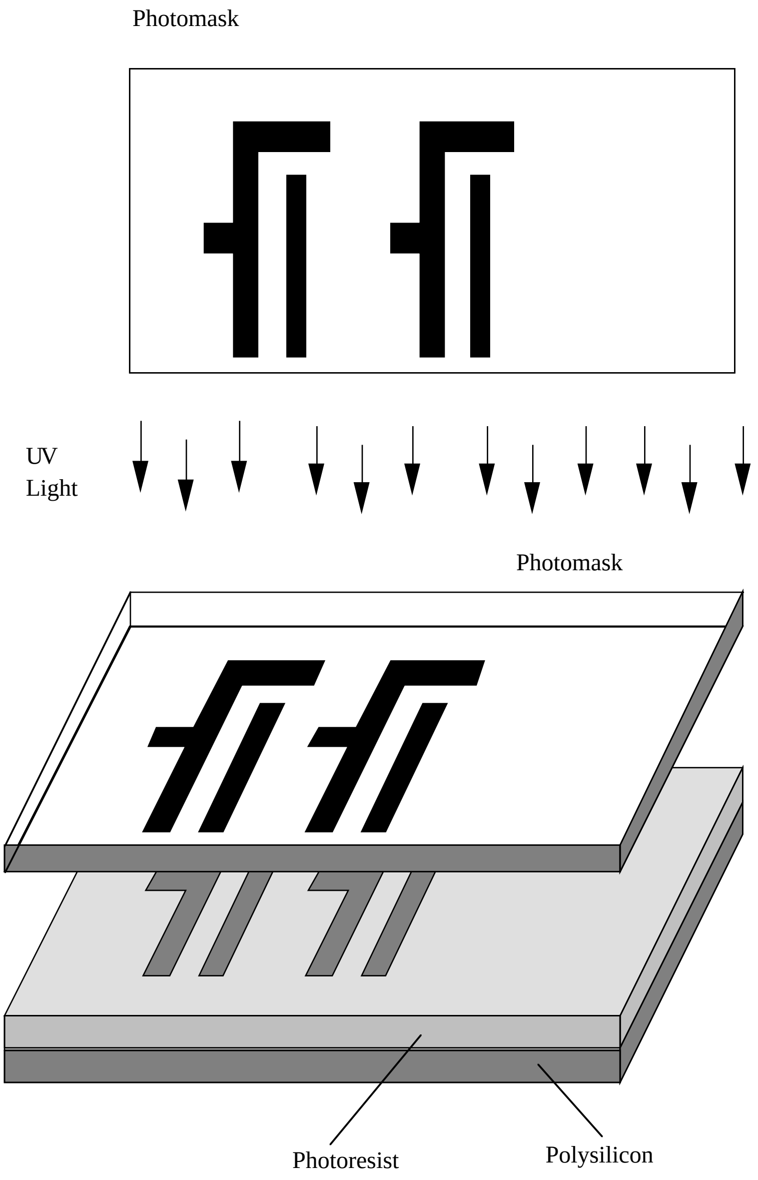
Areas exposed to UV light are soluble in the developer

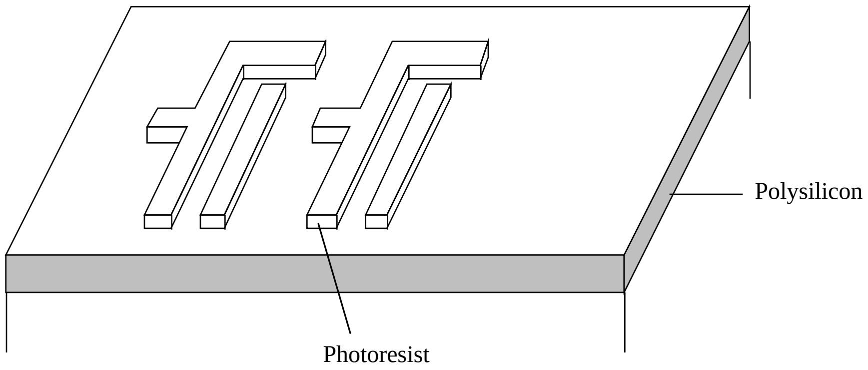
Negative photoresist-

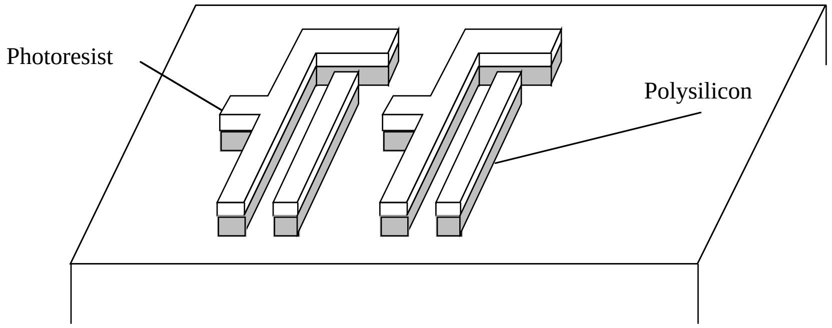
Areas not exposed to UV light are soluble in the developer

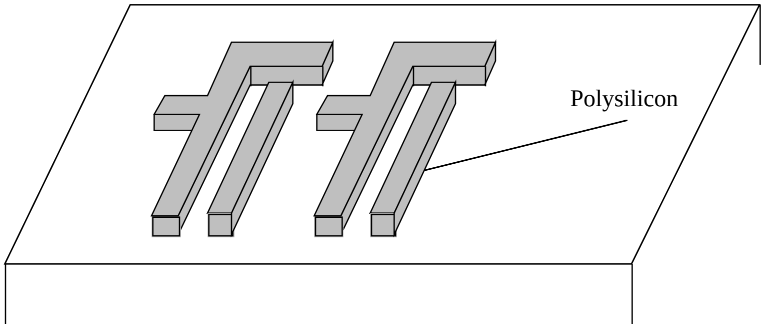
Steps:

1. Apply photoresist
2. Soft bake
3. Expose the photoresist to UV light through photomask
4. Develop (remove unwanted photoresist)
5. Hard bake
6. Etch the exposed layer
7. Remove photoresist


Photomask
UV
Light
Photomask
Photoresist
Polysilicon







Positive Photoresist

II.2 - CMOS TECHNOLOGY

TWIN-WELL CMOS TECHNOLOGY

Features

- Two layers of metal connections, both of them of high quality due to a planarization step.
- Optimal threshold voltages of both p-channel and n-channel transistors
- Lightly doped drain (LDD) transistors prevent hot-electron effects.
- Good latchup protection

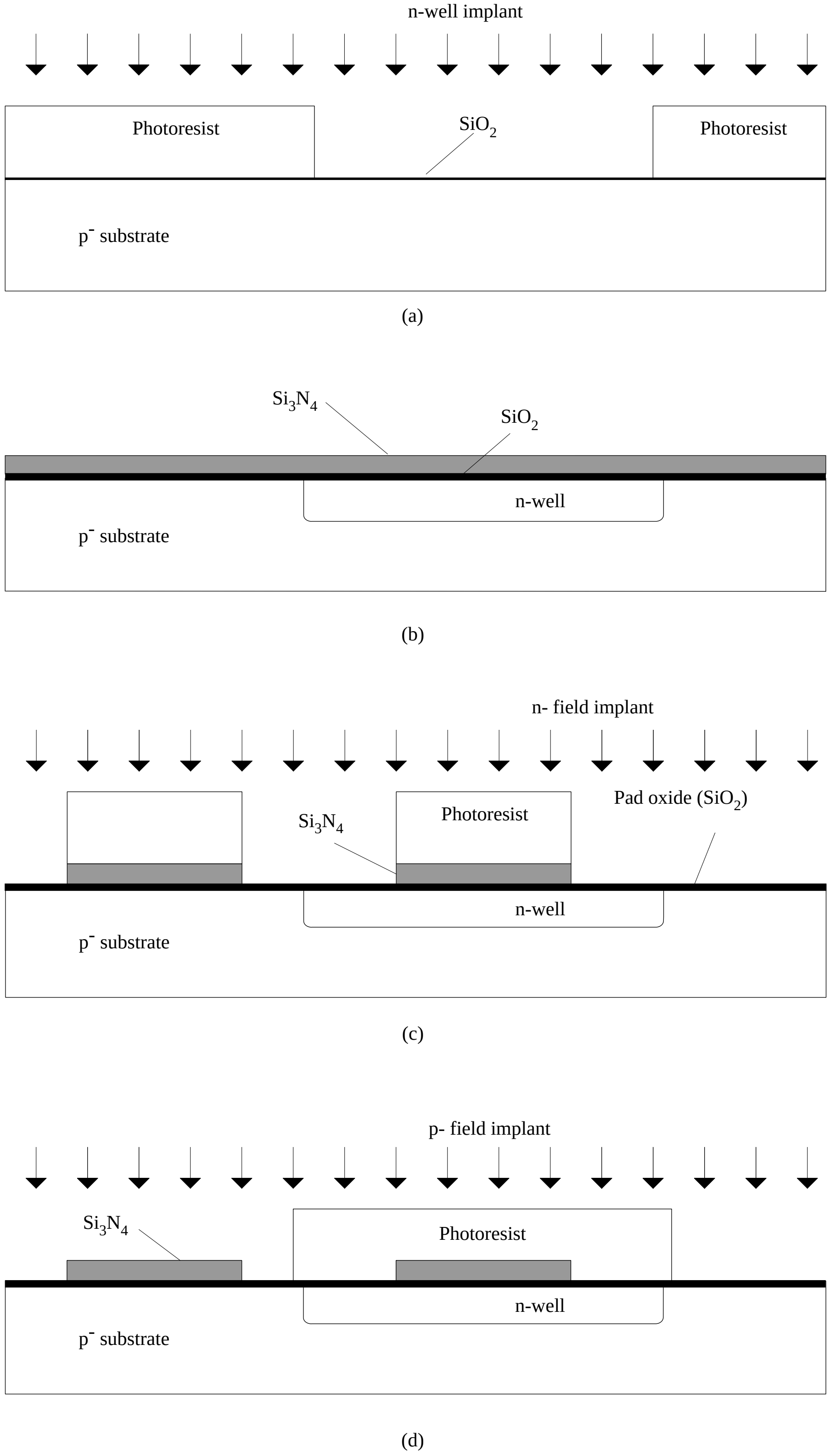
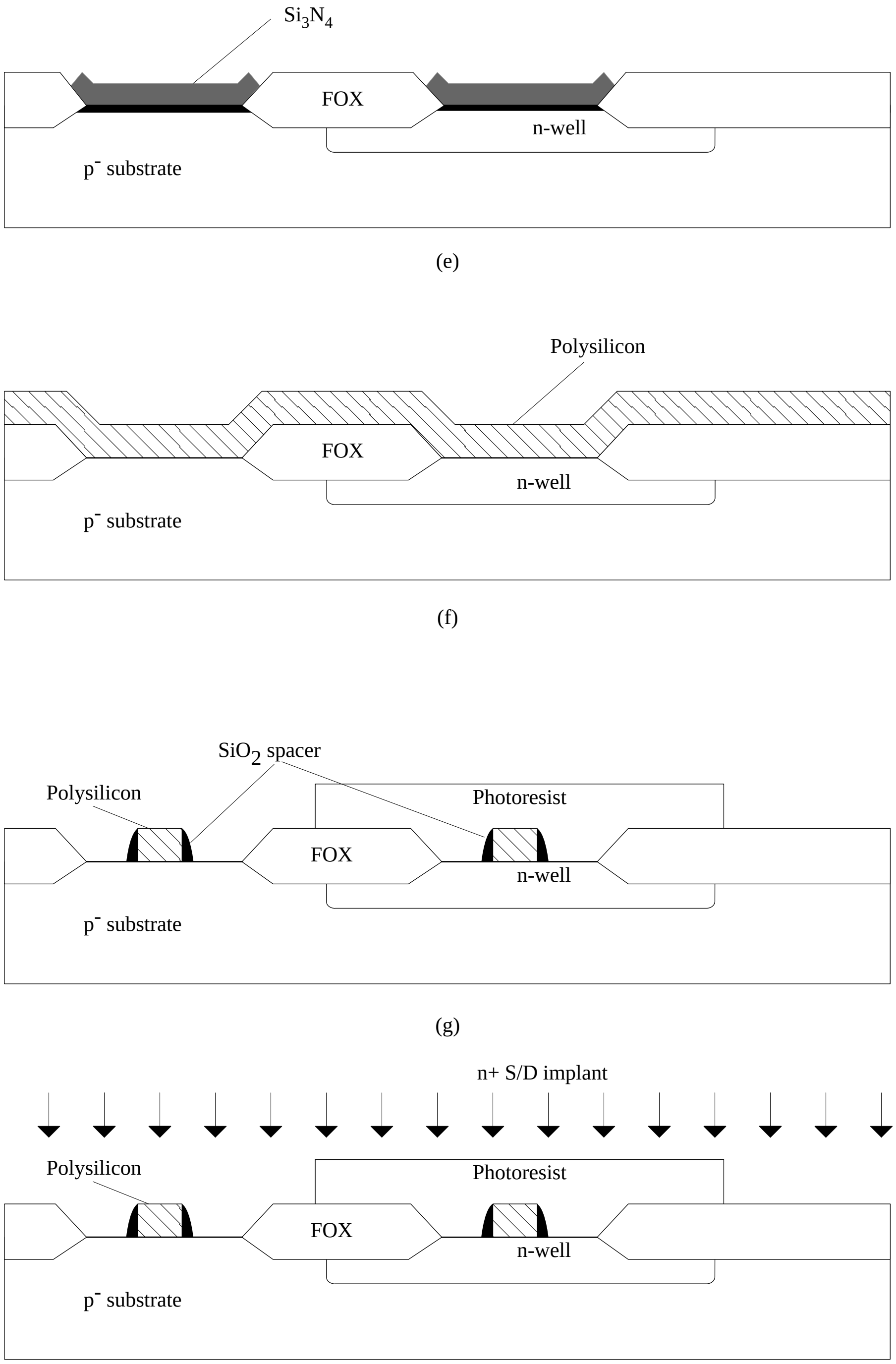


Figure 2.1-5 The major CMOS process steps.



(e)

(f)

(g)

(h)

Figure 2.1-5 The major CMOS process steps (cont'd).

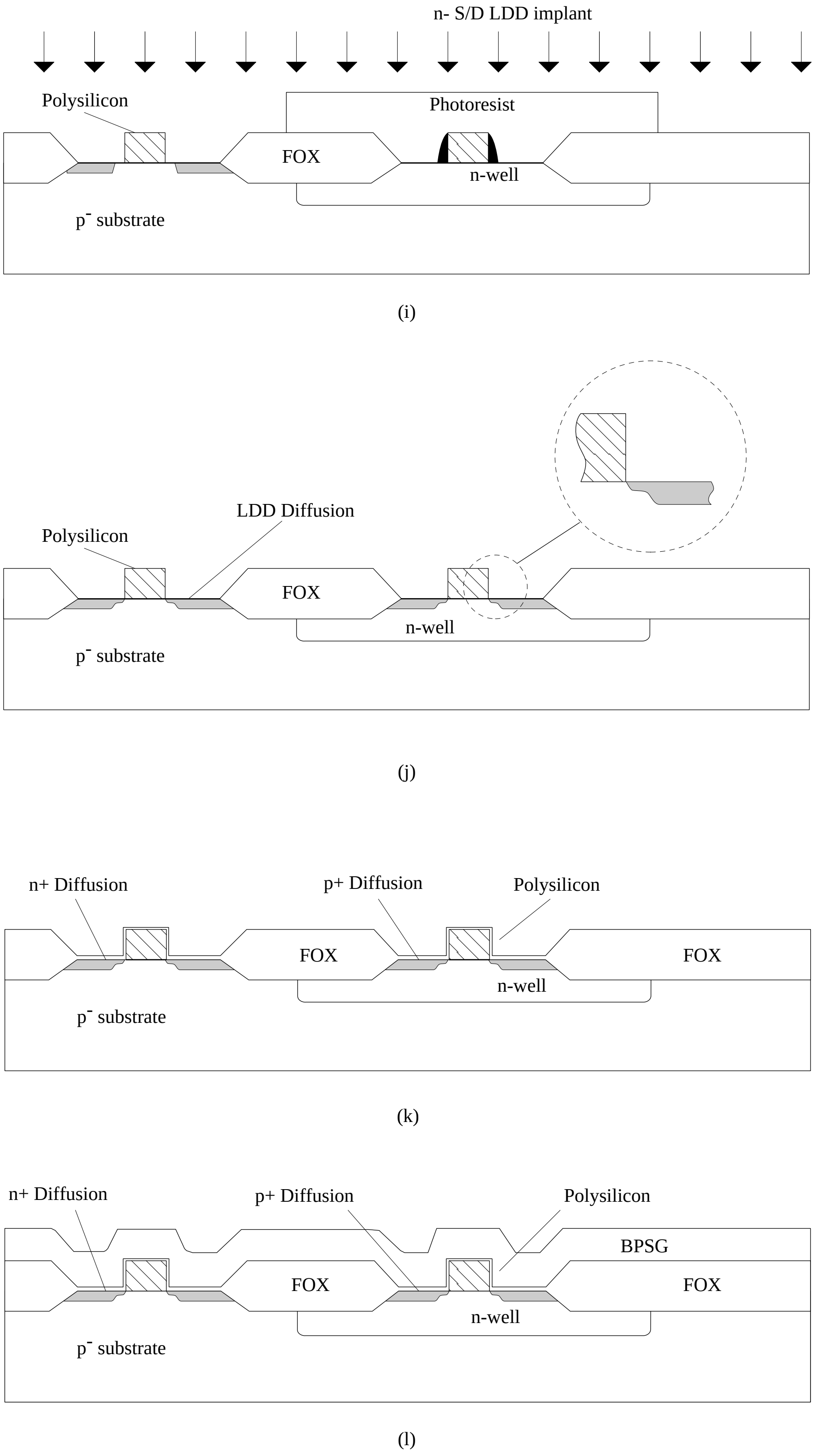
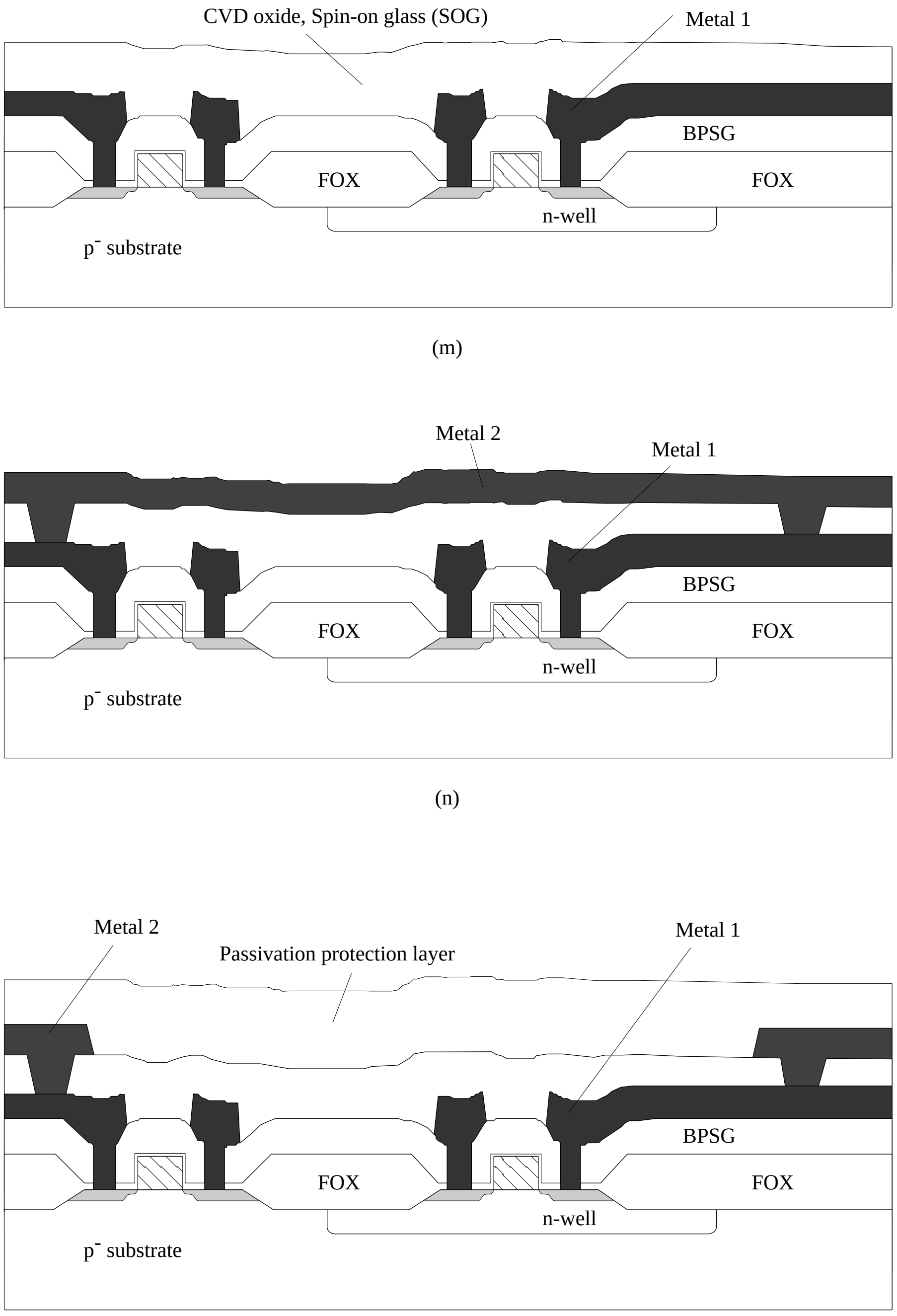


Figure 2.1-5 The major CMOS process steps (cont'd).



(m)

(n)

(o)

Figure 2.1-5 The major CMOS process steps (cont'd).

Silicide/Salicide

Purpose

- Reduce interconnect resistance,

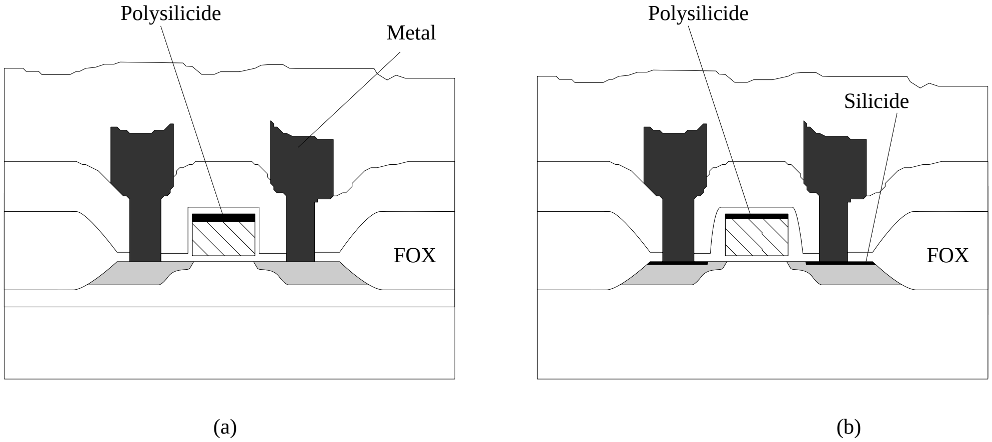
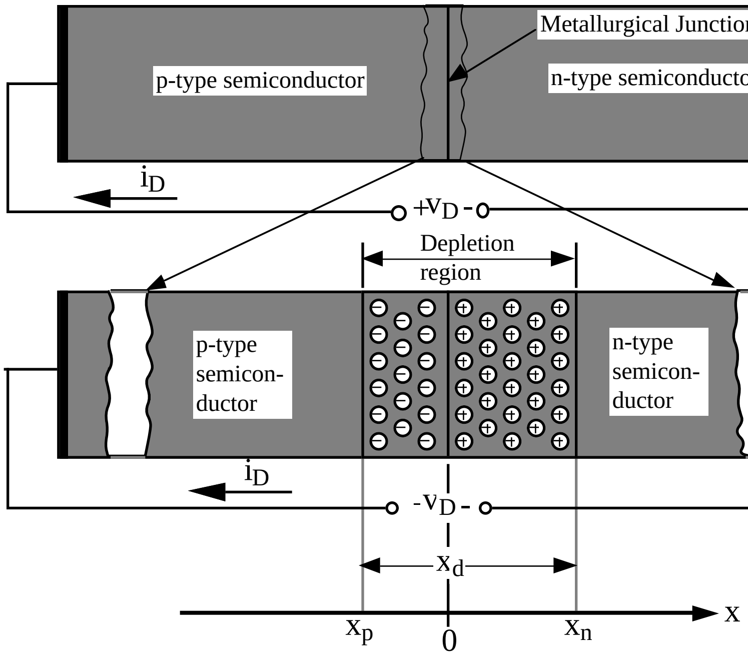


Figure 2.1-6 (a) Polycice structure and (b) Salicide structure.

II.3 - PN JUNCTION

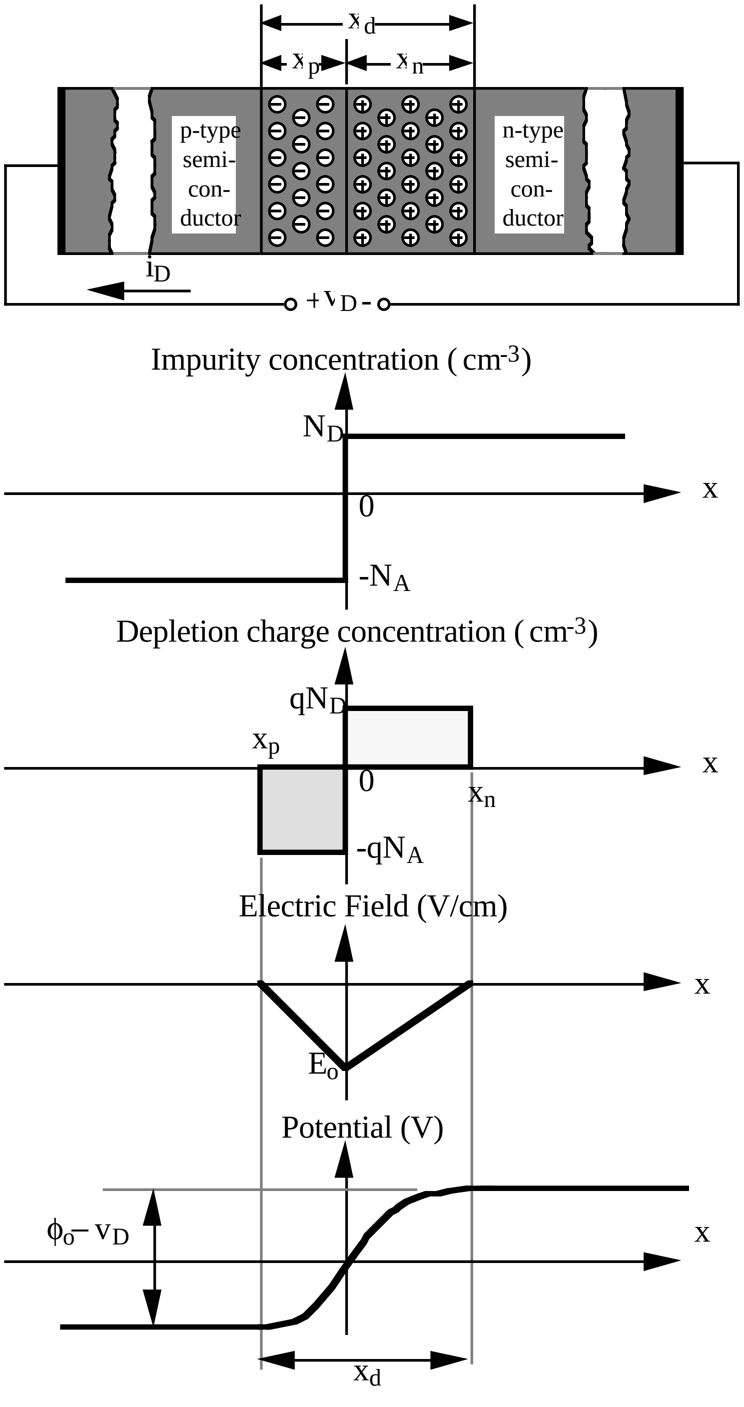
CONCEPT



1. Doped atoms near the metallurgical junction lose their free carriers by diffusion.
2. As these fixed atoms lose their free carriers, they build up an electric field which opposes the diffusion mechanism.
3. Equilibrium conditions are reached when:

> Current due to diffusion = Current due to electric field

PN JUNCTION CHARACTERIZATION



SUMMARY OF PN JUNCTION ANALYSIS

Barrier potential-

$$\phi_o = \frac{kT}{q} \ln\left[\frac{N_A N_D}{n_i^2}\right] = V_t \ln\left[\frac{N_A N_D}{n_i^2}\right]$$

Depletion region widths-

$$\left.\begin{aligned} x_n &= \sqrt{\frac{2\varepsilon_{si}(\phi_o - v_D)N_A}{qN_D(N_A+N_D)}} \\ x_p &= \sqrt{\frac{2\varepsilon_{si}(\phi_o - v_D)N_D}{qN_D(N_A+N_D)}} \end{aligned}\right\} \quad x \propto \sqrt{\frac{1}{N}}$$

Depletion capacitance-

$$C_j = A\sqrt{\frac{\varepsilon_{si} q N_A N_D}{2(N_A+N_D)}} \; \frac{1}{\sqrt{\phi_o - v_D}} = \frac{C_{j0}}{\sqrt{\phi_o - v_D}}$$

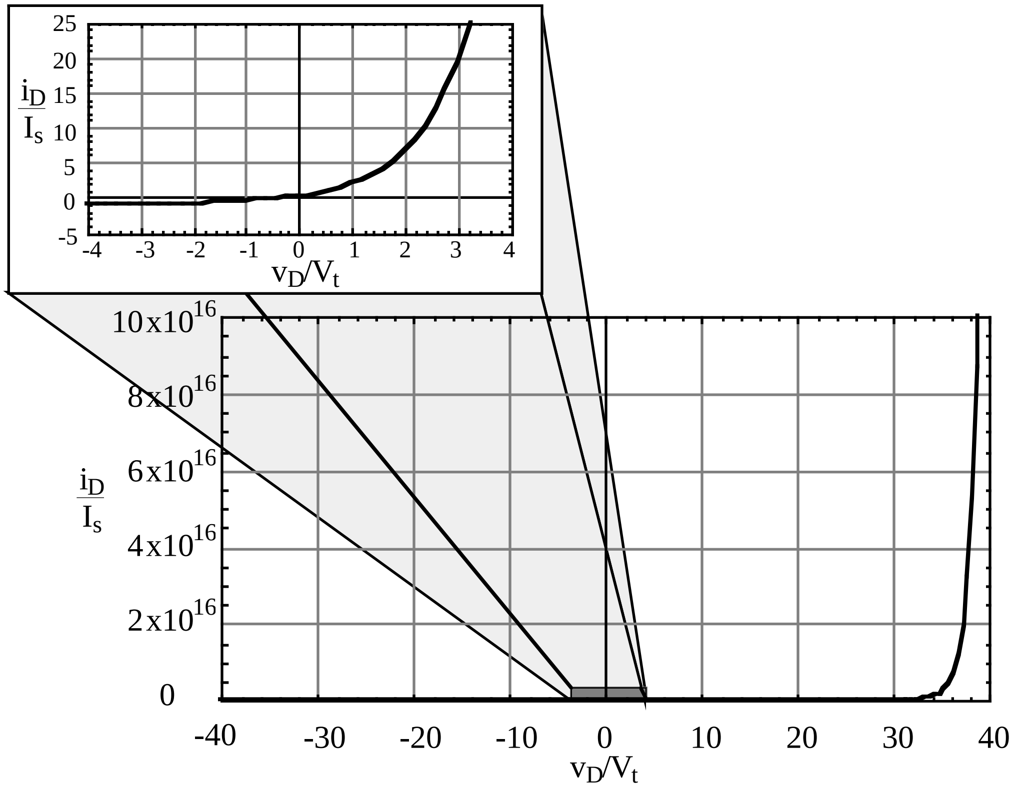
Breakdown voltage-

$$BV = \frac{\varepsilon_{si}(N_A+N_D)}{2qN_A N_D} \; E_{max}^2$$

SUMMARY - CONTINUED

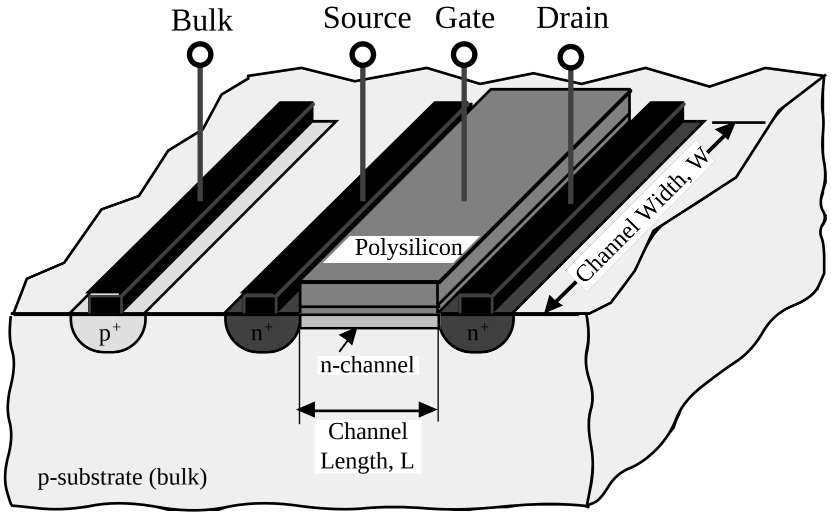
Current-Voltage Relationship-

$$i_D = I_s\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \quad \text{where} \quad I_s = qA\left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right]$$



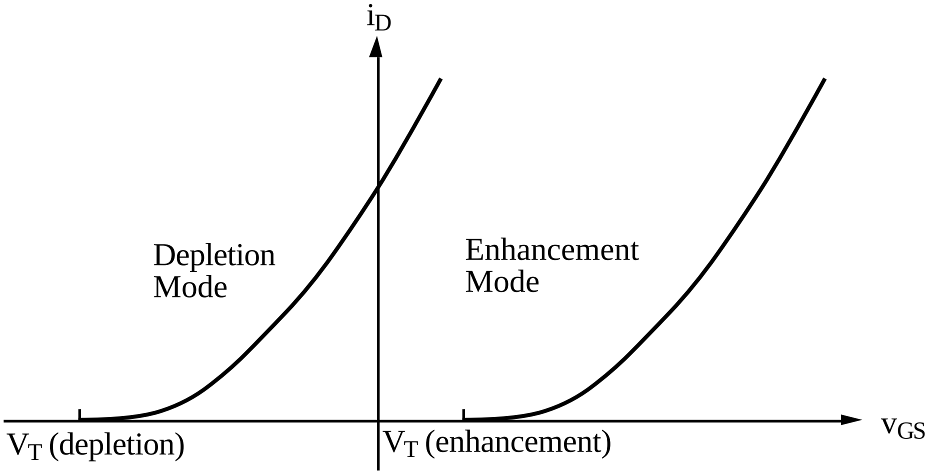
II.4 - MOS TRANSISTOR

ILLUSTRATION



$$t_{OX} = 200 \text{ Angstroms} = 0.2\text{x}10^{-7} \text{ meters} = 0.02\ \mu\text{m}$$

TYPES OF TRANSISTORS



CMOS TRANSISTOR

N-well process

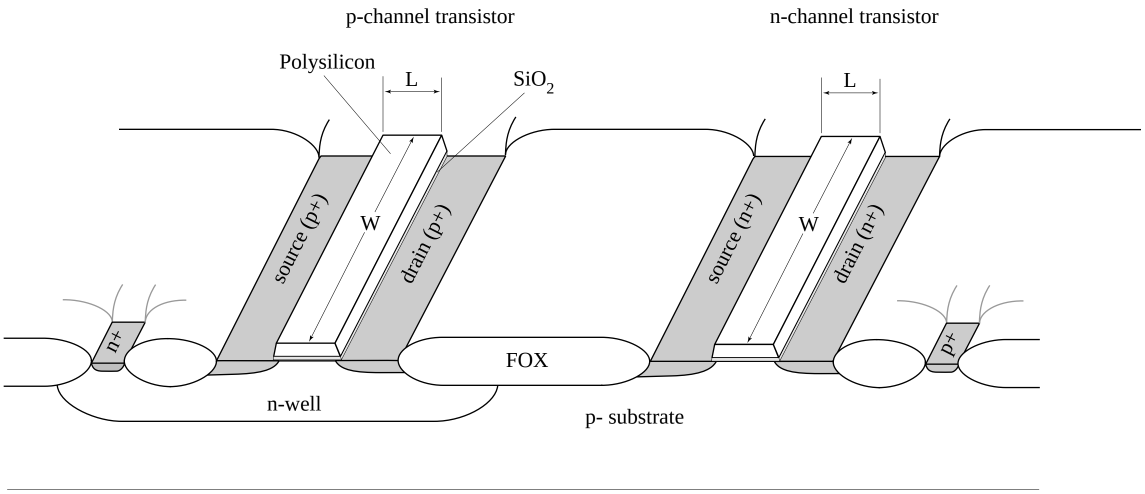


Figure 2.3-1 Physical structure of an n-channel and p-channel transistor in an n-well technology.

P-well process

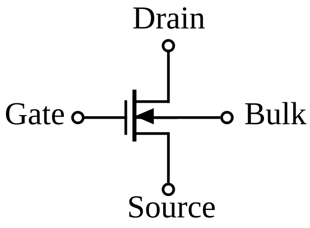
- Inverse of the above.

Normally, all transistors are enhancement mode.

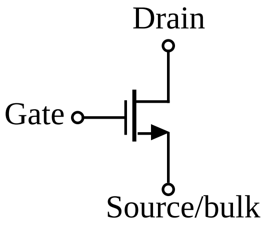
TRANSISTOR OPERATING POLARTIES

Type of Device	Polarity of v_{GS} and V_T	Polarity of v_{DS}	Polarity of v_{BULK}
n-channel, enhancement	+	+	Most negative
n-channel, depletion	-	+	Most negative
p-channel, enhancement	-	-	Most positive
p-channel, depletion	+	-	Most positive

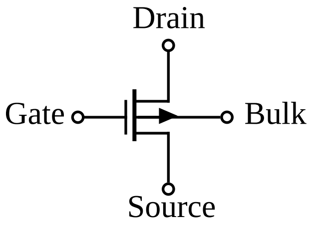
SYMBOLS FOR TRANSISTORS



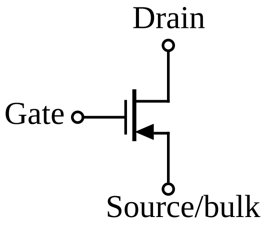
n-channel, enhancement, $V_{BS} \neq 0$



n-channel, enhancement, bulk at most negative supply



p-channel, enhancement, $V_{BS} \neq 0$



p-channel, enhancement, bulk at most positive supply

II.5 - PASSIVE COMPONENTS CAPACITORS

$$C = \frac{\varepsilon_{ox}A}{tox}$$

Polysilicon-Oxide-Channel Capacitor and Polysilicon-Oxide-Polysilicon Capacitor

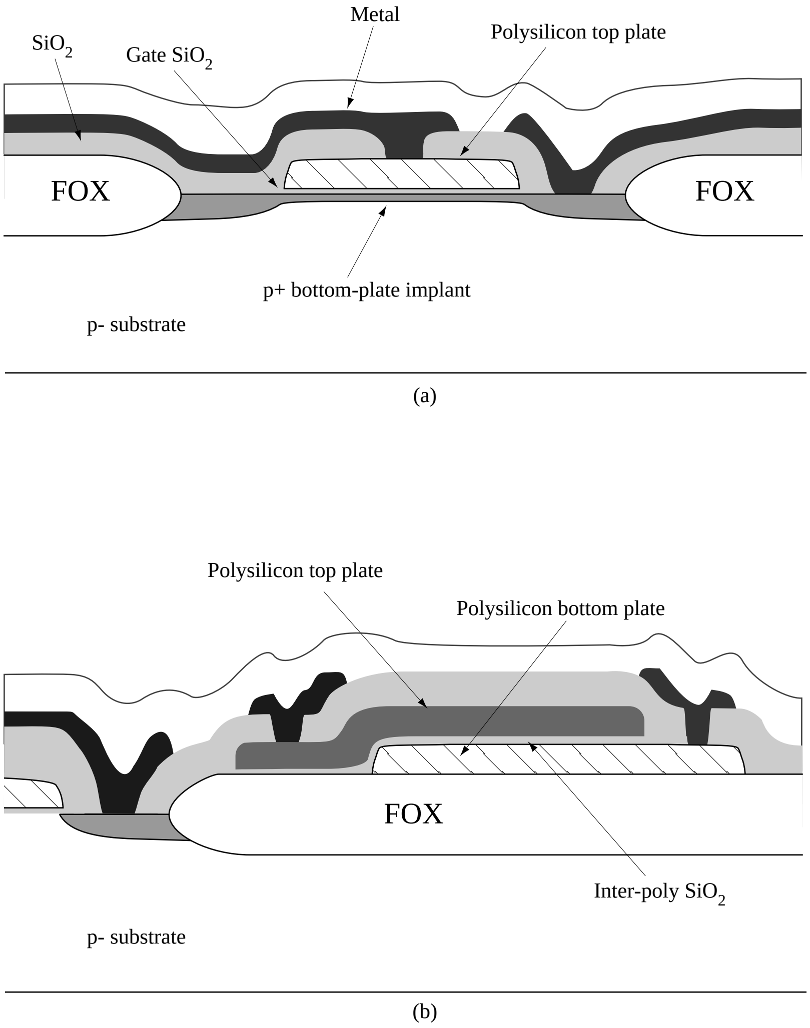


Figure 2.4-1 MOS capacitors. (a) Polysilicon-oxide-channel. (b) Polysilicon-oxide-polysilicon.

Metal-Metal and Metal-Metal-Poly Capacitors

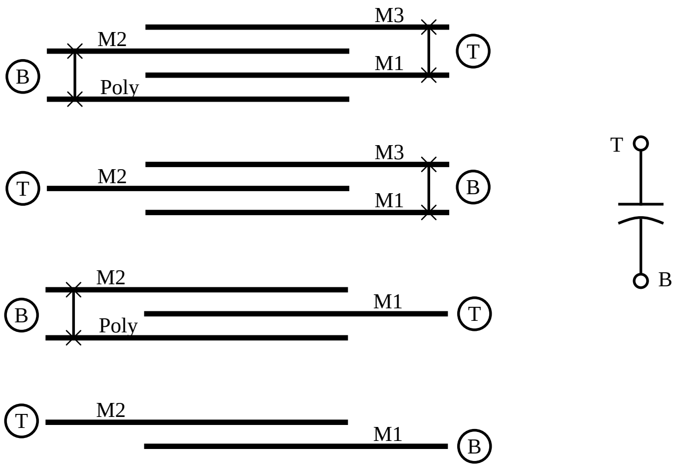


Figure 2.4-2 Various ways to implement capacitors using available interconnect layers. M1, M2, and M3 represent the first, second, and third metal layers respectively.

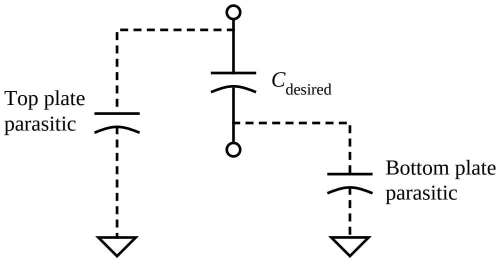


Figure 2.4-3 A model for the integrated capacitors showing top and bottom plate parasitics.

PROPER LAYOUT OF CAPACITORS

- Use “unit” capacitors
- Use “common centroid”

Want A=2*B

Case (a) fails

Case (b) succeeds!

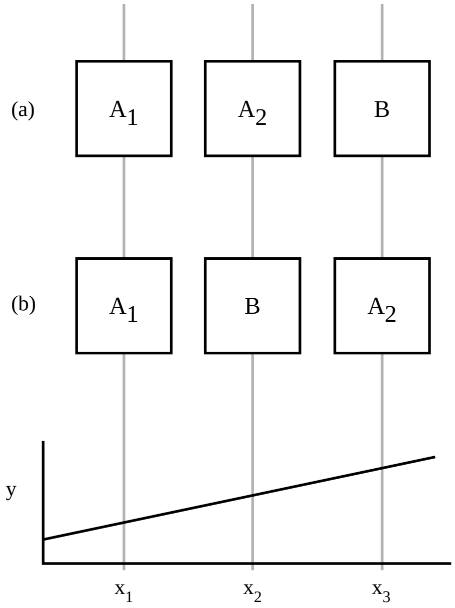
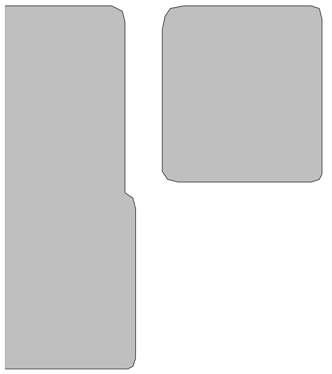
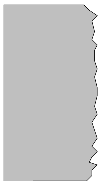


Figure 2.6-2 Components placed in the presence of a gradient, (a) without common-centroid layout and (b) with common-centroid layout.

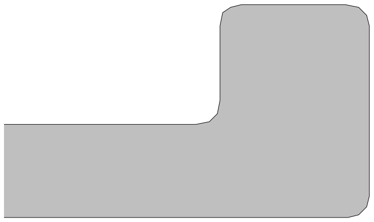
NON-UNIFORM UNDERCUTTING EFFECTS



Large-scale distortion



Random edge distortion



Corner-rounding distortion

VICINITY EFFECT

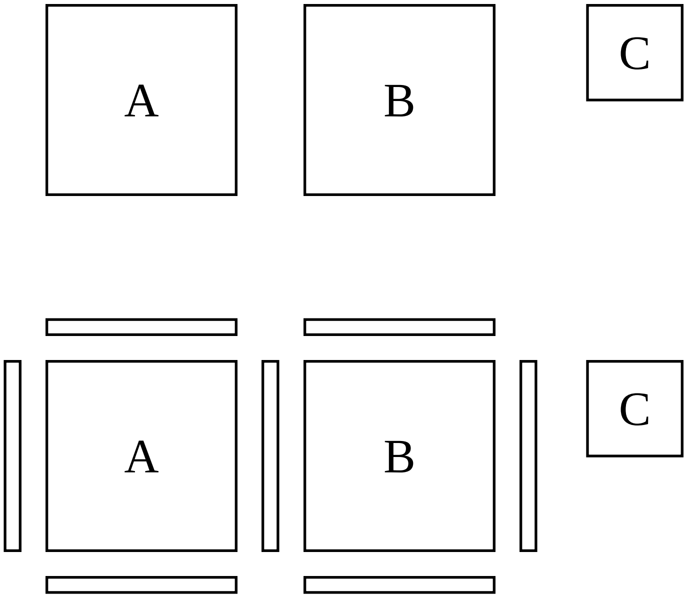
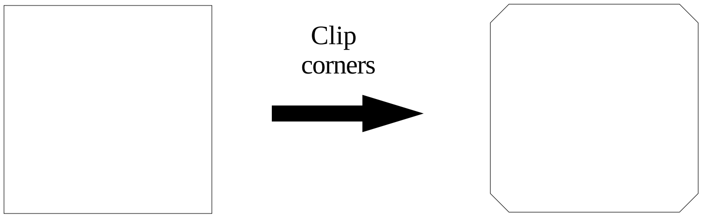


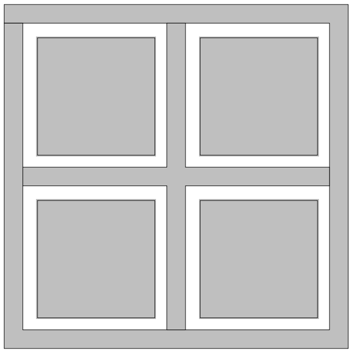
Figure 2.6-1 (a)Illustration of how matching of A and B is disturbed by the presence of C. (b) Improved matching achieved by matching surroundings of A and B

IMPROVED LAYOUT METHODS FOR CAPACITORS

Corner clipping:



Street-effect compensation:



ERRORS IN CAPACITOR RATIOS

Let C_1 be defined as

$$C_1 = C_{1A} + C_{1P}$$

and C_2 be defined as

$$C_2 = C_{2A} + C_{2P}$$

C_{XA} is the bottom-plate capacitance
C_{XP} is the fringe (peripheral) capacitance

$C_{XA} >> C_{XP}$

The ratio of C_2 to C_1 can be expressed as

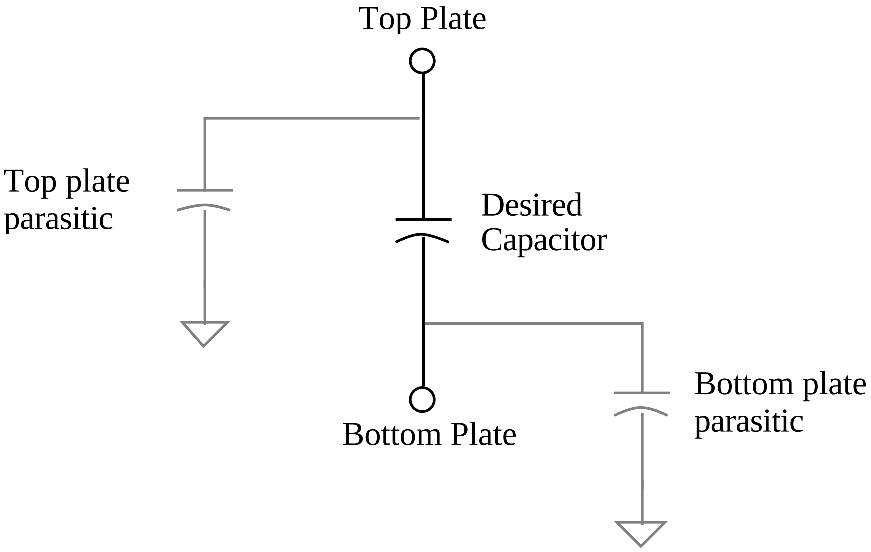
$$\frac{C_2}{C_1} = \frac{C_{2A} + C_{2P}}{C_{1A} + C_{1P}} = \frac{C_{2A}}{C_{1A}}\left[\frac{1 + \frac{C_{2P}}{C_{2A}}}{1 + \frac{C_{1P}}{C_{1A}}}\right]$$

$$\cong \frac{C_{2A}}{C_{1A}}\left[1 + \frac{C_{2P}}{C_{2A}} - \frac{C_{1P}}{C_{1A}} - \frac{(C_{1P})(C_{2P})}{C_{1A}C_{2A}}\right]$$

$$\cong \frac{C_{2A}}{C_{1A}}\left[1 + \frac{C_{2P}}{C_{2A}} - \frac{C_{1P}}{C_{1A}}\right]$$

Thus best matching is achieved when the area to periphery ratio remains constant.

CAPACITOR PARASITICS



Parasitic is dependent upon how the capacitor is constructed.

Typical capacitor performance

(0.8μm Technology)

Capacitor Type	Range of Values	Relative Accuracy	Temperature Coefficient	Voltage Coefficient	Absolute Accuracy
Poly/poly capacitor	0.8-1.0 fF/μm^2	0.05%	50 ppm/°C	50 ppm/V	±10%
MOS capacitor	2.2-2.5 fF/μm^2	0.05%	50 ppm/°C	50 ppm/V	±10%
MOM capacitor	0.02-0.03 fF/μm^2	1.5%			±10%

RESISTORS IN CMOS TECHNOLOGY

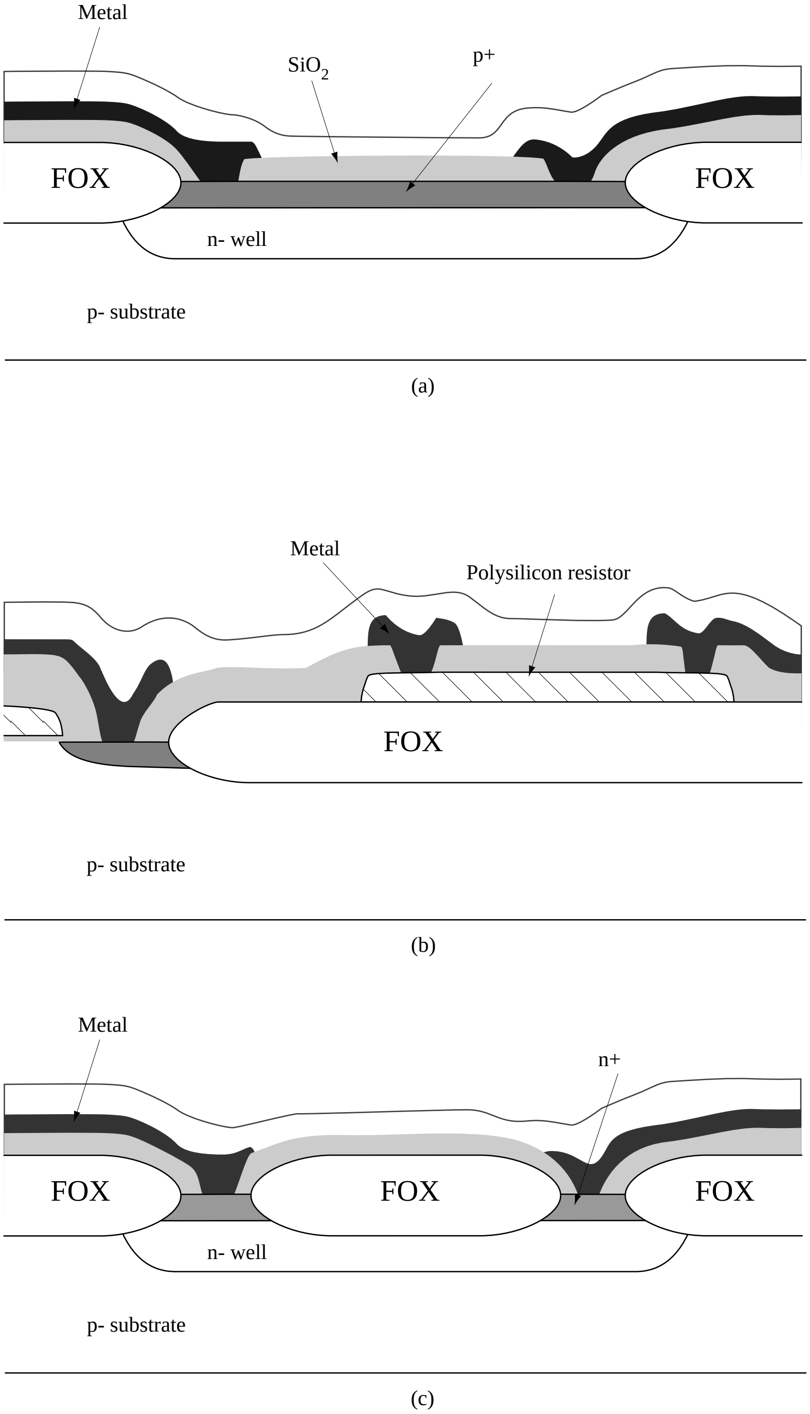


Figure 2.4-4 Resistors. (a) Diffused (b) Polysilicon (c) N-well

PASSIVE COMPONENT SUMMARY

(0.8μm Technology)

Component Type	Range of Values	Matching Accuracy	Temperature Coefficient	Voltage Coefficient	Absolute Accuracy
Poly/poly capacitor	0.8-1.0 fF/μm^2	0.05%	50 ppm/°C	50ppm/V	±10%
MOS capacitor	2.2-2.5 fF/μm^2	0.05%	50 ppm/°C	50ppm/V	±10%
MOM capacitor	0.02-0.03 fF/μm^2	1.5%			±10%
Diffused resistor	20-150 Ω/sq.	0.4%	1500 ppm/°C	200ppm/V	±35%
Polysilicide R	2-15 Ω/sq.				
Poly resistor	20-40 Ω/sq.	0.4%	1500 ppm/°C	100ppm/V	±30%
N-well resistor	1-2k Ω/sq.	0.4%	8000 ppm/°C	10k ppm/V	±40%

BIPOLARS IN CMOS TECHNOLOGY

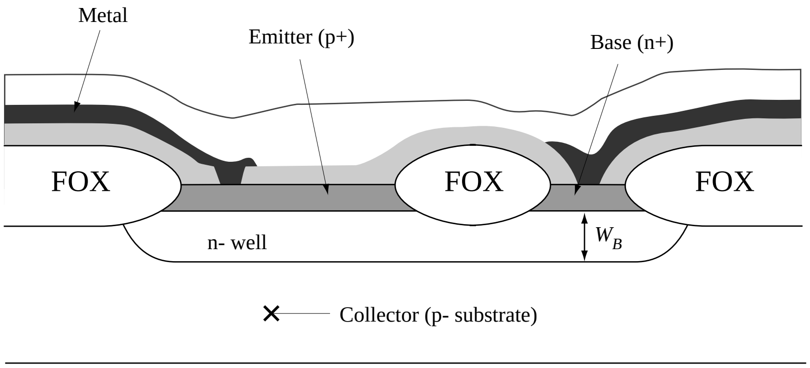


Figure 2.5-1 Substrate BJT available from a bulk CMOS process.

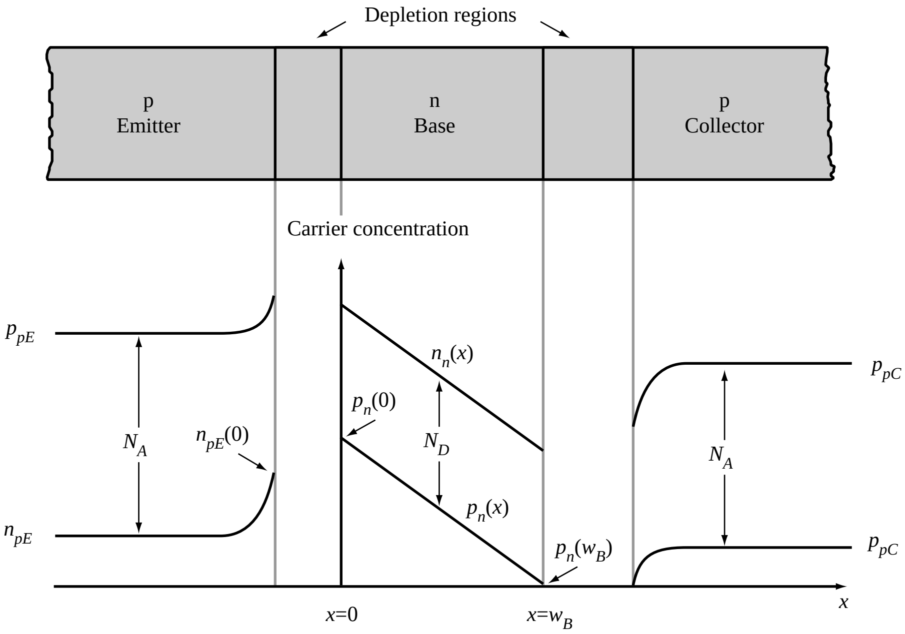
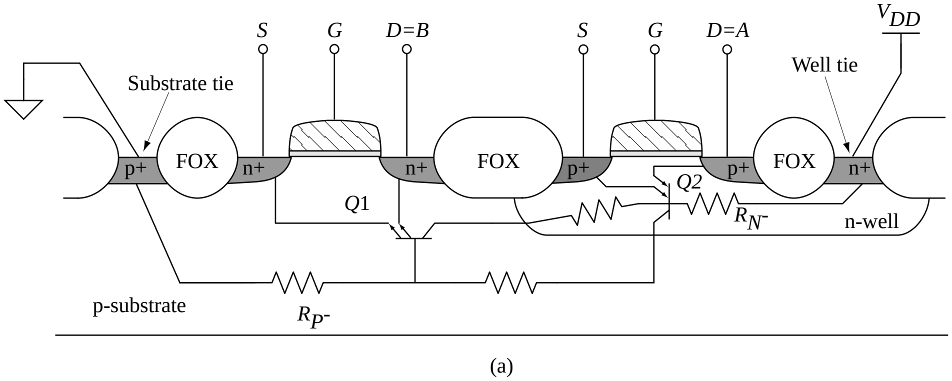


Figure 2.5-2 Minority carrier concentrations for a bipolar junction transistor.

II.6 - LATCHUP



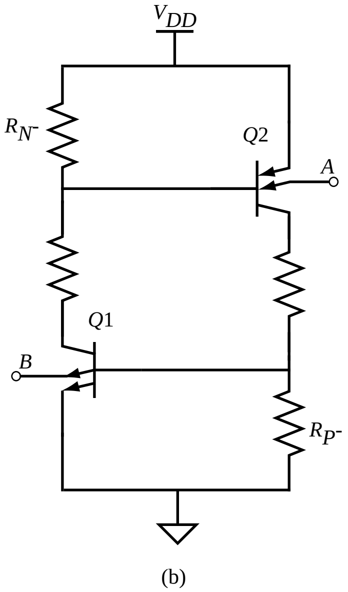


Figure 2.5-3 (a) Parasitic lateral NPN and vertical PNP bipolar transistor in CMOS integrated circuits. (b) Equivalent circuit of the SCR formed from the parasitic bipolar transistors.

PREVENTING LATCHUP

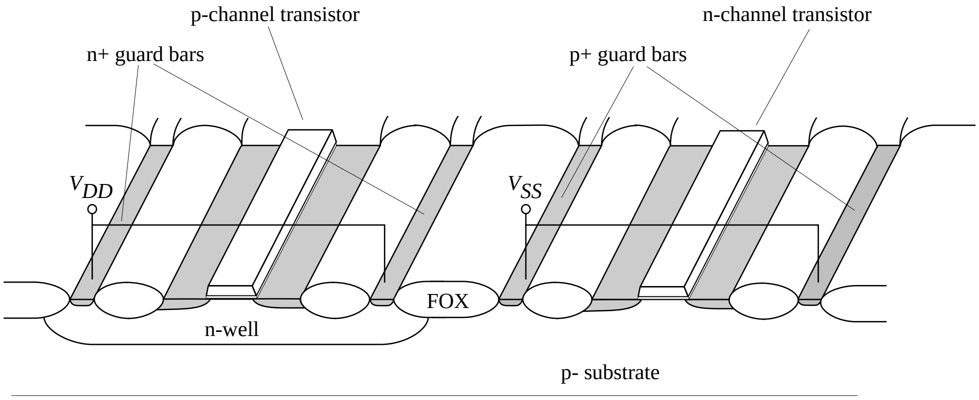


Figure 2.5-4 Preventing latch-up using guard bars in an n-well technology

II.7 - ESD PROTECTION

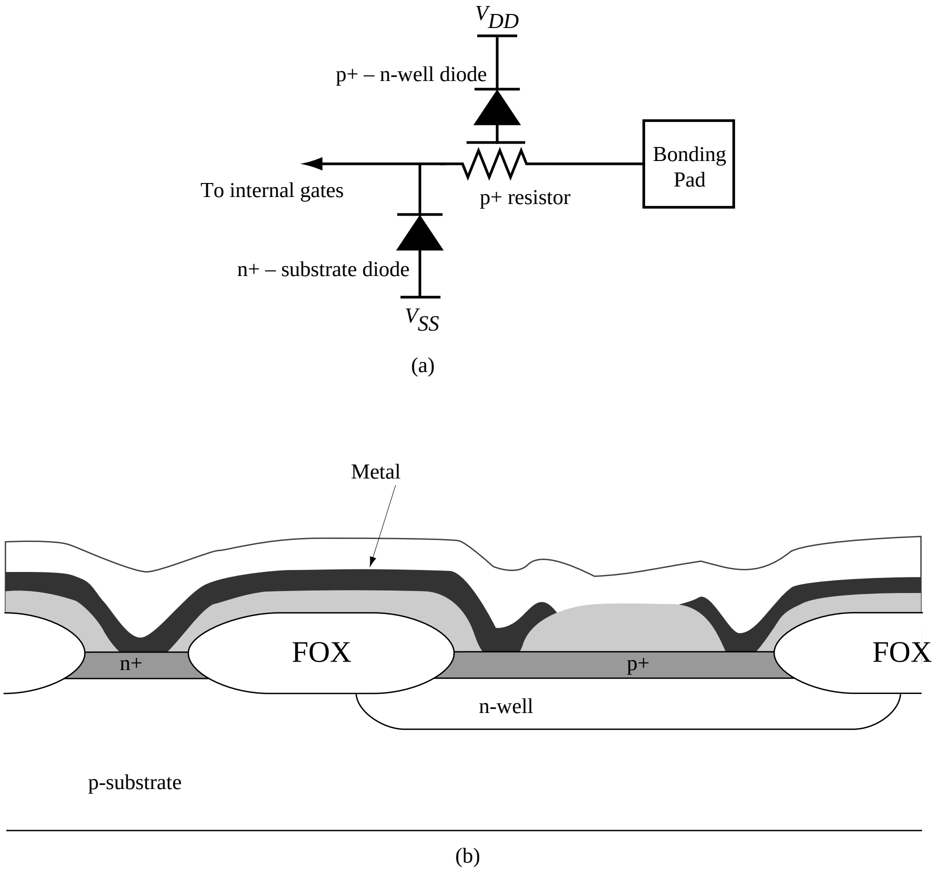


Figure 2.5-5 Electrostatic discharge protection circuitry. (a) Electrical equivalent circuit (b) Implementation in CMOS technology

II.8 - GEOMETRICAL CONSIDERATIONS

Design Rules for a Double-Metal, Double-Polysilicon, N-Well, Bulk CMOS Process.

	Minimum Dimension Resolution (λ)
1. N-Well	
1A. width	6
1B. spacing	12
2. Active Area (AA)	
2A. width	4
Spacing to Well	
2B. AA-n contained in n-Well	1
2C. AA-n external to n-Well	10
2D. AA-p contained in n-Well	3
2E. AA-p external to n-Well	4
Spacing to other AA (inside or outside well)	
2F. AA to AA (p or n)	3
3. Polysilicon Gate (Capacitor bottom plate)	
3A. width	2
3B. spacing	3
3C. spacing of polysilicon to AA (over field)	1
3D. extension of gate beyond AA (transistor width dir.)	2
3E. spacing of gate to edge of AA (transistor length dir.)	4
4. Polysilicon Capacitor top plate	
4A. width	2
4B. spacing	2
4C. spacing to inside of polysilicon gate (bottom plate)	2
5. Contacts	

5A.	size	2x2
5B.	spacing	4
5C.	spacing to polysilicon gate	2
5D.	spacing polysilicon contact to AA	2
5E.	metal overlap of contact	1
5F.	AA overlap of contact	2
5G.	polysilicon overlap of contact	2
5H.	capacitor top plate overlap of contact	2
6.	Metal-1	
6A.	width	3
6B.	spacing	3
7.	Via	
7A.	size	3x3
7B.	spacing	4
7C.	enclosure by Metal-1	1
7D.	enclosure by Metal-2	1
8.	Metal-2	
8A.	width	4
8B.	spacing	3
	Bonding Pad	
8C.	spacing to AA	24
8D.	spacing to metal circuitry	24
8E.	spacing to polysilicon gate	24

9. Passivation Opening (Pad)

9A.	bonding-pad opening	100μm x 100μm
9B.	bonding-pad opening enclosed by Metal-2	8
9C.	bonding-pad opening to pad opening space	40

Note: For a P-Well process, exchange p and n in all instances.

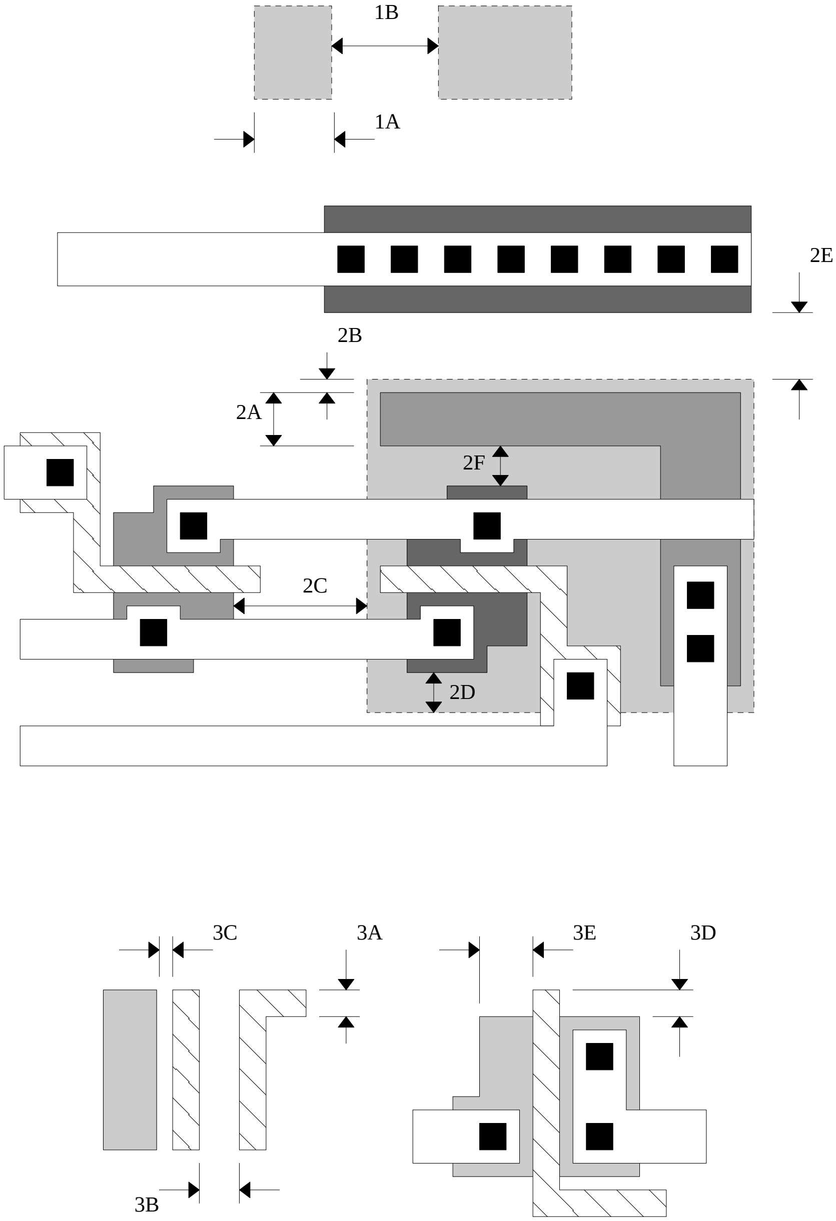


Figure 2.6-8(a) Illustration of the design rules 1-3 of Table 2.6-1.

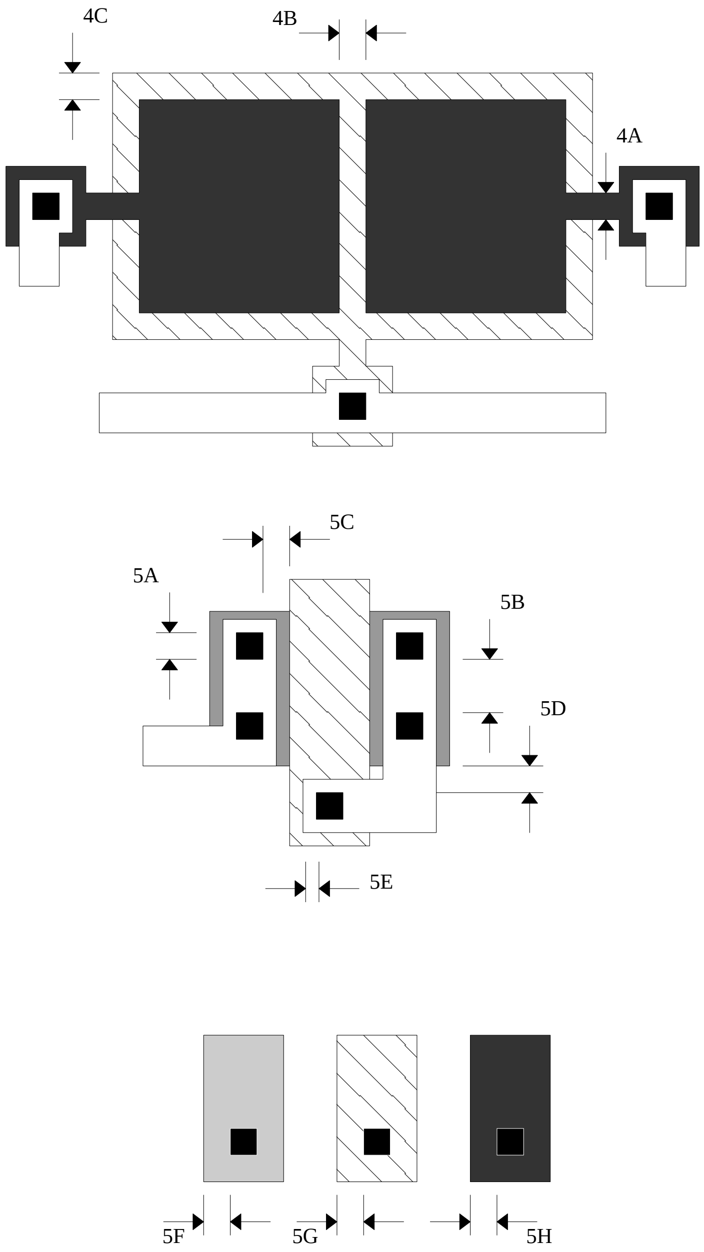


Figure 2.6-8(b) Illustration of the design rules 4-5 of Table 2.6-1.

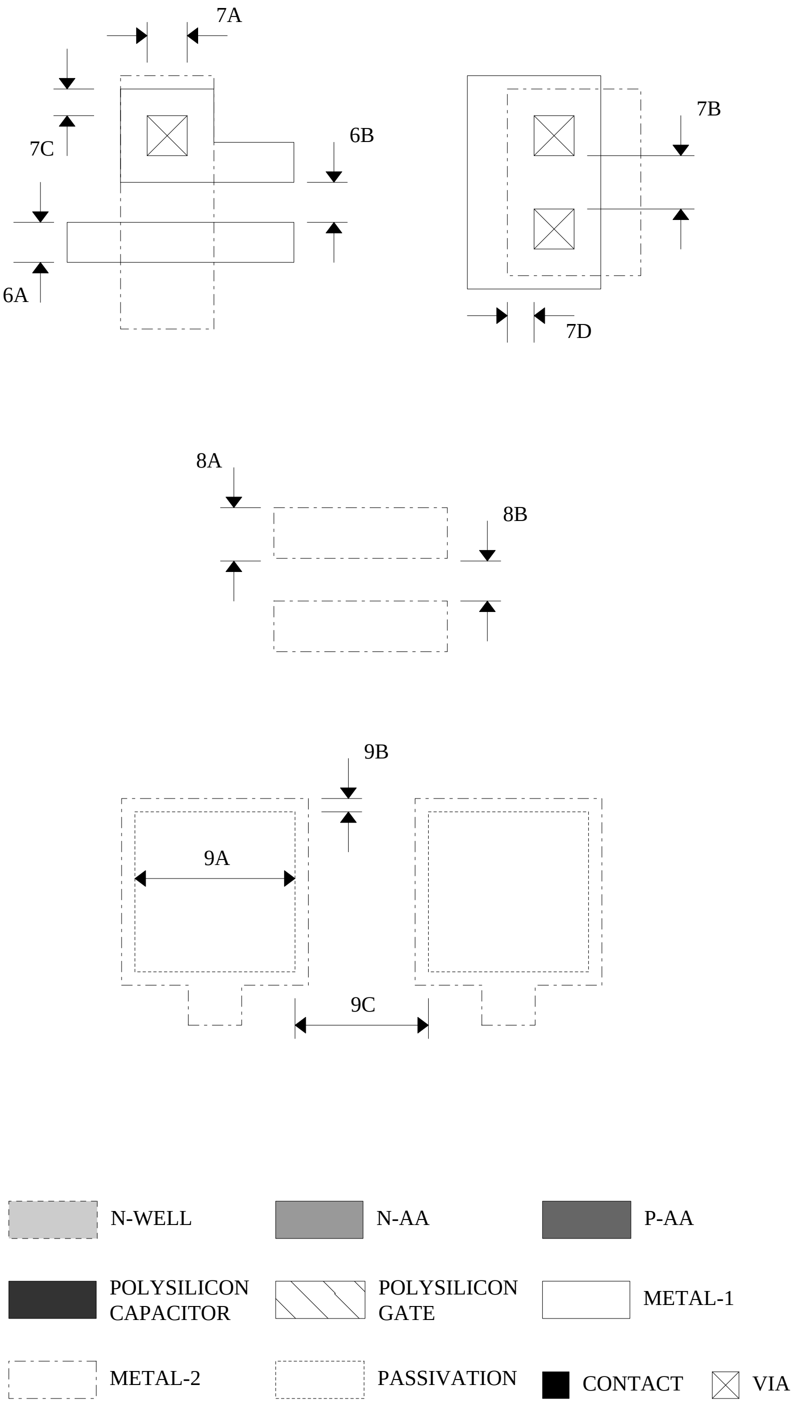


Figure 2.6-8(c) Illustration of the design rules 6-9 of Table 2.6-1.

Transistor Layout

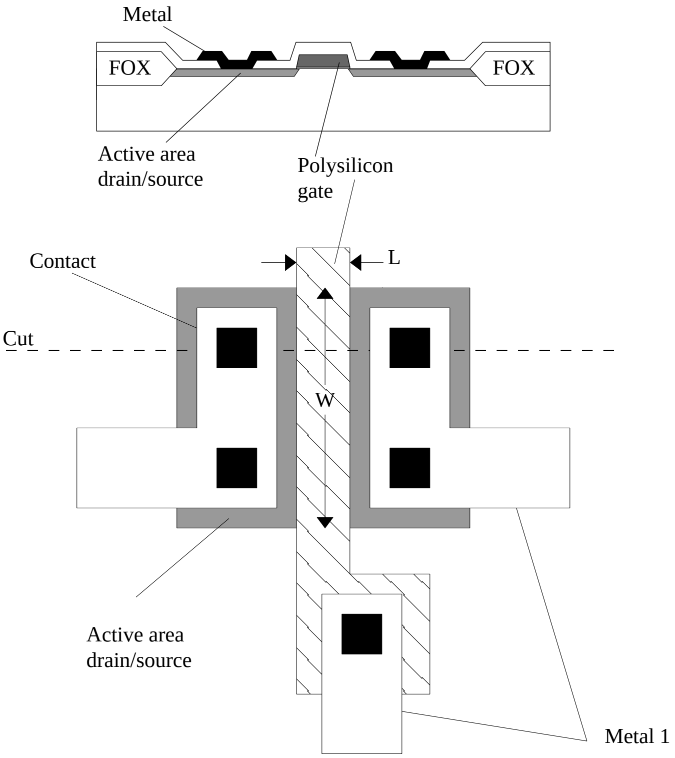


Figure 2.6-3 Example layout of an MOS transistor showing top view and side view at the cut line indicated.

SYMMETRIC VERSUS PHOTOLITHOGRAPHIC INVARIANT

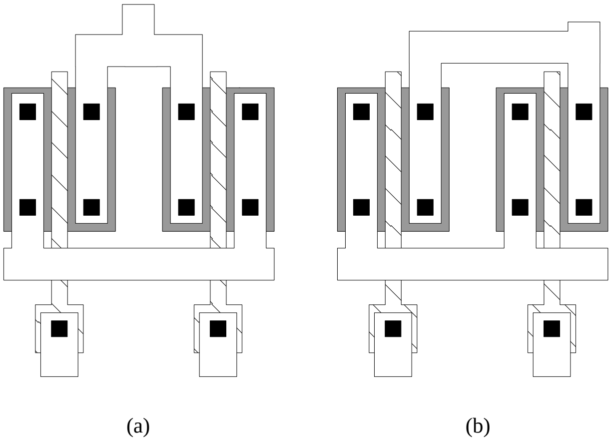
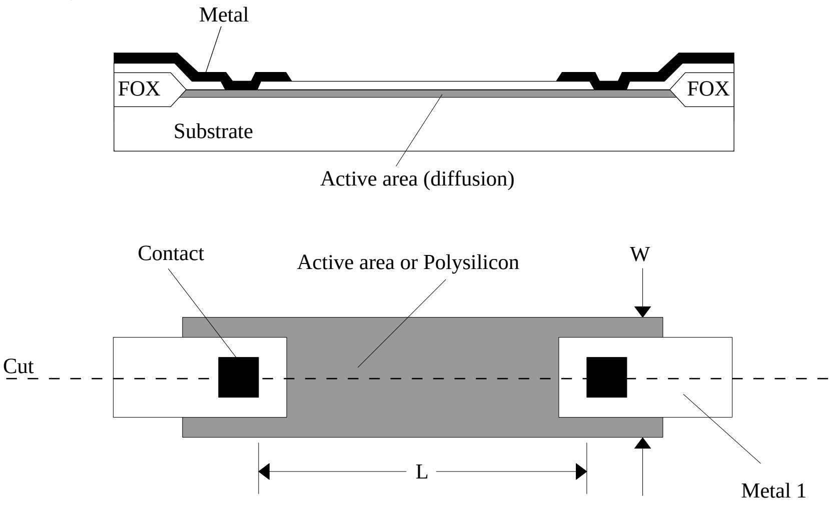


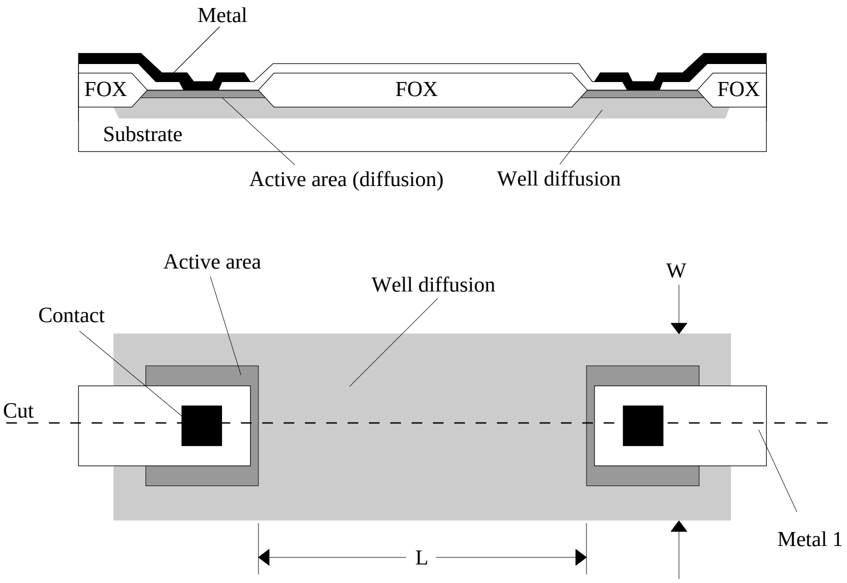
Figure 2.6-4 Example layout of MOS transistors using (a) mirror symmetry, and (b) photolithographic invariance.

PLI IS BETTER

Resistor Layout



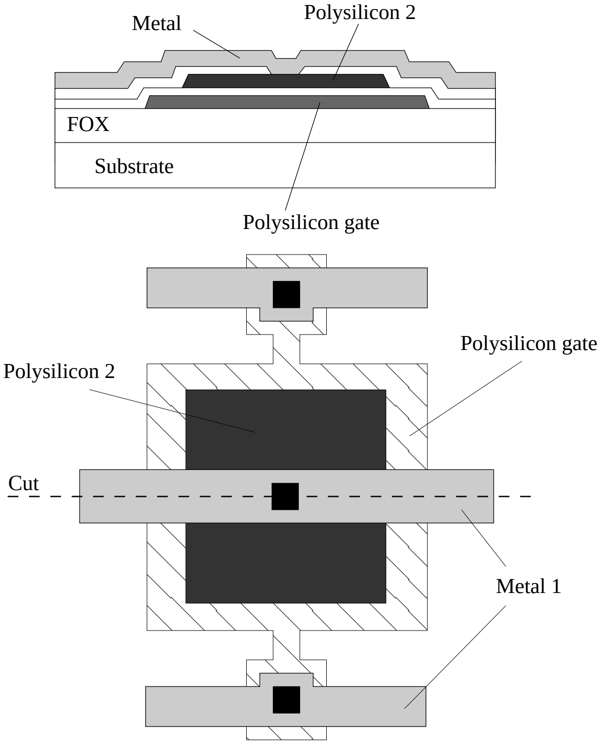
(a) Diffusion or polysilicon resistor



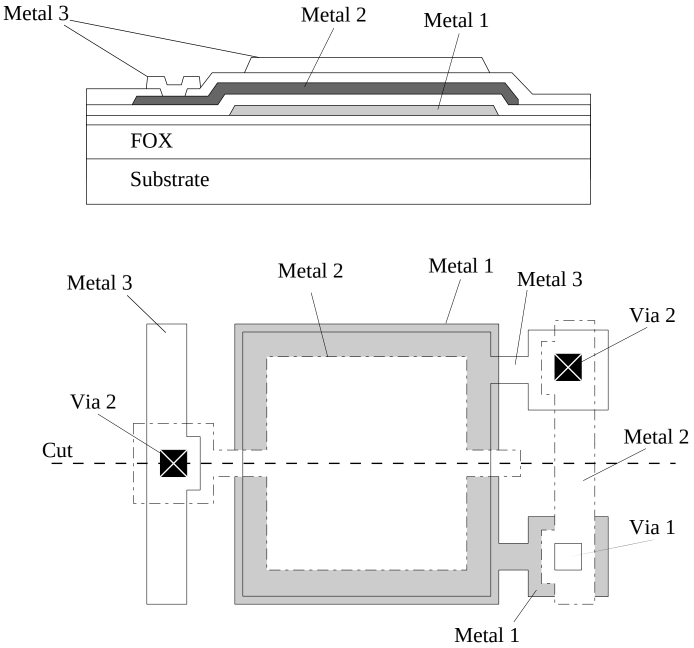
(b) Well resistor

Figure 2.6-5 Example layout of (a) diffusion or polysilicon resistor and (b) Well resistor along with their respective side views at the cut line indicated.

Capacitor Layout



(a)

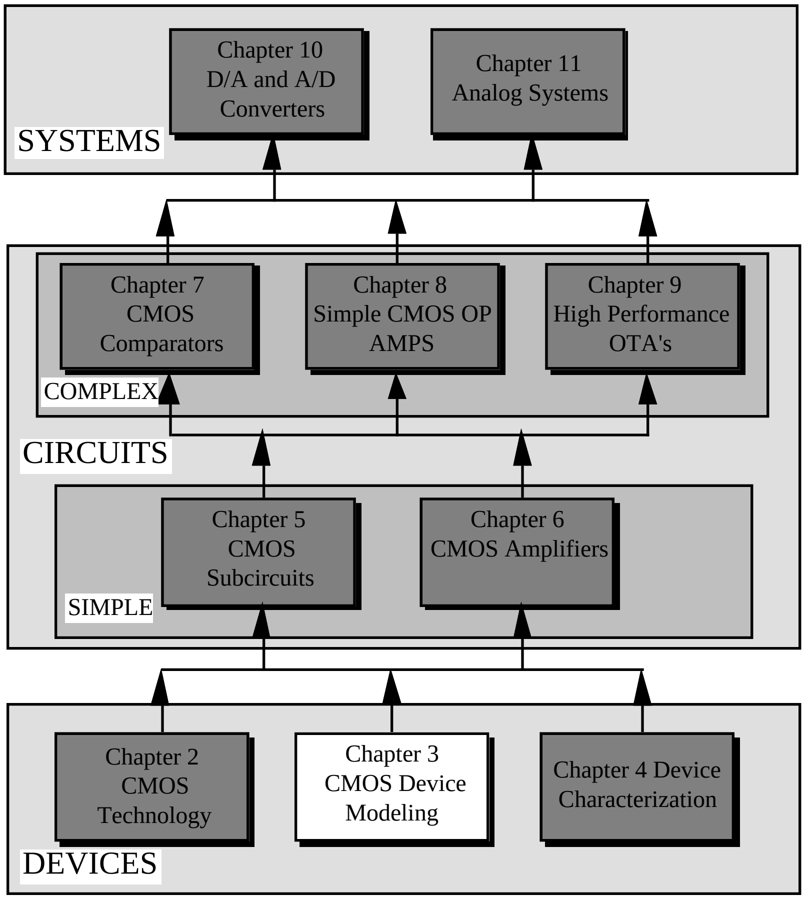


III. CMOS MODELS

Contents

III.1 Simple MOS large-signal model
    Strong inversion
    Weak inversion
III.2 Capacitance model
III.3 Small-signal MOS model
III.4 SPICE Level-3 model

Perspective



III.1 - MODELING OF CMOS ANALOG CIRCUITS

Objective

1. Hand calculations and design of analog CMOS circuits.
2. Efficiently and accurately simulate analog CMOS circuits.

Large Signal Model

The large signal model is nonlinear and is used to solve for the dc values of the device currents given the device voltages.

The large signal models for SPICE:

Basic drain current models -

1. Level 1 - Shichman-Hodges (V_T, K', γ, λ, ϕ, and N_{SUB})

2. Level 2 - Geometry-based analytical model. Takes into account second-order effects (varying channel charge, short-channel, weak inversion, varying surface mobility, etc.)

3. Level 3 - Semi-empirical short-channel model

4. Level 4 - BSIM model. Based on automatically generated parameters from a process characterization. Good weak-strong inversion transition.

Basic model auxilliary parameters include capacitance [Meyer and Ward-Dutton (charge-conservative)], bulk resistances, depletion regions, etc..

Small Signal Model

Based on the linearization of any of the above large signal models.

Simulator Software

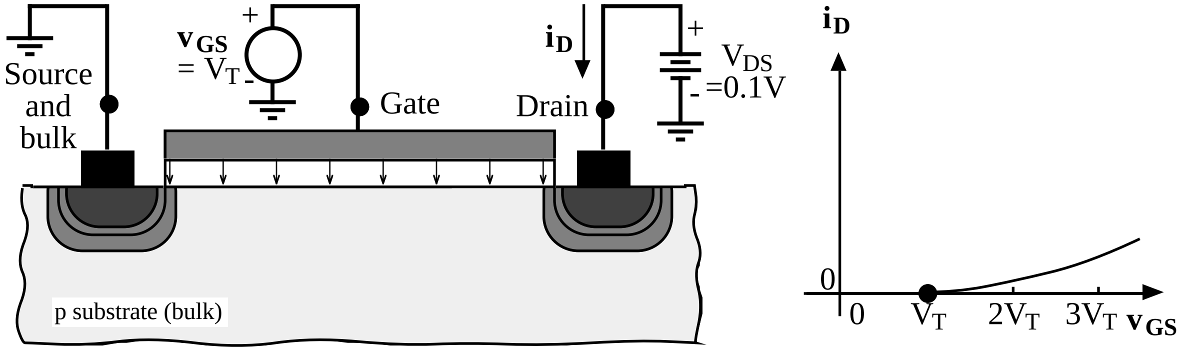
SPICE2 - Generic SPICE available from UC Berkeley (FORTRAN)

SPICE3 - Generic SPICE available from UC Berkeley (C)

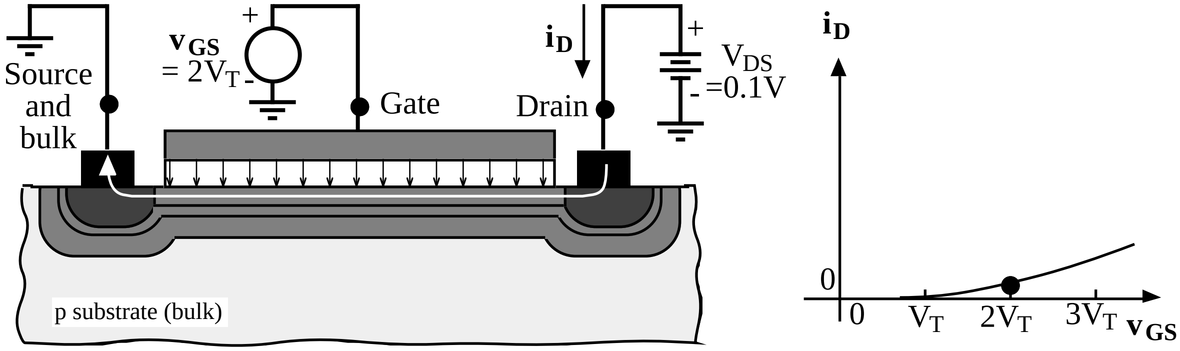
SPICE- Every other SPICE simulator!

Transconductance Characteristics of NMOS when V_{DS} = 0.1V

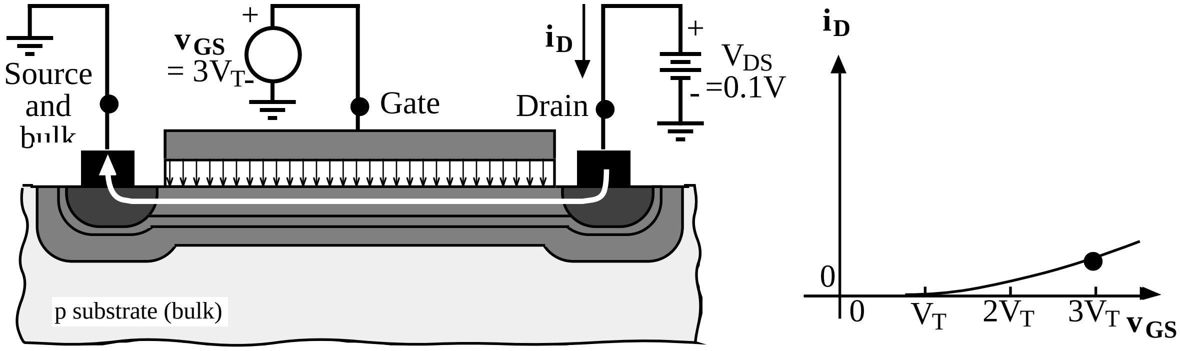
$v_{GS} \leq V_T$:



$v_{GS} = 2V_T$:

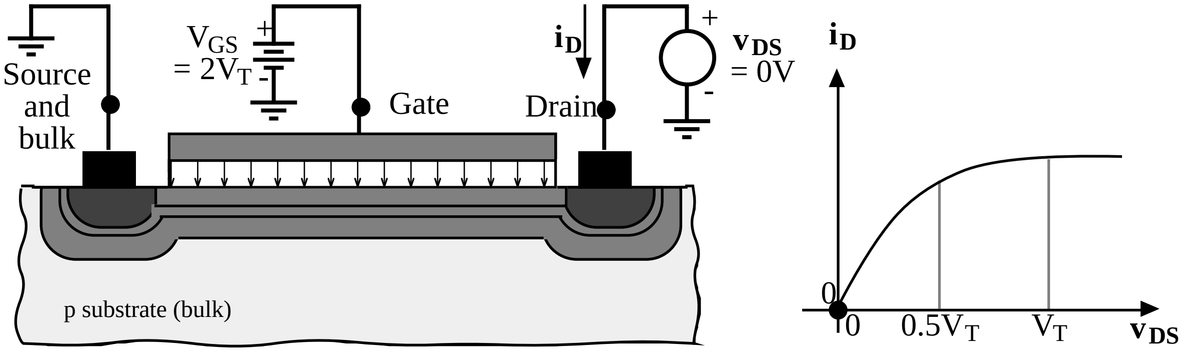


$v_{GS} = 3V_T$:

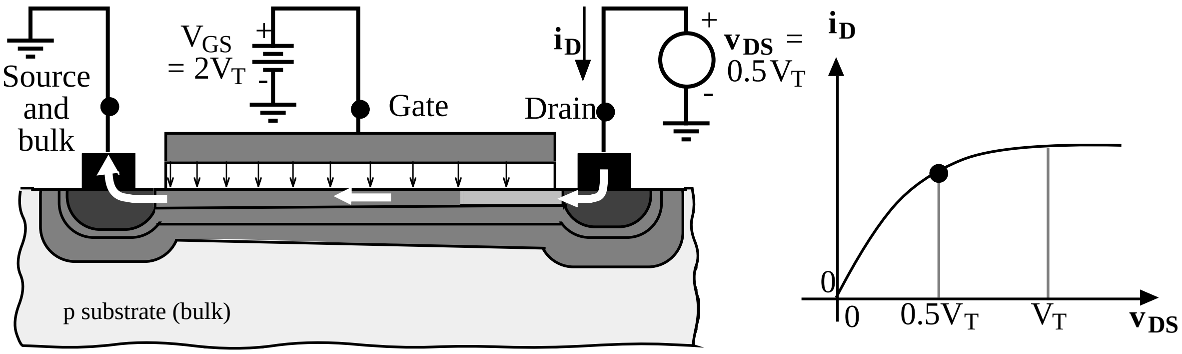


Output Characteristics of NMOS for $V_{GS} = 2V_T$

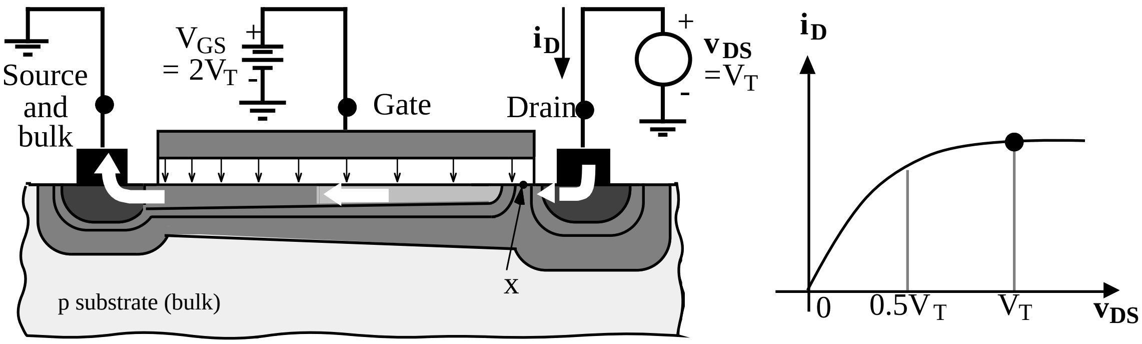
$v_{DS} = 0V$:



$v_{DS} = 0.5V_T$:

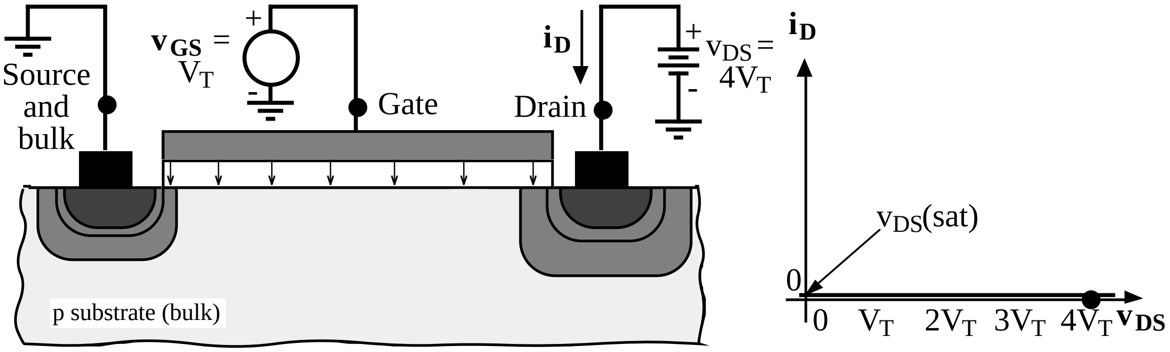


$v_{DS} = V_T$:

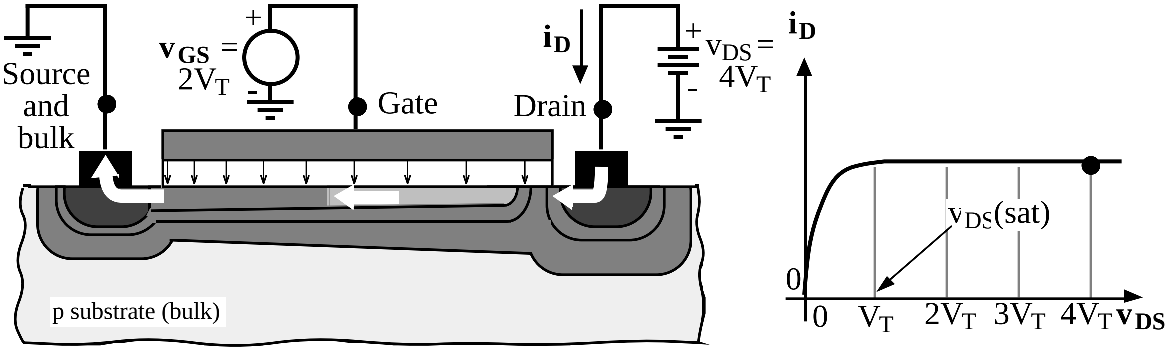


Output Characteristics of NMOS when $v_{DS} = 4V_T$

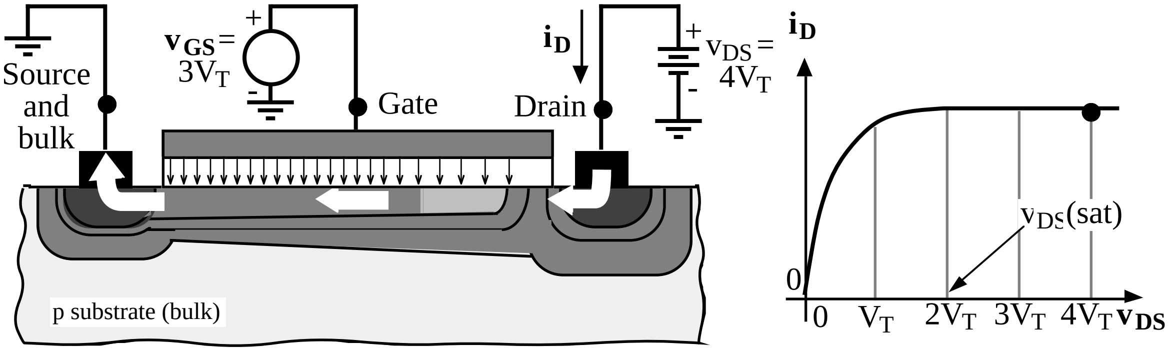
$v_{GS} = V_T$:



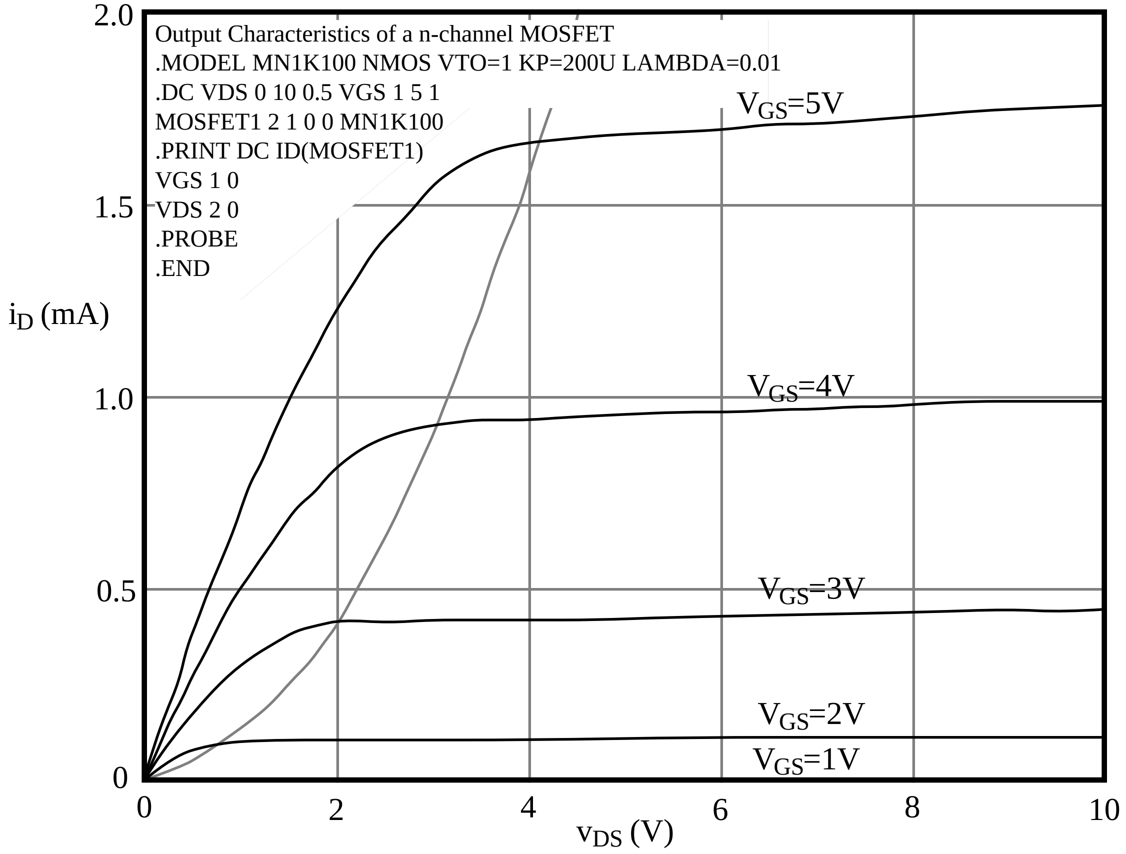
$v_{GS} = 2V_T$:



$v_{GS} = 3V_T$:

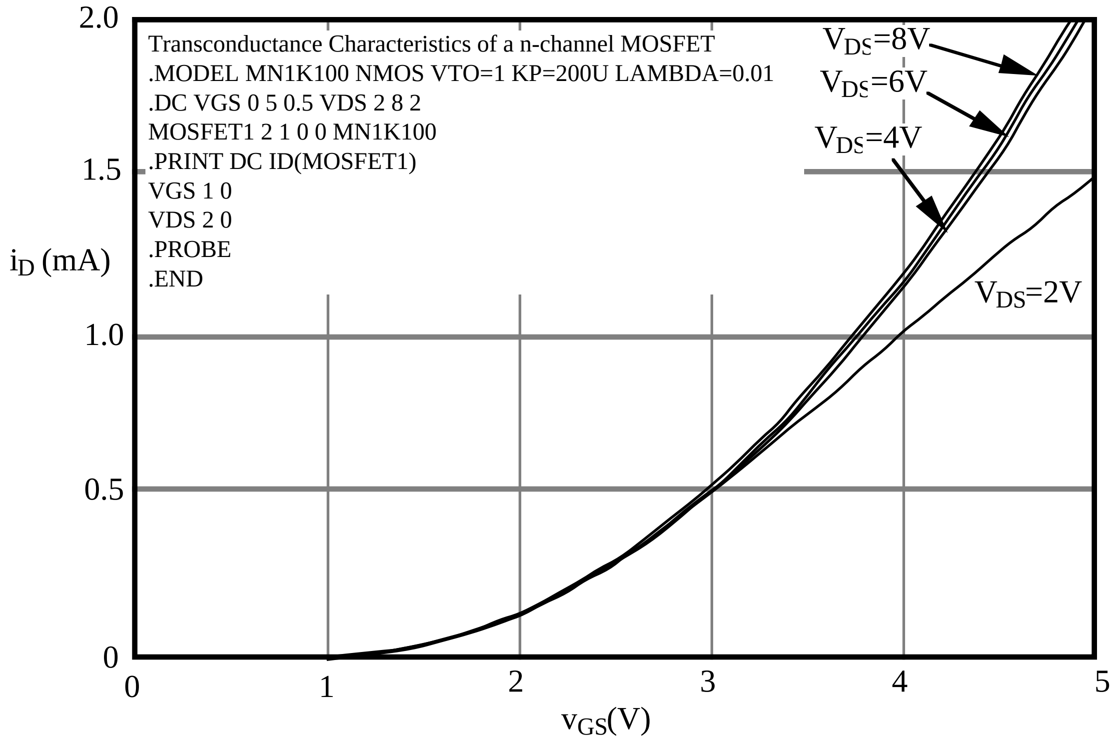


Output Characteristics of an n-channel MOSFET



```
Output Characteristics of a n-channel MOSFET
.MODEL MN1K100 NMOS VTO=1 KP=200U LAMBDA=0.01
.DC VDS 0 10 0.5 VGS 1 5 1
MOSFET1 2 1 0 0 MN1K100
.PRINT DC ID(MOSFET1)
VGS 1 0
VDS 2 0
.PROBE
.END
```

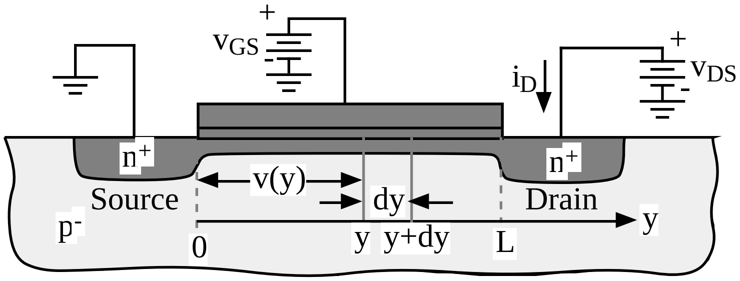
Transconductance Characteristics of an n-channel MOSFET



```
Transconductance Characteristics of a n-channel MOSFET
.MODEL MN1K100 NMOS VTO=1 KP=200U LAMBDA=0.01
.DC VGS 0 5 0.5 VDS 2 8 2
MOSFET1 2 1 0 0 MN1K100
.PRINT DC ID(MOSFET1)
VGS 1 0
VDS 2 0
.PROBE
.END
```

SIMPLIFIED SAH MODEL DERIVATION

Model-



Derivation-

- Let the charge per unit area in the channel inversion layer be

$$Q_I(y) = C_{ox}[v_{GS} - v(y) - V_T] \quad \text{(coulombs/cm}^2\text{)}$$

- Define sheet conductivity of the inversion layer per square as

$$\sigma_S = \mu_o Q_I(y) \quad \left(\frac{\text{cm}2}{\text{v}\cdot\text{s}}\right)\left(\frac{\text{coulombs}}{\text{cm}2}\right) = \frac{\text{amps}}{\text{volt}} = \frac{1}{\Omega/\text{sq.}}$$

- Ohm's Law for current in a sheet is

$$J_S = \frac{i_D}{W} = \sigma_S E_y = \sigma_S \frac{dv}{dy} \ .$$

Rewriting Ohm's Law gives,

$$dv = \frac{i_D}{\sigma_S W}\ dy = \frac{i_D dy}{\mu_o Q_I(y) W}$$

where dv is the voltage drop along the channel in the direction of y.

Rewriting as

$$i_D\ dy = W\mu_o Q_I(y) dv$$

and integrating along the channel for 0 to L gives

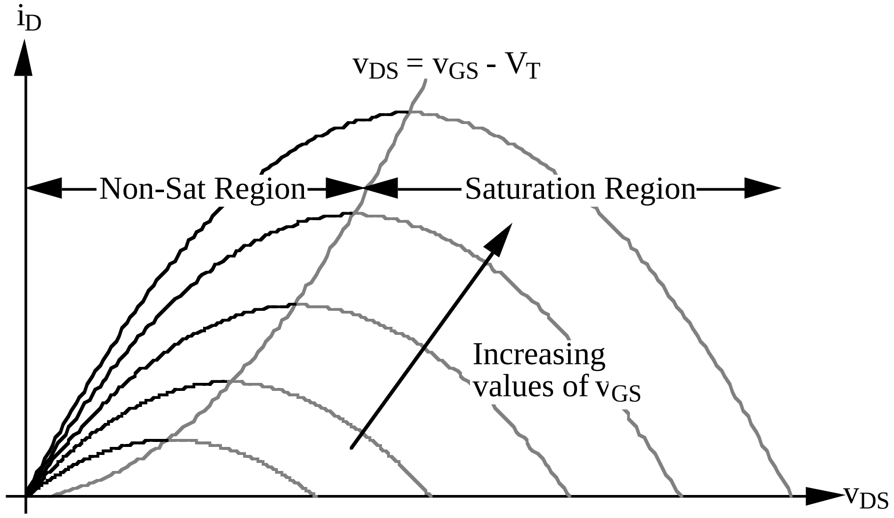
$$\int_0^L i_D dy = \int_0^{v_{DS}} W\mu_o Q_I(y) dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS} - v(y) - V_T]\ dv$$

After integrating and evaluating the limits

$$\boxed{i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

ILLUSTRATION OF THE SAH EQUATION

Plotting the Sah equation as i_D vs. v_{DS} results in -



Define $v_{DS}(sat) = v_{GS} - V_T$

Regions of Operation of the MOS Transistor

1.) Cutoff Region:

$$i_D = 0, \quad v_{GS} - V_T < 0$$

(Ignores subthreshold currents)

2.) Non-saturation Region

$$i_D = \frac{\mu C_{ox} W}{2L}\left[2(v_{GS} - V_T) - v_{DS}\right] v_{DS} \,,\ 0 < v_{DS} < v_{GS} - V_T$$

3.) Saturation Region

$$i_D = \frac{\mu C_{ox} W}{2L}\left[(v_{GS} - V_T)^2\right],\ 0 < v_{GS} - V_T < v_{DS}$$

SAH MODEL ADJUSTMENT TO INCLUDE EFFECTS OF V_{DS} ON V_T

From the previous derivation:

$$\int_0^L i_D\,dy = \int_0^{v_{DS}} W\mu_o Q_I(y)dy = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS} - v(y) - V_T]dv$$

Assume that the threshld voltage varies across the channel in the following way:

$$V_T(y) = V_T + \Delta v(y)$$

where V_T is the value of the threshold voltage at the source end of the channel.

Integrating the above gives,

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v(y) - (1+\Delta)\frac{v^2(y)}{2}\right]_0^{v_{DS}}$$

or

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS} - (1+\Delta)\frac{v^2{}_{DS}}{2}\right]$$

To find $v_{DS}(\text{sat})$, set the derivative of i_D with respect to v_{DS} equal to zero and solve for $v_{DS} = v_{DS}(\text{sat})$ to get,

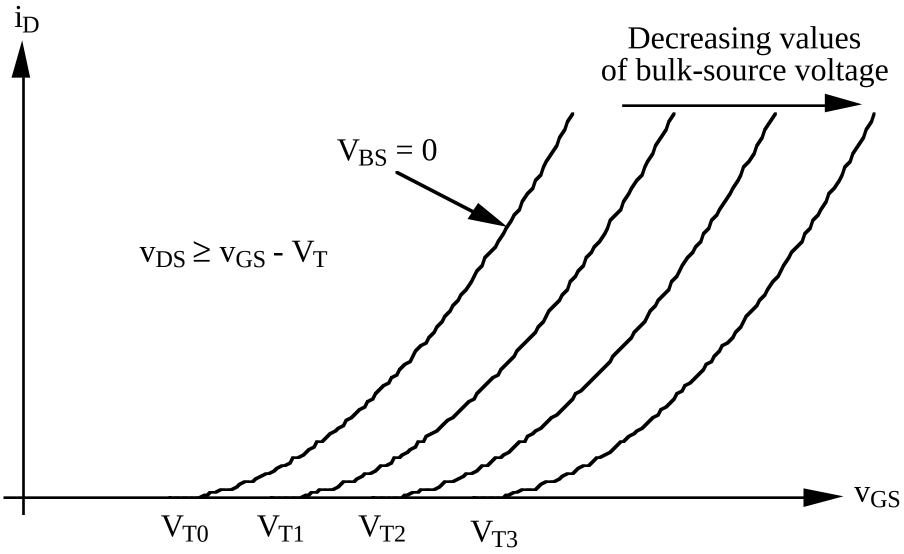
$$v_{DS}(\text{sat}) = \frac{v_{GS} - V_T}{1 + \Delta}$$

Therefore, in the saturation region, the drain current is

$$i_D = \frac{W\mu_o C_{ox}}{2(1+\Delta)L}\left(v_{GS} - V_T\right)^2$$

EFFECTS OF BACK GATE (BULK-SOURCE)

Bulk-Source (v_{BS}) influence on the transconductance characteristics-



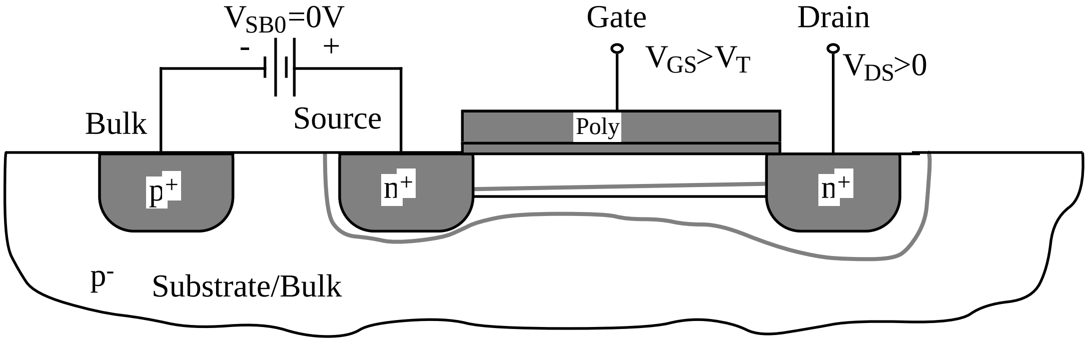
In general, the simple model incorporates the bulk effect into V_T by the following empirically developed equation-

$$V_{T(V_{BS})} = V_{T0} + \gamma\sqrt{2|\phi_f| + |v_{BS}|} - \gamma\sqrt{2|\phi_f|}$$

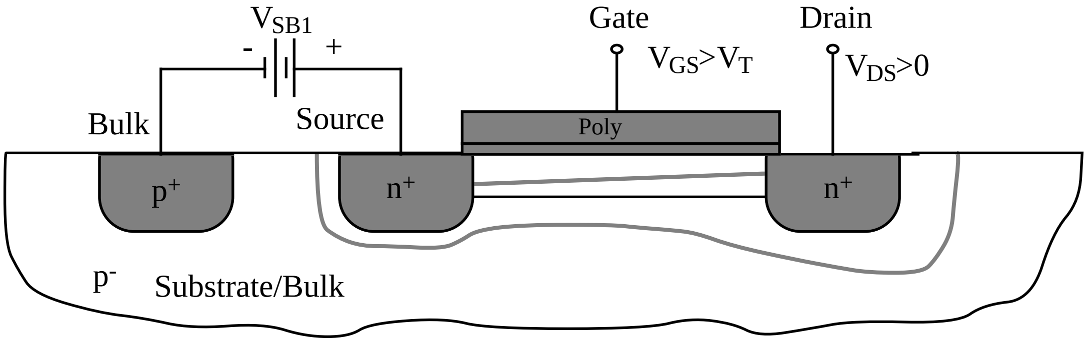
EFFECTS OF THE BACK GATE - CONTINUED

Illustration-

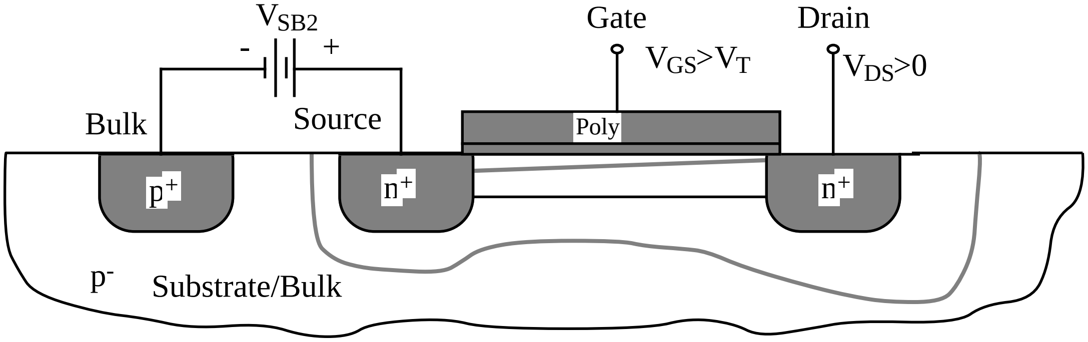
$V_{SB0} = 0V$:



$V_{SB1} > 0V$:

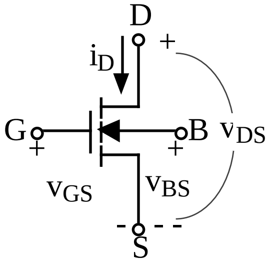


$V_{SB2} > V_{SB1}$:



SAH MODEL INCLUDING CHANNEL LENGTH MODULATION

N-channel reference convention:



Non-saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]$$

Saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS}(\text{sat}) - \frac{v_{DS}(\text{sat})^2}{2}\right](1 + \lambda v_{DS})$$

$$= \frac{W\mu_o C_{ox}}{2L}(v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

where:

μ_o = zero field mobility (cm^2/volt·sec)

C_{ox} = gate oxide capacitance per unit area (F/cm^2)

λ= channel-length modulation parameter (volts^{-1})

$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|}\right)$

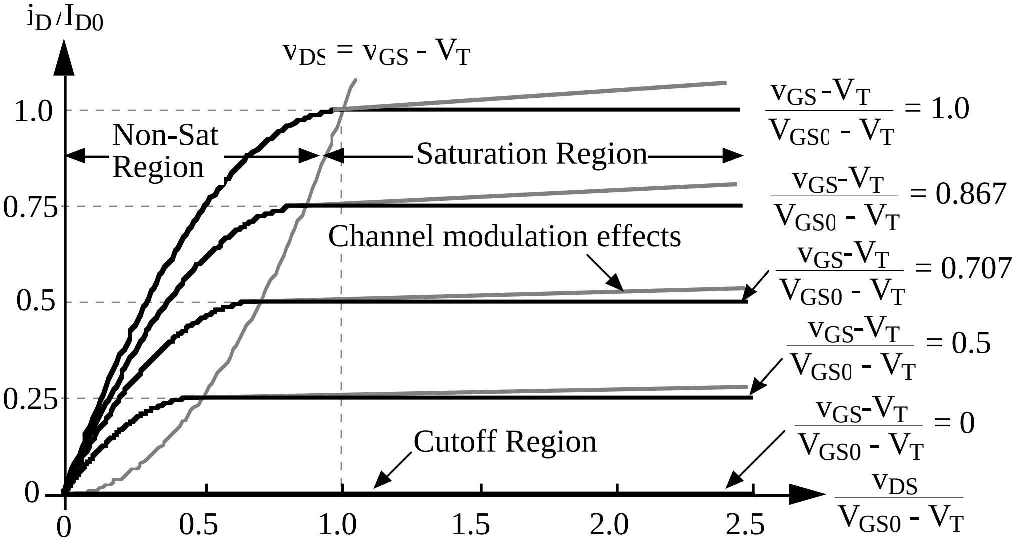
V_{T0} = zero bias threshold voltage

γ = bulk threshold parameter (volts$^{1/2}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

When solving for p-channel devices, negate all voltages and use the n-channel model with p-channel parameters and negate the current. Also negate V_{T0} of the p device.

OUTPUT CHARACTERISTICS OF THE MOS TRANSISTOR



Notation:

$$ß = K'\left(\frac{W}{L}\right) = (\mu_o C_{ox})\frac{W}{L}$$

Note:

$$\mu_o C_{ox} = K'$$

GRAPHICAL INTERPRETATION OF λ

Assume the MOS is transistor is saturated-

$$\therefore\ i_D = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

Define $i_D(0) = i_D$ when $v_{DS} = 0V$.

$$\therefore\ i_D(0) = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2$$

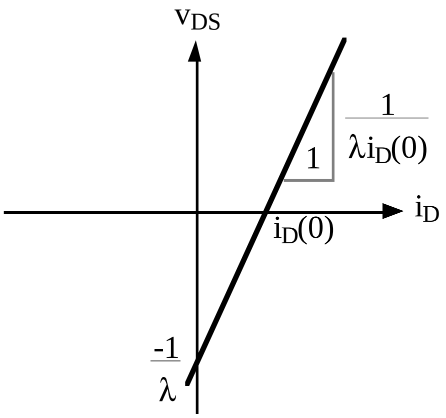
Now,

$$i_D = i_D(0)\,[1+\lambda v_{DS}] = i_D(0) + \lambda i_D(0)\, v_{DS}$$

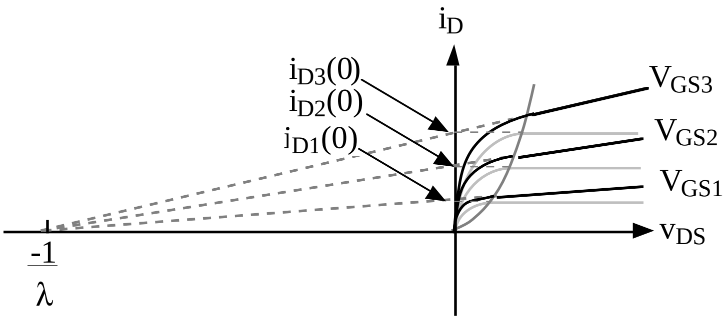
or

$$v_{DS} = \left[\frac{1}{\lambda i_D\,(0)}\right] i_D \ - \frac{1}{\lambda}$$

Matching with y = mx + b gives



or

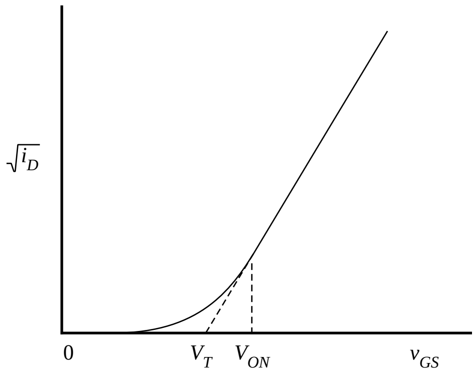


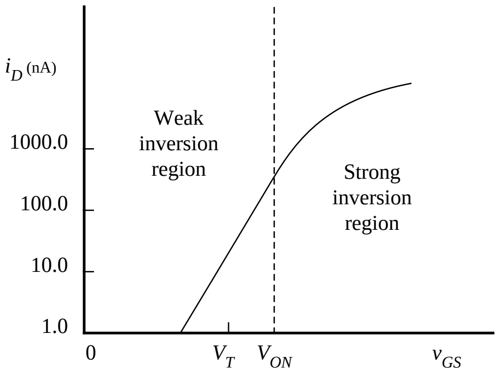
SPICE LEVEL 1 MODEL PARAMETERS FOR A TYPICAL BULK CMOS PROCESS (0.8μm)

Model Parameter	Parameter Description	Typical Parameter Value		Units
		NMOS	PMOS	
V_{T0}	ThresholdVoltage forV_{BS} = 0V	0.75±0.15	−0.85±0.15	Volts
K'	Transconductance Parameter (sat.)	110±10%	50±10%	$\mu A/V^2$
γ	Bulk Threshold Parameter	0.4	0.57	$\sqrt{V}$
λ	Channel Length Modulation Parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	V^{-1}
$\phi = 2\phi_F$	Surface potential at strong inversion	0.7	0.8	Volts

These values are based on a 0.8 μm silicon-gate bulk CMOS n-well process.

WEAK INVERSION MODEL (Simple)





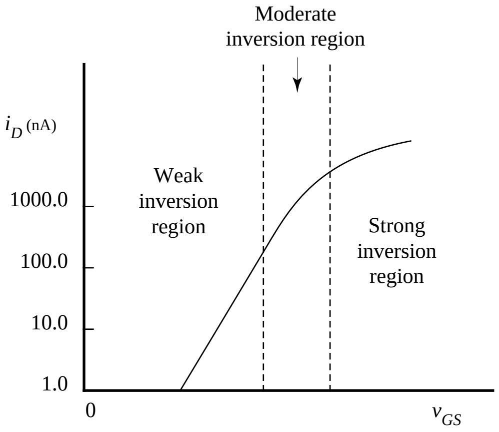
This model is appropriate for hand calculations but it does not accommodate a smooth transition into the strong-inversion region.

$$i_D \cong \frac{W}{L} I_{DO} \exp\left(\frac{q v_{GS}}{nkT}\right)$$

The transition point where this relationship is valid occurs at approximately

$$v_{gs} \; < \; V_T + n\,\frac{kT}{q}$$

<u>Weak-Moderate-Strong Inversion Approximation</u>



INTRINSIC CAPACITORS OF THE MOSFET

Types of MOS Capacitors

1. Depletion capacitance (C_{BD} and C_{BS})
2. Gate capacitances (C_{GS}, C_{GD}, and C_{GB})

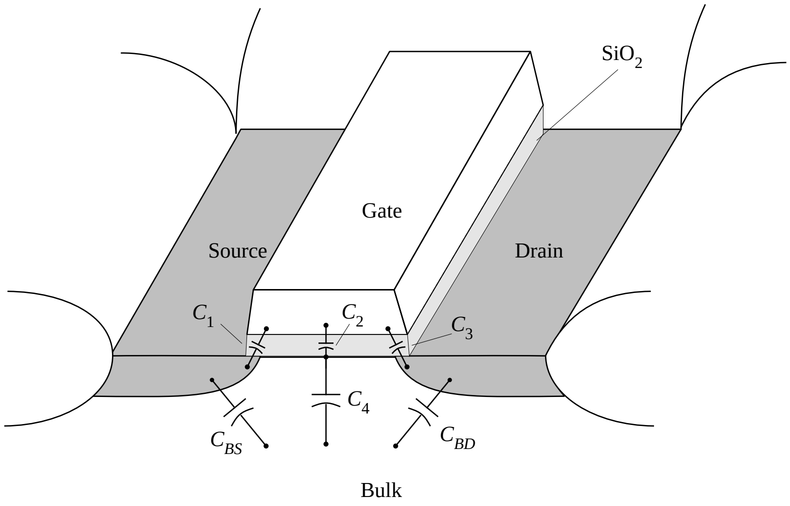
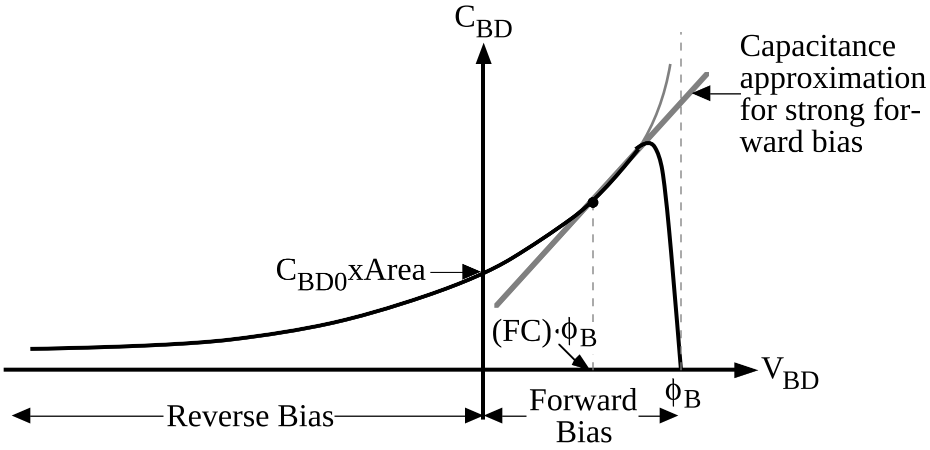


Figure 3.2-4 Large-signal, charge-storage capacitors of the MOS device.

Depletion Capacitors

Bulk-drain pn junction -



$$C_{BD} = \frac{C_{BD0}\,A_{BD}}{\left(1 - \frac{v_{BD}}{\phi_B}\right)^{MJ}} \quad \text{and}\, C_{BS} = \frac{C_{BS0}\,A_{BS}}{\left(1 - \frac{v_{BS}}{\phi_B}\right)^{MJ}}$$

where,

A_{BD} (A_{BS}) = area of the bulk-drain (bulk-source)

ϕ_B = bulk junction potential (barrier potential)

MJ = bulk junction grading coefficient ($0.33 \leq MJ \leq 0.5$)

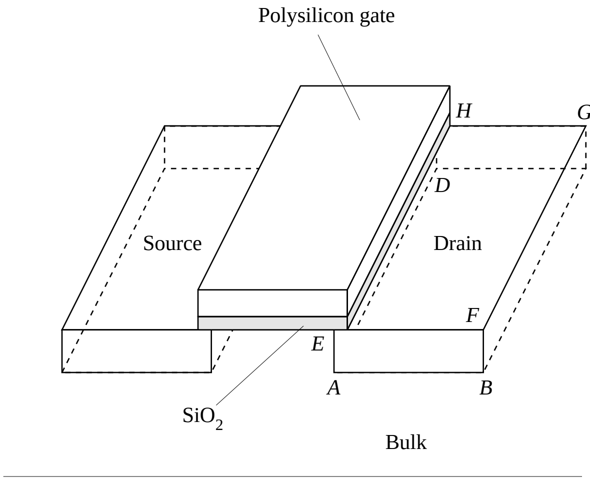
For strong forward bias, approximate the behavior by the tangent to the above C_{BD} or C_{BS} curve at v_{BD} or v_{BS} equal to $(FC)\cdot\phi_B$.

$$C_{BD} = \frac{C_{BD0}A_{BD}}{(1+FC)^{1+MJ}}\left[1 - (1+MJ)FC + FC\left(\frac{v_{BD}}{\phi_B}\right)\right]\ ,\ \ v_{BD} > (FC)\cdot\phi_B$$

and

$$C_{BD} = \frac{C_{BS0}A_{BS}}{(1+FC)^{1+MJ}}\left[1 - (1+MJ)FC + FC\left(\frac{v_{BS}}{\phi_B}\right)\right]\ ,\ \ v_{BS} > (FC)\cdot\phi_B$$

Bottom & Sidewall Approximations



Drain bottom = *ABCD*
Drain sidewall = *ABFE* + *BCGF* + *DCGH* + *ADHE*

$$C_{BX} = \frac{(CJ)(AX)}{\left[1-\left(\dfrac{v_{BX}}{PB}\right)\right]^{MJ}} + \frac{(CJSW)(PX)}{\left[1-\left(\dfrac{v_{BX}}{PB}\right)\right]^{MJSW}}, \quad v_{BX} \le (FC)(PB)$$

and

$$C_{BX} = \frac{(CJ)(AX)}{(1-FC)^{1+MJ}}\left[1-(1+MJ)FC + MJ\,\frac{v_{BX}}{PB}\right]$$

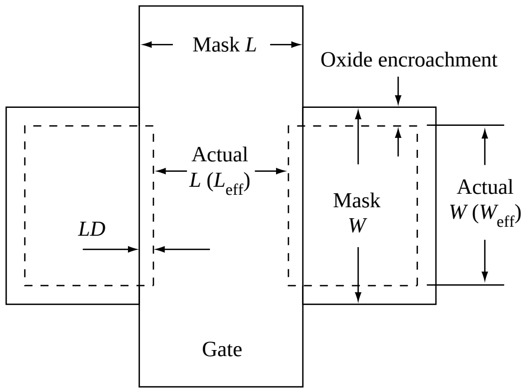
$$+\frac{(CJSW)(PX)}{(1-FC)^{1+MJSW}}\left[1-(1+MJSW)FC + \frac{v_{BX}}{PB}(MJSW)\right],$$

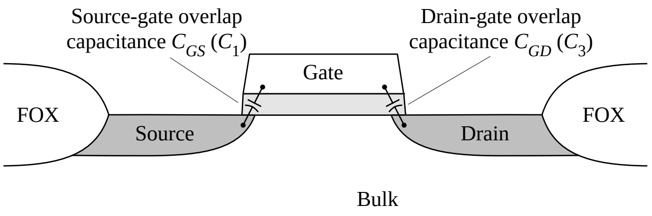
$$v_{BX} \ge (FC)(PB)$$

where

AX = area of the source (*X* = *S*) or drain (*X* = *D*)
PX = perimeter of the source (*X* = *S*) or drain (*X* = *D*)
CJSW = zero-bias, bulk-source/drain sidewall capacitance
MJSW = bulk-source/drain sidewall grading coefficient

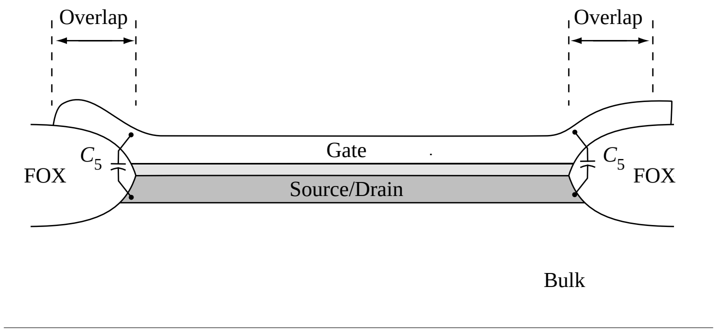
Overlap Capacitance





$$C_1 = C_3 \cong (LD)(W_{\text{eff}})C_{ox} = (CGXO)W_{\text{eff}}$$

Gate to Bulk Overlap Capacitance



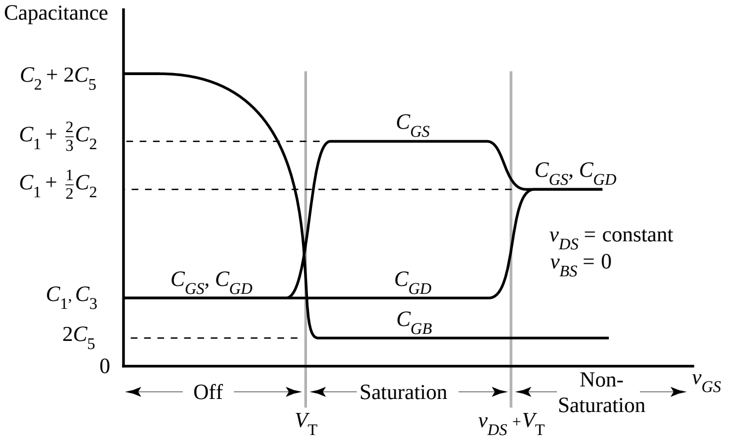
On a per-transistor basis, this is generally quite small

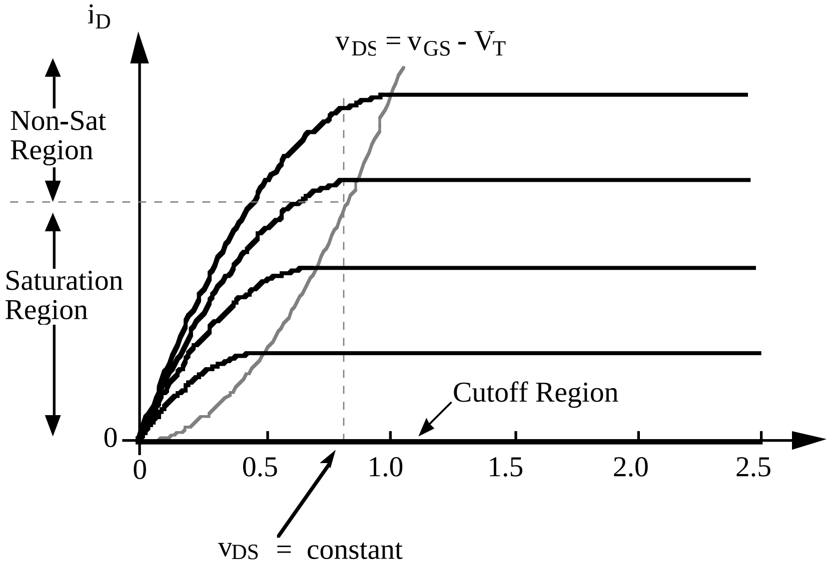
Channel Capacitance

$$C_2 = W_{\text{eff}}(L - 2LD)C_{ox} = W_{\text{eff}}(L_{\text{eff}})C_{ox}$$

Drain and source portions depend upon operating condition of transistor.

MOSFET Gate Capacitance Summary:





C_{GS}, C_{GD}, and C_{GB}

Off

$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{\text{eff}})(L_{\text{eff}}) + CGB\text{O}(L_{\text{eff}})$$

$$C_{GS} = C_1 \cong C_{ox}(LD)(W_{\text{eff}}) = CGS\text{O}(W_{\text{eff}})$$

$$C_{GD} = C_3 \cong C_{ox}(LD)(W_{\text{eff}}) = CGD\text{O}(W_{\text{eff}})$$

Saturation

$$C_{GB} = 2C_5 = CGB\text{O}\ (L_{\text{eff}})$$

$$C_{GS} = C_1 + (2/3)C_2 = C_{ox}(LD + 0.67L_{\text{eff}})(W_{\text{eff}})$$

$$= CGS\text{O}(W_{\text{eff}}) + 0.67C_{ox}(W_{\text{eff}})(L_{\text{eff}})$$

$$C_{GD} = C_3 \cong C_{ox}(LD)(W_{\text{eff}}) = CGD\text{O}(W_{\text{eff}})$$

Nonsaturated

$$C_{GB} = 2C_5 = CGB\text{O}\ (L_{\text{eff}})$$

$$C_{GS} = C_1 + 0.5C_2 = C_{ox}(LD + 0.5L_{\text{eff}})(W_{\text{eff}})$$

$$= (CGS\text{O} + 0.5C_{ox}L_{\text{eff}})W_{\text{eff}}$$

$$C_{GD} = C_3 + 0.5C_2 = C_{ox}(LD + 0.5L_{\text{eff}})(W_{\text{eff}})$$

$$= (CGD\text{O} + 0.5C_{ox}L_{\text{eff}})W_{\text{eff}}$$

Small-Signal Model for the MOS Transistor

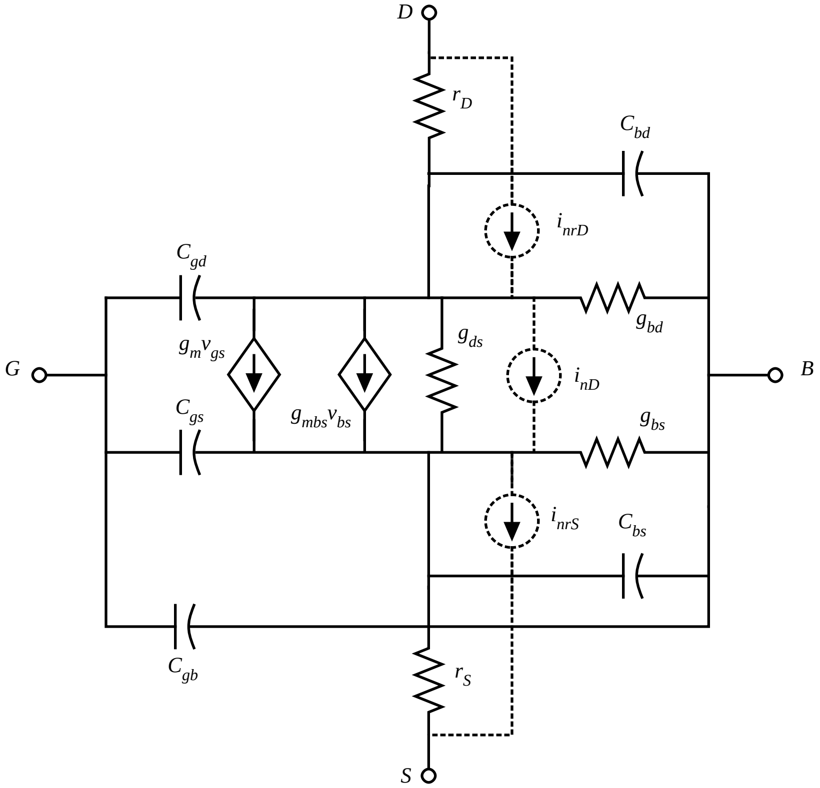


Figure 3.3-1 Small-signal model of the MOS transistor.

$$g_{bd} = \frac{\partial I_{BD}}{\partial V_{BD}} \text{(at the quiescent point)} \cong 0$$

and

$$g_{bs} = \frac{\partial I_{BS}}{\partial V_{BS}} \text{(at the quiescent point)} \cong 0$$

The channel conductances, g_m, g_{mbs}, and g_{ds} are defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{(at the quiescent point)}$$

$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} \text{(at the quiescent point)}$$

and

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \text{(at the quiescent point)}$$

Saturation Region

$$g_m = \sqrt{(2K'W/L)|\,I_D|(1 + \lambda\, V_{DS})} \cong \sqrt{(2K'W/L)|I_D|}$$

$$g_{mbs} = \frac{-\partial I_D}{\partial V_{SB}} = -\left(\frac{\partial I_D}{\partial V_T}\right)\left(\frac{\partial V_T}{\partial V_{SB}}\right)$$

Noting that $\frac{\partial I_D}{\partial V_T} = \frac{-\partial I_D}{\partial V_{GS}}$, we get

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = \eta\, g_m$$

$$g_{ds} = g_o = \frac{I_D\, \lambda}{1 + \lambda\, V_{DS}} \cong I_D\, \lambda$$

Relationships of the Small Signal Model Parameters upon the DC Values of Voltage and Current in the Saturation Region.

Small Signal Model Parameters	DC Current	DC Current and Voltage	DC Voltage
g_m	$\cong (2K'\, I_D W/L)^{1/2}$	–	$\cong \frac{2K'\, W}{L}(V_{GS} - V_T)$
g_{mbs}	—	$\frac{\gamma\,(2I_D\beta)^{1/2}}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$	$\frac{\gamma\,(\,\beta\,(V_{GS} - V_T)\,)}{2(2\lvert\phi_F\rvert + V_{SB})^{1/2}}$
g_{ds}	$\cong\ \lambda\, I_D$	—	—

Nonsaturation region

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = \beta\, V_{DS}$$

$$\mathrm{g_{mbs}} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\beta \gamma V_{DS}}{2(2|\phi_F| + \mathrm{V}_{SB})^{1/2}}$$

and

$$g_{ds} = \beta(V_{GS} - V_T - V_{DS})$$

Relationships of the Small-Signal Model Parameters upon the DC Values of Voltage and Current in the Nonsaturation Region.

Small Signal Model Parameters	DC Voltage and/or Current Dependence
g_m	$= \beta\, V_{DS}$
g_{mbs}	$\dfrac{\beta\, \gamma\, V_{DS}}{2(2\|\phi_F\| + V_{SB})^{1/2}}$
g_{ds}	$= \beta\,(V_{GS} - V_T - V_{DS})$

Noise

$$\overline{i}^{\,2}_{nrD} = \left(\frac{4kT}{r_D}\right)\Delta f \quad (\mathrm{A}^2)$$

$$\overline{i}^{\,2}_{nrS} = \left(\frac{4kT}{r_S}\right)\Delta f \quad (\mathrm{A}^2)$$

and

$$\overline{i}^{\,2}_{nD} = \left[\frac{8kT\, g_m(1+\eta)}{3} + \frac{(\mathrm{KF})I_D}{f\, C_{ox}\, L^2}\right]\Delta f \quad (\mathrm{A}^2)$$

SPICE Level 3 Model

The large-signal model of the MOS device previously discussed neglects many important second-order effects. Most of these second-order effects are due to narrow or short channel dimensions (less than about 3μm). We shall also consider the effects of temperature upon the parameters of the MOS large signal model.

We first consider second-order effects due to small geometries. When v_{GS} is greater than V_T, the drain current for a small device can be given as

Drain Current

$$i_{DS} = \text{BETA}\left[v_{GS} - V_T - \left(\frac{1+f_b}{2}\right)v_{DE}\right]\cdot v_{DE} \tag{1}$$

$$\text{BETA} = \text{KP}\frac{W_{\text{eff}}}{L_{\text{eff}}} = \mu_{\text{eff}}\text{COX}\frac{W_{\text{eff}}}{L_{\text{eff}}} \tag{2}$$

$$L_{\text{eff}} = L - 2(\text{LD}) \tag{3}$$

$$W_{\text{eff}} = W - 2(\text{WD}) \tag{4}$$

$$v_{DE} = \min(v_{DS}\,,\, v_{DS}\,(\text{sat})) \tag{5}$$

$$f_b = f_n + \frac{\text{GAMMA}\cdot f_s}{4(\text{PHI}+v_{SB})^{1/2}} \tag{6}$$

Note that PHI is the SPICE model term for the quantity $2\phi_f$. Also be aware that PHI is always positive in SPICE regardless of the transistor type (p- or n-channel).

$$f_n = \frac{\text{DELTA}}{W_{\text{eff}}}\frac{\pi\varepsilon_{\text{si}}}{2\cdot\text{COX}} \tag{7}$$

$$f_s = 1 - \frac{x_j}{L_{\text{eff}}}\left\{\frac{\text{LD}+wc}{x_j}\left[1-\left(\frac{wp}{x_j+wp}\right)^2\right]^{1/2} - \frac{\text{LD}}{x_j}\right\} \tag{8}$$

$$wp = xd\,(\text{PHI}+v_{SB})^{1/2} \tag{9}$$

$$xd = \left(\frac{2\cdot\varepsilon_{si}}{q\cdot\text{NSUB}}\right)^{1/2} \tag{10}$$

$$wc = x_j\left[k_1 + k_2\left(\frac{wp}{x_j}\right) - k_3\left(\frac{wp}{x_j}\right)^2\right] \tag{11}$$

$k_1 = 0.0631353$, $k_2 = 0.08013292$, $k_3 = 0.01110777$

Threshold Voltage

$$V_T = V_{bi} - \left(\frac{\text{ETA}\cdot 8.15^{-22}}{C_{\text{ox}}\,L_{\text{eff}}^{3}}\right)v_{DS} + \text{GAMMA}\cdot f_s(\text{ PHI} + v_{SB})^{1/2} + f_n(\text{ PHI} + v_{SB}) \tag{12}$$

$$v_{bi} = \mathrm{v}_{fb} + \text{PHI} \tag{13}$$

or

$$v_{bi} = \text{VTO} - \text{GAMMA}\cdot\sqrt{\text{PHI}} \tag{14}$$

Saturation Voltage

$$v_{sat} = \frac{v_{gs} - V_T}{1 + f_b} \tag{15}$$

$$v_{DS}(\text{sat}) = v_{sat} + v_C - \left(v_{\text{sat}}^2 + v_C^2\right)^{1/2} \tag{16}$$

$$v_C = \frac{\text{VMAX}\cdot L_{\text{eff}}}{\mu_{\text{s}}} \tag{17}$$

If VMAX is not given, then $v_{DS}(\text{sat}) = v_{sat}$

Effective Mobility

$$\mu_s = \frac{\text{U0}}{1 + \text{THETA}\,(v_{GS} - V_T)} \text{ when VMAX} = 0 \tag{18}$$

$$\mu_{\text{eff}} = \frac{\mu_s}{1 + \dfrac{v_{DE}}{v_C}} \text{ when VMAX} > 0\text{; otherwise } \mu_{\text{eff}} = \mu_s \tag{19}$$

Channel-Length Modulation

When VMAX = 0

$$\Delta L = xd\left[\text{KAPPA}\ \ (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{20}$$

when VMAX > 0

$$\Delta L = -\frac{ep \cdot xd^{2}}{2} + \left[\left(\frac{ep \cdot xd^{2}}{2}\right)^{2} + \text{KAPPA} \cdot xd^{2} \cdot (v_{DS} - v_{DS}(\text{sat}))\right]^{1/2} \tag{21}$$

where

$$ep = \frac{v_C\,(v_C + v_{DS}(\text{sat}))}{L_{\text{eff}}\, v_{DS}\,(\text{sat})} \tag{22}$$

$$i_{DS} = \frac{i_{DS}}{1 - \Delta L} \tag{21}$$

Weak Inversion Model (Level 3)

In the SPICE Level 3 model, the transition point from the region of strong inversion to the weak inversion characteristic of the MOS device is designated as v_{on} and is greater than V_T. v_{on} is given by

$$v_{on} \ = \ V_T + fast \tag{1}$$

where

$$fast \ = \ \frac{kT}{q}\left[1 + \ \frac{q \cdot NFS}{\text{COX}} + \frac{\text{GAMMA} \cdot f_s\,(\text{PHI} + v_{SB})^{1/2} + f_n\,(\text{PHI} \ + v_{SB})}{2(\text{PHI} \ + v_{SB})}\right] \tag{2}$$

NFS is a parameter used in the evaluation of v_{on} and can be extracted from measurements. The drain current in the weak inversion region, v_{GS} less than v_{on}, is given as

$$i_{DS} \ = \ i_{DS}\,(v_{on}\,,\, v_{DE}\,,\, v_{SB})\, e^{\left(\frac{v_{GS} - v_{on}}{fast}\right)} \tag{3}$$

where i_{DS} is given as (from Eq. (1), Sec. 3.4 with v_{GS} replaced with v_{on})

$$i_{DS} = \text{BETA}\left[v_{on} - V_T - \left(\frac{1 + f_b}{2}\right)v_{DE}\right] \cdot v_{DE} \tag{4}$$

Typical Model Parameters Suitable for SPICE Simulations Using Level-3 Model (Extended Model). These Values Are Based upon a 0.8μm Si-Gate Bulk CMOS n-Well Process

Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	 P-Channel	Units
VTO	Threshold	0.7 ± 0.15	-0.7 ± 0.15	V
UO	mobility	660	210	cm^2/V-s
DELTA	Narrow-width threshold adjust factor	2.4	1.25	—
ETA	Static-feedback threshold adjust factor	0.1	0.1	—
KAPPA	Saturation field factor in channel-length modulation	0.15	2.5	1/V
THETA	Mobility degradation factor	0.1	0.1	1/V
NSUB	Substrate doping	3×10^{16}	6×10^{16}	cm^{-3}
TOX	Oxide thickness	140	140	Å
XJ	Mettallurgical junction depth	0.2	0.2	μm
WD	Delta width			μm
LD	Lateral diffusion	0.016	0.015	μm
NFS	Parameter for weak inversion modeling	7×10^{11}	6×10^{11}	cm^{-2}
CGSO		220×10^{-12}	220×10^{-12}	F/m
CGDO		220×10^{-12}	220×10^{-12}	F/m
CGBO		700×10^{-12}	700×10^{-12}	F/m
CJ		770×10^{-6}	560×10^{-6}	F/m^2
CJSW		380×10^{-12}	350×10^{-12}	F/m
MJ		0.5	0.5	
MJSW		0.38	0.35	
NFS	Parameter for weak inversion modeling	7×10^{11}	6×10^{11}	cm^{-2}

Temperature Dependence

The temperature-dependent variables in the models developed so far include the: Fermi potential, PHI, EG, bulk junction potential of the source-bulk and drain-bulk junctions, PB, the reverse currents of the pn junctions, I_S, and the dependence of mobility upon temperature. The temperature dependence of most of these variables is found in the equations given previously or from well-known expressions. The dependence of mobility upon temperature is given as

$$\mathrm{UO}(T) = \mathrm{UO}(T_0)\left(\frac{T}{T_0}\right)^{\mathrm{BEX}}$$

where BEX is the temperature exponent for mobility and is typically -1.5.

$$v_{therm}(T) = \frac{KT}{q}$$

$$\mathrm{EG}(T) = 1.16 - 7.02 \cdot 10^{-4} \cdot \left[\frac{T^{2}}{T + 1108.0}\right]$$

$$\mathrm{PHI}(T) = \mathrm{PHI}(T_0) \cdot \left(\frac{T}{T_0}\right) - v_{therm}(T)\left[3 \cdot \ln\left(\frac{T}{T_0}\right) + \frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)}\right]$$

$$v_{bi}(T) = v_{bi}(T_0) + \frac{\mathrm{PHI}(T) - \mathrm{PHI}(T_0)}{2} + \frac{\mathrm{EG}(T_0) - \mathrm{EG}(T)}{2}$$

$$\mathrm{VT0}(T) = v_{bi}(T) + \mathrm{GAMMA}\left[\sqrt{\mathrm{PHI}(T)}\right]$$

$$\mathrm{PHI}(T) = 2 \cdot v_{therm} \ln\left(\frac{\mathrm{NSUB}}{n_i(T)}\right)$$

$$n_{i(T)} = 1.45 \cdot 10^{16} \cdot \left(\frac{T}{T_0}\right)^{3/2} \cdot \exp\left[\mathrm{EG} \cdot \left(\frac{T}{T_0} - 1\right) \cdot \left(\frac{1}{2 \cdot v_{therm}(T_0)}\right)\right]$$

For drain and source junction diodes, the following relationships apply.

$$\mathrm{PB}(T) = \mathrm{PB} \cdot \left(\frac{T}{T_0}\right) - v_{therm}(T)\left[3 \cdot \ln\left(\frac{T}{T_0}\right) + \frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)}\right]$$

$$I_S(T) = \frac{I_S(T_0)}{\mathrm{N}} \cdot exp\left[\frac{\mathrm{EG}(T_0)}{v_{therm}(T_0)} - \frac{\mathrm{EG}(T)}{v_{therm}(T)} + 3 \cdot \ln\left(\frac{T}{T_0}\right)\right]$$

where N is diode emission coefficient. The nominal temperature, T_0, is 300 K.

SPICE Simulation of MOS Circuits

Minimum required terms for a transistor instance follows:

M1 3 6 7 0 NCH W=100U L=1U

“M,” tells SPICE that the instance is an MOS transistor (just like “R” tells SPICE that an instance is a resistor). The “1” makes this instance unique (different from M2, M99, etc.)

The four numbers following”M1” specify the nets (or nodes) to which the drain, gate, source, and substrate (bulk) are connected. These nets have a specific order as indicated below:

M<number> <DRAIN> <GATE> <SOURCE> <BULK> ...

Following the net numbers, is the model name governing the character of the particular instance. In the example given above, the model name is “NCH.” There must be a model description of “NCH.”

The transistor width and length are specified for the instance by the “W=100U” and “L=1U” expressions.

The default units for width and length are meters so the “U” following the number 100 is a multiplier of 10^{-6}. [Recall that the following multipliers can be used in SPICE: M, U, N, P, F, for 10^{-3}, 10^{-6}, 10^{-9}, 10^{-12} , 10^{-15} , respectively.]

Additional information can be specified for each instance. Some of these are

- Drain area and periphery (AD and PD) ← calc depl cap and leakage
- Source area and periphery (AS and PS) ← calc depl cap and leakage
- Drain and source resistance in squares (NRD and NRS)
- Multiplier designating how many devices are in parallel (M)
- Initial conditions (for initial transient analysis)

The number of squares of resistance in the drain and source (NRD and NRS) are used to calculate the drain and source resistance for the transistor.

Geometric Multiplier: M

To apply the “unit-matching” principle, use the geometric multiplier feature rather than scale W/L.

This:

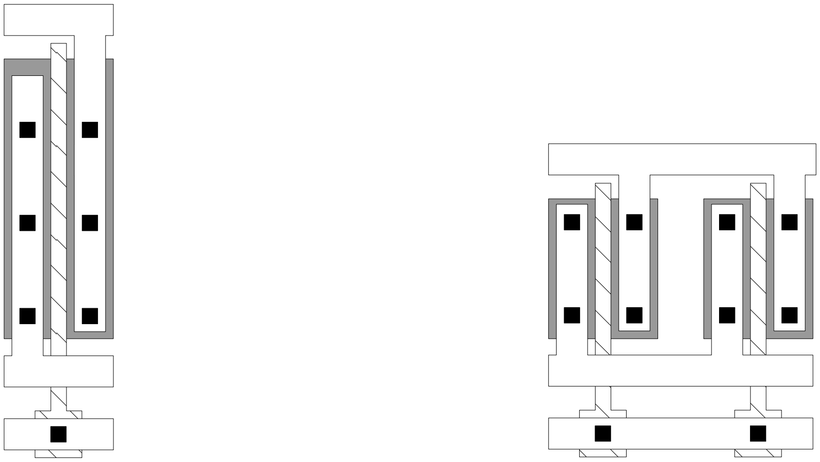
```
M1 3 2 1 0 NCH W=20U L=1U
```

is not the same as this:

```
M1 3 2 1 0 NCH W=10U L=1U M=2
```

The following dual instantiation is equivalent to using a multiplier

```
M1A 3 2 1 0 NCH W=10U L=1U
M1B 3 2 1 0 NCH W=10U L=1U
```



(a)M1 3 2 1 0 NCH W=20U L=1U. (b) M1 3 2 1 0 NCH W=10U L=1U M=1.
.

MODEL Description

A SPICE simulation file for an MOS circuit is incomplete without a description of the model to be used to characterize the MOS transistors used in the circuit. A model is described by placing a line in the simulation file using the following format.

```
.MODEL <MODEL NAME> <MODEL TYPE> <MODEL PARAMETERS>
```

MODEL NAME e.g., “NCH”
MODEL TYPE either “PMOS” or “NMOS.”

MODEL PARAMETERS :

```
     LEVEL=1 VTO=1 KP=50U GAMMA=0.5 LAMBDA=0.01
```

SPICE can calculate what you do not specify

You must specify the following

- surface state density, NSS, in cm^{-2}
- oxide thickness, TOX, in meters
- surface mobility, UO, in cm^2/V-s,
- substrate doping, NSUB, in cm^{-3}

The equations used to calculate the electrical parameters are

$$\text{VTO} = \phi_{MS} - \frac{q(\text{NSS})}{(\varepsilon_{ox}/\text{TOX})} + \frac{(2q \cdot \varepsilon_{si} \cdot \text{NSUB} \cdot \ \text{PHI})^{1/2}}{(\varepsilon_{ox}/\text{TOX})} + \text{PHI}$$

$$\text{KP} = \text{UO}\,\frac{\varepsilon_{ox}}{\text{TOX}}$$

$$\text{GAMMA} = \frac{(2q \cdot \varepsilon_{si} \cdot \text{NSUB})^{1/2}}{(\varepsilon_{ox}/\text{TOX})}$$

and

$$\text{PHI} = \left| \, 2\phi_F \, \right| = \frac{2kT}{q} \ln\left(\frac{\text{NSUB}}{n_i}\right)$$

LAMBDA is not calculated from the process parameters for the LEVEL 1 model.

Other parameters:

IS: Reverse current of the drain-bulk or source-bulk junctions in Amps

JS: Reverse-current density in A/m^2

JS requires the specification of AS and AD on the model line. If IS is specified, it overrides JS. The default value of IS is usually 10^{-14} A.

RD: Drain ohmic resistance in ohms

RS: Source ohmic resistance in ohms

RSH: Sheet resistance in ohms/square. RSH is overridden if RD or RS are entered. To use RSH, the values of NRD and NRS must be entered on the model line.

The drain-bulk and source-bulk depletion capacitors
CJ: Bulk bottom plate junction capacitance
MJ: Bottom plate junction grading coefficient
CJSW: Bulk sidewall junction capacitance
MJSW: Sidewall junction grading coefficient

If CJ is entered as a model parameter it overrides the calculation of CJ using NSUB, otherwise, CJ is calculated using NSUB.

If CBD and CBS are entered, these values override CJ and NSUB calculations.

In order for CJ to result in an actual circuit capacitance, the transistor instance must include AD and AS.

In order for CJSW to result in an actual circuit capacitance, the transistor instance must include PD and PS.

CGSO: Gate-Source overlap capacitance (at zero bias)
CGDO: Gate-Drain overlap capacitance (at zero bias)

AF: Flicker noise exponent
KF: Flicker noise coefficient

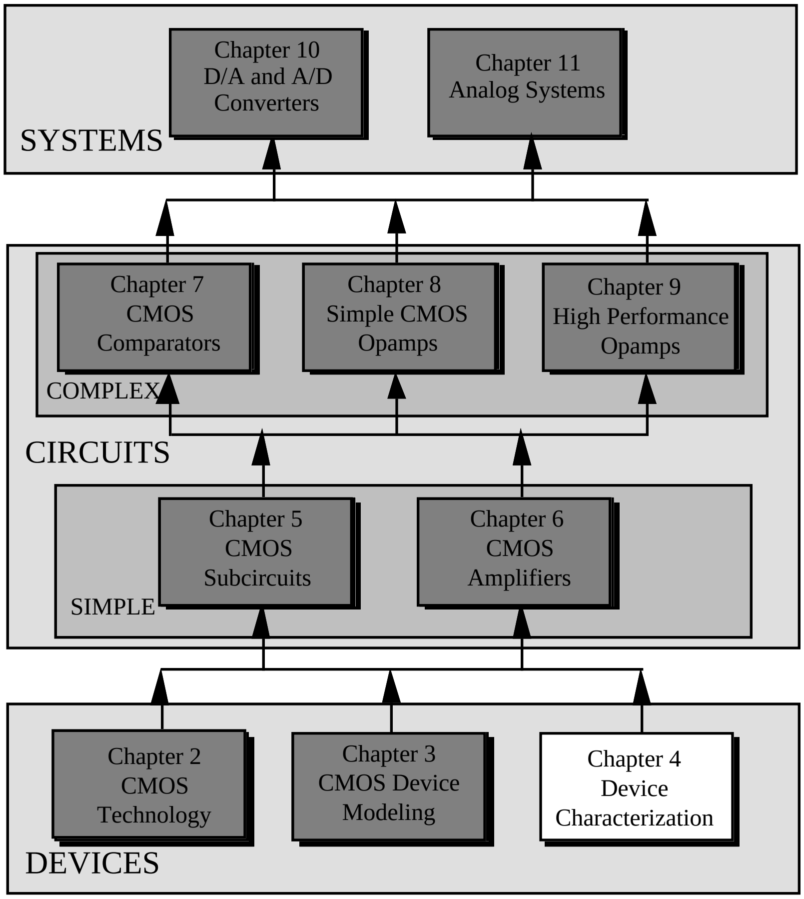
TPG: Indicates type of gate material relative to the substrate
TPG=1 > gate material is opposite of the substrate
TPG=-1 > gate material is the same as the substrate
TPG=0 > gate material is aluminum

XQC: Channel charge flag and fraction of channel charge attributed to the drain

IV. CMOS PROCESS CHARACTERIZATION

Contents

Organization



I. Characterization of the Simple Transistor Model

Determine $V_{T0}(V_{SB} = 0)$, K', γ, and λ.
Terminology:
K'_S for the saturation region
K'_L for the nonsaturation region

$$i_D = K'_S \left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_T)^2 \,(1 + \lambda\, v_{DS}) \tag{1}$$

$$i_D = K'_L \left(\frac{W_{\text{eff}}}{L_{\text{eff}}}\right)\left[(v_{GS} - V_T)\, v_{DS} - \frac{v_{DS}^2}{2}\right] \tag{2}$$

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_{\text{F}}| + v_{SB}} - \sqrt{2|\phi_{\text{F}}|}\,\right] \tag{3}$$

Assume that v_{DS} is chosen such that the $\lambda\, v_{DS} << 1$
$v_{SB} = 0 \to V_T = V_{T0}$.

Therefore, Eq. (1) simplifies to

$$i_D = K'_S \left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_{T0})^2 \tag{4}$$

This equation can be manipulated algebraically to obtain the following

$$i_D^{1/2} = \left(\frac{K'_S\, W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} v_{GS} - \left(\frac{K'_S\, W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0} \tag{5}$$

which has the form

$$y = mx + b \tag{6}$$

$$y = i_D^{1/2} \tag{7}$$

$$x = v_{GS} \tag{8}$$

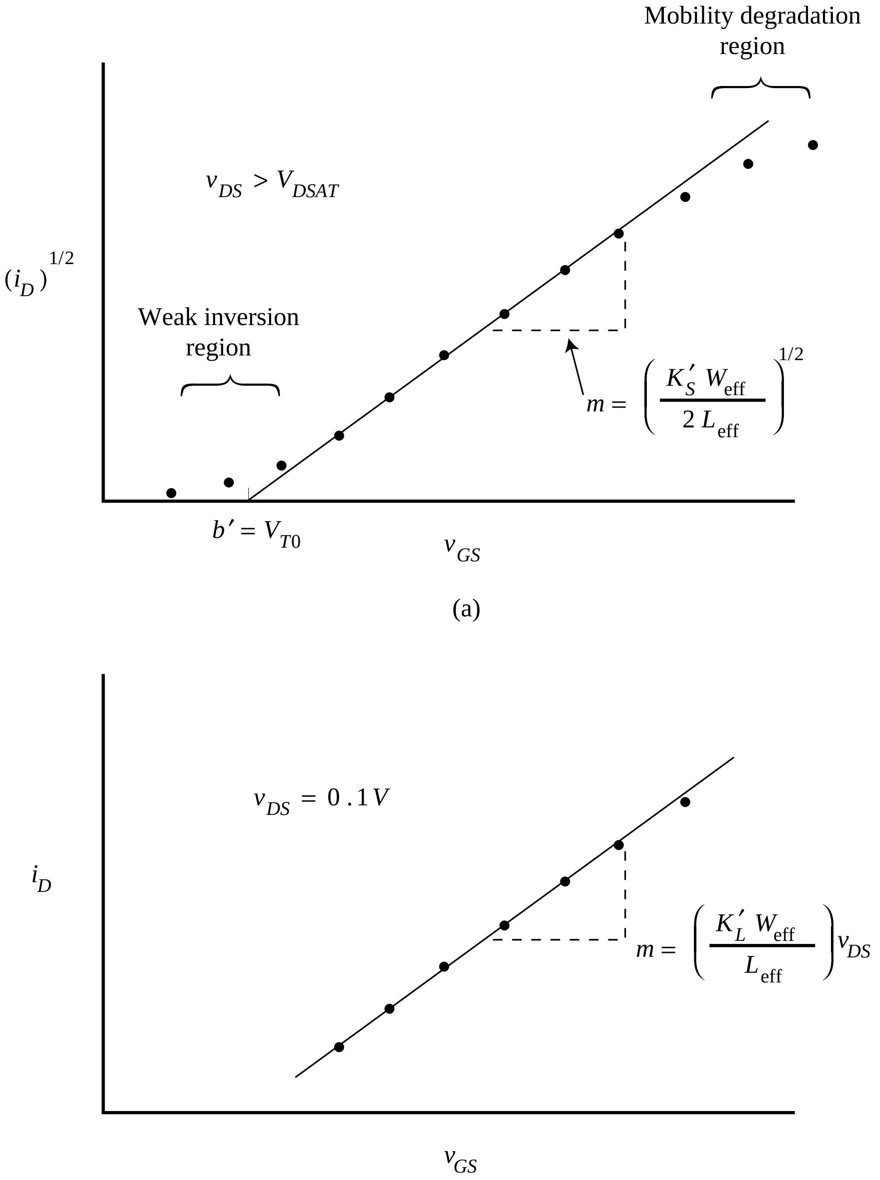
$$m = \left(\frac{K'_S\ W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} \tag{9}$$

and

$$b = -\left(\frac{K'_S\ W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0} \tag{10}$$

Plot $i_D^{1/2}$ versus v_{GS} and measure slope. to get K'_S

When $i_D^{1/2} = 0$ the x intercept (b') is V_{T0}.



(a)

(b)

Figure B.1-1 (a) $i_D^{1/2}$ versus v$_{GS}$ plot used to determine V_{T0} and K'_S. (b) i_D versus v_{GS} plot to determine K'_L.

Extract the parameter K'_L for the nonsaturation region:

$$i_D = K'_L \left(\frac{W_{\text{eff}}}{L_{\text{eff}}}\right) v_{DS}\, v_{GS} - K'_L \left(\frac{W_{\text{eff}}}{L_{\text{eff}}}\right) v_{DS} \left(V_T + \frac{v_{DS}}{2}\right) \qquad (11)$$

Plot i_D versus v_{GS} as shown in Fig. B.1-1(b), the slope is seen to be

$$m = \frac{\Delta i_D}{\Delta v_{GS}} = K'_L\left(\frac{W_{\text{eff}}}{L_{\text{eff}}}\right) v_{DS} \tag{12}$$

Knowing the slope, the term K'_L is easily determined to be

$$K'_L = m\left(\frac{L_{\text{eff}}}{W_{\text{eff}}}\right)\left(\frac{1}{v_{DS}}\right) \tag{13}$$

W_{eff}, L_{eff}, and v_{DS} must be known.

The approximate value μ_o can be extracted from the value of K'_L

At this point, γ is unknown.

Write Eq. (3) in the linear form where

$$y = V_T \tag{14}$$

$$x = \sqrt{2|\phi_{\text{F}}| + v_{SB}} - \sqrt{2|\phi_{\text{F}}|} \tag{15}$$

$$m = \gamma \tag{16}$$

$$b = V_{T0} \tag{17}$$

$2|\phi_{\text{F}}|$ normally in the range of 0.6 to 0.7 volts.

Determine V_T at various values of v_{SB}

Plot V_T versus x and measure the slope to extract γ

Slope m, measured from the best fit line, is the parameter γ.

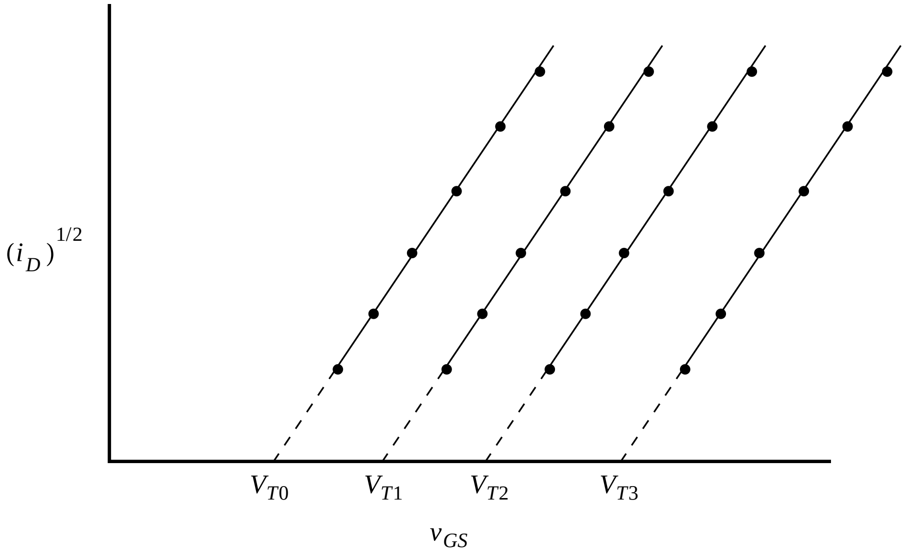


Figure B.1-2 $i_D^{1/2}$ versus v_{GS} plot at different v_{SB} values to determine γ.

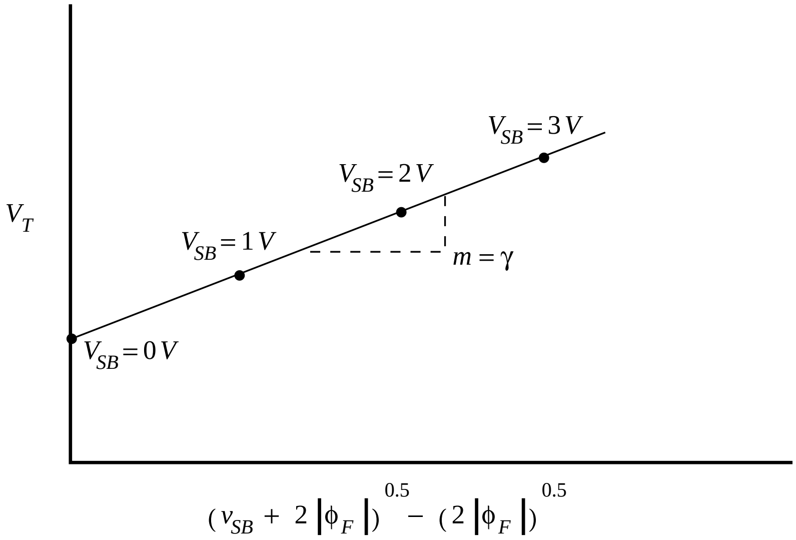


Figure B.1-3 Plot of V_T versus $f(v_{SB})$ to determine γ.

We still need to find λ, ΔL, and ΔW.
λ should be determined for all device lengths that might be used.

Rewrite Eq. (1) is as

$$i_D = i'_D \lambda v_{DS} + i'_D \qquad (18)$$

which is in the familiar linear form where

$$y = i_D \quad \text{(Eq. (1))} \tag{19}$$

$$x = v_{DS} \tag{20}$$

$$m = \lambda\, i'_D \tag{21}$$

$$b = i'_D \quad \text{(Eq. (4) with } \lambda = 0\text{)} \tag{22}$$

Plot i_D versus v_{DS}, and measure the slope of the data in the saturation region, and divide that value by the y-intercept to getλ.

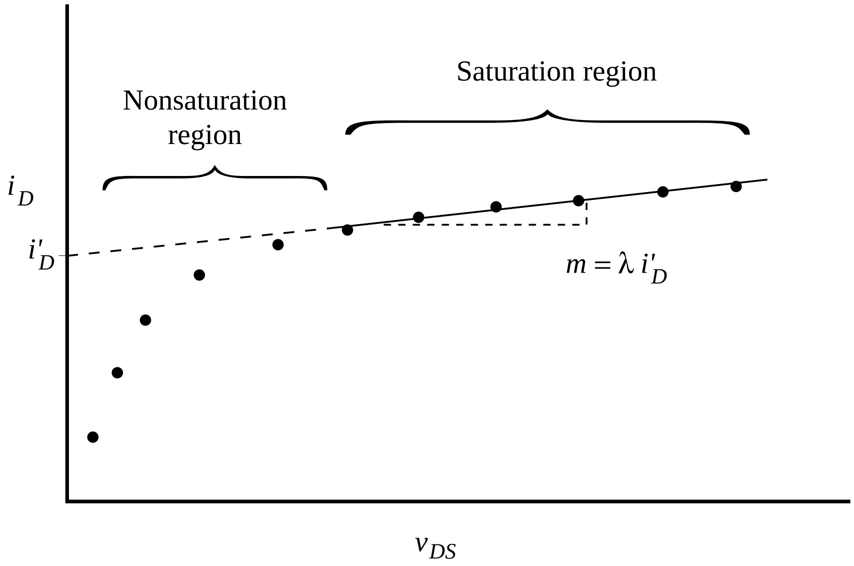


Figure B.1-4 Plot of i_D versus v_{DS} to determine λ.

Calculating ΔL and ΔW.

Consider two transistors, with the same widths but different lengths, operating in the nonsaturation region with the same v_{DS}. The widths of the transistors are assumed to be very large so that $W \cong W_{\text{eff}}$. The large-signal model is given as

$$i_D = \frac{K'_L W_{\text{eff}}}{L_{\text{eff}}}\left[(v_{GS} - V_{T0})v_{DS} - \left(\frac{v_{DS}^2}{2}\right)\right] \tag{23}$$

and

$$\frac{\partial I_D}{\partial V_{GS}} = g_m = \left(\frac{K'_L\ W_{\mathrm{eff}}}{L_{\mathrm{eff}}}\right) V_{DS} \tag{24}$$

The aspect ratios (W/L) for the two transistors are

$$\frac{W_1}{L_1 + \Delta L} \tag{25}$$

and

$$\frac{W_2}{L_2 + \Delta L} \tag{26}$$

Implicit in Eqs. (25) and (26) is that ΔL is assumed to be the same for both transistors. Combining Eq. (24) with Eqs. (25) and (26) gives

$$g_{m1} = \frac{K'_L W}{L_1 + \Delta L}\ v_{DS} \tag{27}$$

and

$$g_{m2} = \frac{K'_L W}{L_2 + \Delta L}\ v_{DS} \tag{28}$$

where $W_1 = W_2 = W$ (and are assumed to equal the effective width). With further algebraic manipulation of Eqs. (27) and (28), one can show that,

$$\frac{g_{m1}}{g_{m1} - g_{m2}} = \frac{L_2 + \Delta L}{L_2 - L_1} \tag{29}$$

which further yields

$$L_2 + \Delta L = L_{\mathrm{eff}} = \frac{(L_2 - L_1)\ g_{m1}}{g_{m1} - g_{m2}} \tag{30}$$

L_2 and L_1 known

g_{m1} and g_{m2} can be measured

Similarly for W_{eff} :

$$W_2 + \Delta W = W_{\mathrm{eff}} = \frac{(W_1 - W_2) g_{m2}}{g_{m1} - g_{m2}} \tag{31}$$

Equation (31) is valid when two transistors have the same length but different widths.

One must be careful in determining ΔL (or ΔW) to make the lengths (or widths) sufficiently different in order to avoid the numerical error due to subtracting large numbers, and small enough that the transistor model chosen is still valid for both transistors.

II. Transistor Characterization for the Extended Model

Equations (1) and (2) represent a simplified version of the extended model for a relatively wide MOS transistor operating in the nonsaturation, strong-inversion region with $V_{SB} = 0$.

$$i_D = \frac{\mu_S C_{ox} W}{L}\left[(v_{GS} - V_T)v_{DS} - \left(\frac{v_{DS}^2}{2}\right) + \gamma v_{DS}\sqrt{2|\phi_F|} - \left(\frac{2\gamma}{3}\right)[(v_{DS} + 2|\phi_F|)^{1.5} - (2|\phi_F|)]^{1.5}\right] \qquad (1)$$

where W and L are effective electrical equivalents (dropping the subscript, "eff", for convenience).

$$\mu_S = \mu_O\left[\frac{(\text{UCRIT})\varepsilon_{Si}}{Cox[v_{GS} - V_T - (\text{UTRA})v_{DS}]}\right]^{\text{UEXP}} \qquad (2)$$

Eq. (2) holds when the denominator term in the brackets is less than unity. Otherwise, $\mu_O = \mu_S$. To develop a procedure for extracting μ_O, consider the case where mobility degradation effects are not being experienced, i.e., $\mu_S = \mu_O$, Eq. (1) can be rewritten in general as

$$i_D = \mu_O f(C_{ox}, W, L, v_{GS}, V_T, v_{DS}, \gamma, 2|\phi_F|) \qquad (3)$$

This equation is a linear function of v_{GS} and is in the familiar form of

$$y = mx + b \qquad (4)$$

where $b = 0$.

Plot i_D versus the function, $f(\mathrm{C_{ox}}, W, L, v_{GS}, V_T, v_{DS}, \gamma, 2|\phi_F|)$ and measure the slope = μ_O.

- The data are limited to the nonsaturation region (small v_{DS}).
- The transistor must be in the strong-inversion region ($v_{GS} > V_T$).
- The transistor must operate below the critical-mobility point.

Keep v_{GS} as low as possible without encroaching on the weak-inversion region of operation.

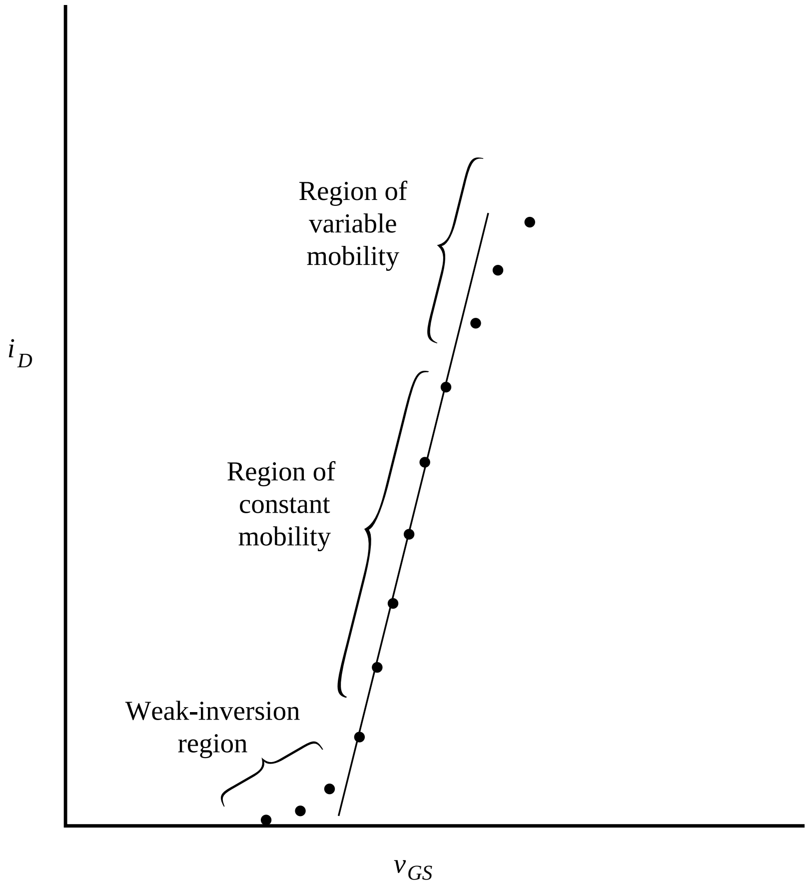


Figure B.2-1 Plot of i_D versus v_{GS} in the nonsaturation region.

Once μ_o is determined, there is ample information to determine UCRIT and UEXP. Consider Eqs. (1) and (2) rewritten and combined as follows.

$$i_D = \mu_o[(\mathrm{UCRIT})f_2]^{\mathrm{UEXP}}f_1 \tag{5}$$

where

$$f_1 = \frac{C_{ox}W}{L}\Bigg[(v_{GS} - V_T)v_{DS} - \left(\frac{v_{DS}^2}{2}\right) + \gamma v_{DS}\sqrt{2|\phi_\mathrm{F}|} - \left(\frac{2\gamma}{3}\right)[(v_{DS} + 2|\phi_\mathrm{F}|)^{1.5} - (2|\phi_\mathrm{F}|)]^{1.5}\Bigg] \tag{1}$$

and

$$f_2 = \frac{\varepsilon_{si}}{[v_{GS} - V_T - (\mathrm{UTRA})v_{DS}]C_{ox}} \tag{7}$$

The units of f_1 and f_2 are FV^2/cm^2 and cm/V respectively. Notice that f_2 includes the parameter UTRA, which is an unknown. UTRA is disabled in most SPICE models.

Equation (5) can be manipulated algebraically to yield

$$\log\left(\frac{i_D}{f_1}\right) = \log(\mu_o) + \mathrm{UEXP}[\log(\mathrm{UCRIT})] + \mathrm{UEXP}[\log(f_2)] \tag{8}$$

This is in the familiar form of Eq. (4) with

$$x = \log(f_2) \tag{9}$$

$$y = \log\left(\frac{i_D}{f_1}\right) \tag{10}$$

$$m = \mathrm{UEXP} \tag{11}$$

$$b = \log(\mu_o) + \mathrm{UEXP}[\log(\mathrm{UCRIT})] \tag{12}$$

By plotting Eq. (8) and measuring the slope, UEXP can be determined. The y-intercept can be extracted from the plot and UCRIT can be determined by back calculation given UEXP, μ_o, and the intercept, b.

III. Characterization of Substrate Bipolar

Parameters of interest are: β_{dc}, and J_S.

For $v_{BE} >> kT/q$,

$$v_{BE} = \frac{kT}{q} \ln\left(\frac{i_C}{J_S A_E}\right) \quad (1)$$

and

$$\beta_{\mathrm{dc}} = \frac{i_E}{i_B} - 1 \quad (2)$$

A_E is the cross-sectional area of the emitter-base junction of the BJT.

$$i_E = i_B(\beta_{\mathrm{dc}} + 1) \quad (3)$$

Plot i_B as a function of i_E and measure the slope to determine β_{dc}.

Once β_{dc} is known, then Eq. (1) can be rearranged and modified as follows.

$$v_{BE} = \frac{kT}{q} \ln\left(\frac{i_E \beta_{\mathrm{dc}}}{1 + \beta_{\mathrm{dc}}}\right) - \frac{kT}{q} \ln(J_S A_E) = \frac{kT}{q} \ln(\alpha_{\mathrm{dc}} i_E) - \frac{kT}{q} \ln(J_S A_E)$$

Plotting $\ln[i_E \beta_{\mathrm{dc}}/(1 + \beta_{\mathrm{dc}})]$ versus v_{BE} results in a graph where

$$m = \text{slope} = \frac{kT}{q} \quad (5)$$

and

$$b = y\text{-intercept} = -\left(\frac{kT}{q}\right) \ln(J_S A_E) \quad (6)$$

Since the emitter area is known, J_S can be determined directly.

IV. Characterization of Resistive Components

- Resistors
- Contact resistance

Characterize the resistor geometry exactly as it will be implemented in a design. Because

- sheet resistance is not constant across the width of a resistor
- the effects of bends result in inaccuracies
- termination effects are not accurately predictable

Figure B.5-1 illustrates a structure that can be used to determine sheet resistance, and geometry width variation (bias).
Force a current into node *A* with node *F* grounded while measuring the voltage drops across *BC* (V_n) and *DE* (V_W), the resistors R_n and R_W can be determined as follows

$$R_n = \frac{V_n}{I} \qquad (1)$$

$$R_W = \frac{V_W}{I} \qquad (2)$$

The sheet resistance can be determined from these to be

$$R_S = R_n \left(\frac{W_n \text{ - Bias}}{L_n} \right) \qquad (3)$$

$$R_S = R_W \left(\frac{W_W \text{ - Bias}}{L_W} \right) \qquad (3)$$

where

R_n = resistance of narrow resistor (Ω)

R_W = resistance of wide resistor (Ω)

R_S = sheet resistance of material (polysilicon, diffusion etc. Ω/square)

L_n = drawn length of narrow resistor

L_W = drawn length of wide resistor

W_n = drawn width of narrow resistor

W_W = drawn width of wide resistor

Bias = difference between drawn width and actual device width

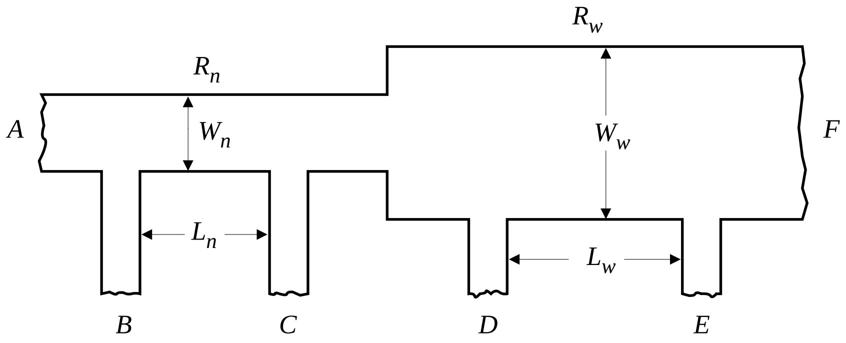


Figure B.5-1 Sheet resistance and bias monitor.

Solving equations (3) and (4) yields

$$\text{Bias} = \frac{W_n - k\ W_W}{1 - k} \tag{5}$$

where

$$k = \frac{R_W L_n}{R_n L_W} \tag{6}$$

and

$$R_S = R_n \left(\frac{W_n - \text{Bias}}{L_n}\right) = R_W \left(\frac{W_W - \text{Bias}}{L_W}\right) \tag{7}$$

Determining sheet resistance and contact resistance

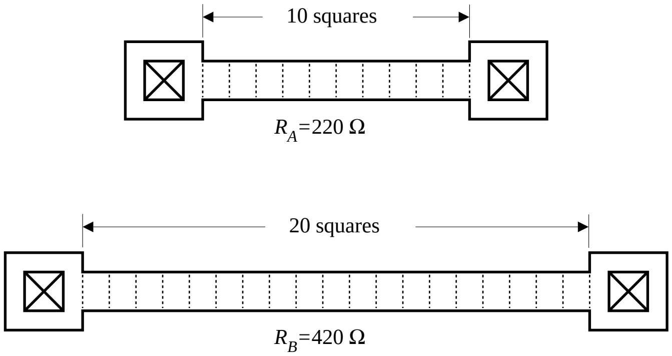


Figure B.5-2 Two resistors used to determine R_S and R_C.

$$R_A = R_1 + 2R_C; \qquad R_1 = N_1 R_S \tag{8}$$

and

$$R_B = R_2 + 2R_C; \qquad R_2 = N_2 R_S \tag{9}$$

N_1 is the number of squares for R_1
R_S is the sheet resistivity in Ω/square
R_C is the contact resistance.

$$R_S = \frac{R_B - R_A}{N_2 - N_1} \tag{10}$$

and

$$2R_C = R_A - N_1 R_S = R_B - N_2 R_S \tag{11}$$

Voltage coefficient of lightly-doped resistors

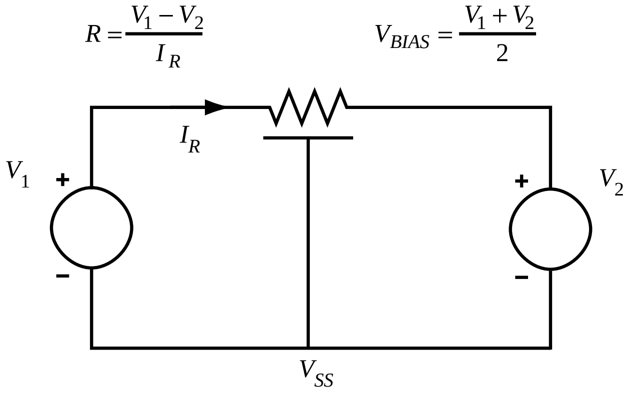


Figure B.5-3 N-well resistor illustrating back-bias dependence.

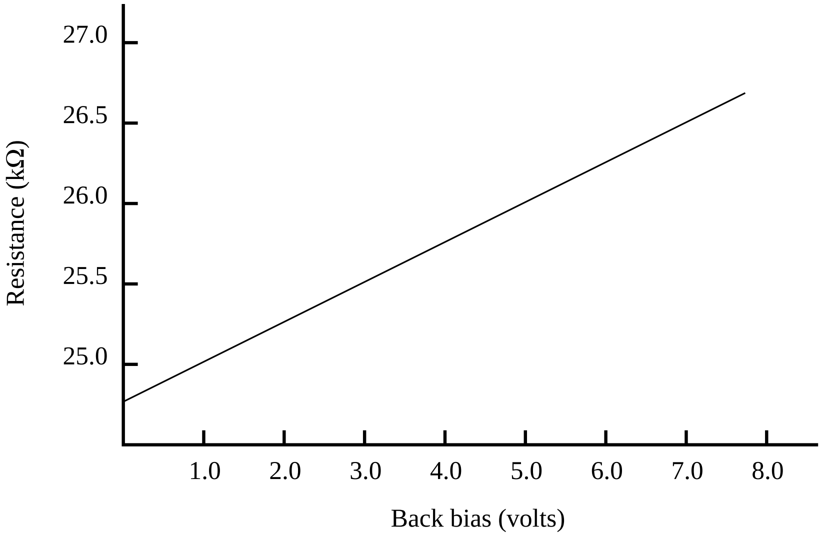
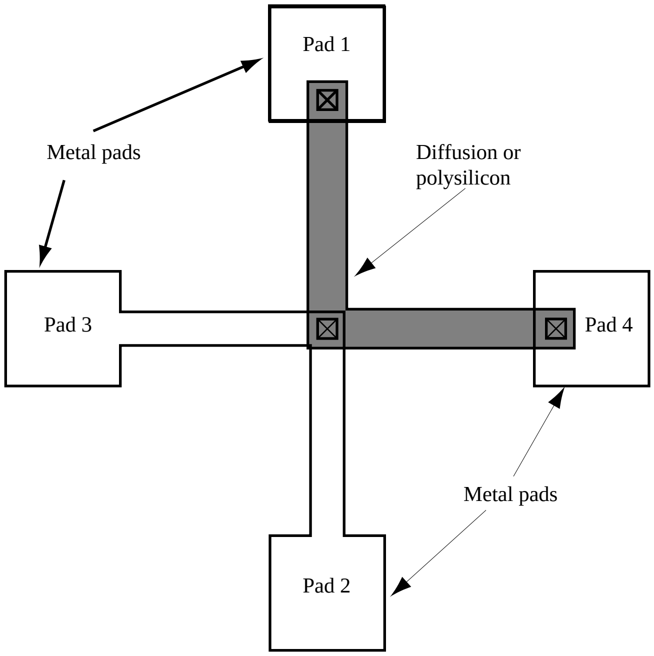
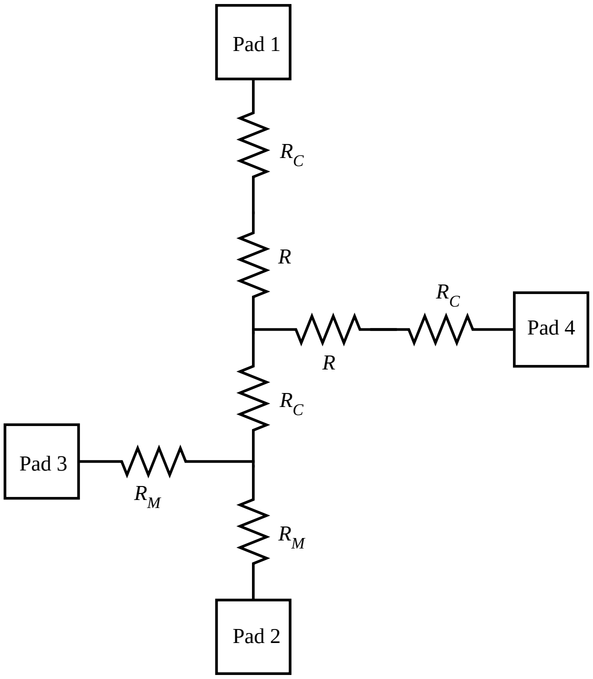


Figure B.5-4 N-well resistance as a function of back-bias voltage

Contact Resistance





V. Characterization of Capacitance

MOS capacitors

C_{GS}, C_{GD}, and C_{GB}

Depletion capacitors

C_{DB} and C_{SB}

Interconnect capacitances

$C_{\text{poly-field}}$, $C_{\text{metal-field}}$, and $C_{\text{metal-poly}}$ (and perhaps multi-metal capacitors

SPICE capacitor models

C_{GS0}, C_{GD0}, and C_{GB0} (at $V_{GS} = V_{GB} = 0$).

Normally SPICE calculates C_{DB} and C_{SB} using the areas of the drain and source and the junction (depletion) capacitance, C_J (zero-bias value), that it calculates internally from other model parameters. Two of these model parameters, *MJ* and *MJSW*, are used to calculate the depletion capacitance as a function of voltage across the capacitor.

C_{GS0}, C_{GD0}, and C_{GB0}

C_{GS0} and C_{GD0}, are modeled in SPICE as a function of the device width, while the capacitor C_{GB0} is per length of the device

Measure the C_{GS} of a very wide transistor and divide the result by the width in order to get C_{GS0} (per unit width).

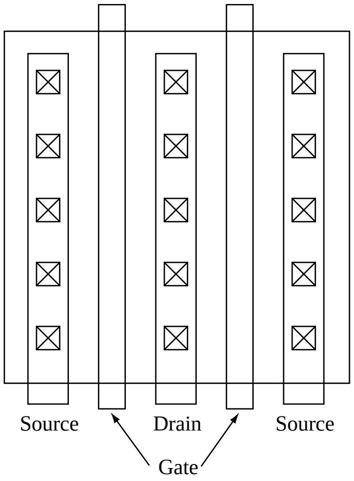


Figure B.6-1 Structure for determining C_{GS} and C_{GD}.

$$C_{\text{meas}} = W(n)(C_{GS0} + C_{GD0}) \tag{1}$$

where

C_{meas} = total measured capacitance

W = total width of one of the transistors

n = total number of transistors

For very narrow transistors, the capacitance determined using the previous technique will not be very accurate because of fringe field and other edge effects at the edge of the transistor. In order to characterize C_{GS0} and C_{GD0} for these narrow devices, a structure similar to that given in Fig. B.6-1 can be used, substituting different device sizes. Such a structure is given in Fig. B.6-3. The equations used to calculate the parasitic capacitances are the same as those given in Eq. (1).

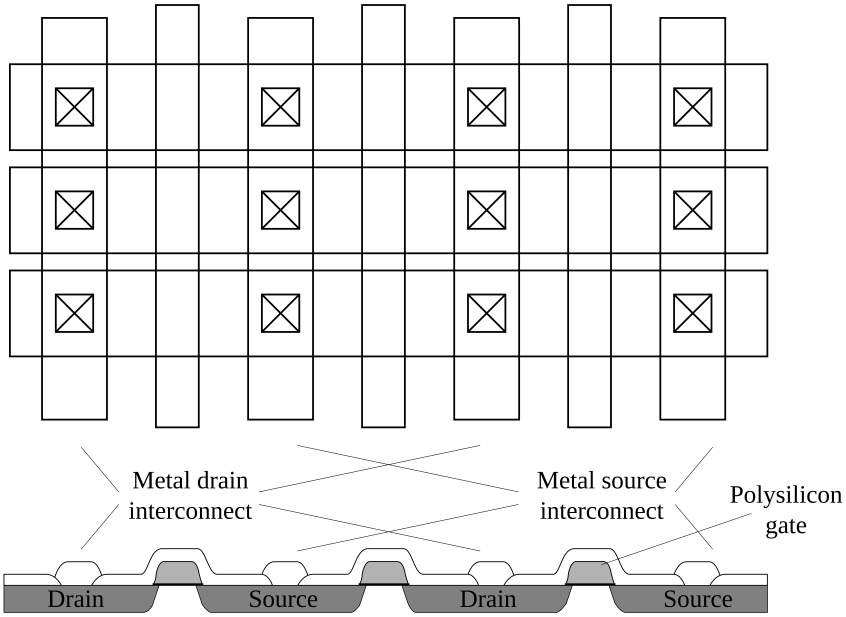


Figure B.6-3 Structure for measuring C_{GS} and C_{GD}, including fringing effects, for transistors having small L.

C_{GB0}

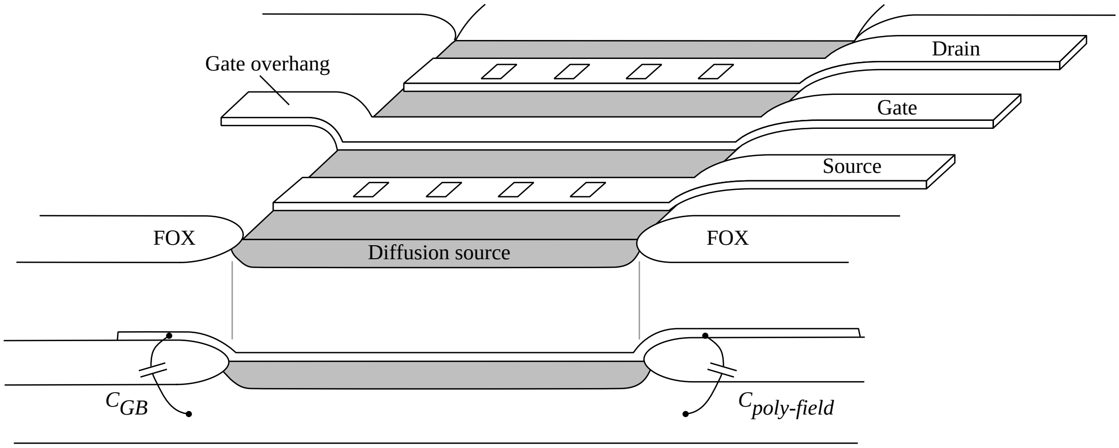


Figure B.6-4 Illustration of gate-to-bulk and poly-field capacitance.

This capacitance is approximated from the interconnect capacitance $C_{\text{poly-field}}$ (overhang capacitor is not a true parallel-plate capacitor)

$$C_{\text{poly-field}} = \frac{C_{\text{meas}}}{L_R W_R} \qquad (\text{F/m}^2) \qquad (2)$$

where

$C_{\text{meas}} = C_{\text{meas}}$ = measured value of the polysilicon strip

L_R = length of the centerline of the polysilicon strip

W_R = width of the polysilicon strip (usually chosen as device length)

Having determined $C_{\text{poly-field}}$, C_{GB0} can be approximated as

$$C_{GB0} \cong 2\,(C_{\text{poly-field}})(d_{\text{overhang}}) = 2\mathrm{C}_5 \ (\text{F/m}) \qquad (3)$$

where

d_{overhang} = overhang dimension (see Rule 3D, Table 2.6-1)

C_{BD} and C_{BS}

$$C_J(V_J) = AC_J(0)\left(1 \ + \ \frac{V_J}{PB}\right)^{-MJ} + PC_{JSW}(0)\left(1 \ + \ \frac{V_J}{PB}\right)^{-MJSW} \qquad (4)$$

where

V_J = the reverse bias voltage across the junction

$C_J(V_J)$ = bottom junction capacitance at V_J

$C_{JSW}(V_J)$ = junction capacitance of sidewall at V_J

A = area of the (bottom) of the capacitor

P = perimeter of the capacitor

PB = bulk junction potential

The constants C_J and MJ can be determined by measuring a large rectangular capacitor structure where the contribution from the sidewall capacitance is minimal. For such a structure, $C_J(V_J)$ can be approximated as

$$C_J(V_J) = AC_J(0)\left(1 \ + \ \frac{V_J}{PB}\right)^{-MJ} \qquad (5)$$

This equation can be rewritten in a way that is convenient for linear regression.

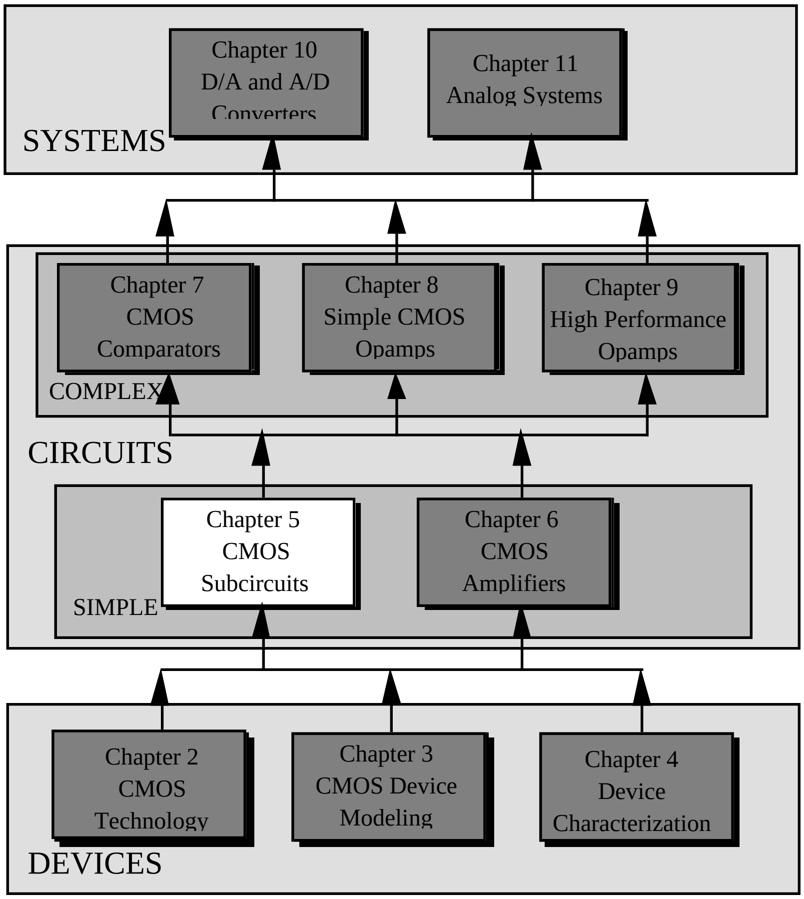
$$\log[C_J(V_J)] = (-MJ)\log\left(1 \ + \ \frac{V_J}{PB}\right) + \log[AC_J(0)] \qquad (6)$$

Plotting $\log[C_J(V_J)]$ versus $\log[1 + V_J/PB]$ and determine the slope, $-MJ$, and the Y intercept (where Y is the term on the left), $\mathrm{Log}[AC_J(0)]$. Knowing the area of the capacitor, the calculation of the bottom junction capacitance is straightforward.

V. CMOS SUBCIRCUITS

Contents

Organization



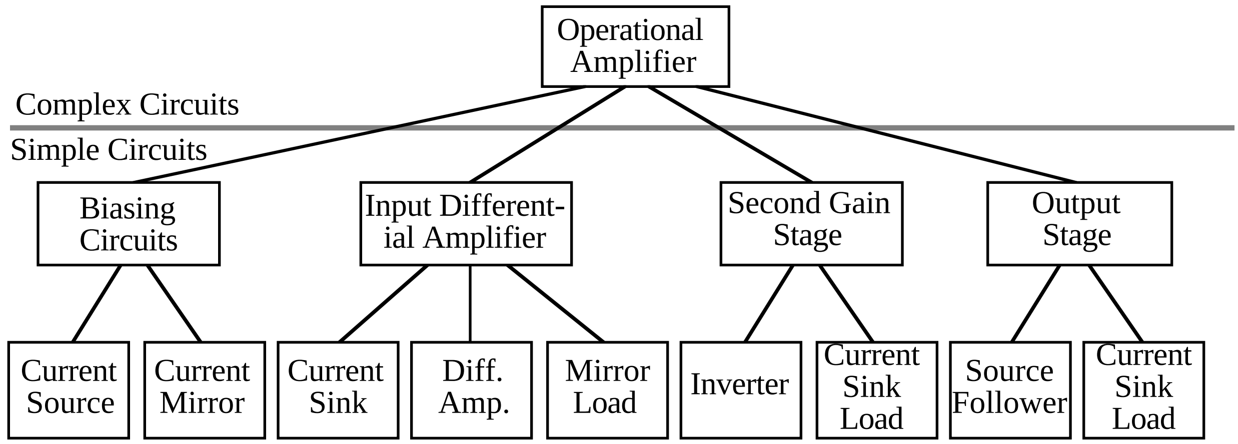
WHAT IS A SUBCIRCUIT?

A subcircuit is a circuit which consists of one or more transistors and generally perfoms only one function.

A subcircuit is generally not used by itself but in conjunction with other subcircuits.

Example

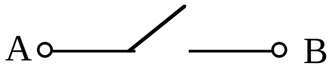
Design hierarchy of analog circuits illustrated by an op amp.



V.1 - MOS SWITCH

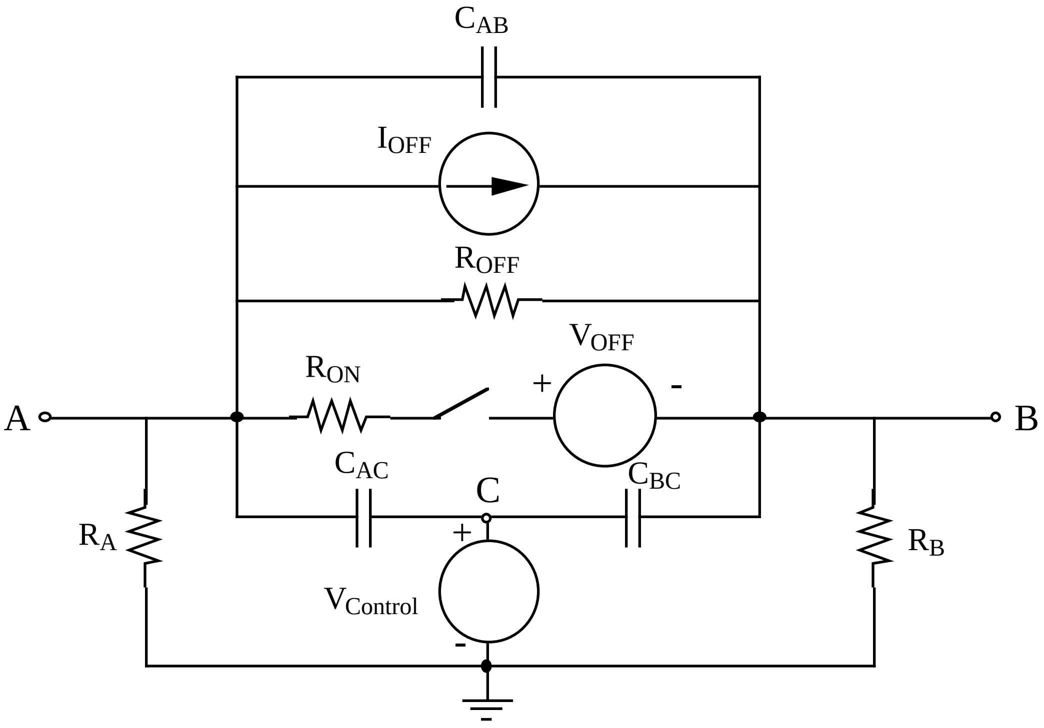
SWITCH PROPERTIES

Ideal Switch



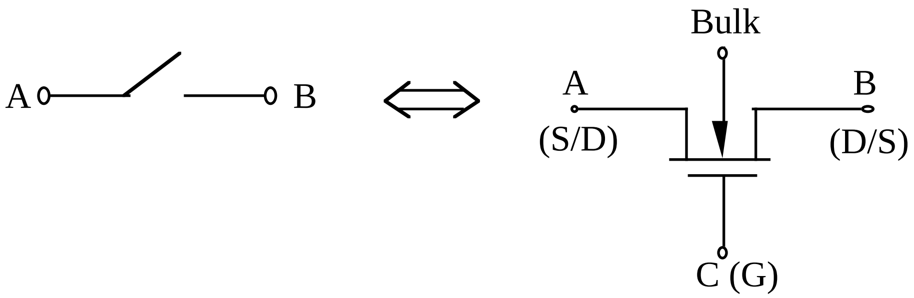
$$\begin{cases} R_{AB}(\text{on}) = 0\Omega \\ R_{AB}(\text{off}) = \infty \end{cases}$$

Nonideal Switch



MOS TRANSISTOR AS A SWITCH

Symbol



On Characteristics of A MOS Switch

Assume operation in non-saturation region ($v_{DS} < v_{GS} - V_T$).

$$i_D = \frac{K'W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right]v_{DS}$$

$$\frac{\partial i_D}{\partial v_{DS}} = \frac{K'W}{L}\left[v_{GS} - V_T - v_{DS}\right]$$

Thus,

$$\boxed{R_{ON} = \frac{\partial v_{DS}}{\partial i_D} = \frac{1}{\frac{K'W}{L}(v_{GS} - V_T - v_{DS})}}$$

OFF Characteristics of A MOS Switch

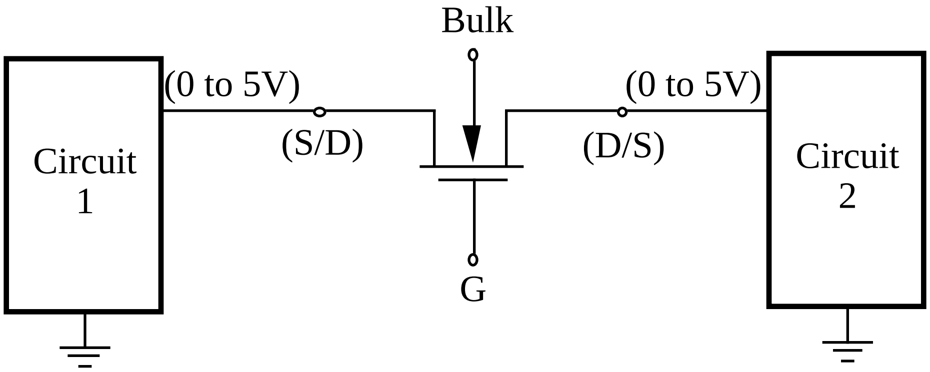
If $v_{GS} < V_T$, then $i_D = I_{OFF} = 0$ when $v_{DS} \approx 0V$.

If $v_{DS} > 0$, then

$$\boxed{R_{OFF} \approx \frac{1}{i_{DS}\lambda} = \frac{1}{I_{OFF}\lambda} \approx \infty}$$

MOS SWITCH VOLTAGE RANGES

Assume the MOS switch connects to circuits and the analog signal can vary from 0 to 5V. What are the voltages required at the terminals of the MOS switch to make it work properly?



- The bulk voltage must be less than or equal to zero to insure that the bulk-source and bulk-drain are reverse biased.
- The gate voltage must be greater than $5 + V_T$ in order to turn the switch on.

Therefore,

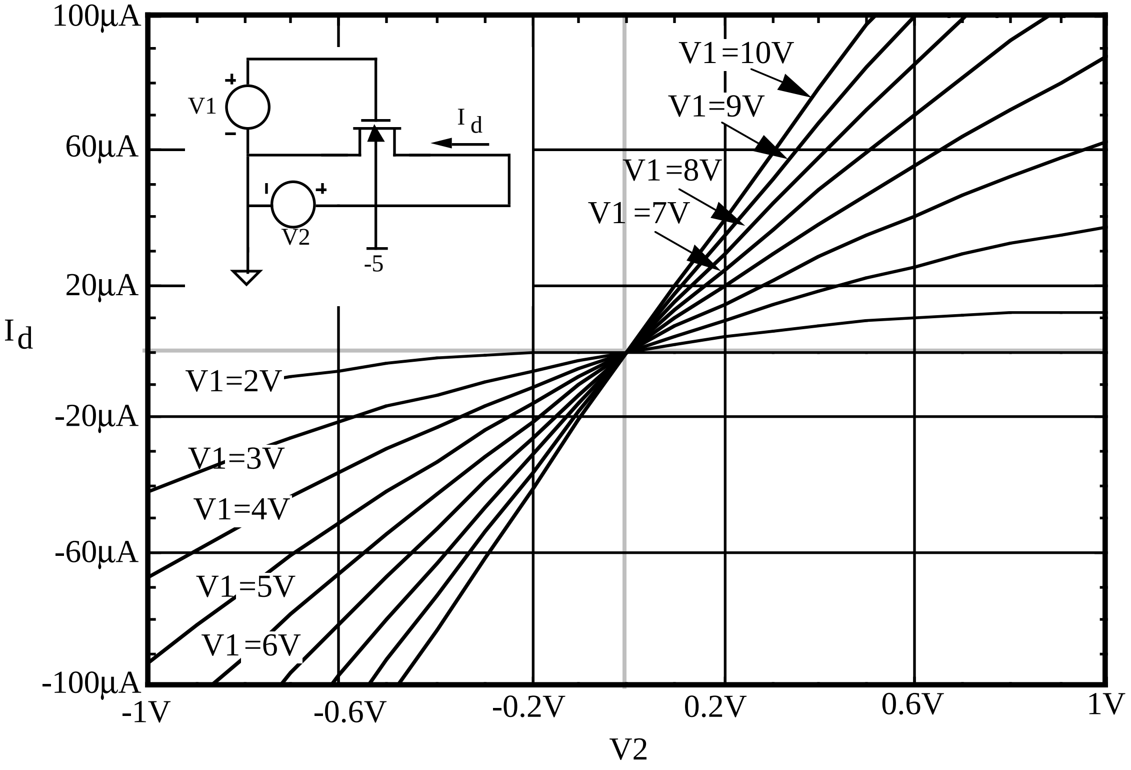
$$V_{Bulk} \leq 0V$$

$$V_G \geq 5 + V_T$$

(Remember that the larger the value of V_{SB}, the larger V_T)

I-V CHARACTERISTICS OF THE MOS SWITCH

SPICE ON Characteristics of the MOS Switch

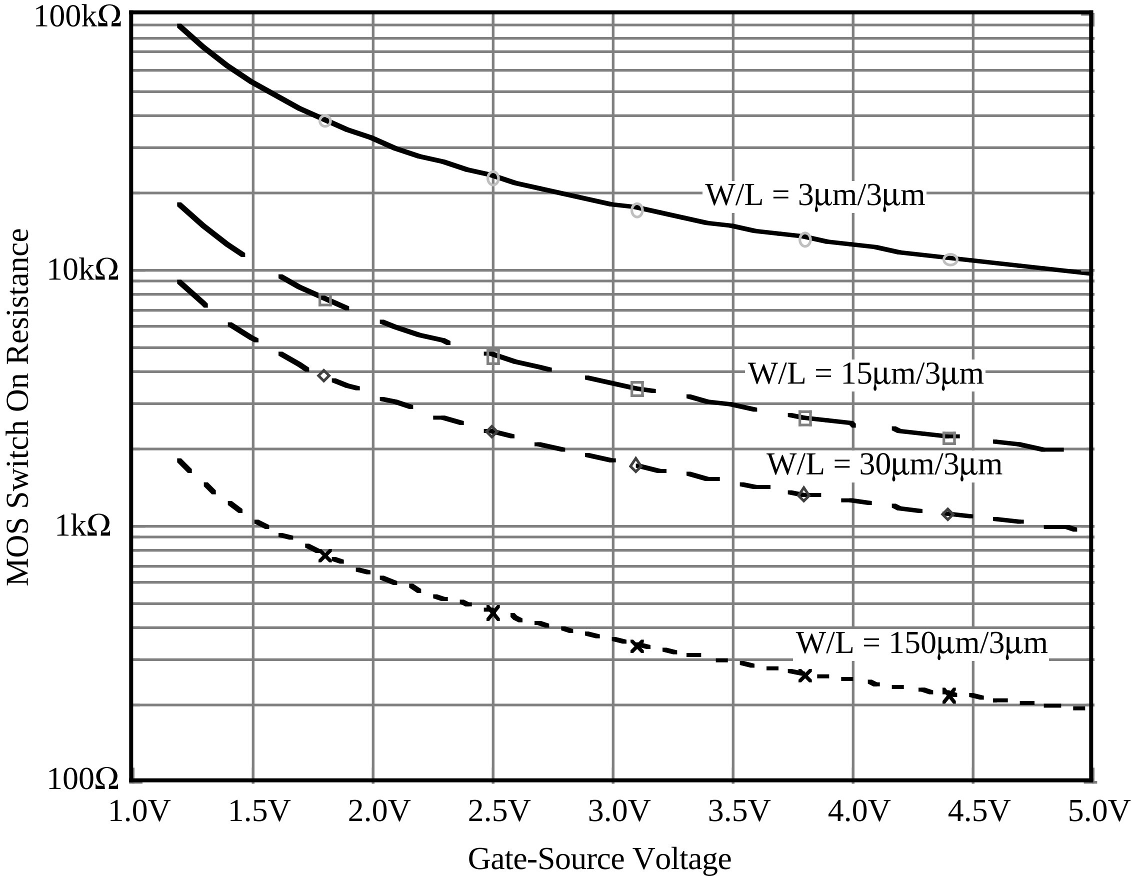


SPICE Input File:

```
MOS Switch On Characteristics
M1 1 2 0 3 MNMOS W=3U L=3U
.MODEL MNMOS NMOS VTO=0.75, KP=25U,
+LAMBDA=0.01, GAMMA=0.8 PHI=0.6
V2 1 0 DC 0.0
V1 2 0 DC 0.0
V3 3 0 DC -5.0
.DC V2 -1 1 0.1 V1 2 10 1
.PRINT DC ID(M1)
.PROBE
.END
```

MOS SWITCH ON RESISTANCE AS A FUNCTION OF V_{GS}

SPICE ON Resistance of the MOS Switch



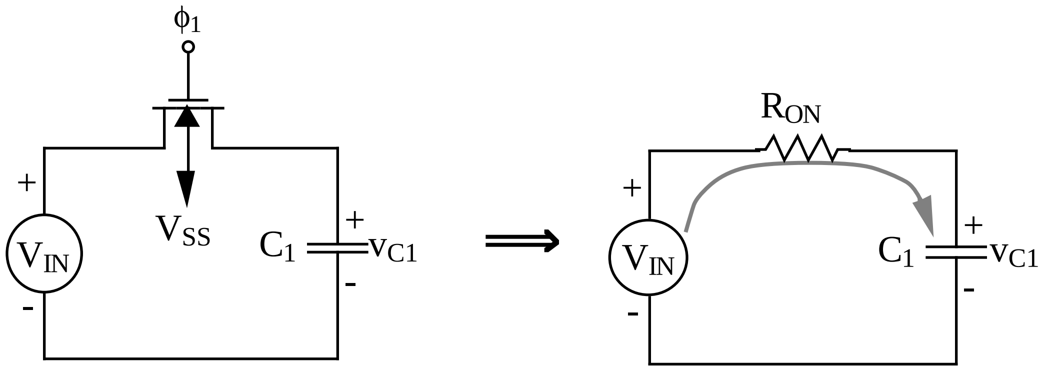
SPICE Input File:

```
MOS Switch On Resistance as a f(W/L)
M1 1 2 0 0 MNMOS W=3U L=3U
M2 1 2 0 0 MNMOS W=15U L=3U
M3 1 2 0 0 MNMOS W=30U L=3U
M4 1 2 0 0 MNMOS W=150U L=3U
.MODEL MNMOS NMOS VTO=0.75, KP=25U, LAMBDA=0.01, GAMMA=0.8
PHI=0.6
VDS 1 0 DC 0.001V
VGS 2 0 DC 0.0
.DC VGS 1 5 0.1
.PRINT DC ID(M1) ID(M2) ID(M3) ID(M4)
.PROBE
.END
```

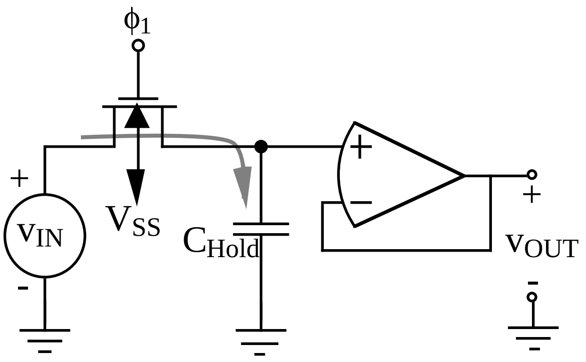
INFLUENCE OF SWITCH IMPERFECTIONS ON PERFORMANCE

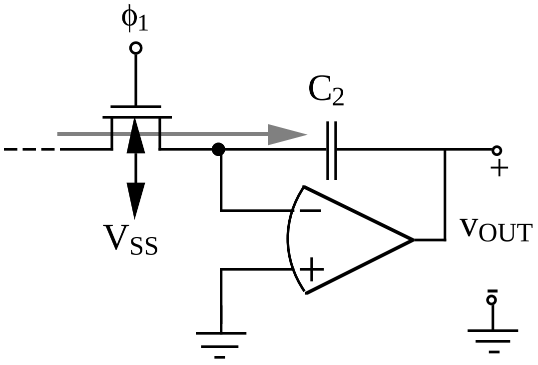
Finite ON Resistance

Non-zero charging and discharging rate.



Finite OFF Current





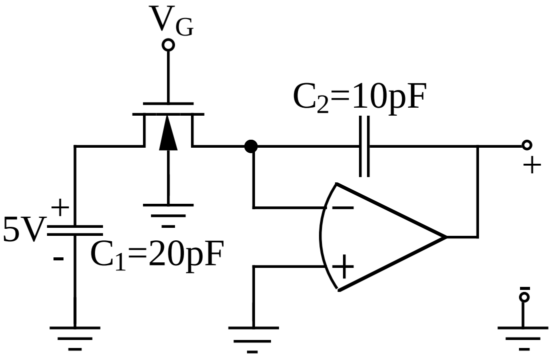
EXAMPLES

1. What is the on resistance of an enhancement MOS switch if $V_S = 0V$, $V_G = 10V$, $W/L = 1$, $V_{TO} = 1V$, and $K' = 25\mu A/V^2$?

   Assume that $v_{DS} \approx 0V$. Therefore,

   $$R_{ON} \approx \frac{v_{DS}}{i_D} = \frac{L/W}{K'(V_G-V_S-V_T)}$$

   $$R_{ON} = \frac{10^6}{25(10-1)} = 4444\Omega$$



2. If V_G=10V at t=0, what is the W/L value necessary to discharge C_1 to with 5% of its intial charge at t=0.1μS? Assume $K'=25\mu A/V^2$ and V_{TO} = 1V.

   $$v(t) = 5\exp(-t/RC) \rightarrow \exp\left(\frac{10^{-7}}{RC}\right) = 20 \rightarrow RC = \frac{10^{-7}}{\ln(20)}$$

   $$\text{Therefore, } R = \frac{10}{6} \times 10^3\Omega$$

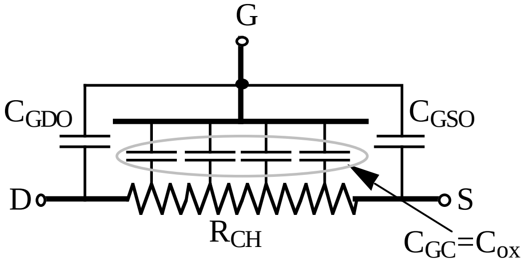
Thus, $$\frac{10\text{x}10^3}{6} = \frac{L/W}{K'(V_G-V_S-V_T)} = \frac{L/W}{(2.5\text{x}10^{-5})(9)}$$

Gives $\frac{W}{L} = 2.67$

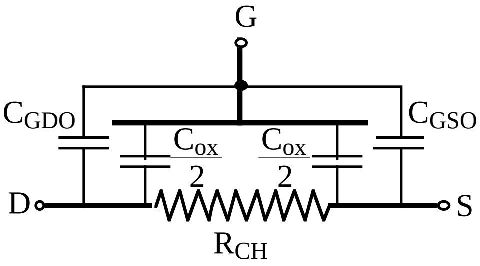
INFLUENCE OF PARASITIC CAPACITANCES

MOSFET Model for Charge Feedthrough Analysis

Distributed Model



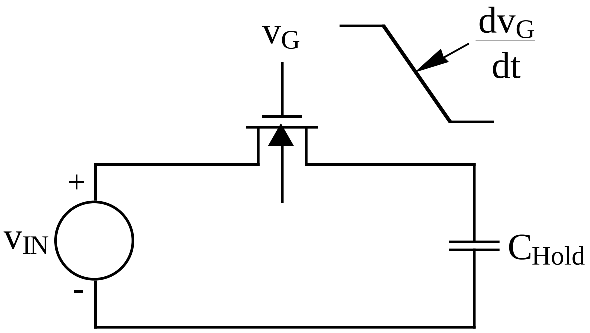
Simplified Distributed Model



C_{GSO} = Voltage independent (1st-order), gate-source, overlap cap.
C_{GDO} = Voltage independent (1st order), drain-source overlap cap.
C_{GC} = Gate-to-channel capacitance (C_{ox})
R_{CH} = Distributed drain-to-source channel resistance

Charge Injection Sensitivity to Gate Signal Rate

Model:



Case 1 - Slow Fall Time:

- Gate is inverted as v_G goes negative .
- Channel time constant small enough so that the charge on C_{Hold} is absorbed by v_{IN}.
- When gate voltage reaches $v_{IN}+V_T$, the device turns off and feedthru occurs via the overlap capacitance.

Case 2 - Fast Fall Time:

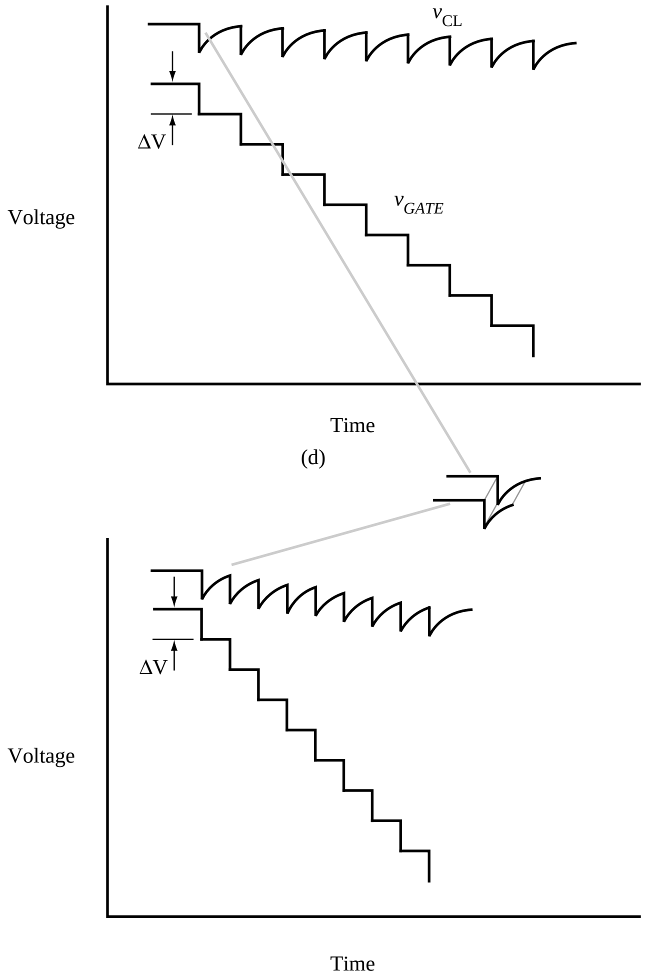
- Gate is inverted as v_G goes negative.
- Fall rate is faster than the channel time constant so that feedthru occurs via the channel capacitance onto C_{Hold} which is not absorbed by v_{IN}.
- Feedthru continues when v_G reaches $v_{IN}+V_T$.
- Total feedthru consists of that due to both the channel capacitance and the overlap capacitances.

Other Considerations:

- Source resistance effects the amount of charge shared between the drain and the source.
- The maximum gate voltage before negative transition effects the amount of charge injected.

Intuition about Fast and Slow Regimes

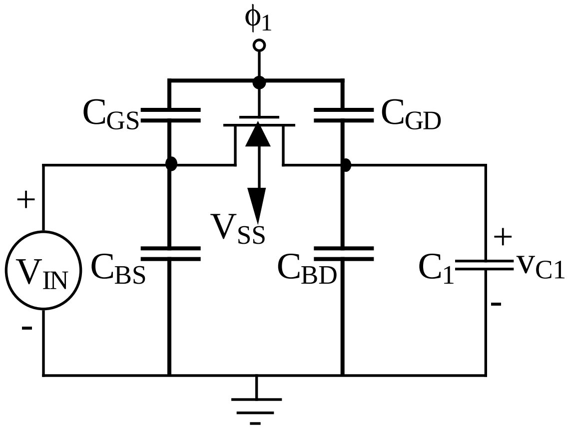
To develop some intuition about the fast and slow cases, it is useful to model the gave voltage as a piecewise constant waveform (a quantized waveform) and consider the charge flow at each transition as illustrated below. In this figure, the range of voltage at C_L illustrated represent the period while the transistor is on. In both cases, the quantized voltage step is the same, but the time between steps is different. The voltage accross C_L is observed to be an exponential whose time constant is due to the channel resistance and channel capacitance and does not change from fast case to slow case.



(d)

(e)

Illustration of Parasitic Capacitances

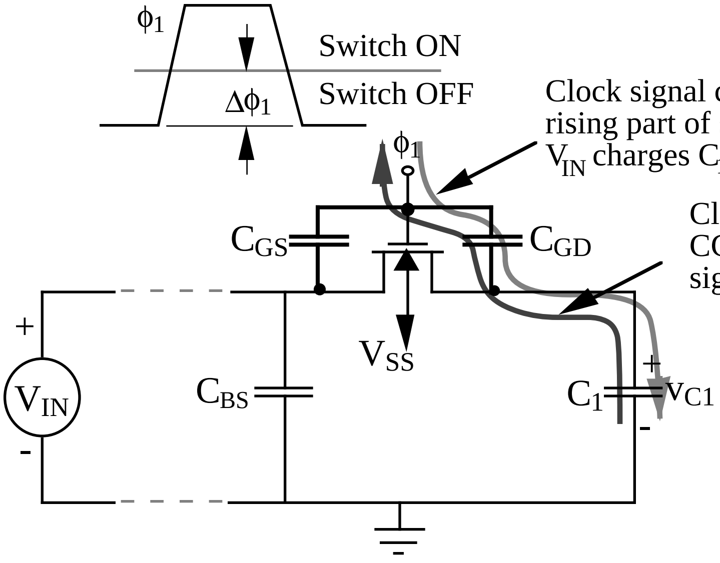


C_{GS} and C_{GD} result in clock feedthrough

C_{BS} and C_{BD} cause loading on the desired capacitances

Clock Feedthrough

Assume slow fall and rise times

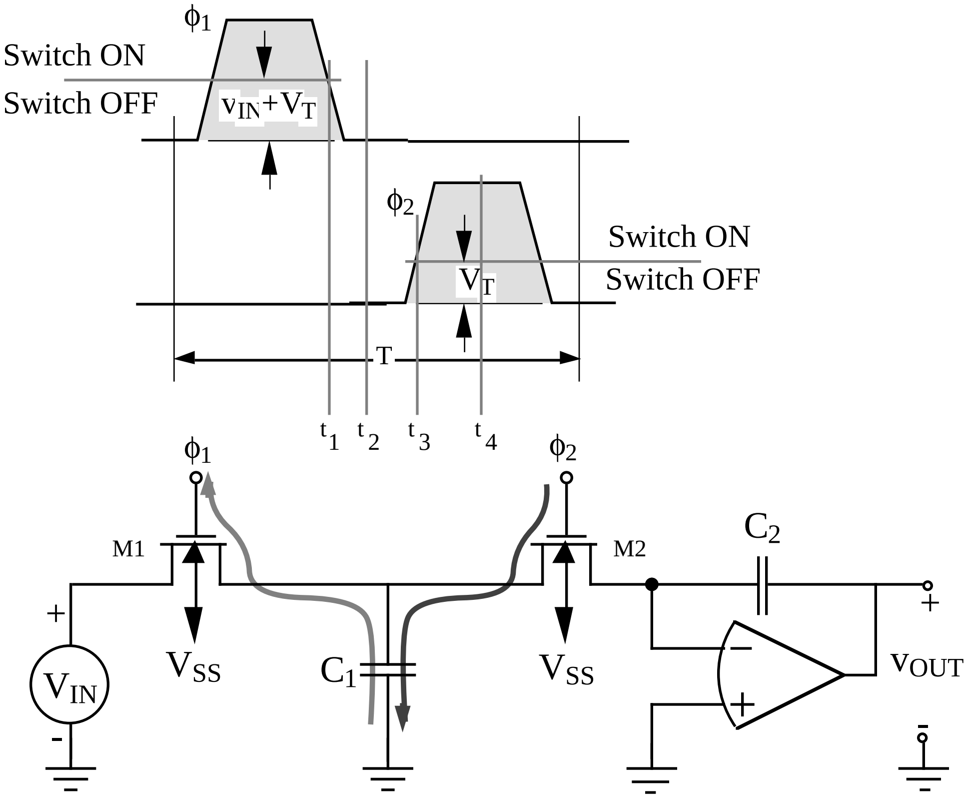


Clock signal couples through CGD on the rising part of signal when switch is off, but V_{IN} charges C_1 to the right value regardless.

Clock signal couples through CGD on the falling part of the signal when the switch is off.

$$\Delta v_{C1} = -\left(\frac{C_{GD}}{C_1+C_{GD}}\right)\Delta\phi_1 \approx -\left(\frac{C_{GD}}{C_1}\right)\Delta\phi_1 = -\left(\frac{C_{GD}}{C_1}\right)(v_{in} + V_T)$$

EXAMPLE - Switched Capacitor Integrator (slow clock edge regime)



assuming: $C_{GS1}=C_{GS2}=C_{GD1}=C_{GD2} = C_G$

Net feedthrough on C_1 at t_2:

$$\Delta V_{C1} = -\left(\frac{C_G}{C_G+C_1}\right)(V_{IN} + V_T)$$

$$V_{C1} = V_{IN}\left(1- \frac{C_G}{C_1+C_G}\right) - V_T\left(\frac{C_G}{C_G+C_1}\right)$$

At t_3, additional charge has been added due to C_{GS} overlap of M2 as ϕ_2 goes positive. Note that M2 has not turned on yet.

$$\Delta V_{C1\ (t2\text{-}t3)} = \left(\frac{C_G}{C_G+C_1}\right) V_T$$

Giving at the end of t_3 (before M2 turns on):

$$V_{C1} = V_{IN}\left(1 - \frac{C_G}{C_1 + C_G}\right)$$

Once M2 turns on (at t_3^+), all of the charge on C_1 is transferred to C_2.

$$\Delta V_O = -V_{C1}\left(\frac{C_1}{C_2}\right) = -V_{IN}\left(\frac{C_1}{C_2}\right)\left(1 - \frac{C_G}{C_1 + C_G}\right)$$

Between times at t_3^+ and t_4 additional charge is transferred to C1 from the channel capacitance of M2.

$$\Delta V_{O\ (t3-t4)} = -\left(\frac{C_{ch}}{C_2}\right)(V_{clk} - V_T)$$

The final change in Vout is:

$$\Delta V_O = -V_{IN}\left(\frac{C_1}{C_2}\right)\left(1 - \frac{C_G}{C_1 + C_G}\right) - \left(\frac{C_{ch}}{C_2}\right)(V_{clk} - V_T)$$

Ideally the output voltage change is $-V_{IN}\left(\frac{C_1}{C_2}\right)$ so the error due to charge feedthrough is:

$$\Delta V_O\ (\text{error}) = V_{IN}\left(\frac{C_1}{C_2}\right)\left(\frac{C_G}{C_1 + C_G}\right) - \left(\frac{C_{ch}}{C_2}\right)(V_{clk} - V_T)$$

Rigorous Quantitative Analysis of Fast and Slow Regimes

Consider the gate voltage traversing from V_H to V_L (e.g., 5.0 volts to 0.0 volts, respectively) described in the time domain as

$$v_G = V_H - Ut \tag{3}$$

When operating in the slow regime defined by the relationship

$$\frac{\beta V_{HT}^{2}}{2C_L} >> U \tag{4}$$

where V_{HT} is defined as

$$V_{HT} = V_H - V_S - V_T \tag{5}$$

the error (the difference between the desired voltage V_S and the actual voltage, V_{C_L}) due to charge injection can be described as

$$V_{error} = \left(\frac{W \cdot \mathrm{CGD0} + \frac{C_{ch}}{2}}{C_L}\right)\sqrt{\frac{\pi\, U\, C_L}{2\beta}} + \frac{W \cdot \mathrm{CGD0}}{C_L}(V_S + V_T - V_L) \quad (6)$$

In the fast swithing regime defined by the relationship

$$\frac{\beta\, V_{HT}^2}{2C_L} << U \quad (7)$$

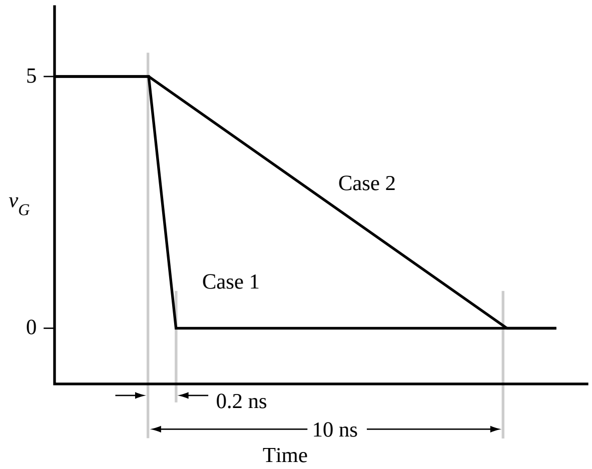
the error voltage is given in Eq. (8) below as

$$V_{error} = \left(\frac{W{\cdot}\mathrm{CGD0} + \frac{C_{ch}}{2}}{C_L}\right)\left(V_{HT} - \frac{\beta\, V_{HT}^3}{6U\, C_L}\right) + \frac{W{\cdot}\mathrm{CGD0}}{C_L}(V_S + V_T - V_L) \quad (8)$$

The following example illustrates the application of the charge-feedthrough model given by Eq's. (3) through (8).

Example 4.1-1 Calculation of charge feedthrough error

Calculate the effect of charge feedthrough on the circuit shown in Fig. 4.1-9 where V_S = 1.0 volts, C_L = 200 fF, W/L = 0.8µm/0.8µm, and V_G is given for two cases illustrated below. Use model parameters from Tables 3.1-2 and 3.2-1. Neglect ΔL and ΔW effects.



Case 1:
The first step is to determine the value of U in the expression

$$v_G = V_H - Ut$$

For a transition from 5 volts to 0 volts in 0.2 ns, $U = 25 \times 10^9$
In order to determine operating regime, the following relationship must be tested.

$$\frac{\beta V_{HT}^2}{2C_L} >> U \text{ for slow or } \frac{\beta V_{HT}^2}{2C_L} << U \text{ for fast}$$

Observin g that there is a backbias on the transistor switch effecting V_T, V_{HT} is

$$V_{HT} = V_H - V_S - V_T = 5 - 1 - 0.887 = 3.113$$

giving

$$\frac{\beta V_{HT}^2}{2C_L} = \frac{110\times10^{-6}\times 3.113^2}{2\times 200\text{f}} = 2.66\times 10^9 << 25\times 10^9 \quad \text{thus fast regime.}$$

Applying Eq. (8) for the fast regime yields

$$V_{error} = \left(\frac{176\times10^{-18} + \frac{1.58\times10^{-15}}{2}}{200\times10^{-15}}\right)\left(3.113 - \frac{3.32\times10^{-3}}{30\times10^{-3}}\right) + \frac{176\times10^{-18}}{200\times10^{-15}}(5 + 0.887 - 0)$$

$$V_{error} = 19.7 \text{ mV}$$

Case 2:

The first step is to determine the value of U in the expression

$$v_G = V_H - Ut$$

For a transition from 5 volts to 0 volts in 10 ns, $U = 5\times 10^8$ thus indicating the slow regime according to the following test

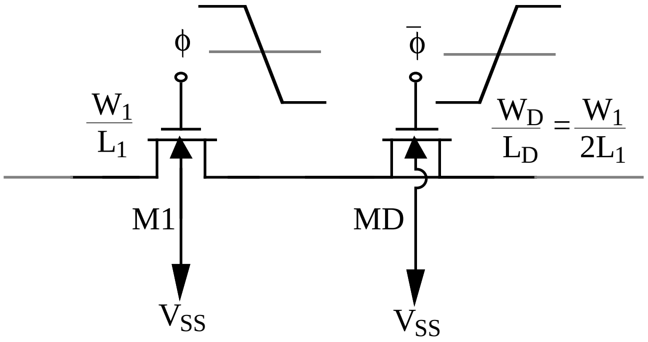
$$2.66\times 10^9 >> 5\times 10^8$$

$$V_{error} = \left(\frac{176\times10^{-18} + \frac{1.58\times10^{-15}}{2}}{200\times10^{-15}}\right)\sqrt{\frac{314\times10^{-6}}{220\times10^{-6}}} + \frac{176\times10^{-18}}{200\times10^{-15}}(5 + 0.887 - 0\,)$$

$$V_{error} = 10.95 \text{ mV}$$

POSSIBLE SOLUTIONS TO CLOCK FEEDTHROUGH

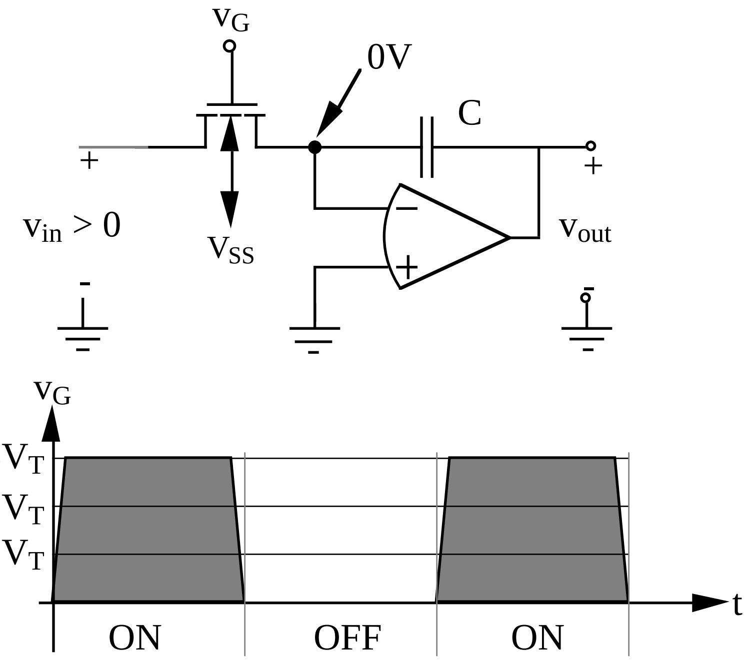
1.) Dummy transistor (MD) -



Complete cancellation is difficult.

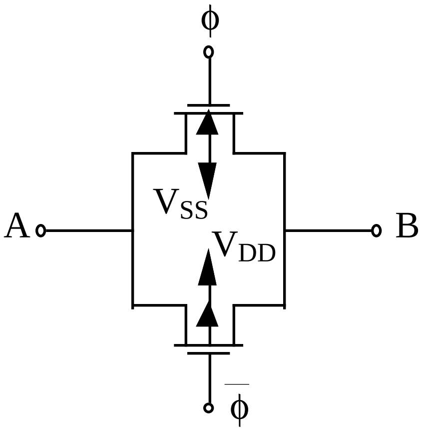
Requires a complementary clock.

2.) Limit the clock swing when one terminal of the switch is at a defined potential.



CMOS SWITCHES

"Transmission Gate"



Advantages -

1.) Larger dynamic range.

2.) Lower ON resistance.

Disadvantages -

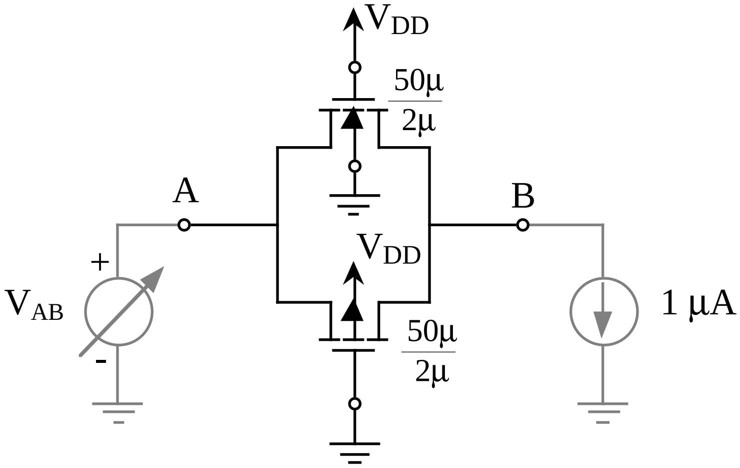
1.) Requires complementary clock.

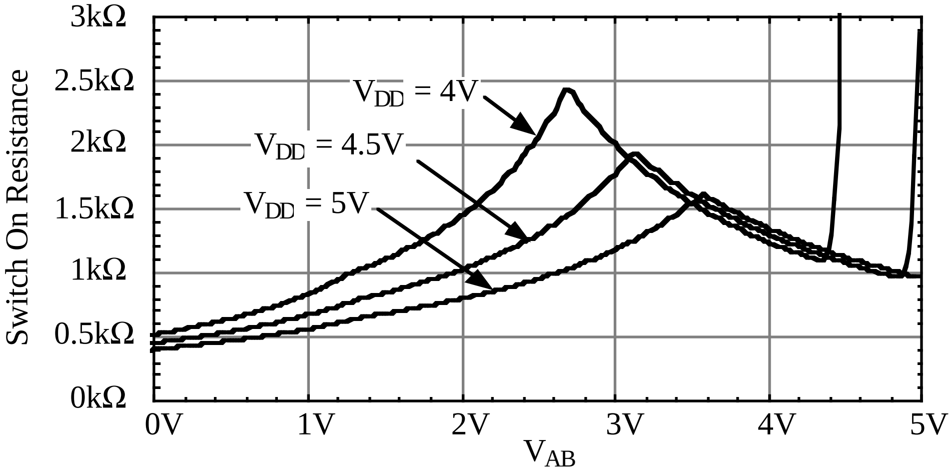
2.) Requires more area.

DYNAMIC RANGE LIMITATIONS OF SWITCHES

Must have sufficient v_{GS} to give a sufficiently low on resistance

Example:



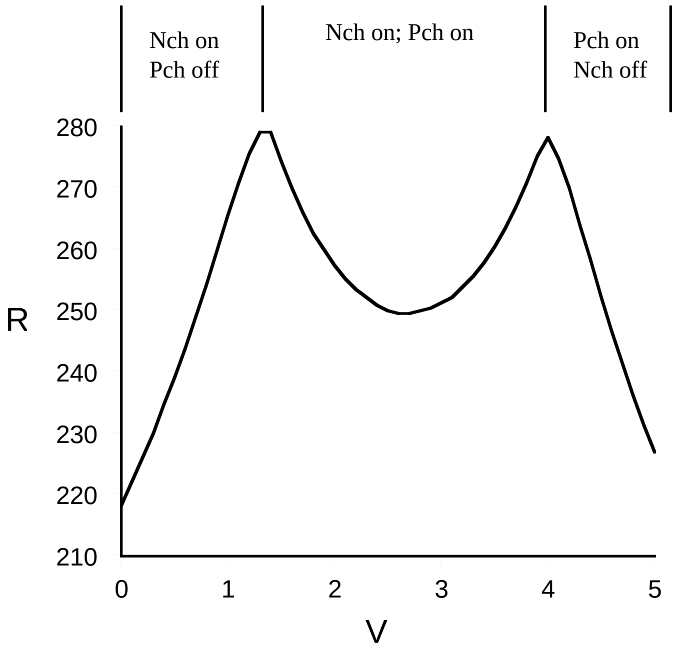


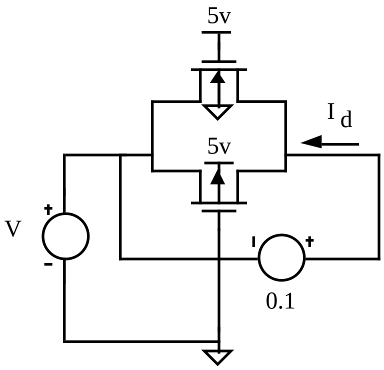
SPICE File:

```
Simulation of the resistance of a CMOS transmission switch
M1 1 3 2 0 MNMOS L=2U W=50U
M2 1 0 2 3 MPMOS L=2U W=50U
.MODEL MNMOS NMOS VTO=0.75, KP=25U,LAMBDA=0.01, GAMMA=0.5, PHI=0.5
.MODEL MPMOS PMOS VTO=-0.75, KP=10U,LAMBDA=0.01, GAMMA=0.5, PHI=0.5
VDD 3 0
VAB 1 0
IA 2 0 DC 1U
.DC VAB 0 5 0.02 VDD 4 5 0.5
.PRINT DC V(1,2)
.END
```

“Brooklyn Bridge” Effect

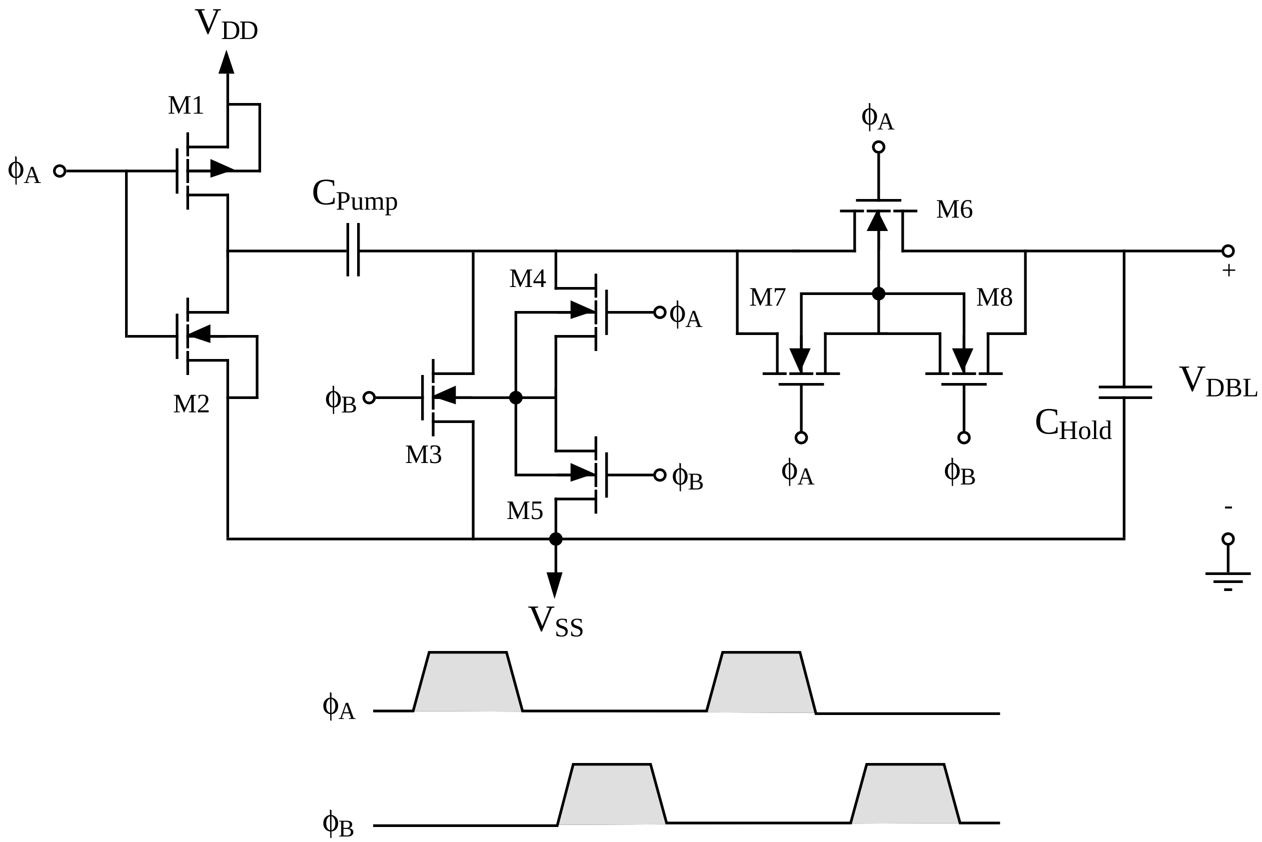
If N-channel and P-channel devices are “resistively” scaled (i.e., sized to have the same conductance at equivalent terminal conditions) the resistance versus voltage (common mode) will appear as shown below.





VOLTAGE DOUBLER USE TO PROVIDE GATE OVERDRIVE

Example



Operation:

1. ϕ_A low, ϕ_B high - C_{Pump} is charged to V_{DD}-V_{SS}.
2. ϕ_A high, ϕ_B low - C_{Pump} transfers negative charge to C_{Hold}

$$V_{DBL} \approx -0.5\left(V_{DD} - V_{SS}\right)$$

3. Eventually, V_{DBL} approaches the voltage of $-V_{DD} + V_{SS}$. If $V_{DD} = - V_{SS}$, then $V_{DBL} \approx - 2V_{DD}$.

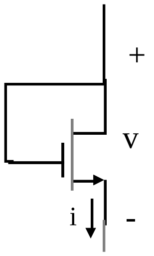
SUMMARY OF MOS SWITCHES

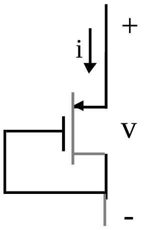
- Symmetrical switching characteristics
- High OFF resistance
- Moderate ON resistance (OK for most applications)
- Clock feedthrough is proportional to size of switch (W) and inversely proportional to switching capacitors.
- Complementary switches help increase dynamic range.
- As power supply reduces, switches become more difficult to fully turn on.
- Switches contribute a kT/C noise which folds back into the baseband.

V.2 - DIODES AND ACTIVE RESISTORS

MOS ACTIVE RESISTORS

Realizations





When the drain is connected to the gate, the transistor is always saturated.

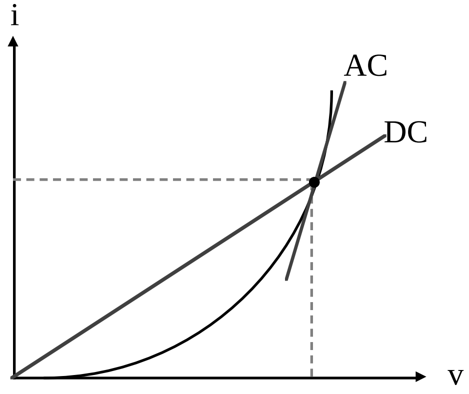
$$v_{DS} \geq v_{GS} - V_T$$

$$v_D - v_S \geq v_G - v_S - V_T$$

$$\therefore \quad v_{DG} \geq -V_T \text{ where } V_T > 0$$

Large Signal

I-V Characteristics -



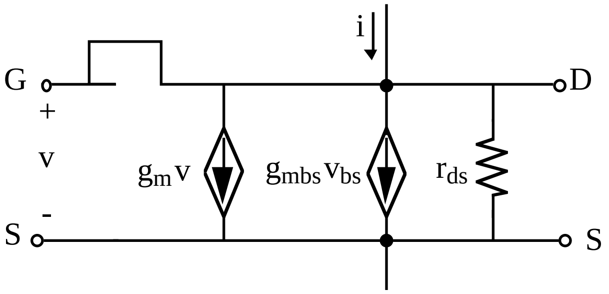
$$i = i_D = \left(\frac{K'W}{2L}\right) [\, v_{GS} - V_T \,]^2$$

$$= \frac{\beta}{2} (\, v_{GS} - V_T \,)^{2}, \quad \text{ignore } \lambda$$

or

$$v = v_{DS} = v_{GS} = V_T + \sqrt{\frac{2i_D}{\beta}}$$

Small signal



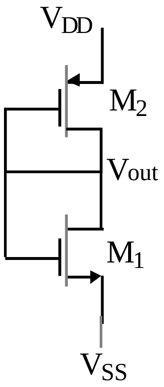
If $V_{BS} = 0$, then $R_{OUT} = \dfrac{v}{i} = \dfrac{1}{g_M + g_{DS}} \approx \dfrac{1}{g_M}$

If $V_{BS} \neq 0$?

Note: Generally, $g_m \approx 10\, g_{mbs} \approx 100\, g_{ds}$

VOLTAGE DIVISION USING ACTIVE RESISTORS

Objective : Derive a voltage Vout from V_{SS} and V_{DD}



Equating i_{D1} to i_{D2} results in :

$$v_{DS1} = \sqrt{\frac{\beta_2}{\beta_1}}\left|v_{DS2} - V_{T2}\right| + V_{T1}$$

where

$$v_{GS1} = v_{DS1} \quad \text{and} \quad v_{GS2} = v_{DS2}$$

Example :

If $V_{DD} = -V_{SS} = 5$ volts, $V_{out} = 1$ volt, and $I_{D1} = I_{D2} = 50$ µamps, then use the model parameters of Table 3.1-2 to find W/L ratios.

$$i_{D1} = \frac{\beta}{2}(v_{GS} - V_T)^2$$

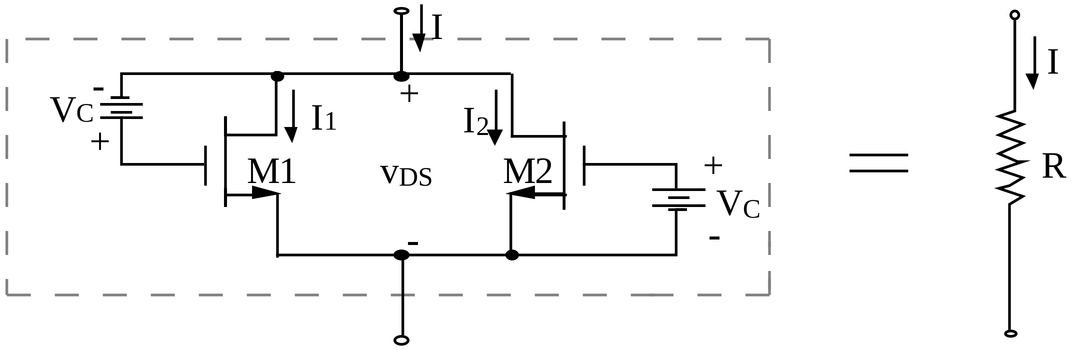
$\beta_1 = 4.0\ \mu A/V^2$ $\beta_2 = 11.1\ \mu A/V^2$

$K'_n = 17\ \mu A/V^2$ $K'_p = 8\ \mu A/V^2$

then $(W/L)_1 = \dfrac{1}{4.25}$ and $(W/L)_2 = 1.34$

EXTENDED DYNAMIC RANGE OF ACTIVE RESISTORS

Concept:



Consider :

Assume both devices are non-saturated

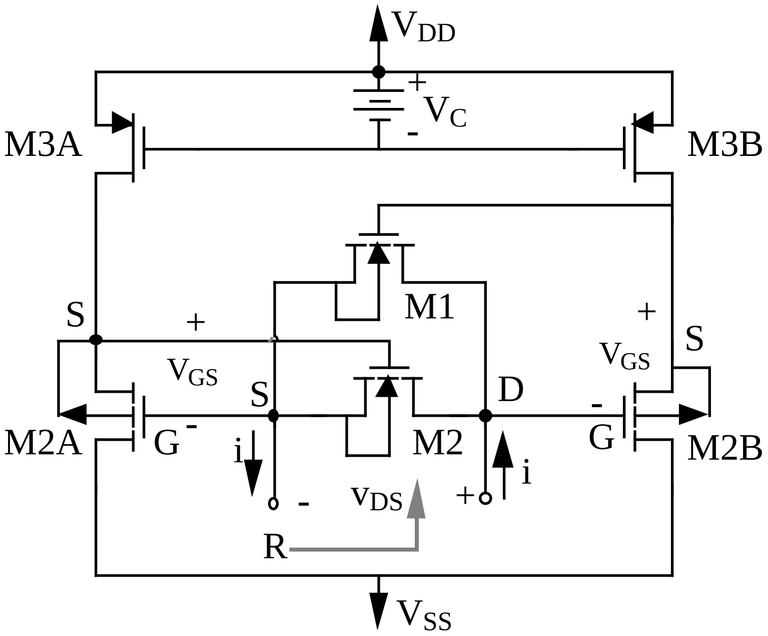
$$I_1 = \beta_1\left[(v_{DS} + V_C - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]$$

$$I_2 = \beta_2\left[(V_C - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]$$

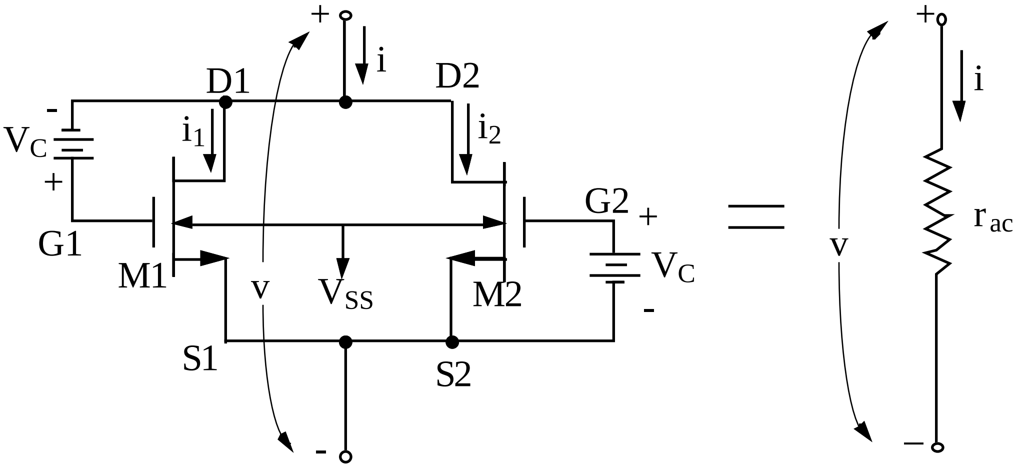
$$I = I_1 + I_2 = \beta\left[v_{DS}{}^2 + (V_C - V_T)v_{DS} - \frac{v_{DS}^2}{2} + (V_C - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]$$

$$I = 2\beta(V_C - V_T)v_{DS} \qquad \boxed{R = \frac{1}{2\beta(V_C - V_T)}}$$

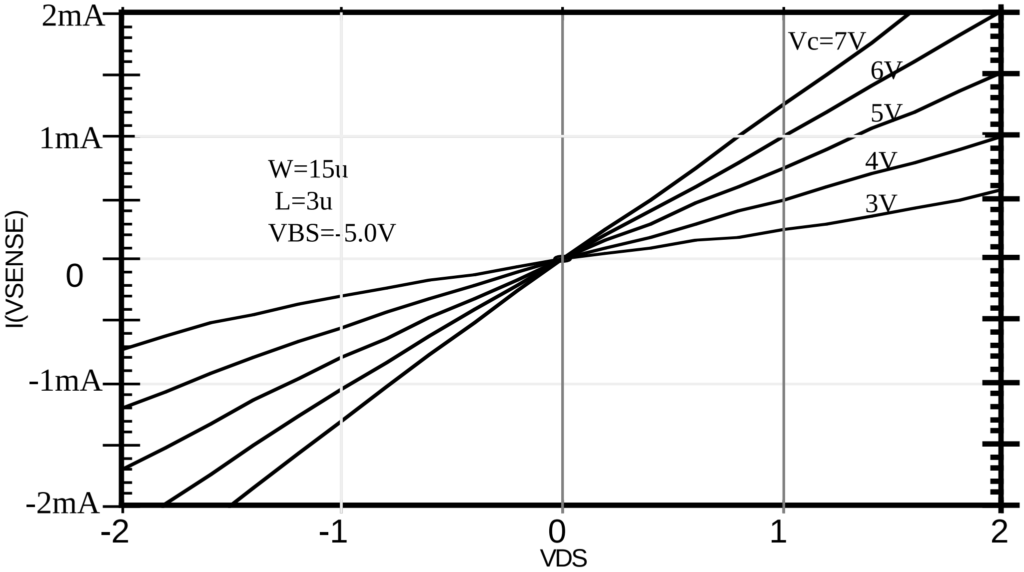
Implementation :



NMOS Parallel Transistor Realization :

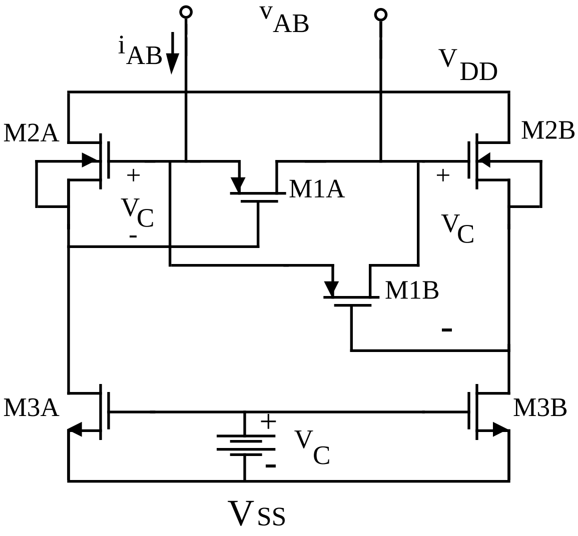


Voltage-Current Characteristic :

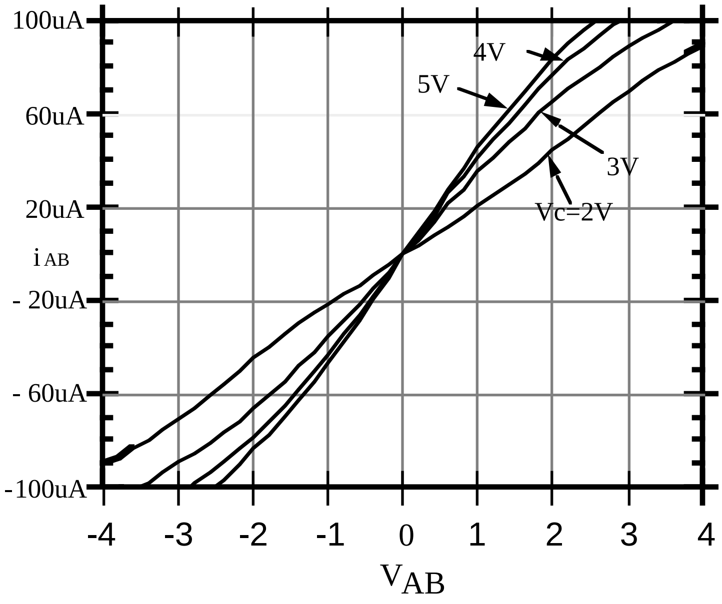


```
NMOS parallel transistor realization
M1 2 1 0 5 MNMOS W=15U L=3U
M2 2 4 0 5 MNMOS W=15U L=3U
.MODEL MNMOS NMOS VTO=0.75, KP=25U, LAMBDA=0.01, GAMMA=0.8
PHI=0.6
VC 1 2
E1 4 0 1 2 1.0
VSENSE 10 2 DC 0
VDS 10 0
VSS 5 0 DC -5
.DC VDS -2.0 2.0 .2 VC 3 7 1
.PRINT DC I(VSENSE)
.PROBE
.END
```

P-Channel Extended Range Active Resistor Circuit

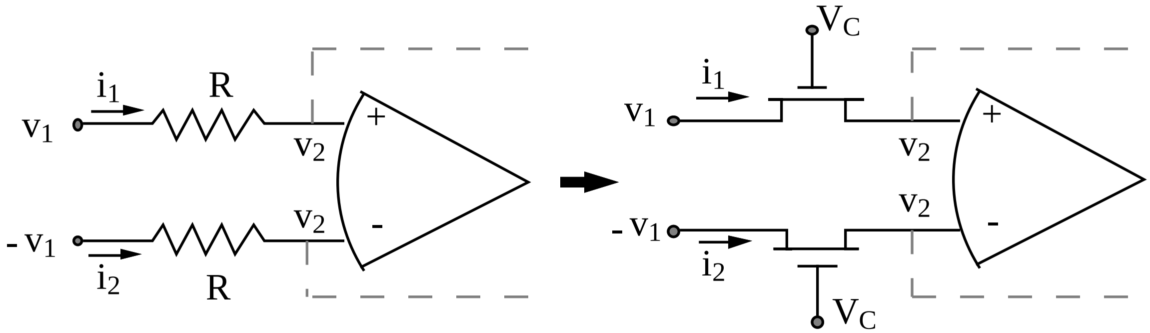


Voltage Current Characteristics



```
P-Channel Extended Range Active Resistor
M1A 3 4 5 10 MPMOS W=3U L=3U
M1B 3 6 5 10 MPMOS W=3U L=3U
M2A 10 3 4 4 MNMOS W=3U L=3U
M2B 10 5 6 6 MNMOS W=3U L=3U
M3A 4 7 0 0 MNMOS W=3U L=3U
M3B 6 7 0 0 MNMOS W=3U L=3U
VSENSE  1 3 DC 0V
VC 7 0
VAB 1 5
VDD 10 0 DC 5V
.MODEL MNMOS NMOS VTO=0.75, KP=25U
+ LAMBDA=0.01, GAMMA=0.8 PHI=0.6
.MODEL MPMOS PMOS VTO=-0.75 KP=8U
+LAMBDA=0.02 GAMMA=0.4 PHI=0.6
.DC VAB -4.0 4.0 0.2 VC 2 5 1
.PRINT DC I(VSENSE)
.PROBE
.END
```

THE SINGLE MOSFET DIFFERENTIAL RESISTOR



Assume the MOSFET's are in the non-saturation region

$$i_1 = \beta\left[(V_C - v_2 - V_T)(v_1 - v_2) - \frac{1}{2}(v_1 - v_2)^2\right]$$

$$i_2 = \beta\left[(V_C - v_2 - V_T)(-v_1 - v_2) - \frac{1}{2}(-v_1 - v_2)^2\right]$$

Rewrite as

$$i_1 = \beta\left[(V_C - v_2 - V_T)(v_1 - v_2) - \frac{1}{2}(v_1^2 - 2v_1v_2 + v_2^2)\right]$$

$$i_2 = \beta\left[(V_C - v_2 - V_T)(-v_1 - v_2) - \frac{1}{2}(v_1^2 + 2v_1v_2 + v_2^2)\right]$$

$$i_1 - i_2 = \beta\left[(V_C - v_2 - V_T)(2v_1) - \frac{1}{2}(v_1^2 - 2v_1v_2 + v_2^2 - v_1^2 - 2v_1v_2 - v_2^2)\right]$$

$$i_1 - i_2 = 2\beta\ [\ (V_C - V_T)v_1 - 2v_1v_2 + 2v_1v_2\ ]$$

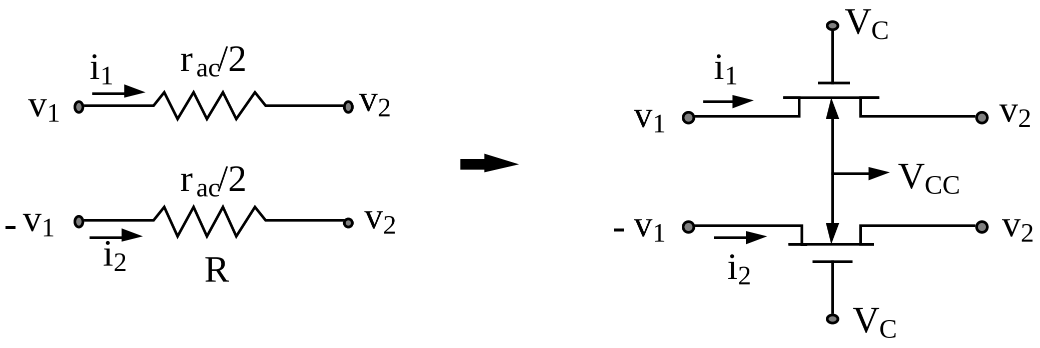
$$2R = \frac{v_1-(-v_1)}{i_1-i_2} = \frac{2v_1}{i_1-i_2} = \frac{2v_1}{2\beta(V_C-V_T)v_1} = \frac{1}{\beta(V_C-V_T)}$$

or

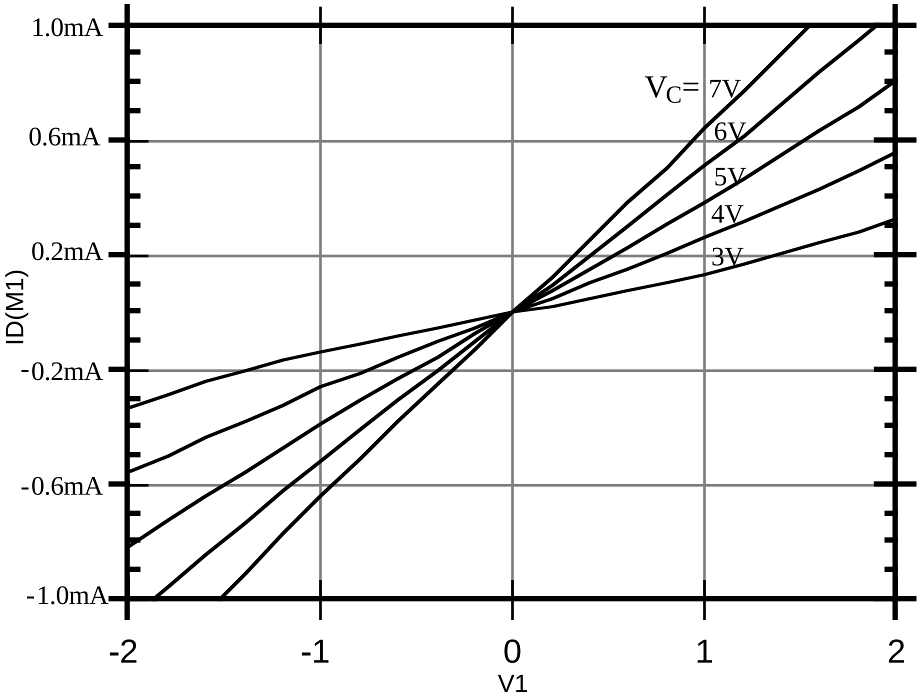
$$\boxed{R = \frac{1}{2K\frac{W}{L}(V_C-V_T)}}$$

$$v_1 \le V_C - V_T$$

Single-MOSFET, Differential Resistor Realization

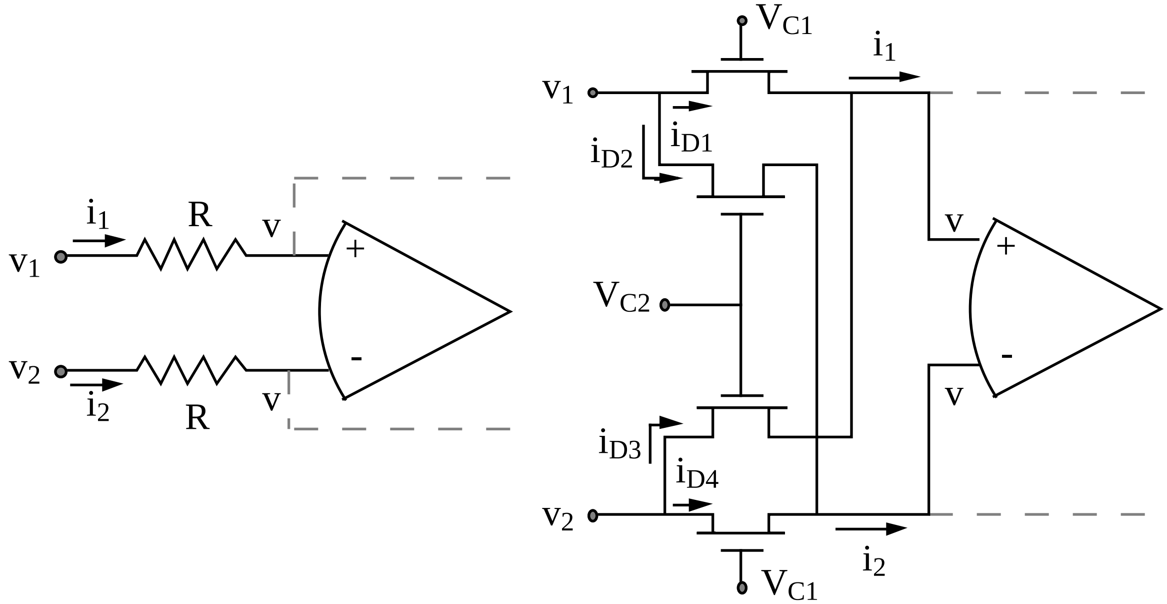


Voltage-Current Characteristics



```
Single MOSFET Differential Resistor Realization
M1 1 2 3 4 MNMOS1 W=15U L=3U
M2 5 2 3 4 MNMOS1 W=15U L=3U
VC 2 0
VCC 4 0 DC -5V
V1 1 0
E1 5 0 1 0 -1
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
.DC V1 -2.0 2.0 0.2 VC 3 7 1
.PRINT DC ID(M1)
.PROBE
.END
```

The Double MOSFET Differential Resistor



$$i_{D1} = \beta\left[(V_{C1}\text{-}v\text{-}V_T)(v_1\text{-}v) - \frac{1}{2}(v_1\text{-}v)^2\right]$$

$$i_{D2} = \beta\left[(V_{C2}\text{-}v\text{-}V_T)(v_1\text{-}v) - \frac{1}{2}(v_1\text{-}v)^2\right]$$

$$i_{D3} = \beta\left[(V_{C1}\text{-}v\text{-}V_T)(v_2\text{-}v) - \frac{1}{2}(v_2\text{-}v)^2\right]$$

$$i_{D4} = \beta\left[(V_{C2}\text{-}v\text{-}V_T)(v_2\text{-}v) - \frac{1}{2}(v_2\text{-}v)^2\right]$$

$$i_1 = i_{D1}+i_{D3} = \beta\left[(V_{C1}\text{-}v\text{-}V_T)(v_1\text{-}v)\text{-}\frac{1}{2}(v_1\text{-}v)^2 + (V_{C2}\text{-}v\text{-}V_T)(v_2\text{-}v)\text{-}\frac{1}{2}(v_2\text{-}v)^2\right]$$

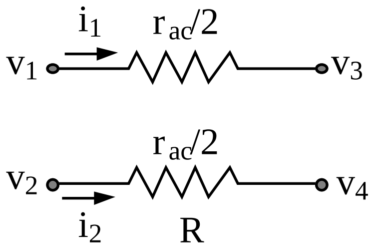
$$i_2 = i_{D2}+i_{D4} = \beta\left[(V_{C2}\text{-}v\text{-}V_T)(v_1\text{-}v)\text{-}\frac{1}{2}(v_1\text{-}v)^2 + (V_{C1}\text{-}v\text{-}V_T)(v_2\text{-}V)\text{-}\frac{1}{2}(v_2\text{-}v)^2\right]$$

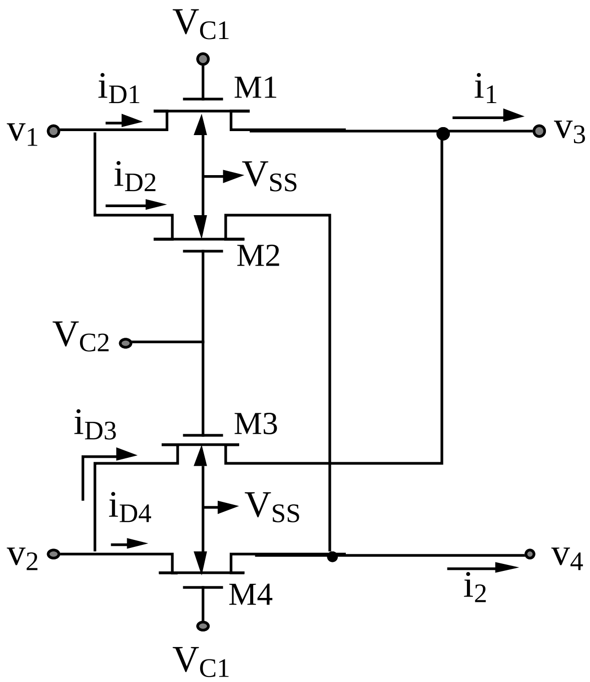
$$\begin{aligned} i_1 - i_2 = {} & \beta[(V_{C1}\text{-}v\text{-}V_T)(v_1\text{-}v) + (V_{C2}\text{-}v\text{-}V_T)(v_2\text{-}v) \\ & - (V_{C2}\text{-}v\text{-}V_T)(v_1\text{-} v) - (V_{C1}\text{-}v\text{-}V_T)(v_2\text{-}v)] \\ = {} & \beta[v_1(V_{C1}\text{-}V_{C2}) + v_2(V_{C2}\text{-}V_{C1})] = \beta(V_{C1}\text{-}V_{C2})(v_1\text{-}v_2) \end{aligned}$$

$$R_{in} = \frac{v_1\text{-}v_2}{i_1\text{-}i_2} = \frac{v_1\text{-}v_2}{\beta(V_{C1}\text{-}V_{C2})(v_1\text{-}v_2)} = \frac{1}{\frac{KW}{L}(V_{C1}\text{-}V_{C2})}$$

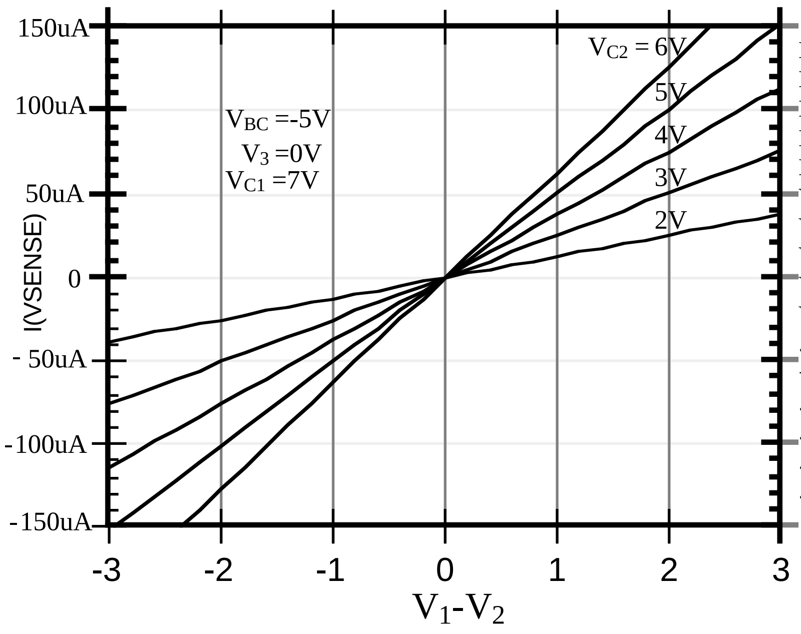
or $\boxed{R_{in} = \frac{1}{\frac{KW}{L}(V_{C1}\text{-}V_{C2})}}$ $v_1, v_2 \leq \min\,[(V_{C1}\text{-}V_T),(V_{C2}\text{-}V_T)]$

Double-MOSFET, Differential Resistor Realization





Voltage-Current Characteristics



```
Double MOSFET Differential Resistor Realization
M1 1 2 3 4 MNMOS1 W=3U L=3U
M2 1 5 8 4 MNMOS1 W=3U L=3U
M3 6 5 3 4 MNMOS1 W=3U L=3U
M4 6 2 8 4 MNMOS1 W=3U L=3U
VSENSE 3 8 DC 0
VC1 2 0 DC 7V
VC2 5 0
VSS 4 0 DC -5V
V12 1 6
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
.DC V12 -3 3 0.2 VC2 2 6 1
.PRINT DC I(VSENSE))
.PROBE
.END
```

SUMMARY OF ACTIVE RESISTOR REALIZATIONS

AC Resistance Realization	Linearity	How Controlled	Restrictions
Single MOSFET	Poor	V_{GS} or W/L	$v_{BULK} < \text{Min}\ (v_S, v_D)$
Parallel MOSFET	Good	V_C or W/L	$v \leq (V_C - V_T)$
Single-MOSFET, differential resistor	Good	V_C or W/L	$\|v_1\| < V_C - V_T$ $v_{BULK} < -v_1$ Differential around v_1
Double-MOSFET, differential resistor	Very Good	$V_{C1} - V_{C2}$ or W/L	$v_1, v_2 < \min(V_{C1}-V_T, V_{C2}-V_T)$ $v_{BULK} < \min(v_1,v_2)$ Transresistance only

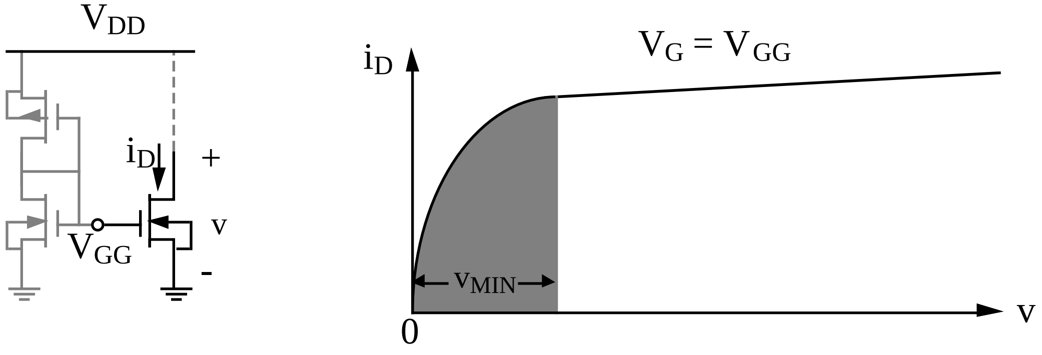
V.3 - CURRENT SINKS & SOURCES

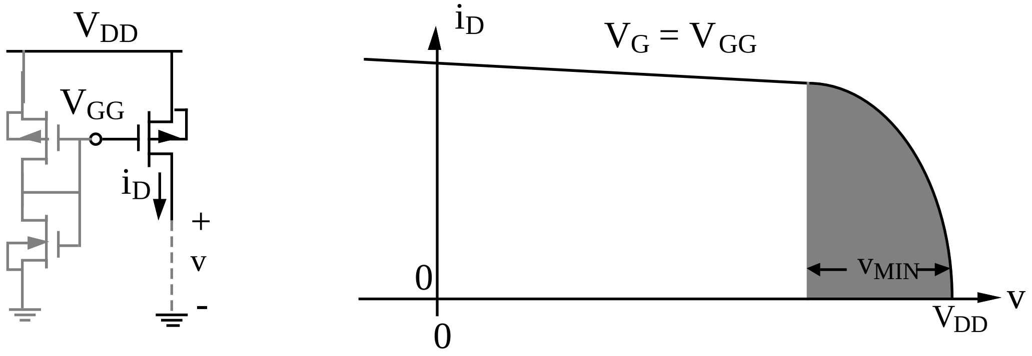
CHARACTERIZATION OF SOURCES & SINKS

1). Minimum voltage (v_{MIN}) across sink or source for which the current is no longer constant.

2). Output resistance which is a measure of the "flatness" of the current sink or source.

CMOS Current Sinks & Sources

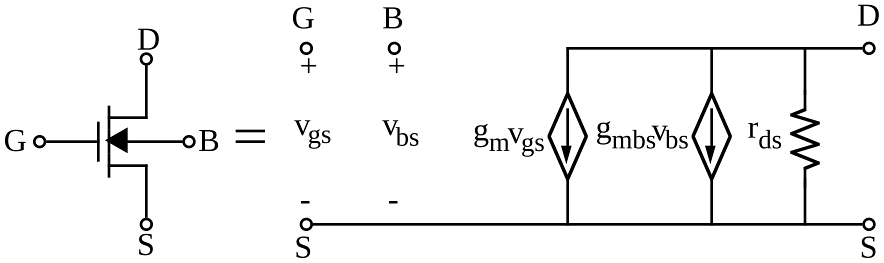




$$r_{OUT} = \frac{1}{\lambda I_D}$$

$v_{MIN} = v_{DS(SAT.)} = v_{ON}$ where $v_{ON} = v_{GS} - V_T$

SMALL SIGNAL MODEL FOR THE MOSFET



$$g_m = \sqrt{\frac{2K'WI_D}{L}}$$

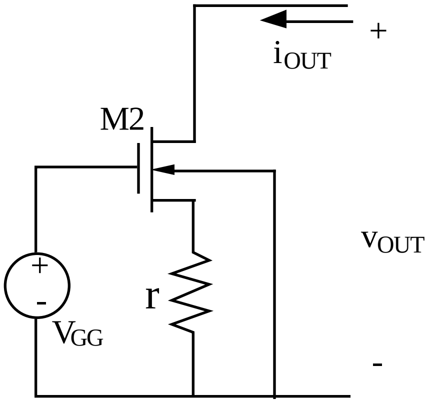
$$g_{mbs} = \frac{g_m \gamma}{2\sqrt{2\phi_F + |V_{BS}|}}$$

$$r_{ds} \approx \frac{1}{g_{ds}} = \frac{1}{\lambda I_D}$$

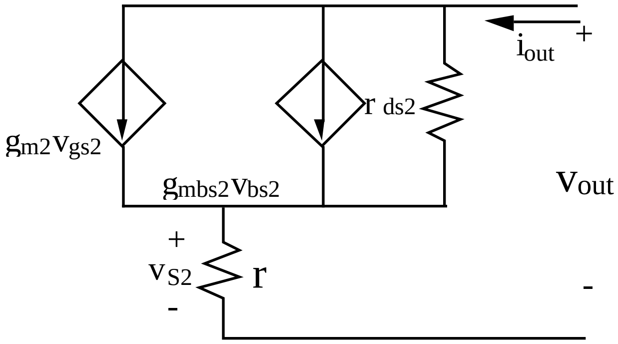
INCREASING THE R_{OUT} OF A CURRENT SOURCE

MOS

Circuit



Small-Signal Model



Loop equation:

$$v_{out} = [i_{out} - (g_{m2}v_{gs2} + g_{mbs2}v_{bs2})]r_{ds2} + i_{out}\,r$$

But, $v_{gs2} = -v_{s2}$ and $v_{bs2} = -\, v_{s2}$.

$$v_{out} = [i_{out} + g_{m2}v_{s2} + g_{mbs2}v_{s2}]r_{ds2} + i_{out}\,r$$

Replace v_{s2} by $i_{out}r$-

$$v_{out} = i_{out}\,[\, r_{ds2} + g_{m2}r_{ds2}r + g_{mbs2}r_{ds2}r + r\,]$$

Therefore,

$$r_{out} = r_{ds2} + r\,[1 + g_{m2}r_{ds2} + g_{mbs2}r_{ds2}]$$

MOS Small Signal Simplifications

Normally,

$$\boxed{g_m \approx 10g_{mbs} \approx 100g_{ds}}$$

Continuing

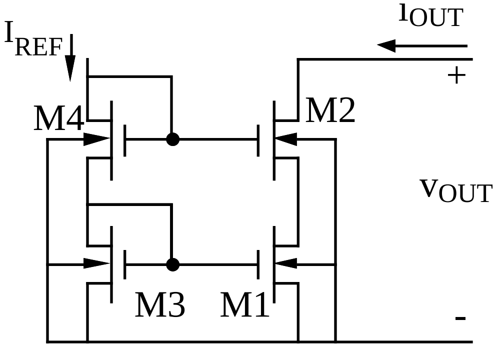
$$r_{out} \cong r g_{m2} r_{ds2}$$

$$\mathbf{r_{out} \approx r \ x \ (voltage\ gain\ of\ M2\ from\ source\ to\ drain)}$$

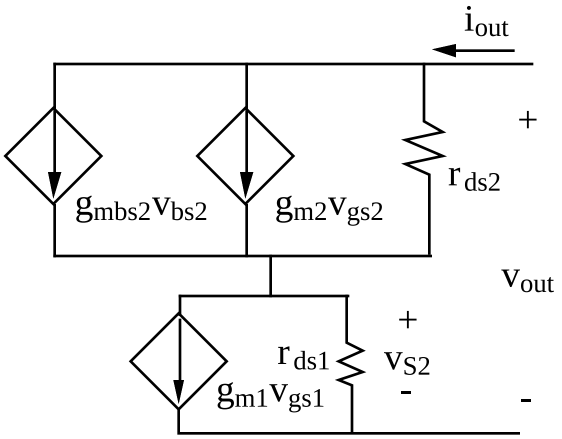
CASCODE CURRENT SINK

MOS

Circuit



Small-Signal Model



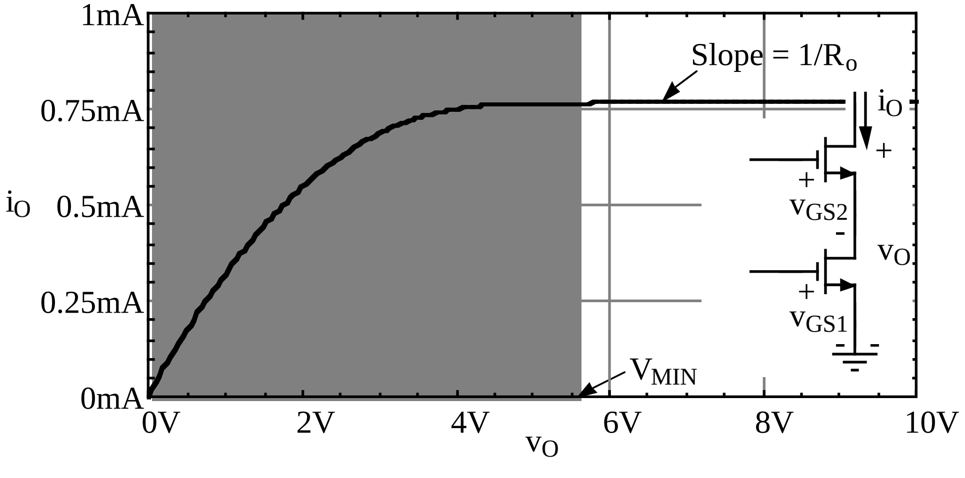
$$v_{out} = [i_{out} - (g_{m2}v_{gs2} + g_{mbs2}v_{bs2})]r_{ds2} + i_{out}r_{ds1}$$

$$v_{out} = i_{out}[r_{ds2} + g_{m2}r_{ds2}r(1 + \eta_2) + r_{ds1}]$$

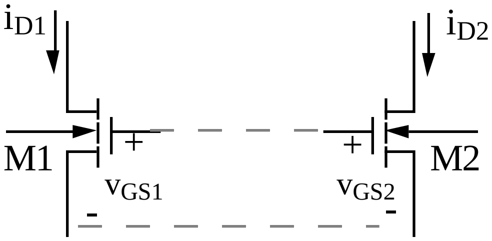
$$r_{out} = r_{ds2} + r[1 + g_{m2}r_{ds2}(1 + \eta_2)] \cong r_{ds1}g_{m2}r_{ds2}(1 + \eta_2)$$

Note : $v_{MIN} = V_T + 2V_{ON} \cong 0.75 + 1.5 = 2.25$ (assuming $V_{ON} \approx V_T$)

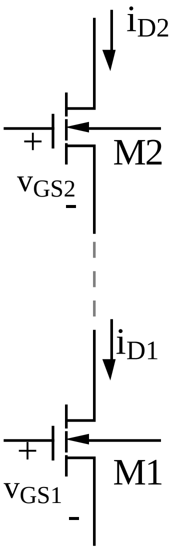
NMOS Cascode-



Gate-Source Matching Principle



$S = W/L$



Assume that M1 and M2 are matched but may not have the same W/L ratios.

1). If $v_{GS1} = v_{GS2}$, then $i_{D1} = (S_1/S_2)i_{D2}$
  a). v_{GS1} may be physically connected together , or
  b). v_{GS1} may be equal to v_{GS2} by some other means.

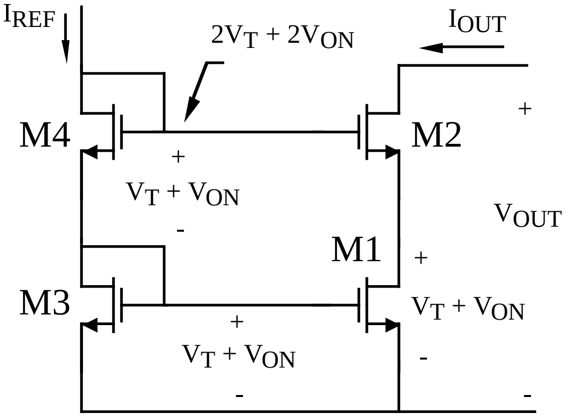
2). If $i_{D1} = i_{D2}$, then
  a). $v_{GS1} = V_T + \sqrt{S_2/S_1}(v_{GS2} - V_T)$, or
  b). If $S_1 = S_2$ and $V_{S1} \approx V_{S2}$ then
    $v_{GS1} = v_{GS2}$

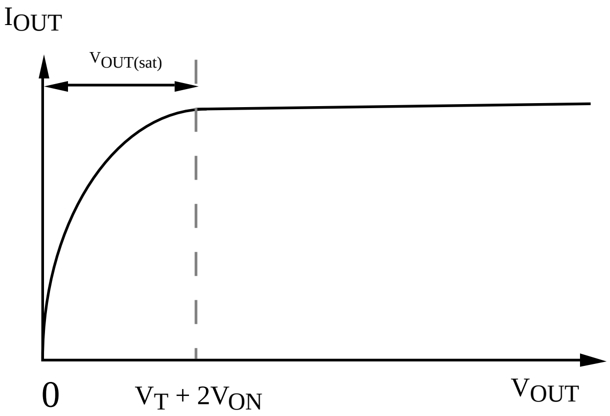
Strictly speaking, absolute matching requires that v_{DS} be equal for two matched devices.

Reduction of V_{MIN} or $V_{OUT}(sat)$

High-Swing Cascode

Method 1 for Reducing the Value of $v_{OUT}(sat)$

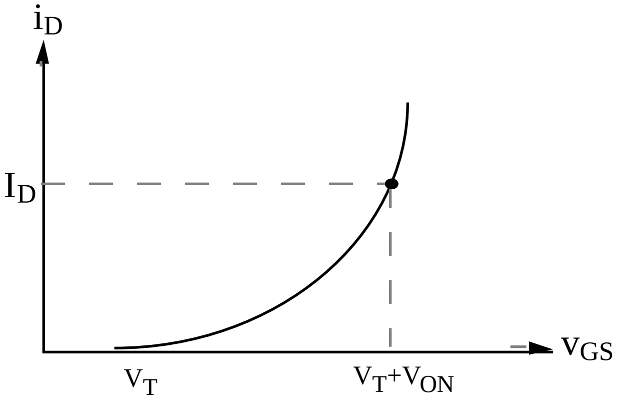




Standard Cascode Sink :

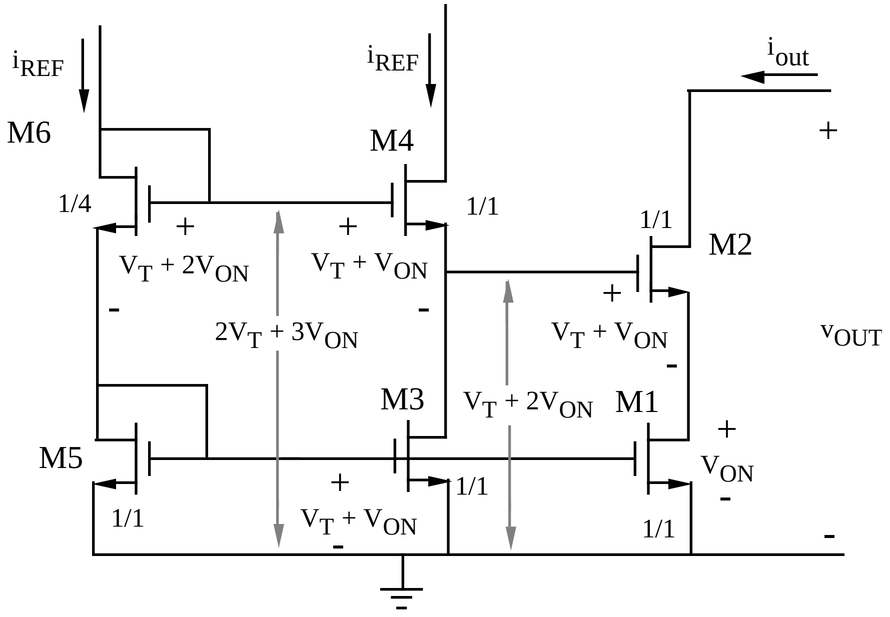
$$v_{GS} = V_{ON} + V_T = \begin{bmatrix} \text{Part of } v_{GS} \\ \text{to achieve} \\ \text{drain current} \end{bmatrix} + \begin{bmatrix} \text{Part of } v_{GS} \text{ to} \\ \text{enhance the channel} \end{bmatrix}$$

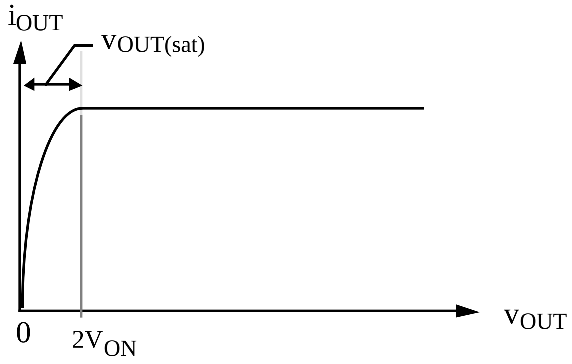
$$\therefore \; v_{DS(sat)} = v_{GS} - V_T = (V_{ON} + V_T) - V_T = V_{ON}$$

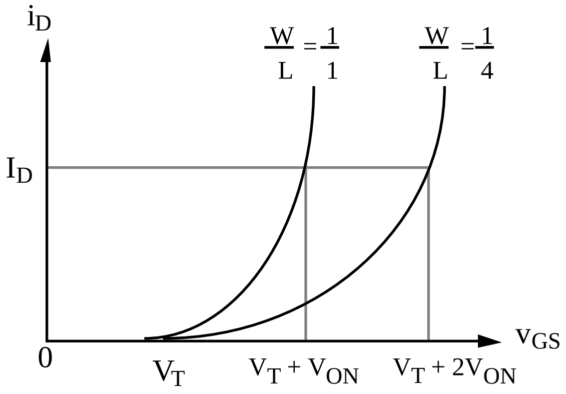


Above is based on the Gate-Source matching principle.

Circuit Which Reduces the Value of Vout(sat) of the Cascode Current Sink

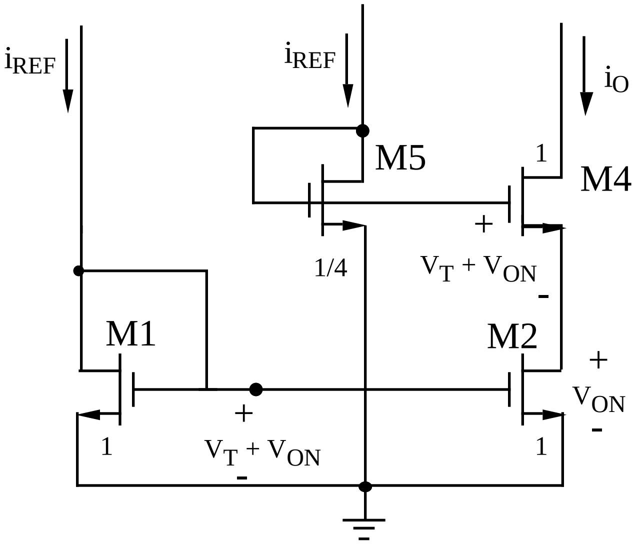






$$i_D = \frac{K'W}{2\,L}(v_{GS} - V_T)^2 = \frac{K'W}{2\,L}(V_{ON})^2$$

Method 2 for Reducing V_{MIN} for MOS Cascode Sink/Source



Assume $(W/L)_1 = (W/L)_2 = (W/L)_4 = 4(W/L)_5$ values are identical and ignore bulk effects.

Let $I_{REF} = I_O$

$$V_{GS1} = \sqrt{\frac{2I_{REF}}{K'\left(\frac{W_1}{L_1}\right)}} + V_T = V_{ON} + V_T$$

and

$$V_{GS5} = \sqrt{\frac{2I_{REF}}{K'\left(\frac{W_5}{L_5}\right)}} + V_T$$

Since $(W/L)_1 = 4(W/L)_5$

$$V_{GS5} = \sqrt{\frac{2I_{REF}}{K'\left(\frac{W_1}{4L_1}\right)}} + V_T = 2\left[\sqrt{\frac{2I_{REF}}{K'\left(\frac{W_1}{L_1}\right)}}\right] + V_T = 2\,V_{ON} + V_T$$

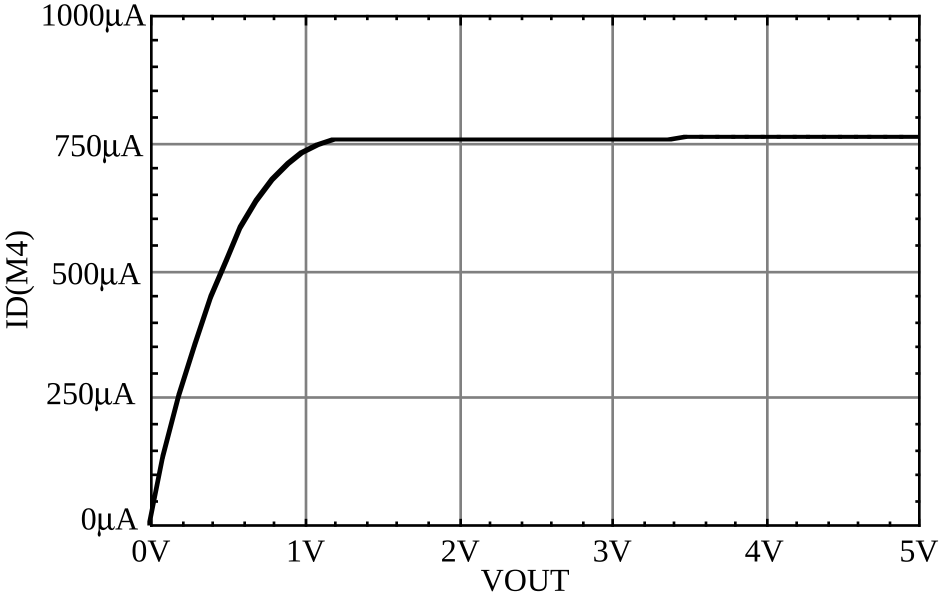
Since $V_{GS3} = V_{GS4} = V_{ON} + V_T$

$$V_{DS1} = V_{DS2} = V_{ON}$$

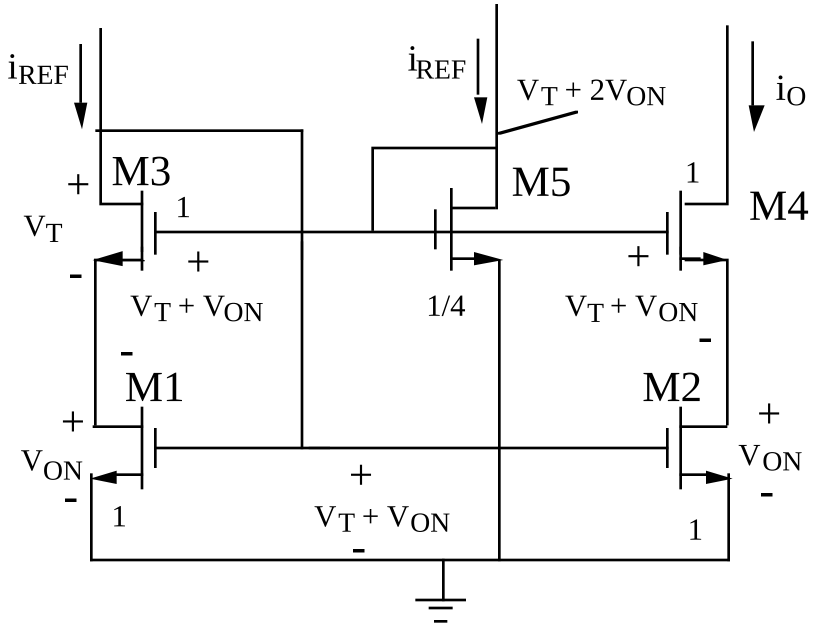
which gives a minimum output voltage while keeping all devices in saturation of

$$\boxed{v_{MIN} = 2\ V_{ON}}$$

Output Plot:



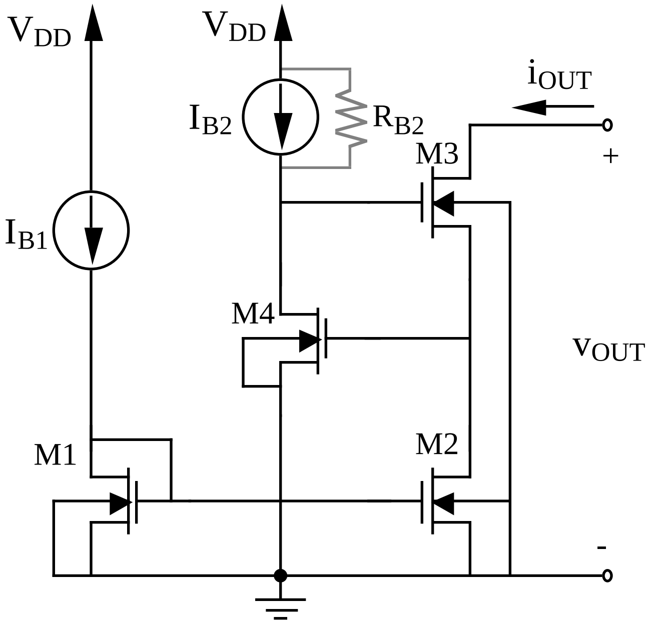
Matching Improved by Adding M3

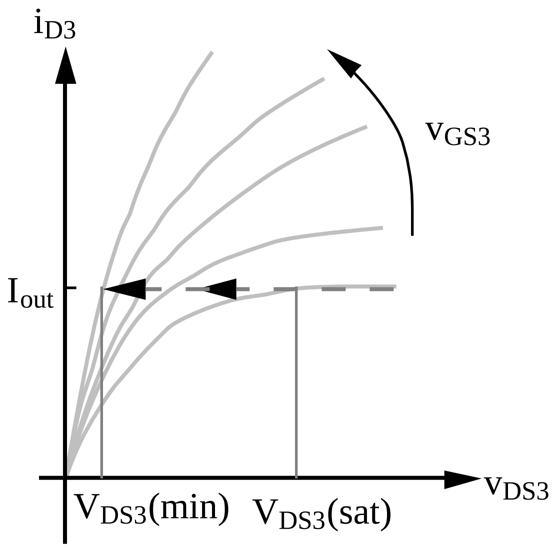


What is the purpose of M3?
The presence of M3 forces the $V_{DS1} = V_{DS2}$ which is necessary to guarantee that M1 and M2 act alike (e.g., both will have the same V_T).

CMOS REGULATED CASCODE CURRENT SOURCE

Circuit Diagram





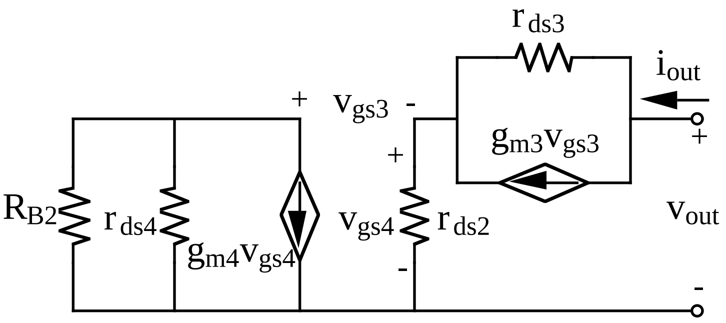
Principle of operation:

As v_{OUT} decreases, M3 will enter the non-saturation region and i_{OUT} will begin to decrease. However, this causes a decrease in the gate-source voltage of M4 which causes an increase in the gate voltage of M3. The minimum value of v_{OUT} is determined by the gate-source voltage of M4 and Vdsat of M3. Assume that all devices are in saturation.

$$v_{OUT}(\min) = \sqrt{\frac{2I_{B2}}{K'(W/L)_4}} + \sqrt{\frac{2I_{out}}{K'(W/L)_3}} + V_{T4}$$

CMOS REGULATED CASCODE CURRENT SOURCE - CONT.

Small Signal Model



(Ignore bulk effects)

$$i_{out} = g_{m3}v_{gs3} + g_{ds3}(v_{out} - v_{gs4})$$

$$v_{gs4} = i_{out}r_{ds2}$$

$$v_{gs3} = v_{g3} - v_{s3} = -g_{m4}(r_{ds4}||R_{B2})v_{gs4} - v_{gs4}$$

$$= -r_{ds2}[1 + g_{m4}(r_{ds4}||R_{B2})]i_{out}$$

$$\therefore \quad i_{out} = -g_{m3}r_{ds2}[1 + g_{m4}(r_{ds4}||R_{B2})]i_{out} + g_{ds3}v_{out} - g_{ds3}r_{ds2}i_{out}$$

Solving for v_{out},

$$v_{out} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}||R_{B2})]i_{out}$$

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}||R_{B2})]$$

$$\boxed{r_{out} = r_{ds3}g_{m3}r_{ds2}g_{m4}(r_{ds4}||R_{B2}) = \frac{g_m{}^2r^3}{2}}$$

Example

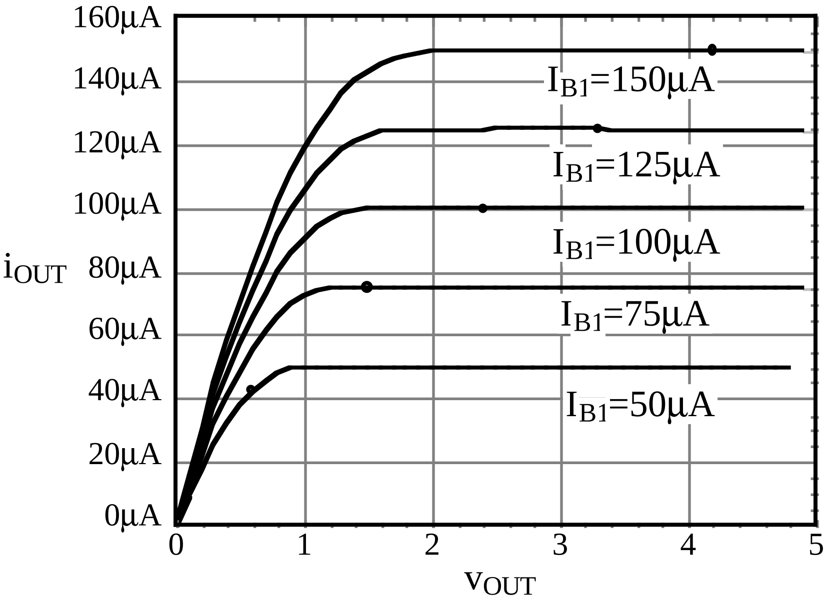
$K'_N = 25\mu A/V^2$, $\lambda = 0.01$, $I_{B1} = I_{B2} = 100\mu A$, all transistors with minimum geometry (W = 3µm, L=3µm), and $R_{B2} = r_{ds}$, we get

$r_{ds} = 1M\Omega$ and $g_m = 70.7\mu mho$

$r_{out} \approx (1M\Omega)(70.7\mu mho)((1M\Omega)(70.7\mu mho)(1M\Omega||1M\Omega) = 2.5G\Omega$!!!

CMOS REGULATED CASCODE CURRENT SOURCE - CONT.

SPICE Simulation



SPICE Input File

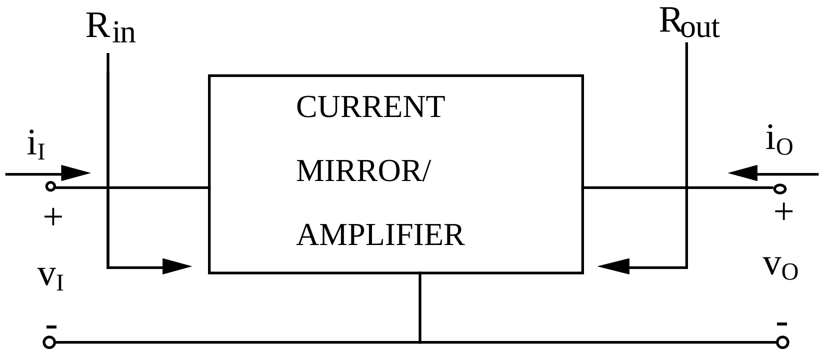
```
CMOS Regulated Cascode Current Sink
VDD 6 0 DC 5.0
IB1 6 4 DC 25U
VOUT 1 0 DC 5.0
M1 4 4 0 0 MNMOS1 W=15U L=3U
M2 3 4 0 0 MNMOS1 W=15U L=3U
M3 1 2 3 0 MNMOS1 W=30U L=3U
M4 2 3 0 0 MNMOS1 W=15U L=3U
M5 5 4 0 0 MNMOS1 W=15U L=3U
M6 5 5 6 6 MPMOS1 W=15U L=3U
M7 2 5 6 6 MPMOS1 W=6U L=3U
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
.MODEL MPMOS1 PMOS VTO=-0.75 KP=8U
+LAMBDA=0.02 GAMMA=0.4 PHI=0.6
.DC VOUT 5 0 0.1 IB1 50U 150U 25U
.OP
.PRINT DC ID(M3)
.PROBE
.END
```

SUMMARY OF CURRENT SINKS/SOURCES

Current Sink/Source	r_{OUT}	Minimum Voltage
Simple	r_{ds}	V_{ON}
Cascode	$\approx g_{m2}r_{ds2}r_{ds1}$	$V_T + 2\ V_{ON}$
High-Swing Cascode	$\approx g_{m2}r_{ds2}r_{ds1}$	$2\ V_{ON}$
Regulated Cascode	$\approx g_m{}^2r_{ds}{}^3$	$V_T + 2\ V_{ON}$

V.4 - CURRENT MIRRORS/AMPLIFIERS

What Is A Current Mirror/Amplifier ?

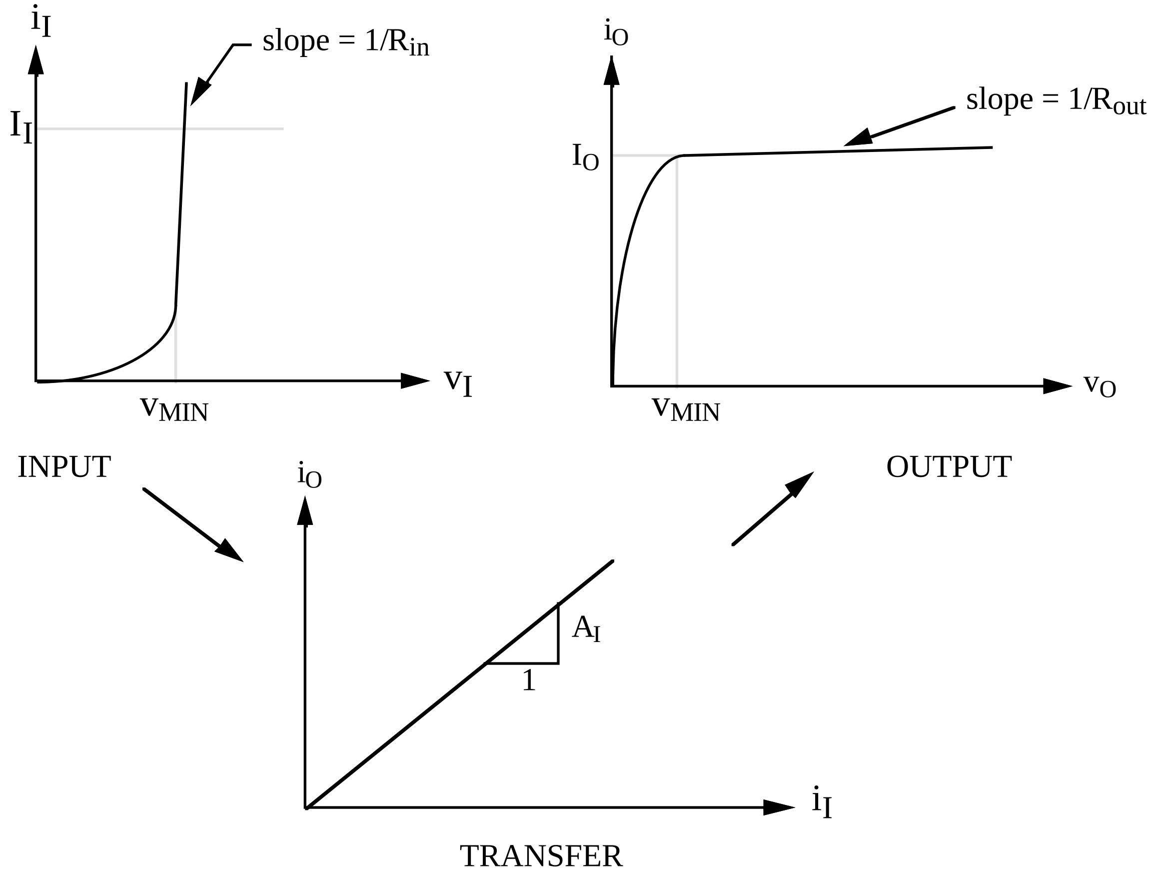


Ideally,

$$i_O = A_I\, i_I$$

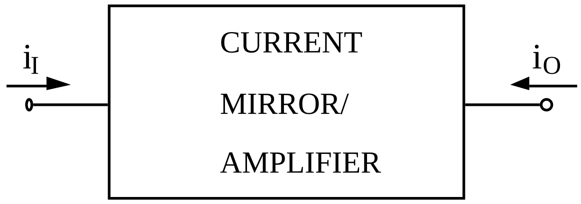
$$R_{in} \approx 0 \qquad R_{out} \approx \infty$$

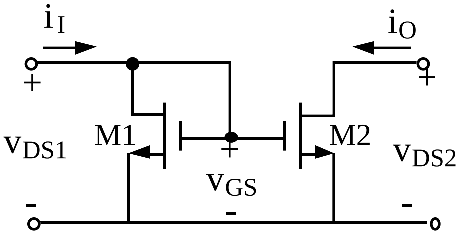
Graphical Characterization



CURRENT MIRROR AND CURRENT AMPLIFIERS

Sources of Errors





In general,

$$\frac{i_O}{i_I} = \left(\frac{W_2L_1}{W_1L_2}\right)\left(\frac{v_{GS} - V_{T2}}{v_{GS} - V_{T1}}\right)^2 \left(\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right)\left(\frac{\mu_{o2}C_{ox2}}{\mu_{o1}C_{ox1}}\right)$$

If the devices are matched,

$$\frac{i_O}{i_I} = \left(\frac{W_2L_1}{W_1L_2}\right)\left(\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right)$$

If $v_{DS1} = v_{DS2}$,

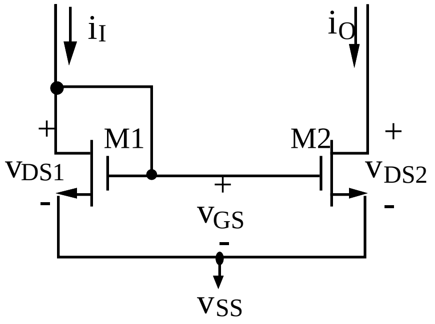
$$\boxed{\frac{i_O}{i_I} = \frac{W_2L_1}{W_1L_2}}$$

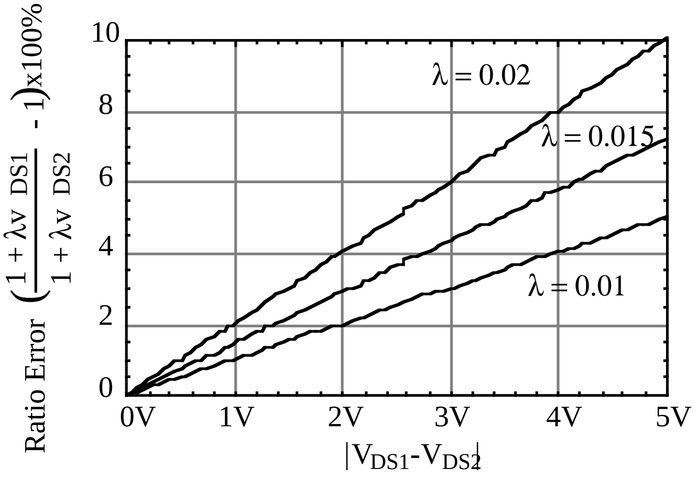
Therefore the sources of error are:

1). $v_{DS1} \neq v_{DS2}$
2). M1 and M2 not matched ($\Delta\beta$ and ΔV_T)

Simple Current Mirror With $\lambda \neq 0$

Circuit -





Ratio error (%) versus drain voltage difference -

Used to measure λ -

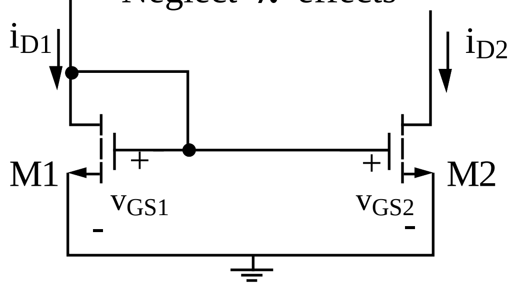
$$\frac{i_O}{i_I} = \left(\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}}\right)\left(\frac{S_1}{S_2}\right)$$

If $S_1 = S_2$, $v_{DS2} = 10\text{V}$, $v_{DS1} = 1\text{V}$, and $i_O/i_I = 1.501$, then

$$\therefore \frac{i_O}{i_I} = 1.501 = \frac{1+10\lambda}{1+\lambda} \quad \text{--->} \ \lambda = \frac{0.5}{8.5} = 0.059$$

Matching Accuracy of MOS Current Mirrors

Neglect λ effects



$$\frac{i_O}{i_I} = \frac{i_{D2}}{i_{D1}} = \frac{\beta_2(v_{GS2}-V_{T2})^2}{\beta_1(v_{GS1}-V_{T1})^2}$$

$(v_{DS2} > v_{GS2} - V_{T1})$

Define: $\Delta\beta = \beta_2 - \beta_1$ and $\beta = \dfrac{\beta_1 + \beta_2}{2}$

$\Delta V_T = V_{T2} - V_{T1}$ and $V_T = \dfrac{V_{T1}+V_{T2}}{2}$

$$\therefore\ \beta_1 = \beta - \frac{\Delta\beta}{2}\ ,\ \beta_2 = \beta + \frac{\Delta\beta}{2}\ ,\ V_{T1} = V_T - \frac{\Delta V_T}{2}$$

and $V_{T2} = V_T + \dfrac{\Delta V_T}{2}$

Thus,

$$\frac{i_O}{i_I} = \frac{\left(\beta+\frac{\Delta\beta}{2}\right)\left(v_{GS} - v_T - \frac{\Delta V_T}{2}\right)^2}{\left(\beta-\frac{\Delta\beta}{2}\right)\left(v_{GS} - v_T + \frac{\Delta V_T}{2}\right)^2} = \frac{\left(1 + \frac{\Delta\beta}{2\beta}\right)}{\left(1 - \frac{\Delta\beta}{2\beta}\right)}\left(\frac{1-\frac{\Delta V_T}{2(v_{GS}-V_T)}}{1+\frac{\Delta V_T}{2(v_{GS}-V_T)}}\right)^2$$

$$\frac{i_O}{i_I} \approx \left(1+\frac{\Delta\beta}{2\beta}\right)\left(1+\frac{\Delta\beta}{2\beta}\right)\left[\left(1-\frac{\Delta V_T}{2(v_{GS}-V_T)}\right)\left(1-\frac{\Delta V_T}{2(v_{GS}-V_T)}\right)\right]^2$$

$$\frac{i_O}{i_I} \approx 1 + \frac{\Delta\beta}{\beta} - \frac{2\Delta V_T}{(v_{GS} - V_T)},$$

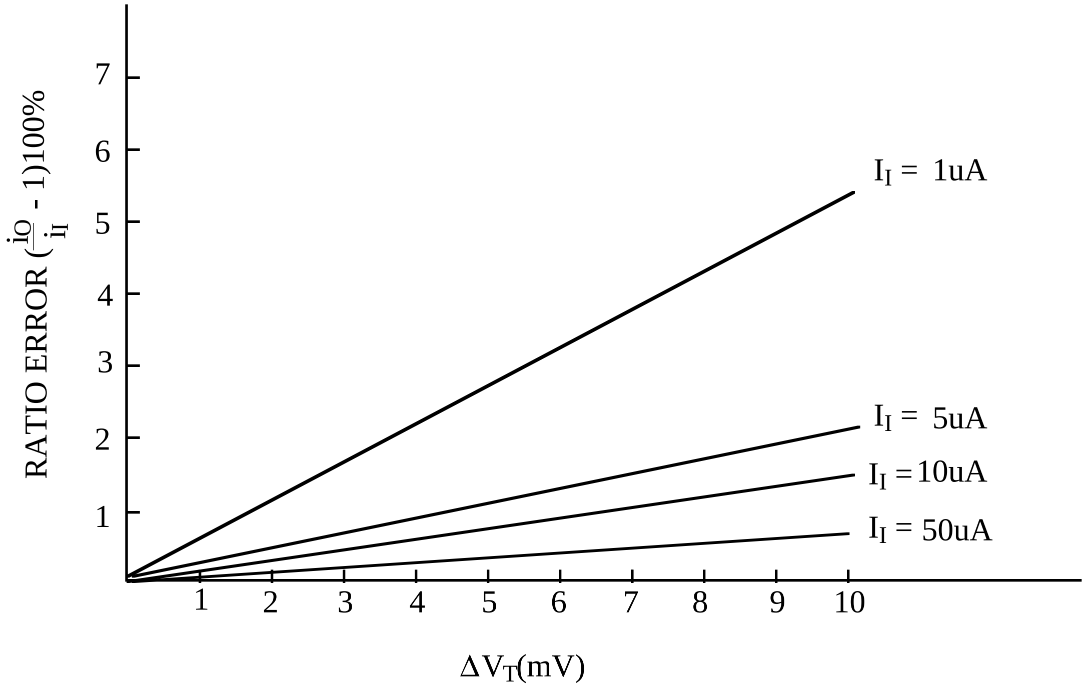
$$\frac{\Delta\beta}{\beta} \approx \pm 5\%\ ,\quad \frac{\Delta V_T}{(v_{GS} - V_T)} = \pm 10\%$$

$$\therefore\quad \frac{i_O}{i_I} \approx 1 \pm 0.05 - (\pm 0.2) = 1 \pm 0.15$$

$= 1 \pm 0.25$ if β and V_T are correlated

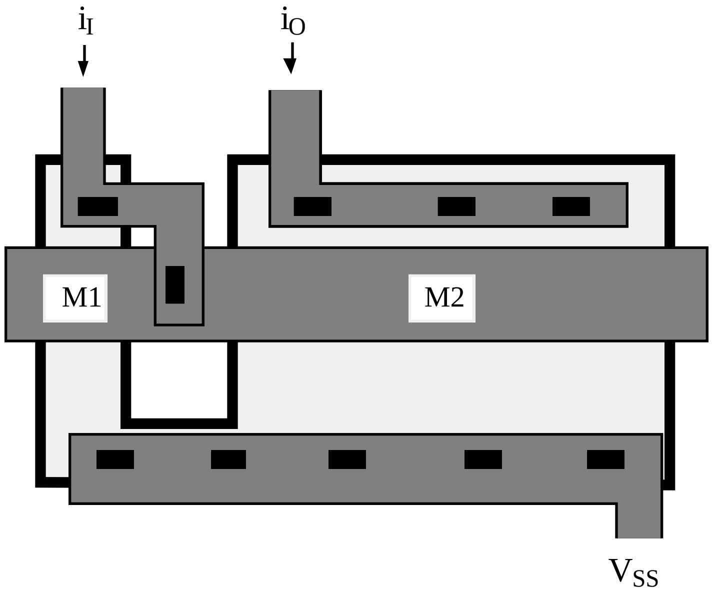
Matching Accuracy - Continued

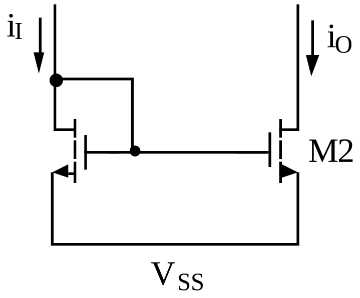
Illustration



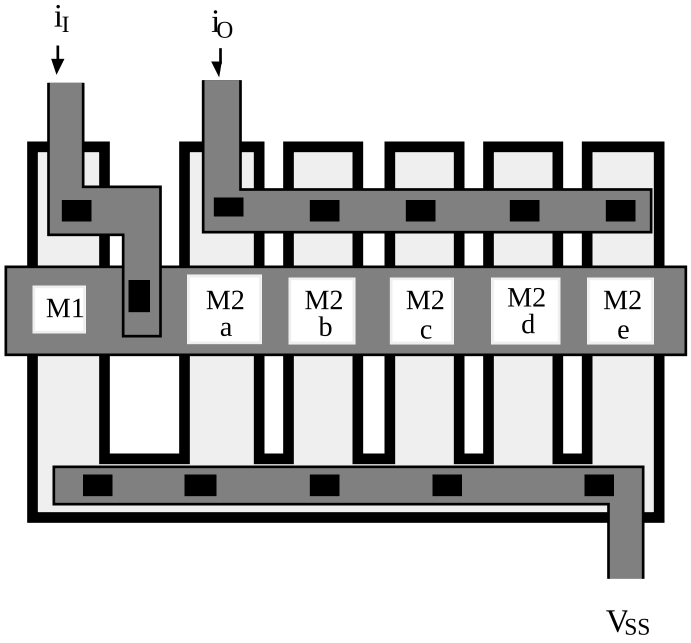
Layout Techniques to Remove Layout Error

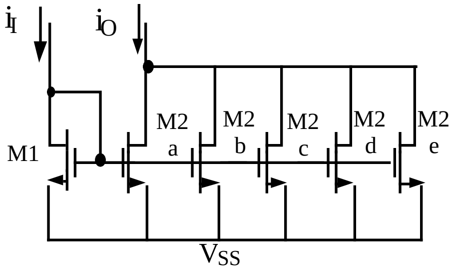
Layout without correction technique -





Layout with correction technique -

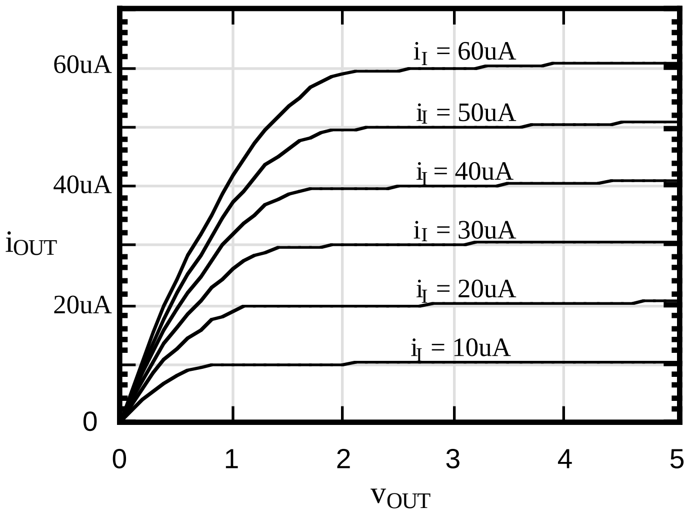




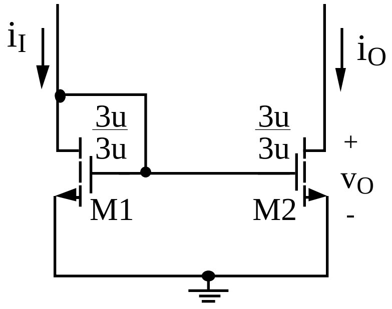
Practical Current Mirrors/Amplifiers

- Simple mirror
- Cascode current mirror
- Wilson current mirror

Simple Current Mirror -

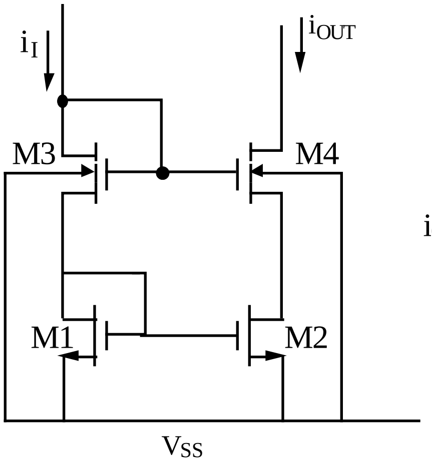


```
Current mirrors and amplifiers
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
M1 1 1 0 0 MNMOS1 W=3U L=3U
M2 3 1 0 0 MNMOS1 W=3U L=3U
IIN 0 1
VOUT 3 0
.DC VOUT 0 5 0.1
+IIN 0 60U 10U
.PRINT DC ID(M2)
.PROBE
.END
```

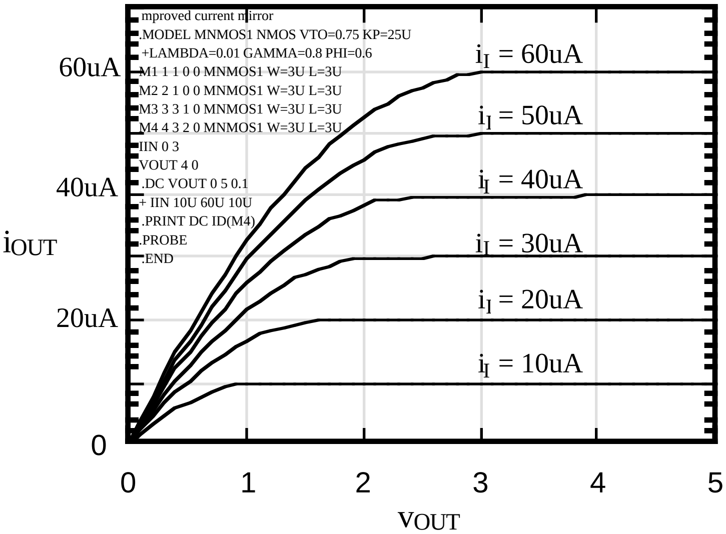


Cadcode Current Mirror

CIRCUIT

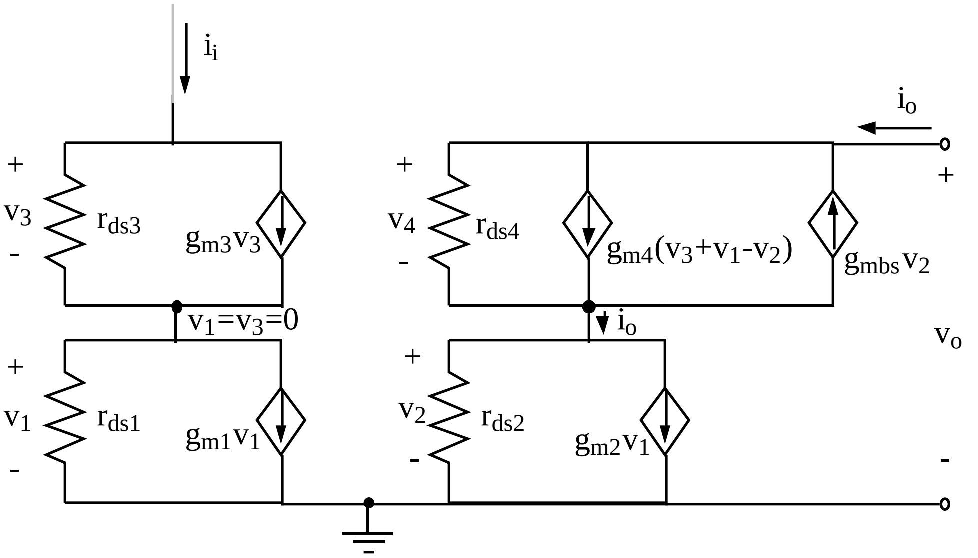


SPICE



```
mproved current mirror
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
 +LAMBDA=0.01 GAMMA=0.8 PHI=0.6
M1 1 1 0 0 MNMOS1 W=3U L=3U
M2 2 1 0 0 MNMOS1 W=3U L=3U
M3 3 3 1 0 MNMOS1 W=3U L=3U
M4 4 3 2 0 MNMOS1 W=3U L=3U
IIN 0 3
VOUT 4 0
 .DC VOUT 0 5 0.1
+ IIN 10U 60U 10U
 .PRINT DC ID(M4)
.PROBE
 .END
```

Example of Small Signal Output Resistance Calculation -



1). $v_o = v_4 + v_2 = r_{ds4}\,[i_o - g_{m4}(v_3 + v_1 - v_2) + g_{mbs4}v_2] + r_{ds2}(i_o - g_{m2}v_1)$

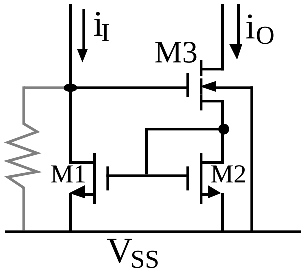
2). $v_2 = i_o r_{ds2}$

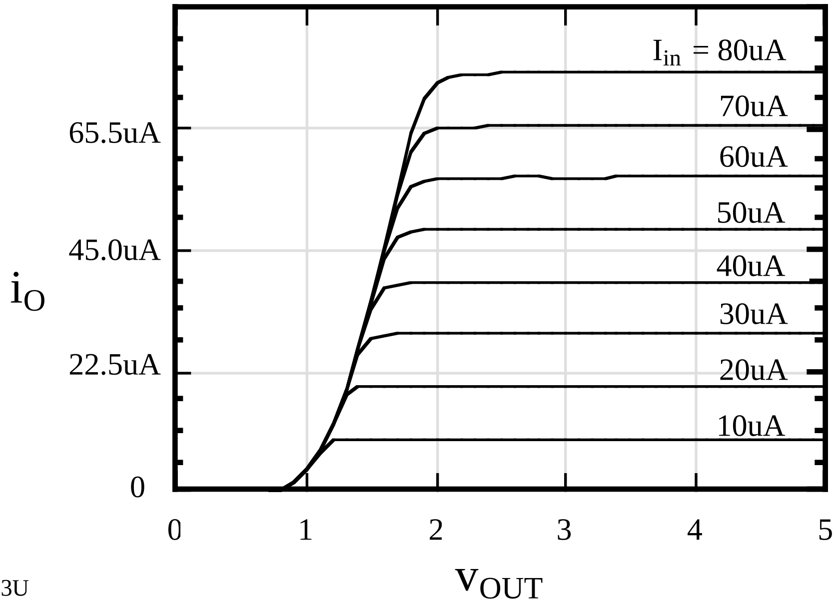
3). $v_o = i_o\,[r_{ds4} + (g_{m4}r_{ds2})r_{ds4} + (r_{ds2}g_{mbs4})r_{ds4} + r_{ds2}]$

4). $r_{out} = \dfrac{v_o}{i_o} = r_{ds4} + r_{ds2} + r_{ds2}r_{ds4}(g_{m4} + g_{mbs4})$

Wilson Current Mirror

Circuit and Performance-





```
Wilson Current Source
M1 1 2 0 0 MNMOS W=15U L=3U
M2 2 2 0 0 MNMOS W=15U L=3U
M3 3 1 2 0 MNMOS W=15U L=3U
R  1 0 100MEG
.MODEL MNMOS NMOS VTO=0.75, KP=25U,
+LAMBDA=0.01, GAMMA=0.8 PHI=0.6
IIN 0 1
VOUT 3 0
.DC VOUT 0 5 0.1 IIN 10U 80U 10U
.PRINT DC  V(2)  V(1) ID(M3)
.PROBE
.END
```

Principle of Operation:

Series negative feedback increase output resistance

1. Assume input current is constant and that there is high resistance to ground from the gate of M3 or drain of M1.

2. A positive increase in output current causes an increase in v_{GS2}.

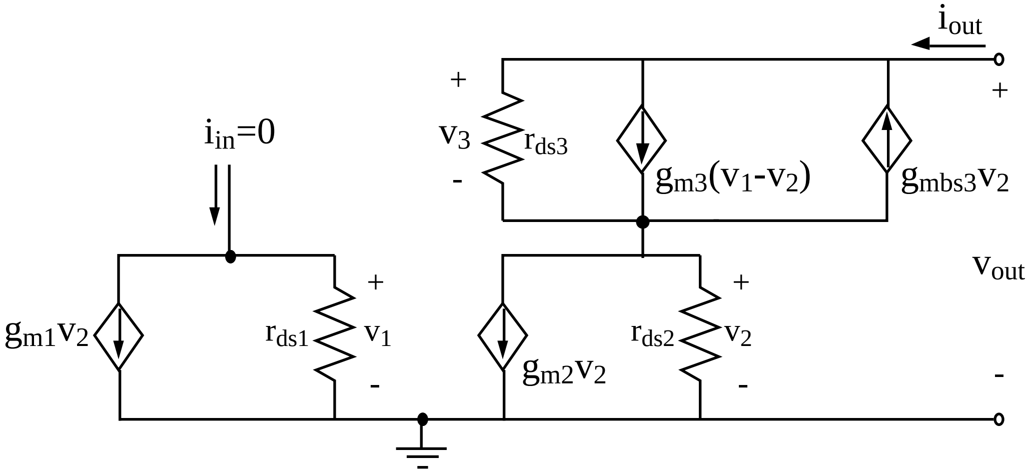
3. The increase in v_{GS2} causes an increase in v_{GS1}.

4. The increase in v_{GS1} causes an increase in i_{D1}.

5. If the input current is constant, then the current through the resistance to ground from the gate of M3 or the drain of M1 decreases resulting in a decrease in v_{GS3}.

6. A decrease in v_{GS3} causes a decrease in the output current opposing the assumed increase in step 2.

Output Impedance of the Wilson Current Source



$$v_{out} = r_{ds3}[i_{out} - g_{m3}v_1 + g_{m3}v_2 + g_{mbs3}v_2] + v_2$$

$$v_{out} = r_{ds3}i_{out} - g_{m3}r_{ds3}(-g_{m1}r_{ds1}v_2) + g_{m3}r_{ds3}v_2 + g_{mbs3}r_{ds3}v_2 + v_2$$

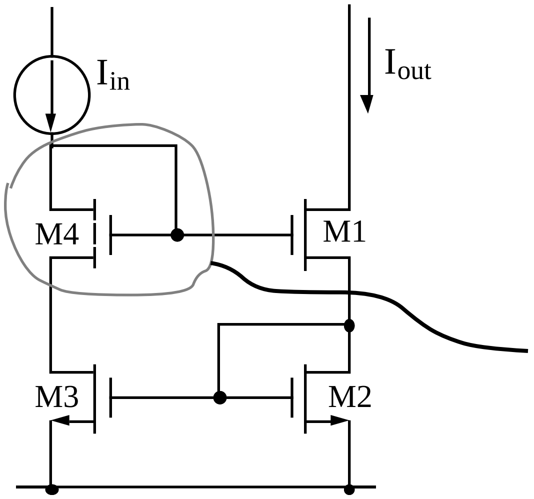
$$v_2 \;\; = i_{out}\left[\frac{rds2}{1 + gm2rds2}\right]$$

$$v_{out} = i_{out}r_{ds3} + [g_{m3}r_{ds3} + g_{mbs3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3}]v_2 + v_2$$

$$r_{out} = r_{ds3} + r_{ds2}\left[\frac{1 + gm3rds3 + gmbs3rds3 + gm1rds1gm3rds3}{1+gm2rds2}\right]$$

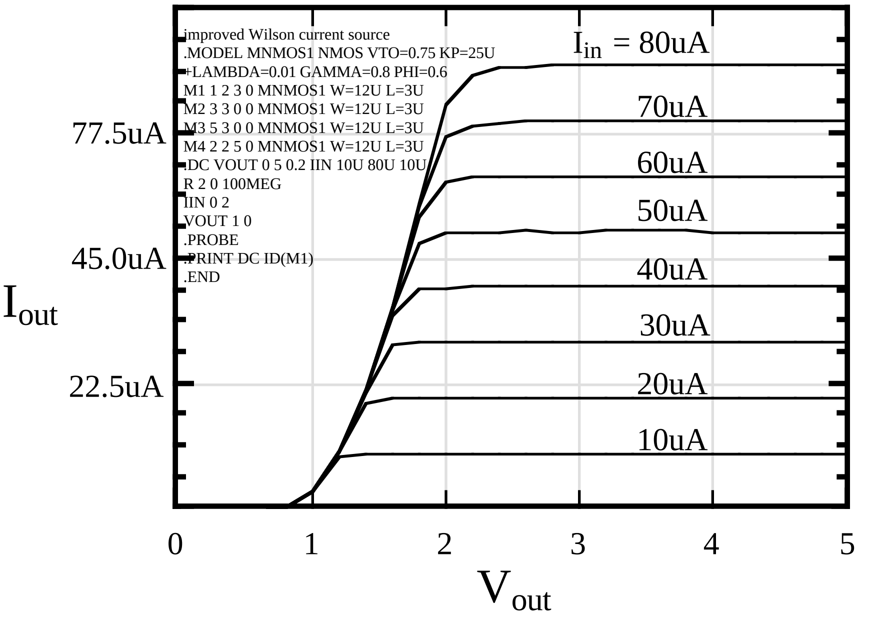
$$\boxed{r_{out} \approx \frac{r_{ds2}g_{m1}r_{ds1}g_{m3}r_{ds3}}{g_{m2}r_{ds2}} \approx r_{ds1} \times (g_{m3}r_{ds3}) \text{ if } g_{m1} = g_{m2}}$$

Improved Wilson Current Mirror



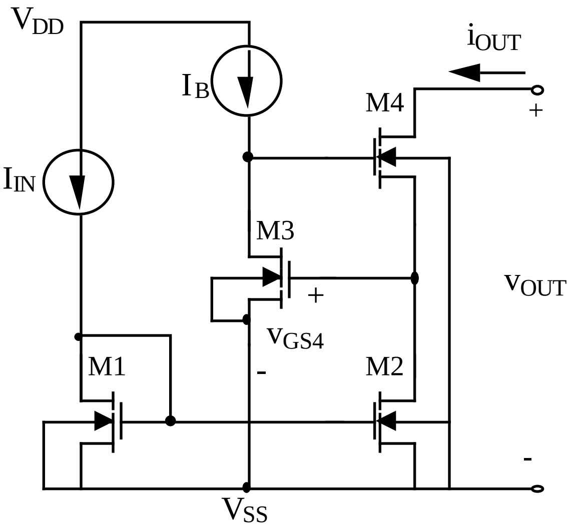
Additional diode-connected transistor equalizes the drain-source voltage drops of transistors M2 and M3

SPICE simulation

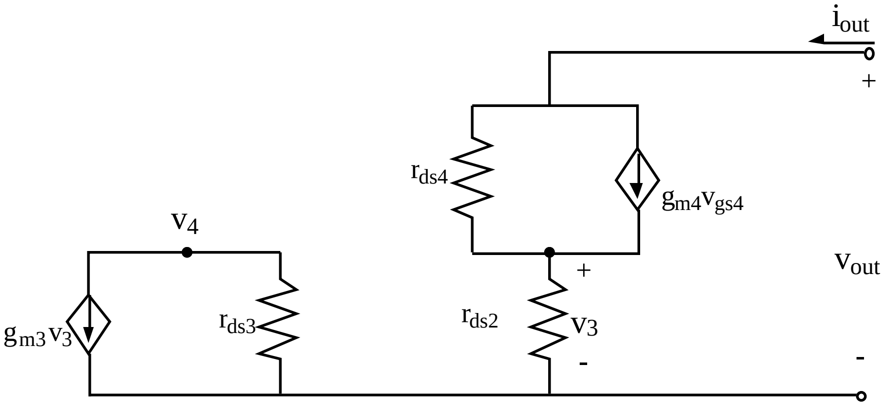


```
improved Wilson current source
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
M1 1 2 3 0 MNMOS1 W=12U L=3U
M2 3 3 0 0 MNMOS1 W=12U L=3U
M3 5 3 0 0 MNMOS1 W=12U L=3U
M4 2 2 5 0 MNMOS1 W=12U L=3U
.DC VOUT 0 5 0.2 IIN 10U 80U 10U
R 2 0 100MEG
IIN 0 2
VOUT 1 0
.PROBE
.PRINT DC ID(M1)
.END
```

Regulated Cascode Current Mirror



Small Signal Equivalent Model (g_{mbs} effects ignored) -



$v_{out} = (i_{out} - g_{m4}v_{gs4})r_{ds4} + i_{out}r_{ds2}$

$v_{gs4} = v_4 - v_3$

$v_3 \ \ = i_{out}r_{ds2}$

$v_4 \ \ = -g_{m3}v_3r_{ds3}$

$v_{out} = i_{out}r_{ds4} - g_{m4}(-g_{m3}i_{out}r_{ds2}r_{ds3} - i_{out}r_{ds2})r_{ds4} + i_{out}r_{ds2}$

$r_{out} = r_{ds4} + g_{m4}g_{m3}\, r_{ds2}r_{ds3}r_{ds4} + r_{ds2} + g_{m4}r_{ds2}r_{ds4}$

$$v_{OUT}(\min) = \sqrt{\frac{2I_B}{K'(W/L)_4}} + \sqrt{\frac{2I_{out}}{K'(W/L)_3}} + V_{T4}$$

SUMMARY OF CURRENT MIRRORS

Current Mirror	Accuracy	Output Resistance	Minimum Voltage
Simple	Poor (Lambda)	r_{ds}	V_{ON}
Cascode	Excellent	$g_m r_{ds}^2$	$V_T + 2V_{ON}$
Wilson	Excellent	$g_m r_{ds}^2$	$2V_{ON}$
Regulated Cascode	Good	$g_m^2 r_{ds}^3$	$V_T + 2V_{ON}$

V.5 - REFERENCE CIRCUITS

Introduction

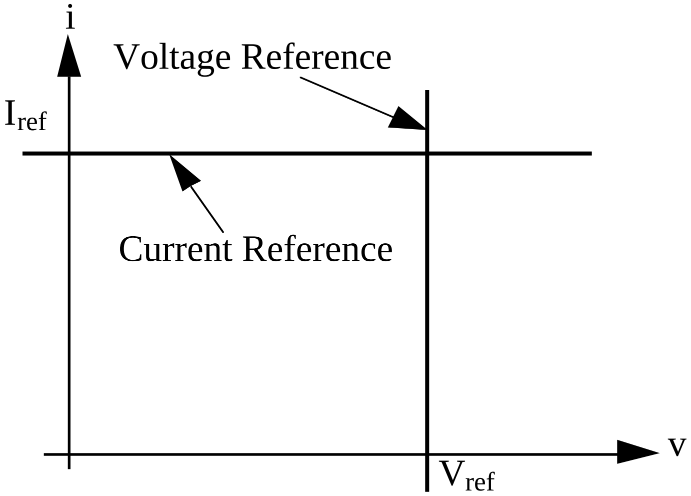
What is a Reference Circuit?

A reference circuit is an independent voltage or current source which has a high degree of precision and stability.

Requirements for a Reference Circuit

1.) Output voltage/current should be independent of power supply.
2.) Output voltage/current should be independent of temperature.
3.) Output voltage/current should be independent of processing variations.

V-I Characteristics of an Ideal Reference



Concept of Sensitivity

Definition

Sensitivity is a measure of dependence of V_{ref} (I_{ref}) upon a parameter or variable *x* which influences V_{ref} (I_{ref}).

$$\underset{x}{\overset{V_{ref}}{S}} = \frac{\dfrac{\partial V_{ref}}{V_{ref}}}{\dfrac{\partial x}{x}} = \left(\frac{x}{V_{ref}}\right)\left(\frac{\partial V_{ref}}{\partial x}\right)$$

where

$x = V_{DD}$ or temperature

Application of Sensitivity

$$\frac{\partial V_{ref}}{V_{ref}} = \left(\underset{x}{\overset{V_{ref}}{S}}\right)\left(\frac{\partial x}{x}\right)$$

For example, if the sensitivity is 1, then a 10% change in x will cause a 10% change in V_{ref}.

Ideally, $\underset{x}{\overset{V_{ref}}{S}} \rightarrow 0$

V.5-1 - SIMPLE REFERENCES

Objective is to minimize,

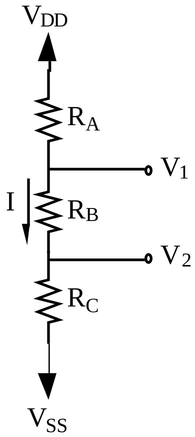
$$S_{V_{DD}}^{V_{ref}} = \frac{\dfrac{\partial V_{ref}}{V_{ref}}}{\dfrac{\partial V_{DD}}{V_{DD}}}$$

Types of references include,

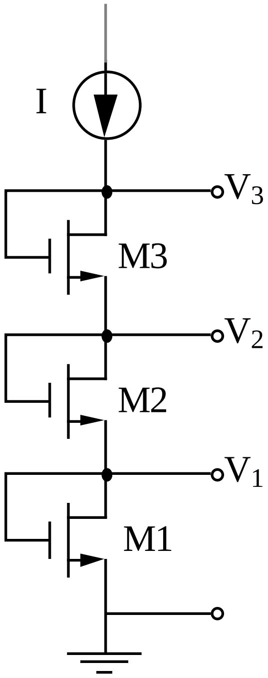
1. Voltage dividers - passive and active.
2. MOS diode reference.
3. PN junction diode reference.
4. Gate-source threshold referenced circuit.
5. Base-emitter referenced circuit.

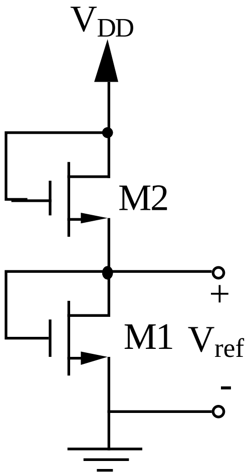
Passive Divider

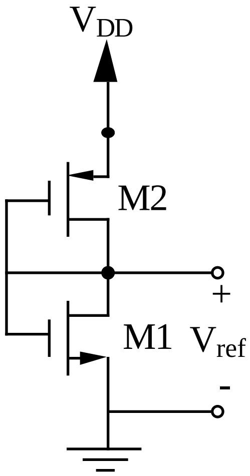
Accuracy is approximately equivalent to 6 bits (1/64).



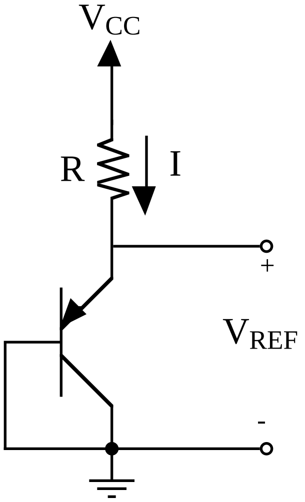
Active Dividers







PN Junction Voltage References



$$V_{REF} = V_{BE} = \frac{kT}{q}\ln\left(\frac{I}{I_s}\right) = V_t \ln\left(\frac{I}{I_s}\right)$$

$$\text{If } I = \frac{V_{CC} - V_{BE}}{R} \approx \frac{V_{CC}}{R}$$

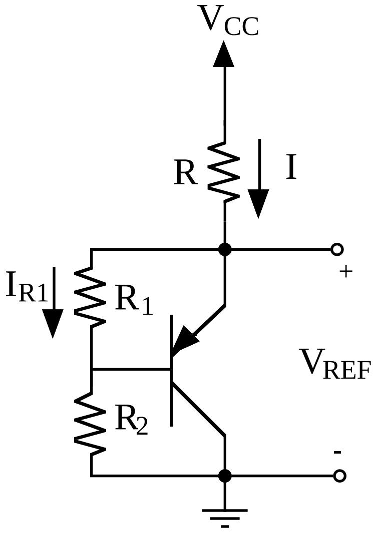
$$\boxed{V_{REF} \approx V_t \ln\left(\frac{V_{CC}}{RI_s}\right)}$$

Sensitivity:

$$S_{V_{CC}}^{V_{REF}} = \frac{1}{\ln\left(\frac{V_{CC}}{RI_s}\right)}$$

If V_{CC} = 10V, R = 10 kΩ, and $I_s = 10^{-15}$A, then $S_{V_{CC}}^{V_{REF}} = 0.0362$.

Modifying the Value of V_{REF}



If β >> 1, then $V_{REF} \approx I_{R1}(R_1+R_2)$

replacing $I_{R1}$by $\frac{V_{BE}}{R_1}$ gives,

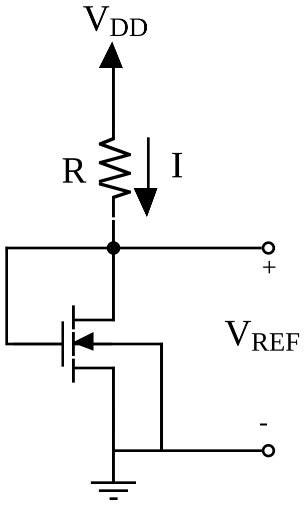
$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_1}\right)V_{BE}$$

or

$$\boxed{V_{REF} \approx \left(\frac{R_1+R_2}{R_1}\right)V_t \ln\left(\frac{V_{CC}}{RI_s}\right)}$$

Gate-Source Referenced Circuits

(MOS equivalent of the pn junction referenced circuit)



$$V_{REF} = V_{GS} = V_T + \sqrt{\frac{2(V_{DD}-V_{REF})}{\beta R}}$$

$$\boxed{V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD}-V_T)}{\beta R} + \frac{1}{\beta^2 R^2}}}$$

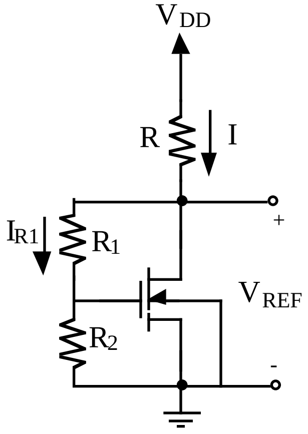
Sensitivity:

$$S_{V_{DD}}^{V_{REF}} = \frac{V_{DD}}{V_{REF}}\left(\frac{1}{1 + \beta R(V_{REF} - V_T)}\right)$$

If V_{DD} = 10V, W/L = 10, R = 100kΩ and using the results of Table 3.1-2 gives

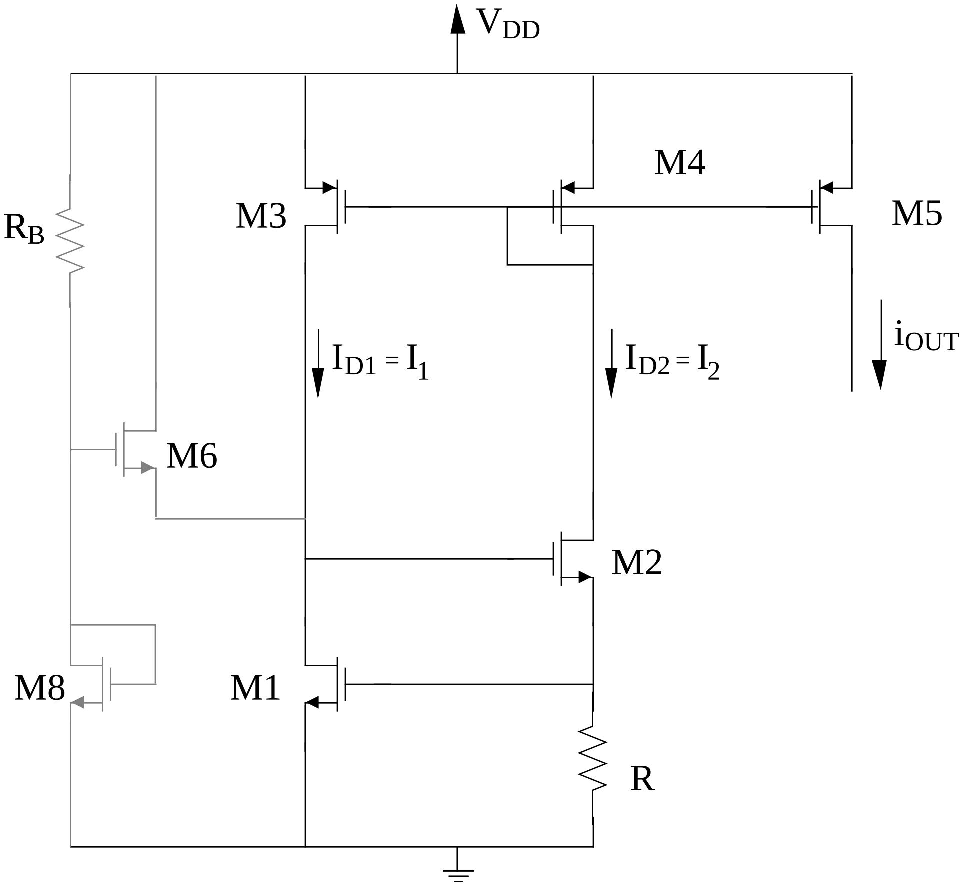
V_{REF} = 1.97V.and $S_{V_{DD}}^{V_{REF}}$ = 0.29.

Modifying the Value of V_{REF}



$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_2}\right) V_{GS}$$

Bootstrapped Current Source



Principle:

If M3 = M4, then

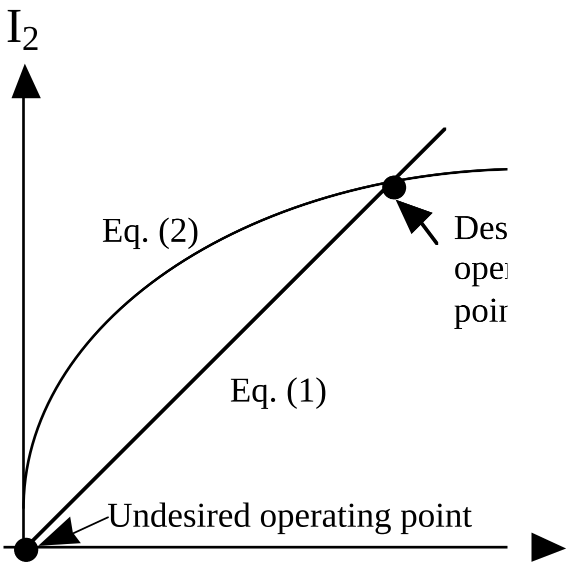
$$I_1 = I_2 \qquad (1)$$

also,

$$V_{GS1} = V_{T1} + \sqrt{\frac{2I_1}{K_N S_1}} = I_2 R$$

therefore,

$$I_2 = \frac{V_{T1}}{R} + \left(\frac{1}{R}\right)\sqrt{\frac{2I_1}{K_N S_1}} \qquad (2)$$



Bootstrapped Current Sink/Source - Continued

An examination of the second-order effects of this circuit-

The relationship between M1 and R can be expressed as,

$$I_2R = V_{T1} + \sqrt{\frac{2I_1}{\beta_1}}$$

Instead of assuming that $I_1 = I_2$ because of the current mirror, M3-M4, let us consider the effects of the channel modulation which gives

$$I_2 = I_1\left[\frac{1 + \lambda_P V_{GS4}}{1 + \lambda_P(V_{DD} - V_{DS1})}\right]$$

Solving for I_1 from the above two expressions gives

$$I_1R(1 + \lambda_P V_{GS4}) = [1 + \lambda_P(V_{DD} - V_{DS1})]\sqrt{\frac{2I_1}{\beta_1}}$$

Differentiating with respect to V_{DD} and assuming the V_{DS1} and V_{GS4} are constant gives ($I_{OUT} = I_1$),

$$S_{V_{DD}}^{I_{OUT}} = \frac{20V_{DD}\lambda_P\left[V_{T1} + \sqrt{\frac{2I_1}{\beta_1}}\right]}{I_{OUT}\left[R(1 + \lambda_P V_{GS4}) - \frac{1 + \lambda_P(V_{DD} - V_{DS1})}{\sqrt{2\beta_1 I_1}}\right]}$$

Bootstrapped Current Sink/Source - Continued

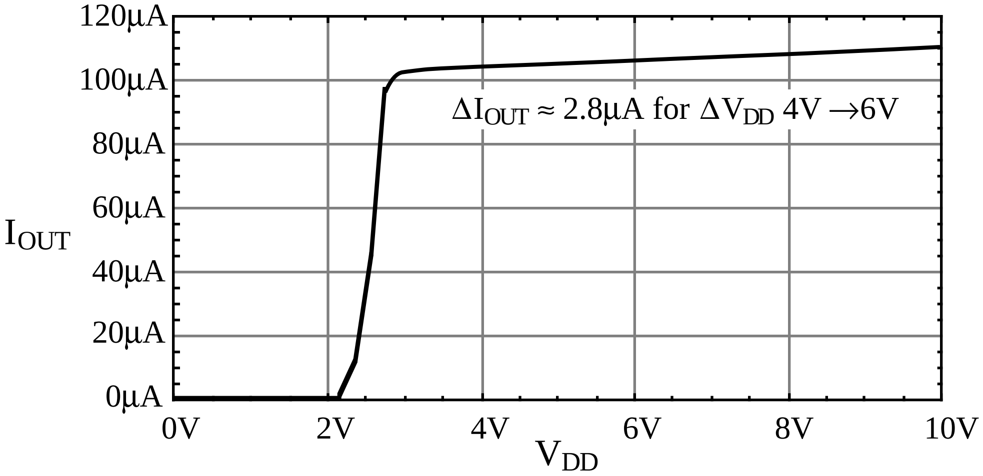
Assume that V_{DD}=5V, K_N' = 23.6 μA/V^2, V_{TN}=0.79V, γ_N=0.53V$^{0.5}$, ϕ_P = 0.590V, λ_N=0.02V^{-1}, K_P' = 5.8μA/V^2, V_{TP}=-0.52V, γ_P=0.67V$^{0.5}$, ϕ_P = 0.6V, λ_N=0.012V^{-1}. Therefore,

V_{GS4} = 1.50V, V_{T2} = 1.085V, V_{GS2} = 1.545V, and V_{DS1} = 2.795V which gives

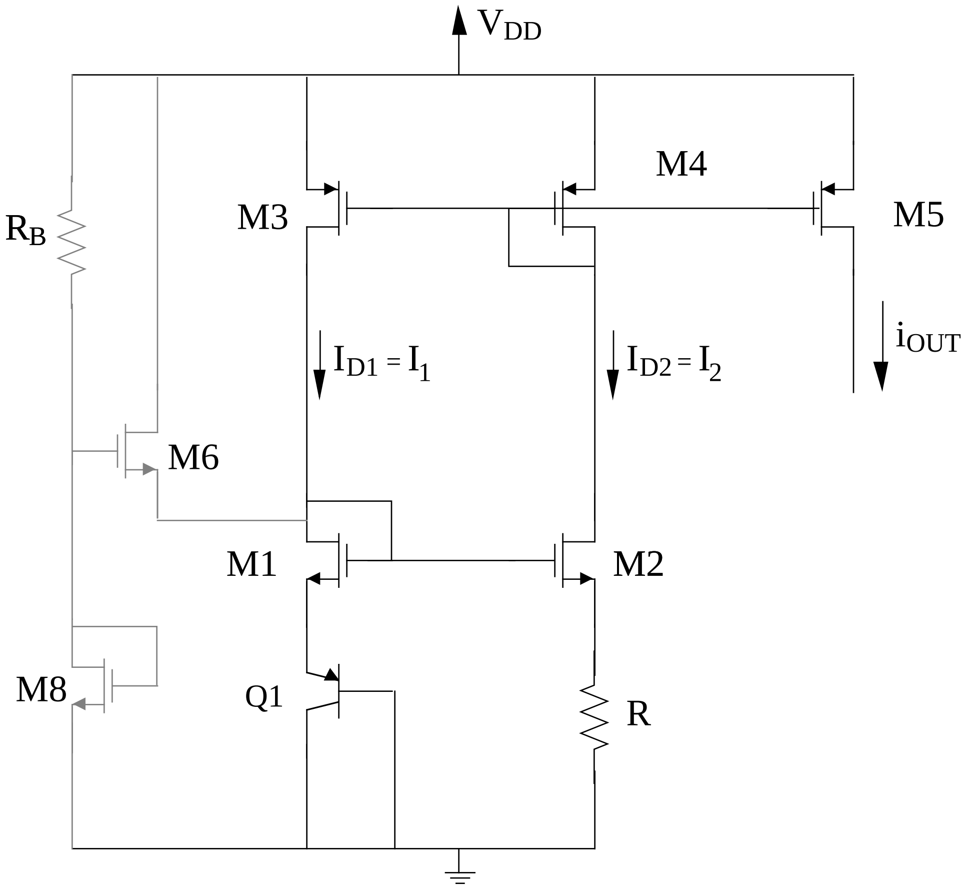
$$\underset{V_{DD}}{\overset{I_{OUT}}{S}} = 0.08 = \frac{\Delta I_{OUT}/I_{OUT}}{\Delta V_{DD}/V_{DD}}$$

If ΔV_{DD} = 6V - 4V = 2V, then $\Delta I_{OUT} = 0.08\ I_{OUT}\left(\frac{\Delta V_{DD}}{V_{DD}}\right) = 3.2\mu A$

SPICE Results:



Base-Emitter Voltage Referenced Circuit



$$I_2 \approx \frac{V_{BE1}}{R} = I_5$$

$$V = I_2 R \approx V_{BE1}$$

V.5-2 - TEMPERATURE DEPENDENCE

Objective

Minimize the fractional temperature coefficient which is defined as

$$T_{CF} = \frac{1}{V_{ref}}\left[\frac{\partial V_{ref}}{\partial T}\right] \quad \text{parts per million per °C or ppm/°C}$$

Temperature Variation of References

PN Junction:

$$\left.\begin{aligned} i &\approx I_s \exp\left(\frac{v}{V_t}\right) \\ I_s &= KT^3 \exp\left(\frac{-V_{GO}}{V_t}\right) \end{aligned}\right\} \frac{1}{I_s}\left(\frac{\partial I_s}{\partial T}\right) = \frac{\partial(\ln I_s)}{\partial T} = \frac{3}{T} + \frac{V_{GO}}{TV_t} \approx \frac{V_{GO}}{TV_t}$$

$$\frac{dv_{BE}}{dT} \approx \frac{V_{BE} - V_{GO}}{T} = -2\text{mV/°C at room temperature}$$

(V_{GO} = 1.205 V and is called the bandgap voltage)

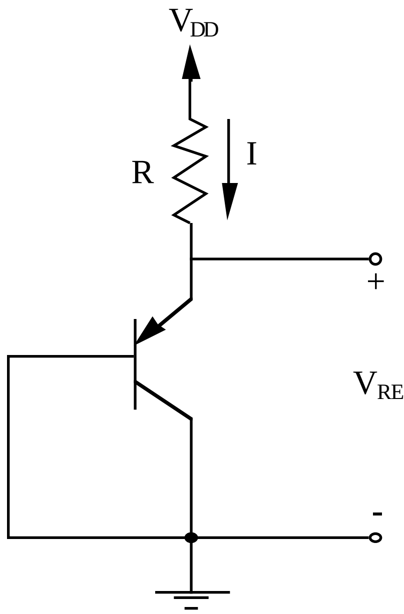
Gate-Source Voltage with constant current (Strong Inversion):

$$\frac{dV_{GS}}{dT} = \frac{dV_T}{dT} + \sqrt{\frac{2L}{WC_{ox}}}\frac{d}{dT}\left(\sqrt{\frac{I_D}{\mu_o}}\right)$$

$$\mu_o = KT^{-1.5} \;\; ; \;\; V_T = V_{T0} - \alpha T \;\; \text{or} \;\; V_T(T) = V_T(T_o) - \alpha(T-T_o)$$

$$\boxed{\frac{dV_{GS}}{dT} = -\alpha + \frac{3}{4}\left(\frac{V_{GS} - V_T}{T}\right)}$$

PN Junction Voltage Reference



$$V_{REF} = V_{BE} = \frac{kT}{q}\ln\left(\frac{I}{I_s}\right) = V_t \ln\left(\frac{I}{I_s}\right)$$

$$I = \frac{V_{DD} - v_{BE}}{R} \approx \frac{V_{DD}}{R} \quad \text{------->} \quad \boxed{V_{REF} = V_t \ln\left(\frac{V_{DD}}{RI_s}\right)}$$

$$TC_F = \frac{1}{V_{REF}}\left(\frac{dV_{REF}}{dT}\right) = \frac{V_{REF} - V_{GO}}{TV_{REF}} - \frac{V_t}{V_{REF}}\left(\frac{dR}{RdT}\right)$$

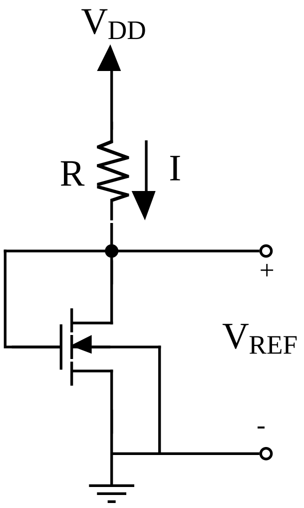
Assume $V_{REF} = 0.6$ volts and that R is a polysilicon resistor $\left(\frac{dR}{RdT} = +1500\text{ ppm/°C}\right)$ gives a

$$TC_F = \frac{0.6 - 1.205}{(300\text{K})(0.6)} - \frac{0.026}{0.6}(0.0015)$$

$$= -0.003361 - 0.000065 = \underline{-3426\text{ ppm/}}\text{°C}$$

Gate - Source Referenced Circuits

MOS Equivalent of the PN Junction Referenced Circuit



$$\boxed{V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD}-V_T)}{\beta R} + \frac{1}{\beta^2 R^2}}}$$

$$\boxed{TC_F = \frac{1}{V_{REF}}\frac{dV_{REF}}{dT} = \frac{1}{V_{REF}}\,\frac{-\alpha + \sqrt{\frac{V_{DD}-V_{REF}}{2\beta R}}\left(\frac{1.5}{T} - \frac{1}{R}\frac{dR}{dT}\right)}{1 + \frac{1}{\sqrt{2\beta R\,(V_{DD}-V_{REF})}}}}$$

Example

W = 2L, V_{DD} = 5V, R = 100 KΩ , K'=110 μ, V_T = 0.7, T = 300 K, α = 2.3 mV/°C

Solving for V_{REF} gives

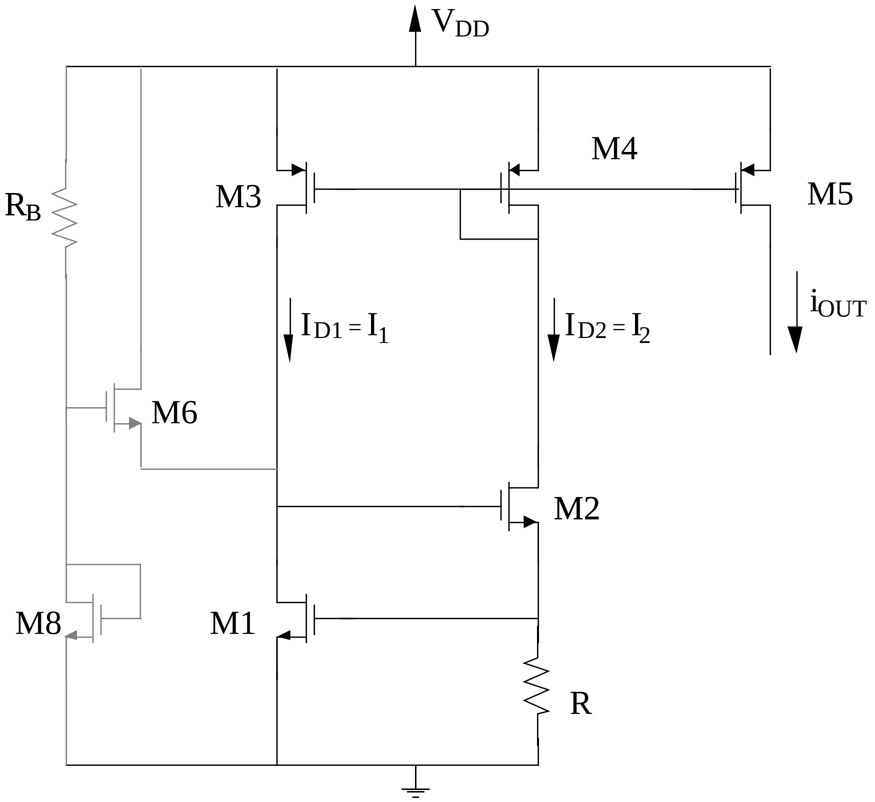
$$V_{REF} = 1.281\text{ V}$$

$$\frac{dR}{RdT} = +1500\text{ ppm/°C}$$

$$TC_F = \frac{1}{1.281}\frac{dV_{REF}}{dT} = \frac{1}{1.281}\,\frac{-2.3\text{€}\times 10^{-3} + \sqrt{\dfrac{5-1.281}{2\times 2\left(110\times 10^{-6}\right)\times 100\text{K}}}\left(\dfrac{1.5}{300} - 1500\times 10^{-6}\right)}{1+\dfrac{1}{\sqrt{2\times 2\left(110\times 10^{-6}\times 100\text{K}\right)\ (5\text{ - }1.281)}}}$$

$$TC_F = -\ 928\text{ ppm/°C}$$

Bootstrapped Current Source/Sink



$$I_{D2} = \frac{V_{GS1}}{R} = \frac{\sqrt{\frac{2I_{D1}L}{K'W}} + V_T}{R} = \frac{V_{ON} + V_T}{R} = I_{D1} = I_{OUT}$$

Assuming that V_{ON} is constant as a function of temperature because of the bootstrapped current reference, then

$$\therefore\ TC_F = \frac{1}{V_T}\frac{dV_T}{dT} - \frac{1}{R}\frac{dR}{dT} = \frac{-\alpha}{V_T} - \frac{1}{R}\frac{dR}{dT}$$

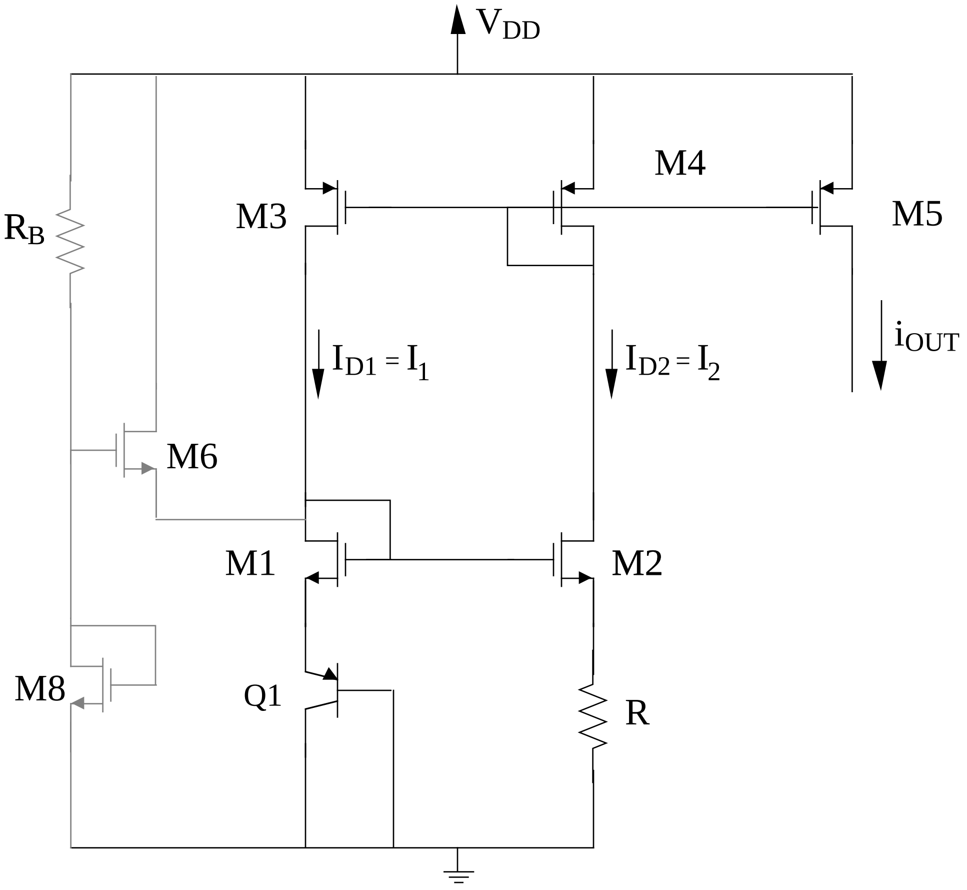
If R is a polysilicon resistor, then

$$TC_F = \frac{-2.3 \times 10^{-3}}{1} - 1.5\text{x}10^{-3} = -3800 \text{ ppm/°C}$$

If R is an implanted resistor, then

$$TC_F = \frac{-2.3 \times 10^{-3}}{1} - 0.4\text{x}10^{-3} = -2700 \text{ ppm/°C}$$

Base-Emitter Voltage - Referenced Circuit



$$I_2 \approx \frac{v_{BE1}}{R} \quad \text{----->} \quad TC_F = \frac{1}{v_{BE}}\frac{dv_{BE}}{dT} - \frac{1}{R}\frac{dR}{dT}$$

Assuming V_{BE} = 0.6 volts and a polysilicon resistor gives

$$TC_F = \frac{1}{0.6}(-2\text{x}10^{-3}) - (1.5\text{x}10^{-3}) = -4833 \text{ ppm/°C}$$

V.6 - SUMMARY

- The circuits in this chapter represent the first level of building blocks in analog circuit design.

- The MOS transistor makes a good switch and a variable resistor with reasonable ranges of linearity in certain applications.

- Primary switch imperfection is clock feedthrough. In order for switches to be used with lower power supplies, V_T must be decreased.

- The primary characteristics defining a current sink or source are V_{MIN} and R_{out}. $V_{MIN} \rightarrow 0$ and $R_{out} \rightarrow \infty$. Typically the product of V_{MIN} times R_{out} is a constant in most designs.

- Current mirrors are characterized by:

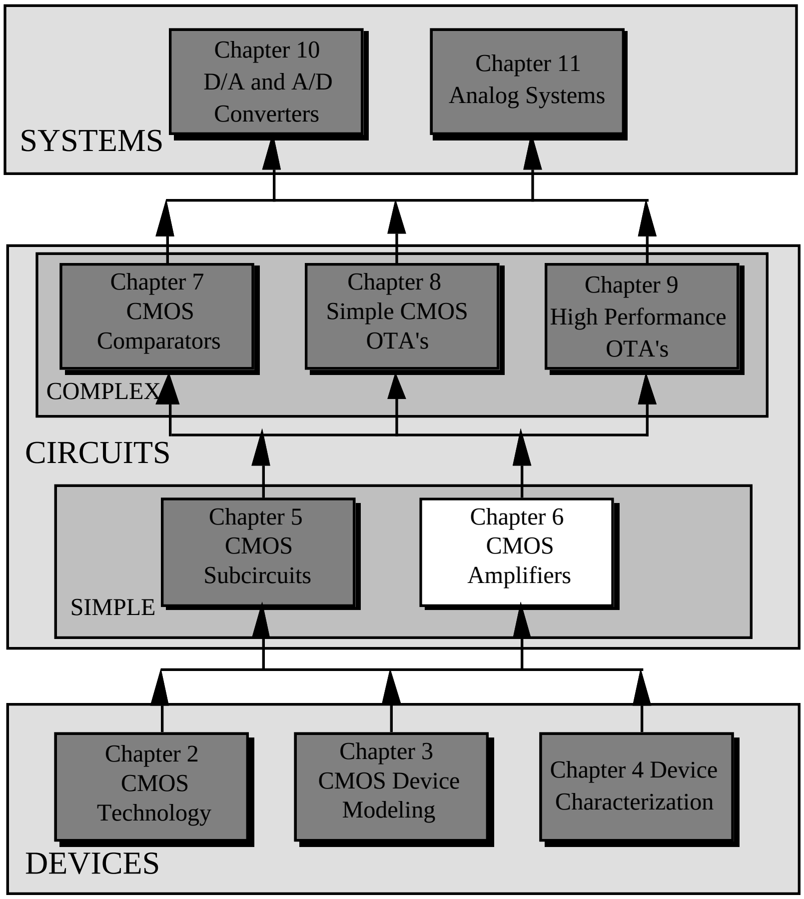
  Gain accuracy
  Gain linearity
  V_{MIN} on output
  R_{out}
  R_{in}

- Reasonably good power supply independent and temperature independent voltage and current references are possible. These references do not satisfy very stable reference requirements.

VI. CMOS AMPLIFIERS

Contents

Organization



VI.1 SIMPLE INVERTING AMPLIFIERS

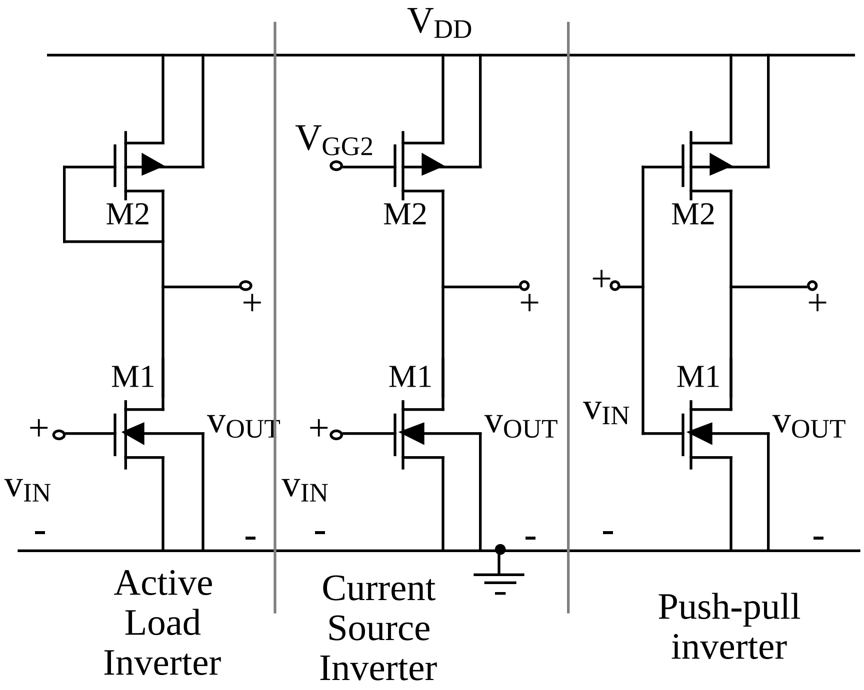
CHARACTERIZATION OF AMPLIFIERS

We shall characterize the amplifiers of this Chapter by the following aspects:

- Large Signal Voltage Transfer Characteristics
- Maximum Signal Swing Limits
- Small Signal Midband Performance
    - Gain
    - Input resistance
    - Output resistance
- Small Signal Frequency Response
- Other Considerations
    - Noise
    - Power
    - Etc.

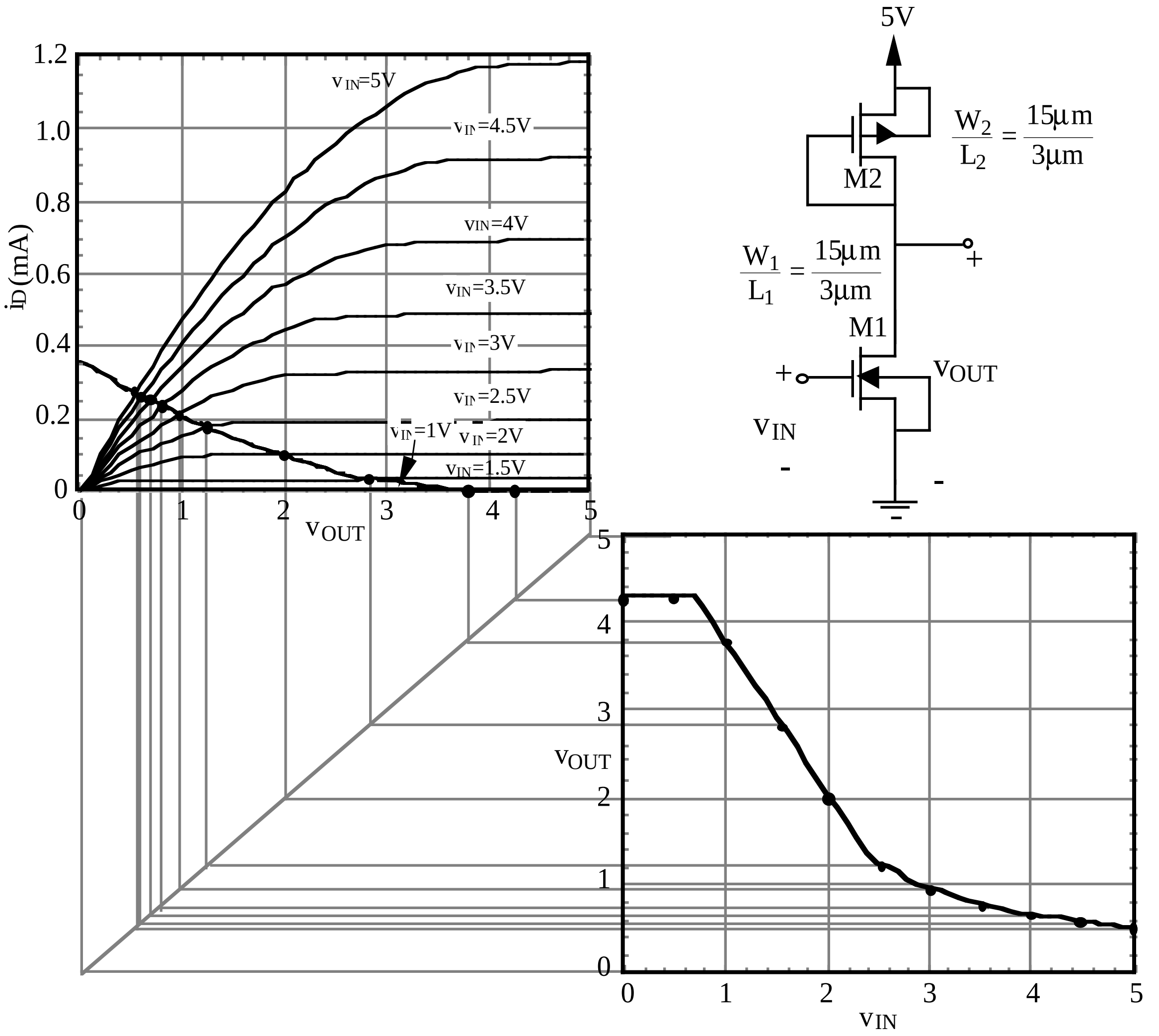
VI.1.1 - CMOS INVERTERS

Types



ACTIVE LOAD INVERTER - VOLTAGE TRANSFER CURVE

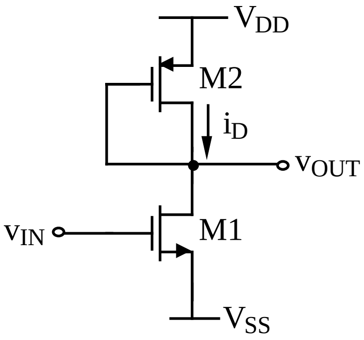
```
CMOS Active Load Inverter
VDD 3 0 DC 5.0
```



SPICE Input File:

```
VIN 1 0 DC 0.0
M1 2 1 0 0 MNMOS1 W=15U L=3U
M2 2 2 3 3 MPMOS1 W=15U L=3U
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U LAMBDA=0.01 GAMMA=0.8 PHI=0.6
.MODEL MPMOS1 PMOS VTO=-0.75 KP=8U LAMBDA=0.02 GAMMA=0.4 PHI=0.6
.DC VIN 0 5 0.1
.OP
.PRINT DC V(2)
.PROBE
.END
```

Active Load CMOS Inverter Output Swing Limits



Maximum:

$$v_{IN}=0 \;\Rightarrow\; i_D=0 \;\Rightarrow\; v_{SD2}=|V_{T2}|$$

$$\therefore \quad \boxed{v_{OUT}(\max) \approx V_{DD} - |V_{TP}|}$$

Minimum:

Assume $v_{IN} = V_{DD}$, M1 active, M2 saturated, and $V_{T1} = V_{T2} = V_T$.

M1: $$i_D = \beta 1\left[(v_{GS1}-V_T)v_{DS1}-\frac{v_{DS1}{}^2}{2}\right]$$

$$= \beta 1\left[(V_{DD}-V_{SS}-V_T)(v_{OUT}-V_{SS})-\frac{(v_{OUT}-V_{SS})^2}{2}\right]$$

M2: $$i_D = \frac{\beta_2}{2}(v_{GS}-V_T)^2 = \frac{\beta_2}{2}(V_{DD}-v_{OUT}-V_T)^2 = \frac{\beta_2}{2}(v_{OUT}+V_T-V_{DD})^2$$

$$i_D = \frac{\beta_2}{2}(v_{OUT}-V_{SS}+V_{SS}+V_T-V_{DD})^2$$

$$=\frac{\beta_2}{2}\left[(v_{OUT}-V_{SS})-(V_{DD}-V_{SS}-V_T)\right]^2$$

Define $v_{OUT}' = v_{OUT} - V_{SS}$ and $V_X = V_{DD} - V_{SS} - V_T$

$$\therefore \qquad i_D = \beta_1\left(V_X v_{OUT}' - \frac{(v_{OUT}')^2}{2}\right) \qquad \text{(M1)}$$

$$i_D = \frac{\beta_2}{2}\left(v_{OUT}' - V_X\right)^2 \qquad \text{(M2)}$$

Equate currents -

$$\frac{\beta_2}{2}\left(v_{OUT}'^2 - 2V_X v_{OUT}' + V_X{}^2\right) = \beta_1\left[V_X v_{OUT}' - \frac{v_{OUT}'^2}{2}\right]$$

or $$\frac{\beta_2}{\beta_1}\left(v_{OUT}'^2 - 2V_X v_{OUT}' + V_X{}^2\right) = 2V_X v_{OUT}' - v_{OUT}'^2$$

$$\left(1 + \frac{\beta_2}{\beta_1}\right) v_{OUT}'^2 - 2V_X\left(1 + \frac{\beta_2}{\beta_1}\right) v_{OUT}' + \frac{\beta_2}{\beta_1} V_X{}^2 = 0$$

$$v_{OUT}'^2 - 2V_X v_{OUT}' + \left(\frac{\beta_2/\beta_1}{1+\beta_2/\beta_1}\right) V_X{}^2 = 0$$

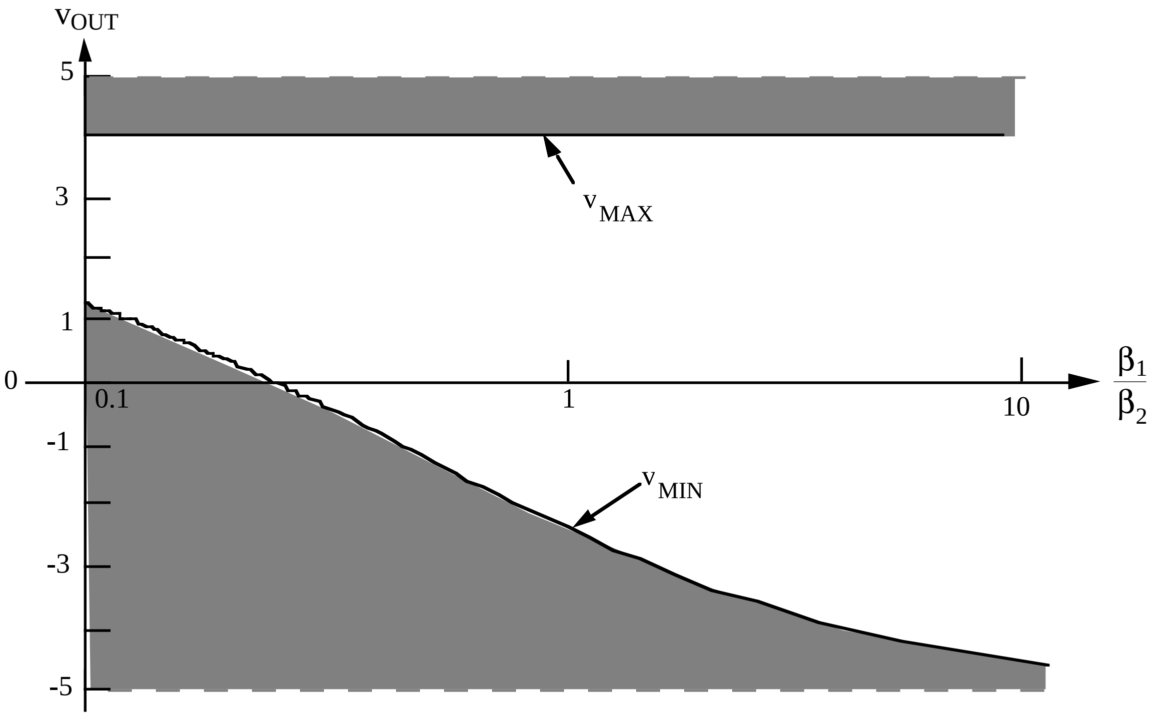
$$\therefore \qquad v_{OUT}' = V_X\left[1 \pm \sqrt{1 - \frac{\beta_2/\beta_1}{1+\beta_2/\beta_1}}\;\right] = V_X\left(1 - \frac{1}{\sqrt{1 + \beta_2/\beta_1}}\right)$$

$$\boxed{v_{OUT}(\text{min.}) = V_{DD} - V_T - \frac{V_{DD} - V_{SS} - V_T}{\sqrt{1 + \beta_2/\beta_1}}}$$

Interpretation of $v_{OUT(min.)}$

$$v_{OUT(min.)} = (V_{DD} - V_{SS} - V_T)\left[1 - \frac{1}{\sqrt{1 + \frac{\beta_2}{\beta_1}}}\right] + V_{SS}$$

$V_{DD} = -V_{SS} = 5V$
$V_T = 1V$

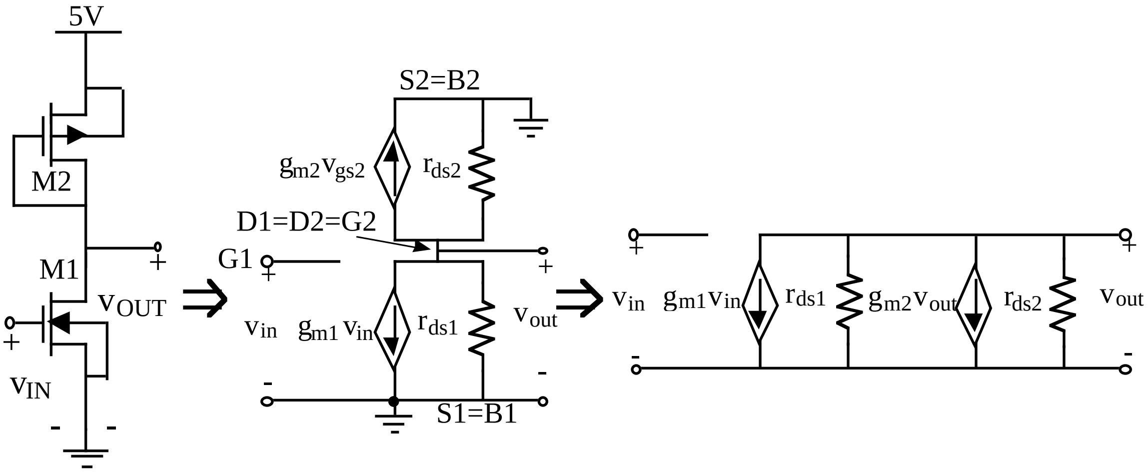


$$\text{Gain} \sim \sqrt{\frac{\beta_1}{\beta_2}}$$

Active Load Inverters

Small Signal Characteristics

Model:



Small Signal Voltage Gain

$$v_{out} = -\left(g_{m1}v_{in} + g_{m2}v_{out}\right)\left(r_{ds1} \,||\, r_{ds2}\right)$$

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \approx \frac{-g_{m1}}{g_{m2}} = -\sqrt{\frac{2K_N\left(\frac{W_1}{L_1}\right)I_1}{2K_P\left(\frac{W_2}{L_2}\right)I_2}} = -\sqrt{\frac{\beta_1}{\beta_2}}$$

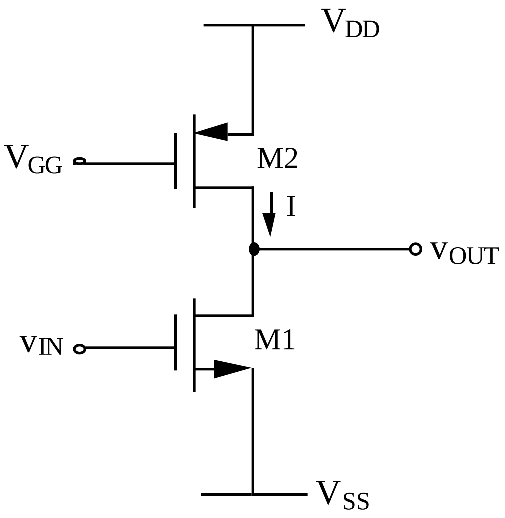
$$\frac{v_{out}}{v_{in}} = -\sqrt{\left(\frac{K_N'}{K_P'}\right)\left(\frac{W_1L_2}{W_2L_1}\right)} = -\sqrt{\left(\frac{\mu_{NO}}{\mu_{PO}}\right)\left(\frac{W_1L_2}{W_2L_1}\right)}$$

If $\frac{W_1/L_1}{W_2/L_2} = 20$, then $\frac{v_{out}}{v_{in}} = -6.67$ using the parameters of Table 3.1-2

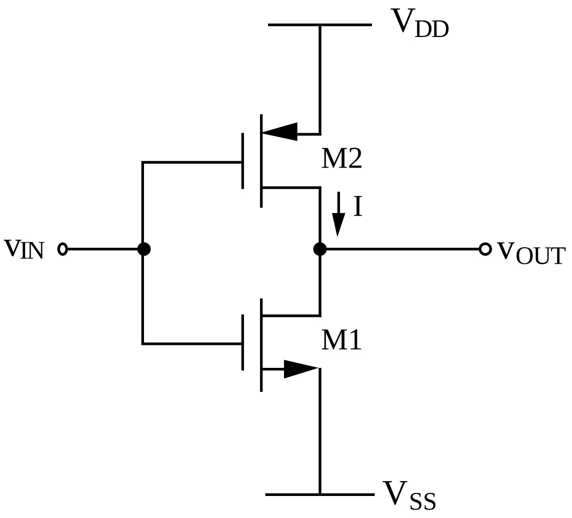
Small Signal Output Resistance

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \approx \frac{1}{g_{m2}}$$

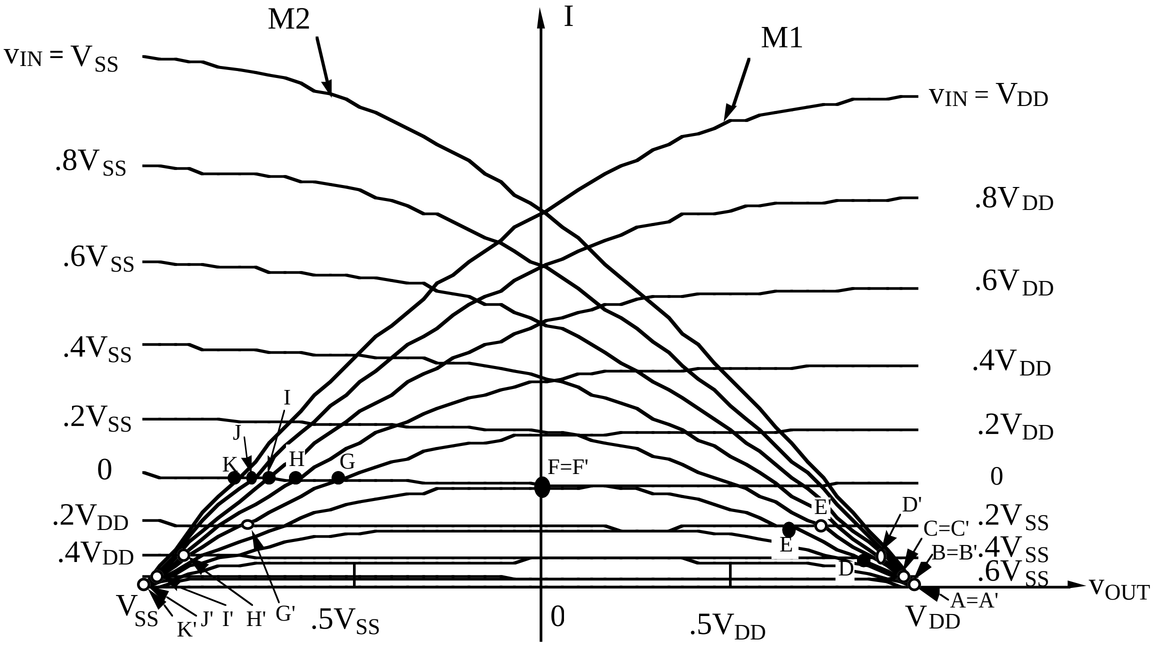
High Gain CMOS Inverters



Inverter with current source load



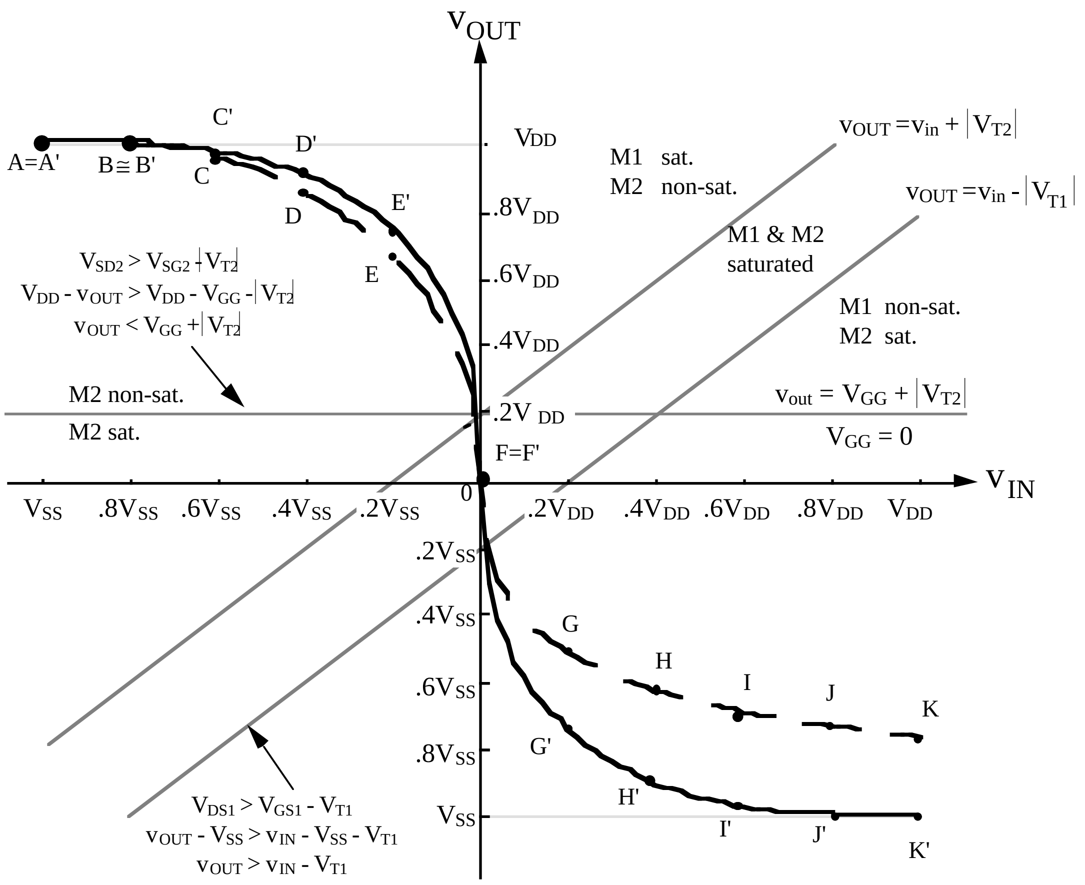
Push-pull, inverter



Large signal transfer characteristics of inverter with a current source and push pull inverter

High Gain, CMOS Inverter

Large Signal Transfer Characteristics

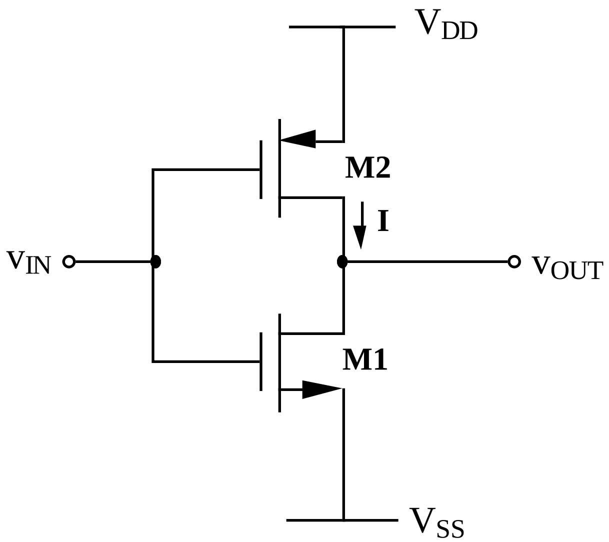


Advantages:

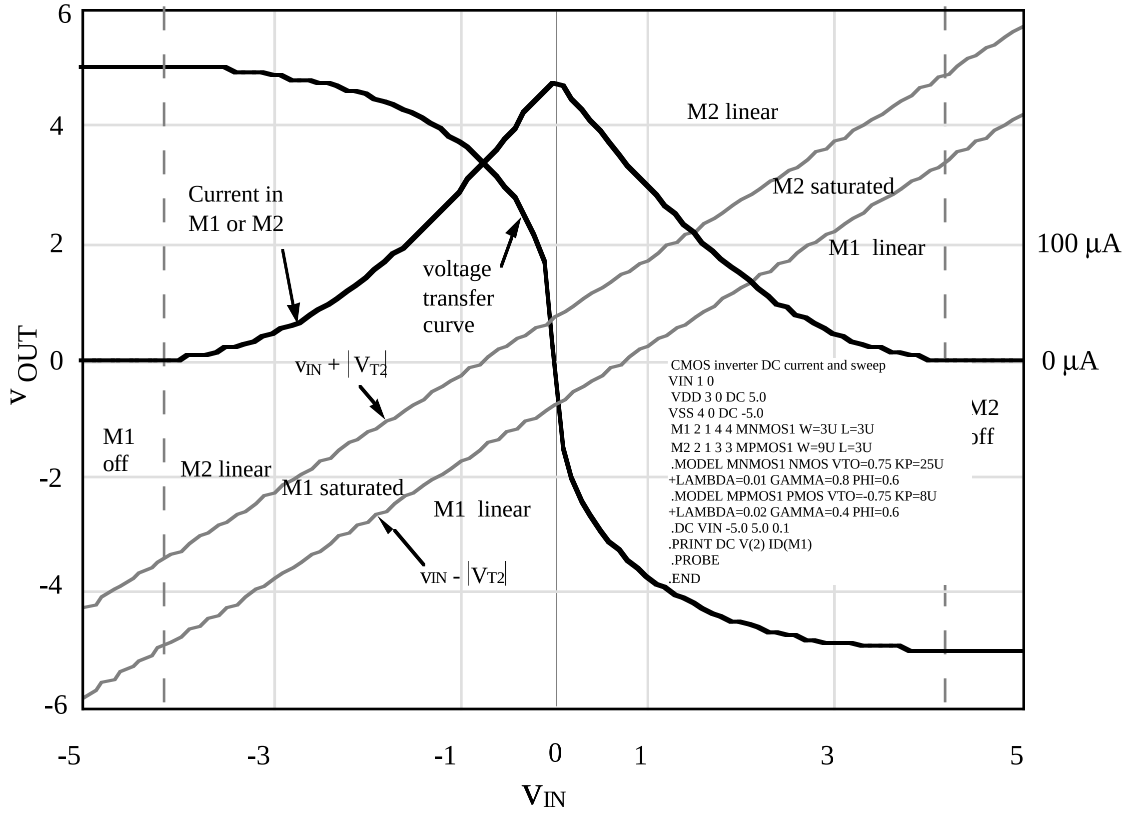
1. High gain.
2. Large output signal swing.
3. Large current sink and source capability in push pull inverter.

CMOS Inverter Characteristics

Circuit:

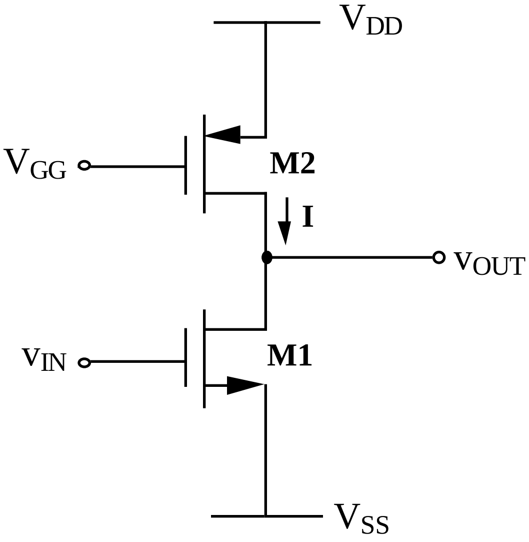


PSPICE Characteristics:



```
 CMOS inverter DC current and sweep
VIN 1 0
 VDD 3 0 DC 5.0
VSS 4 0 DC -5.0
 M1 2 1 4 4 MNMOS1 W=3U L=3U
 M2 2 1 3 3 MPMOS1 W=9U L=3U
 .MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
 .MODEL MPMOS1 PMOS VTO=-0.75 KP=8U
+LAMBDA=0.02 GAMMA=0.4 PHI=0.6
 .DC VIN -5.0 5.0 0.1
.PRINT DC V(2) ID(M1)
 .PROBE
.END
```

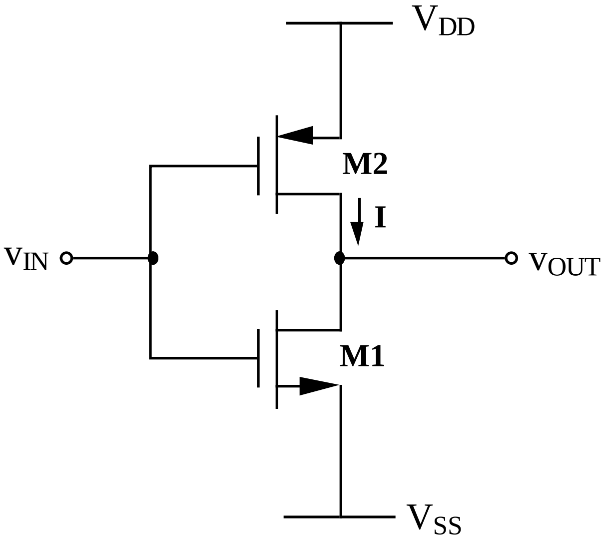
Current Source Inverter - Output Swing Limits



$$\boxed{v_{OUT(max.)} \approx V_{DD}}$$

$$\boxed{v_{OUT(min.)} = V_{DD}-V_{T1}-(V_{DD}-V_{SS}-V_{T1})\sqrt{1-\left(\frac{\beta_2}{\beta_1}\right)\left(\frac{V_{DD}-V_{GG}-V_{T2}}{V_{DD}-V_{SS}-V_{T1}}\right)}}$$

CMOS Push - Pull Inverter - Output Swing Limits



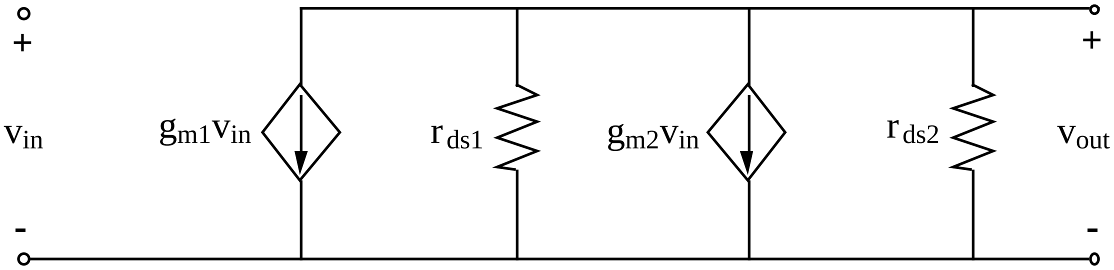
$$\boxed{v_{OUT(max.)} \approx V_{DD}}$$

$$\boxed{v_{OUT(min.)} \approx V_{SS}}$$

High Gain, CMOS Inverters

Small Signal Characteristics

Model



Small Signal Voltage Gain:

$$v_{OUT} = -\left(g_{m1}v_{in} + g_{m2}v_{in}\right)\left(r_{ds1} \,||\, r_{ds2}\right)$$

OR

$$\frac{v_{out}}{v_{in}} = \frac{-\left(g_{m1} + g_{m2}\right)}{\left(g_{ds1} + g_{ds2}\right)} = \frac{-\sqrt{\left(\frac{2}{I_D}\right)}\left[\sqrt{K_N'\frac{W_1}{L_1}} + \sqrt{K_P'\frac{W_2}{L_2}}\right]}{\lambda_1 + \lambda_2} = \frac{K}{\sqrt{I_D}} \quad !!!$$

Set $g_{m2} = 0$ for the current source inverter

Assume that $i_D = 1\ \mu A$ and $\frac{W_1}{L_1} = \frac{W_2}{L_2}$, using the values of Table 3.1-2 gives

$$\frac{v_{OUT}}{v_{in}} = -328 \qquad \text{for the push-pull inverter (L=10 } \mu\text{m)}$$

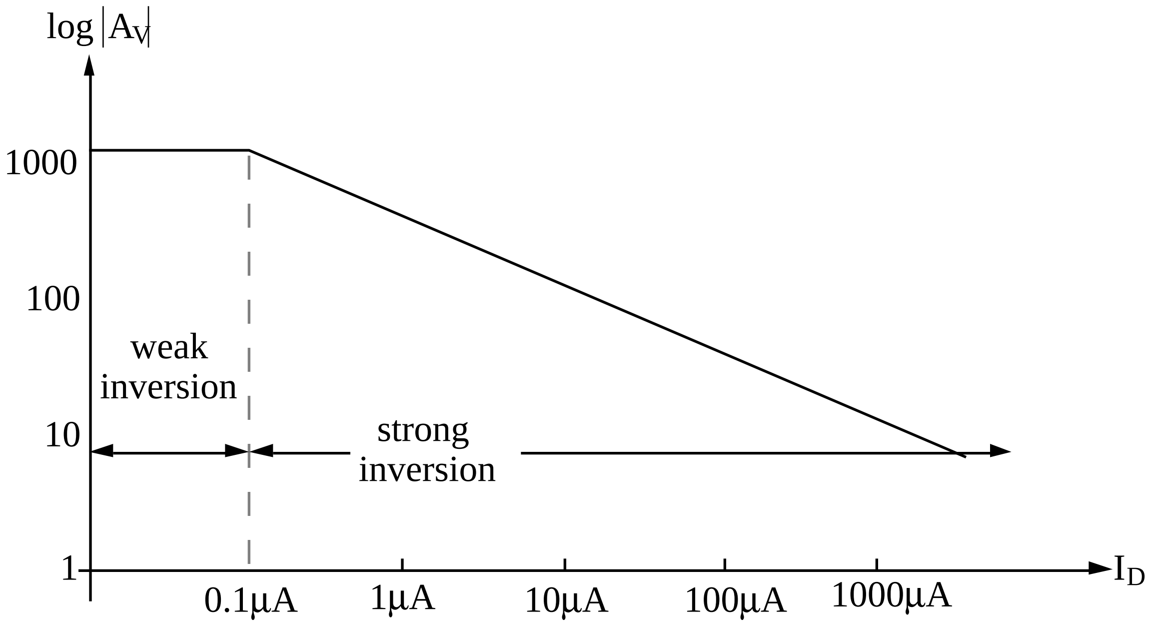
$$= -194 \qquad \text{for the current source inverter (L=10 } \mu\text{m)}$$

Small Signal Output Resistance:

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}}$$

High Gain, CMOS Inverters

Dependence of Gain upon Bias Current



Limit is the subthreshold current where square law characteristic turns into an exponential characteristic.

Assume that the level where subthreshold effects begin is approximately 0.1μA, the maximum gains of the CMOS inverters become:

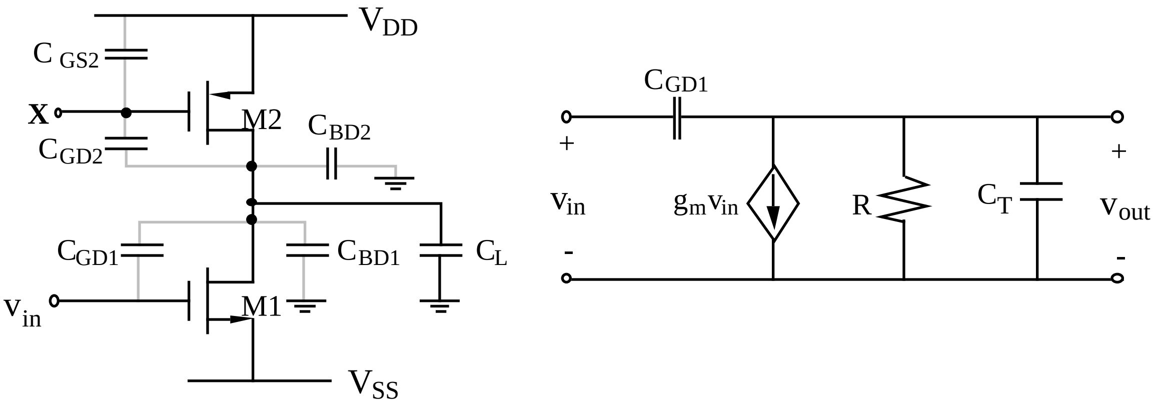
The CMOS inverters become:

$$\left.\begin{array}{lr} \text{Push-Pull:} & -1036 \\ \text{Current source load:} & -615 \\ \text{Current sink load:} & -422 \end{array}\right\} \frac{W}{L} = 1,\ L=10\ \mu\text{m}$$

Frequency Response of CMOS Inverters

General Configuration

X = v_{OUT} ;   Active Load CMOS Inverter ($g_m = g_{m1}$)
X = V_{GG} ;   CMOS Inverter with a Current Source Load ($g_m = g_{m1}$)
X = v_{IN} ;   CMOS Push Pull Inverter ($g_m = g_{m1} + g_{m2}$)



(a) (b)

(a) General configuration of an inverter illustrating parasitic capacitances.
(b) Small signal model of (a)

C_{GD1} and C_{GD2} are overlap capacitances
C_{BD1} and C_{BD2} are the bulk-drain capacitances
C_L is the load capacitance seen by the inverter

Frequency Response

$$\frac{v_{OUT}}{v_{IN}} = \frac{-g_m R \omega_1 (1 - s/z)}{\left(s + \omega_1\right)} , \qquad \omega_1 = \frac{1}{RC} \quad \text{and} \quad z = \frac{g_m}{C_{GD1}}$$

$$R = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \quad (g_{m2} = 0 \text{ for push pull and current source inverters})$$

$$C \approx C_{GD1} + C_{GS2} + C_{BD1} + C_{BD2} + C_L \text{ (Active load inverter)}$$

$$C \approx C_{GD1} + C_{GD2} + C_{BD1} + C_{BD2} + C_L \text{ (Current source \& push-pull inverter)}$$

if $g_m R >> 1$

Frequency Response of CMOS Inverters

Dependence of Frequency Response on Bias Current -

When $g_{m2} \neq 0$ (active load inverter):

$$R \approx \frac{1}{g_{m2}} \quad \text{or} \quad \omega_{-3dB} = \frac{\sqrt{2K'\frac{W}{L} I_D}}{C} \sim \sqrt{I_D}$$

When $g_{m2} = 0$ (push pull and current source inverter):

$$R = \frac{1}{(\lambda_1 + \lambda_2)\, I_D} \quad \text{or} \quad \omega_{-3dB} = \frac{(\lambda_1 + \lambda_2)\, I_D}{C} \sim I_D$$

Example:

Find the –3dB frequency for the CMOS inverter using a current source load and the CMOS push pull inverter assuming that $i_D = 1\mu A$, $C_{GD1}=C_{GD2}=0.2pF$ and $C_{BD1}=C_{BD2}=0.5pF$

Using the parameters of Table 3.1-2 and assuming that $\frac{W_1}{L_1} = \frac{W_2}{L_2} = 1$

Gives,

For the active load CMOS inverter,

$$\omega_{-3dB} = \frac{g_{m2}}{C} = 3.124\text{x}10^{-6} \text{ rads/sec or 512KHz}$$

For the push pull or current source CMOS inverter,

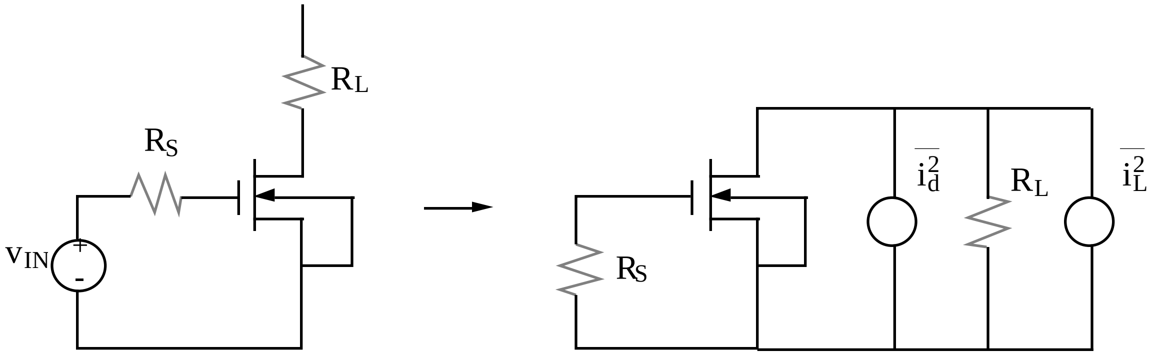
$$\omega_{-3dB} = \frac{g_{gd1} + g_{ds2}}{C} = 14.3\text{x}10^{3} \text{ rads/sec or 2.27 KHz}$$

$$z = \frac{g_{m1}}{C_{GD1}} = 29.155 \text{ Mrads/sec or 4.64 MHz}$$

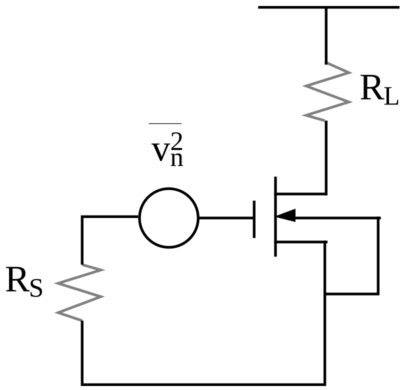
The reason for the difference is the higher output resistance of the push pull or current source CMOS inverters

NOISE IN MOS INVERTERS

Noise Calculation



We wish to determine the equivalent input noise voltage, $\overline{v_n^2}$ as shown below:



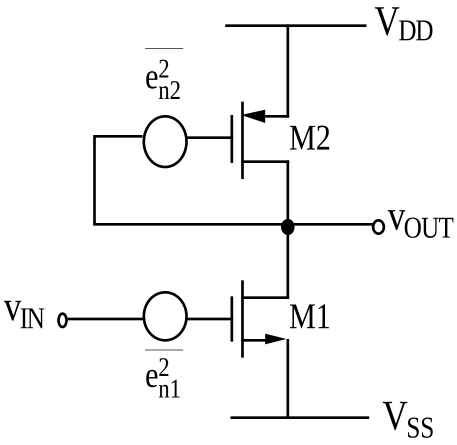
$$\overline{i_d^2} = \frac{8}{3}KTg_m \quad (A^2/Hz)$$

$$\overline{i_L^2} = \frac{4KT}{R_L} \quad (A^2/Hz)$$

Comments:

1.) 1/f noise has been ignored.
2.) Resistors are noise-free, they are used to show topological aspects. Can repeat the noise analysis for the resistors if desired.

Noise in an Active Load Inverter



$$\overline{e_{out}^2}\Big|_{v_{IN}=0} = \overline{e_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{e_{n2}^2}$$

$$\overline{e_{eq}^2} = \frac{\overline{e_{out}^2}}{\left(\frac{g_{m1}}{g_{m2}}\right)^2} = \overline{e_{n1}^2} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \overline{e_{n2}^2}$$

$$\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2\left(\frac{\overline{e_{n2}^2}}{\overline{e_{n1}^2}}\right)\right]$$

Sec 3.2, Eq (15)

1/f noise: $\overline{e_n^2} = \frac{B}{fWL}$; B=constant for a process

Sec. 3.3, Eq (6)

$$g_m = \sqrt{\frac{2K'\,W}{L}I_D}$$

So $$\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[1 + \frac{\left(2K_P'\left(\frac{W_2}{L_2}I_D\right)\right)}{\left(2K_N'\left(\frac{W_1}{L_1}I_D\right)\right)}\left(\frac{B_P}{fW_2L_2}\right)\left(\frac{fW_1L_1}{B_N}\right)\right]$$

$$\boxed{\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[1 + \left(\frac{K_P'B_P}{K_N'B_N}\right)\left(\frac{L_1}{L_2}\right)^2\right]}$$

To minimize 1/f noise -

1). $L_2 \gg L_1$ -----> Gain = $-\sqrt{\frac{K_N'W_1}{K_P'W_2}}\sqrt{\frac{L_2}{L_1}}$

2). $\overline{e_{n1}^2}$ small

Noise in An Active Load Inverter - (Cont'd)

Suppose the noise is thermal - Sec. 3.2, Eq,(13)

$$\overline{e_n^2} = \frac{8kT(1+\eta)}{3g_m}$$

$$\overline{e_{eq}^2} = \frac{8kT(1+\eta_1)}{3g_{m1}}\left[1 + \left(\frac{g_{m2}{}^2}{g_{m1}{}^2}\right)\left(\frac{(1+\eta_2)g_{m1}}{(1+\eta_1)g_{m2}}\right)\right]$$

$$\boxed{\overline{e_{eq}^2} = \frac{8kT(1+\eta_1)}{3g_{m1}}\left[1 + \frac{(1+\eta_2)}{(1+\eta_1)}\left(\frac{K_P'\frac{W_2}{L_2}}{K_N'\frac{W_1}{L_1}}\right)^{1/2}\right]}$$

or

$$\boxed{\overline{e_{eq}^2} = \frac{8kT(1+\eta_1)}{3g_{m1}}\left[1 + \left(\frac{1+\eta_2}{1+\eta_1}\right)\left(\frac{g_{m2}}{g_{m1}}\right)\right]}$$

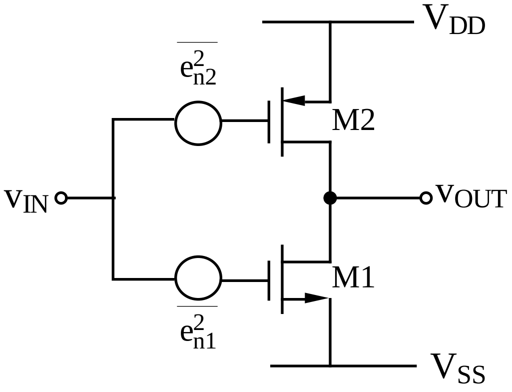
To minimize thermal noise -

1. Maximize gain $\left(\frac{g_{m1}}{g_{m2}}\right)$
2. Increase $g_{m1} = \sqrt{\frac{2K_N W_1}{L_1} I_D}$

Noise in Other Types of Inverters

Current Source Load Inverter -> same as active load inverter

Push-Pull Inverter-



$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}}$$

$$\overline{e_{out}^2} = (g_{m1}r_{out})^2\,\overline{e_{n1}^2} + (g_{m2}r_{out})^2\,\overline{e_{n2}^2}$$

$$v_{out} = -(g_{m1} + g_{m2})r_{out}v_{in}$$

$$\overline{e_{eq}^2} = \left(\frac{g_{m1}}{g_{m1} + g_{m2}}\right)^2 \overline{e_{n1}^2} + \left(\frac{g_{m2}}{g_{m1} + g_{m2}}\right)^2 \overline{e_{n2}^2}$$

$$\overline{e_{eq}^2} = \overline{e_{n1}^2}\left[\frac{1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \frac{\overline{e_{n2}^2}}{\overline{e_{n1}^2}}}{\left(1 + \frac{g_{m2}}{g_{m1}}\right)^2}\right] = \overline{e_{n1}^2}\left[\frac{1 + \left(\frac{K'_P B_P}{K'_N B_N}\right)\left(\frac{L_1}{L_2}\right)^2}{\left(1 + \frac{K'_P W_2 L_1}{K'_N W_1 L_2}\right)^2}\right]$$

To minimize noise - Reduce $\overline{e_{n1}^2}$ and $\overline{e_{n2}^2}$.

SUMMARY OF MOS INVERTERS

Inverter Type	AC Voltage Gain	AC Output Resistance	Bandwidth (C_{GB}=0)	Equivalent, input-referred,mean-square noise voltage
p-channel active load sinking inverter	$\frac{-g_{m1}}{g_{m2}}$	$\frac{1}{g_{m2}}$	$\frac{g_{m2}}{C_{BD1}+C_{GS1}+C_{GS2}+C_{BD2}}$	$\overline{v_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2+\overline{v_{n2}^2}$
n-channel active load sinking inverter	$\frac{-g_{m1}}{g_{m2+gmb2}}$	$\frac{1}{g_{m2}+g_{mb2}}$	$\frac{g_{m2}+g_{mb2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\overline{v_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2+\overline{v_{n2}^2}$
Current source load sinking inverter	$\frac{-g_{m1}}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\overline{v_{n1}^2}\left(\frac{g_{m1}}{g_{m2}}\right)^2+\overline{v_{n2}^2}$
Push-Pull inverter	$\frac{-(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_{BD1}+C_{GD1}+C_{GS2}+C_{BD2}}$	$\left(\frac{\overline{v_{n1}^2}g_{m1}}{g_{m1}+g_{m2}}\right)^2+\left(\frac{\overline{v_{n2}^2}g_{m2}}{g_{m1}+g_{m2}}\right)^2$

KEY MOSFET RELATIONSHIP USEFUL FOR DESIGN

Assume MOSFET is in saturation.

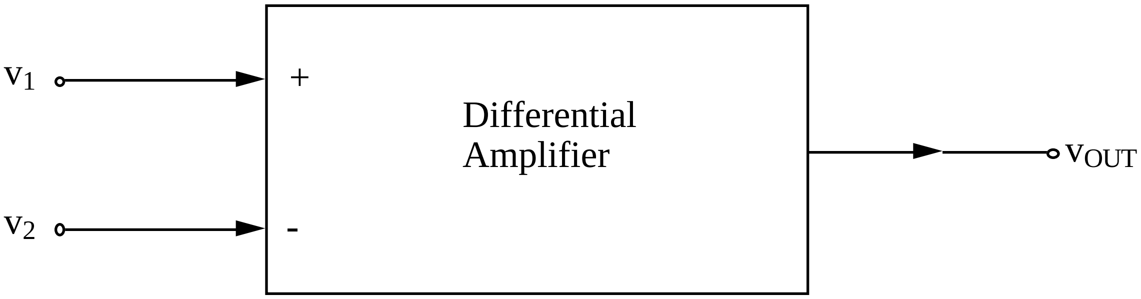
1.) $i_D = \frac{KW}{2L}(v_{GS} - V_T)^2$ or $v_{GS} = \sqrt{\frac{2i_D}{KW/L}} - V_T$

2.) $v_{DS}(\text{sat}) = \sqrt{\frac{2i_D}{KW/L}}$ or $i_D(\text{sat}) = \frac{KW}{2L}\, v_{DS}(\text{sat})^2$

3.) $g_m = \sqrt{\frac{2I_D KW}{L}}$ or $g_m = \frac{KW}{L}(V_{GS} - V_T)$

VI.2 - DIFFERENTIAL AMPLIFIERS

Definition of a Differential Amplifier

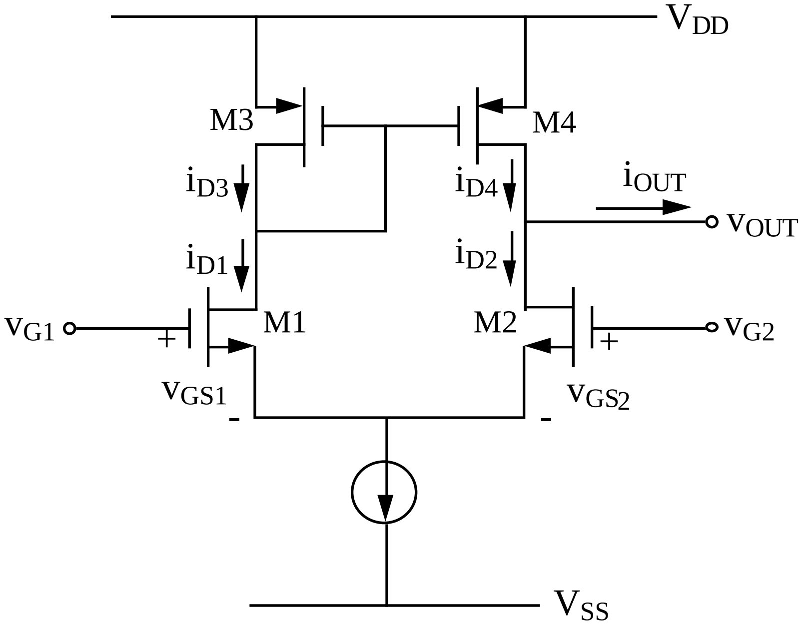


$$v_{OUT} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)$$

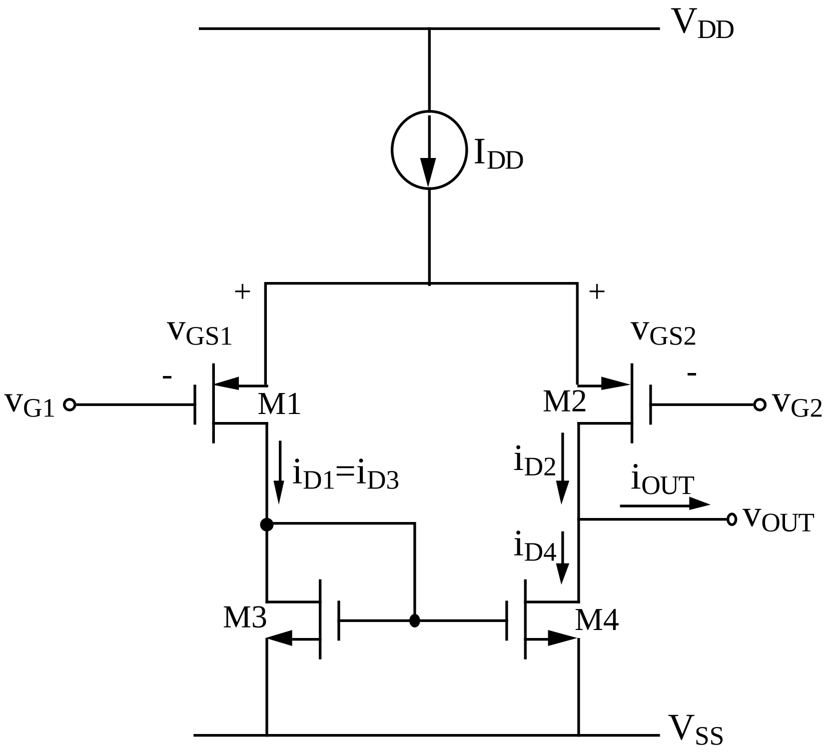
Differential voltage gain = A_{VD}	(100)
Common mode voltage gain = A_{VC}	(1)
Common mode rejection ratio = $\frac{A_{VD}}{A_{VC}}$	(1000)
Input offset voltage = $V_{OS}(in) = \frac{V_{OS}(out)}{A_{VD}}$	(2-10mV)
Common mode input range = V_{ICMR}	($V_{SS}+2V<V_{ICMR}<V_{DD}-2V$)
Power supply rejection ratio	(PSRR)
Noise	

VI.2-1 - CMOS DIFFERENTIAL AMPLIFIERS

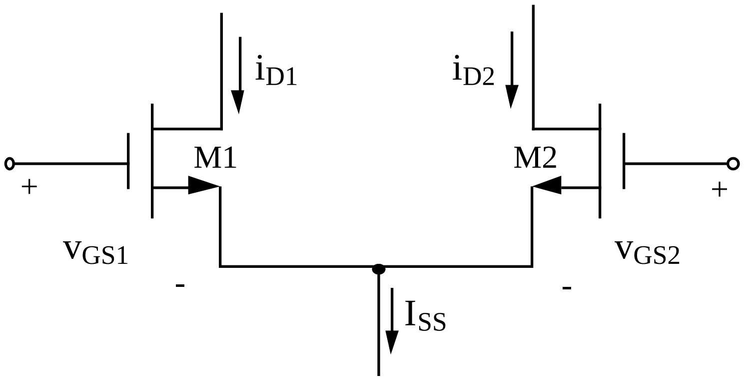
N-Channel Input Pair Differential Amplifier



P-Channel Input Pair Differential Amplifier



Large Signal Analysis of CMOS Differential Amplifiers



$$(1).\quad v_{ID} = v_{GS1} - v_{GS2} = \sqrt{\frac{2i_{D1}}{\beta}} - \sqrt{\frac{2i_{D2}}{\beta}}$$

$$(2).\quad I_{SS} = i_{D1} + i_{D2}$$

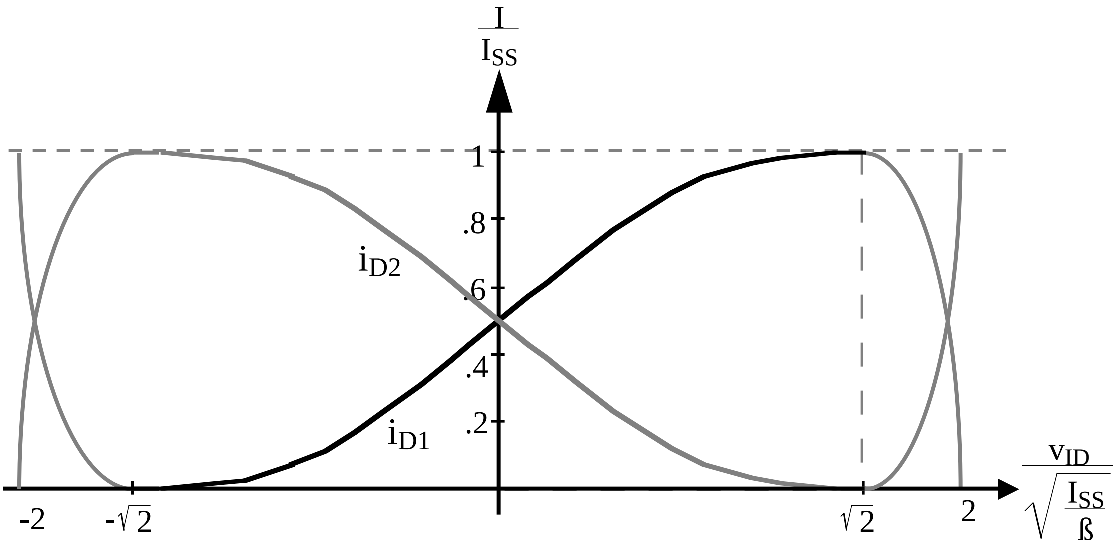
Solving for i_{D1} and i_{D2} gives,

$$(3).\quad i_{D1} = \left(\frac{I_{SS}}{2}\right) + \left(\frac{I_{SS}}{2}\right) v_{ID} \sqrt{\frac{\beta}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}}$$

And

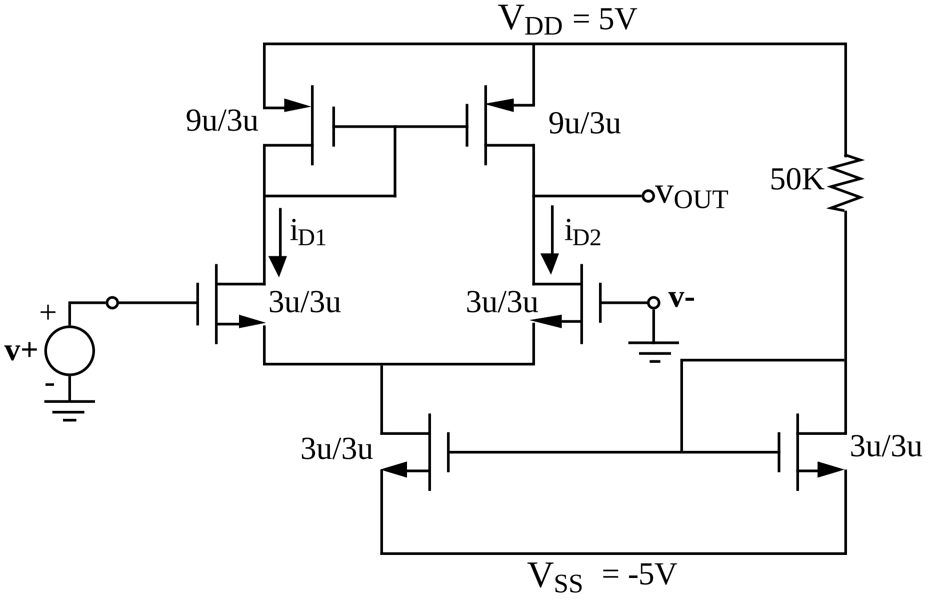
$$(4).\quad i_{D2} = \left(\frac{I_{SS}}{2}\right) - \left(\frac{I_{SS}}{2}\right) v_{ID} \sqrt{\frac{\beta}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}}$$

Where $v_{ID} < 2\sqrt{\frac{I_{SS}}{\beta}}$ $\qquad g_m = \frac{\partial i_{D1}}{\partial v_{ID}} = \sqrt{\frac{\beta I_{SS}}{4}}$

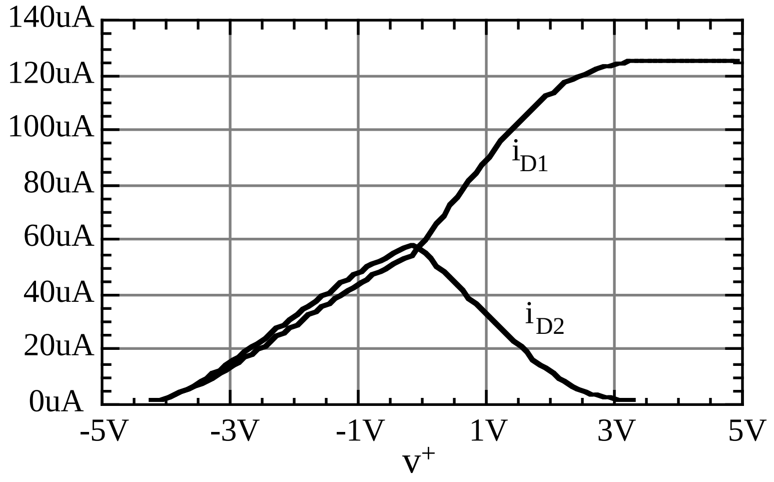


Transconductance Characteristics of the Differential Amplifier

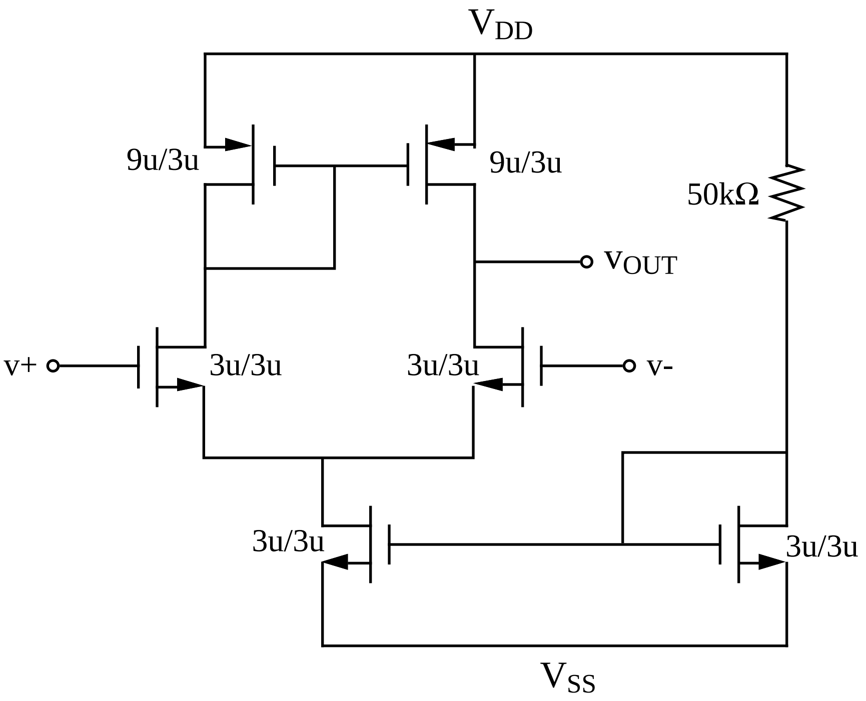
Circuit

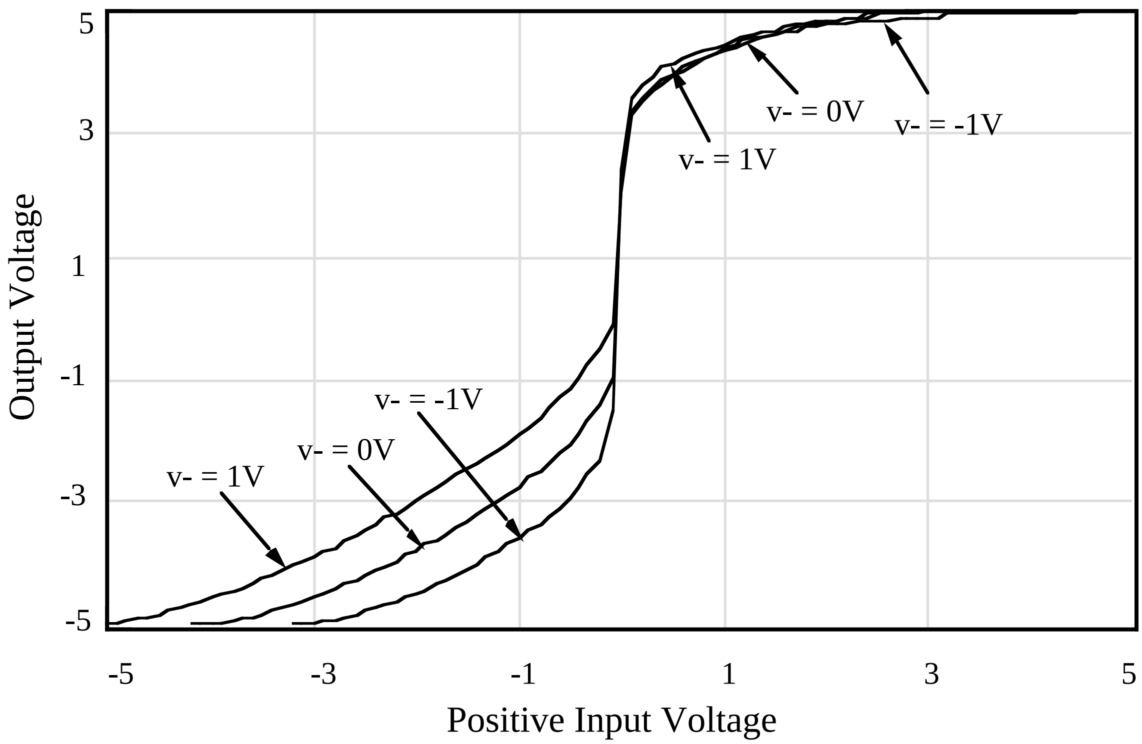


Simulation Results

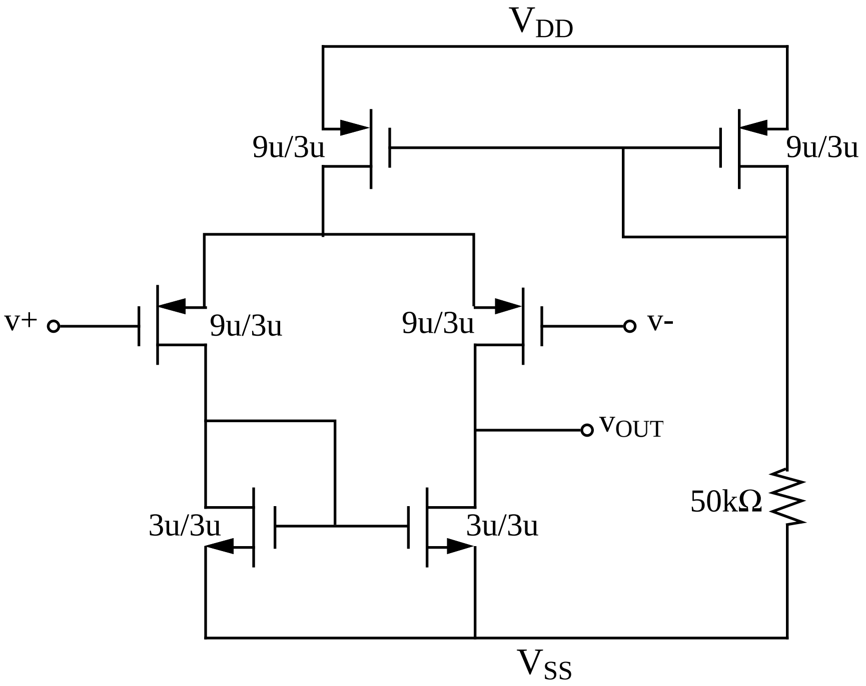


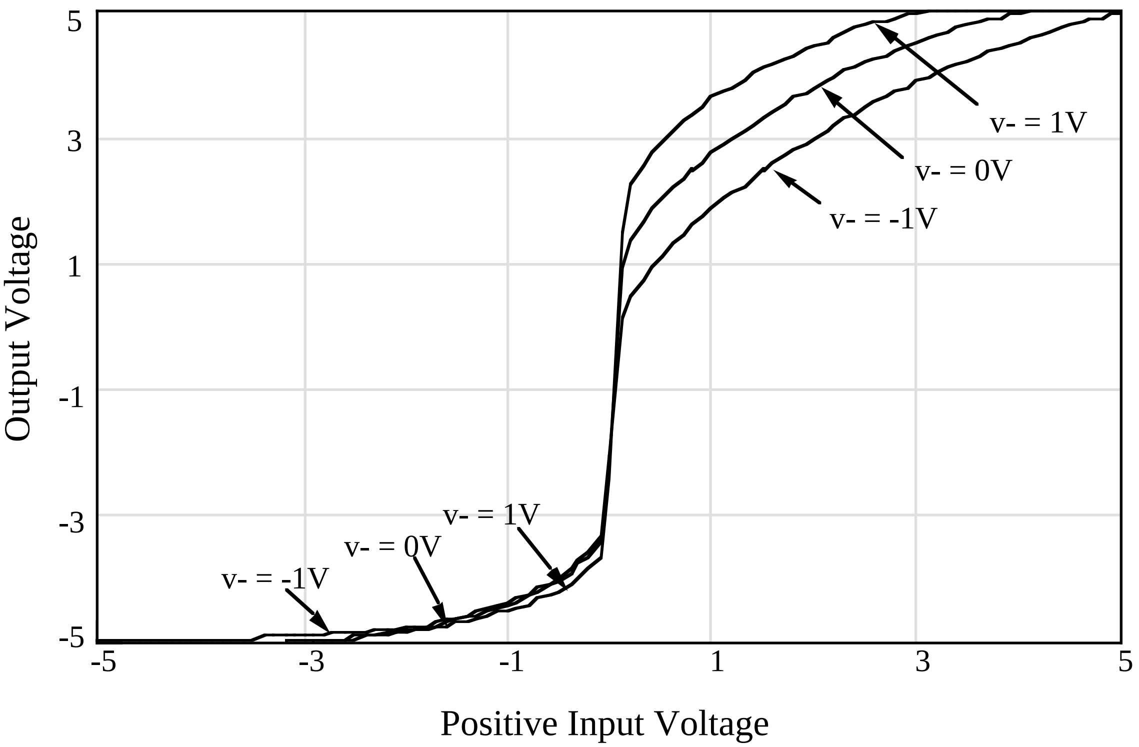
Voltage Transfer Curve of n-channel Differential Amplifier





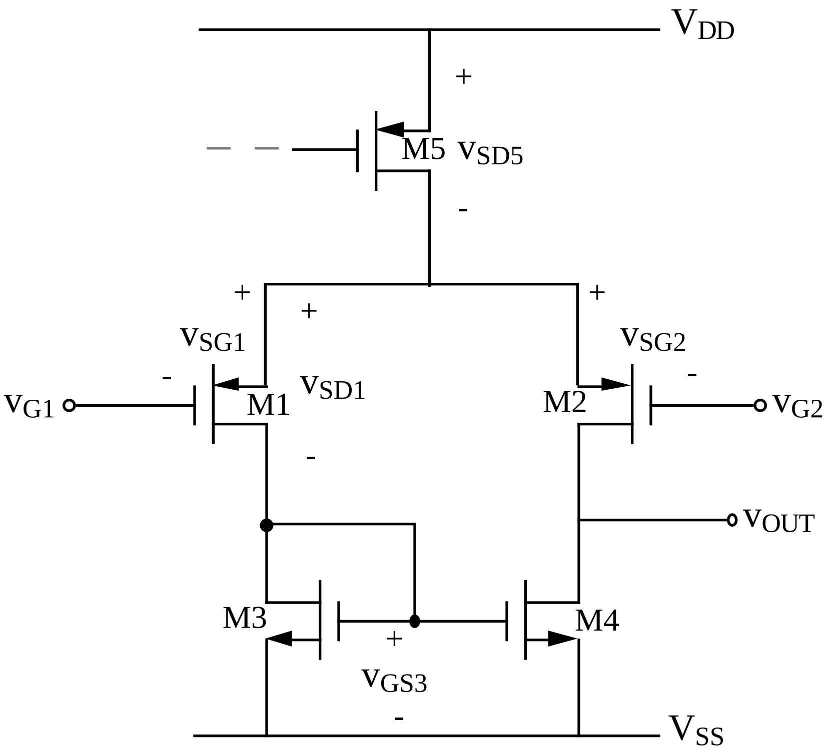
Voltage Transfer Curve for a p-channel Differential Amplifier





COMMON MODE INPUT RANGE

P-Channel Input Pair Differential Amplifier



Lowest common mode input voltage at gate of M1(M2)

$v_{G1(min)} = V_{SS} + v_{GS3} + v_{SD1} - v_{SG1}$

for saturation, the minimum value of $v_{SD1} = v_{SG1} - |V_{T1}|$

Therefore, $v_{G1(min)} = V_{SS} + v_{GS3} - |V_{T1}|$

or, $v_{G1(min)} = V_{SS} + \sqrt{\frac{I_{SS}}{\beta}} + V_{TO3} - |V_{T1}|$

$v_{G1(max)} = V_{DD} - v_{SD5} - v_{SG1} = V_{DD} - v_{SD5} - \sqrt{\frac{2I_{D1}}{\beta_1}} - |V_{T1}|$

COMMON MODE RANGE-CONT'D

Example

Assume that V_{DD} varies from 8 to 12 volts and that $V_{SS} = 0$. Using the values of Table 3.1-2, find the common mode range for worst case conditions. Assume that $I_{SS} = 100\mu A$, $W_1/L_1 = W_2/L_2 = 5$, $W_3/L_3 = W_4/L_4 = 1$, and $v_{SD5} = 0.2V$. Include the worst case value of K' in the calculations.

If V_{DD} varies 10 ± 2V, then we get

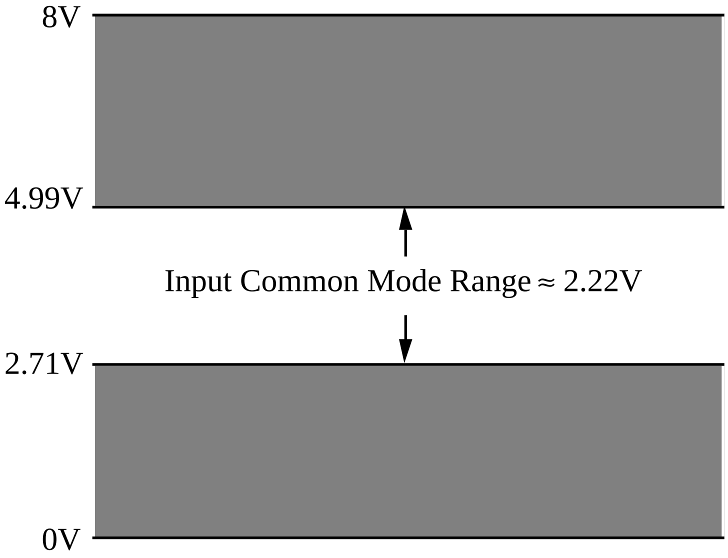
$$v_{G1(max)} = V_{DD} - v_{SD5} - \sqrt{\frac{I_{SS}}{\beta_1}} - |V_{T1}|$$

$$= 8 - 0.2 - \sqrt{\frac{100}{5x7.2}} - 1.2 = 6.6 - 1.67 = 4.99V$$

$$v_{G1(min)} = V_{SS} + \sqrt{\frac{I_{SS}}{\beta_3}} + V_{TO3} - |V_{T1}|$$

$$= 0 + \sqrt{\frac{100}{1x18.7}} + 1.2 - 0.8 = 0.4 + 2.31 = 2.71V$$

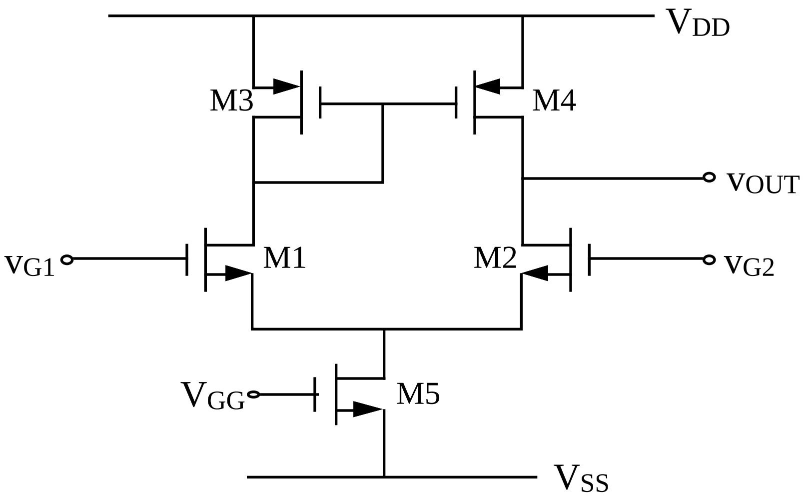
Therefore, the input common mode range of the p-channel input differential amplifier is from 2.71V to 4.99V


8V
4.99V
Input Common Mode Range ≈ 2.22V
2.71V
0V

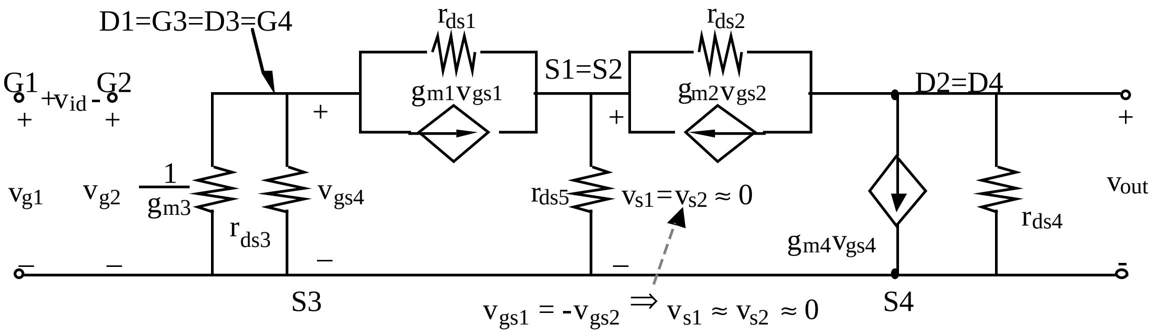
CMOS DIFFERENTIAL AMPLIFIER

Small Signal Differential Mode Gain

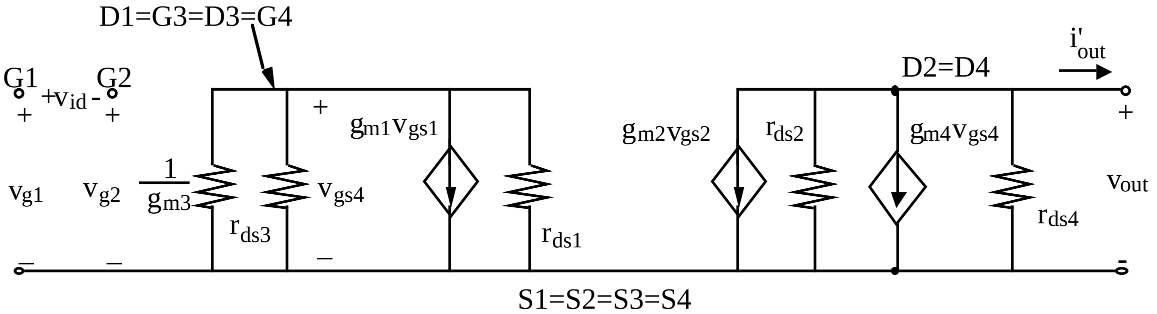
N-Channel input differential amplifier -



Exact small signal model -



Simplified small signal model using symmetry -



$v_{gs1} = 0.5v_{id}$ and $v_{gs2} = -0.5v_{id}$

CMOS DIFFERENTIAL AMPLIFIER

Unloaded Differential Transconductance Gain

$(R_L = 0)$

$$i_{out}' = -g_{m4}v_{gs4} - g_{m2}v_{gs2} = \frac{g_{m1}g_{m4}(r_{ds1} \parallel r_{ds3})}{1 + g_{m3}(r_{ds1} \parallel r_{ds3})} v_{gs1} - g_{m2}v_{gs2}$$

If $g_{m3}(r_{ds1} \parallel r_{ds3}) >> 1$, $g_{m3} = g_{m4}$, and $g_{m1} = g_{m2} = g_{md}$, then

$$i_{out}' \approx g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}(v_{gs1} - v_{gs2}) = g_{md}v_{id}$$

or

$$\boxed{i_{out}' \approx g_{md}v_{id} = \sqrt{\frac{K_N'WI_{SS}}{L}}\, v_{id}}$$

Unloaded Differential Voltage Gain

$(R_L = \infty)$

$$\boxed{v_{out} \approx \frac{g_{md}}{g_{ds2} + g_{ds4}} v_{id} = \frac{2}{(\lambda_N + \lambda_P)}\sqrt{\frac{K_N'W}{I_{SS}L}}\, v_{id}}$$

Example

If all W/L ratios are 3µm/3µm and I_{SS} = 10µA, then

$$g_{md}(\text{N-channel}) = \sqrt{(17\text{x}10^{-6})(10\text{x}10^{-6})} = 13\ \mu\text{A/V}$$

$$g_{md}(\text{P-channel}) = \sqrt{(8\text{x}10^{-6})(10\text{x}10^{-6})} = 8.9\ \mu\text{A/V}$$

and

$$\frac{v_{out}}{v_{id}}(\text{N-channel}) = \frac{2(13\text{x}10^{-6})}{(0.01+0.02)10\text{x}10^{-6}} = 86.67$$

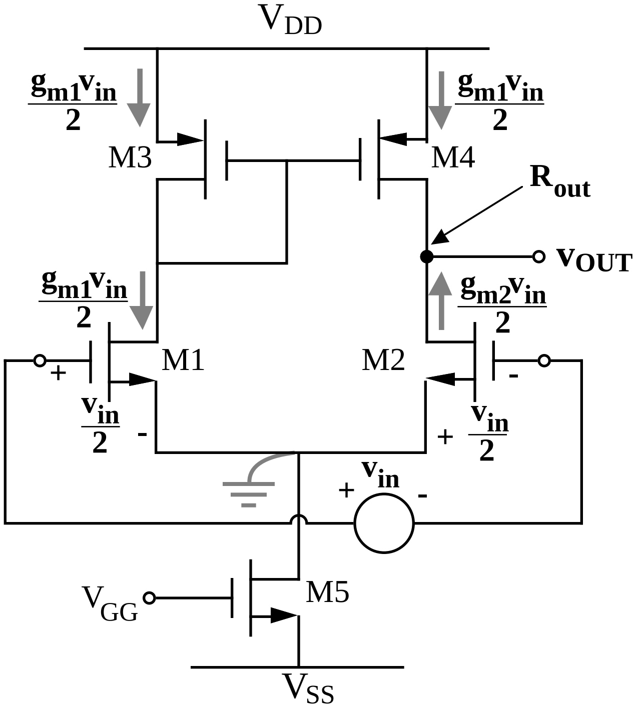
$$\frac{v_{out}}{v_{id}}(\text{P-channel}) = \frac{2(8.9\text{x}10^{-6})}{(0.01+0.02)10\text{x}10^{-6}} = 59.33$$

INTUITIVE SMALL SIGNAL ANALYSIS OF MOSFET CIRCUITS

Principle: Consider only small changes superimposed on the dc conditions.

Technique: Identify the transistor(s) that convert input voltage to current (these transistors are called the active devices). Trace the currents to where they flow into the resistance seen from a given node and multiply this resistance times the currents to find the voltage at this node.

Example - Differential Amplifier



Current flowing into the output node (drains of M2 and M4) is

$$i_{out} = \frac{g_{m1}v_{in}}{2} + \frac{g_{m2}v_{in}}{2}$$

Output resistance, R_{out}, seen at this node is

$$R_{out} = r_{ds2}||r_{ds4} = \frac{1}{g_{ds2}+g_{ds4}}$$

Therefore, the open circuit voltage gain is

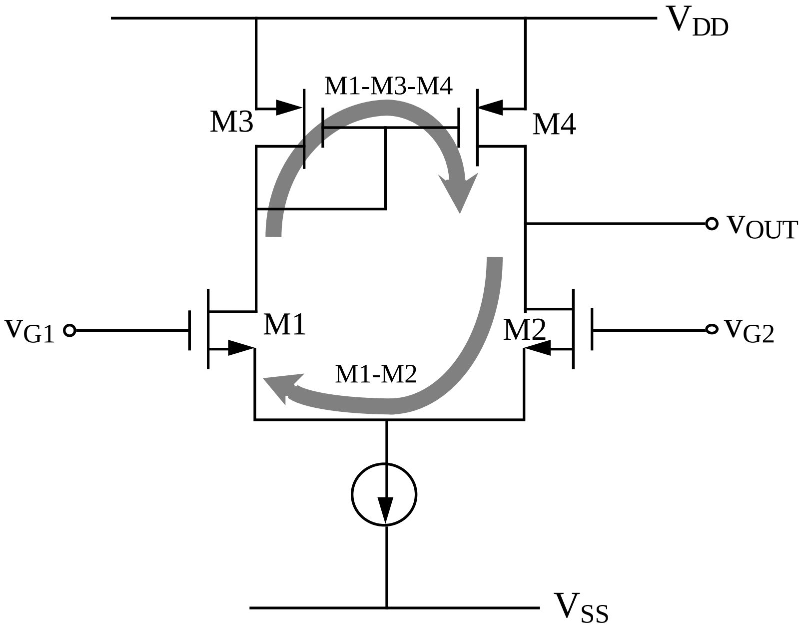
$$\boxed{\frac{v_{out}}{v_{in}} = \frac{g_{m1}+g_{m2}}{2(g_{ds2}+g_{ds4})} = \frac{g_{m1}}{g_{ds2}+g_{ds4}} = \frac{g_{m2}}{g_{ds2}+g_{ds4}}}$$

CMOS DIFFERENTIAL AMPLIFIER

Common Mode Gain

The differential amplifier that uses a current mirror load should theoretically have zero common mode gain.

For example:

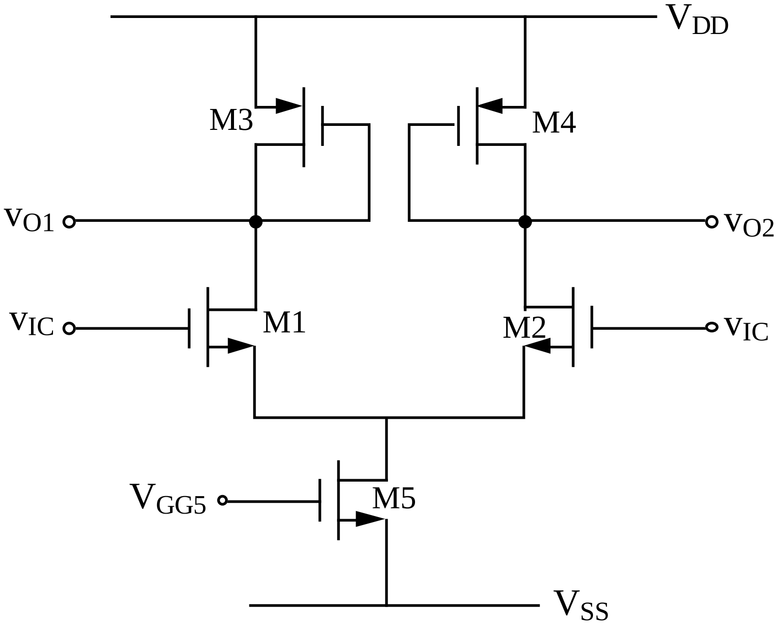


$$\begin{bmatrix}\text{Total Common}\\ \text{mode output}\\ \text{due to } v_{IC}\end{bmatrix} = \begin{bmatrix}\text{Common mode}\\ \text{output due to}\\ \text{M1-M3-M4 path}\end{bmatrix} - \begin{bmatrix}\text{Common mode}\\ \text{output due to}\\ \text{M1–M2 path}\end{bmatrix}$$

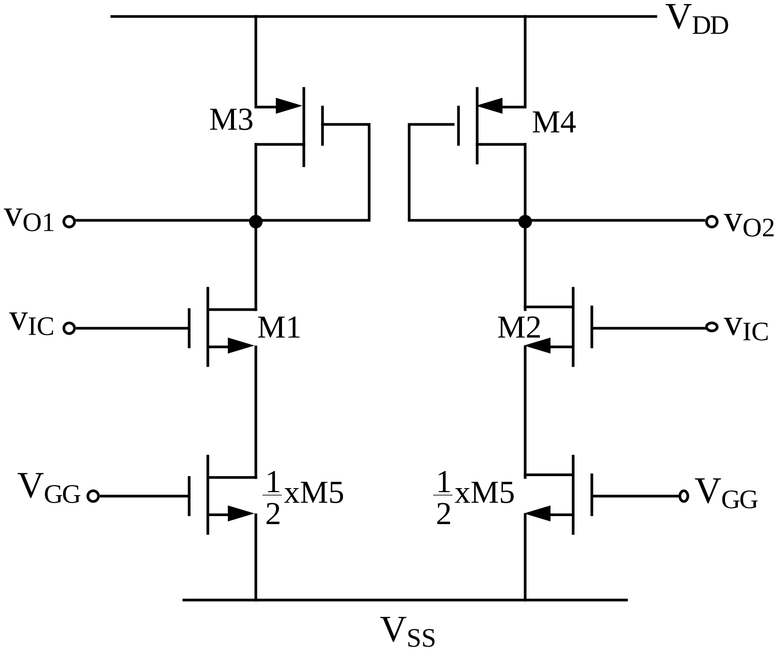
Therefore, the common mode gain will approach zero and is nonzero because of mismatches in the gain between the two paths.

CMOS DIFFERENTIAL AMPLIFIER

Consider the following differential amplifier -

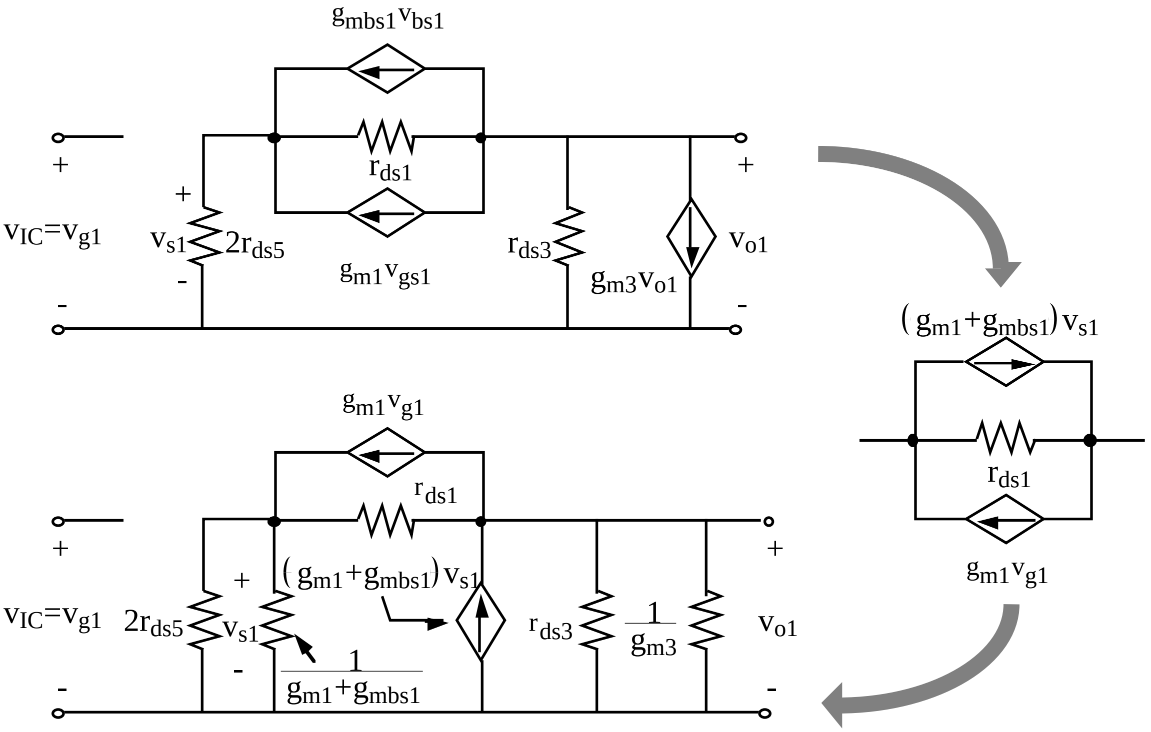


Use of symmetry to simplify gain calculations -



CMOS DIFFERENTIAL AMPLIFIER

Small signal model -



Writing nodal equations -

$$\left[0.5g_{ds} + g_{ds1} + g_{mbs1}\right] v_{s1} - \left[g_{ds1}\right] v_{o1} = g_{m1}v_{IC}$$

$$-\left[g_{ds1} + g_{m1} + g_{mbs1}\right] v_{o1} + \left[g_{ds1} + g_{ds3} + g_{m3}\right] v_{o1} = -g_{m1}v_{IC}$$

Solving for $\dfrac{v_{o1}}{v_{IC}}$ gives,

$$\frac{v_{o1}}{v_{IC}} = \frac{-0.5g_{m1}g_{ds5}}{\left(g_{ds3}+g_{m3}\right)\left[0.5g_{ds} + g_{m1} + g_{mbs1} + g_{ds1}\right] + 0.5g_{ds1}g_{ds5}}$$

or

$$\frac{v_{o1}}{v_{IC}} \approx \frac{-0.5g_{m1}g_{ds5}}{g_{m3}\left(g_{m1} + g_{mbs1}\right)} \approx \frac{-g_{ds5}}{2g_{m3}}$$

COMMON MODE REJECTION RATIO (CMRR)

$$\text{CMRR} = \frac{\text{Differential mode gain}}{\text{Common mode gain}} = \frac{A_{vd}}{A_{vc}}$$

For the previous example,

$$|\text{CMRR}| = \frac{\left(\dfrac{g_{m1}}{g_{m3}}\right)}{\left(\dfrac{g_{m1}g_{ds5}}{2g_{m3}\left(g_{m1} + g_{mbs1}\right)}\right)} = \frac{2(g_{m1} + g_{mbs1})}{g_{ds5}} \approx \frac{2g_{m1}}{g_{ds5}}$$

Therefore, current sinks/sources with a larger output resistance(r_{ds5}) will increase the CMRR.

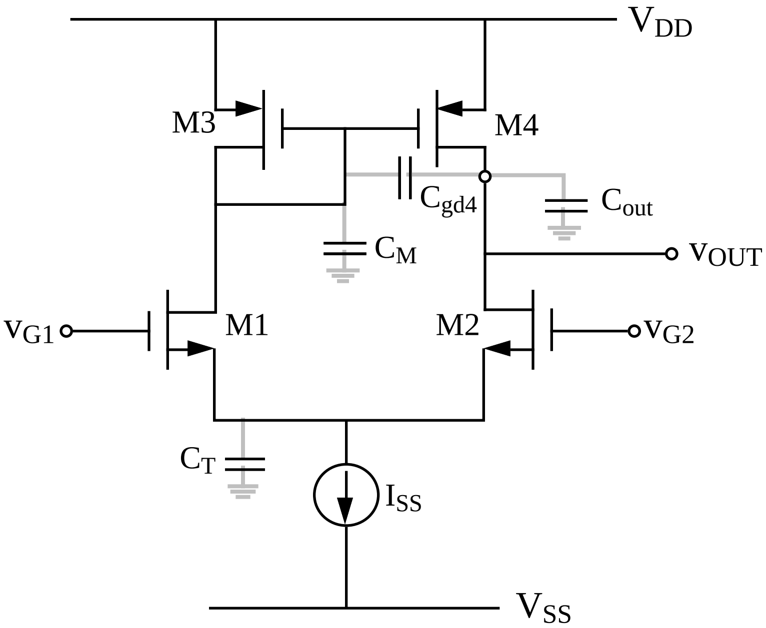
Example

Let all W/L ratios be unity, I_{SS} = 100µA, and use the values of Table 3.1-2 to find the CMRR of a CMOS differential amplifier.

$g_{m1} = \sqrt{2\text{x}17(\mu\text{A/V}^2)\text{x}100\mu\text{A}}$ = 58.3µS
$g_{ds5} = 0.01\text{V}^{-1}$ x 100µA =1µS
Therefore, |CMRR| = 116

CMOS DIFFERENTIAL AMPLIFIERS

Parasitic Capacitances

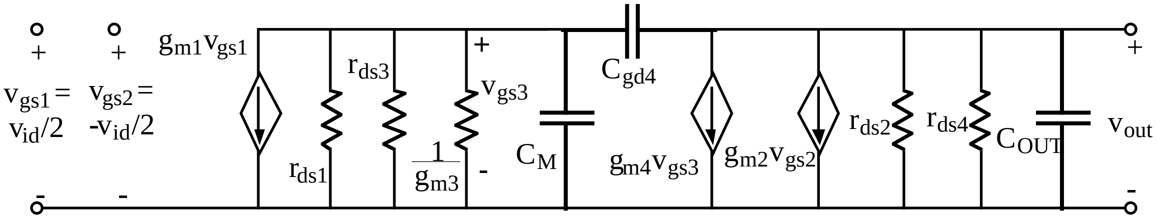


C_T = tail capacitor (common mode only)

C_M = mirror capacitor = $C_{dg1} + C_{db1} + C_{gs3} + C_{gs4} + C_{db3}$

C_{OUT} = output capacitor ≈ $C_{bd4} + C_{bd2} + C_{gd2} + C_L$

Small Signal Model



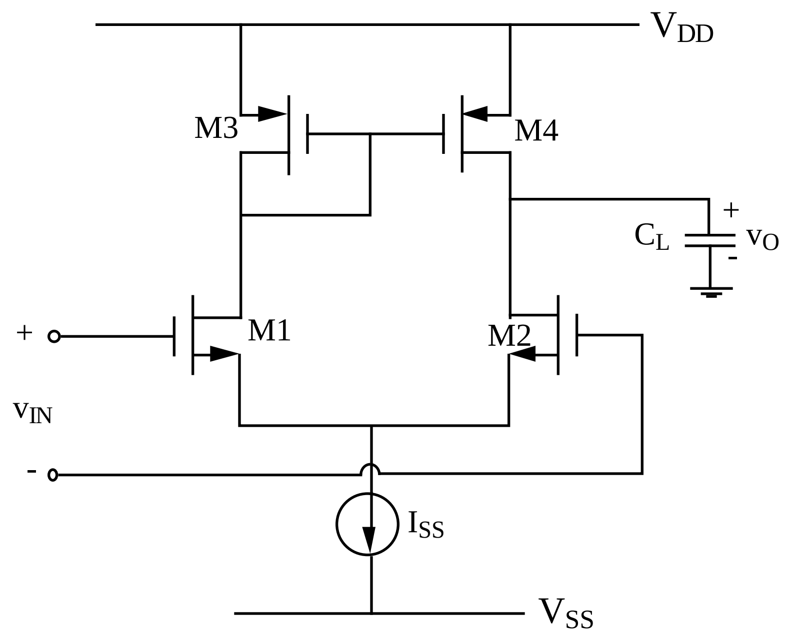
We will examine the frequency response of the differential amplifier in more detail later.

SLEW RATE

Slew rate is defined as an output voltage rate limit usually caused by the current necessary to charge a capacitance.

i.e. $i = C\left(\frac{dV}{dT}\right)$

For the CMOS differential amplifier shown,



Slew rate = $\frac{I_{SS}}{C_L}$

where C_L is the total capacitance seen from the output node to ground.

If C_L = 5pF and I_{SS} = 10µA, then the SR = 2V/µS

CMOS DIFFERENTIAL AMPLIFIERS

NOISE

Assumption:

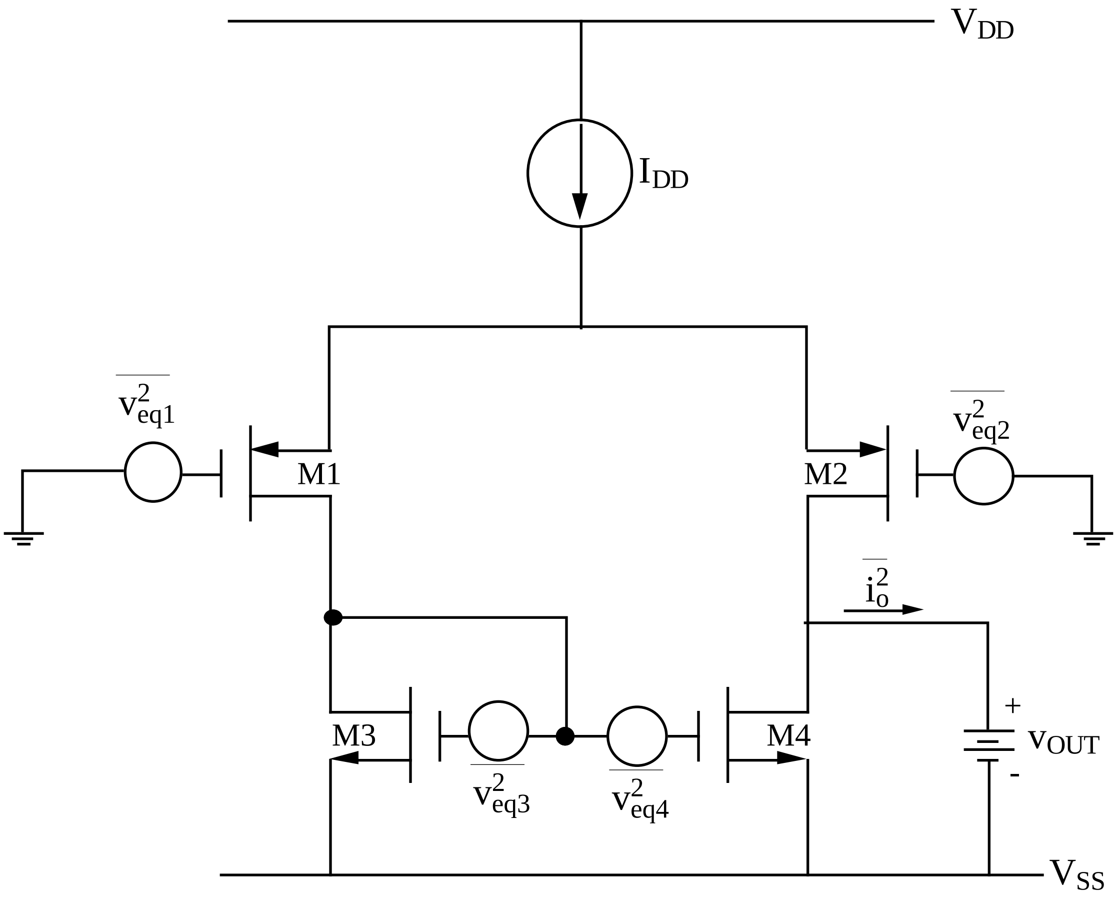
Neglect thermal noise(low frequency) and ignore the thermal noise sources of r_d and r_s .

Therefore:

$$\overline{i_{nd}^2} = \left(\frac{KF}{fC_{ox}L^2}\right) i_D^{AF} \quad (AF = 0.8 \text{ and } KF = 10^{-28})$$

or

$$\overline{v_{nd}^2} = \frac{\overline{i_{nd}^2}}{g_m^2} = \left(\frac{KF}{2f\mu_o C_{ox}^2 WL}\right) i_D^{(AF-1)}$$


V_{DD}
I_{DD}
$\overline{v_{eq1}^2}$
$\overline{v_{eq2}^2}$
M1
M2
$\overline{i_o^2}$
M3
M4
$\overline{v_{eq3}^2}$
$\overline{v_{eq4}^2}$
+
v_{OUT}
-
V_{SS}

CMOS DIFFERENTIAL AMPLIFIERS

NOISE

Total output noise current is found as,

$$\overline{i_{od}^2} = g_{m1}^2\,\overline{v_1^2} + g_{m2}^2\,\overline{v_2^2} + g_{m3}^2\,\overline{v_3^2} + g_{m4}^2\,\overline{v_4^2}$$

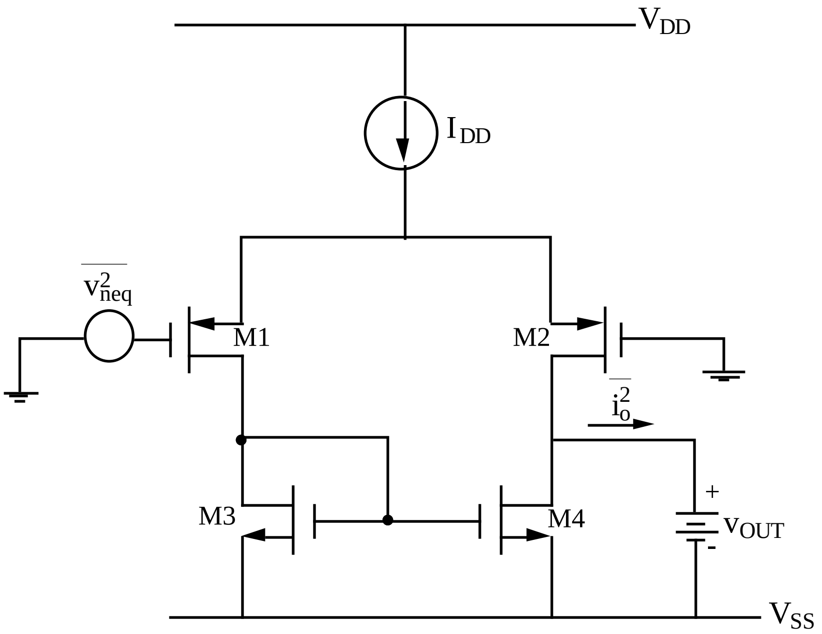
Define $\overline{v_{neq}^2}$ as the equivalent input noise voltage of the differential amplifier. Therefore,

$$\overline{i_{od}^2} = g_{m1}^2\,\overline{v_{neq}^2}$$

or

$$\overline{v_{neq}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right)$$

Where $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$



It is desirable to increase the transconductance of M1 and M2 and decrease the transconductance of M3 and M4. (Empirical studies suggest p-channel devices have less noise)

CMOS DIFFERENTIAL AMPLIFIERS

Minimization of Noise

$$\overline{v_{neq}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right)$$

In terms of voltage spectral-noise densities we get,

$$\overline{e_{eq}^2} = \overline{e_{n1}^2} + \overline{e_{n2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\overline{e_{n3}^2} + \overline{e_{n4}^2}\right)$$

1/f noise

Let $\overline{e_n^2} = \dfrac{KF}{2fC_{ox}WLK'} = \dfrac{B}{fWL}$

assume $\overline{e_{n1}^2} = \overline{e_{n2}^2}$ and $\overline{e_{n3}^2} = \overline{e_{n4}^2}$

$$\therefore \quad \overline{e_{eq}^2}\,(1/f) = \left(\frac{2B_P}{fW_1L_1}\right)\left[1 + \frac{K_N'B_N}{K_P'B_P}\left(\frac{L_1}{L_3}\right)^2\right]$$

1) Since $B_N \approx 5B_P$ use PMOS for M1 and M2 with large area.

2) Make $\dfrac{L_1}{L_3} < \dfrac{K_P'B_P}{K_N'B_N} \approx \dfrac{1}{12.5}$ so that $\overline{e_{eq}^2}\,(1/f) \approx \sqrt{\dfrac{2B_P}{fW_1L_1}}$

Thermal Noise

$$\overline{e_{eq}^2}\,(th) = \frac{16KT(1+\eta_1)}{3\sqrt{2K_P'I_1\left(\frac{W_1}{L_1}\right)}}\left[1 + \frac{K_N'\left(\frac{W_3}{L_3}\right)}{K_P'\left(\frac{W_1}{L_1}\right)}\right]$$

1) Large value of g_{m1}.

2) $\dfrac{L_1}{L_3} < 1$.

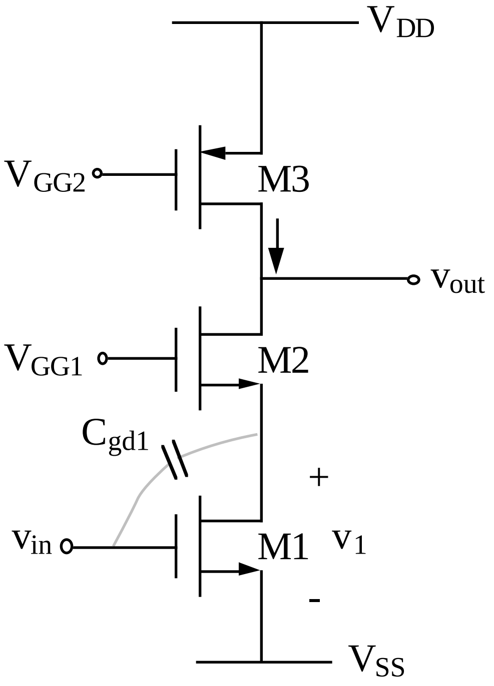
VI.3 - CASCODE AMPLIFIERS

VI.3.1-CMOS CASCODE AMPLIFIERS

Objective

Prevent C_{gd} of the inverter from loading the previous stage. Gives very high gain.

Cascode Amplifier Circuit



Miller effect:

Inverter

$C_{in} \approx$ Gain x C_{gd1}

Cascode

$C_{in} \approx 3C_{gd1}$

$$\left(\frac{v_1}{v_{in}} \approx 2\right)$$

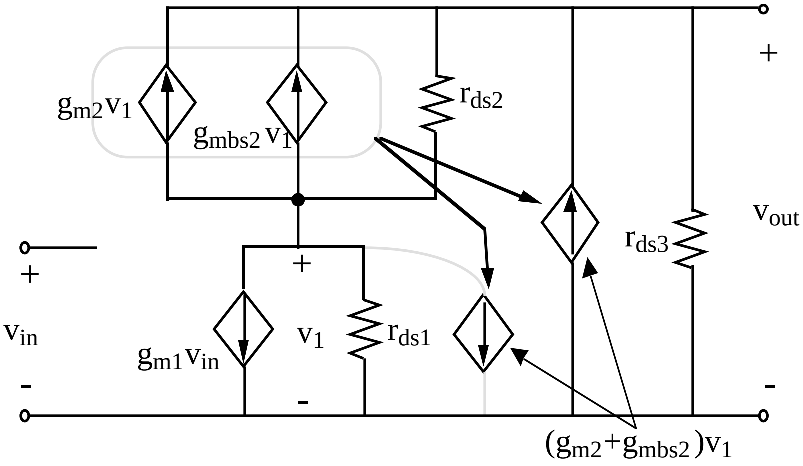
Large Signal Characteristics

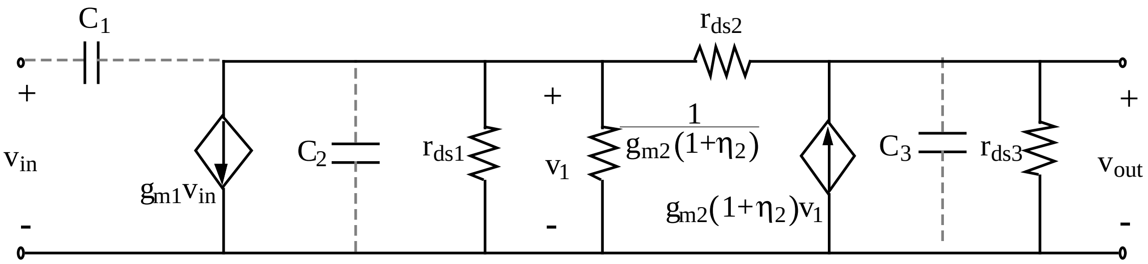
When V_{GG1} designed properly,

$v_{out(min)} = V_{on1} + V_{on2}$

CASCODE AMPLIFIER-CONTINUED

Small Signal Model





Nodal Equations:

$$(g_{m1} - sC_1)v_{in} + (g_{m2} + g_{mbs2} + g_{ds1} + g_{ds2} + sC_1 + sC_2)v_1 - (g_{ds2})v_{out} = 0$$

$$-(g_{ds2} + g_{m2} + g_{mbs2})v_1 + (g_{ds2} + g_{ds3} + sC_3)v_{out} = 0$$

Solving for v_{out}/v_{in} gives

$$\cong \frac{(sC_1-g_{m1})g_{m2}(1+\eta)}{s^2(C_3C_1+C_3C_2)+s\left[(C_1+C_2)(g_{ds2}+g_{ds3}) +C_3g_{m2}(1+\eta)\right]+g_{ds3}g_{m2}(1+\eta)}$$

Small Signal Characteristics

Low-frequency Gains:

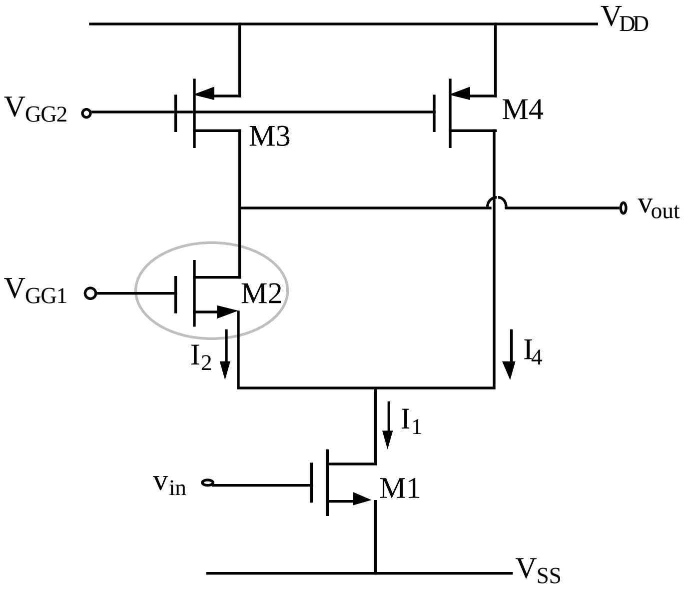
$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}(g_{ds2} + g_{m2} + g_{mbs2})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{mbs2} + g_{ds1} + g_{ds2})}$$

$$\approx \frac{-g_{m1}}{g_{ds3}} = \frac{\sqrt{2K'(W_1/L_1)I_{D1}}}{\lambda_3 I_{D3}}$$

Also (see next page),

$$\frac{v_1}{v_{in}} = \frac{-2g_{m1}}{g_{m2}(1 + \eta_2)}$$

Gain Enhancement:



$$\frac{v_{out}}{v_{in}} \approx \frac{-g_{m1}}{g_{ds3}}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{\sqrt{\frac{2K'W_1}{L_1}}\sqrt{I_1}}{\lambda I_2}$$

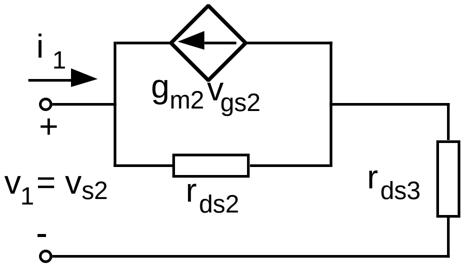
But $I_1 = I_2 + I_4$

$I_4 = 24I_2 \Rightarrow$ x5 Gain enhancement

Voltage Gain of M1:

$$\frac{v_1}{v_{in}} = \frac{-g_{m1}}{g_{m2}} \quad ?$$

What is the small signal resistance looking into the source of M2? Consider the model below:



$$v_{s2} = (i_1 + g_{m2}v_{gs2})r_{ds2} + i_1r_{ds3} = r_{ds2}i_1 + g_{m2}(-v_{s2})r_{ds2} + i_1r_{ds3}$$

or

$$v_{s2}(1 + g_{m2}r_{ds2}) = i_1(r_{ds2} + r_{ds3})$$

Therefore,

$$R = \frac{v_{s2}}{i_1} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2}r_{ds2}} \approx \frac{r_{ds2} + r_{ds3}}{g_{m2}r_{ds2}} = \frac{1}{g_{m2}}\left(1 + \frac{r_{ds3}}{r_{ds2}}\right)$$

Some limiting cases:

$$r_{ds3} = 0 \Rightarrow R = \frac{1}{g_{m2}}$$

$$r_{ds3} = r_{ds2} \Rightarrow R = \frac{2}{g_{m2}}$$

and

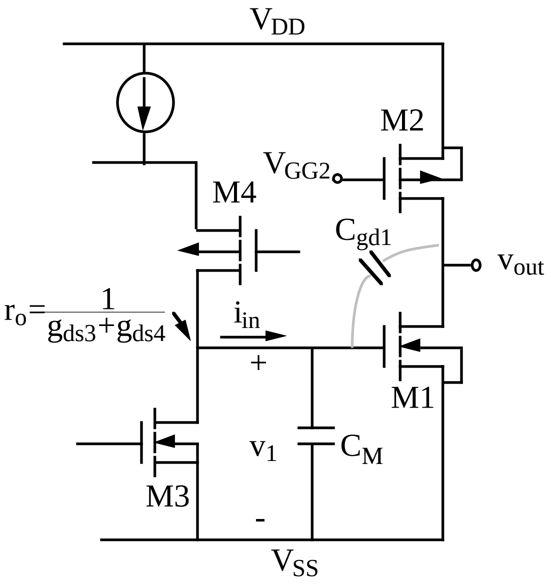
$$r_{ds3} >> r_{ds2} \Rightarrow R = \frac{r_{ds3}}{g_{m2}r_{ds2}}$$

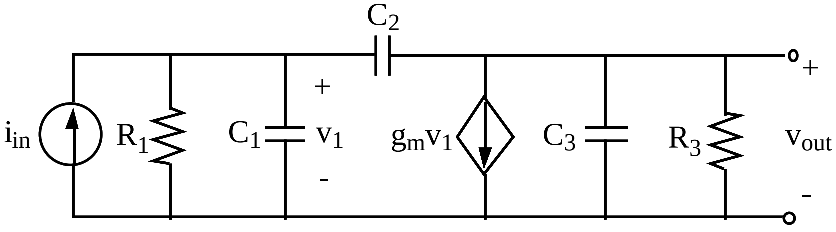
Therefore, the gain v_{in} to v_1 is

$$\frac{v_1}{v_{in}} \approx \frac{-g_{m1}(g_{ds2} + g_{ds3})}{(g_{m2} + g_{mbs2})g_{ds3}} \approx \frac{-2g_{m1}}{g_{m2} + g_{mbs2}} \approx \frac{-2g_{m1}}{g_{m2}}$$

CASCODE AMPLIFIER-CONTINUED

High Resistance Driver for the Inverter M1-M2





$R_1 = (g_{ds3} + g_{ds4})^{-1}$ $R_3 = (g_{ds1} + g_{ds2})^{-1}$

$C_1 = C_{gs1} + C_{bd3} + C_{bd4} + C_{gd3} + C_{gd4}$

$C_2 = C_{gd1}$ $C_3 = C_{bd1} + C_{bd2} + C_{gd2} + C_L$

$$\frac{v_{out}(s)}{i_{in}(s)} =$$

$$\left(\frac{\left[\frac{-g_{m1}}{G_1 G_3}\right]\left[1 - s\left(\frac{g_{m1}}{C_2}\right)\right]}{1 + \left[R_1(C_1+C_3) + R_3(C_2+C_3) + g_{m1}R_1R_3C_2\right]s + (C_1C_2 + C_1C_3 + C_2C_3)R_1R_3s^2} \right)$$

Note:

$$d(s) = 1 + as + bs^2 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2}$$

If $|p_2| >> |p_1|$, then

$$d(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2} \quad \text{or} \quad \boxed{p_1 = -\frac{1}{a}} \quad \text{and} \quad \boxed{p_2 = -\frac{a}{b}}$$

Using this technique we get,

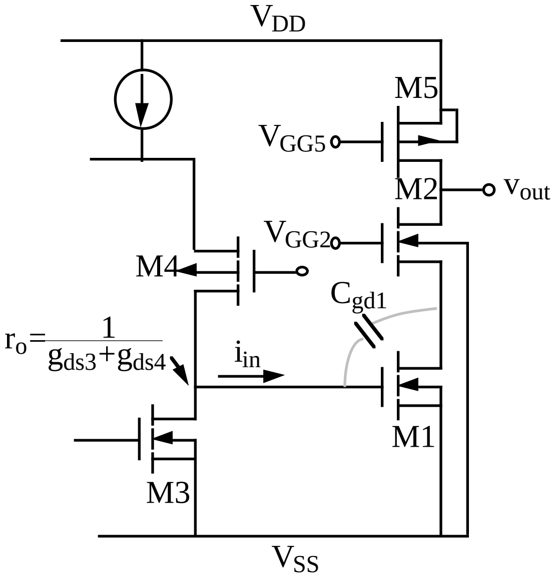
$$p_1 \approx \frac{-1}{R1(C1+C3)+R3(C2+C3)+gm1R1R3C2} \approx \frac{-1}{g_{m1}R_1R_3C_2}$$

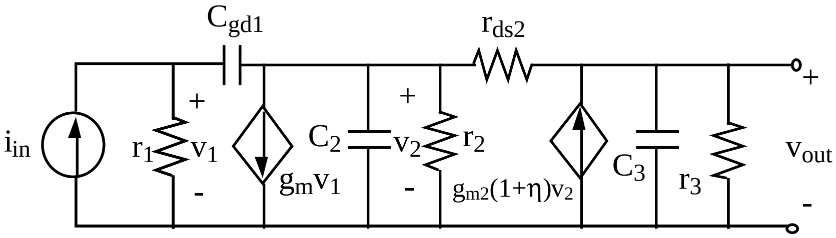
(Miller effect on C_2 causes p_1 to be dominant; $C_M \approx g_{m1}R_2C_{gd1}$)

$$p_2 \approx \frac{-g_{m1}C_2}{C_1C_2+C_1C_3+C_2C_3}$$

CASCODE AMPLIFIER - CONTINUED

How does the Cascode Amplifier solve this problem?





$$r_1 = r_o = (g_{ds3} + g_{ds4})^{-1}$$

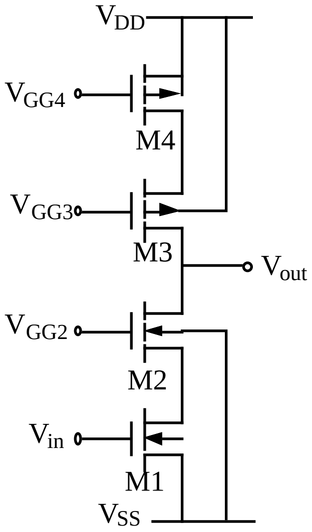
$$C_2 = C_{gs2} + C_{sb2} + C_{db1} + C_{gd1}$$

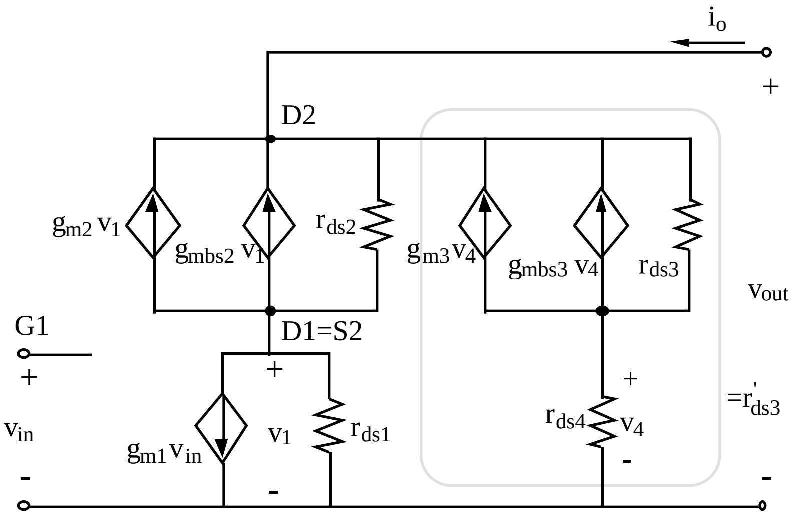
$$r_2 = \left[g_{ds1} + g_{m2}(1+\eta)\right]^{-1} \approx \frac{1}{g_{m2}}$$

$$C_3 = C_{gd2} + C_{db2} + C_{gd5} + C_{db5} + C_L$$

$$r_3 \approx \left(\frac{g_{m2}}{g_{ds1}\, g_{ds2}} + g_{ds5}\right)^{-1} \approx \frac{1}{g_{ds5}}$$

Cascode amplifier with higher gain and output resistance





VI.4 - OUTPUT AMPLIFIERS

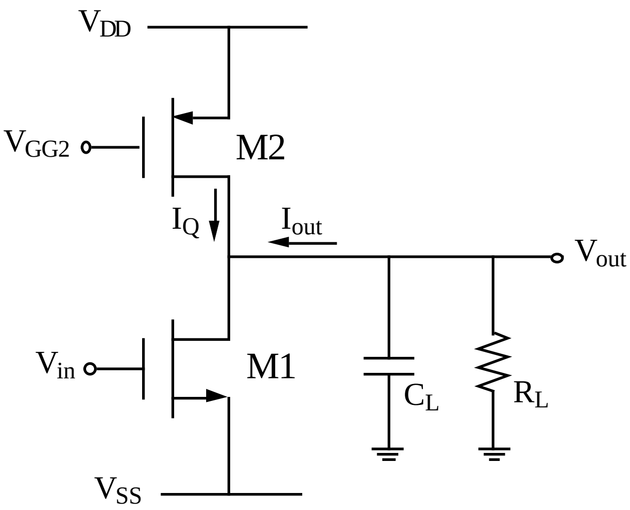
Requirements

1. Provide sufficient output power in the form of voltage or current.
2. Avoid signal distortion for large signal swings.
3. Be efficient.
4. Provide protection from abnormal conditions.

Types of Output Stages

1. Class A amplifier.
2. Source follower.
3. Push-Pull amplifier (inverting and follower).
4. Substrate BJT.
5. Negative feedback (OP amp and resistive).

CLASS A AMPLIFIER



$$I_{out}^{+} = \frac{KnW_1}{2L_1}(V_{DD} - V_{SS} - V_{T1})^{2} - I_Q$$

$$I_{out}^{-} = \frac{KpW_2}{2L_2}(V_{DD} - V_{GG2} - |V_{T2}|)^{2} < I_{out}^{+}$$

$|I_{out}|$ determined by:

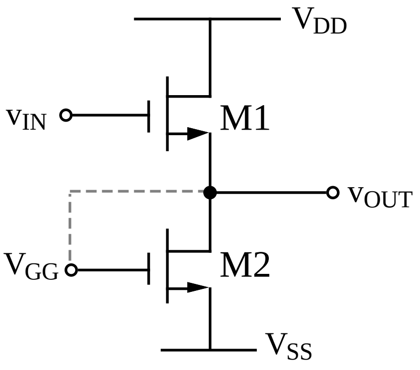
1. $|I_{out}| = C_L \dfrac{dv_{out}}{dt} = C_L$ (slew rate)
2. $|I_{out}| = \dfrac{v_{out}(\text{peak})}{R_L}$

$$\text{Efficiency} = \frac{P_{RL}}{P_{supply}} = \left(\frac{V_{out}(\text{peak})}{(V_{DD} + V_{SS})}\right)^{2} \leq 25\%$$

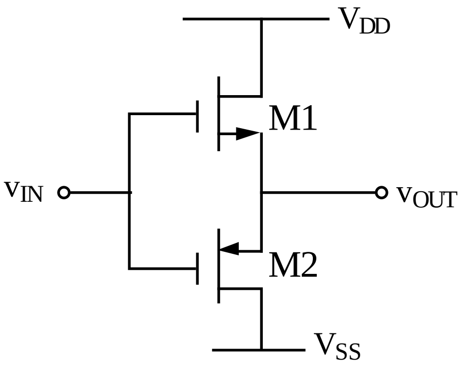
$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{2\lambda I_D} \qquad \text{(typically large)}$$

SOURCE FOLLOWER

N-Channel



Push Pull



Large Signal Characteristics

$$v_{OUT} = v_{IN} - v_{GS1}$$

Maximum Output Swing Limits

$v_{OUT}(\mathrm{MAX}) = V_{DD} - V_{T1}$
(V_{T1} greater than V_{T0} because of v_{BS})

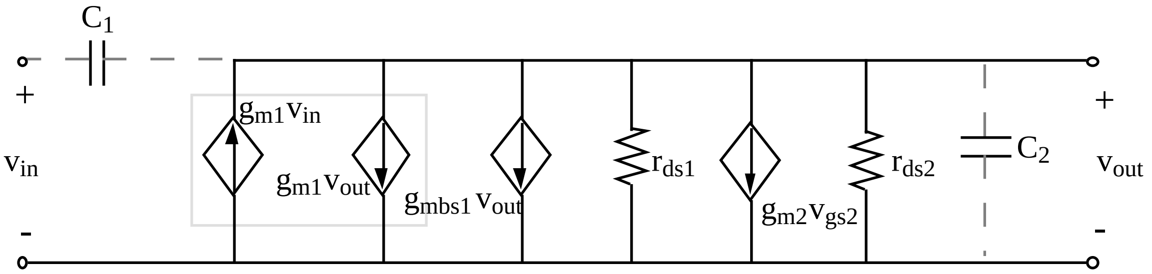
Single Channel Follower:
$v_{OUT}(\mathrm{MIN}) = V_{SS}$

Push Pull Follower:
$v_{OUT}(\mathrm{MIN}) = V_{SS} + |V_{T2}|$
(V_{T2} greater than V_{T0} because of v_{BS})

SOURCE FOLLOWERS

Small Signal Characteristics

Single Channel Follower (Current source and active load):



Small Signal Voltage Transfer Function:

$$\boxed{\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}} \quad \text{where } g_{m2} = 0 \text{ if } v_{GS2} = V_{GG}}$$

Example:

If $V_{DD}= -V_{SS} = 5\text{V}$, $v_{OUT} = 0\text{V}$, $i_D = 100\mu\text{A}$, and $\frac{W}{L} = \frac{10\ \mu\text{m}}{10\ \mu\text{m}}$,

then;

$$\frac{v_{out}}{v_{in}} = \frac{41.23}{1+1+41.23(1+0.2723)+41.23} = 0.4309 \text{ when } v_{GS2} = v_{OUT}$$

$$\frac{v_{out}}{v_{in}} = \frac{41.23}{1+1+41.23(1+0.2723)} = 0.751 \text{ when } v_{GS2} = V_{GG}$$

Approximation gives $\frac{vout}{v_{in}} \approx 0.786$ $(g_{ds1}= g_{ds2} \approx 0)$

Output Resistance:

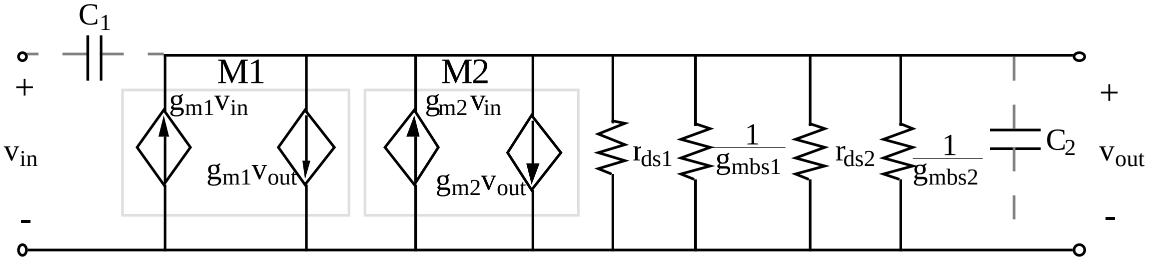
$$\boxed{r_{out} = \frac{1}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}} \text{ where } g_{m2} = 0 \text{ if } v_{GS2}= V_{GG}}$$

$r_{out} = 10.5\ \text{K}\Omega$ $(v_{GS2} = v_{OUT})$ and $r_{out} = 18.4\ \text{K}\Omega$ $(v_{GS2} = V_{GG})$

SOURCE FOLLOWERS

Push Pull Source Follower

Model:



Small Signal Voltage Transfer Function:

$$\boxed{\frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2}}}$$

Example:

If $V_{DD} = -V_{SS} = 5\text{V}$, $v_{OUT} = 0\text{V}$, $i_D = 100\mu\text{A}$, and $\frac{W}{L} = \frac{10\mu\text{m}}{10\mu\text{m}}$

then,

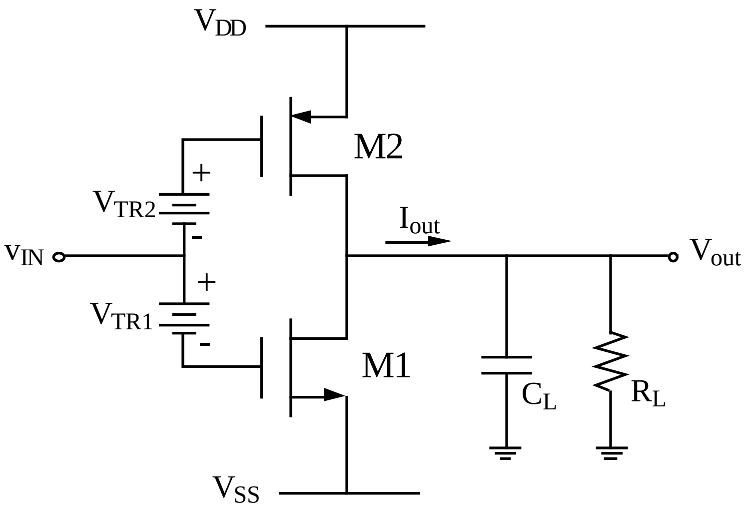
$$\frac{v_{out}}{v_{in}} = \frac{41.23 + 28.28}{1 + 0.5 + 41.23(1 + 0.2723) + 28.28(1 + 0.1268)} = 0.81$$

Output Resistance:

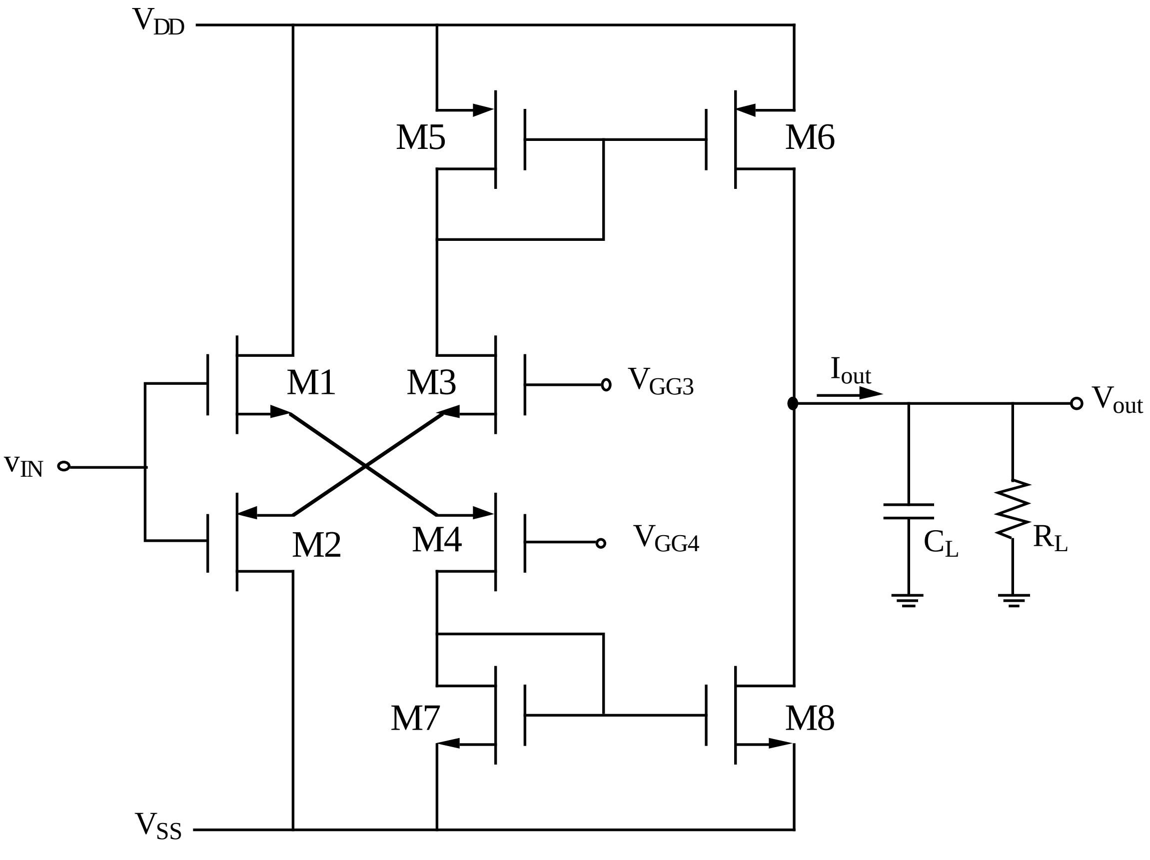
$$\boxed{r_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2}} = 11.7\text{K}\Omega}$$

PUSH-PULL INVERTERING CMOS AMPLIFIER

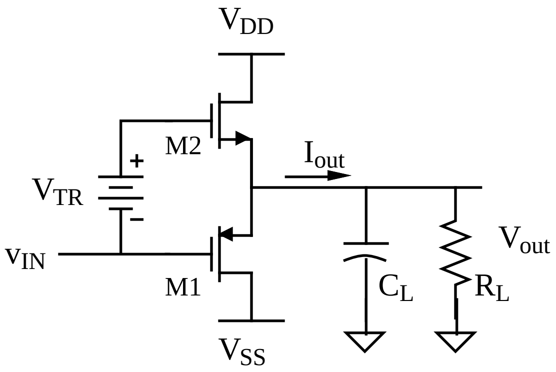
Concept-

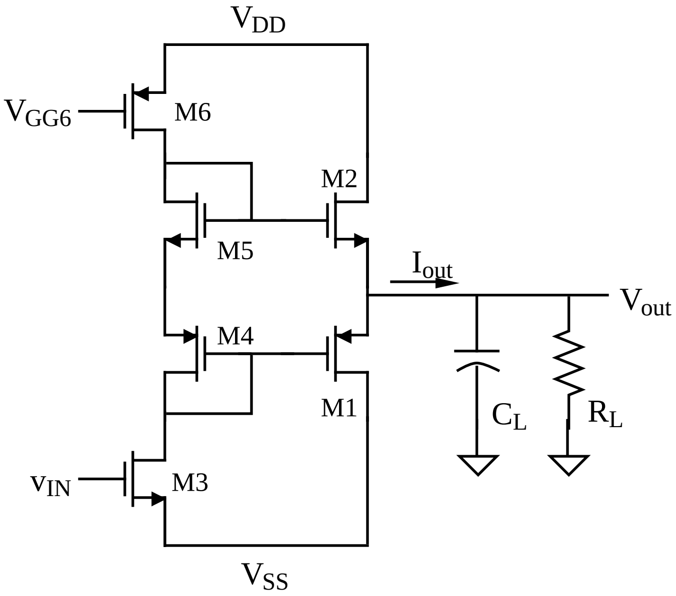


Implementation-

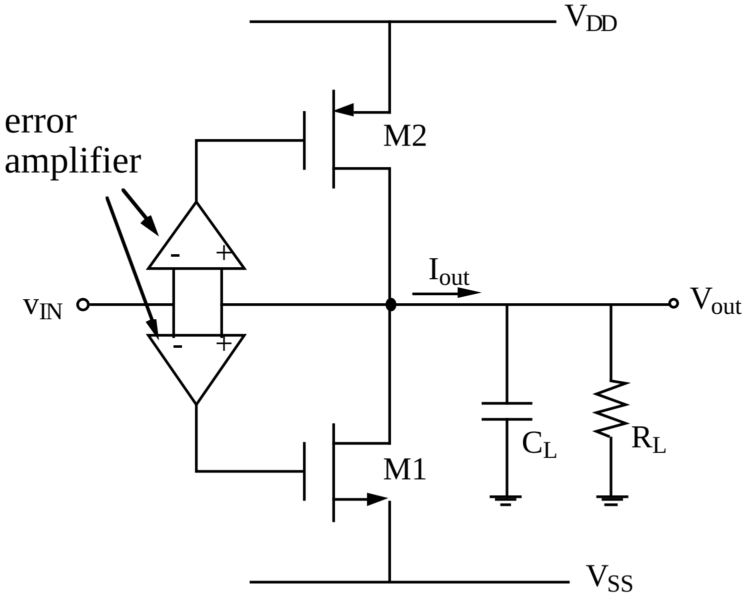


PUSH-PULL SOURCE FOLLOWER

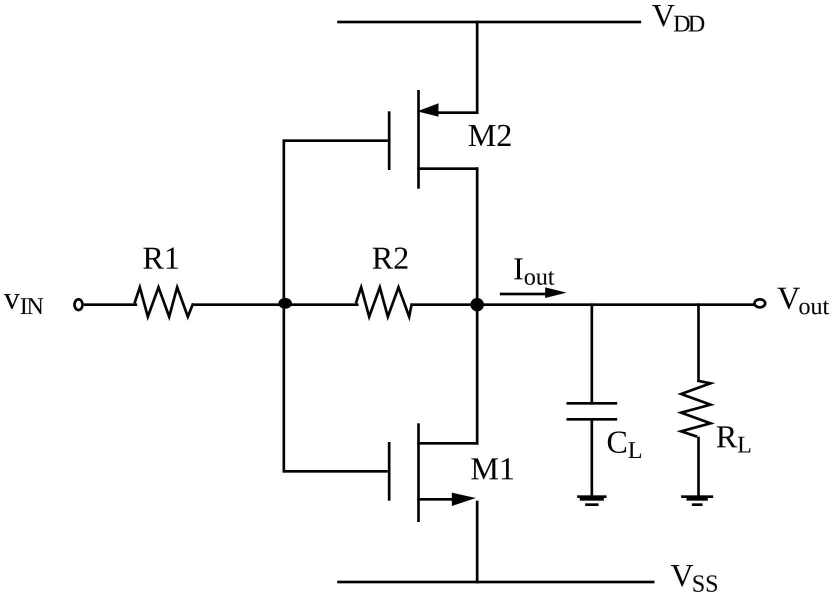




USE OF NEGATIVE FEEDBACK TO REDUCE ROUT



Use of negative feedback to reduce the output resistance of Fig. 6.3-4.



Use of resistive feedback to decrease the output resistance of Fig.6.3-4.

VI.5 - SUMMARY

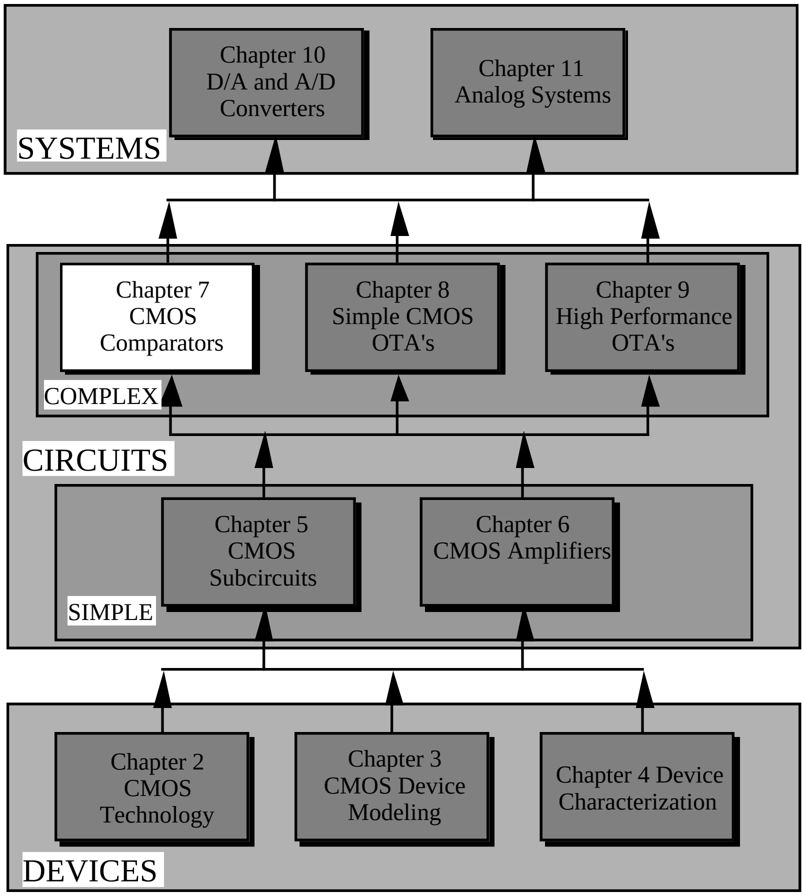
- Analog Amplifier Building Blocks
  - Inverters - Class A
  - Push-Pull - Class AB or B
  - Cascode - Increased bandwidth
  - Differential - Common mode rejection, good input stage
  - Output - Low output resistance with minimum distortion

SECTION 7 - COMPARATORS

VII. COMPARATORS

Contents

Organization



VII.1 - CHARACTERIZATION OF COMPARATORS

What is a Comparator?

A comparator is a circuit which compares two analog signals and outputs a binary signal based on the comparsion. (It can be an op amp without frequency compensation.)

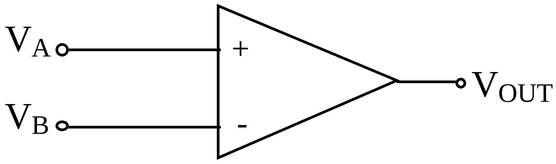
Characterization of Comparators

We shall characterize the comparator by the following aspects:

- Resolving capability
- Speed or propagation time delay
- Maximum signal swing limits
- Input offset voltage
- Other Considerations
    - Noise
    - Power
    - Etc.

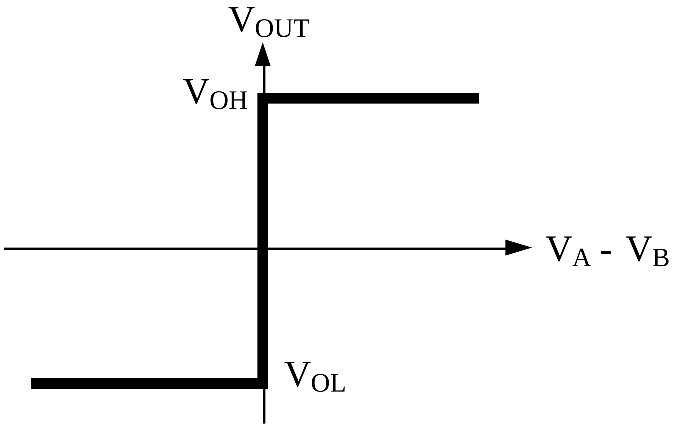
VOLTAGE COMPARATORS

Definition of a Comparator



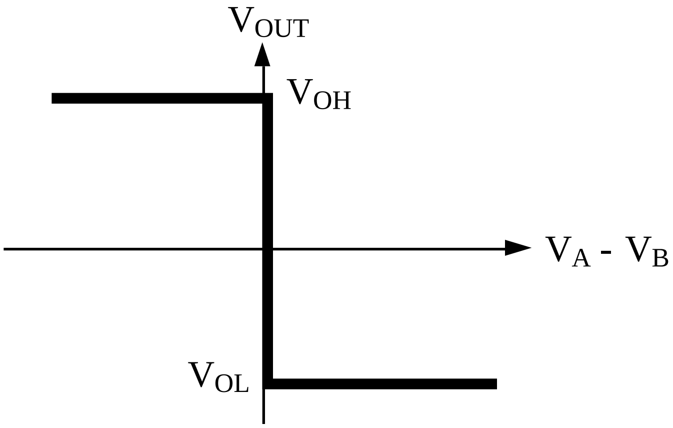
Noninverting

$$V_{OUT} = \begin{cases} V_{OH} & \text{when } V_A \geq V_B \\ V_{OL} & \text{when } V_A < V_B \end{cases}$$



Inverting

$$V_{OUT} = \begin{cases} V_{OL} & \text{when } V_A \geq V_B \\ V_{OH} & \text{when } V_A \leq V_B \end{cases}$$



COMPARATOR PERFORMANCE

1. Speed or propagation time delay.

    The amount of time between the time when V_A - V_B = 0 and the output is 50% between initial and final value.

2. Resolving capability.

    The input change necessary to cause the output to make a transition between its two stable states.

3. Input common mode range.

    The input voltage range over which the comparator can detect $V_A = V_B$.

4. Output voltage swing (typically binary).

5. Input offset voltage.

    The value of V_{OUT} reflected back to the input when V_A is physically connected to V_B.

APPROACHES TO THE DESIGN OF VOLTAGE COMPARATORS

Open Loop

Use of a high-gain differential amplifier.

$$\text{Gain} = \frac{V_{OH} - V_{OL}}{\text{resolution of the comparator}}$$

Regenerative

Use of positive feedback to detect small differences between two voltages, V_A and V_B. I.e., sense amplifiers in digital memories.

Open Loop - Regenerative

Use of low gain, high speed comparator cascaded with a latch. Results in comparators with very low propagation time delay.

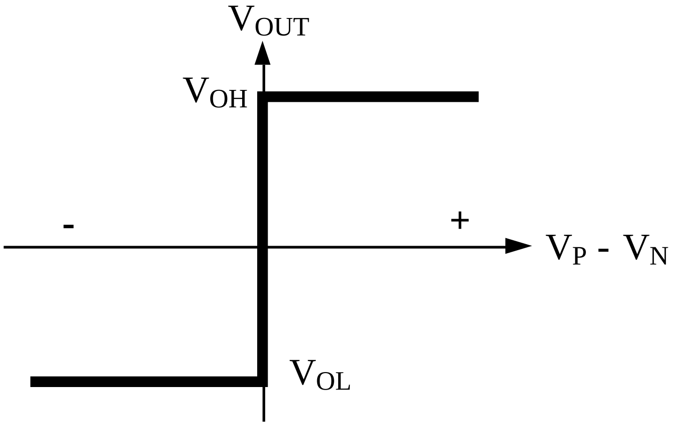
Charge Balancing

Differential charging of a capacitor. Compatible with switched capacitor circuit techniques.

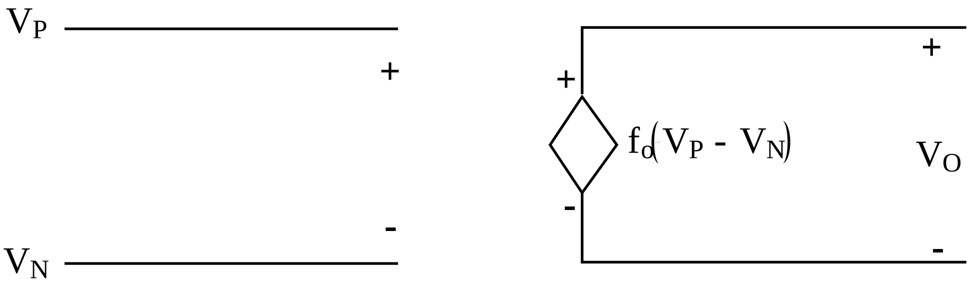
Type	Offset Voltage (Power supply)	Resolution	Speed (8 bit)
Open-loop	1-10 mV	300µV (±5V)	10 MHz
Regenerative	0.1 mV	50µV (±5V)	50 MHz
Charge Balancing	0.1 mV	5mV (5V)	30 MHz

COMPARATOR MODELS - OPEN LOOP

Zero Order Model



Model

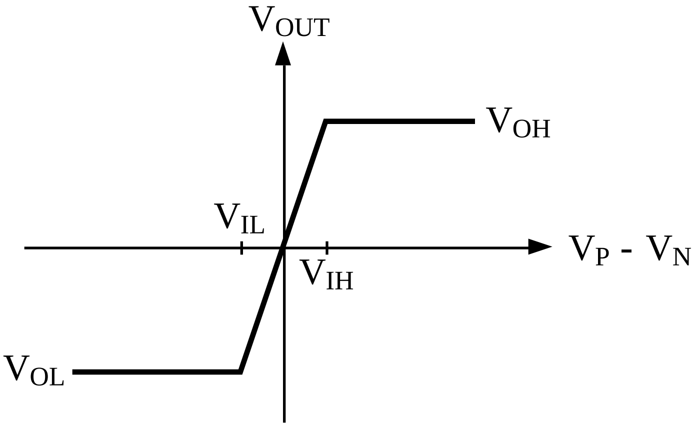


$$f_o(V_P - V_N) = \begin{cases} V_{OH} & \text{for } (V_P - V_N) \geq 0 \\ V_{OL} & \text{for } (V_P - V_N) \leq 0 \end{cases}$$

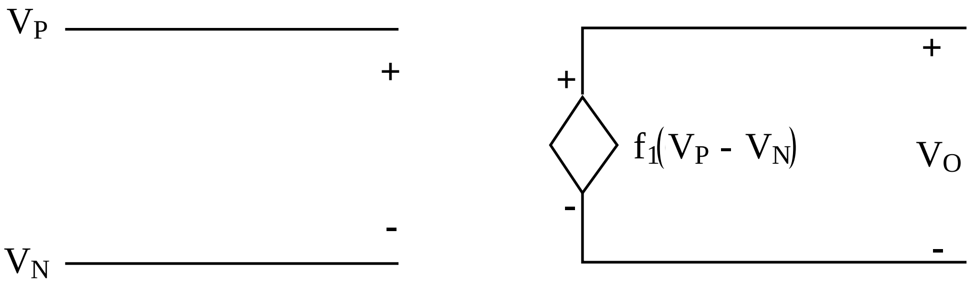
COMPARATOR MODELS - CONT'D

First Order Model

Transfer Curve



Model

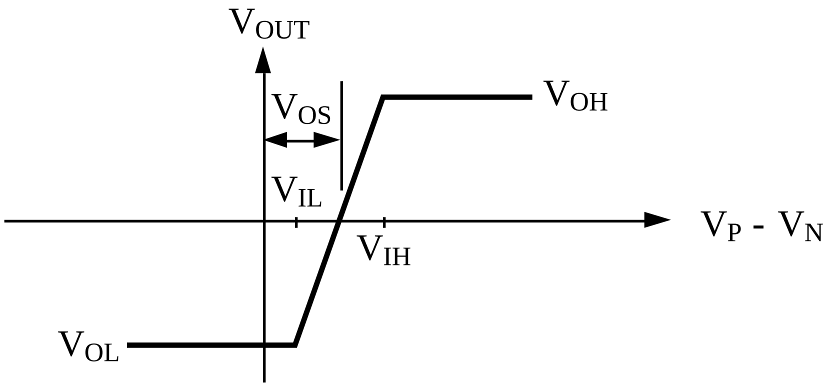


$$f_1(V_P - V_N) = \begin{cases} V_{OH} & \text{for } (V_P - V_N) \geq V_{IH} \\ A_V(V_P - V_N) & \text{for } V_{IL} \leq (V_P - V_N) \leq V_{IH} \\ V_{OL} & \text{for } (V_P - V_N) \leq V_{IL} \end{cases}$$

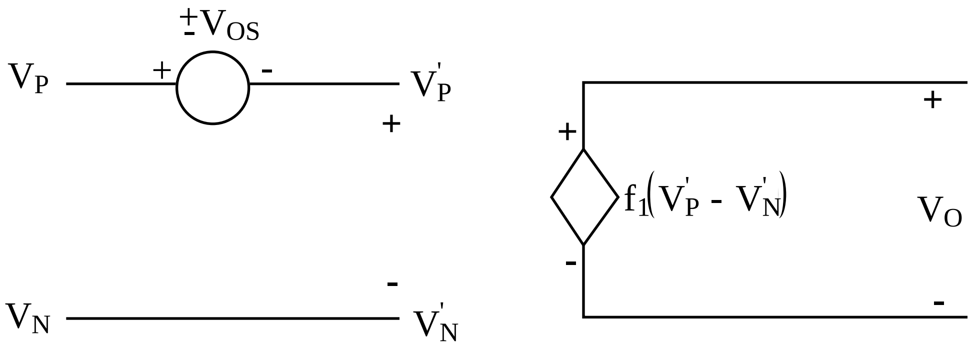
COMPARATOR MODELS - CONT'D

First Order Model with Offset

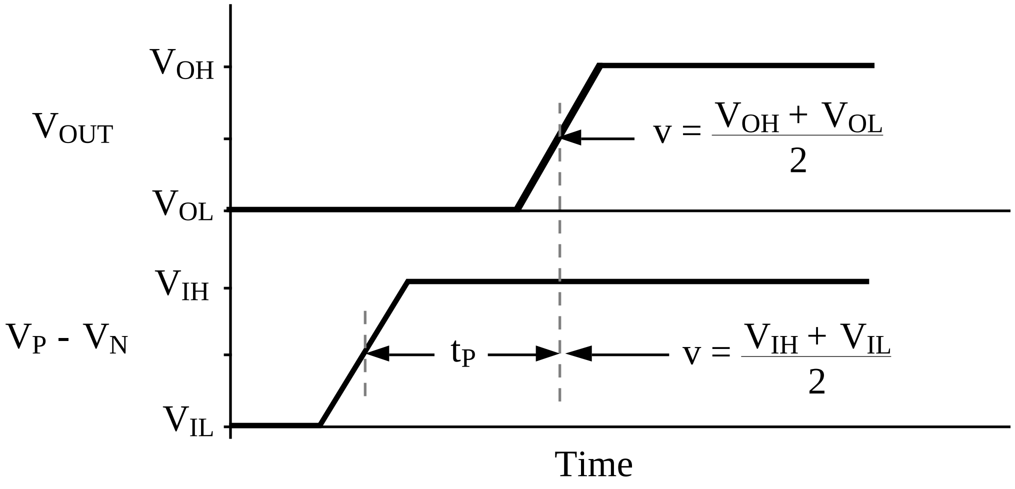
Transfer Curve



First Order Model with Offset



Time Response of Noninverting, first order model



VII.2 - DEVELOPMENT OF A CMOS COMPARATOR

SIMPLE INVERTING COMPARATOR

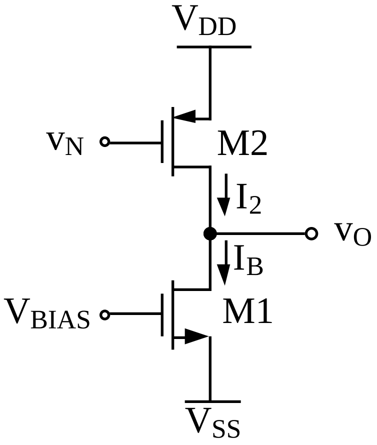


Fig. 7.2-1 Simple inverting comparator

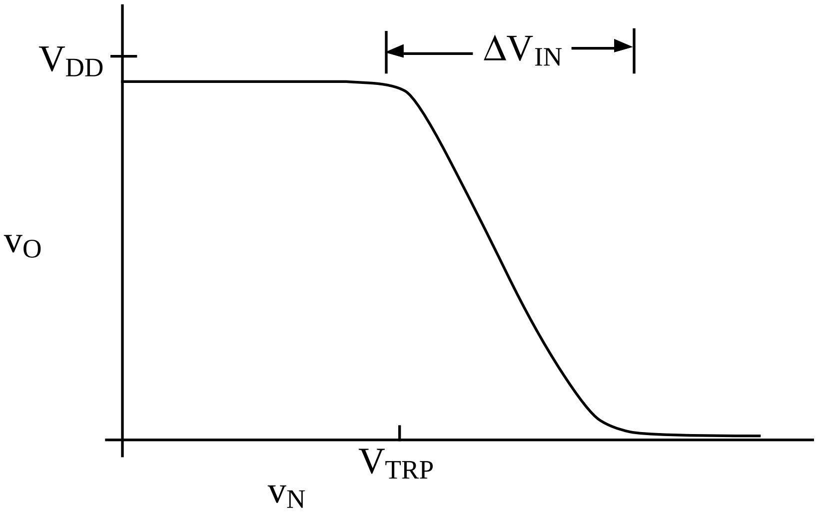
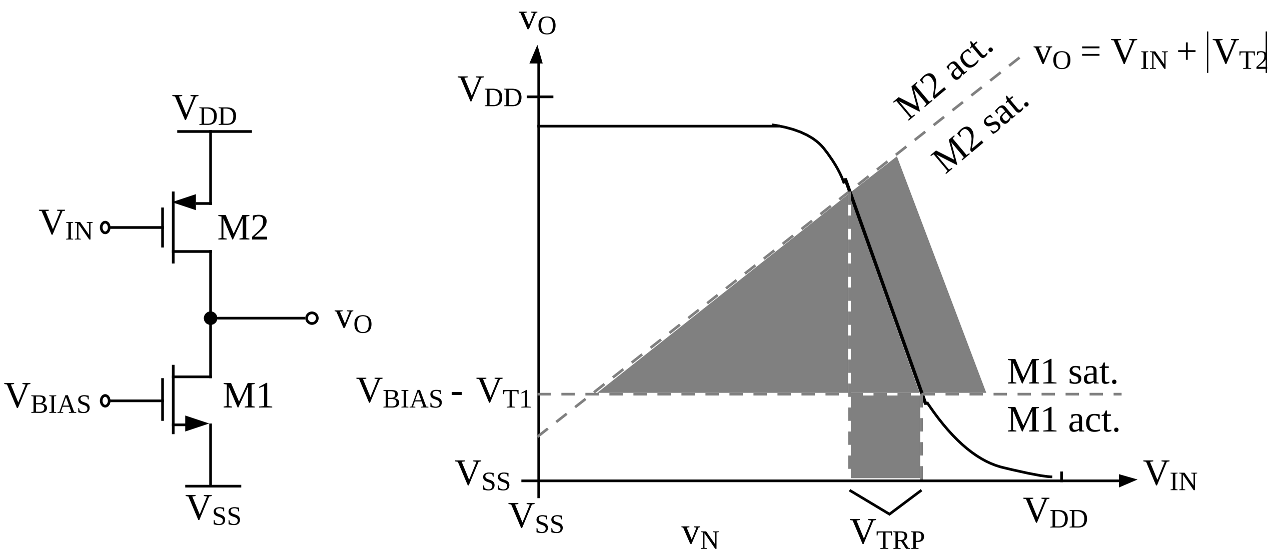


Fig. 7.2-2 DC transfer curve of a simple comparator

Low gain ⇒ Poor resolution

$V_{TRP} = f(V_{DD}) +$ process parameters

CALCULATION OF THE TRIP POINT, V_{TRP}



Operating Regions-

$v_{DS1} \geq v_{GS1} - V_T$ ‘ $v_O - V_{SS} \geq V_{BIAS} - V_{SS} - V_{T1}$

$$\underline{\underline{v_O \geq V_{BIAS} - V_{T1}}}$$

$v_{SD2} \geq v_{SG2} - |V_{T2}|$ ‘ $V_{DD} - v_O \geq V_{DD} - v_{IN} - |V_{T2}|$

$$\underline{\underline{v_O \leq v_{IN} + |V_{T2}|}}$$

Trip Point-

Assume both M1 and M2 are saturated, solve and equate drain currents for V_{TRP}. Assume $\lambda \approx 0$.

$$i_{D1} = \frac{K_N}{2}\frac{W_1}{L_1}\left(V_{BIAS} - V_{SS} - V_{T1}\right)^2$$

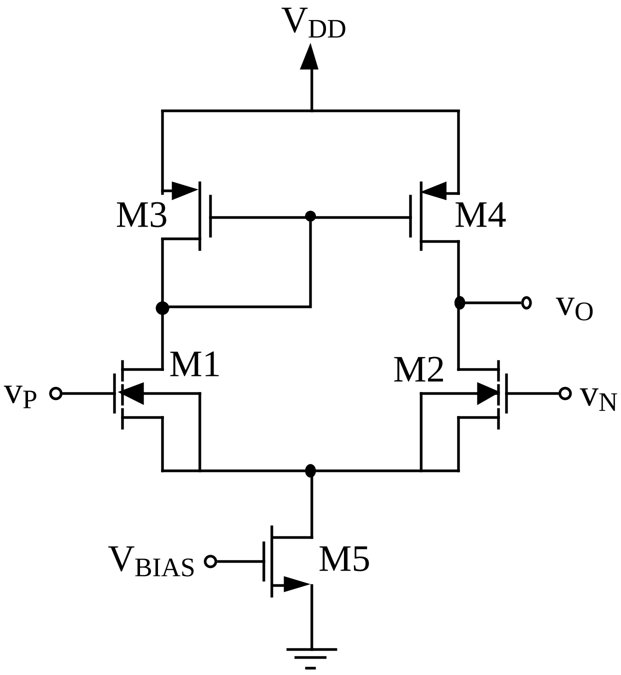
$$i_{D2} = \frac{K_P}{2}\frac{W_2}{L_2}\left(V_{DD} - v_{IN} - |V_{T2}|\right)^2$$

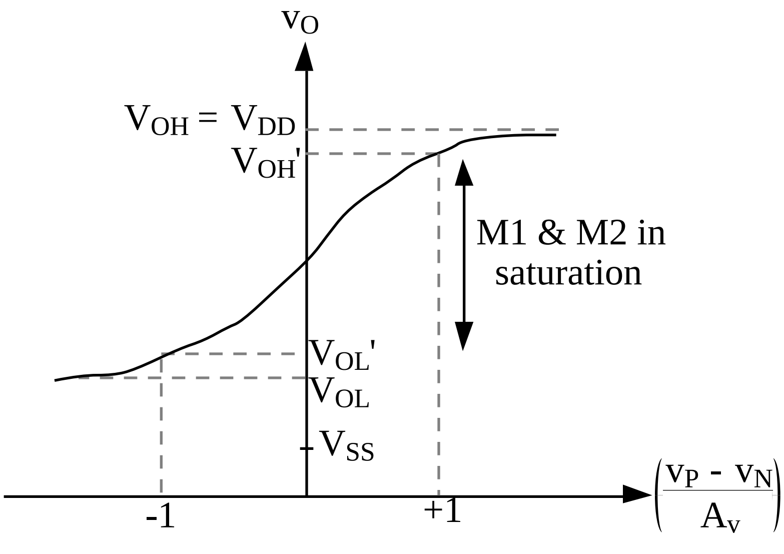
$i_{D1}=i_{D2}$ ‘ $\boxed{v_{IN} = V_{TRP} = V_{DD} - |V_{T2}| - \sqrt{\frac{K_N(W_1/L_1)}{K_P(W_2/L_2)}}(V_{BIAS} - V_{SS} - V_{T1})}$

I.e. $V_{DD} = -V_{SS} = 5V$, $V_{BIAS} = -2V$ and $K_N\left(\frac{W_1}{L_1}\right) = K_P\left(\frac{W_2}{L_2}\right)$

$V_{TRP} = 5-1-(-2+5-1) = 4-2 = \underline{\underline{2V}}$

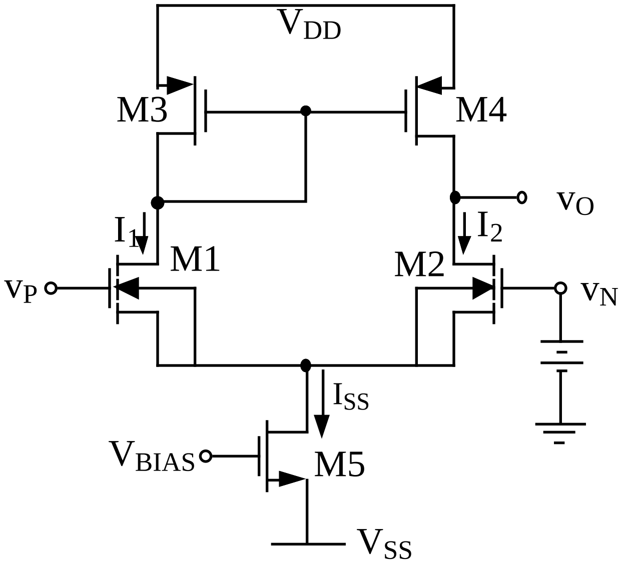
COMPARATOR USING A DIFFERENTIAL AMPLIFIER





Gain is still low for a comparator

DERIVATION OF OUTPUT SWING LIMITS



$v_P < v_N$

Assume v_N is a fixed DC voltage

1. v_O starts to decrease, M3-M4 mirror is valid so that $I_1 = I_2 = I_{SS}/2$.
2. $V_{OL}' = v_N - V_{GS2} + V_{DS2}$
   when M2 becomes non-sat. we have $V_{DS2}(sat) = V_{GS2} - V_T$ so that

$$V_{OL}' = v_N - V_{T2}$$

3. For further decrease in v_O, M2 is non-sat
   and therefore the V_{GS2} can increase allowing the sources of M1 and M2 to fall(as v_P falls).

$\}$ I_1 still equals I_2 due to mirror

4. Eventually M5 becomes non-sat and I_5 starts to decrease to zero. M2 becomes a switch and v_O tracks $V_{S2}(V_{DS5})$ all the way to V_{SS}.

$$\therefore\ V_{OL} = V_{SS}.$$

$v_P > v_N$

1. Current in M1 increases and current in M2 decreases.
2. Mirroring of M3-M4 will cause v_O to approach V_{DD} .
3. $V_{OH}' = V_{DD} - V_{DS4}(sat)$

$$V_{OH}' = V_{DD} - \sqrt{\frac{I_4}{\beta_4}}$$

$$V_{OH}' = V_{DD} - \sqrt{\frac{I_5}{K_p'(W_4/L_4)}}$$

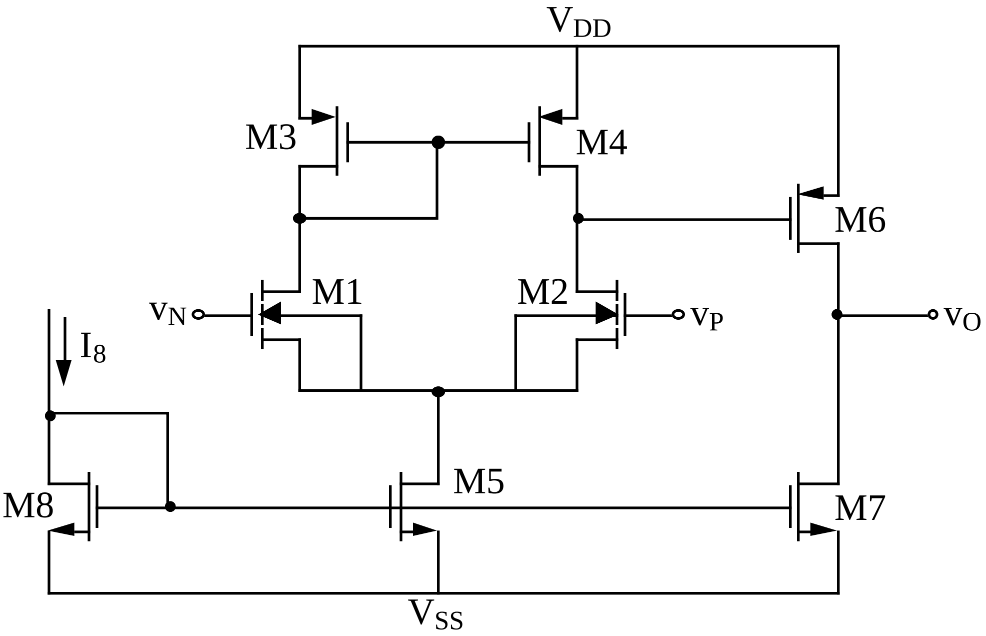
$$V_{OH}' = V_{DD} - \sqrt{\frac{I_5}{K_p'(W_3/L_3)}}$$

4. Finally, v_O ‘ V_{DD} causing the mirror M3-M4 to no longer be valid and $V_{OH} \approx V_{DD}.$
   $(I_2 = I_4 = 0\ ,\ I_3 = I_1 = I_5)$

TWO-STAGE COMPARATOR

Combine the differential amplifier stage with the inverter stage.

- Sufficient gain.
- Good signal swing.



VII.3 - DESIGN OF A TWO-STAGE CMOS COMPARATOR

DC BALANCE CONDITIONS FOR TWO-STAGE COMPARATOR

- Try to keep all devices in saturation - more gain and wider signal swings.

- Based on gate-source and DC current relationship. I.e. if M1 and M2 are two matched devices and if $V_{GS1} = V_{GS2}$, then $I_{D1} = I_{D2}$ or vice versa.

Let $S_1 = \frac{W_1}{L_1}$,

M1 and M2 matched gives $S_1 = S_2$.

M3 and M4 matched gives $S_3 = S_4$.

also, $I_1 = I_2 = 0.5I_5$.

From gate-source matching, we have

$$V_{GS5} = V_{GS7} \text{ ‘ } I_7 = I_5\left(\frac{S_7}{S_5}\right) \text{ and } I_6 = I_4\left(\frac{S_6}{S_4}\right) \leftarrow \text{Assume } V_{GS4} = V_{GS6}$$

For balance conditions, I_6 must be equal to I_7, thus

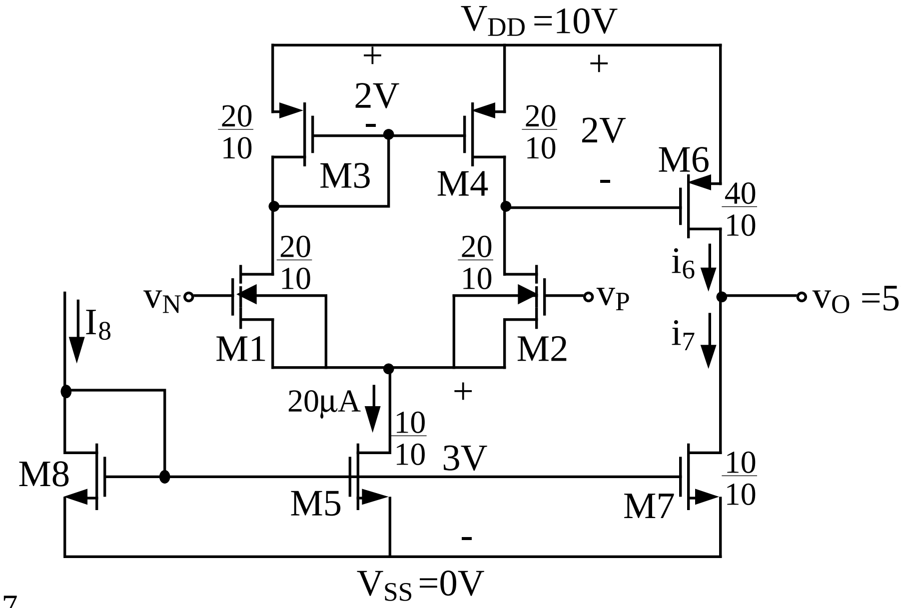
$$\frac{I_5}{I_4} \cdot \frac{S_7}{S_5} = \frac{S_6}{S_4}$$

Since $\frac{I_5}{I_4} = 2$, then DC balance is achieved under the following:

$$\boxed{\frac{S_6}{S_4} = 2 \cdot \frac{S_7}{S_5}} \text{ ‘ } V_{DG4} = 0 \text{ ‘ M4 is saturated.}$$

SYSTEMATIC OFFSET ERROR

$K_N = 24.75\ \mu A/V^2$
$K_P = 10.125\ \mu A/V^2$
$V_{TN} = -V_{TP} = 1V$
$\lambda_N = 0.015V^{-1}$
$\lambda_P = 0.020V^{-1}$



Find V_{OS} to make $i_6 = i_7$

(1) Find the mismatch between i_6 and i_7

$$\frac{i_7}{i_5} = \left(\frac{1+\lambda_N v_{DS7}}{1+\lambda_N v_{DS5}}\right)\left(\frac{W_7/L_7}{W_5/L_5}\right) = \frac{1+(0.015)(5)}{1+(0.015)(3)}(1) = 1.029$$

$$\frac{i_6}{i_4} = \left(\frac{1+\lambda_P v_{DS6}}{1+\lambda_P v_{DS4}}\right)\left(\frac{W_6/L_6}{W_4/L_4}\right) = \frac{1+(0.02)(5)}{1+(0.02)(2)}(2) = 2.115$$

$i_5 = 2i_4$

$\therefore\ i_7 = (1.029)(2)i_4 = 2.057i_4$ and $i_6 = 2.115i_4$

(2) Find how much v_{GS6} must be reduced to make $i_6 = i_7$

$$\Delta v_{GS6} = v_{GS6}(2.115i_4) - v_{GS6}(2.057i_4)$$

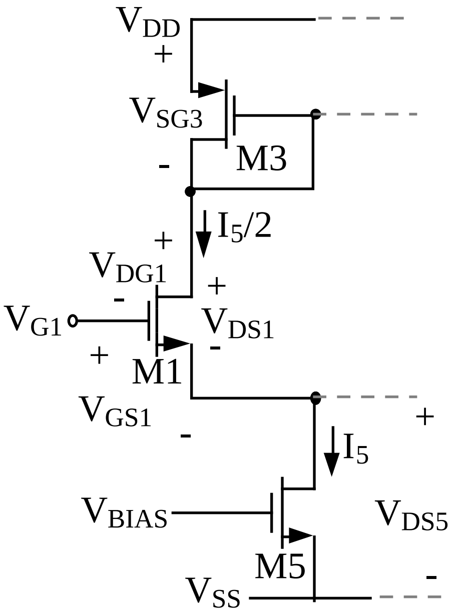
$$\Delta v_{GS6} = \sqrt{\frac{2L_6}{K_P W_6}\, i_4}\left(\sqrt{2.115} - \sqrt{2.057}\right) = 14.11 \text{ mV}$$

(3) Reflecting Δv_{GS6} into the input

$$A_v(\text{diff}) = \left(\frac{2}{\lambda_2+\lambda_4}\right)\sqrt{\frac{K_N(W_2/L_2)}{I_5}} = 89.9$$

$$\therefore\ V_{OS} = \frac{\Delta v_{GS6}}{A_v(\text{diff})} = \frac{14.1 \text{ mV}}{89.9} = \underline{\underline{0.157 \text{ mV}}}$$

DESIGNING FOR COMMON MODE INPUT RANGE



$$v_{G1}(\min) = V_{SS} + V_{DS5} + V_{GS1}$$

$$\boxed{v_{G1}(\min) = V_{SS} + V_{DS5} + V_{T1}(\max) + \sqrt{\frac{I_5}{2\beta_1}}}$$

$$v_{G1}(\max) = V_{DD} - V_{SG3} - V_{DG1}(\mathrm{sat})$$

$$\boxed{v_{G1}(\max) = V_{DD} - \sqrt{\frac{I_5}{2\beta_3}} - \left|V_{T3}(\max)\right| + V_{T1}(\min)}$$

where $V_{DG1}(\mathrm{sat}) = -V_{T1}$

<u>Example</u>

Design M1 through M4 for a CM input range 1.5 to 9 Volts when V_{DD} = 10 V, I_{SS} = 40µA, and V_{SS} = 0V. Table 3.1-2 parameters with $|V_{TN,P}|$ = 0.4 to 1.0 Volts,

$$v_{G1}(\min) = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max)$$

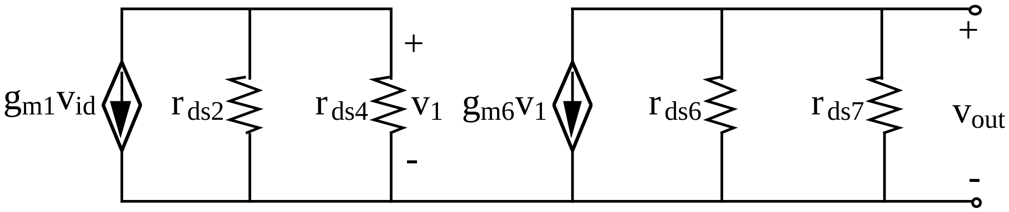
$1.5 = 0 + 0.1 + \sqrt{\frac{40\mu A}{\beta_1}} + 1$ (assumed $V_{DS5} \approx 0.1$V- it probably more reasonable to assume β_1 is already defined and find β_5)

$$\beta_1 = \frac{K_N W_1}{L_1} = 250\ \mu A/V^2 \text{ ‘ } \quad \boxed{\frac{W_1}{L_1} = \frac{W_2}{L_2} = 14.70}$$

$$v_{G1}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T3}(\max)| + V_{T1}(\min)$$

$$\beta_3 = \frac{K_P W_3}{L_3} = 250\ \mu A/V^2 \text{ ‘ } \quad \boxed{\frac{W_3}{L_3} = \frac{W_4}{L_4} = 31.25}$$

GAIN OF THE TWO-STAGE COMPARATOR



$v_{id} = v_P - v_N$

$$A_v = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right)$$

$$A_v = \frac{2\sqrt{K_N K_P \left(\frac{W_1}{L_1}\right)\left(\frac{W_6}{L_6}\right)}}{(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)\sqrt{I_1 I_6}}$$

Using $\frac{W_1}{L_1} = 5$, $\frac{W_6}{L_6} = 5$, $\lambda_N = 0.015\text{V}^{-1}$, $\lambda_P = 0.02\text{V}^{-1}$

and Table 3.1-2 values;

$$A_v = \frac{2\sqrt{(17)(8)(5)(5)}}{(0.015+0.02)^2\sqrt{I_1 I_6}} \cdot 10^{-6} = \frac{95199 \cdot 10^{-6}}{\sqrt{I_1 I_6}}$$

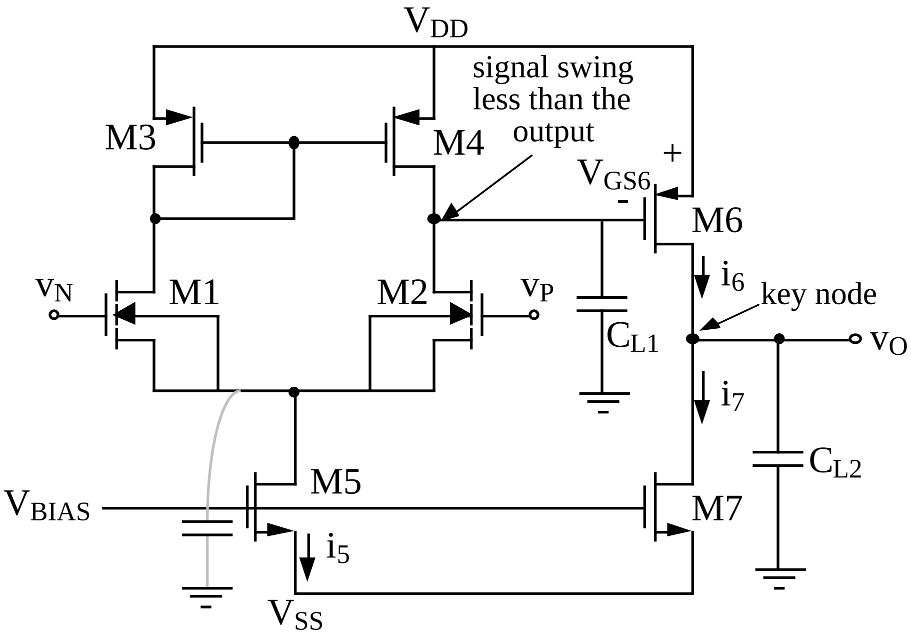
Assume $I_1 = 10\ \mu\text{A}$ and $I_6 = 100\ \mu\text{A}$

$$\underline{\underline{A_v = 3010}}$$

$$\frac{V_{OH} - V_{OL}}{A_v} = \text{Resolution} = 5 \text{ mV (assume)}$$

then $V_{OH} - V_{OL} = \frac{5}{1000} \cdot 3000 = 15$ Volts

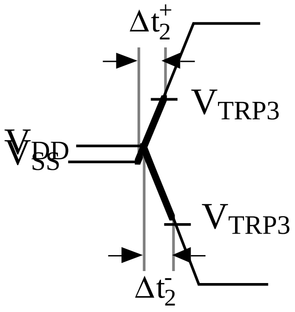
PROPAGATION DELAY OF THE TWO-STAGE COMPARATOR



$$V_{GS6} = V_{DD} - \left(v_P + V_{DG2}\right)$$

$i_C = C\frac{dv}{dt}$, $\Delta t = C\frac{\Delta v}{I}$

$$\Delta t_2+ = C_{L2}\left[\frac{V_{TRP3} - V_{SS}}{\frac{K_P W_6}{2\ L_6}\left(V_{DD} - v_P - V_{DG2} - |V_{T6}|\right)^2 - I_7}\right]$$

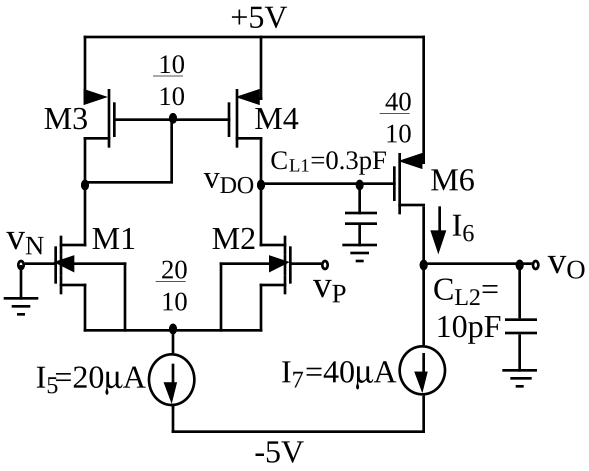


$$\Delta t_2- = C_{L2}\left[\frac{V_{DD} - V_{TRP3}}{\left(\frac{W_7}{L_7}\right)\left(\frac{L_5}{W_5}\right) i_5}\right]$$

$$\text{Slew rate} = \frac{i_{source/sink}}{C_{Li}}$$

CALCULATION OF COMPARATOR PROPAGATION DELAY

Find the total propagation delay of the comparator shown when the input v_P goes from -1 to +1 in 2ns. Assume the trip point of the output(next stage) is zero.



Total delay = 1st stage delay + 2nd stage delay

$$\Delta t = \Delta t_1 + \Delta t_2$$

$$\Delta t_1 = \frac{(v_{DO}(t_0) - V_{TRP2})}{I_5} C_{L1} ,$$

$v_{DO}(t_0) = 5$ because $v_P = -1V$

$$V_{TRP2} = V_{DD} - V_{GS6}, \quad V_{GS6} = |V_{T6}| + \sqrt{\frac{2I_7}{K_P'(W_6/L_6)}}$$

$$V_{GS6} = 1 + \sqrt{\frac{2\cdot 40}{8\cdot 4}} = 2.58 \text{ V ‘ } V_{TRP2} = 5 - 2.58 = 2.42 \text{ V}$$

$$\therefore \ \Delta t_1 = (5 - 2.42)\left(\frac{0.3\text{pF}}{20\mu\text{A}}\right) = 38.7\text{ns}$$

$$\Delta t_2 = \left|v_O(t_0) - 0\right| \left(\frac{C_{L2}}{I_6 - I_7}\right) = 5\left(\frac{C_{L2}}{I_6 - I_7}\right)$$

$$I_6 = \frac{K_{P6}'}{2}\left(\frac{W_6}{L_6}\right)\left(V_{DD} - V_{DO}(\text{min}) - \left|V_{T6}\right|\right)^2$$

[V_{DO}(min) is an optimistic assumption based on $v_{DS2} \approx 0$]

$$V_{DO}(\text{min}) \approx v_{DS2}(\approx 0) - v_{GS1} + v_N = -V_{T1} - \sqrt{\frac{I_5}{K_N\cdot 2}} = -1.77$$

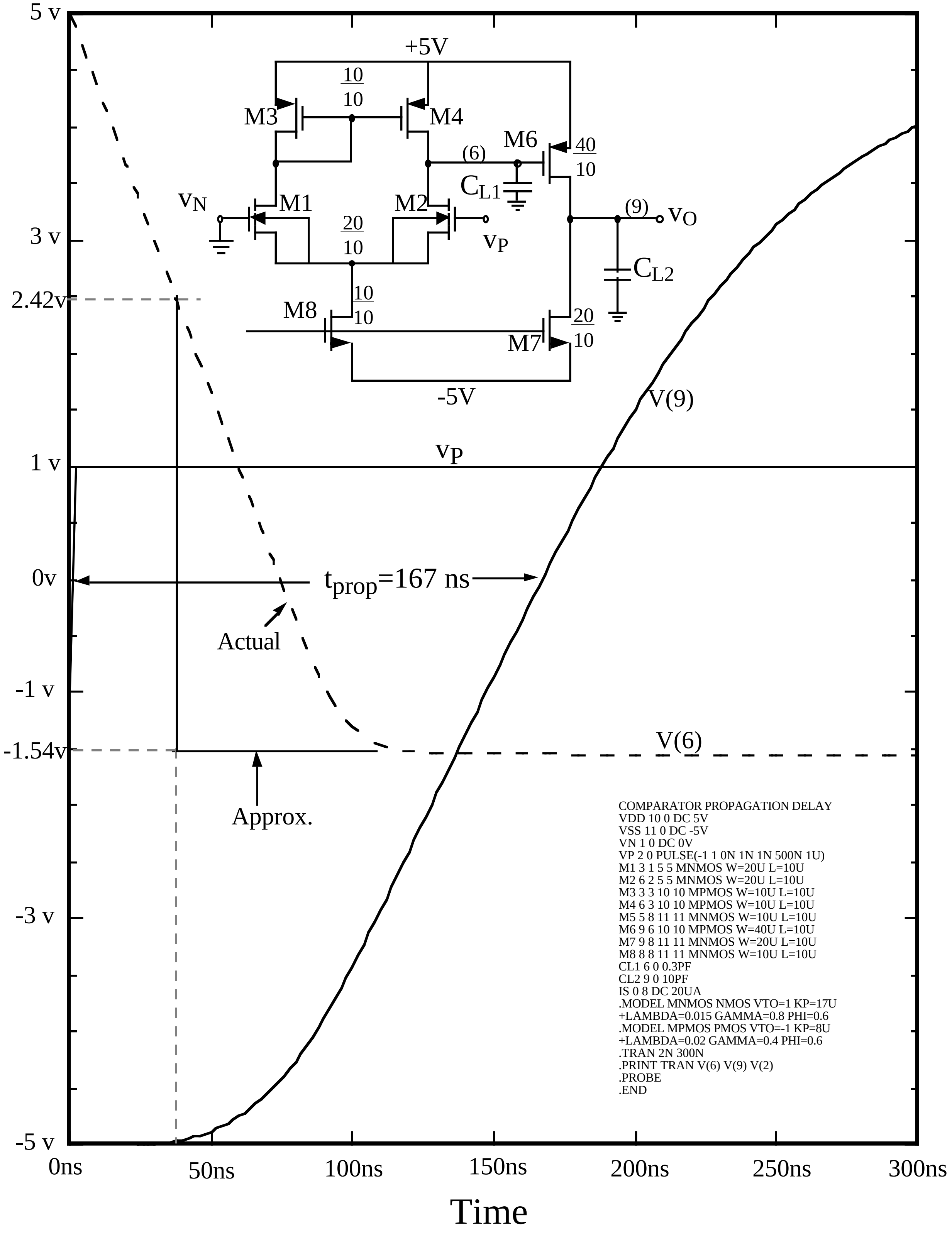
$$I_6 = \frac{8\cdot 10^{-6}}{2}(4)(5 - (-1.77) - 1)^2 = 533\ \mu\text{A}$$

$$\therefore \ \Delta t_2 = 5\,\frac{10 \text{ pF}}{(533 - 40)\ \mu\text{A}} = 101 \text{ ns}$$

$$\underline{\Delta t = \Delta t_1 + \Delta t_2 \approx 139 \text{ ns}}$$

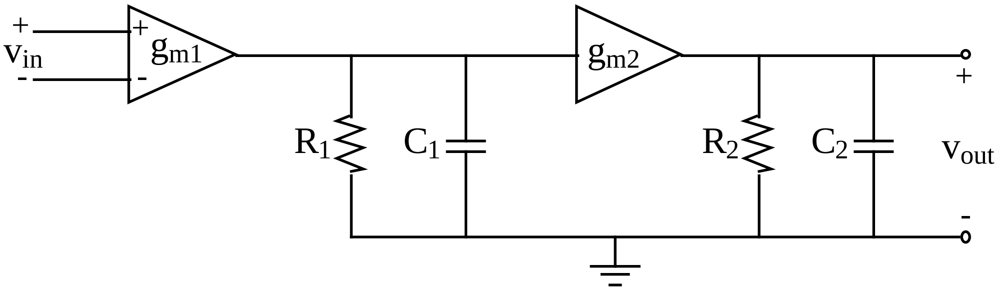
Second order consideration: Charging of C_{sb} of M1 and M2

SIMULATION OF THE PROPAGATION DELAY



```
COMPARATOR PROPAGATION DELAY
VDD 10 0 DC 5V
VSS 11 0 DC -5V
VN 1 0 DC 0V
VP 2 0 PULSE(-1 1 0N 1N 1N 500N 1U)
M1 3 1 5 5 MNMOS W=20U L=10U
M2 6 2 5 5 MNMOS W=20U L=10U
M3 3 3 10 10 MPMOS W=10U L=10U
M4 6 3 10 10 MPMOS W=10U L=10U
M5 5 8 11 11 MNMOS W=10U L=10U
M6 9 6 10 10 MPMOS W=40U L=10U
M7 9 8 11 11 MNMOS W=20U L=10U
M8 8 8 11 11 MNMOS W=10U L=10U
CL1 6 0 0.3PF
CL2 9 0 10PF
IS 0 8 DC 20UA
.MODEL MNMOS NMOS VTO=1 KP=17U
+LAMBDA=0.015 GAMMA=0.8 PHI=0.6
.MODEL MPMOS PMOS VTO=-1 KP=8U
+LAMBDA=0.02 GAMMA=0.4 PHI=0.6
.TRAN 2N 300N
.PRINT TRAN V(6) V(9) V(2)
.PROBE
.END
```

SMALL SIGNAL PERFORMANCE



$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{A_o\omega_{p1}\omega_{p2}}{(s+\omega_{p1})(s+\omega_{p2})}$$

$$\omega_{p1} = \frac{1}{R_1C_1}$$

$$\omega_{p2} = \frac{1}{R_2C_2}$$

$$A_o = g_{m1}g_{m2}R_1R_2$$

Example - (Fig 7.3-4)

$$I_5 = 20\mu A \text{ ‘ } R_1 = \frac{1}{g_{ds2}+g_{ds4}} = \frac{1}{10\mu A} = 3.33M\Omega$$

$$\omega_{p1} = \frac{1}{(0.3pF)(3.33M\Omega)} = 1Mrps$$

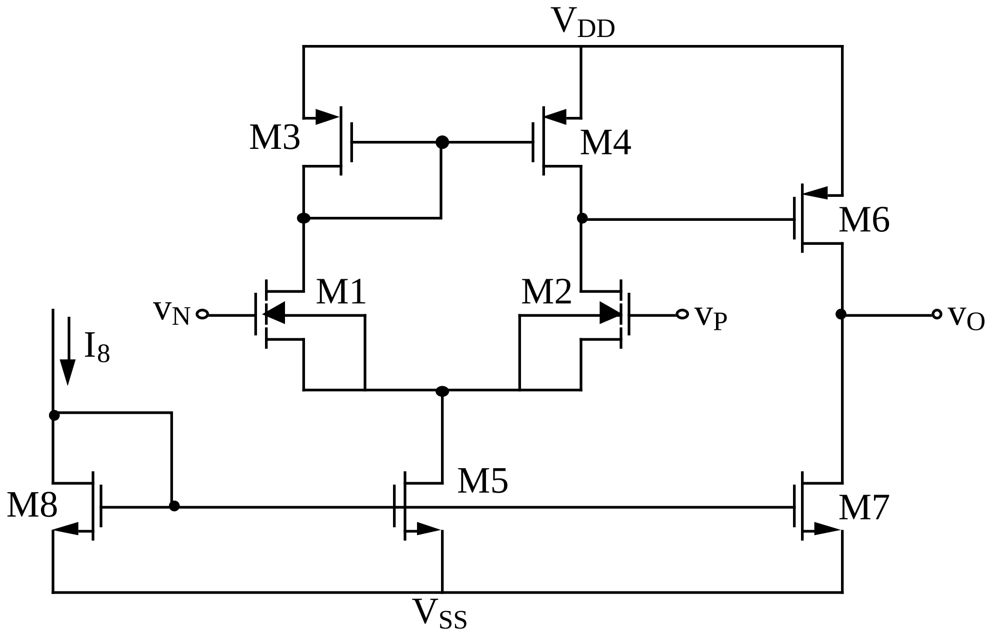
$$I_7 = 40\mu A \text{ ‘ } R_2 = \frac{1}{g_{ds6}+g_{ds7}} = \frac{1}{40\mu A(.03)} = 833K\Omega$$

$$\omega_{p2} = \frac{1}{(10pF)(833K\Omega)} = 120Krps$$

$$g_{m1} = 26\mu s,\ g_{m2} = 50.6\mu s \text{ ‘ } \underline{\underline{A_o = 1099}}$$

TWO-STAGE, CMOS COMPARATOR

General Schematic



Key Relationships for Design:

$$\boxed{i_D = \frac{\beta}{2}(v_{GS} - V_T)^2} \quad \Rightarrow \quad i_D(\text{sat}) = \frac{\beta}{2}\,[v_{DS}(\text{sat})]^2$$

or

$$\boxed{v_{DS}(\text{sat}) = \sqrt{\frac{2i_D(\text{sat})}{\beta}}}$$

Also,

$$\boxed{g_m = \sqrt{2\beta I_D}}$$

where

$$\beta = \frac{KW}{L}$$

COMPARATOR DESIGN PROCEDURE

1. Set the output current to meet the slew rate requirements.

$$i = C\frac{dV}{dt}$$

2. Determine the minimum sizes for M6 and M7 for the proper ouput voltage swing.

$$v_{DS}(sat) = \sqrt{\frac{2I_D}{\beta}}$$

3. Knowing the second stage current and minimum device size for M6, calculate the second stage gain.

$$A_2 = \frac{-g_{m6}}{g_{ds6} + g_{ds7}}$$

4. Calculate the required first stage gain from A_2 and gain specifications.

5. Determine the current in the first stage based upon proper mirroring and minimum values for M6 and M7. Verify that P_{diss} is met.

6. Calculate the device size of M1 from A_1 and I_{DS1}.

$$A_1 = \frac{-g_{m1}}{g_{ds1} + g_{ds3}} \quad \text{and} \quad g_{m1} = \sqrt{\frac{2K'W/L}{I_{DS1}}}$$

7. Design minimum device size for M5 based on negative CMR requirement using the following ($I_{DS1} = 0.5I_{DS5}$):

$$v_{G1}(min) = V_{SS} + V_{DS5} + \sqrt{\frac{I_{DS5}}{\beta_1}} + V_{T1}(max)$$

$$\text{where } V_{DS5} = \sqrt{\frac{2I_{DS5}}{\beta_5}} = V_{DS5}(sat)$$

8. Increase either M5 or M7 for proper mirroring.

9. Design M4 for proper positive CMR using:

$$v_{G1}(max) = V_{DD} - \sqrt{\frac{I_{DS5}}{\beta_3}} - |V_{TO3}|(max) + V_{T1}$$

10. Increase M3 or M6 for proper mirroring.

11. Simulate circuit.

DESIGN OF A TWO-STAGE COMPARATOR

Specifications:

$A_{vo} > 66$ dB Lambda $= 0.05\text{V}^{-1}$ (L = 5 μm)

$P_{diss} < 10$ mW $V_{DD} = 10$ V

$C_L = 2$ pF $V_{SS} = 0$ V

$t_{prop} < 1$ μs Recall that $\beta = \dfrac{K'W}{L}$

CMR = 4-6 V

Output swing is V_{DD} - 2V and V_{SS} + 2V

1). For $t_{prop} << 1$ μs choose slew rate at 100 V/μs

$$\therefore\ I_7 = C_L\frac{dv_{OUT}}{dt} = (2\cdot 10^{-12})(100\cdot 10^{-6}) = 200\ \mu\text{A}$$

2). Size M6 and M7 to get proper output swing,

M7:

$$2\text{V} > v_{DS7}(\text{sat}) = \sqrt{\frac{2I_7}{\beta_7}} = \sqrt{\frac{2(200\mu\text{A})}{17.0\mu\text{A/V}^2(W_7/L_7)}} \rightarrow \underline{\underline{\frac{W_7}{L_7} > 5.88}}$$

M6:

$$2\text{V} > v_{DS6}(\text{sat}) = \sqrt{\frac{2(I_{OUT}+I_7)}{\beta_6}} = \sqrt{\frac{2(400\mu\text{A})}{8.0\mu\text{A/V}^2(W_6/L_6)}} \rightarrow \underline{\underline{\frac{W_6}{L_6} > 12.5}}$$

3). $$A_2 = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \left(\frac{-1}{\lambda_N + \lambda_P}\right)\sqrt{\frac{2K_P'W_6}{I_6L_6}} \approx -10$$

4). $A_{vo} = A_1A_2 = 66$ dB $\approx 2000 \rightarrow A_1 = 200$

COMPARATOR DESIGN - CONT'D

5). Assuming $v_{GS4} = v_{GS6}$, then $I_4 = \frac{S_4}{S_6}\ I_6$

choose $S_4 = 1$ which gives $I_4 = \frac{1}{12.5}(200\mu A) = 16.0\ \mu A$

Assume $S_5 = 1$ which gives $I_5 = \frac{S_5}{S_7}\ I_7 = \frac{200\mu A}{5.88} = 34\ \mu A$

and $I_4 = \frac{1}{2}\ I_5 = 17\ \mu A$

Choose $\underline{\underline{I_4 = 17\ \mu A}}$ to keep $\frac{W}{L}$ ratios greater than 1.

$\therefore\ I_5 = 34\ \mu A \qquad \frac{W_4}{L_4} = \frac{W_6}{L_6}\left(\frac{17}{200}\right) = 1.06 \approx 1.0$

$P_{diss} = 10(I_7 + I_5) = 2.34\text{ mW} < 10\text{ mW}$

6). $A_1 = \frac{1}{\lambda_1 + \lambda_4}\sqrt{\frac{2K_N'W_1}{I_4L_1}} \rightarrow \frac{W_1}{L_1} = [(\lambda_1 + \lambda_4)A_1]^2\ \frac{I_4}{2K_N'} = 200$

$\therefore\ \underline{\underline{\frac{W_1}{L_1} = 200}}$ (Good for noise)

7). $V_{DS5} = v_{G1}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max)$

$V_{DS5} = 4 - 0 - \sqrt{\frac{(34)}{2(17.0)(200)}} -1 = 2.90\text{ V}$

$V_{DS5} = \sqrt{\frac{2I_5}{\beta_5}} = \sqrt{\frac{2(34\mu)}{(17\mu)S_5}} \rightarrow \frac{W_5}{L_5} > 0.48$

8). $S_5 = \frac{I_5}{I_7}\ S_7 = \frac{34}{200}(5.88) = 1.0 \rightarrow \underline{\underline{\frac{W_5}{L_5} = 1.0}}$

COMPARATOR DESIGN - CONT'D

9). $V_{G1}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - \left|V_{TO3}\right|(\max) + V_{T1}(\min)$

$$\beta_3 = \frac{I_5}{\left[V_{DD} - V_{G1}(\max) - \left|V_{TO3}\right|(\max) + V_{T1}(\min)\right]^2}$$

$$= \frac{34\ \mu A}{(10 - 6 - 1 + 0.5)^2} = 2.76 \cdot 10^{-6}$$

$$\therefore \frac{W_3}{L_3} = \frac{(2.76)(2)}{8} = 0.69 \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} > 0.69$$

(Previously showed $\frac{W_4}{L_4} > 1.06$ so no modification is necessary)

10). Summary

$$W_{drawn} = \left(\frac{W}{L}\right)(L - 1.6)$$

Design Ratios	Actual Values with 5µm minimum geometry	Proper Mirroring and L_D = 0.8µm
$\frac{W_1}{L_1} = \frac{W_2}{L_2} = 200$	$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{1000}{5}$	$\frac{680}{5}$
$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 1.0$	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{5}{5}$	$\frac{3.4}{5}$ ‘ $\frac{5}{5}$
$\frac{W_5}{L_5} = 1.0$	$\frac{W_5}{L_5} = 1.0$	$\frac{3.4}{5}$ ‘ $\frac{5}{5}$
$\frac{W_6}{L_6} = 12.5$	$\frac{W_6}{L_6} = \frac{62.5}{5}$	$\frac{60}{5}$
$\frac{W_7}{L_7} = 5.88$	$\frac{W_7}{L_7} = \frac{30}{5}$	$\frac{30}{5}$

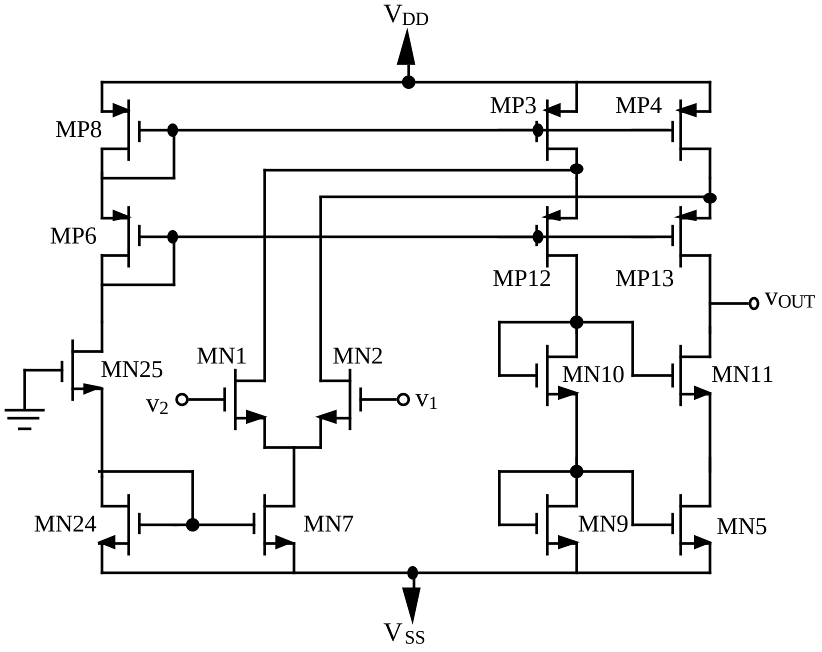
↑

(Need to adjust for proper mirroring) ⇒ $\frac{S_6}{S_4} = 2\,\frac{S_7}{S_5}$

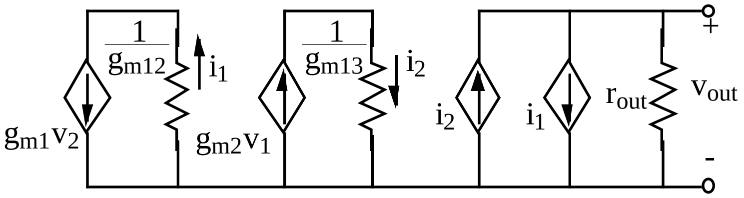
VII.4 - OTHER TYPES OF COMPARATORS

FOLDED CASCODE CMOS COMPARATOR

Circuit Diagram



Small Signal Model



where

$$R_{out} \approx (r_{ds5}g_{m11}r_{ds11})||((r_{ds4}||r_{ds2})g_{m13}r_{ds13}) =$$

$$= \frac{1}{\frac{g_{ds5}g_{ds11}}{g_{m11}} + \frac{(g_{ds2}+g_{ds4})g_{ds13}}{g_{m13}}}$$

The small signal voltage gain is

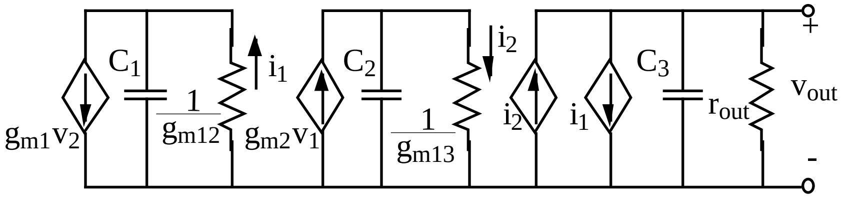
$$v_{out} = r_{out}(i_2 - i_1) = (g_{m2}+g_{m1})R_{out}v_{in} = \left(\frac{g_{m1}+g_{m2}}{\frac{g_{ds5}g_{ds11}}{g_{m11}} + \frac{(g_{ds2}+g_{ds4})g_{ds13}}{g_{m13}}} \right) v_{in}$$

where $v_{in} = v_1 - v_2$.

FOLDED CASCODE CMOS COMPARATOR - CONTINUED

Frequency Response

Small signal model-



where

$$C_1 = C_{GS12} + C_{BS12} + C_{DG3} + C_{BD3}$$

$$C_2 = C_{GS13} + C_{BS13} + C_{DG4} + C_{BD4}$$

and $$C_3 = C_{DG11} + C_{BD11} + C_{DG13} + C_{BD13} + C_{Load}$$

$$A_{VD}(s) \approx \frac{A_{VD0}\omega_3}{s + \omega_3}$$

where

$$\omega_3 = \frac{1}{r_{out}C_3}$$

Typical performance-

$I_{D1} = I_{D2} = 50\mu A$ and $I_{D3} = I_{D4} = 100\mu A$, $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_{11}}{L_{11}} = \frac{W_{13}}{L_{13}}$ $=1$, assume $C_3 \approx 0.5pF$, and using the values of Table 3.1-2 gives:

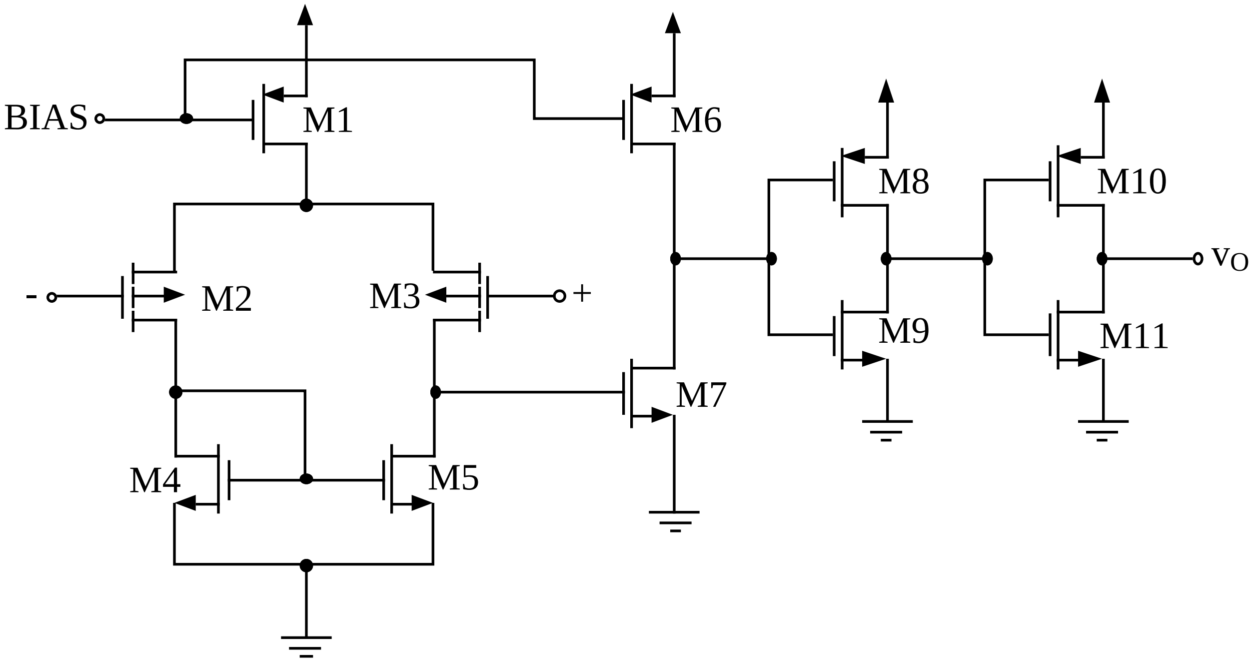
$$g_{m1} = g_{m2} = g_{m11} = 41.2\mu S \qquad g_{m13} = 28.3\mu S$$

$$g_{ds5} = g_{ds11} = 0.5\mu S \qquad g_{ds4} = g_{ds13} = 0.25\mu S$$

Therefore, $r_{out} = 121M\Omega$, $\omega_3 = 16.553$krps, and $A_{VD0} = 4{,}978$ resulting in a gain-bandwidth of 13.11MHz.

$$\text{Delay} = \Delta T = \frac{C_3\Delta V}{I_{max}} = \frac{0.5pF\text{x}10V}{100\mu A} = 50nS$$

OPEN LOOP COMPARATOR - MC 14575



Performance (I_{SET} = 50 μA)

$\frac{\text{Rise time}}{\text{Fall time}}$ = 100 ns into 50 pF

Propagation delay = 1 μs

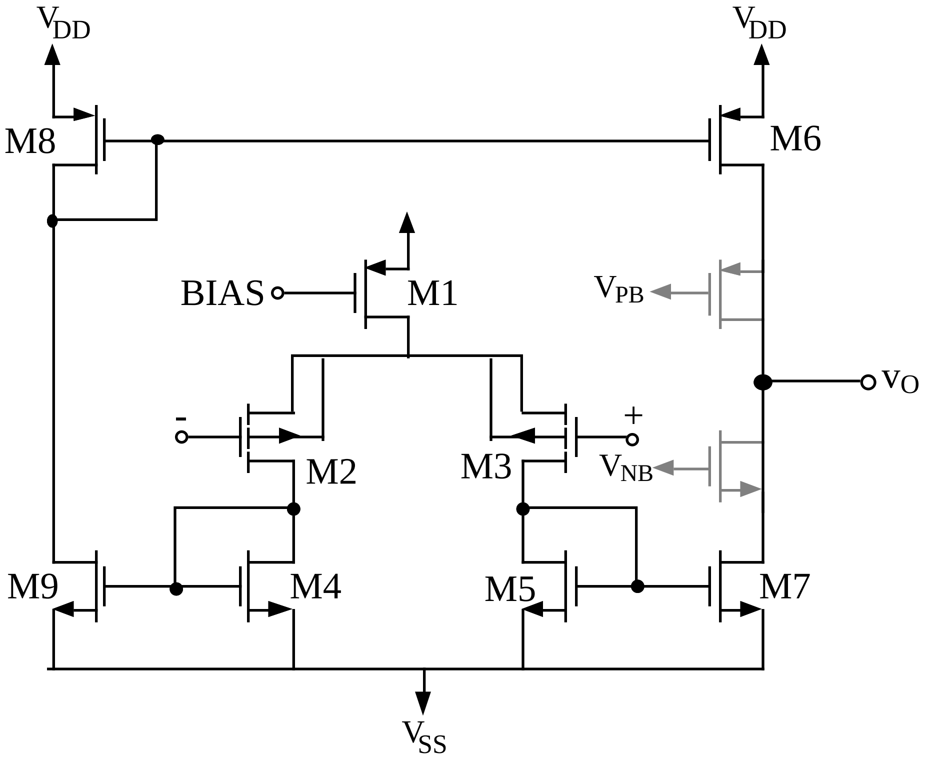
Slew rate = 2.7 Volts/μs

Loop Gain = 32,000

Comments

The inverter pair of M8-M9 and M10-M11 are for the purpose of providing an output drive capability and minimizing the propagation delay.

CLAMPED CMOS VOLTAGE COMPARATOR



Drain of M2 and M3 clamped to the gate voltages of M4 and M5.

M6 and M7 provide a current, push-pull output drive capability similiar to the current , push-pull CMOS OP amp.

Comparator is really a voltage comparator with a current output.

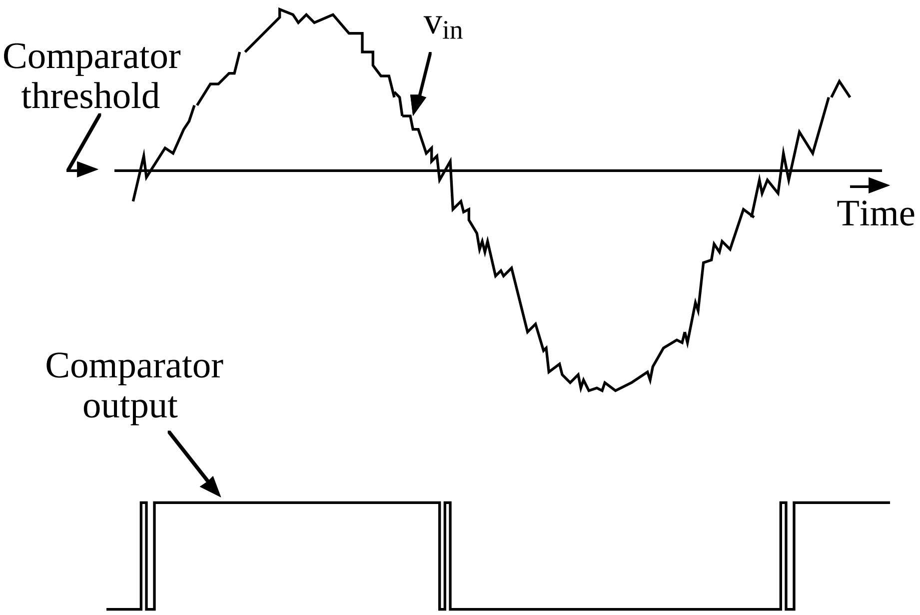
VII.5 - COMPARATORS WITH HYSTERESIS

HYSTERESIS

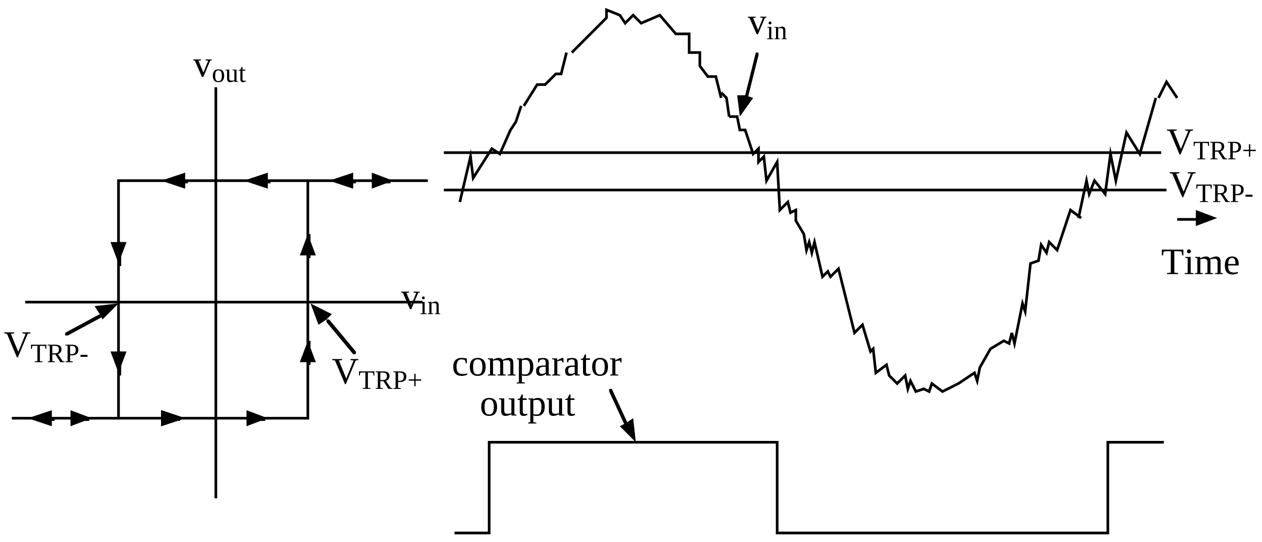
Why Hysteresis?

Eliminates "chattering" when the input is noisy.

Comparator with no Hysteresis

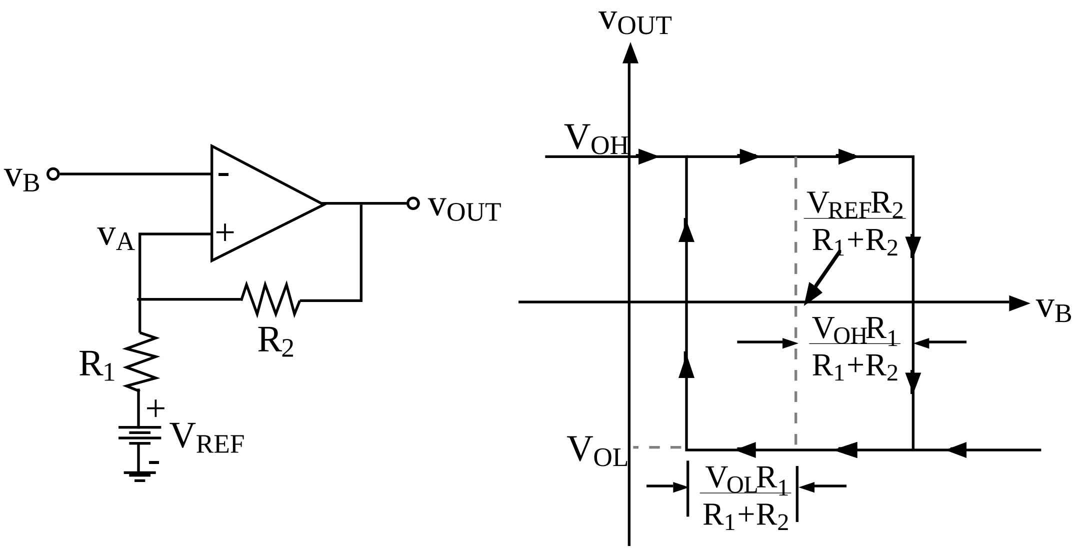


Comparator with Hysteresis

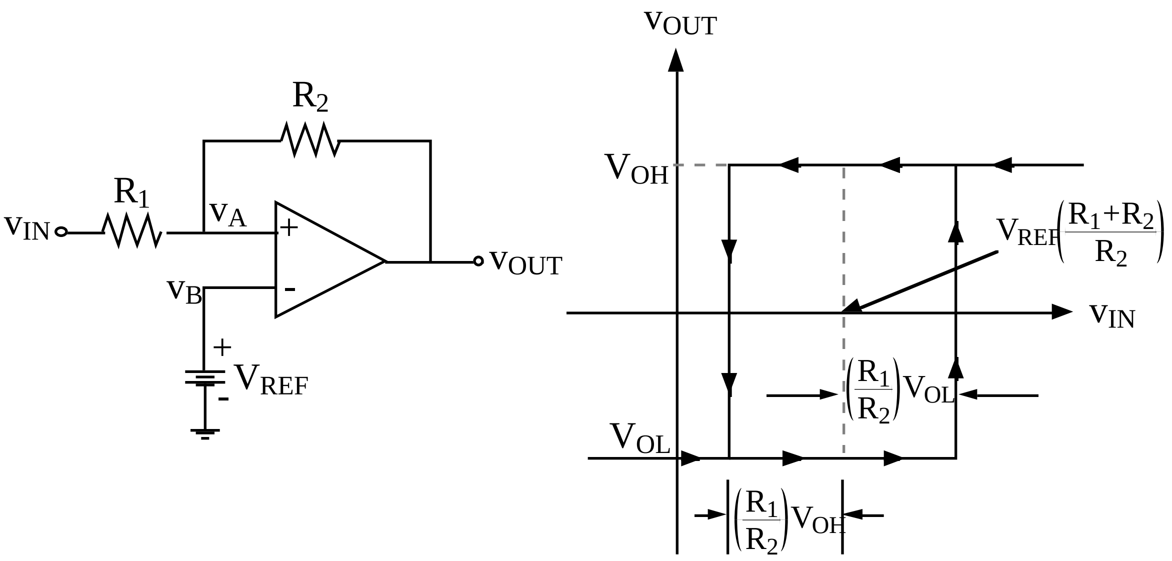


VOLTAGE COMPARATORS USING EXTERNAL FEEDBACK

Inverting

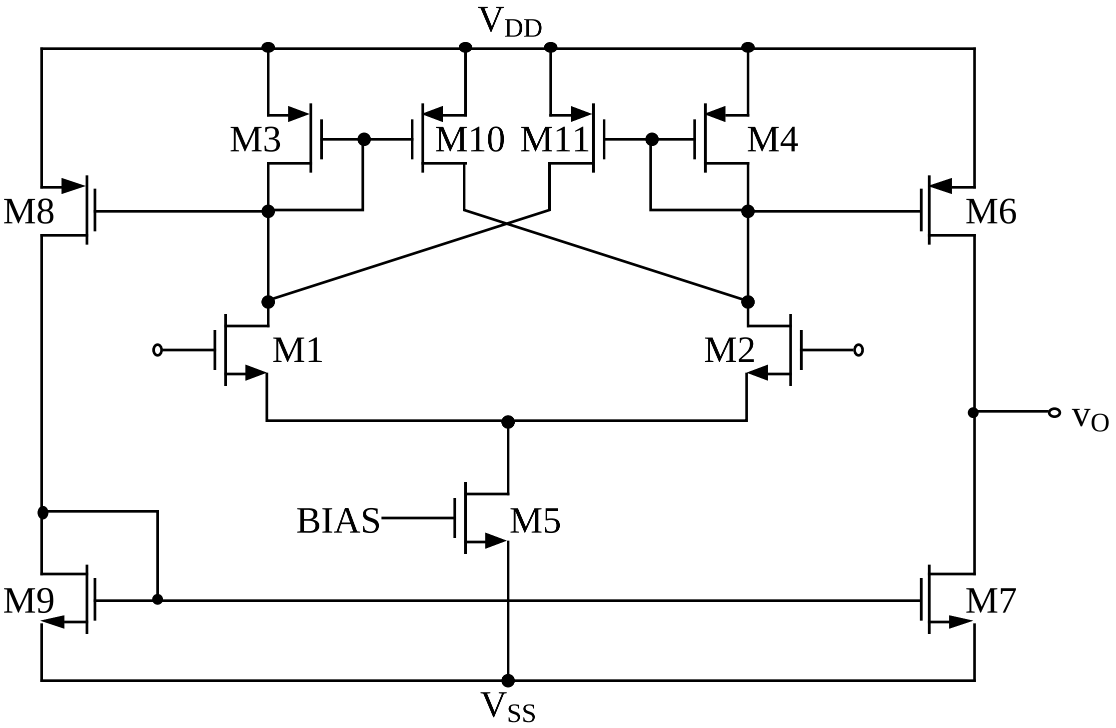


Noninverting



COMPARATORS WITH INTERNAL FEEDBACK

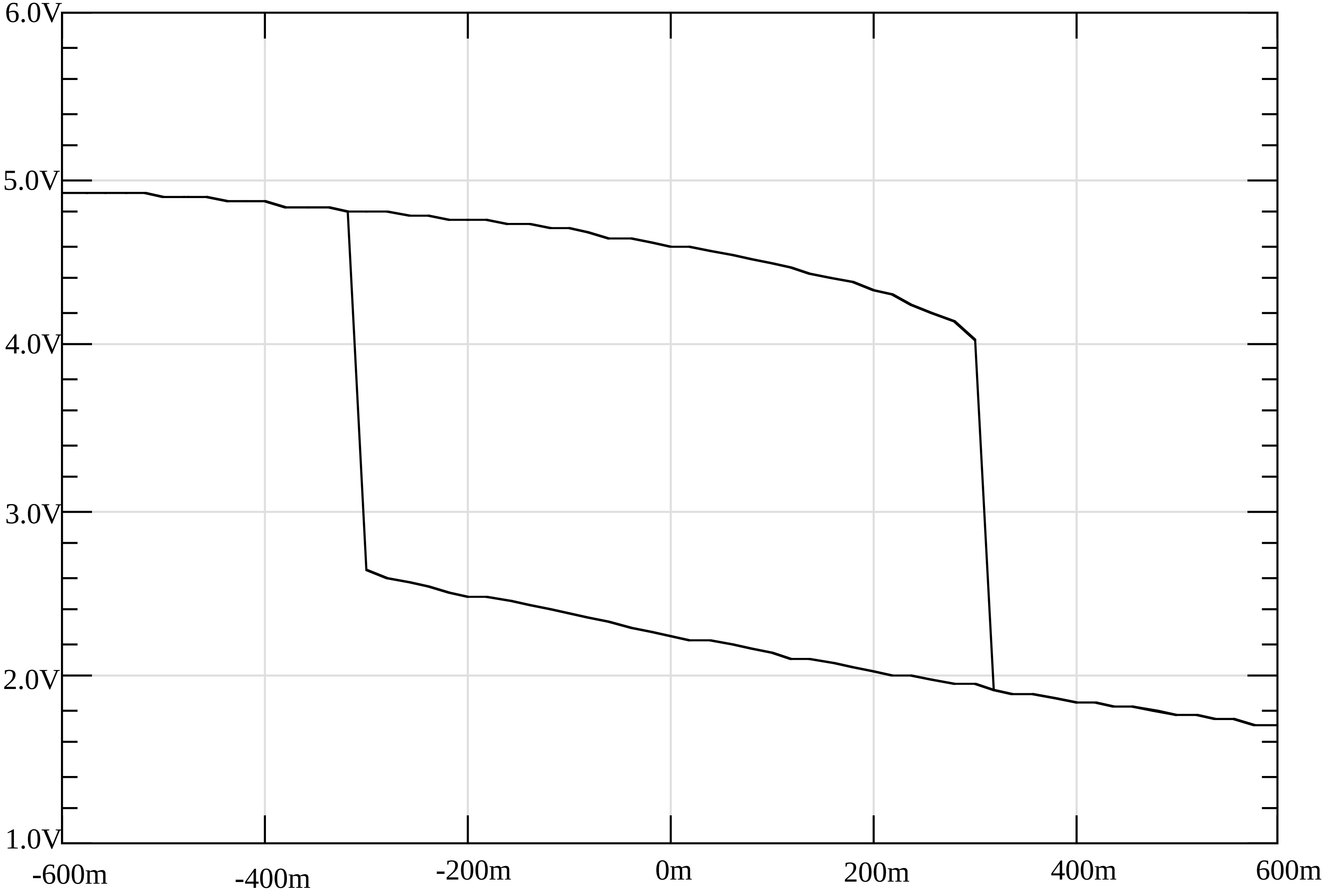
Cross-Coupled Bistable



(1). Positive feedback gives hysteresis.

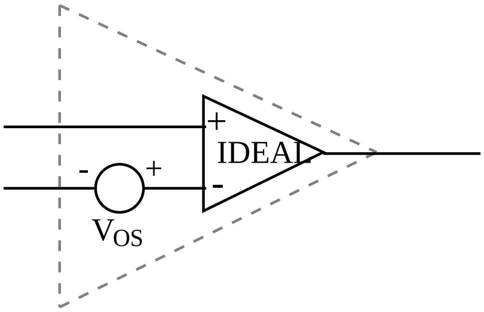
(2). Also speeds up the propagation delay time.

EXAMPLE 7.4-1 COMPARATOR WITH HYSTERESIS

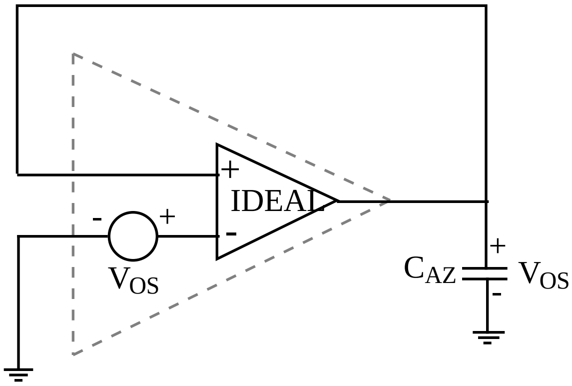


AUTO ZEROING OF VOLTAGE COMPARATORS

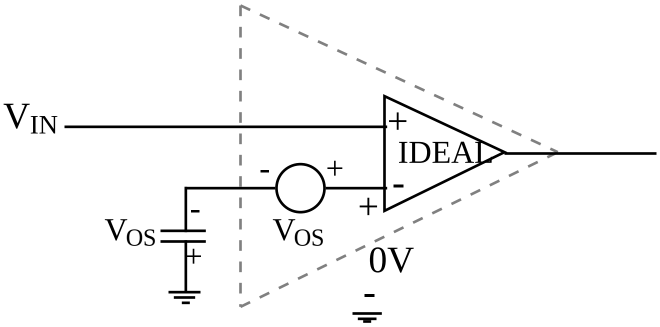
Model of the Comparator Including Offset



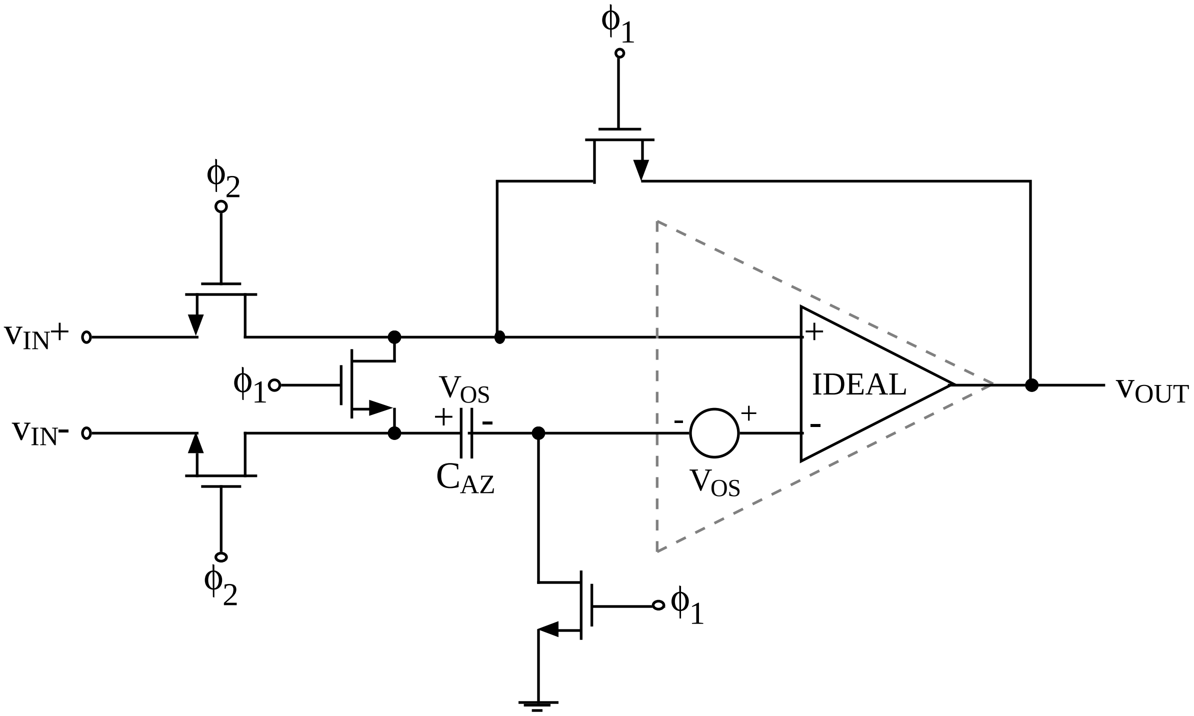
Auto Zero Scheme-First Half of Cycle



Auto Zero Scheme-Second Half of Cycle

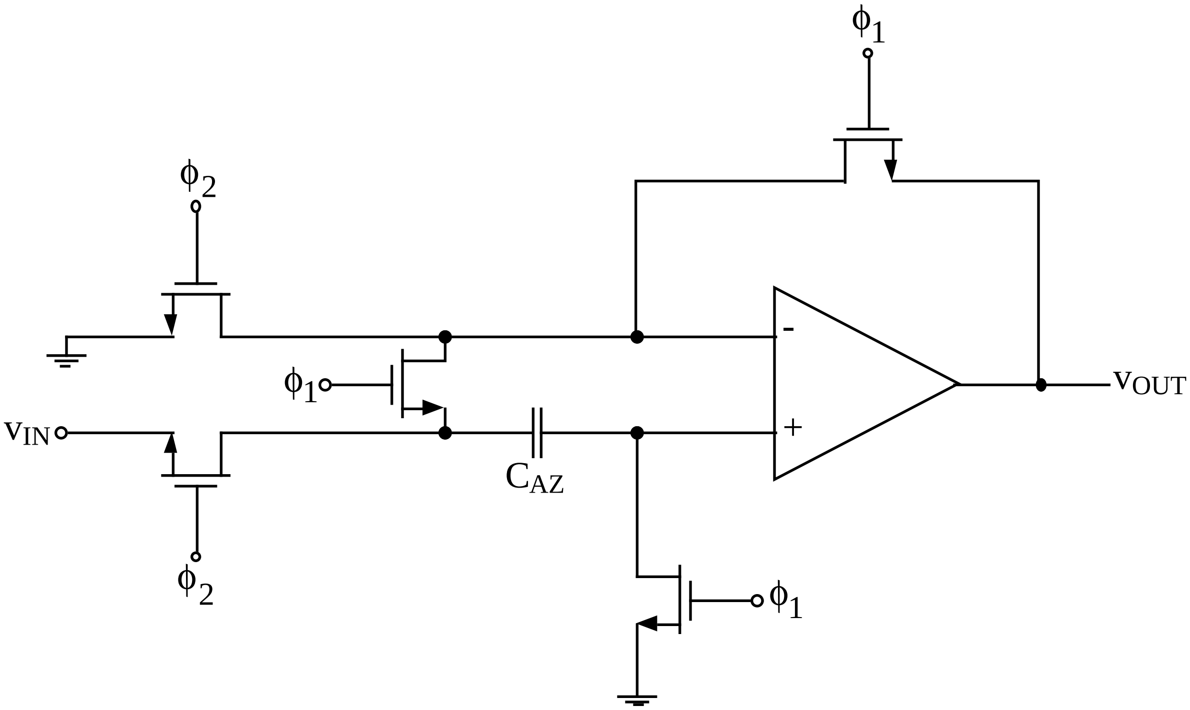


GENERALIZED AUTO ZERO CONFIGURATION

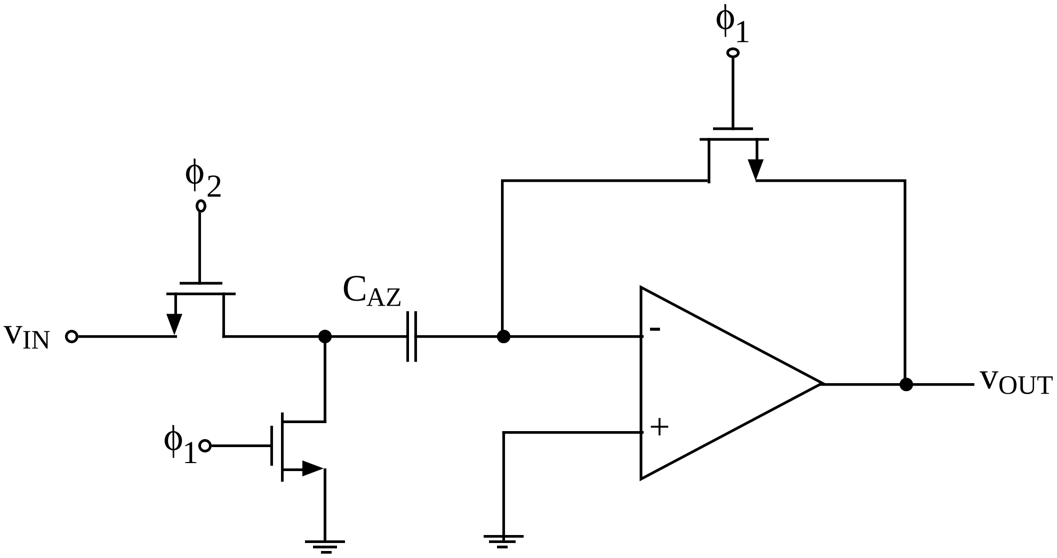


Good for inverting or noninverting when the other terminal is not on ground.

Noninverting Auto-Zeroed Comparator



Inverting Auto-Zeroed Comparator

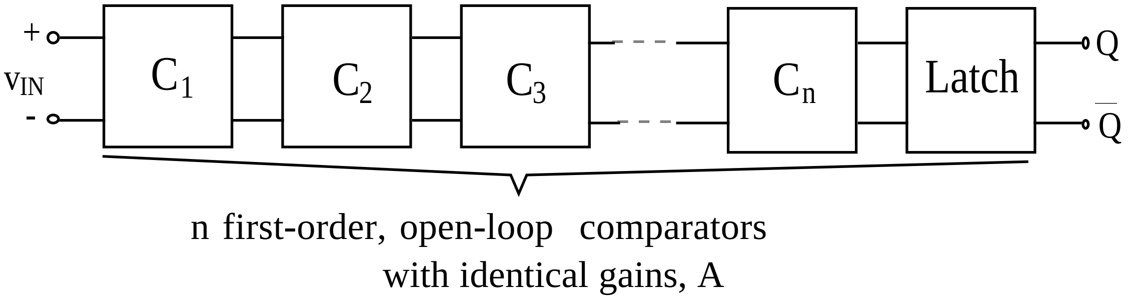


Use nonoverlapping, two-phase clock.

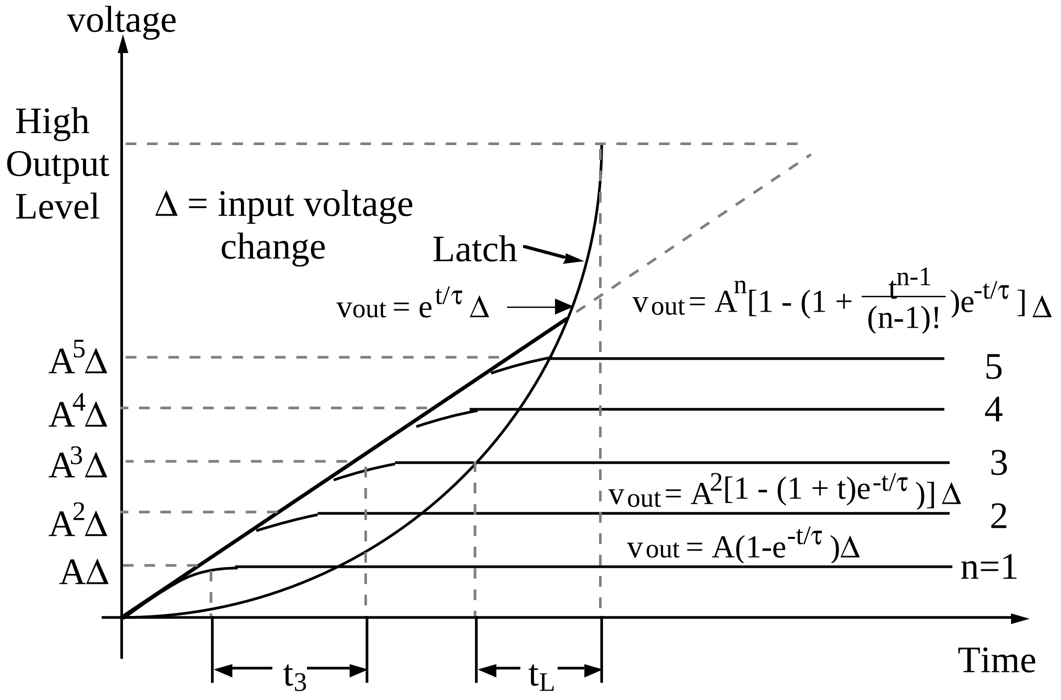
VII.6 - HIGH SPEED COMPARATORS

Concept

Question: For a given input change, what combination of first-order open-loop comparators and a latch gives minimum propagation delay?



Concept:



Propagation delay time = $t_3 + t_L$ for n=3

Answer:

t_p(min) occurs when n=6 and A=2.72=e

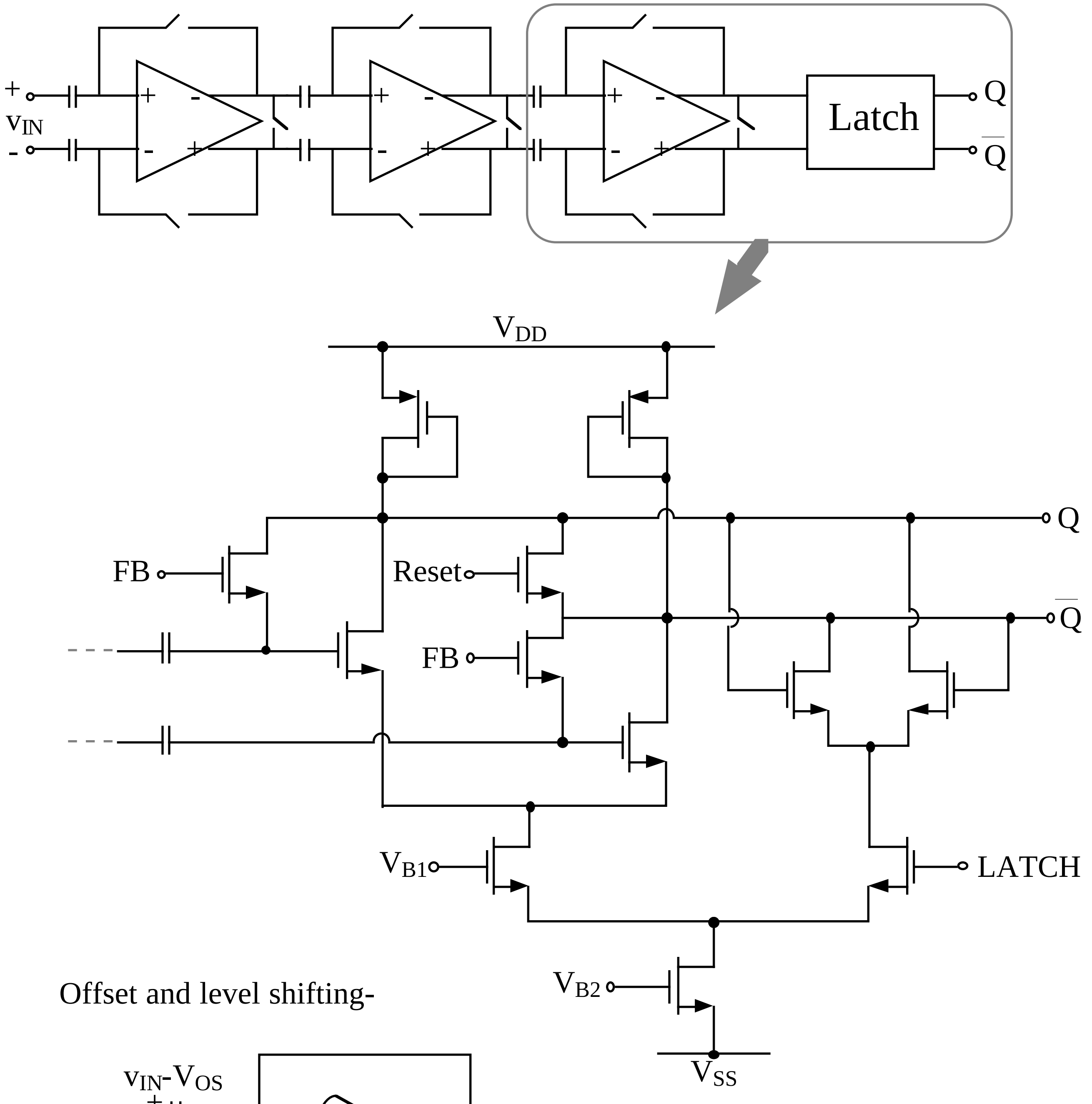
Implementation:

n=3 and A≈6 gave nearly the same result with less area.

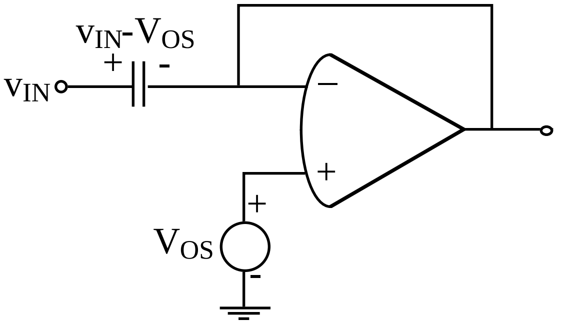
[Ref: Doernberg et al., “A 10-bit 5 MSPS CMOS Two-Step FLASH ADC”JSSC April 1989 pp 241-249]

HIGH SPEED COMPARATORS-CONT'D

Conceptual Implementation-



Offset and level shifting-



VII.7 - COMPARATOR SUMMARY

- Key performance parameters:
  - Propagation time delay
  - Resolving capability
  - Input common mode swing
  - Input offset voltage
- Types of comparators:
  - Open loop
  - Regenerative
  - Open loop and regenerative
  - Charge balancing
- Open loop comparator needs differential input and second stage
- Systemative offset error is offset (using perfectly matched transistors) that is due to current mirror errors.
- For fast comparators, keep all node swings at a minimum except for the output (current comparators?).
- Key design equations:

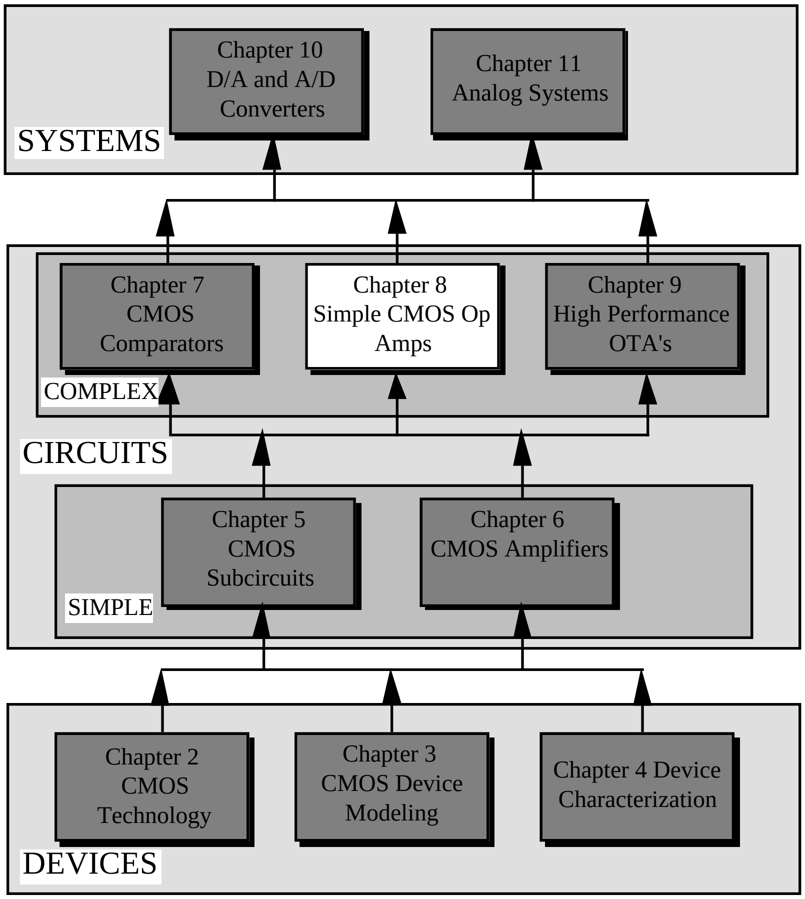
$$i_D = \frac{KW}{2L}(v_{GS}-V_T)^2, \quad v_{DS}(sat) = \sqrt{\frac{2i_D}{K(W/L)}}, \text{ and } g_m = \sqrt{\frac{2KWI_D}{L}}$$

- Positive feedback is used for regenerative comparators.
- Use autozeroing to remove offset voltages (charge injection is limit).
- Fastest comparators using low-gain, fast open loop amplifiers cascaded with a latch.

VIII. SIMPLE CMOS OPERATIONAL AMPLIFIERS (OP AMPS) AND OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS (OTA'S)

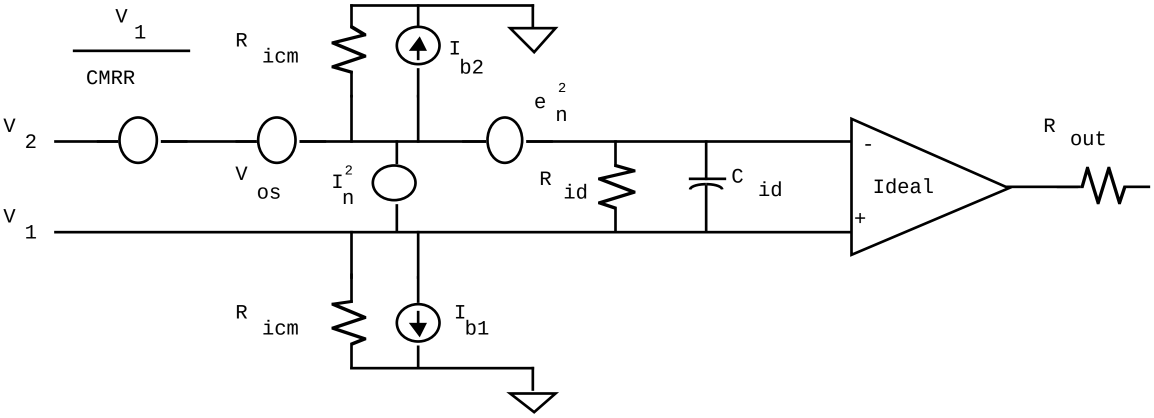
Contents

Organization



Op Amp Characteristics

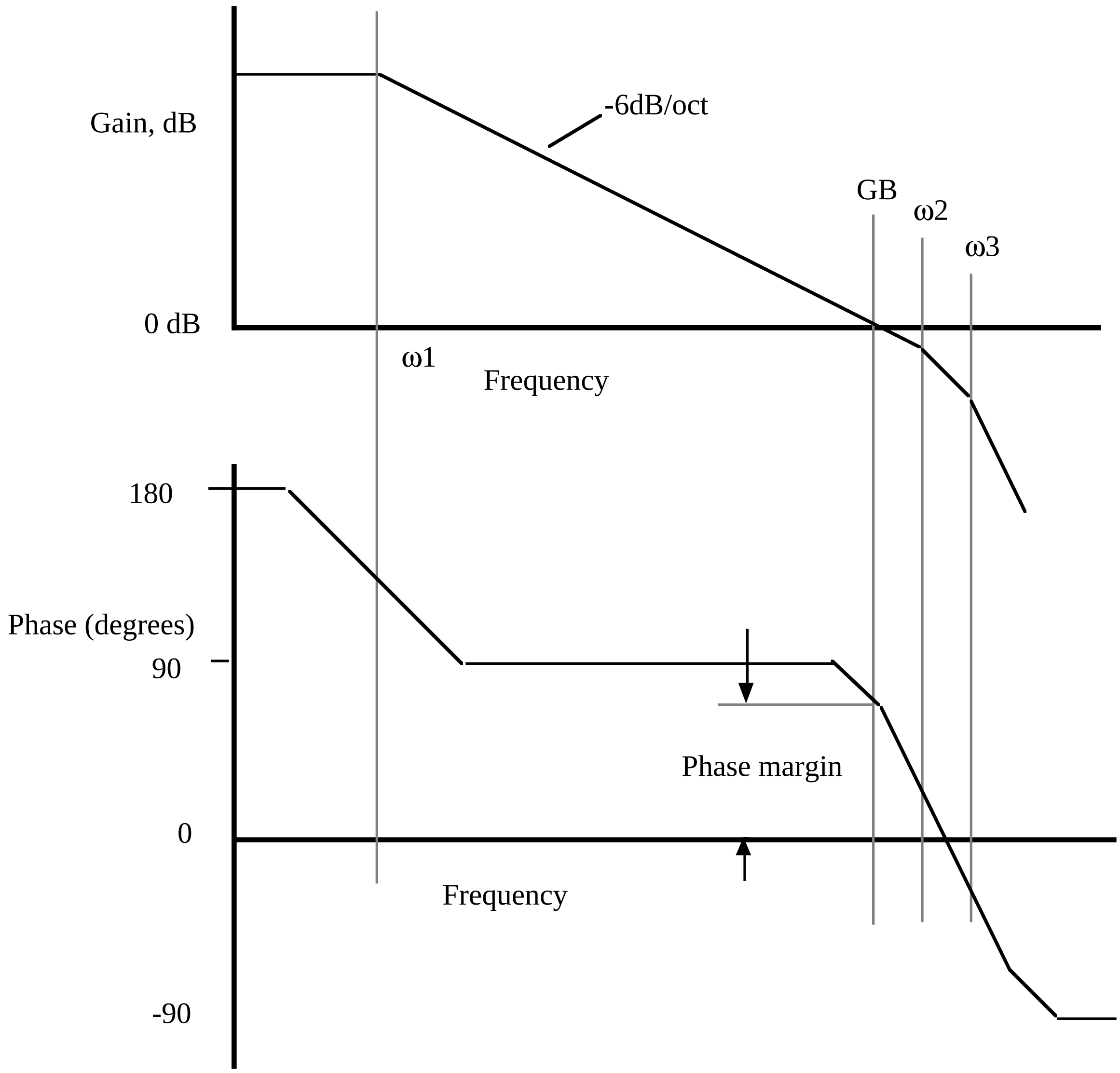
Non-ideal model for an op amp



Boundary Conditions	Requirement
Process Specification	See Tables 3.1-1 and 3.1-2
Supply Voltage	+5 V ±10%
Supply Current	100 μA
Temperature Range	0 to 70°C
Typical Specifications	
Gain	≥ 80 dB
Gainbandwidth	≥ 10 MHz
Settling Time	≤ 0.1 μsec
Slew Rate	≥ 2 V/μsec
Input CMR	≥ ±2 V
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Output Swing	≥ 2 VP-P
Output Resistance	Capacitive load only
Offset	≤ ±5 mV
Noise	≤ 50nV/$\sqrt{\text{Hz}}$ at 1KHz
Layout Area	≤ 10,000 square μm

Frequency Response

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\cdots}$$



Power supply rejection ratio (PSRR):

$$\text{PSRR} = \left(\frac{\Delta V_{DD}}{\Delta v_{OUT}}\right) \cdot A_{vd}(s) = \frac{A_{vd}(s)}{A_{ps}(s)} = \frac{\frac{v_{out}}{v_{in}}(v_{ps}=0)}{\frac{v_{out}}{v_{ps}}(v_{in}=0)}$$

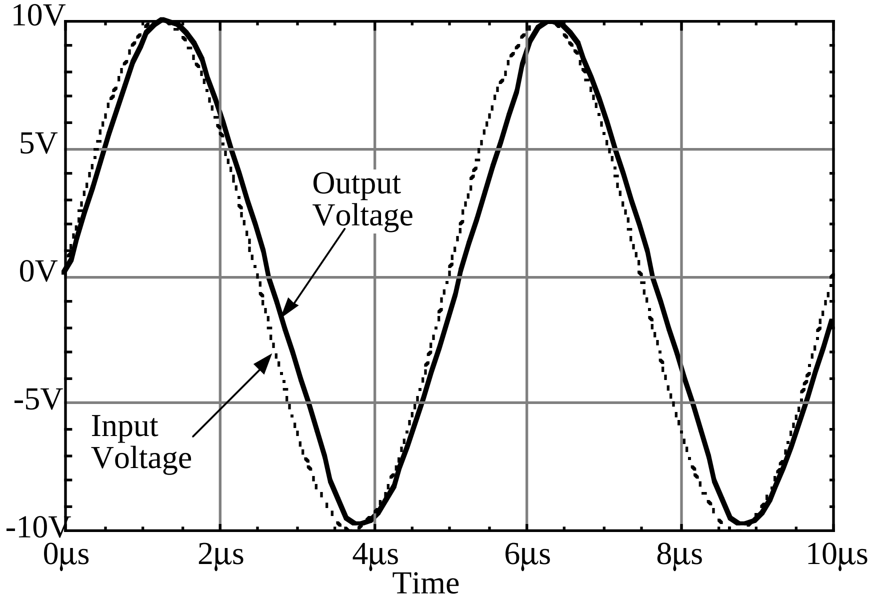
Common-mode input range (ICMR).

Maximum common mode signal range over which the differential voltage gain of the op amp remains constant.

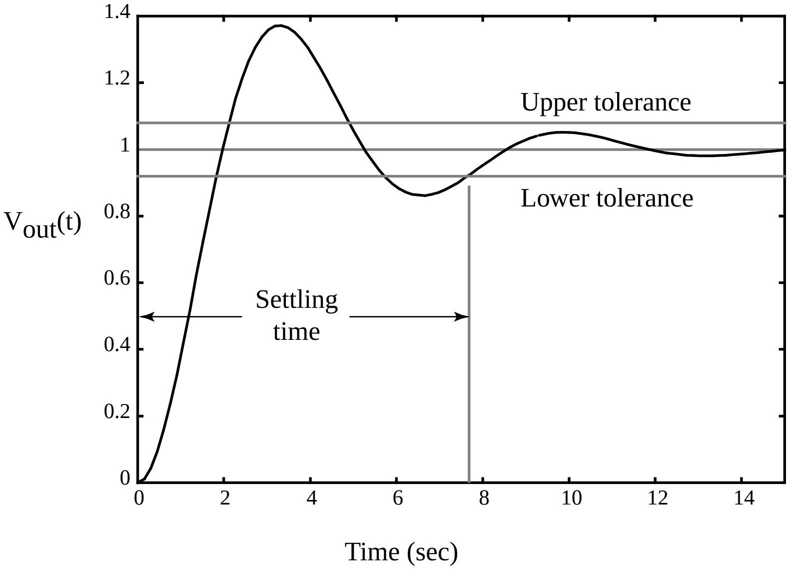
Maximum and minimum output voltage swing.

Slew rate:

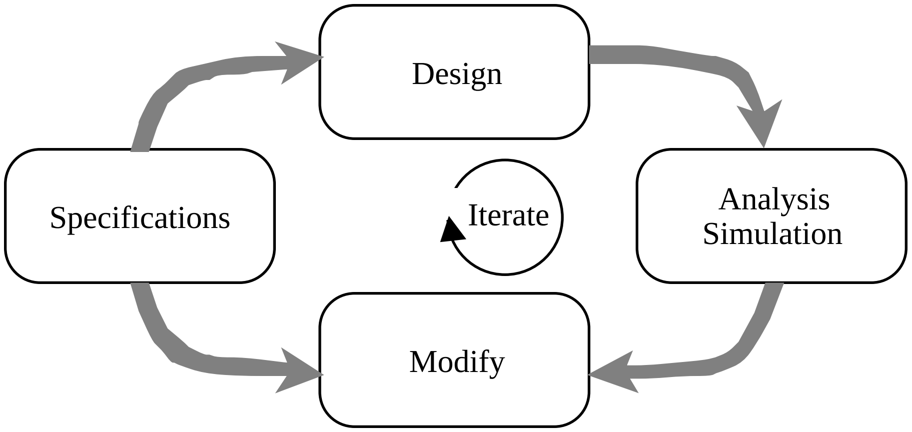
$$\text{Slew rate} = \max\left(\frac{\Delta v_{OUT}}{\Delta t}\right)$$



Settling Time



Design Approach



Specifications:

- Gain
- Output voltage swing
- Settling time
- Power dissipation
- Supply voltage
- Silicon area
- Bandwidth
- PSRR
- CMRR
- Noise
- Common-mode input range

Design Strategy

The design process involves two distinct activities:

Architecture Design

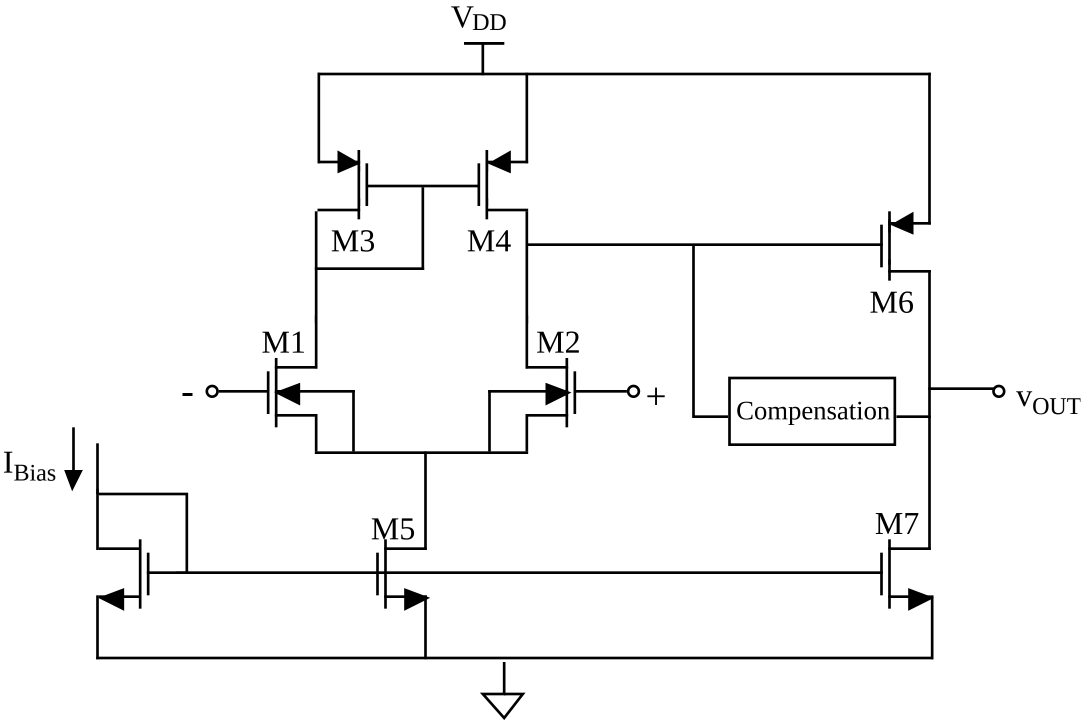
- Find an architecture already available and adapt it to present requirements
- Create a new architecture that can meet requirements

Component Design

- Design transistor sizes
- Design compensation network

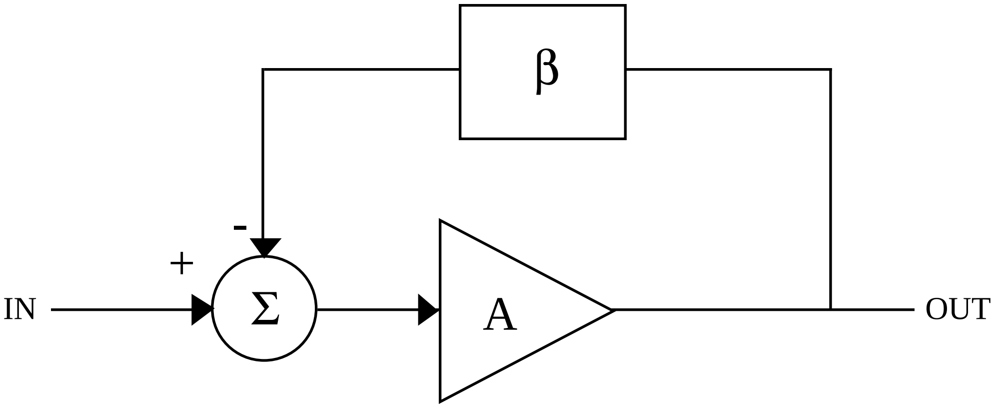
If available architectures do not meet requirements, then an existing architecture must be modified, or a new one designed. Once a satisfactory architecture has been obtained, then devices and the compensation network must be designed.

Op Amp Architecture



Compensation

In virtually all op amp applications, feedback will be applied around the amplifier. Therefore, stable performance requires that the amplifier be compensated. Essentially we desire that the loop gain be less than unity when the phase shift around the loop is greater than 135°

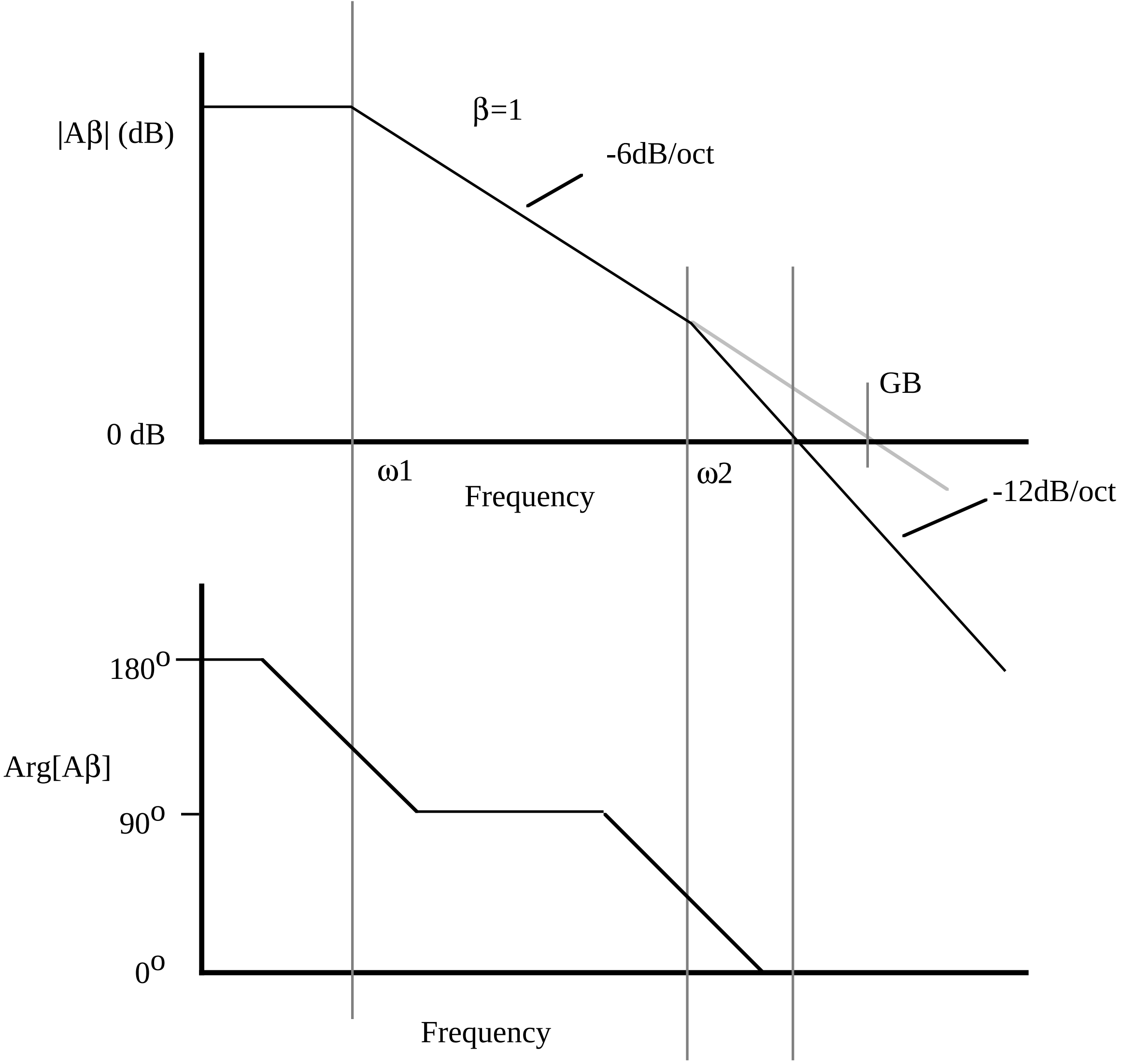


$$\frac{OUT}{IN} = \frac{A}{1 + A\beta}$$

Goal: $1 + A\beta > 0$

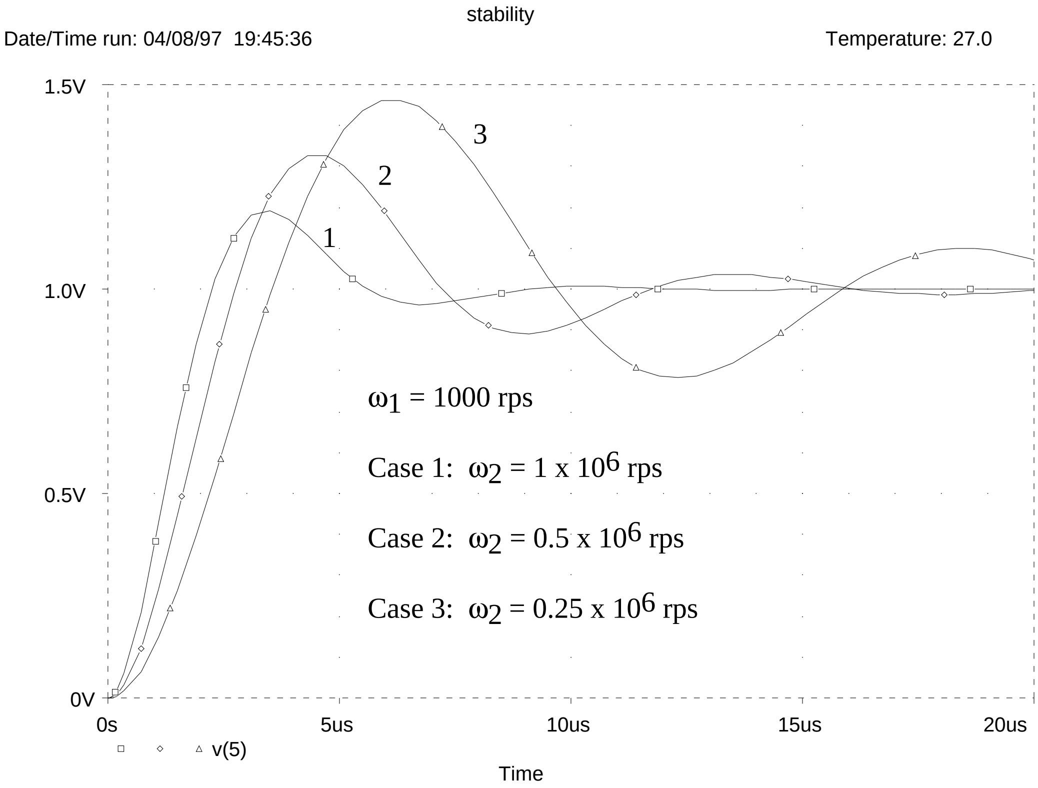
Rule of thumb: $\arg[A\beta] < 135^\circ$ at $\mathrm{mag}[A\beta] = 1$

Graphical Illustration of Stability Requirements



Step Response of Two-Pole System

Impact of placing ω_2 at different locations:



ω_1 = 1000 rps

Case 1: $\omega_2 = 1 \times 10^6$ rps

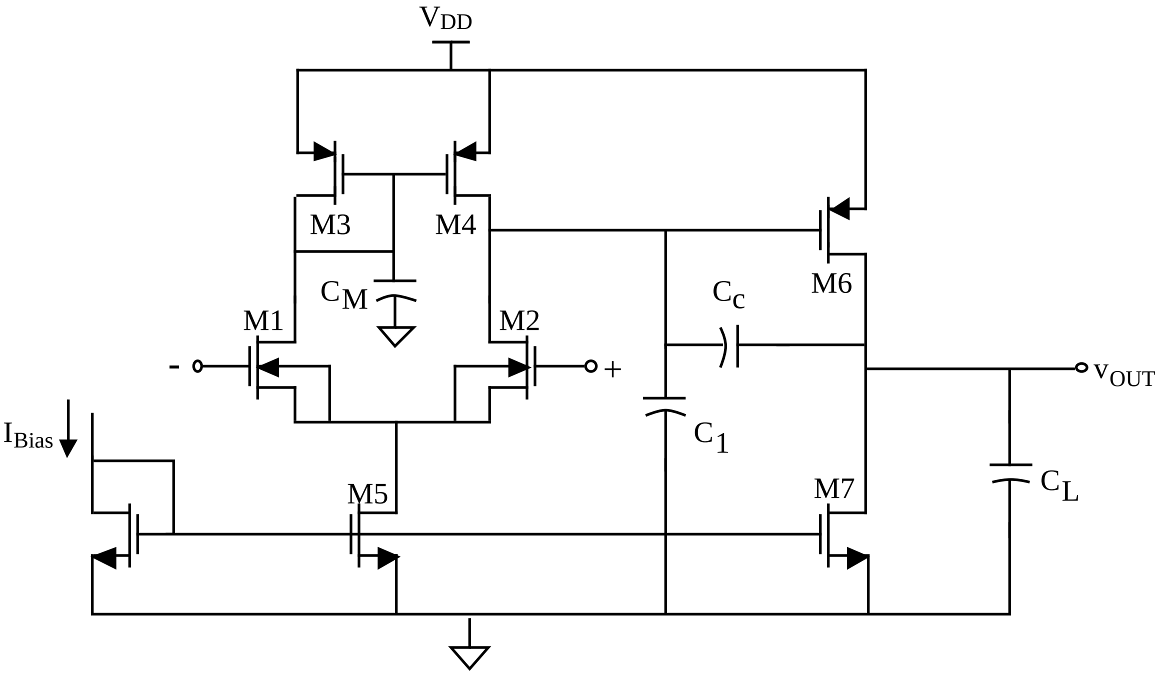
Case 2: $\omega_2 = 0.5 \times 10^6$ rps

Case 3: $\omega_2 = 0.25 \times 10^6$ rps

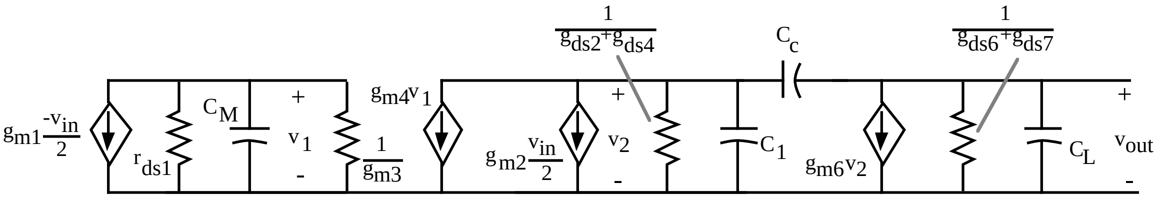
Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
    - Miller capacitor only
    - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
    - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Self compensating - Load capacitor compensates the op amp (later).
3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

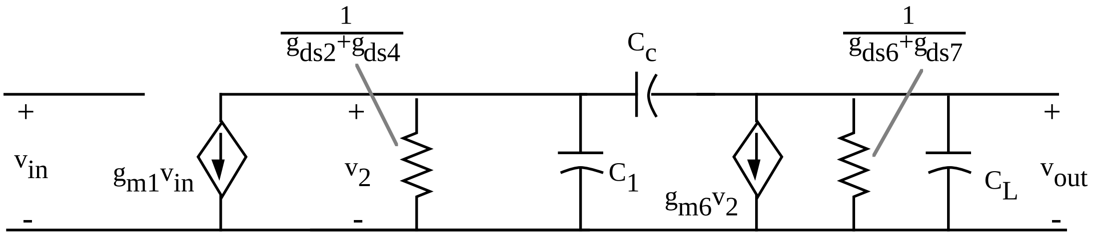
Miller Compensation



Small-signal model



Simplified small-signal model



Analysis

$$\frac{V_o(s)}{V_{\text{in}}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})(1 - sC_c/g_{mII})}{1 + s[R_I(C_1 + C_c) + R_{II}(C_L + C_c) + g_{mII}R_IR_{II}C_c] + s^2R_IR_{II}[C_1C_L + C_c(C_1 + C_L)]}$$

$$p_1 \cong \frac{-1}{g_{mII}\,R_I\,R_{II}\,C_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_1C_L + C_LC_c + C_1C_c}$$

$$p_2 \cong \frac{-g_{mII}}{C_L}$$

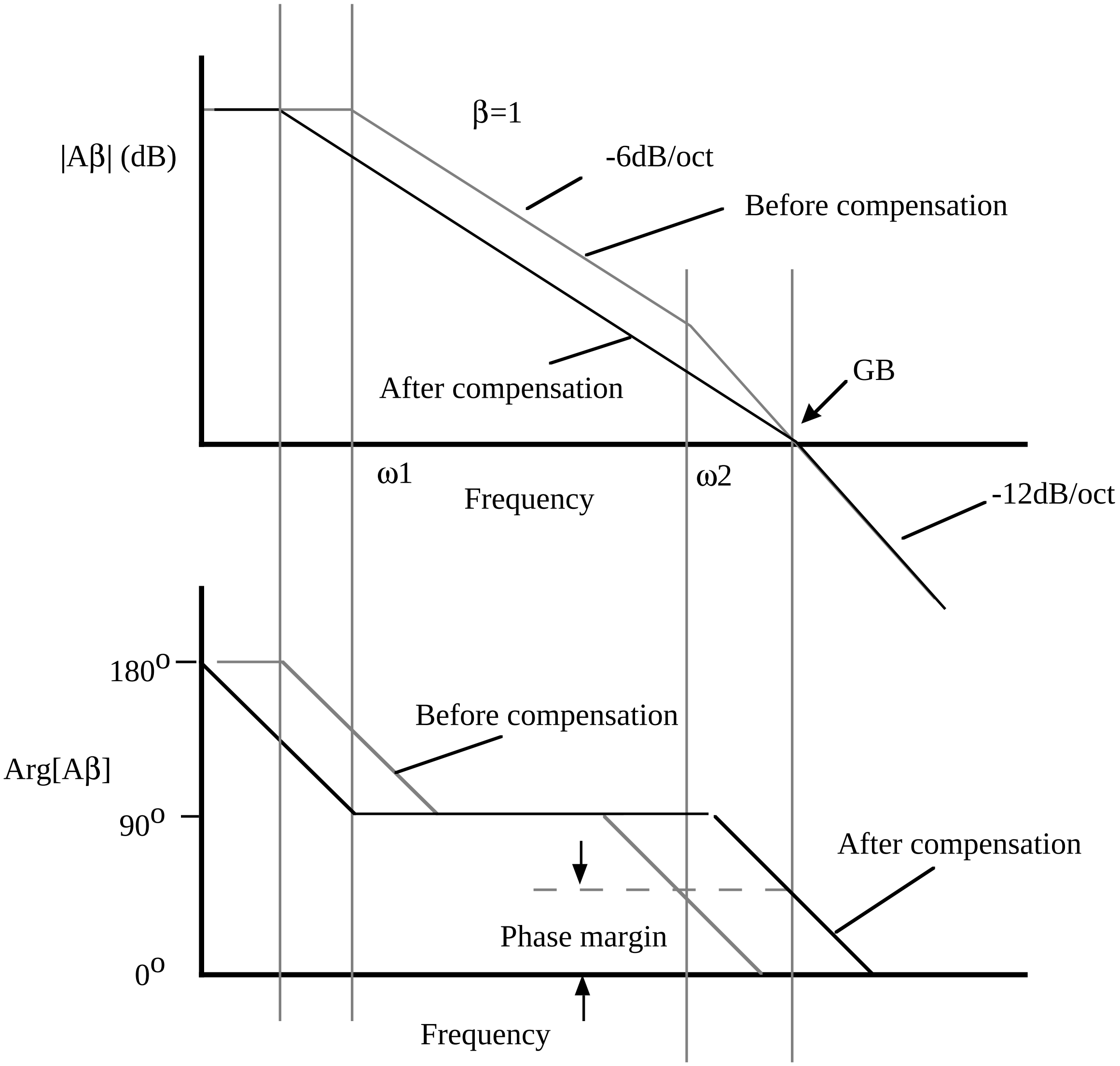
$$z_1 = \frac{g_{mII}}{C_c}$$

where

$g_{mI} = g_{m1} = g_{m2}$ $\qquad$ $g_{mII} = g_{m6}$

$R_I = \dfrac{1}{g_{ds2}+g_{\text{ds4}}}$ $\qquad$ $R_{II} = \dfrac{1}{g_{ds6}+g_{ds7}}$

Miller Compensation



Conditions for Stability

- Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\cdot\left(\frac{1}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c}$$

- The requirement for 45° phase margin is:

$$\text{Arg}[A\beta] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let ω = GB and assume that z ≥ 10GB, therefore we get,

$$\pm 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

or

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow \boxed{|p_2| \geq 1.22GB}$$

- The requirement for 60° phase margin:

$$\boxed{|p_2| \geq 2.2GB \text{ if } z \geq 10GB}$$

- If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{mII}}{C_c} > \frac{10g_{mI}}{C_c} \quad \Rightarrow \quad \boxed{g_{mII} > 10g_{mI}}$$

Furthermore,

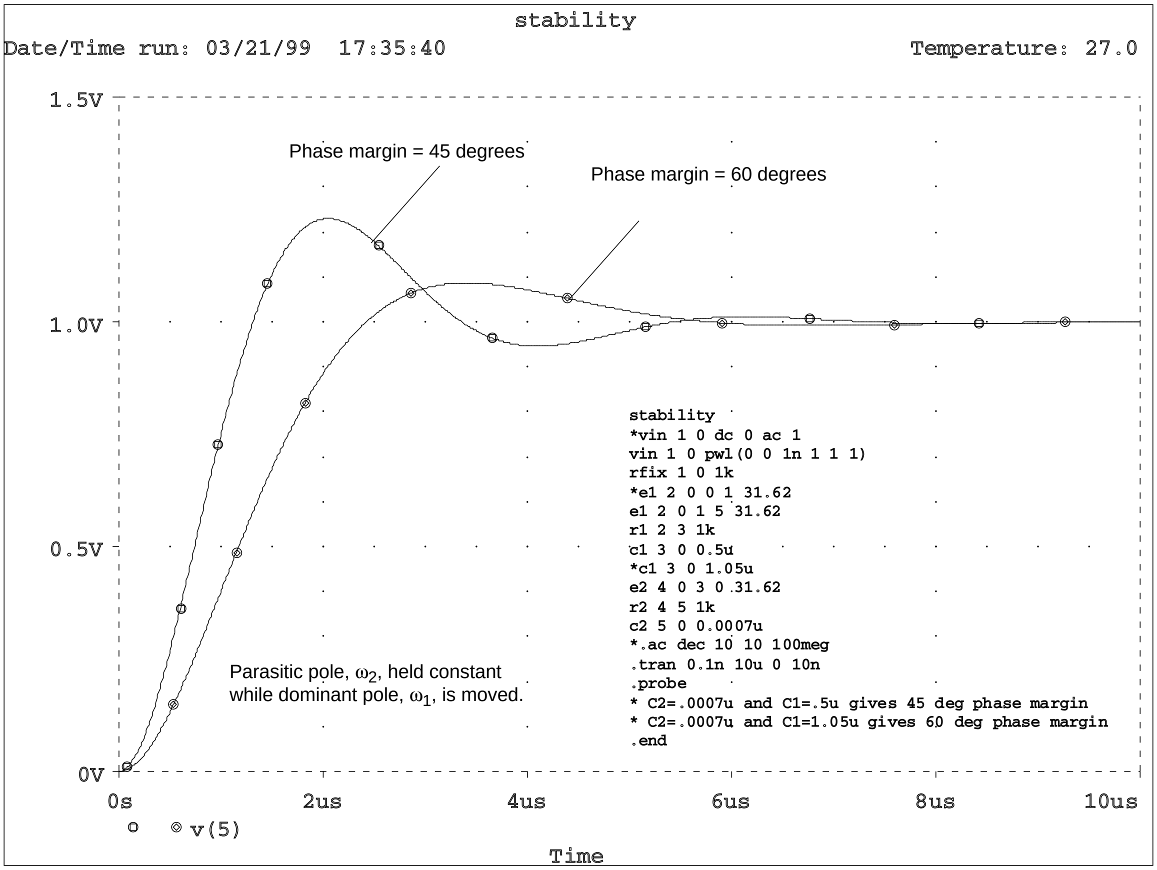
$$\frac{g_{mII}}{C_2} > \frac{2.2g_{mI}}{C_c}$$

which after substitution gives:

$$\boxed{C_c > 0.22C_2}$$

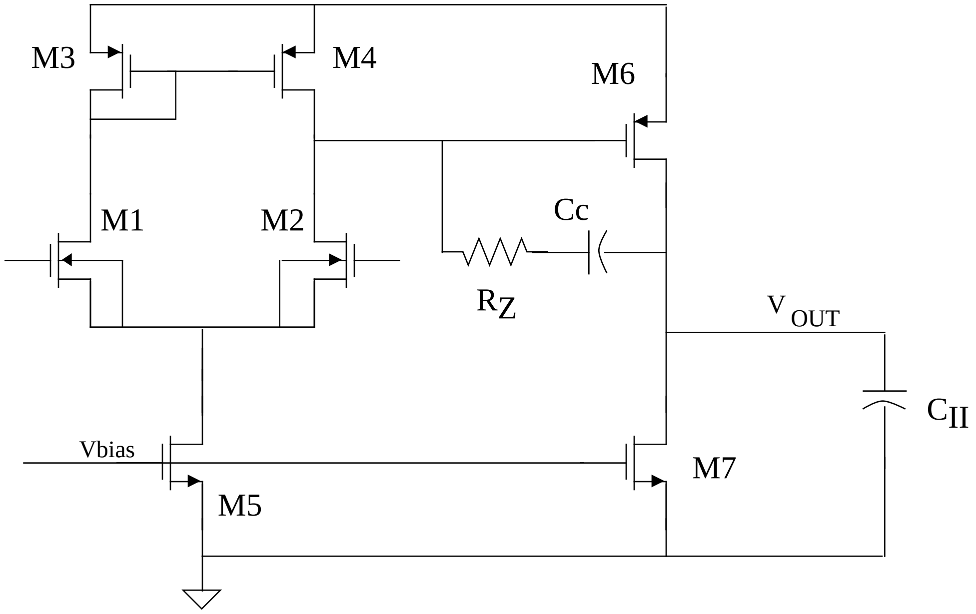
Note:

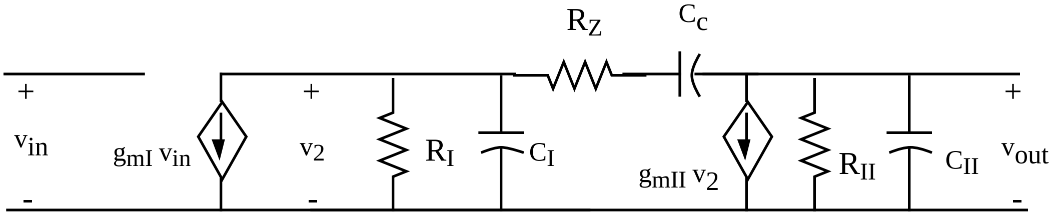
$$g_{mI} = g_{m1} = g_{m2} \quad \text{and} \quad g_{mII} = g_{m6}$$



```
stability
*vin 1 0 dc 0 ac 1
vin 1 0 pwl(0 0 1n 1 1 1)
rfix 1 0 1k
*e1 2 0 0 1 31.62
e1 2 0 1 5 31.62
r1 2 3 1k
c1 3 0 0.5u
*c1 3 0 1.05u
e2 4 0 3 0 31.62
r2 4 5 1k
c2 5 0 0.0007u
*.ac dec 10 10 100meg
.tran 0.1n 10u 0 10n
.probe
* C2=.0007u and C1=.5u gives 45 deg phase margin
* C2=.0007u and C1=1.05u gives 60 deg phase margin
.end
```

Eliminating RHP Zero





$$g_{mI}V_{\text{in}} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_I - V_o) = 0$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_o + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_o - V_I) = 0$$

These equations can be solved to give

$$\frac{V_o(s)}{V_{\text{in}}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_zC_c]\}}{1 + bs + cs^2 + ds^3}$$

where

$$a = g_{mI}g_{mII}R_IR_{II}$$

$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_IR_{II}C_c + R_zC_c$$

$$c = [R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II}) + R_z C_c(R_I C_I + R_{II} C_{II})]$$

$$d = R_I R_{II} R_z C_I C_{II} C_c$$

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots are

$$p_1 \cong \frac{-1}{(1 + g_{mII} R_{II}) R_I C_c} \cong \frac{-1}{g_{mII} R_{II} R_I C_c}$$

$$p_2 \cong \frac{-g_{mII} C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \cong \frac{-g_{mII}}{C_{II}}$$

$$p_3 = \frac{-1}{R_z C_I}$$

and

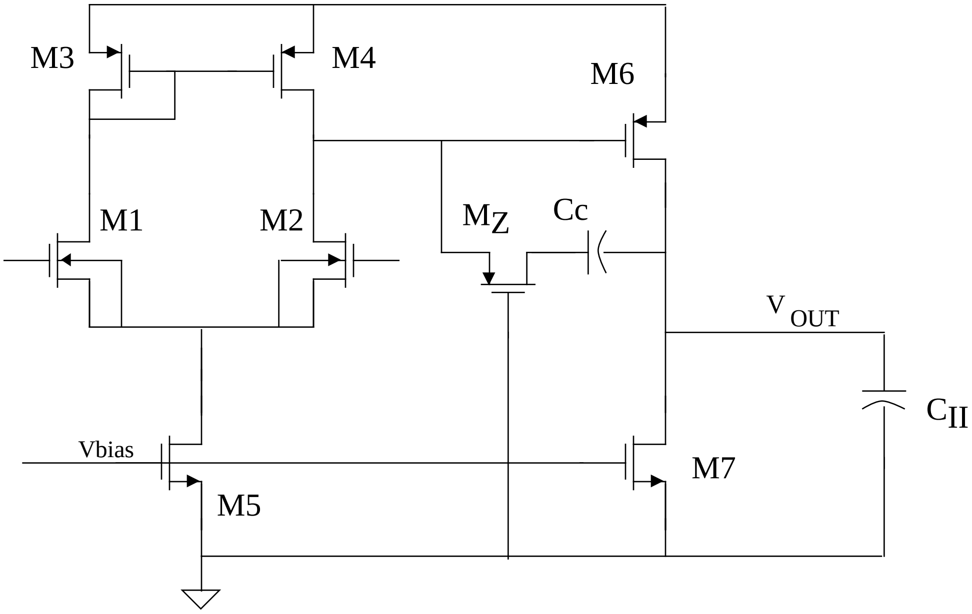
$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

By setting

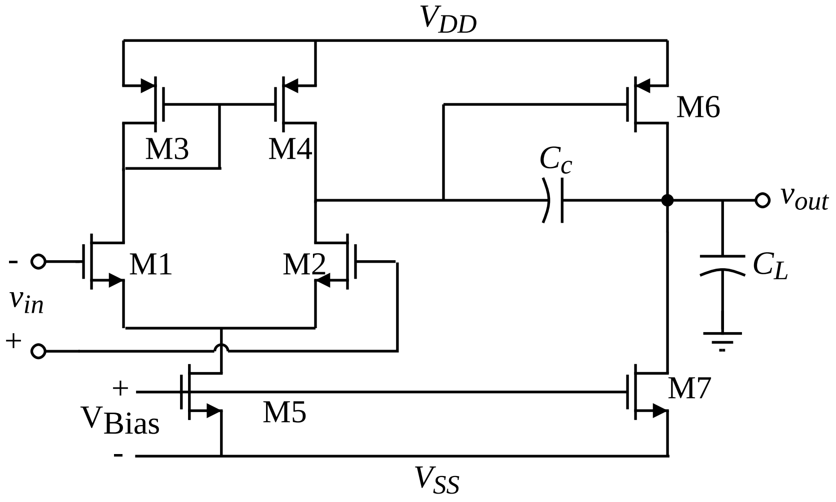
$$R_z = 1/g_{mII}$$

The RHP zero moves to infinity

Implementing Compensation Resistor



Two-Stage Operational Amplifier Design



Important relationships:

$g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$.

$$\text{Slew rate } SR = \frac{I_5}{C_c} \qquad (1)$$

$$\text{First-stage gain } A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \qquad (2)$$

$$\text{Second-stage gain } A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)} \qquad (3)$$

$$\text{Gain-bandwidth } GB = \frac{g_{m1}}{C_c} \qquad (4)$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L} \qquad (5)$$

$$\text{RHP zero } z_1 = \frac{g_{m6}}{C_c} \qquad (6)$$

$$\text{Positive CMR } V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{\text{(max)}} + V_{T1\text{(min)}}) \qquad (7)$$

$$\text{Negative CMR } V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\text{max})} + V_{DS5}(\text{sat}) \tag{8}$$

$$\text{Saturation voltage} V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \tag{9}$$

All transistors are in saturation for the above relationships.

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Input common-mode range, ICMR
4. Load Capacitance, C_L
5. Slew-rate, SR
6. Output voltage swing
7. Power dissipation, P_{diss}

Choose a device length to establish of the channel-length modulation parameter λ.

Design the compensation capacitor C_c. It was shown that placing the loading pole p_2 2.2 times higher than the GB permitted a 60° phase margin (assuming that the RHP zero z_1 is placed at or beyond ten times GB). This results in the following requirement for the minimum value for C_c.

$$C_c > (2.2/10)C_L$$

Next, determine the minimum value for the tail current I_5, based upon slew-rate requirements. Using Eq. (1), the value for I_5 is determined to be

$$I_5 = SR\ (C_c)$$

If the slew-rate specification is not given, then one can choose a value based upon settling-time requirements. Determine a value that is roughly ten times faster than the settling-time specification, assuming that the output slews approximately one-half of the supply rail. The value of I_5 resulting from this calculation can be changed later if need be.

The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ was derived from Eq. (7).

$$S_3 = (W/L)_3 = \frac{I_5}{(K'_3)\ [V_{DD} - V_{\text{in}}(\text{max}) - |V_{T03}|(\text{max}) + V_{T1}(\text{min})]^2}$$

If the value determined for $(W/L)_3$ is less than one, then it should be increased to a value that minimizes the product of W and L. This minimizes the area of the gate region, which in turn reduces the gate capacitance. This gate capacitance will affect a pole-zero pair which causes a small degradation in phase margin.

Requirements for the transconductance of the input transistors can be determined from knowledge of C_c and GB. The transconductance g_{m2} can be calculated using the following equation

$$g_{m1} = GB(C_c)$$

The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below

$$\mathrm{S}_1 = (W/L)_1 = \frac{g_{m1}^2}{(K'_2)(I_5)}$$

Enough information is now available to calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate V_{DS5} using the following relationship derived from Eq. (8).

$$V_{DS5} = V_{\text{in}}(\text{min}) - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{1/2} - V_{T1}(\text{max})$$

If the value for V_{DS5} is less than about 100 mV then the possibility of a rather large $(W/L)_5$ may result. This may not be acceptable. If the value for V_{DS5} is less than zero, then the ICMR specification may be too stringent. To solve this problem, I_5 can be reduced or $(W/L)_1$ increased. The effects of these changes must be accounted for in previous design steps. One must iterate until the desired result is achieved. With V_{DS5} determined, $(W/L)_5$ can be extracted using Eq. (9) in the following way

$$\mathrm{S}_5 = (W/L)_5 = \frac{2(I_5)}{K'_5(V_{DS5})^2}$$

For a phase margin of 60°, the location of the loading pole was assumed to be placed at 2.2 times GB. Based upon this assumption and the relationship for $|p_2|$ in Eq. (5), the transconductance g_{m6} can be determined using the following relationship

$$g_{m6} = 2.2(g_{m2})(C_L/C_c)$$

Since S_3 is known as well as g_{m6} and g_{m3}, assuming balanced conditions,

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

I_6 can be calculated from the consideration of the “proper mirroring” of first-stage the current mirror load of Fig. 6.3-1. For accurate current mirroring, we want V_{SD3} to be equal to V_{SD4}. This will occur if V_{SG4} is equal to V_{SG6}. V_{SG4} will be equal to V_{SG6} if

$$I_6 = \frac{(W/L)_6}{(W/L)_4} I_1 = \left(\frac{S_6}{S_4}\right) I_1$$

Choose the larger of these two values for I_6 (Eq. 19 or Eq. 20). If the larger value is found in Eq (19), then $(W/L)_6$ must be increased to satisfy Eq. (20). If the larger value is found in Eq. (20), then no other adjustments must be made. One also should check the power dissipation requirements since I_6 will most likely determine the majority of the power dissipation.

The device size of M7 can be determined from the balance equation given below

$$S_7 = (W/L)_7 = (W/L)_5 \left(\frac{I_6}{I_5}\right) = S_5 \left(\frac{I_6}{I_5}\right)$$

The first-cut design of all *W/L* ratios are now complete. Fig. 6.3-2 illustrates the above design procedure showing the various design relationships and where they apply in the two-stage CMOS op amp.

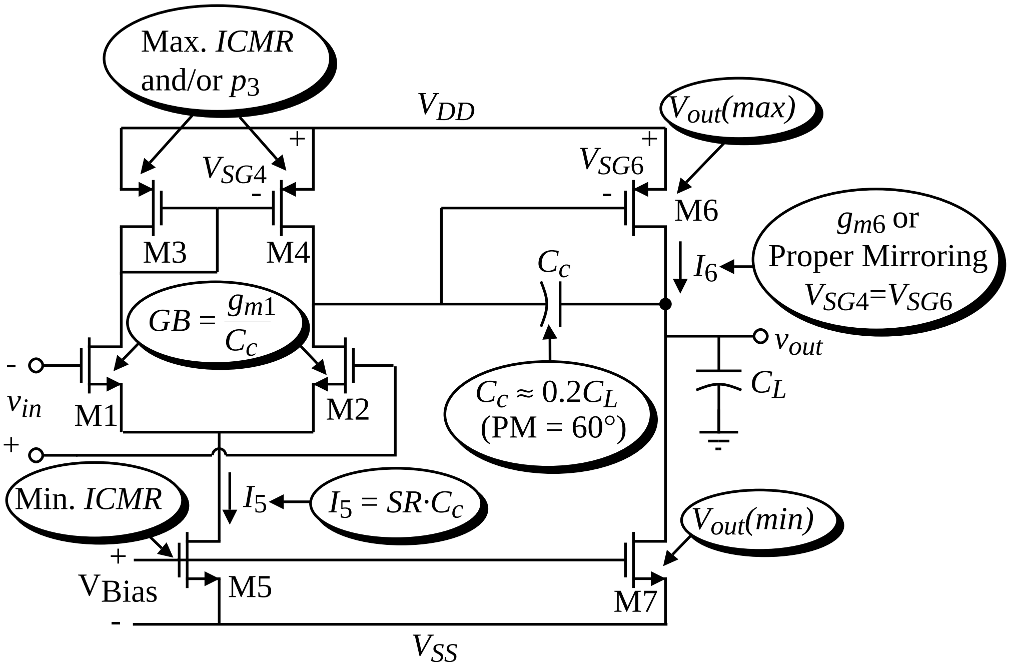


Figure 6.3-2 Illustration of the design relationships and the circuit for a two-stage CMOS op amp.

At this point in the design procedure, the total amplifier gain must be checked against the specifications.

$$A_v = \frac{(2)(g_{m2})(g_{m6})}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

If the gain is too low, a number of things can be adjusted. The best way to do this is to use the table below, which shows the effects of various device sizes and currents on the different parameters generally specified. Each adjustment may require another pass through this design procedure in order to insure that all specifications have been met. Table 6.3-2 summarizes the above design procedure.

Dependencies of device performance on various parameters

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Comp. Cap..
	I_5	I_7	W/L	L	W	L	W_6/L_6	W_7	L_7	C_c
Increase DC Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase GB	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$							$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$					$(\uparrow)^{1/2}$			$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\downarrow$

Design Procedure:

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given.

1. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.
2. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

3. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

$$I_5 = SR \cdot C_c$$

$$I_5 \cong 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

4. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\text{max}) - |V_{T03}|(\text{max}) + V_{T1}(\text{min})]^2} \geq 1$$

5. Verify that the pole of M3 due to C_{gs3} and C_{gs4} ($=0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

6. Design for S_1 (S_2) to achieve the desired GB.

$$g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}^2}{K'_2 I_5}$$

7. Design for S_5 from the minimum input voltage. First calculate V_{DS5}(sat) then find S_5.

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100\text{ mV}$$

$$S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

8. Find g_{m6} and S_6 by the relationship relating to phase margin, load, and compensation capacitors, and the balance condition.

$$g_{m6} = 2.2g_{m2}(C_L/C_c)$$

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

9. Calculate I_6 :

$$I_6 = (S_6/S_4)I_4 = (S_6/S_4)(I_5/2)$$

10. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = (I_6/I_5)S_5$$

11. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

12. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they have been satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

13. Simulate the circuit to check to see that all specifications are met.

Example: Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1μm.

$A_v > 3000$V/V $\quad V_{DD} = 2.5$V $\quad V_{SS} = -2.5$V

$GB = 5$MHz $\quad C_L = 10$pF $\quad SR > 10$V/μs

V_{out} range = ±2V $\quad ICMR = -1$ to 2V $\quad P_{diss} \leq 2$mW

<u>*Solution*</u>

Calculate the minimum value of the compensation capacitor C_c,

$$C_c > (2.2/10)(10 \text{ pF}) = 2.2 \text{ pF}$$

Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3 \times 10^{-12})(10 \times 10^{6}) = 30\ \mu\text{A}$$

Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(50 \times 10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 15$$

$$g_{m3} = \sqrt{2 \times 50\text{x}10^{-6}\ \text{x}15\text{x}10^{-6} \times 15} = 150\mu\text{S}$$

Therefore

$$(W/L)_3 = (W/\text{L})_4 = 15$$

Check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 0.4\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = 15.75\text{x}10^{9}\text{(rads/sec)}$$

or 2.98 GHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

The next step in the design is to calculate g_{m1}

$$g_{m1} = (5 \times 10^{6})(2\pi)(3 \times 10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}{}^2}{2K'_N I_1} = \frac{(94.25)^2}{2 \cdot 110 \cdot 15} = 2.79 \approx 3.0$$

Next calculate V_{DS5}

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30 \times 10^{-6}}{110 \times 10^{-6} \cdot 3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from Eq. (16)

$$(W/L)_5 = \frac{2(30 \times 10^{-6})}{(50 \times 10^{-6})(0.35)^2} = 4.49 \approx 4.5$$

From Eq. (20) of Sec. 6.2, we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$

$$(W/L)_6 = 15 \;\frac{942.5 \times 10^{-6}}{150 \times 10^{-6}} = 94.25$$

Using the equations for proper mirroring, I_6 is determined to be

$$I_6 = (15 \times 10^{-6})(94.25/15) = 94.25\ \mu\text{A}$$

Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5 \left(\frac{94.25 \times 10^{-6}}{30 \times 10^{-6}}\right) \approx 14.14$$

Check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{min}(\text{out}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \times 94.25}{110 \times 14.14}} = 0.348\text{V}$$

which is much less than required. At this point, the first-cut design is complete. Examining the results shows that the large value of M7 is due to the large value of M5 which in turn is due to a tight specification on the negative input common mode range. To reduce these values the specification should be loosened or a different architecture (i.e. p-channel input pair) examined.

Now check to see that the gain specification has been met

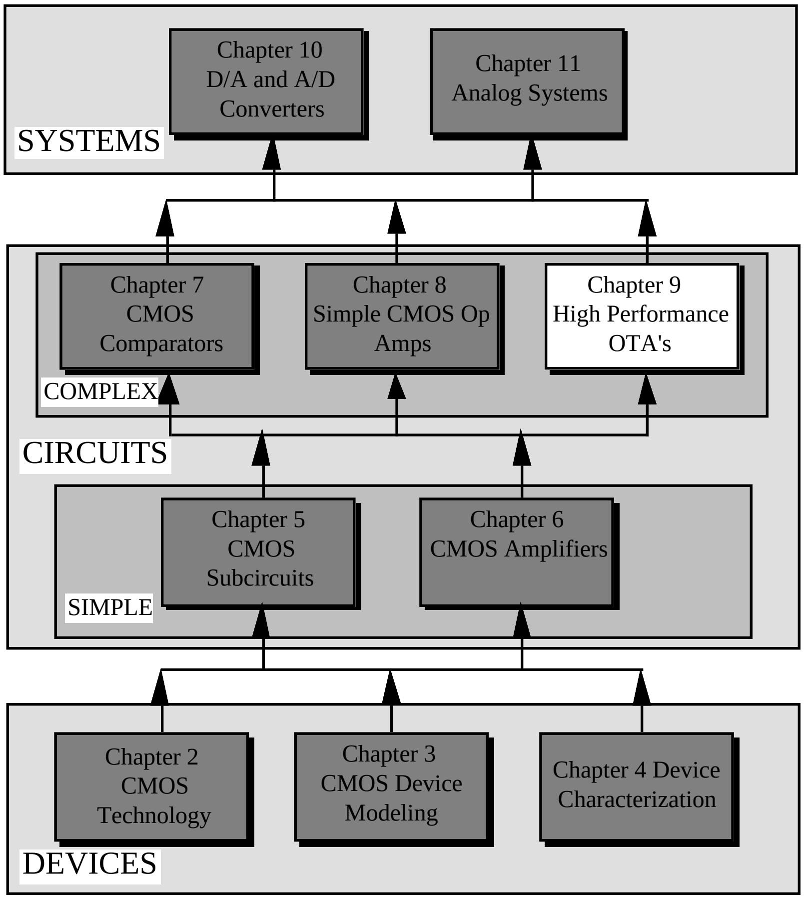
$$A_v = \frac{(2)(94.25 \times 10^{-6})(942.5 \times 10^{-6})}{30 \times 10^{-6}(.04 + .05)38 \times 10^{-6}(.04 + .05)} = 19{,}240$$

which meets specifications.

IX. HIGH PERFORMANCE CMOS AMPLIFIERS

Contents

Organization

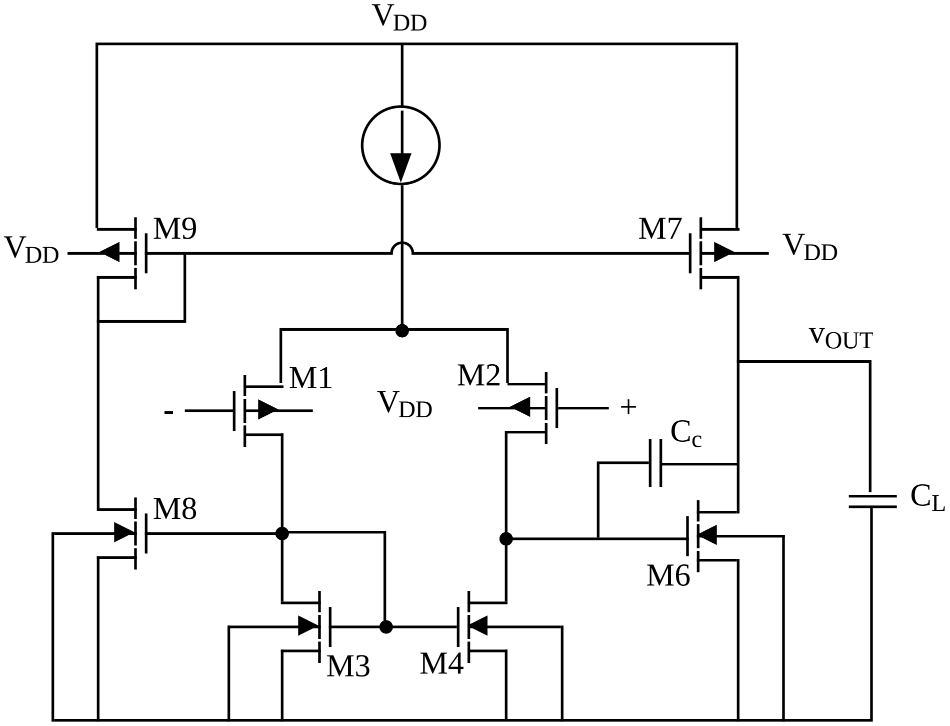


IX.1 IMPROVING THE TWO-STAGE ARCHITECTURE

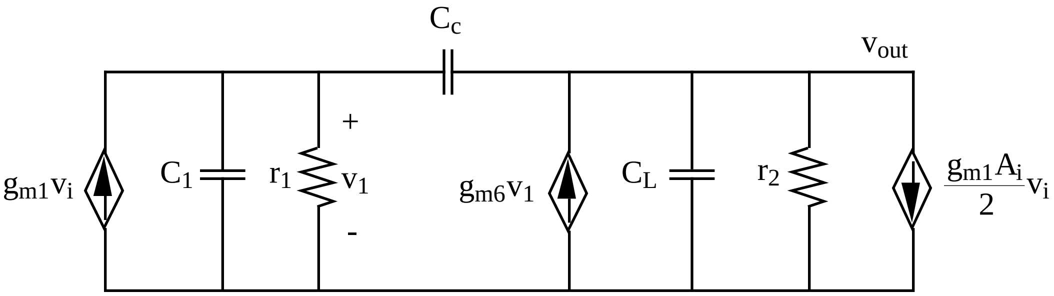
Amplifiers Using an MOS Output Stage

PUSH-PULL CMOS OTA

This amplifier is a simple extension of the seven-transistor OTA studied in Section 8.



small-signal equivalent circuit:



where $g_{m1} = g_{m2}$, $r_1 = \dfrac{1}{g_{ds2} + g_{ds4}}$, $r_2 = \dfrac{1}{g_{ds6} + g_{ds7}}$

Amplifiers Using an MOS Output Stage - Continued

Network equations:

$$[g_1 + s(C_1 + C_L)]v_1 - sC_c v_2 = g_{m1}v_i$$

$$[g_5 + sC_c]v_1 + [g_2 + s(C_c + C_L)]v_2 = \frac{g_{m1}A_I v_i}{2}$$

A_I is the current gain from M1 to M7: $A_I = \dfrac{i_7}{i_1}$

$$z = \frac{-g_{m6}}{\left(\frac{A_I}{2} - 1\right)C_c}$$

$$p_1 \approx \frac{-g_1 g_2}{g_{m6}C_c}$$

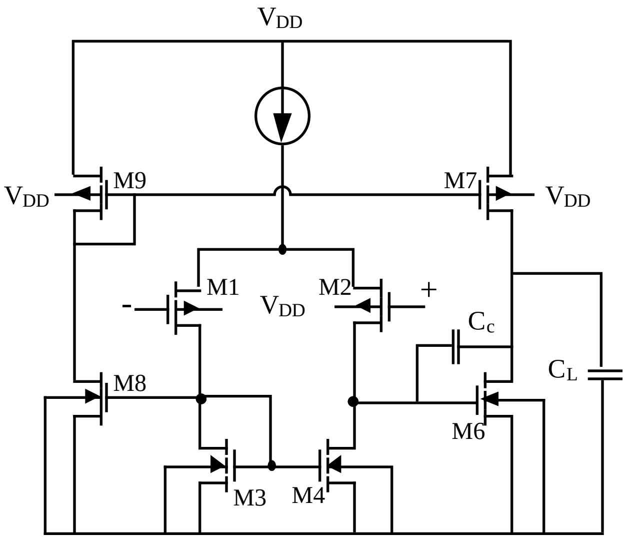
$$p_2 \approx \frac{-g_{m6}}{C_L}$$

$$A_V \approx \frac{g_{m1}g_{m6}}{g_1 g_2}$$

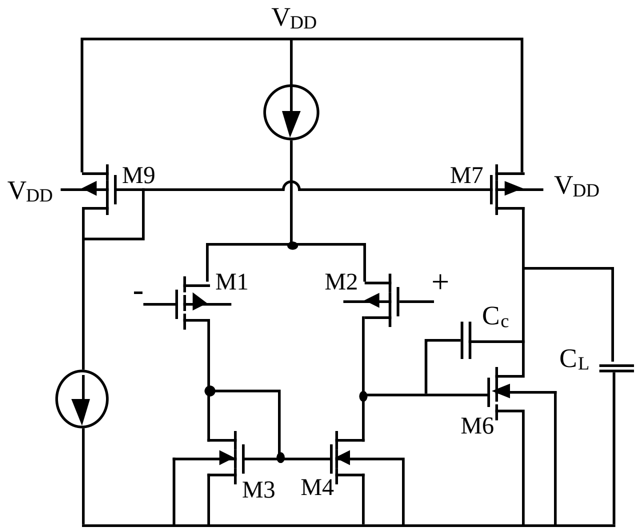
To guarantee that the zero stays in the left-half plane, $A_I > 2$

Amplifiers Using an MOS Output Stage - Continued

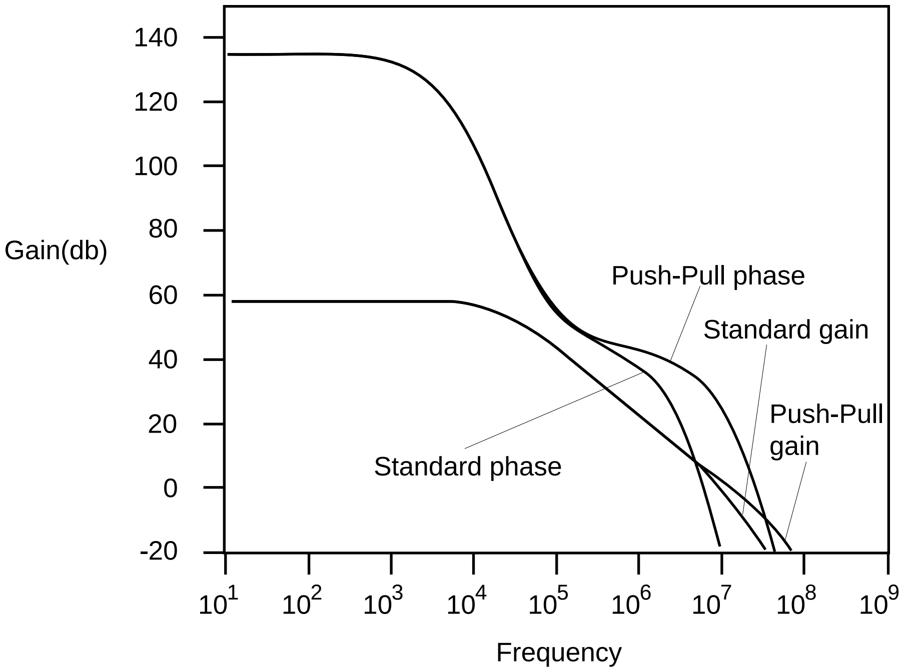
Example:



Push-Pull ($A_I \approx 3$)



Standard ($A_I = 0$)



IX.2 Two-Stage Cascode Architecture

Why Cascode Op Amps?

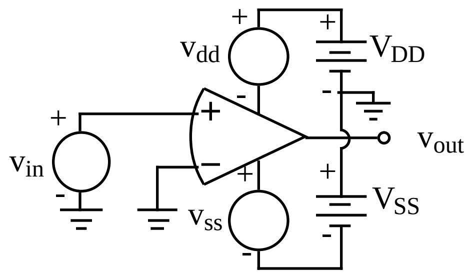
- Control the frequency behavior
- Increase PSRR
- Simplifies design

Where is the Cascode Technique Applied?

- First stage -
  - Good noise performance
  - Requires level translation to second stage
  - Requires Miller compensation
- Second stage -
  - Self compensating
  - Reduces the efficiency of the Miller compensation
  - Increases PSRR

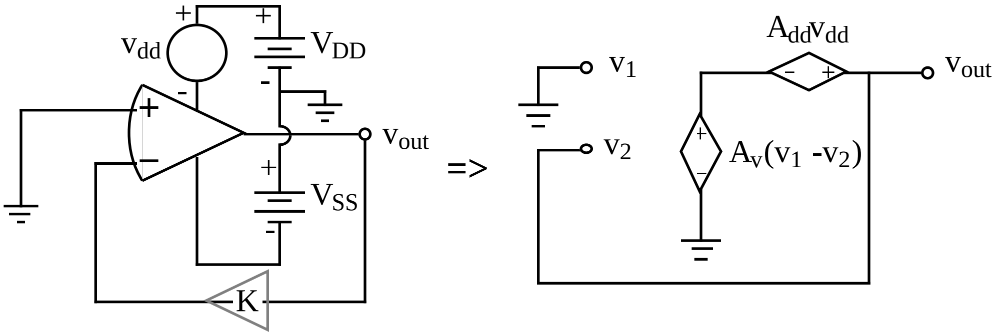
Power Supply Rejection Ratio (PSRR)

Definition:



$$PSRR^+ = \frac{A_v(v_{dd}=0)}{A_{dd}(v_{in}=0)} = \frac{\frac{v_{out}}{v_{in}}(v_{dd}=0)}{\frac{v_{out}}{v_{dd}}(v_{in}=0)}$$

Calculation of PSRR:



$$v_{out} = A_{dd}v_{dd} + A_v(v_1 - v_2) = A_{dd}v_{dd} - A_v v_{out}$$

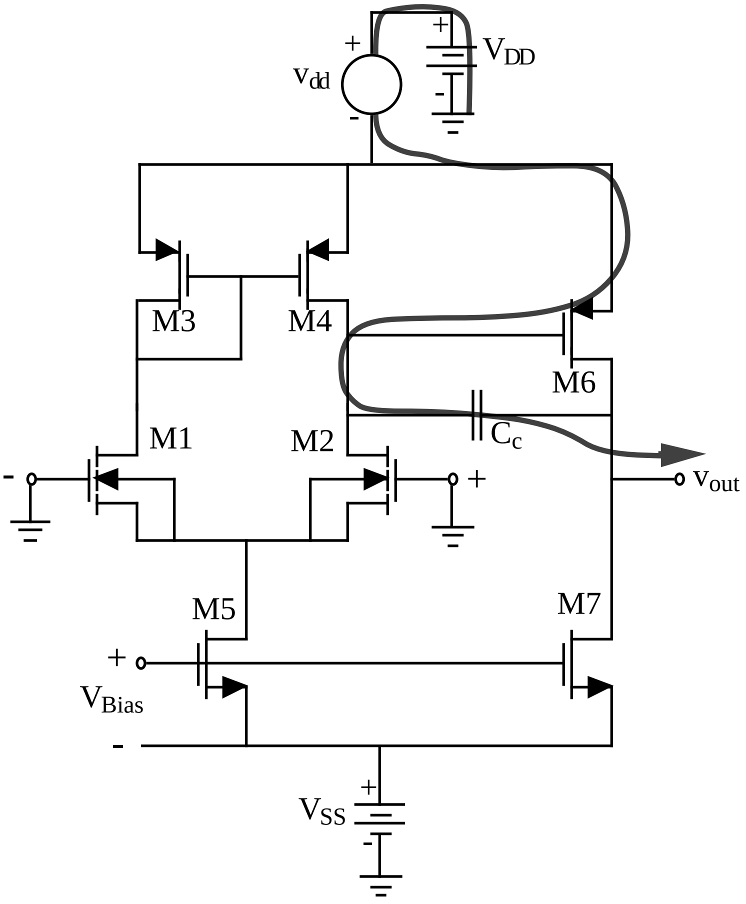
$$v_{out}(1 + A_v) = A_{dd}v_{dd}$$

Extends bandwidth beyond GB

↓

$$\frac{v_{out}}{v_{dd}} = \frac{A_{dd}}{1 + A_v} \approx \frac{A_{dd}}{A_v} = \frac{1}{PSRR^+} \qquad \frac{v_{out}}{v_{dd}} = \frac{KA_{dd}}{1+KA_v} \approx \frac{A_{dd}}{A_v}$$

Intuitive Interpretation of Positive PSRR for the Two-Stage OTA

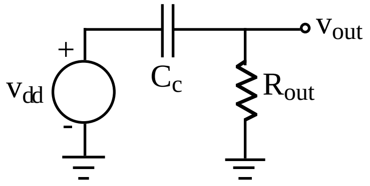


1.) The M7 current sink causes V_{GS6} to act like a battery.

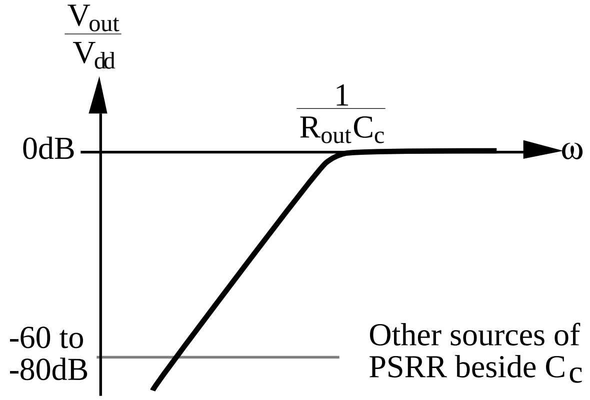
2.) Therefore, v_{dd} couples from the source to gate of M6.

3.) The path to the output is through any capacitance from gate to drain of M6.

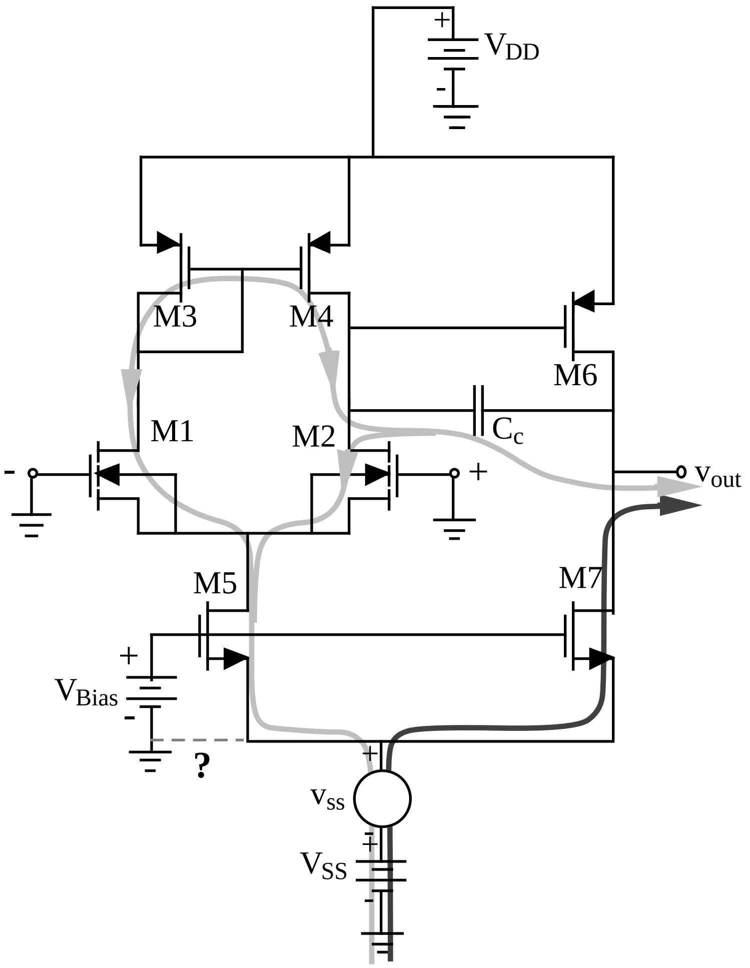
4.) Resultant circuit model-



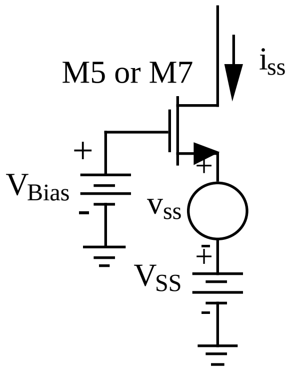
Must reduce C_c!



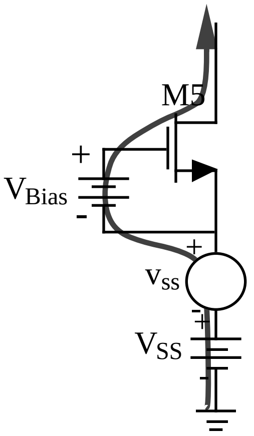
Intuitive Interpretation of the Negative PSRR for the Two-Stage OTA



Two mechanisms of v_{SS} injection:



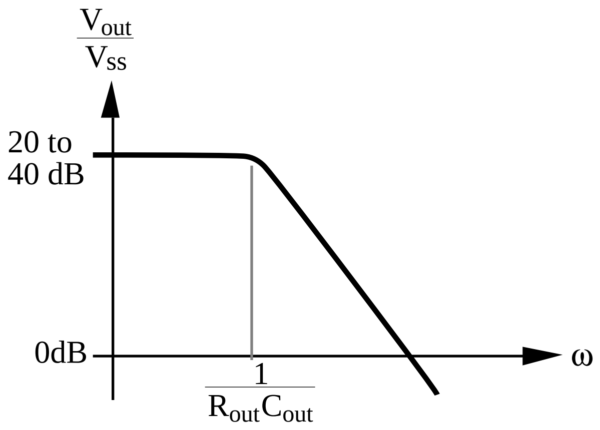
Transconductance injection



Capacitance injection

Intuitive Interpretation of the Negative PSRR for the Two-Stage OTA - Continued

Transconductance injection:



Path through the input stage:

Not important as long as CMRR is high.

Path through the output stage:

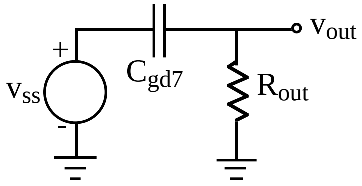
$$v_{out} \approx i_{ss}R_{out} = g_{m7}v_{ss}R_{out}$$

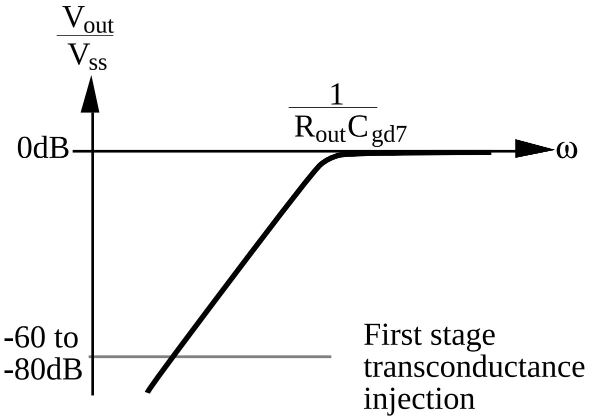
$$\frac{v_{out}}{v_{ss}} = g_{m7}R_{out}$$

Frequency dependence -

$$R_{out} \rightarrow R_{out}||\left(\frac{1}{sC_{out}}\right)$$

Capacitance injection:





Reduce C_{gd7}!

Problems with the two-stage OTA:

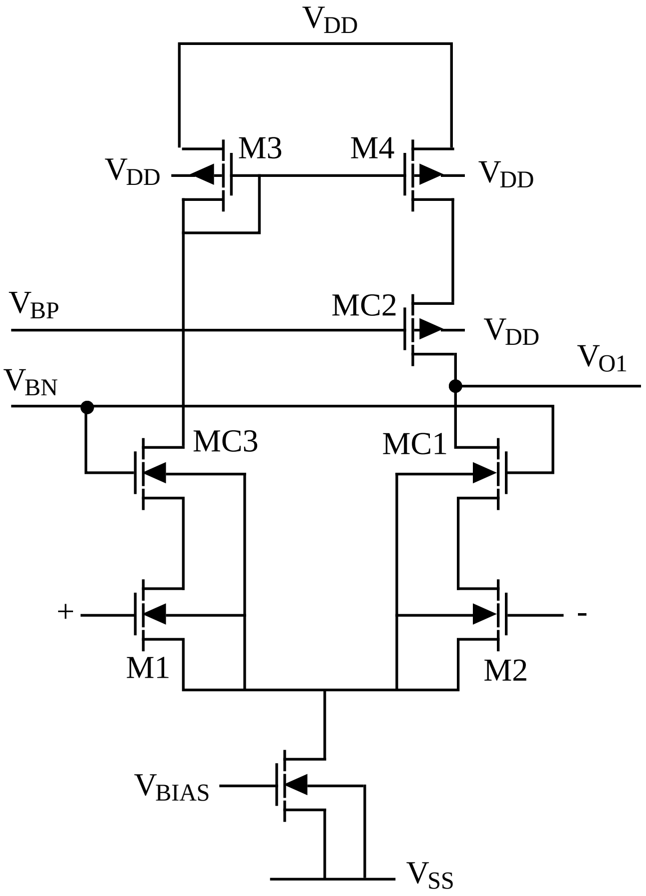
- Insufficient gain
- Poor stability for large load capacitance
- Poor PSRR

These problems can be addressed using various cascode structures.

We will consider several approaches:

- Cascoding the first stage
- Cascoding the second stage
- Folded cascode

First Stage Cascode



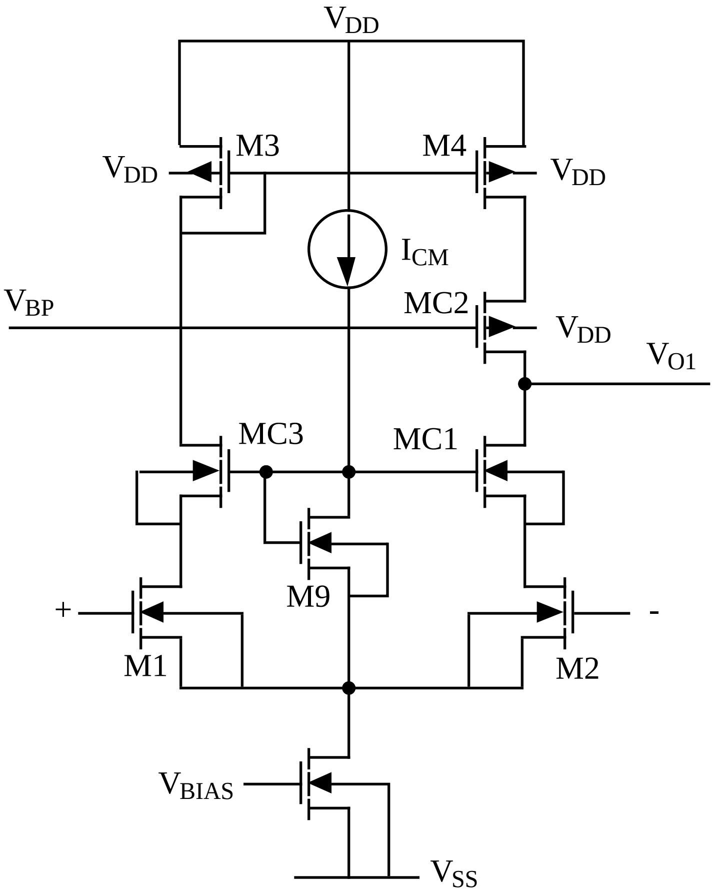
$r_{o1} \approx (g_{mc2} r_{dsc2}) r_{ds4} \parallel (g_{mc1} r_{dsc1}) r_{ds2}$

$\text{Gain} \approx g_{m2} r_{o1}$

- Overall gain increased by $\approx \dfrac{g_{mc} r_{dsc}}{2}$
- Requires voltage translation to drive next stage
- Requires additional biasing for cascode devices
- Common-mode problem at drains of M1 and M2

First Stage Cascode - Continued

Common-mode improvement:



Common-mode circuitry (M9) maintains V_{ds} of M1 and M2

$$A_V = g_{m1} r_{o1}$$

$$r_{o1} \approx (g_{mc2} r_{dsc2}) r_{ds4} \,\|\, (g_{mc1} r_{dsc1}) r_{ds2}$$

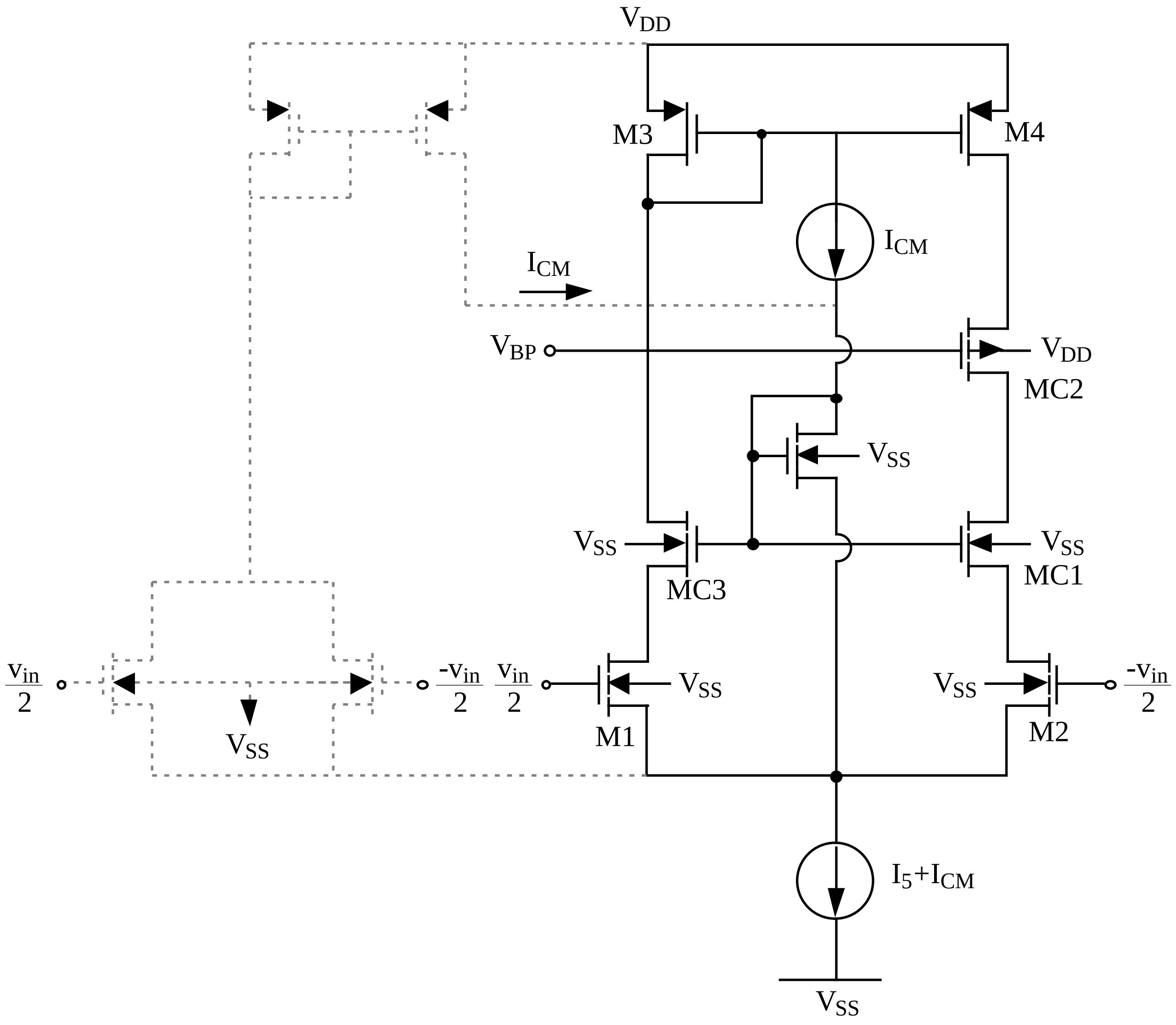
$$p_1 \approx \frac{-1}{C_L r_{o1}}$$

$$GB \approx A_V |p_1| \approx \frac{g_{m1}}{C_L}$$

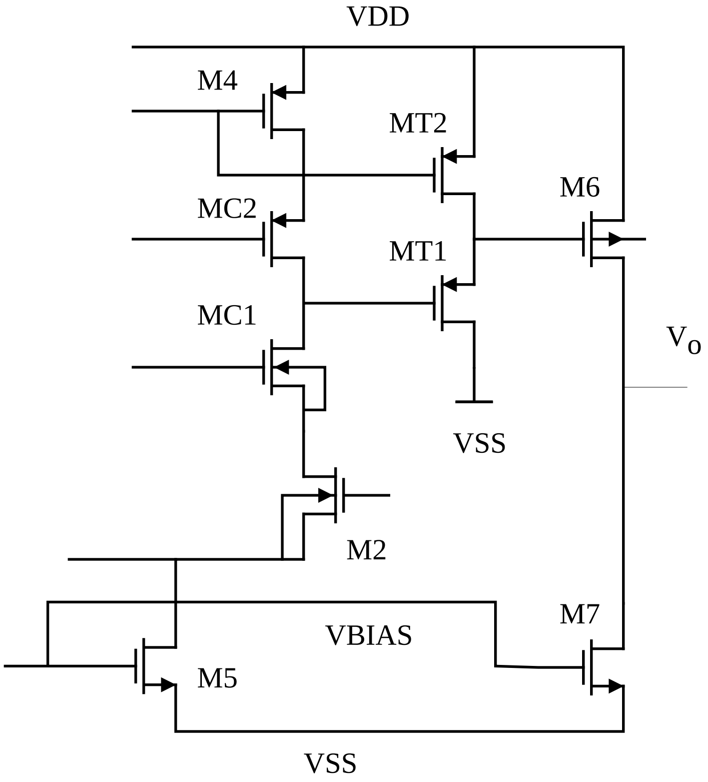
Output range of this amplifier is poor when used by itself. It needs an output stage to be practical.

First Stage Cascode - Continued

Implementation of I_{CM}

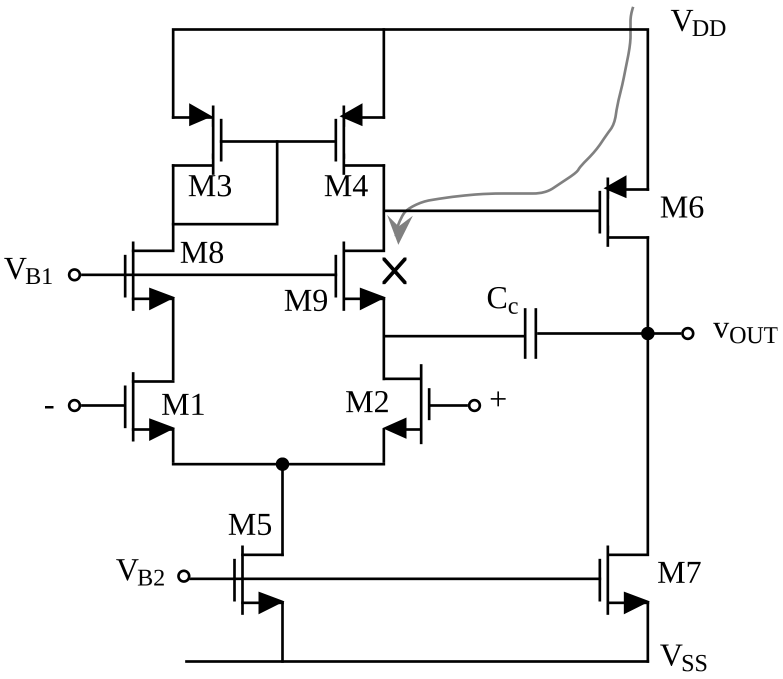


Level Translator for First Stage Cascode



Improved PSRR For Two-Stage OTA

Use cascode to reject C_c feedforward



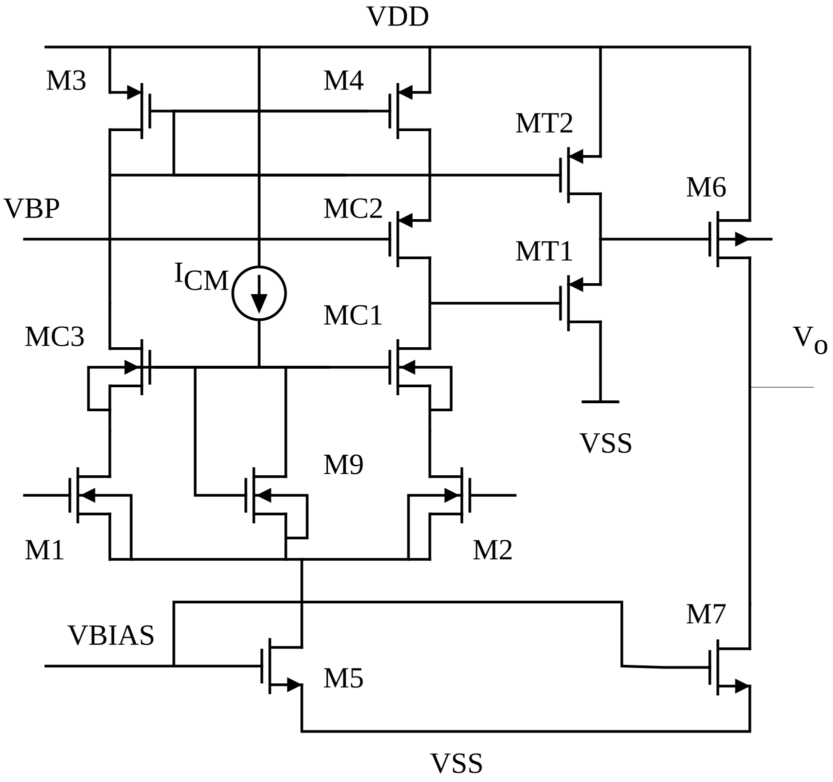
+PSRR is reduced by M9

Disadvantage -

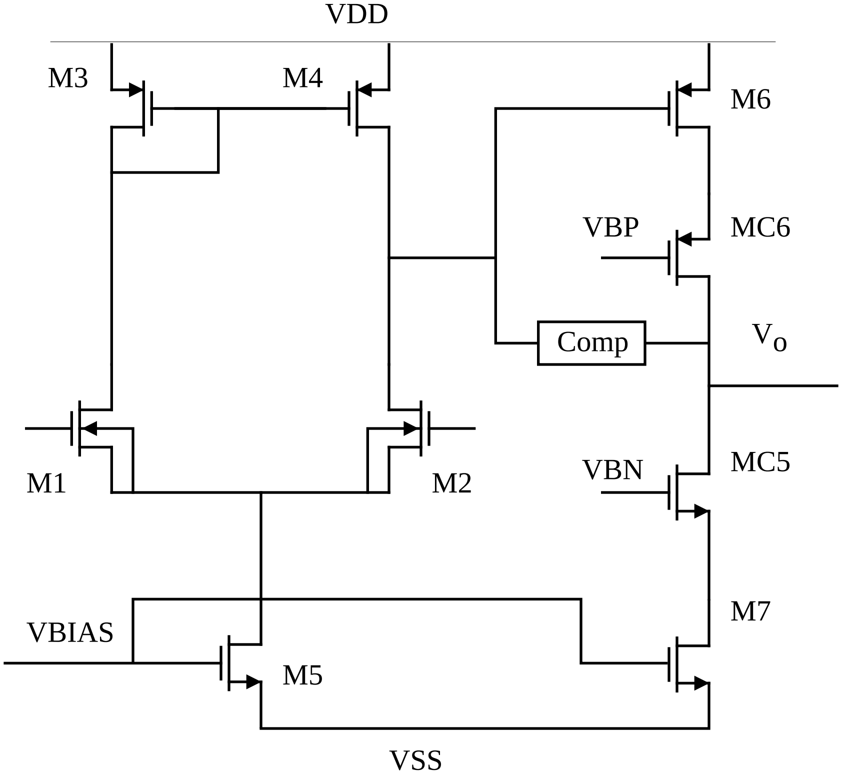
Miller pole is larger because $R_1 \approx \dfrac{1}{g_{m9}}$

positive input common mode range is restricted

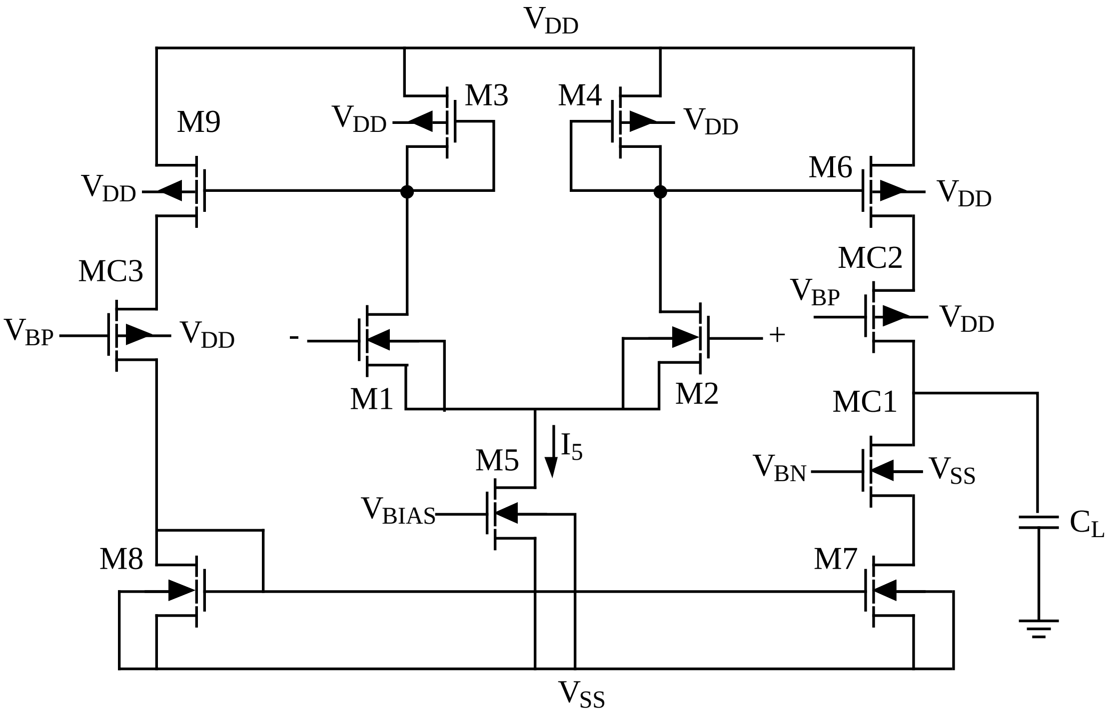
Complete Two Stage Cascode



Second Stage Cascode



LOAD COMPENSATED CASCODE AMPLIFIER



$$\left.\begin{aligned} A_{V1} &= \frac{g_{m2}}{g_{m4}} \\ A_{V2} &= \frac{1}{2}(g_{m6}+g_{m9})R_o \end{aligned}\right\} \quad A_V = \frac{g_{m2}}{2(g_{m4})}(g_{m6}+g_{m9})\,R_o$$

where

$$R_o \approx (g_{mc2}r_{dsc2})r_{ds6} \,||\, (g_{mc1}r_{dsc1})r_{ds7} \text{ and } M7 = M8$$

Or,

$$A_V = \left(\frac{g_{m1}+g_{m2}}{2}\right) KR_o$$

where

$$K = \frac{W_6/L_6}{W_4/L_4} = \frac{W_9/L_9}{W_3/L_3}$$

Design Example

Pertinent design equations:

$$SR = \frac{i_{OUT}}{C_L}$$

$$A_V = \frac{g_{m2}}{2(g_{m4})}(g_{m6} + g_{m7})\, r_o$$

$$GB = \frac{g_{m2}(g_{m6} + g_{m7})}{2(g_{m4})C_L}$$

$$V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{ß_3}} - |V_{T3}|_{(max)} + V_{T1(min)}$$

$$V_{in(min)} = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{ß_1}} + V_{T1(max)}$$

Specifications:

$V_{DD} = -V_{SS} = 5V$

$SR = 5V/\mu s$ into $C_L = 50pf$

GB = 5 MHz

$A_V > 5000$

CMR = ±3V

Output swing = ±3V

Design Procedure

1.) Design for maximum source/sink current

$I_{source/sink} = C_L(SR) = 50pf(5V/\mu s) = 250\ \mu A$

2.) Note that -

$$\text{Max. } I_{OUT}\text{ (source)} = \frac{S_6}{S_4} I_5$$

Max. I_{OUT} (Sink) = Max. I_{OUT} (source) if $S_3 = S_4$,

$S_9 = S_6$ and $S_7 = S_8$

3.) Choose $\underline{I_5 = 100\ \mu A}$

$\therefore \underline{S_9 = S_6 = 2.5\ S_4 = 2.5\ S_3}$

4.) Design for ± 3V output capability

a.) Negative peak

Let $V_{DSC1}(\text{sat.}) = V_{DS7}(\text{sat.}) = 1V$

under negative peak conditions, $I_{C1} = I_7 = 250\ \mu A$

Divide 2V equally,

$$\therefore 2V = \sqrt{\frac{2I_7}{K_N'S_7}} + \sqrt{\frac{2I_{C1}}{K_N'S_{C1}}} = 2\sqrt{\frac{2I_7}{K_N'S_7}} = 2\sqrt{\frac{500\ \mu A}{17\ \mu A/V^2\ S_7}}$$

$\therefore \underline{S_7 = S_{C1} = 29.4}$ -> $\underline{S_8 = S_7 = 29.4}$

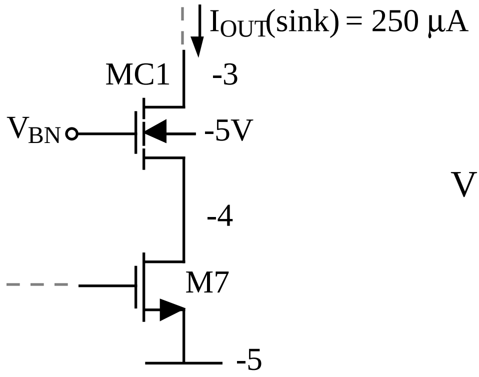
b.) Positive peak, divide voltage equally,

$$V_{SD6} = V_{SDC2} = 1V, \text{ --> } 2V = \sqrt{\frac{2I_6}{K_P'S_6}} + \sqrt{\frac{2I_{C2}}{K_P'S_{C2}}} = 2\sqrt{\frac{2I_6}{K_P'S_6}}$$

$$\therefore \underline{S_6 = S_{C2} = 62.5} \quad \text{-->} \quad \underline{S_3 = S_4 = 25}$$

5.) Design of V_{BP} and V_{BN}

a.) V_{BN} (Assume max. I_{OUT} (sink) conditions)

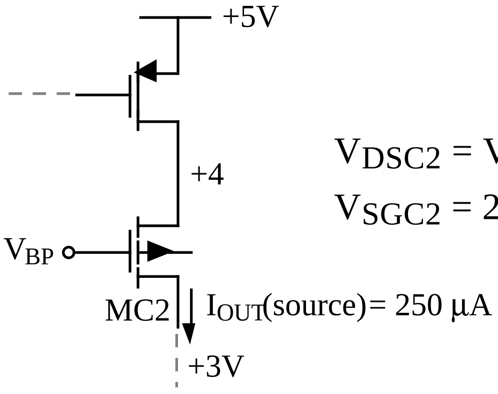


$$V_{DSC1} = V_{GSC1} - V_{TC1} \text{ (ignoring bulk effects)}$$

$$1 = V_{GSC1} - 1 \text{ --> } V_{GSC1} = 2V$$

$$\therefore \underline{V_{BN} = -2V}$$

b.) V_{BP} (Assume max. I_{OUT} (source) conditions)



$$V_{DSC2} = V_{GSC2} - |V_{TC2}| \text{ (ignoring bulk effects)}$$

$$V_{SGC2} = 2V \quad \therefore \underline{V_{BP} = +2V}$$

6.) Check max. V_{in} influence on S_3 (S_4)

$$V_{in}\,(\max) = V_{DD} - \sqrt{\frac{I_5}{ß_3}} - |V_{T03}|_{\max} + V_{T1}(\min)$$

$$+3 = +5 - \sqrt{\frac{100\ \mu A}{K_P'S_3}} - 1.2 + 0.8$$

$$S_3 = \frac{100\ \mu A}{8\ \frac{\mu A}{V^2}\,(1.6V)^2} = 4.88 \quad (\text{Use } S_3 = S_4 = 25)$$

With $S_3 = 25$, $V_{in}\,(\max) = 3.89V$ which exceeds the specification.

7.) Find g_{m1} (g_{m2})

a.) A_V specification

$$A_V = \frac{g_{m1}}{g_{m4}}\left(\frac{g_{m6} + g_{m7}}{2}\right) R_{II}$$

$$g_{m4} = \sqrt{2I_4K_p'S_4} = 141.1\ \mu s$$

$$g_{m6} = \sqrt{2I_6K_P'S_6} = 353.5\ \mu s$$

$$g_{m7} = \sqrt{2I_7K_N'S_7} = 353.5\ \mu s$$

$$g_{mc1} = g_{m7}$$

$$g_{mc2} = g_{m6}$$

$$r_{ds6} = r_{dsc2} = \frac{1}{I_6\lambda_P} = 0.4\ M\Omega$$

$$r_{ds7} = r_{dsc1} = \frac{1}{I_7\lambda_N} = 0.8\ M\Omega$$

$$R_{II} \approx (g_{mc1}r_{dsc1}r_{ds7}) \,||\, (g_{mc2}r_{dsc2}r_{ds6}) = 45.25\ M\Omega$$

$$\therefore \quad \left(\frac{g_{m1}}{141.1}\right)\left(\frac{707\ \mu s}{2}\right)(226.24\ M\Omega \,||\, 56.56\ M\Omega) > 5000\ V/V$$

$$\therefore \quad g_{m1} > 44\ \mu s$$

b.) GB specification

$$GB = \frac{g_{m1}(g_{m6} + g_{m7})}{2g_{m4}}(50pF) = 10\pi \cdot 10^6 \text{ rps}$$

$$g_{m1} = \frac{(10\pi \cdot 10^6)(141.1 \cdot 10^{-6})(50 \cdot 10^{-12})}{707 \cdot 10^{-6}/2} = 627\ \mu S$$

$$\therefore\ \underline{S_1 = S_2 = \frac{g_m{}^2}{I_5 K_N'} = 231}$$

$$A_V = \frac{g_{m1}}{g_{m4}}\left(\frac{g_{m6}+g_{m7}}{2}\right)R_{II} = \frac{627}{141.1}\left(\frac{707\mu S}{2}\right)(45.25M\Omega) = 71{,}080$$

8.) Find S_5 from V_{in} (min)

$$V_{in}\text{ (min)} = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{ß_1}} + V_{T1}(\text{max})$$

$$-3 = -5 + V_{DS5} + \sqrt{\frac{100\ \mu A}{17\ \frac{\mu A}{V^2}\ S_1}} + 1.2$$

$$V_{DS5} = 0.8 - \sqrt{\frac{100}{(17)(231)}} = 0.8 - 0.1596 = 0.641$$

$$V_{DS5\ (sat)} = 0.641 = \sqrt{\frac{2(100\ \mu A)}{(17\ \frac{\mu A}{V^2})S_5}}$$

$$S_5 = \frac{2(100\mu A)}{17\mu A/V^2(0.641)^2} = 28.6$$

9.) V_{BIAS} -

$$I_5 = \frac{K_N' \cdot 28.6}{2}(V_{BIAS} + 5 - 1)^2 = 100\ \mu A$$

$$V_{BIAS} = 0.411 - 4 = -3.359V$$

10.) Summary of design -

$S_1 = S_2 = 231$

$S_3 = S_4 = 25$

$S_5 = 28.6$

$S_6 = S_9 = S_{C2} = S_{C3} = 62.5$

$S_7 = S_8 = S_{C1} = 29.4$

$V_{BP} = 2V$

$V_{BN} = -2V$

$V_{BIAS} = -3.359V$

11.) Check on power dissipation

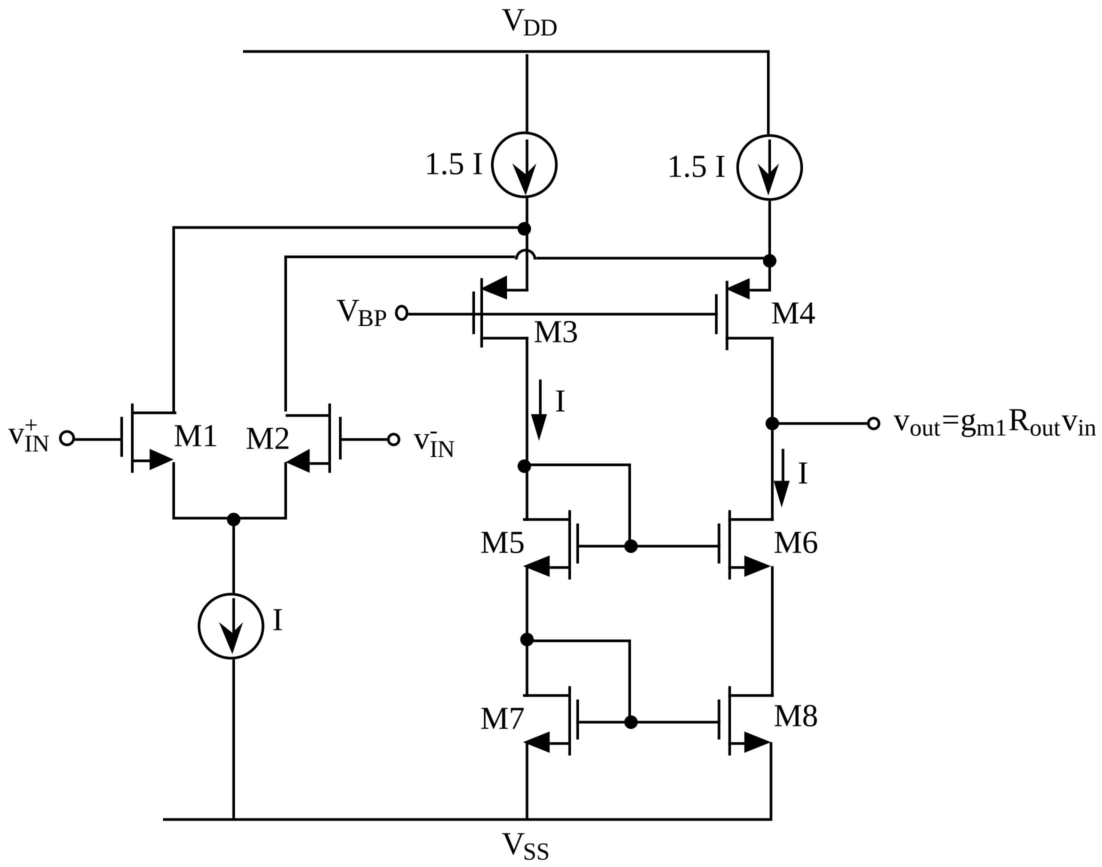
$$P_{diss} = 10(I_8 + I_5 + I_7) = 10(125\mu A + 100\mu A + 125\mu A)$$

$$= 3.5mW$$

12.) Design W's for lateral diffusion and simulate

X.3 FOLDED CASCODE ARCHITECTURE

Principle



Currents in upper current sinks must be greater than I to avoid zero current in the cascode mirror (M5-M8).

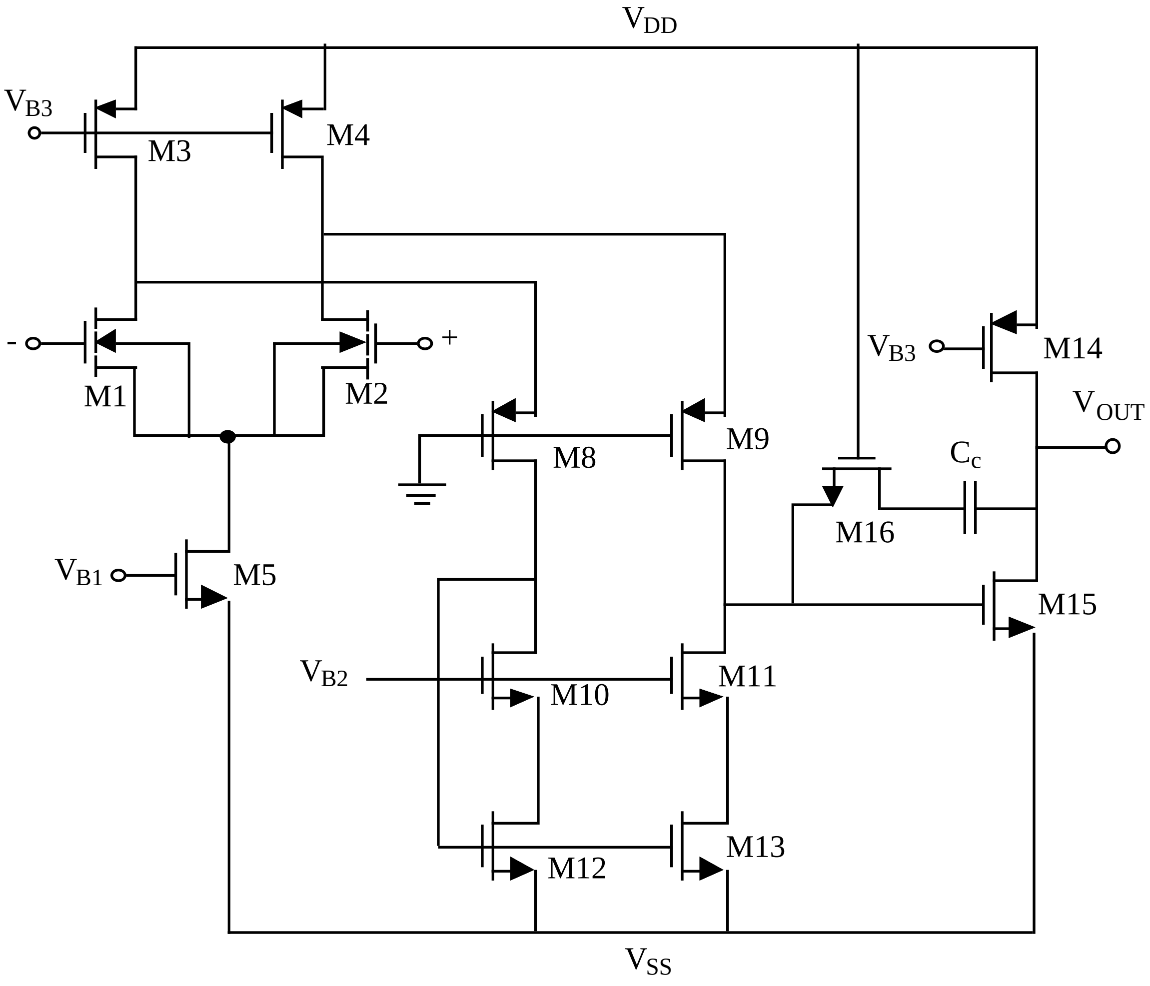
Advantages

Good input CMR.

Good frequency response.

Self compensating.

Folded Cascode OP Amp

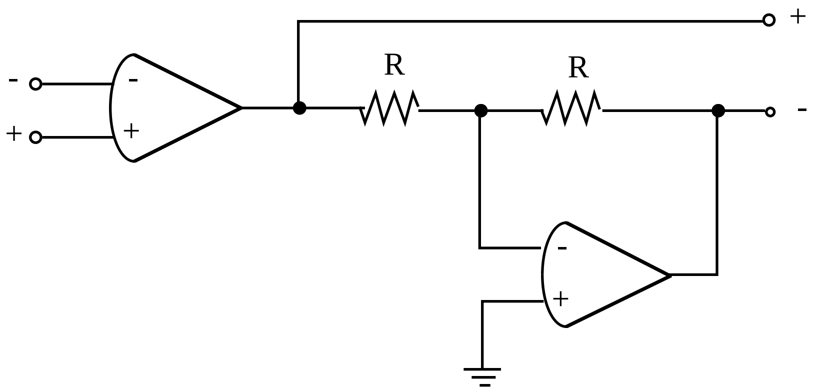


High gain, High speed, cascode amp

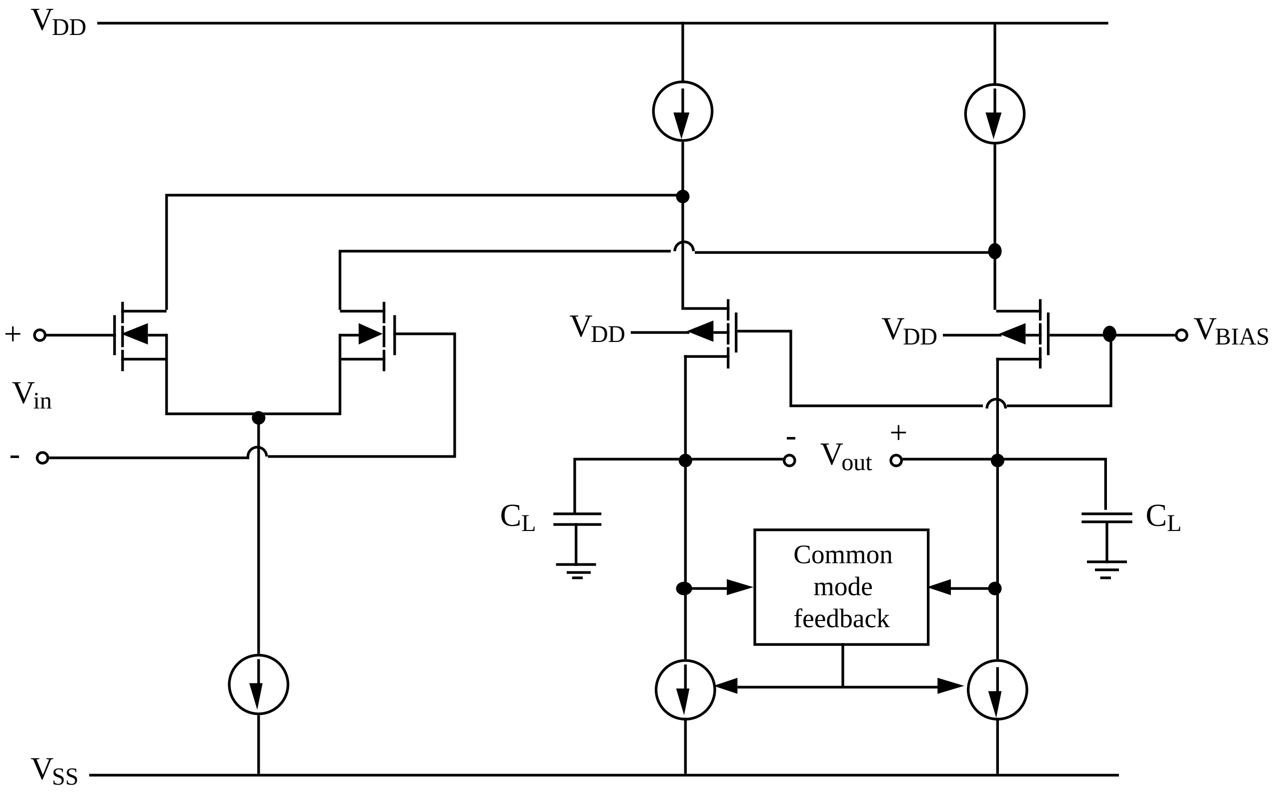
GB ≈ 10 MHz, A_{VDC} ≈ 100 dB

XI. 4 DIFFERENTIAL OUTPUT OTA'S

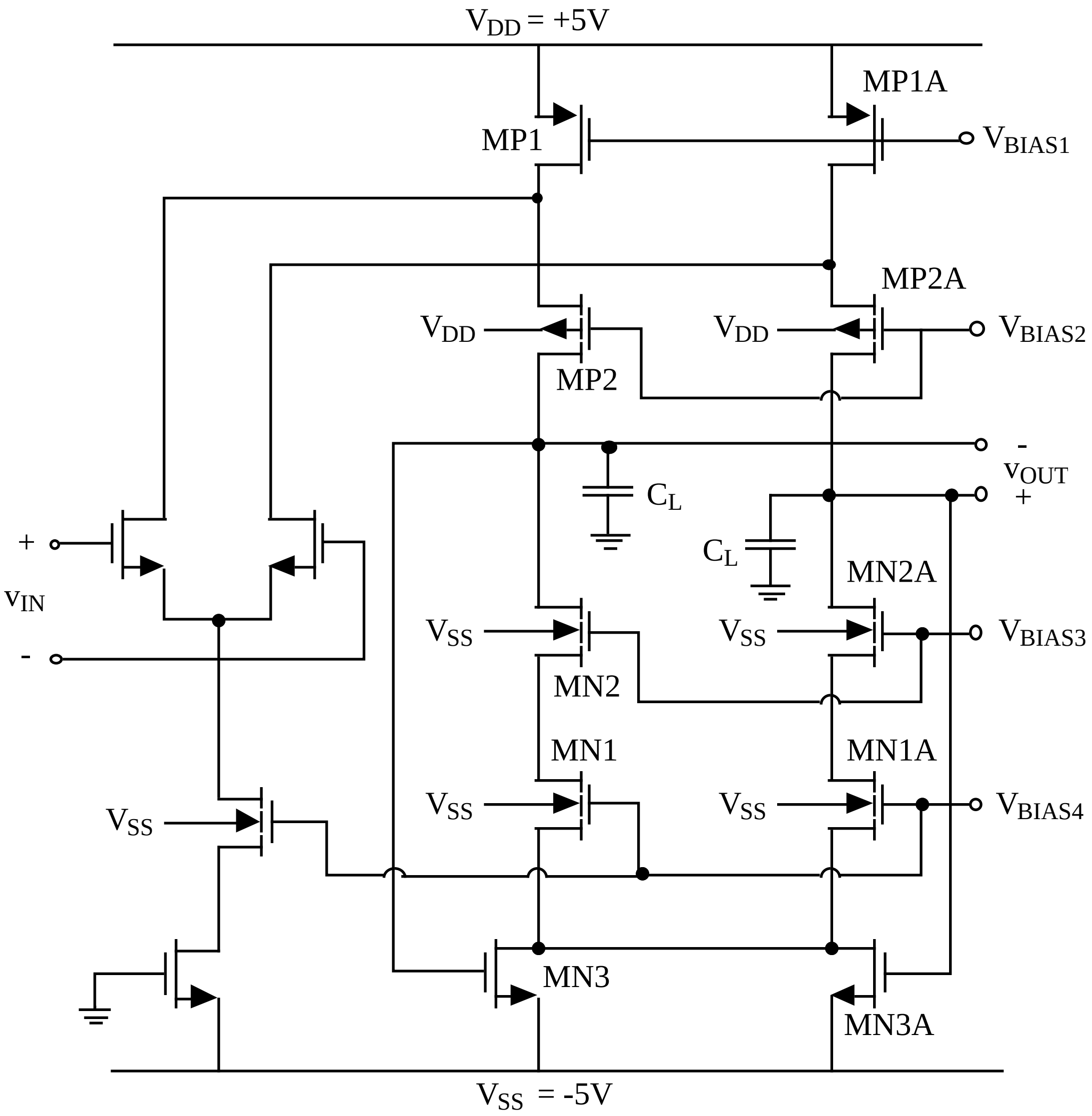
Implementation Using Two Differential-In, Singled-Ended Op Amps



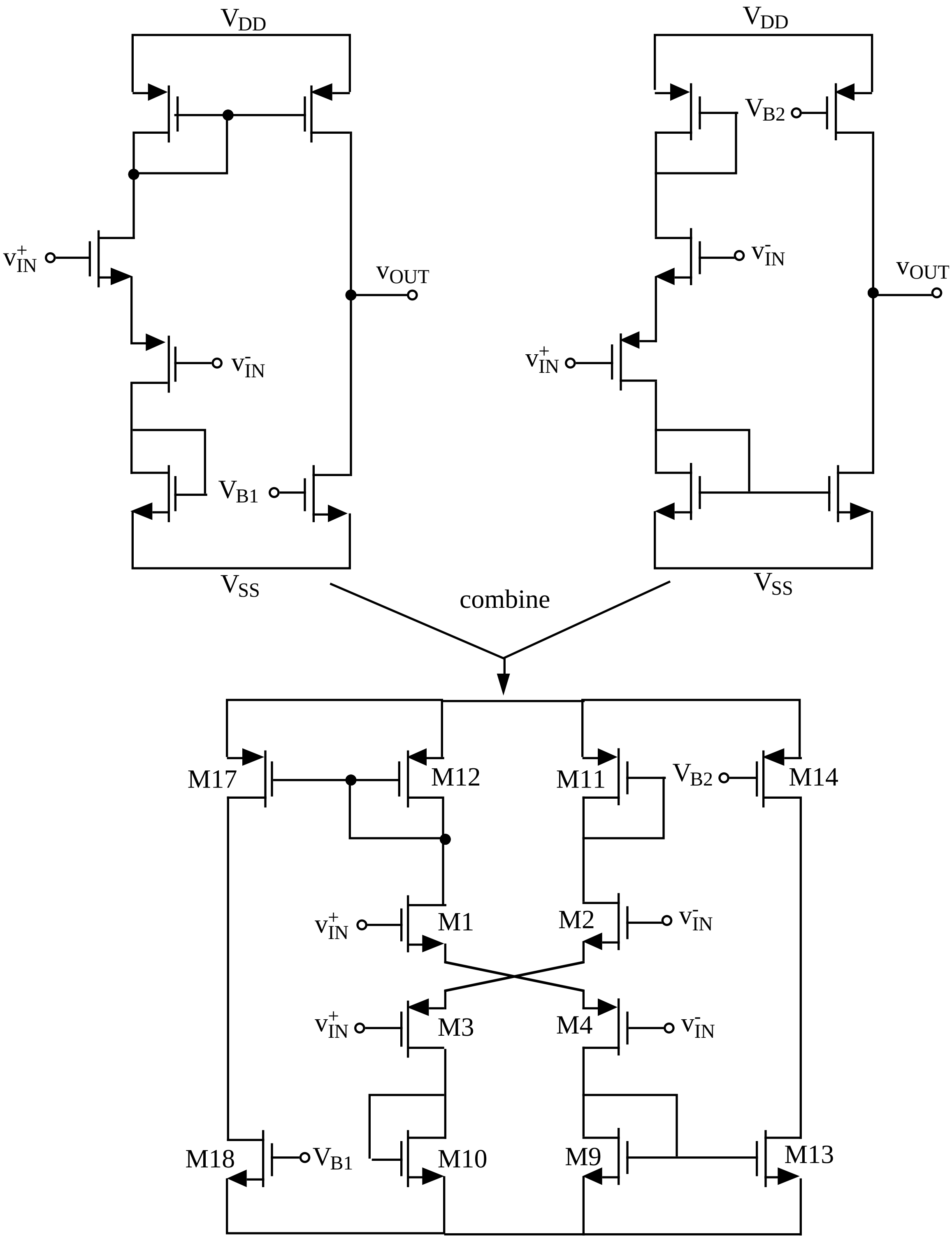
Conceptual Implementation of Differential In-Out OP Amp



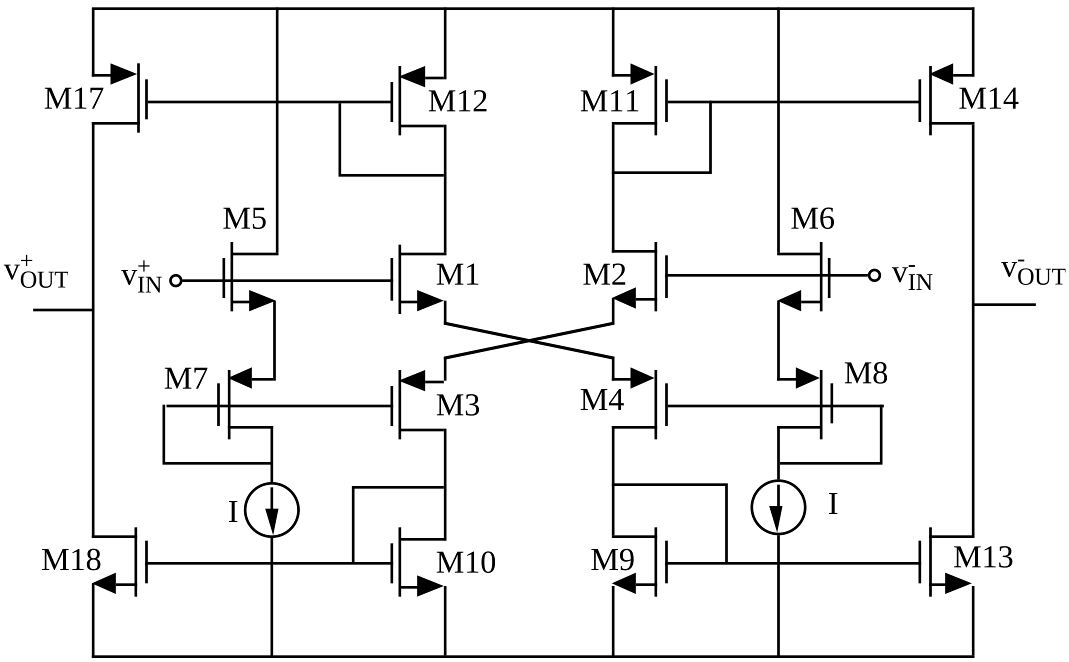
Schematic of a Fully Differential In-Out, FoldedCascode Op Amp



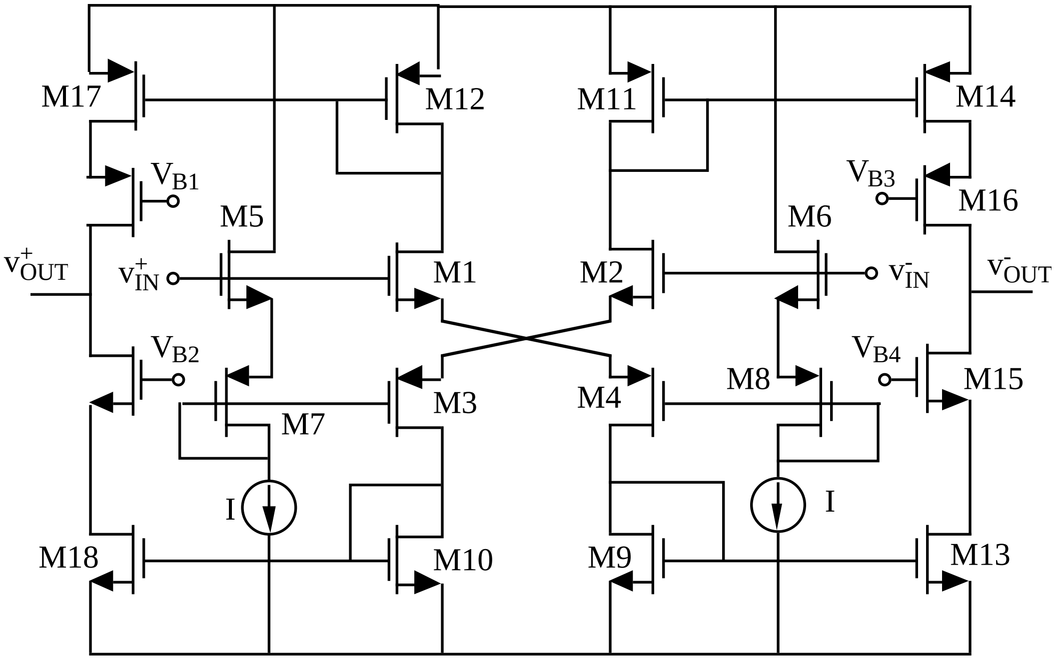
Evolution of Class AB Amplifier



Problem: DC levels of input voltages incompatible



DC problem solved, but amplifier has low gain and requires CM feedback



Gain improved using cascode

IX.5 LOW POWER AMPLIFIERS

General

Objective is to minimize the dc power dissipation.

Typical applications are:

1. Battery powered circuits.
2. Biomedical instrumentation.
3. Low power analog "VLSI."

Weak Inversion or Subthreshold Operation

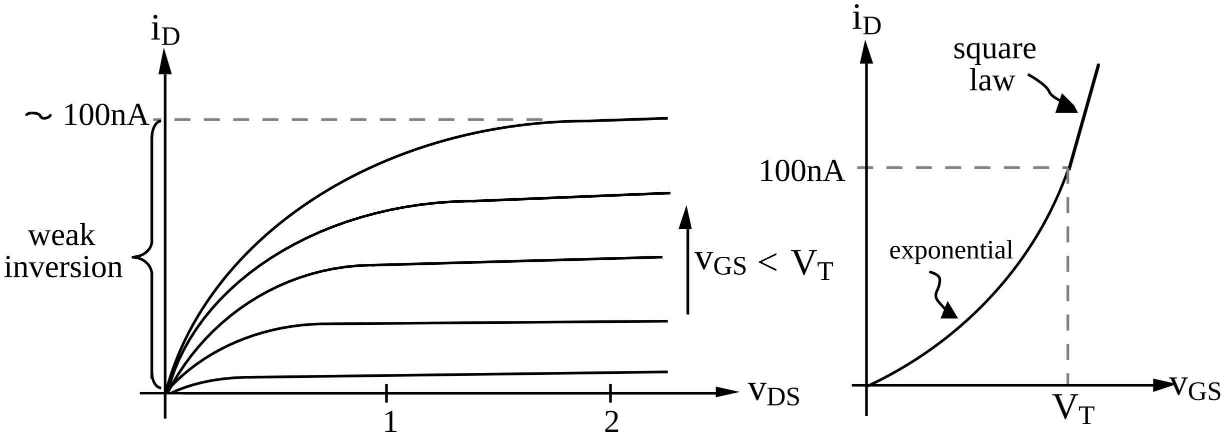
Drain current -

$$i_D = \left(\frac{W}{L}\right) I_D \exp\left(\frac{qv_{GS}}{nkT}\right)(1 + \lambda v_{DS})$$

Small signal parameters -

$$g_m = \frac{qi_D}{nkT}\ , \qquad r_{ds} \approx (\lambda i_D)^{-1}$$

Device characteristics -



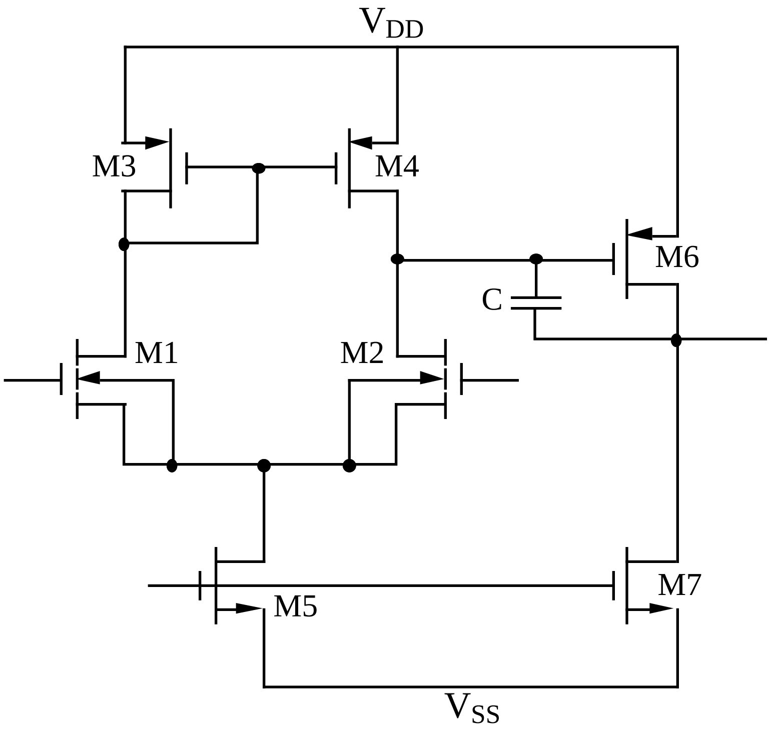
Op Amp Operating in Weak Inversion

Consider the two-stage op amp with reduced currents and power supplieds,

$$A_V = \frac{g_{m2}g_{m6}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} = \frac{1}{n_2 n_6 (kT/q)^2 (\lambda_2+\lambda_4)(\lambda_6+\lambda_7)}$$

where,

$$GB = \frac{g_{m1}}{C} = \frac{I_{D1}}{(n_1 kT/q)C} \quad \text{and} \quad SR = \frac{2I_{D1}}{C} = 2GB\left(\frac{n_1 kT}{q}\right)$$



Design Example

Calculate the gain, unity-gain bandwidth, and slew rate of the previous two-stage op amp used in weak inversion if:

$I_{D5} = 200\text{nA}$ $n_P = 1.5$ $\lambda_P = 0.02\text{V}^{-1}$

$L = 10\ \mu\text{m}$ $n_N = 2.5$ $\lambda_N = 0.01\text{V}^{-1}$

$C = 5\text{pF}$ $T = 27^\circ\text{C}$

$$A_V = \frac{1}{(1.5)(2.5)(0.026)(2)(0.1+0.02)(0.01+0.02)} = 5698$$

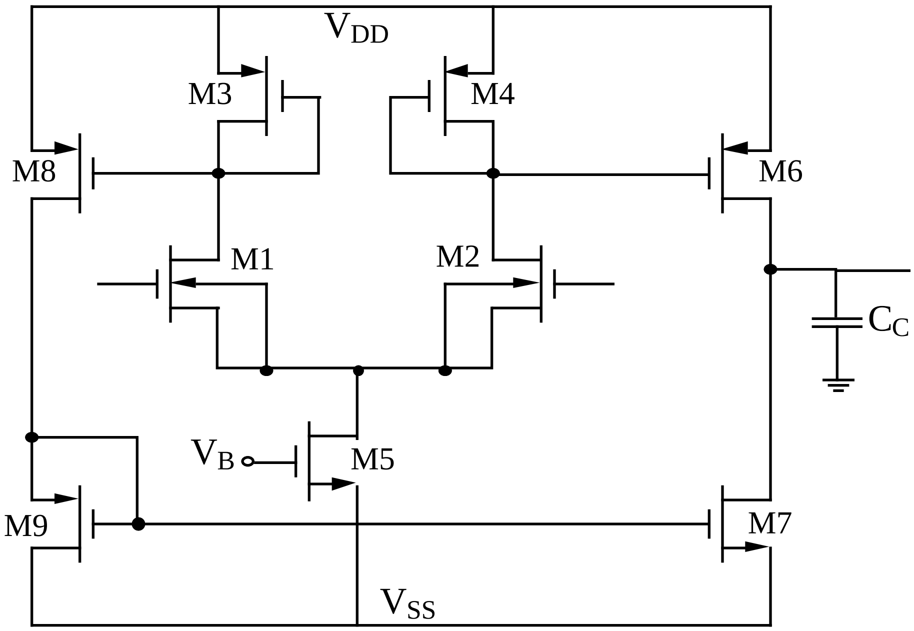
$$GB = \frac{100\cdot 10^{-9}}{(2.5)(0.026)(5\cdot 10^{-12})} = 307.69\text{Krps or } 48.97\text{KHz}$$

$$SR = 2(153.85\cdot 10^{3})(2.5)(0.026) = 0.04\text{V}/\mu\text{s}$$

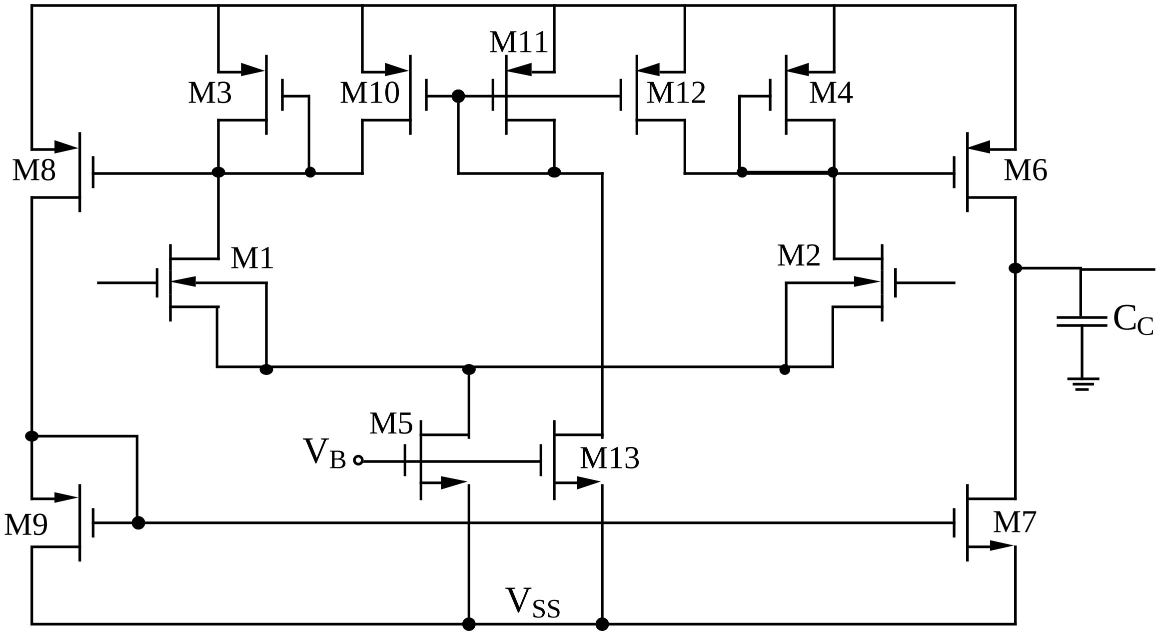
If $V_{DD} = -V_{SS} = 2.5$, the power dissipation is 0.2μW assuming $I_{D7} = I_{D5}$.

Push-Pull Micropower Op Amp

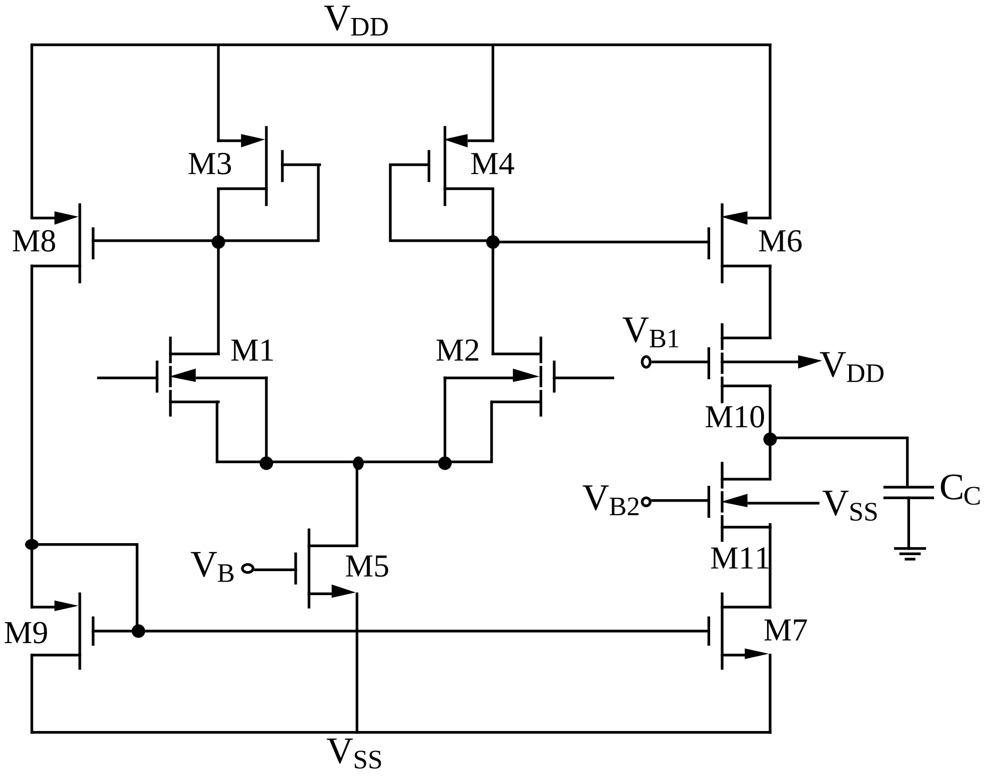
First stage clamped (low gain, low bias current)-



Gain enhancement for Push-Pull Micropower Op Amp



Push-Pull Cascode Micropower Op Amp

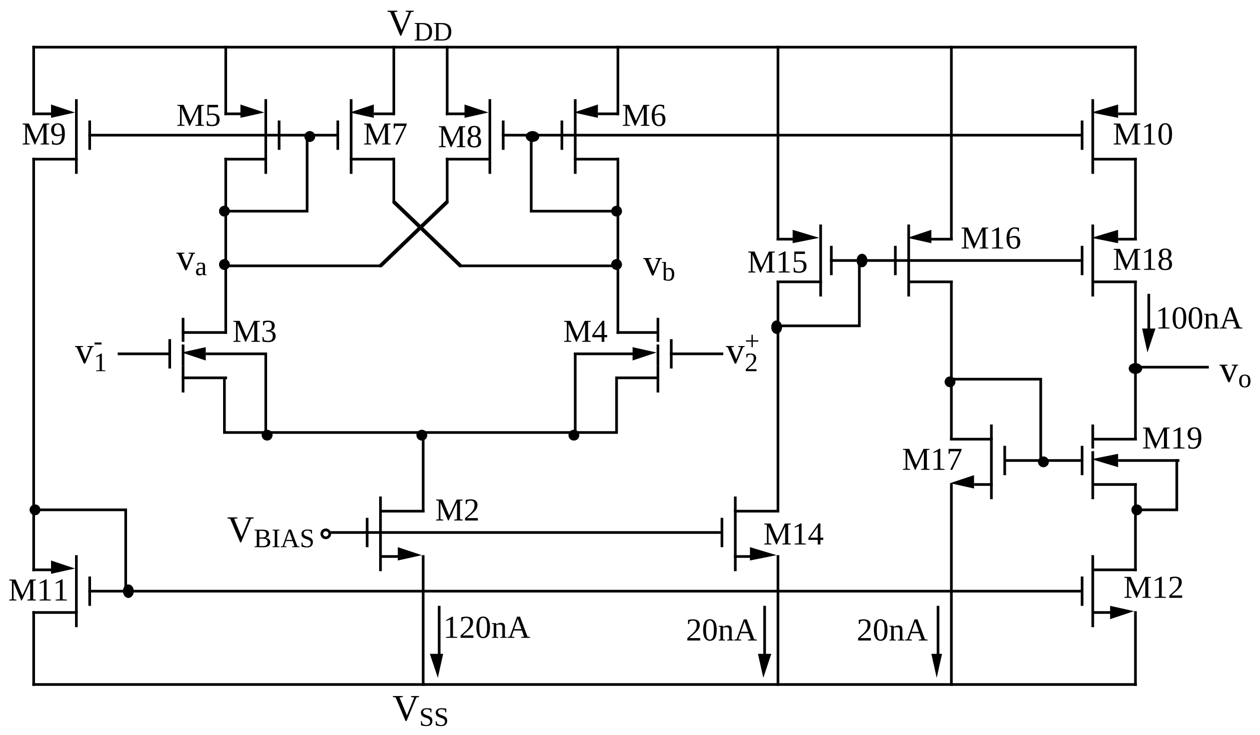


$$A_V = \frac{\frac{1}{n_N} + \frac{1}{n_P}}{V_t^2(\lambda_P{}^2 n_P + \lambda_N{}^2 n_N{}^2)} \approx 10{,}000$$

self-compensating

Low power << 1 μW

Micropower Op Amp



$$P_{diss} = |V_{DD}-V_{SS}|(260nA)$$

$$v_o = v_a g_{m9} r_o - v_b g_{m10} r_o \approx g_{m9} r_o (v_a - v_b) \quad ; g_{m9} = g_{m10}$$

where

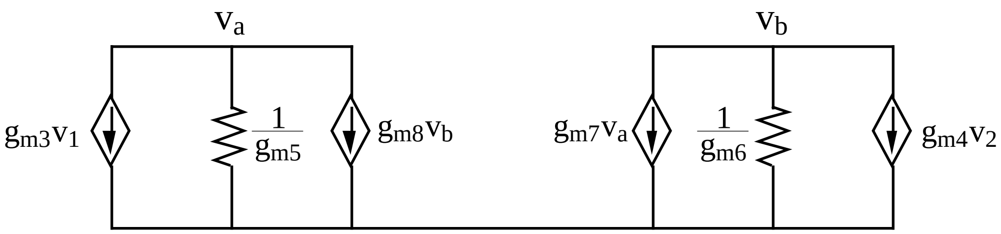
$$r_o \approx (r_{ds10} g_{m18} r_{ds18})||(r_{ds12} g_{m19} r_{ds19})$$

and

$$(v_a - v_b) = \quad v_a - v_b = \frac{n_P}{n_N}\left(\frac{1 + k}{1 - k}\right)(v_2 - v_1)$$

(See following pages)

Small-Signal Analysis



$$v_a = -v_1 \frac{g_{m3}}{g_{m5}} - v_b \frac{g_{m8}}{g_{m5}}$$

$$v_b = -v_2 \frac{g_{m4}}{g_{m6}} - v_a \frac{g_{m7}}{g_{m6}}$$

$$\begin{bmatrix} v_1\frac{g_{m3}}{g_{m5}} \\ v_2\frac{g_{m4}}{g_{m6}} \end{bmatrix} = \begin{bmatrix} -1 & -\frac{g_{m8}}{g_{m5}} \\ -\frac{g_{m7}}{g_{m4}} & -1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix}$$

$$v_a = \frac{\begin{vmatrix} v_1\frac{g_{m3}}{g_{m5}} & -\frac{g_{m8}}{g_{m5}} \\ v_2\frac{g_{m4}}{g_{m6}} & -1 \end{vmatrix}}{\begin{vmatrix} -1 & -\frac{g_{m8}}{g_{m5}} \\ -\frac{g_{m7}}{g_{m4}} & -1 \end{vmatrix}} = \frac{-v_1\frac{g_{m3}}{g_{m5}} + v_2\frac{g_{m4}g_{m8}}{g_{m5}g_{m6}}}{1 - \frac{g_{m7}g_{m8}}{g_{m5}g_{m6}}}$$

$$v_b = \frac{\begin{vmatrix} -1 & v_1\dfrac{g_{m3}}{g_{m5}} \\ -\dfrac{g_{m7}}{g_{m6}} & v_2\dfrac{g_{m4}}{g_{m6}} \end{vmatrix}}{\begin{vmatrix} -1 & -\dfrac{g_{m8}}{g_{m5}} \\ -\dfrac{g_{m7}}{g_{m4}} & -1 \end{vmatrix}} = \frac{-v_2\dfrac{g_{m4}}{g_{m6}} + v_1\dfrac{g_{m3}g_{m7}}{g_{m5}g_{m6}}}{1 - \dfrac{g_{m7}g_{m8}}{g_{m5}g_{m6}}}$$

$$v_a - v_b = \frac{\left(-v_1\dfrac{g_{m3}}{g_{m5}} + v_2\dfrac{g_{m4}g_{m8}}{g_{m5}g_{m6}}\right) - \left(-v_2\dfrac{g_{m4}}{g_{m6}} + v_1\dfrac{g_{m3}g_{m7}}{g_{m5}g_{m6}}\right)}{1 - \dfrac{g_{m7}g_{m8}}{g_{m5}g_{m4}}}$$

$g_{m3} = g_{m4} = g_{mI}$; $g_{m5} = g_{m6} = g_{mII}$; $g_{m7} = g_{m8} = g_{mIII}$

Then

$$v_a - v_b = \frac{\left(-v_1\dfrac{g_{mI}}{g_{mII}} + v_2\dfrac{g_{mI}g_{mIII}}{g_{mII}^2}\right) - \left(-v_2\dfrac{g_{mI}}{g_{mII}} + v_1\dfrac{g_{mI}g_{mIII}}{g_{mII}^2}\right)}{1 - \dfrac{g_{mIII}^2}{g_{mII}^2}}$$

Define: $\dfrac{g_{mIII}}{g_{mII}} = k$

$$v_a - v_b = \frac{(v_2 - v_1)\dfrac{g_{mI}}{g_{mII}}(1 + k)}{1 - k^2} = (v_2 - v_1)\frac{\left(\dfrac{g_{mI}}{g_{mII}}\right)}{1 - k}$$

$$v_a - v_b = \frac{g_{mI}}{g_{mII}}\left(\frac{1}{1 - k}\right)(v_2 - v_1)$$

Consider dc currents under balanced condititions:

$$I_4 = I_6 + I_7$$

$$I_3 = I_5 + I_8$$

$$I_8 = I_6\left(\frac{S_8}{S_6}\right) \;;\quad I_7 = I_5\left(\frac{S_7}{S_5}\right)$$

$$\frac{I_8}{I_6} = \frac{S_8}{S_6} \;\Rightarrow\; \text{in W.I. } g_m \text{ is proportional to I}$$

$$\frac{I_8}{I_6} = \frac{S_8}{S_6} = k; \quad \frac{I_7}{I_5} = \frac{S_7}{S_5} = k$$

Since under balanced conditions

$$I_3 = I_4 \;;\; I_4 = I_5$$

$$I_4 = I_6\,(1 + k)$$

$$I_3 = I_5\,(1 + k)$$

Again, since $g_m \propto I$ in weak inversion, then

$$g_{m4} \propto I_6(1 + k) \quad \text{or} \quad g_{m4} = \frac{I_6}{n_N \frac{kT}{q}}(1 + k)$$

and

$$g_{m3} \propto I_5(1 + k)$$

since

$$g_{m3} = g_{m4} = g_{mI} \;\Rightarrow\; g_{mI} = \frac{I_6}{n_N \frac{kT}{q}}(1 + k)$$

Also

$$g_{m4} = g_{mII} = \frac{I_6}{n_N \frac{kT}{q}}$$

then

$$\frac{g_{mI}}{g_{mII}} = \left(\frac{n_P}{n_N}\right)(1 + k)$$

finally:

$$v_a - v_b = \frac{n_P}{n_N}\left(\frac{1 + k}{1 - k}\right)(v_2 - v_1)$$

$$\approx \frac{1 + k}{1 - k}(v_2 - v_1)$$

Therefore,

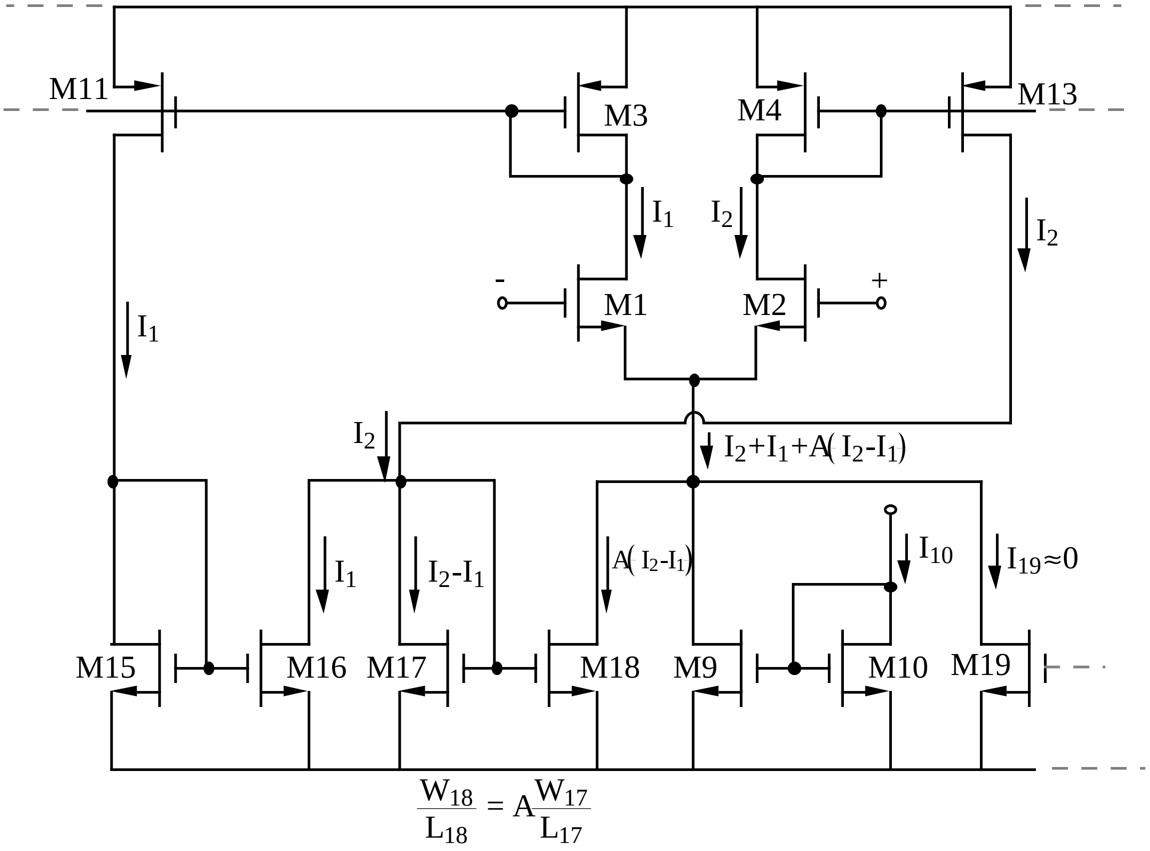
$$v_o = g_{m9}\, r_o\left(\frac{1+k}{1-k}\right)v_{id}$$

OTA CURRENT OVERDRIVE

Need large sinking and source currents without having to have large quiescent currents.

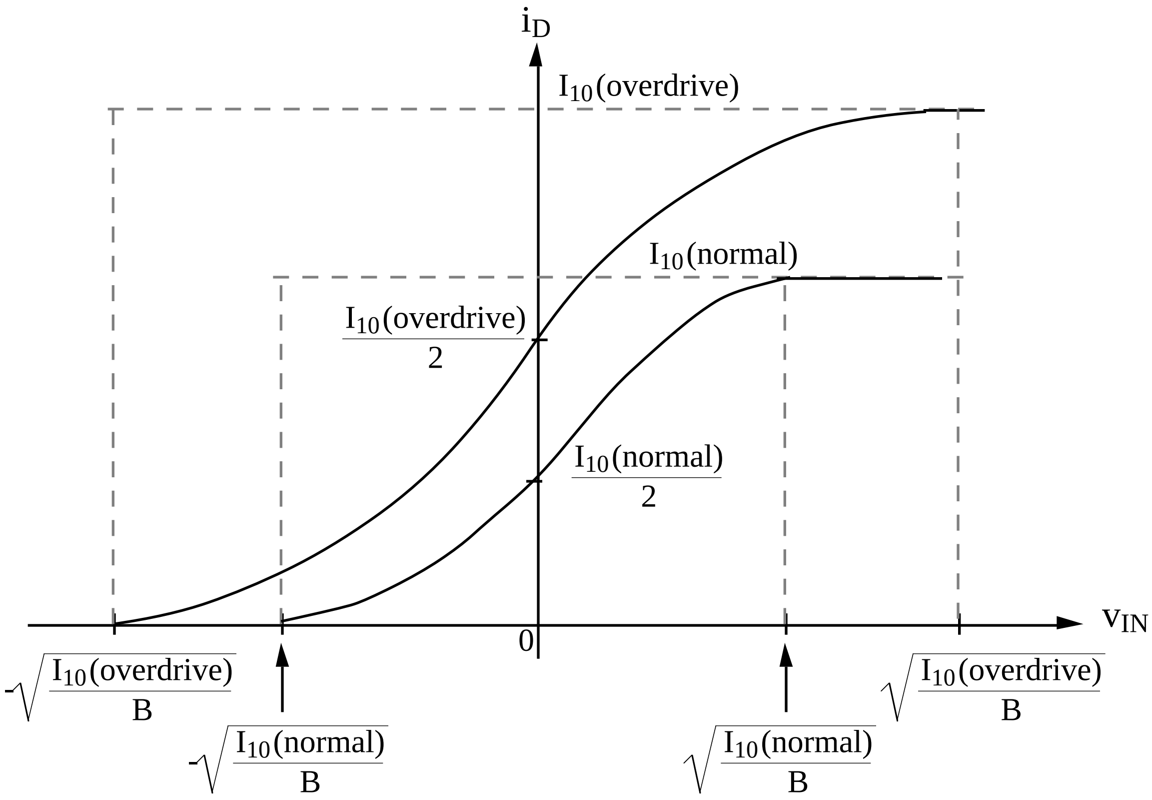
One possible solution uses "tail current boosting" -

Assume that $S_3 = S_4 = S_{11} = S_{13}$, $S_{18} = AS_{17}$, $S_{15} = S_{16} = S_{17} = ..$



Principle in Achieving Current Overdrive

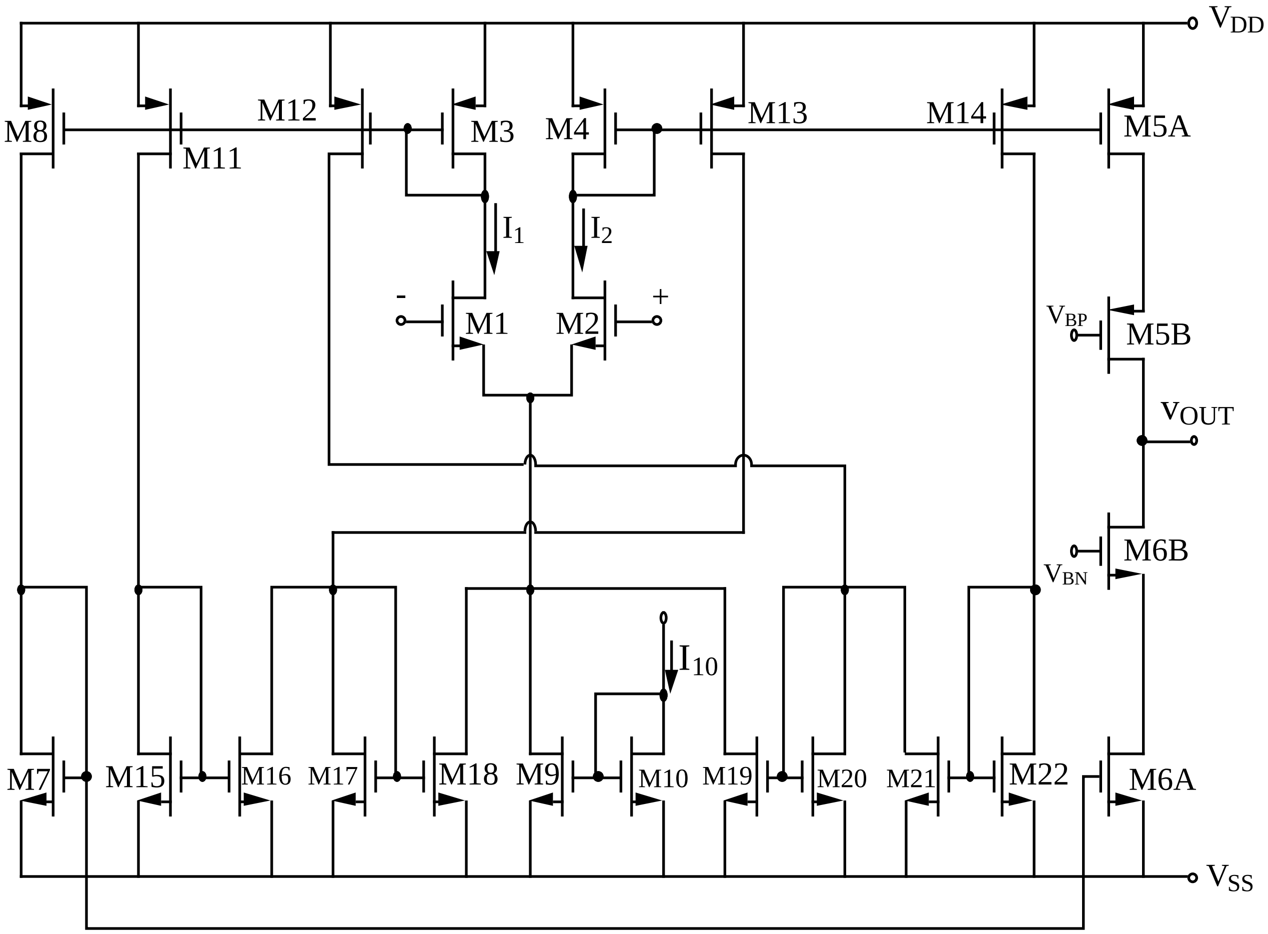
Differential amplifier transconductance characteristics -



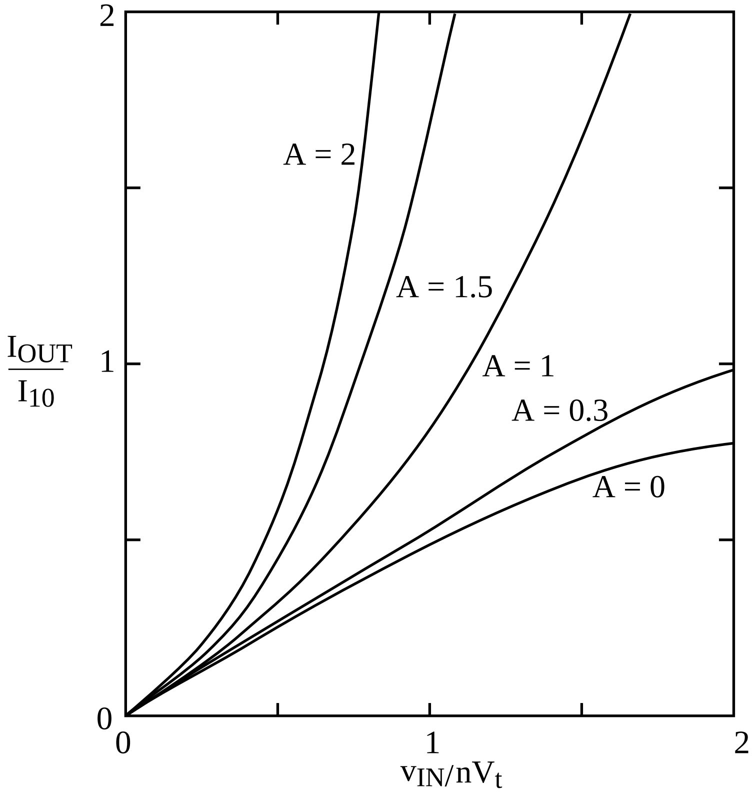
Positive feedback -

$$i_{OUT}\,(\text{max/min}) \approx \frac{I_{10}}{1 - \text{Loop gain}} = \frac{I_{10}}{1 - \frac{g_{m18}}{g_{m17}}\frac{g_{m13}}{g_{m14}}} = \frac{I_{10}}{1 - \frac{g_{m13}}{g_{m9}}A}$$

A Dynamically Biased Micropower Op Amp



Parametric Overdrive Curves for Dynamically Biased Op Amp



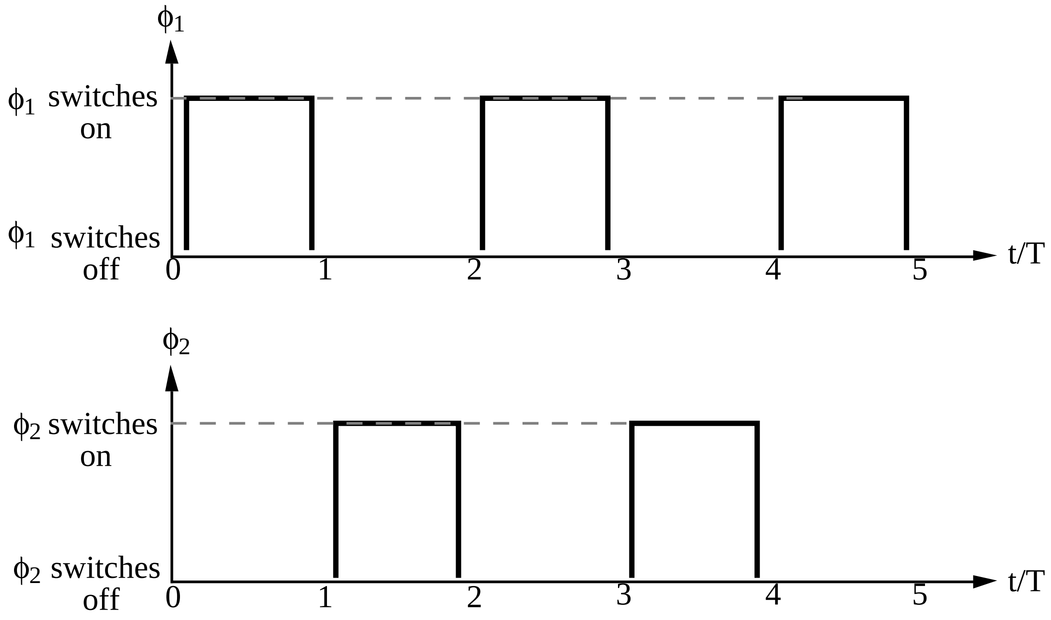
IX.7 - DYNAMICALLY BIASED AMPLIFIERS

Dynamic circuits take advantage of the fact that many applications are synchronously clocked resulting in periods of time where the circuits is not functioning.

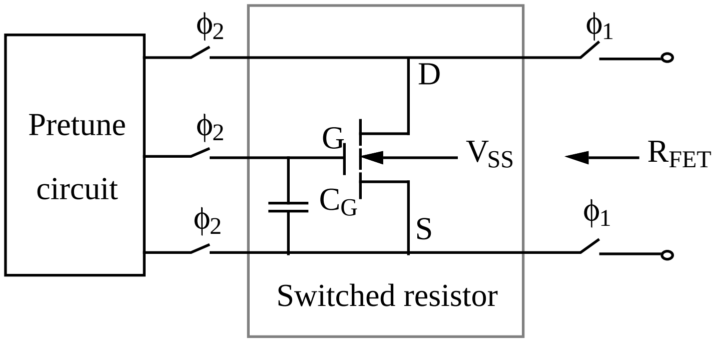
Will examine:

- Dynamic or switched resistors
- Dynamically biased amplifiers
- Dynamically biased, push-pull, cascode op amp

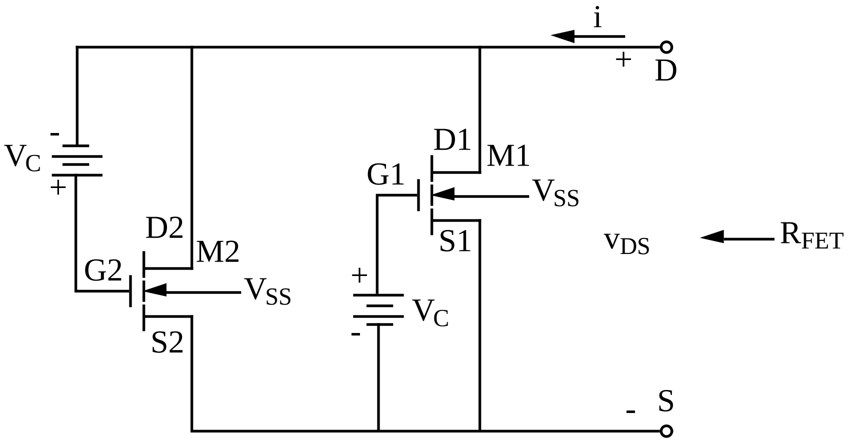
Two Phase Clock



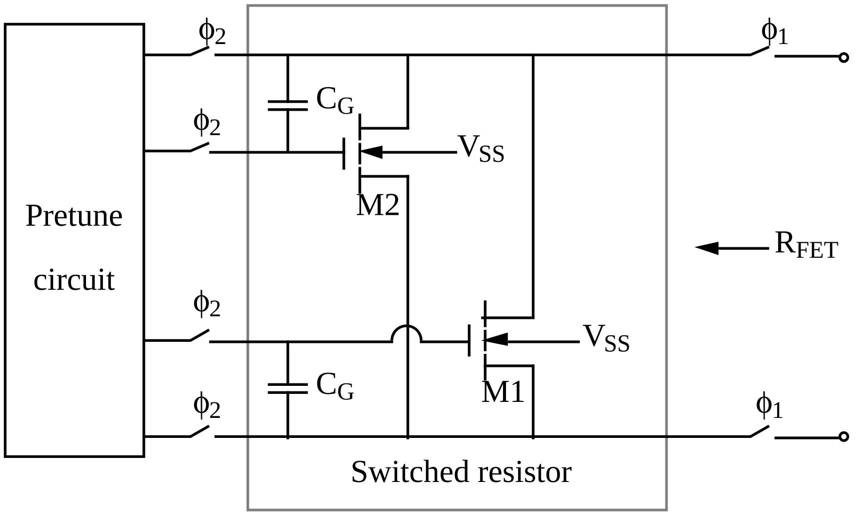
A Switched Resistance Realization



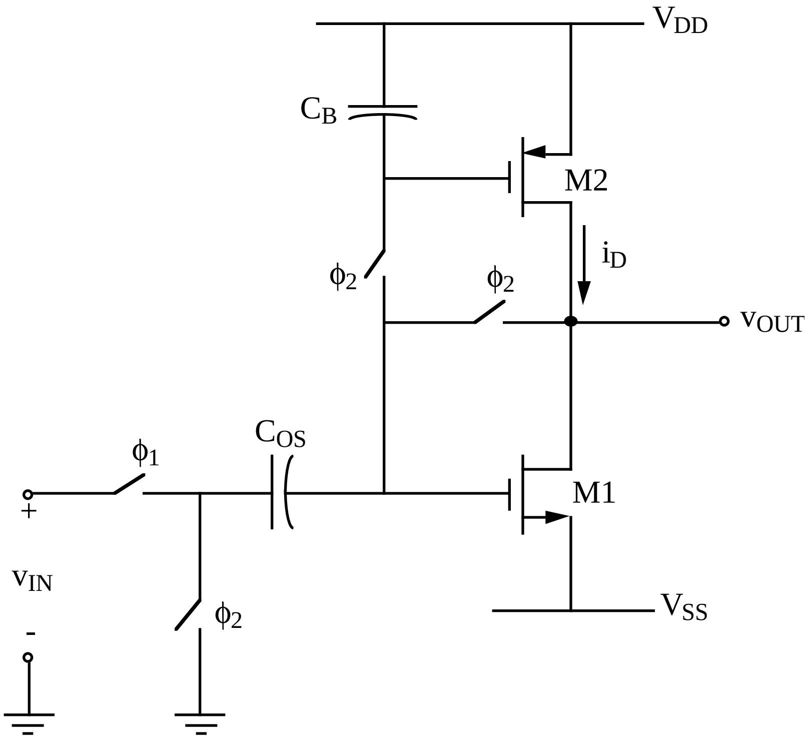
A Continuous Time Resistor Realization with Increased Signal Swing



Implementation of the Continuous Time Switched Resistor Realization using Dynamic Techniques



Dynamically Biased Inverter

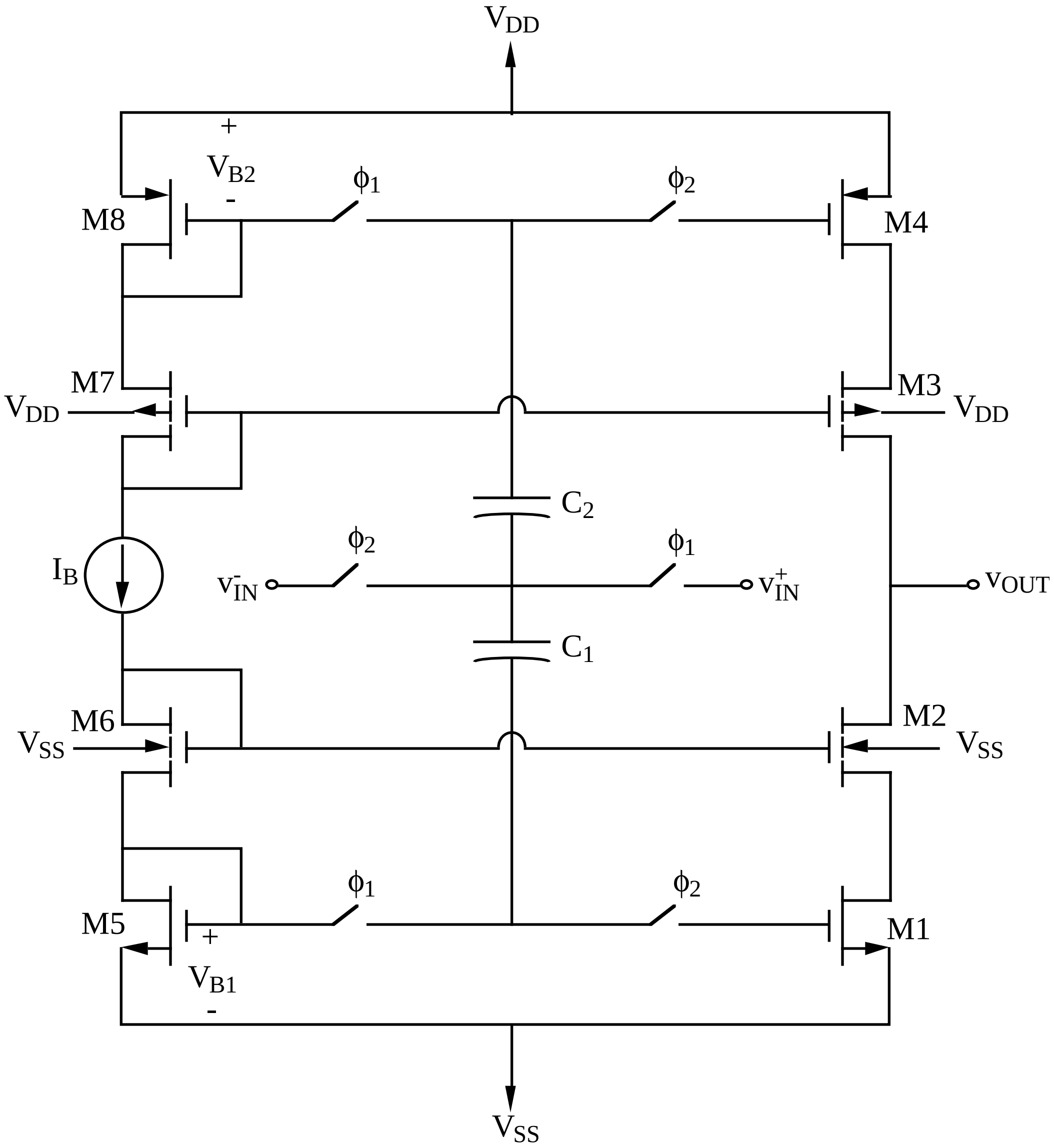


During phase 2 the offset and bias of the inverter is sampled and applied to C_{OS} and C_B.

During phase 1 C_{OS} is connected in series with the input and provides offset cancelling plus bias for M1. C_B provides the bias for M2.

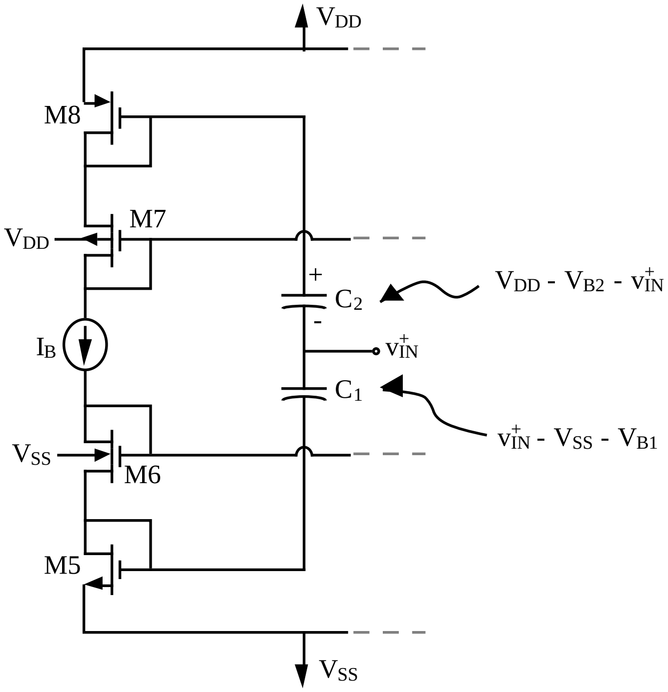
Dynamic, Push-pull, Cascode Op Amp

Simplified schematic -

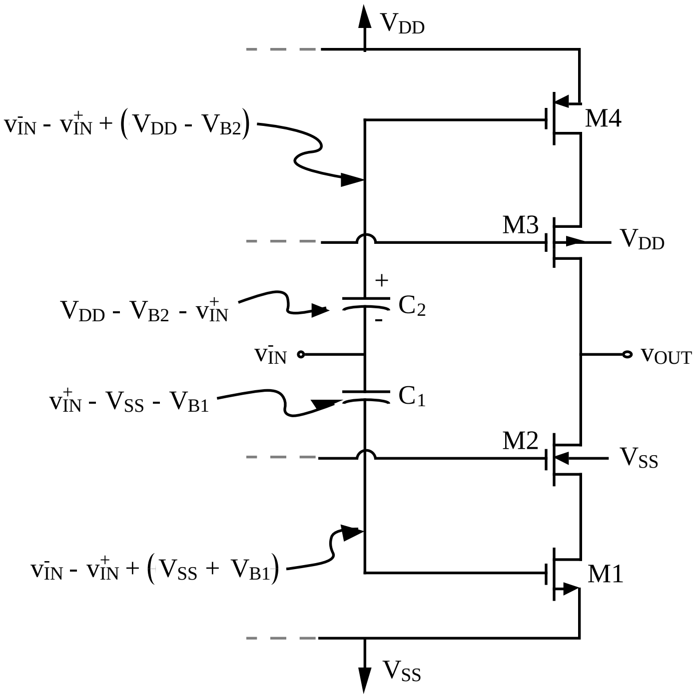


Dynamic, Push-pull, Cascode Op Amp - Cont'd

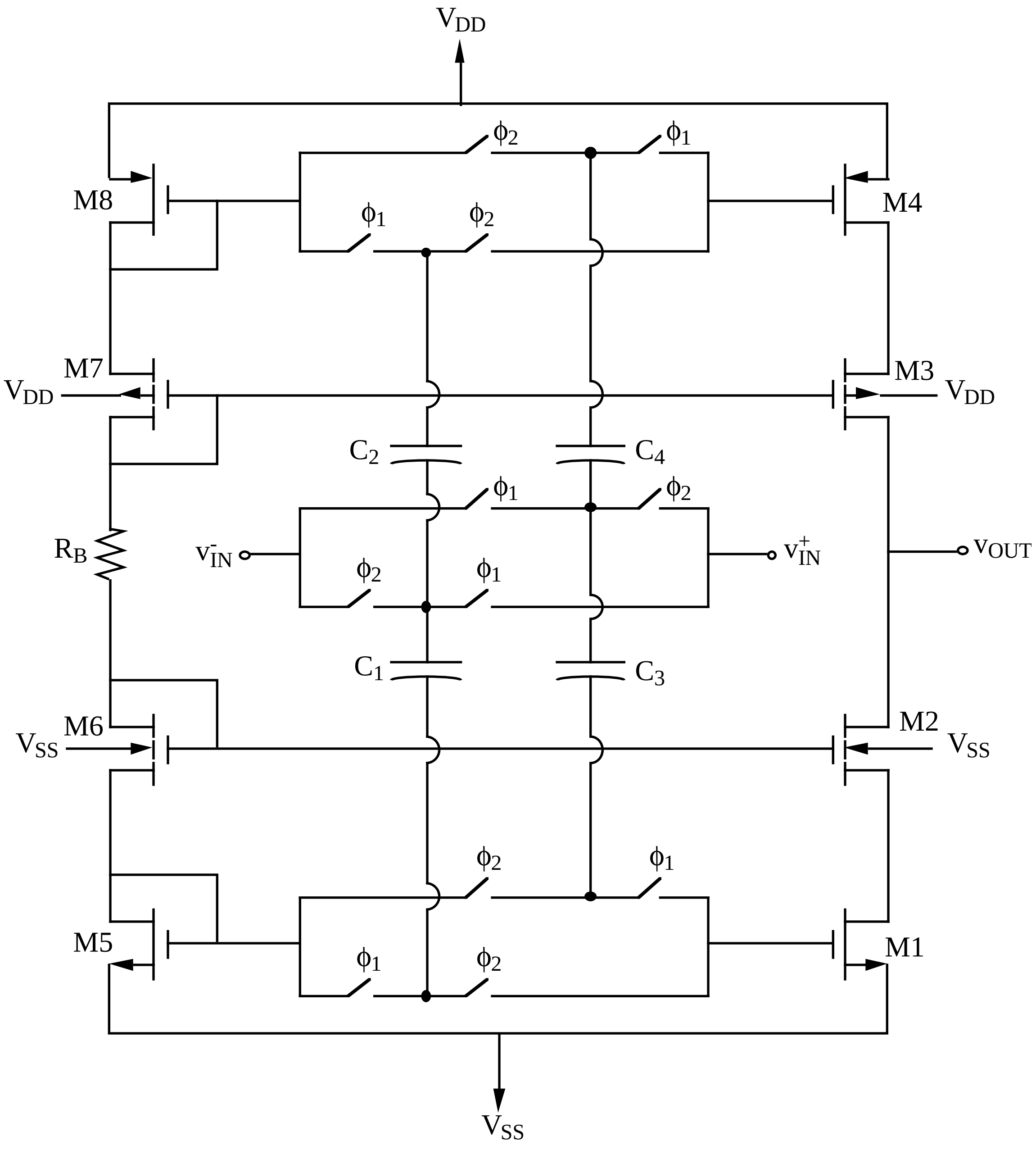
Phase 1 Clock Period



Phase 2 Clock Period



A Dynamic Op Amp which Operates on Both Clock Phases



1.6 mW dissipation Settling time = 10 ns into 5 pF

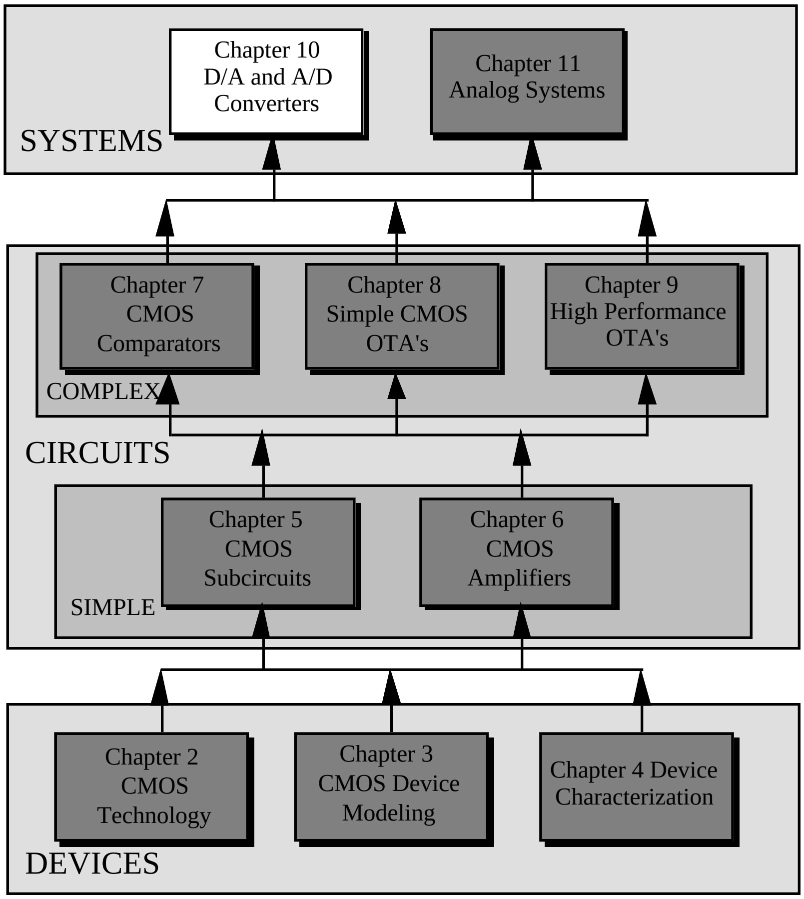
GB ≈ 130 MHz with C_L = 2.2 pF 1.5 µm technology

Used with a 28.6 MHz clock to realize a 5th order switched capacitor filter with a cutoff frequency of 3.5 MHz.

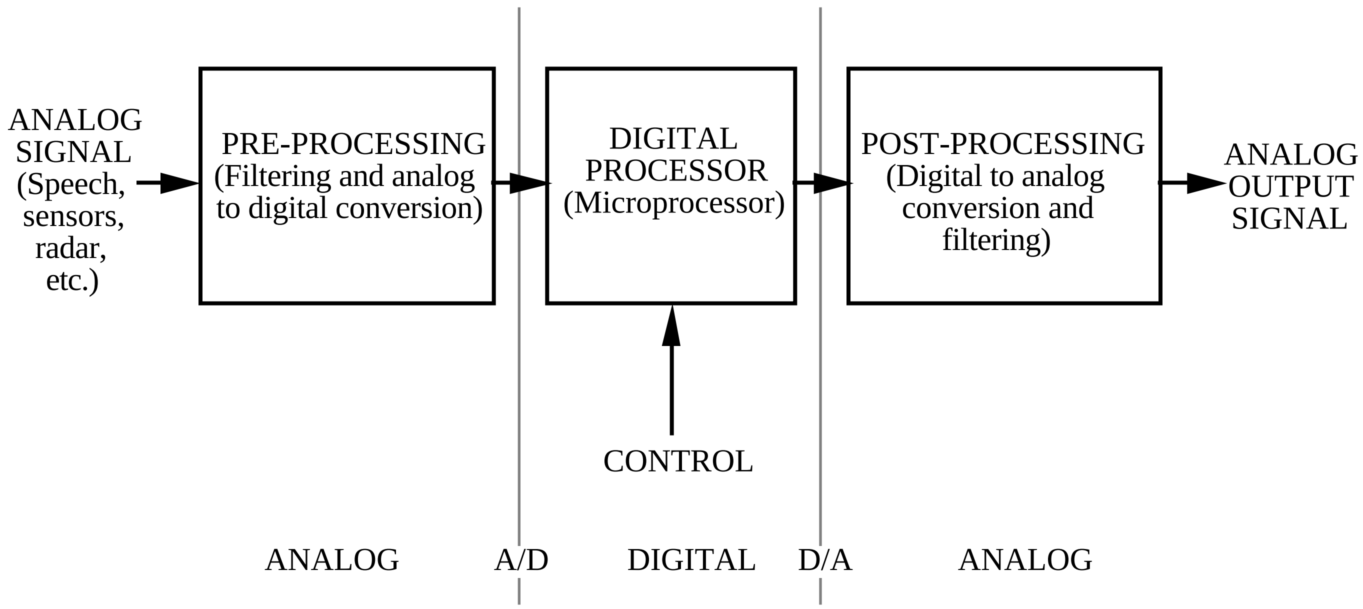
X. CMOS DATA CONVERTERS

Contents

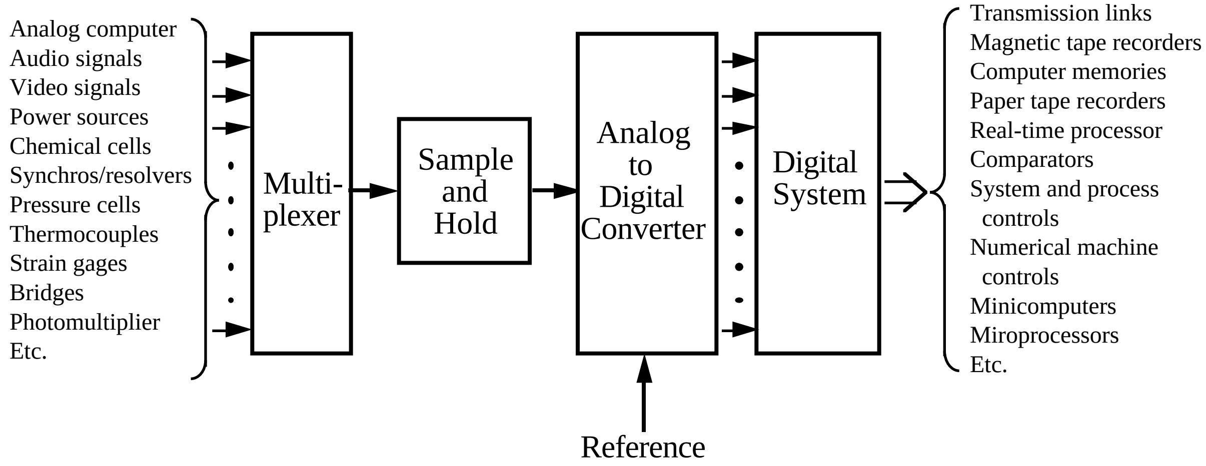
Organization

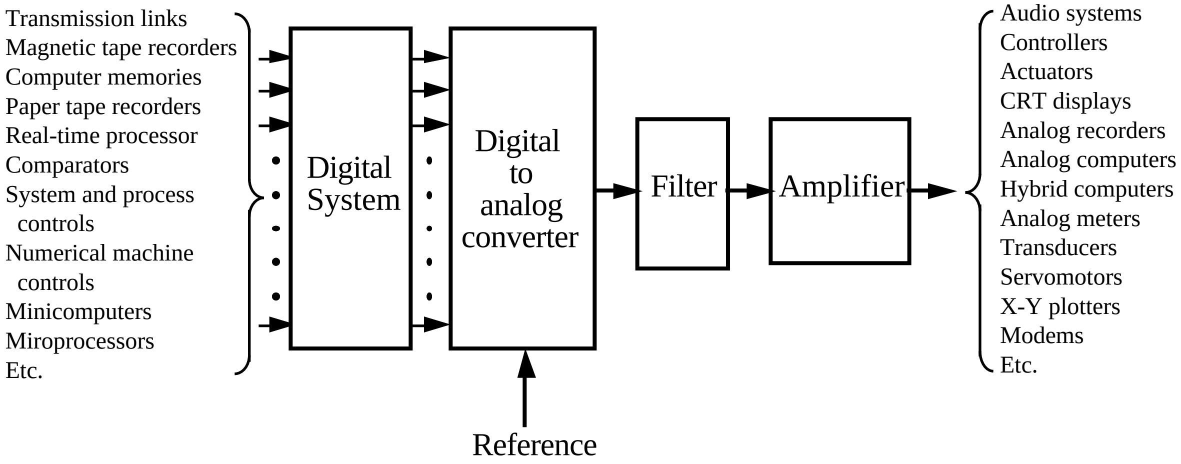


Importance of Data Converters in Signal Processing



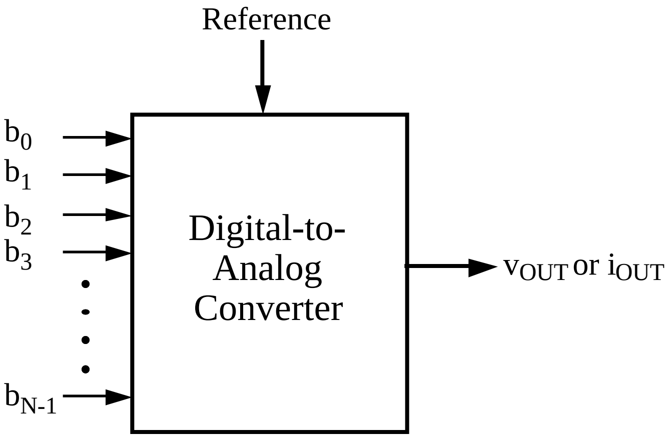
A/D and D/A Converters in Data Systems





X.1 - CHARACTERIZATION AND DEFINITION OF CONVERTERS

General Concept of Digital-to-Analog (D/A) Converters



$$v_{OUT} = KV_{ref}D \quad \text{or} \quad i_{OUT} = KI_{ref}D$$

where

K = gain constant (independent of digital input)

$$D = \frac{b_0}{2^N} + \frac{b_1}{2^{N-1}} + \frac{b_2}{2^{N-2}} + \cdots + \frac{b_{N-1}}{2^1} = \text{scaling factor}$$

V_{ref} (I_{ref}) = voltage (current) reference

b_{N-1} = most significant bit (MSB)

b_0 = least significant bit (LSB)

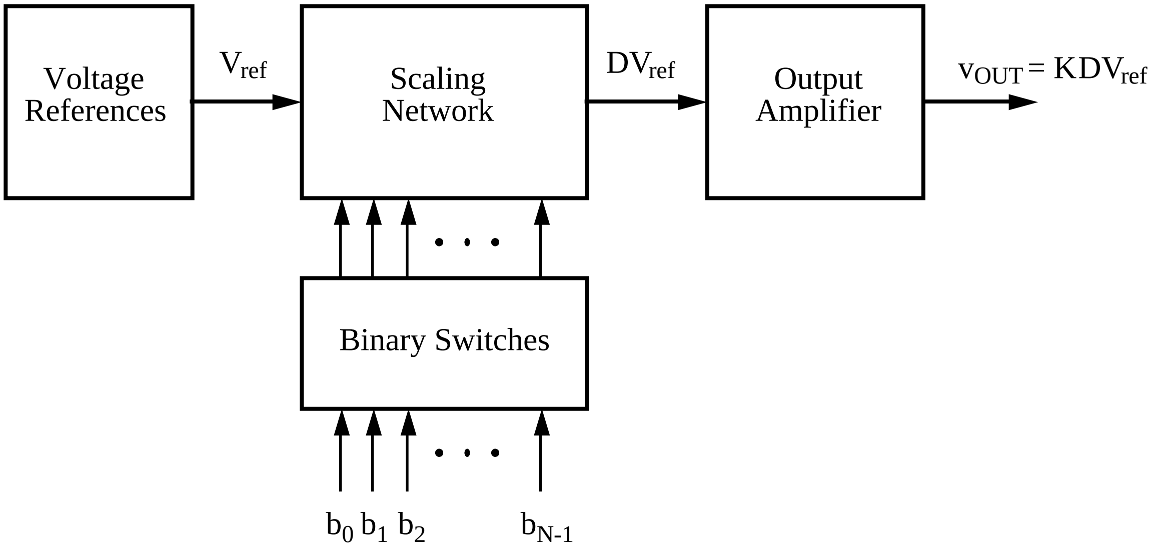
For example,

$$v_{OUT} = KV_{ref}\left(\frac{b_0}{2^N} + \frac{b_1}{2^{N-1}} + \frac{b_2}{2^{N-2}} + \cdots + \frac{b_{N-1}}{2^1}\right)$$

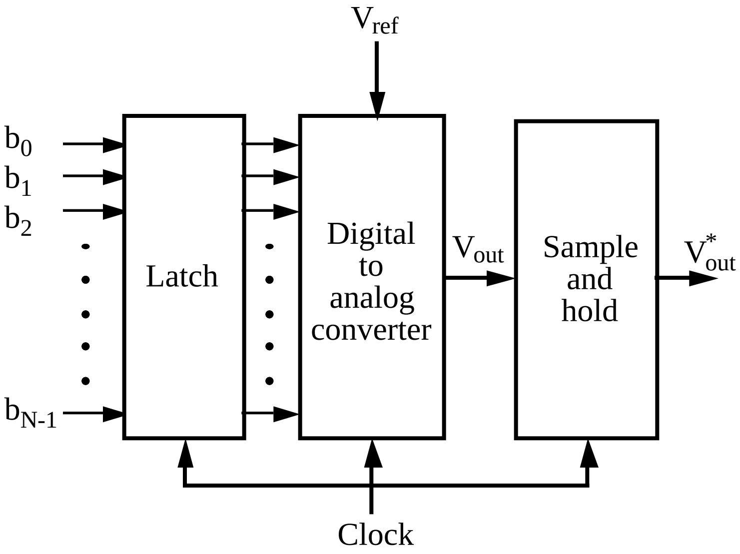
$$= KV_{ref}\frac{1}{2^N}\sum_{j=0}^{N-1} b_j 2^j$$

Basic Architecture of a D/A Converter

Continuous Time D/A Converter-

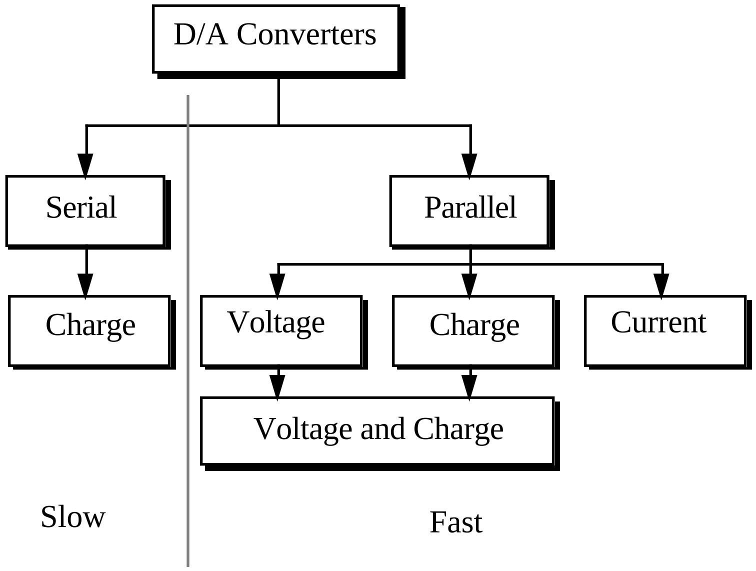


Clocked D/A Converter-



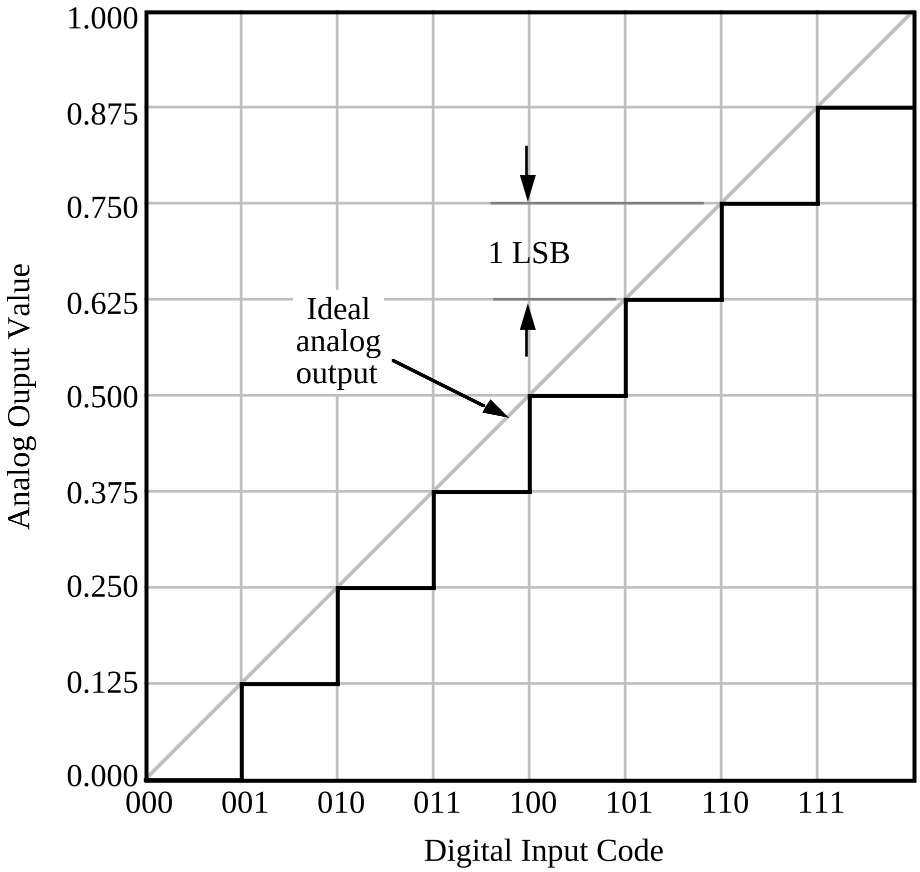
Classification of D/A Converters

Done by how the converter is scaled-



Static Characterization of D/A Converters

Ideal input-output D/A converter Static Characteristic -

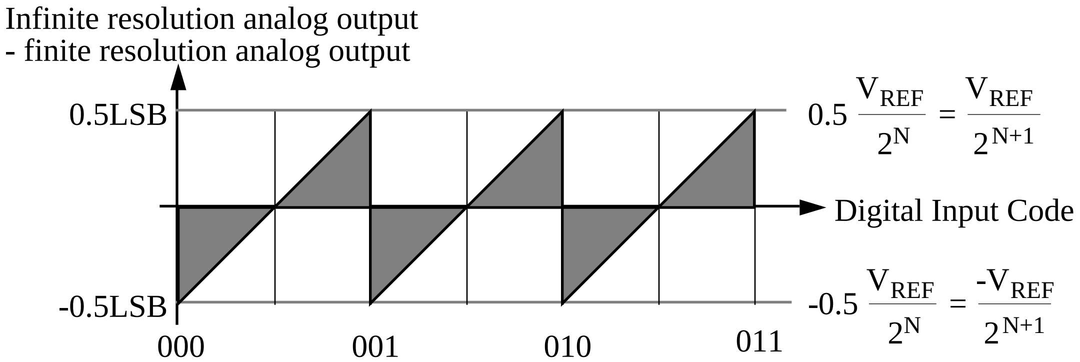


An ideal LSB change causes an analog change of $\frac{V_{ref}}{2^N}$

Definitions

Resolution is the smallest analog change resulting from a 1 LSB digital change (quantified in terms of N bits).

Quantization Noise is the inherent uncertainty in digitizing an anlog value with a finite resolution converter.



Dynamic range (DR) is the ratio of FS to the smallest resolvable difference.

$$DR = \frac{FS}{\text{LSB change}} = \frac{V_{REF}\,\frac{2^N - 1}{2^N}}{V_{REF}\,\frac{1}{2^N}} = 2^N - 1$$

$$DR(dB) = 20\log_{10}(2^N - 1) \cong 6N\ dB$$

Signal to noise ratio (SNR) for a sawtooth waveform
Approximating FS = LSB(2^N -1) ≅ LSB(2^N),

$$SNR = \frac{\text{Full scale RMS value}}{\text{RMS value of quantization noise}} = \frac{\frac{2^N}{2\sqrt{2}}}{\frac{1}{\sqrt{12}}} = \frac{\sqrt{12}}{2\sqrt{2}}\,2^N$$

$$SNR\ (dB) = 20\log_{10}\left[\left(\frac{\sqrt{6}}{2}\right)2^N\right] = 20\log_{10}\left(\frac{\sqrt{6}}{2}\right) + 20\log_{10}(2^N)$$

$$= 20\log_{10}(1.225) + 6.02N = 1.76\ dB + 6.02N\ dB$$

Definitions - Continued

Full scale (FS) is the the maximum DAC analog output value. It is one LSB less than V_{REF} .

$$FS = V_{REF}\frac{2^N - 1}{2^N}$$

A *monotonic* D/A (A/D) converter is one in which an increasing digital input code (analog input) produces a continuously increasing analog output value (digital output code).

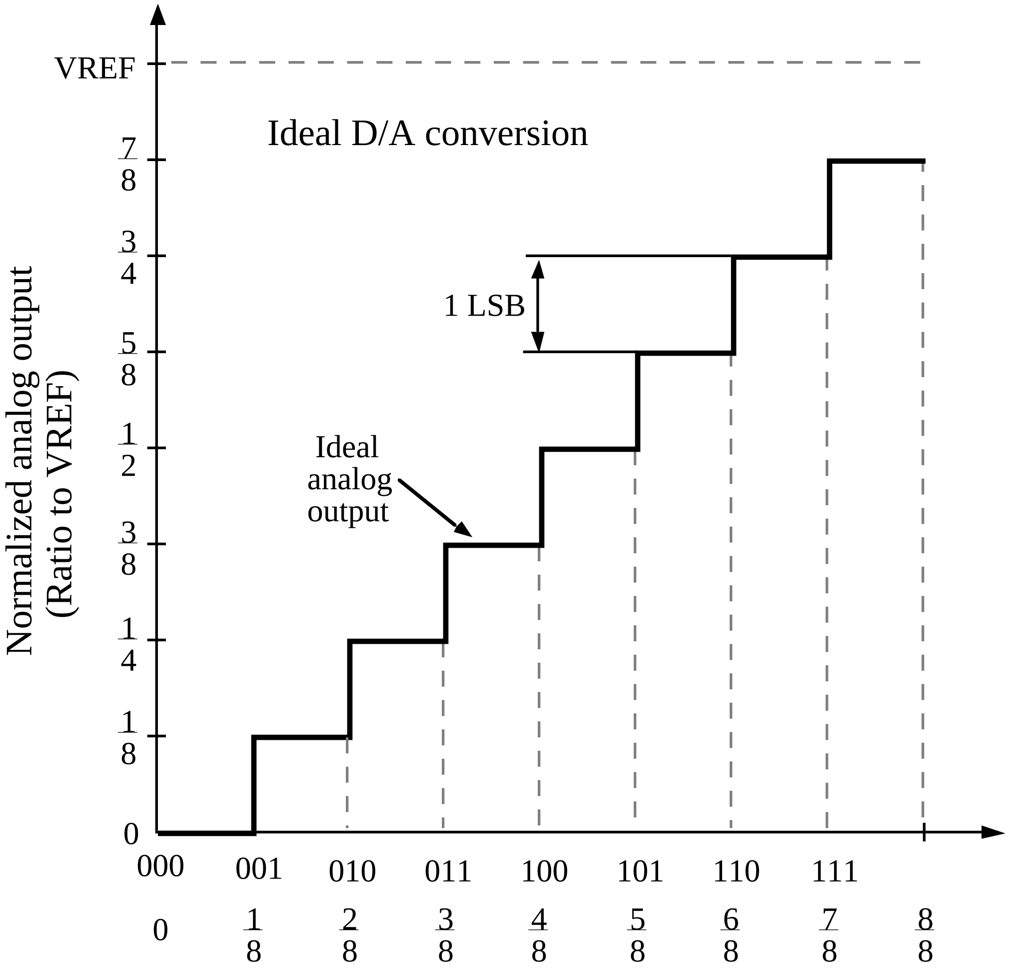
Offset error is a constant shift of the actual finite resolution characteristic from the ideal infinite resolution characteristic.

Gain error is a deviation between the actual finite resolution characteristic and the ideal infinite resolution characteristic which changes with the input.

Integral nonlinearity (INL) is the maximum difference between the actual finite resolution characteristic and the infinite resolution characteristic.

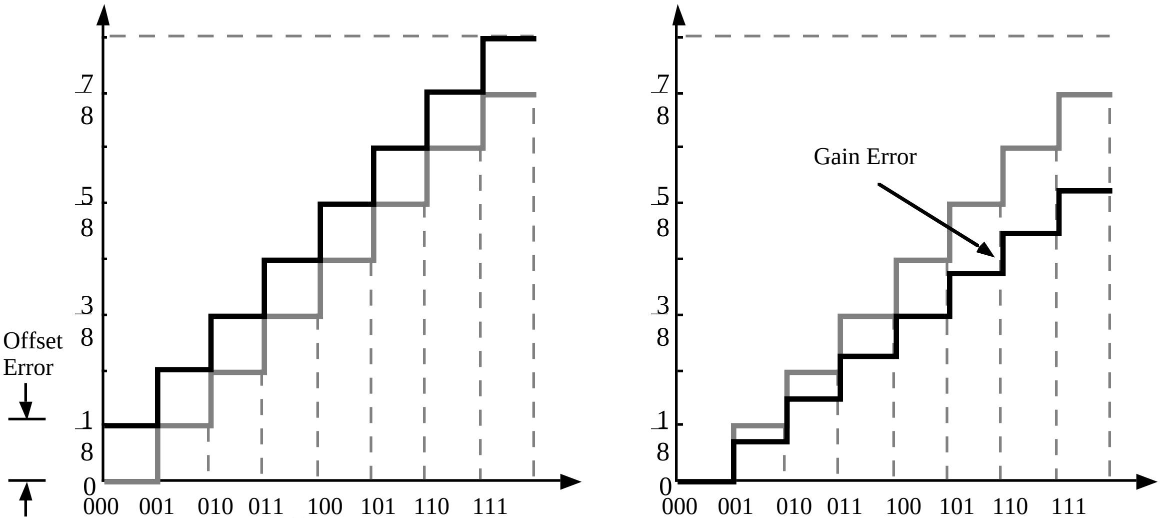
Differential nonlinearity (DNL) is the maximum deviation of any analog output changes caused by an input LSB change from its ideal change of $\frac{FS}{2^N}$.

3-BIT D/A CONVERTER ILLUSTRATION

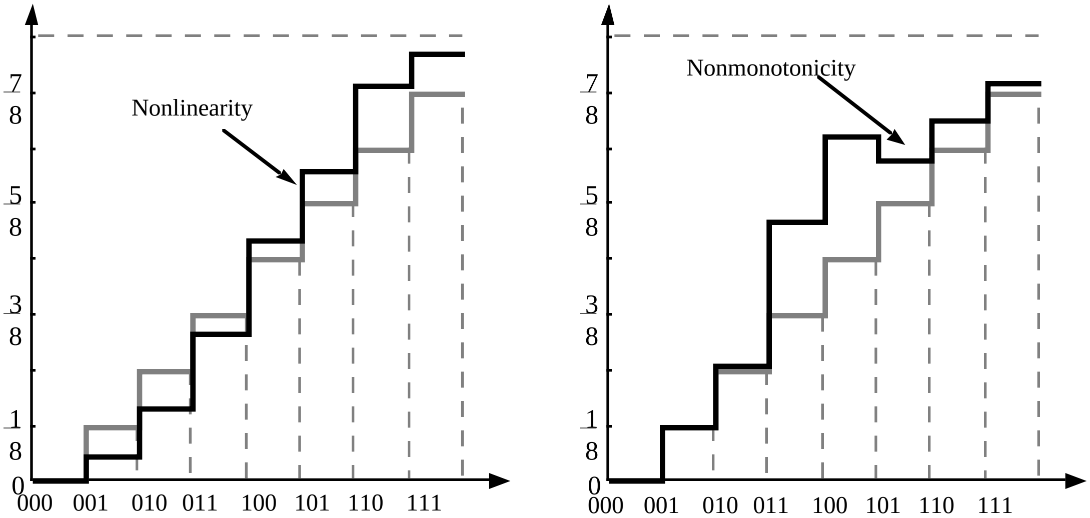


Digital input, code and fractional value

Ideal relationship



Offset Error Gain Error

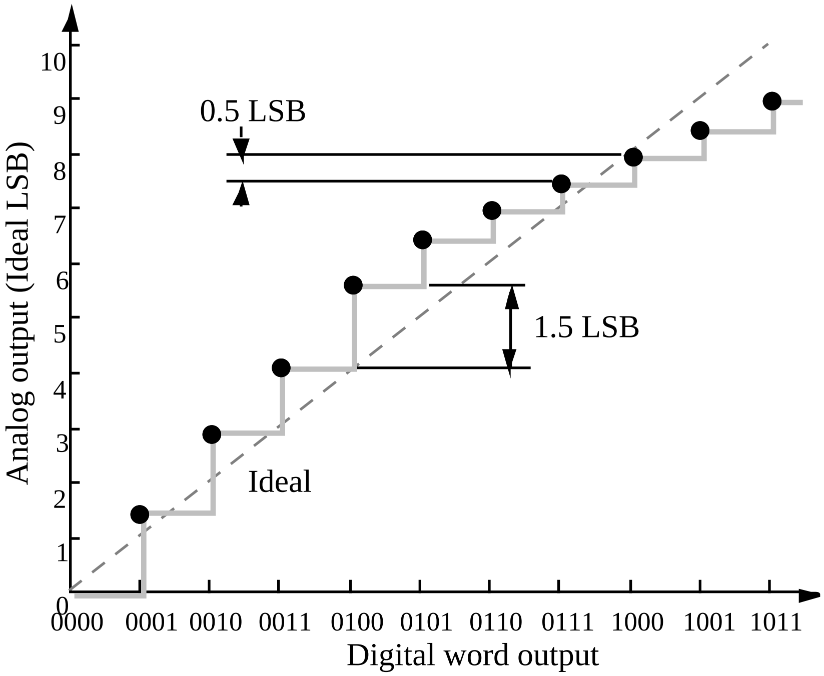


Linearity Error Nonmonotonicity (Due to Excessive Differential Nonlinearity)

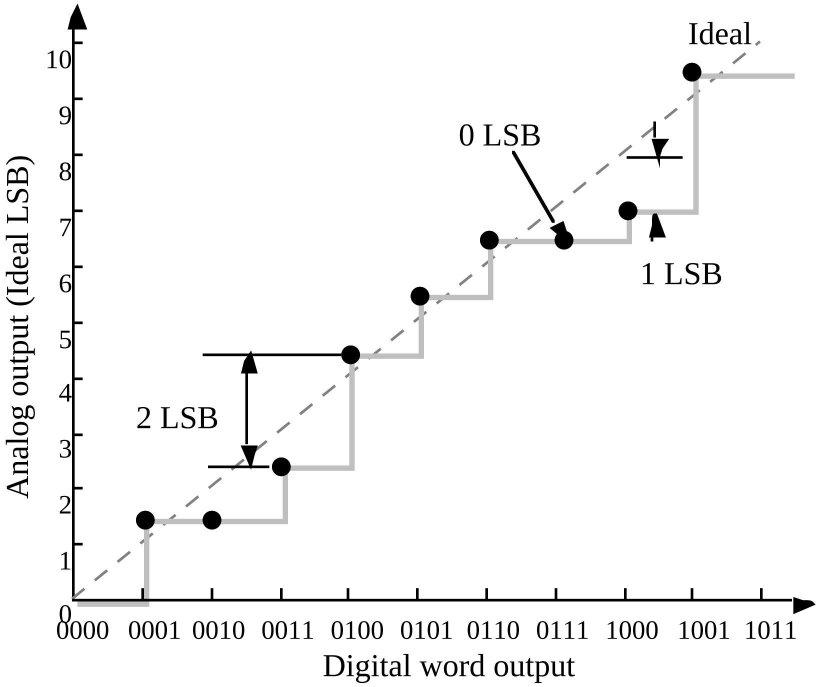
Typical sources of errors

Integral and Differential Linearity for a D/A Converter

D/A Converter with ±1.5 LSB integral nonlinearity and ±0.5 LSB differential nonlinearity



D/A converter with ±1 LSB integral nonlinearity and ±1 LSB differential nonlinearity



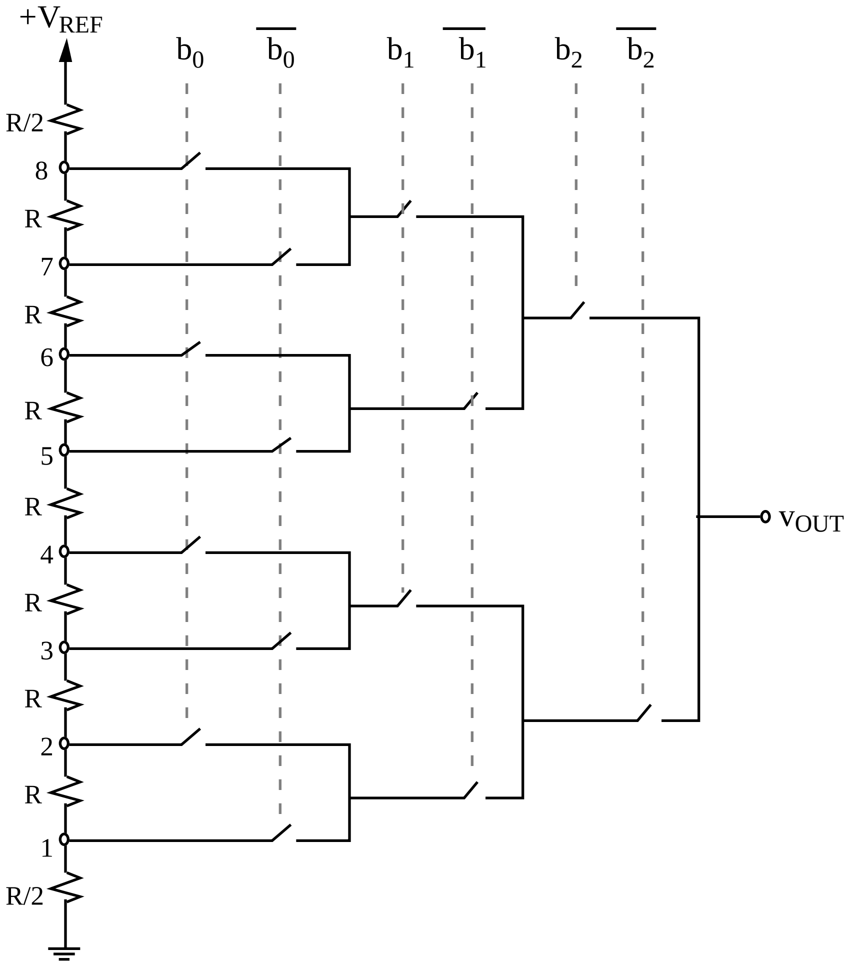
X.2 VOLTAGE SCALING CONVERTERS

3-BIT VOLTAGE SCALING D/A CONVERTER

Assume that $b_0 = 1$, $b_1 = 0$, and $b_2 = 1$

MSB: b_2

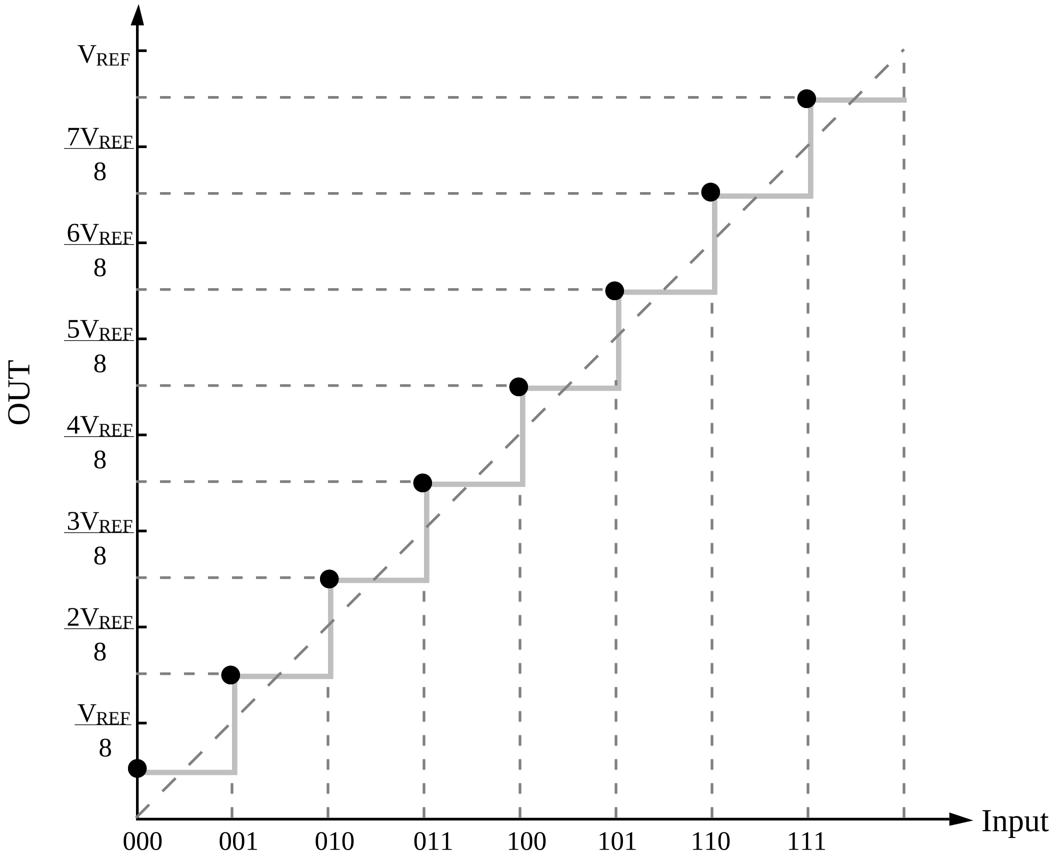
LSB: b_0



$$v_{OUT} = \frac{V_{REF}}{8}(D+0.5) = \frac{V_{REF}}{16}(2D+1) = 0.6875V_{REF} = \frac{11}{16}V_{REF}$$

3-BIT VOLTAGE SCALING D/A CONVERTER - CONT'D

Input-Output Characteristics:



Advantages:

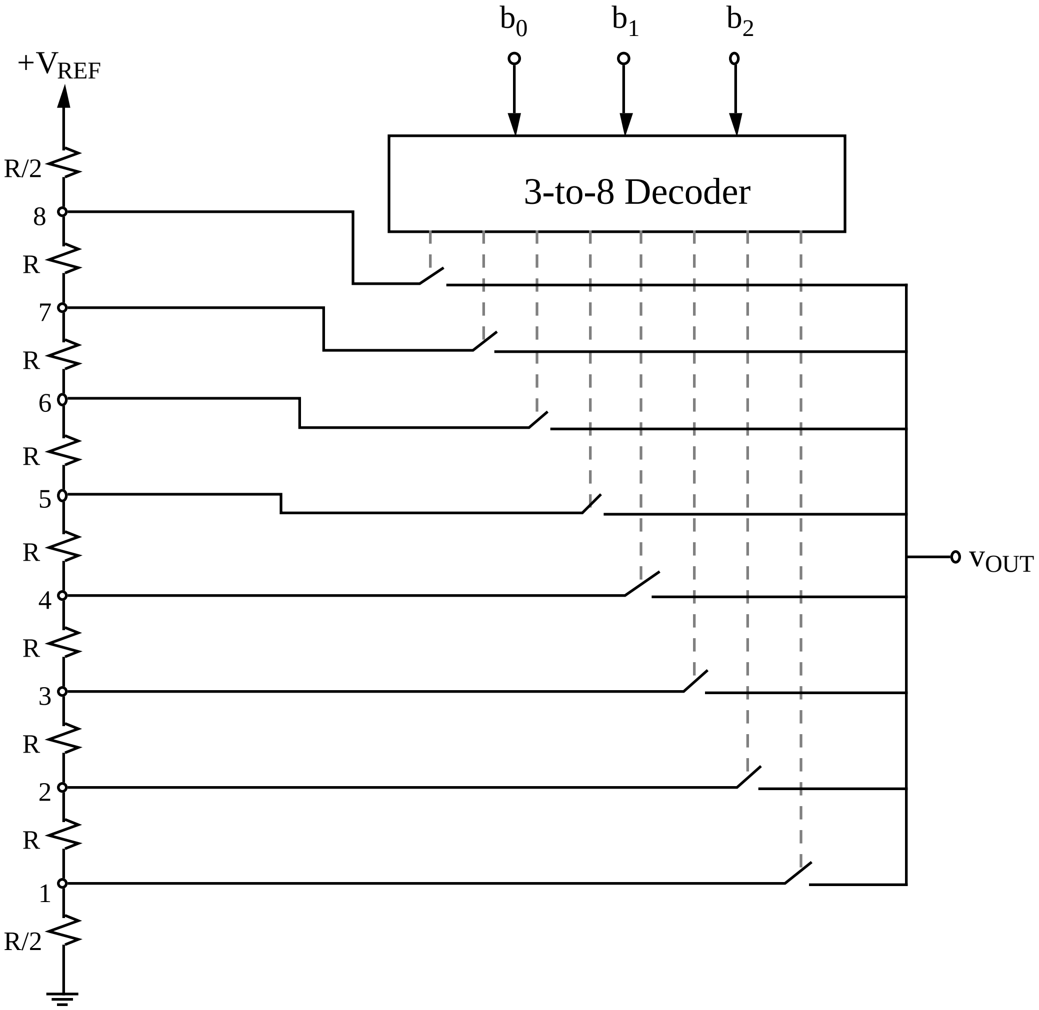
- Inherent monotonicity
- Compatible with CMOS technology
- Small area if n < 8 bits

Disadvantages:

- Large area if n > 8 bits
- Requires a high input impedance buffer at output
- Integral linearity depends on the resistor ratios

3-BIT VOLTAGE SCALING D/A CONVERTER WHICH MINIMIZES THE SWITCHES

Require time for the logic to perform



Accuracy Requirements of a Voltage Scaling D/A

Find the accuracy requirements for the voltage scaling D/A converter as a function of the number of bits N if the resistor string is a 5 micron wide polysilicon strip. If the relative accuracy is 2%, what is the largest number of bits that can be resolved to within ±0.5 LSB?

Assume that the ideal voltage to ground across k resistors is

$$V_k = \frac{kR}{2^N R} V_{REF}$$

The worst case variation in V_k is found by assuming all resistors above this point in the string are maximum and below this are minimum. Therefore,

$$V_k' = \frac{kR_{min}V_{REF}}{(2^N\text{-}k)R_{max} + kR_{min}}$$

The difference between the ideal and worst case voltages is,

$$\left|\frac{V_k}{V_{REF}} - \frac{V_k'}{V_{REF}}\right| = \left|\frac{kR}{2^N R} - \frac{kR_{min}}{(2^N\text{-}k)R_{max} + kR_{min}}\right|$$

Assuming that this difference should be less than 0.5 LSB gives,

$$\left|\frac{kR}{2^N R} - \frac{kR_{min}}{(2^N\text{-}k)R_{max} + kR_{min}}\right| < \frac{0.5}{2^N}$$

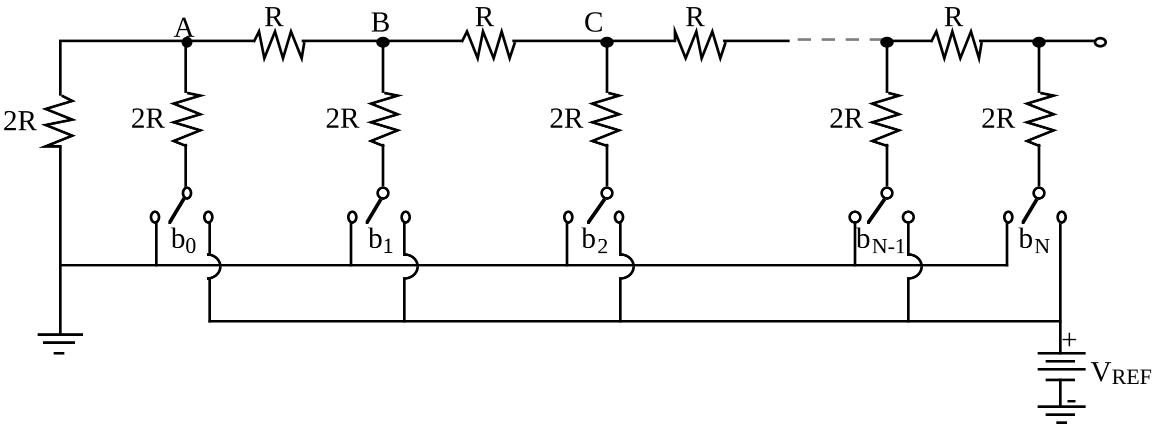
Expressing R_{max} as R+0.5ΔR and R_{min} as R-0.5ΔR and assuming the worst case occurs midway in the resistor string where $k=0.5(2^N)$ and assuming that 5 micron polysilicon has a 2% relative accuracy gives,

$$\left|0.5 - \frac{0.5(R- 0.5\Delta R)}{0.5(R + 0.5\Delta R) + 0.5(R- 0.5\Delta R)}\right| = \left|\frac{1}{4}\frac{\Delta R}{R}\right| < \frac{1}{2}\ 2^{-N}$$

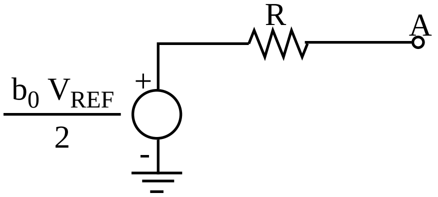
$$\Rightarrow \quad \left|\frac{\Delta R}{R} < \frac{1}{2^{N-1}}\right| \qquad \text{or} \qquad |0.25(0.02)| < 0.5(2^{-N}) \quad \Rightarrow \quad N = 6$$

R-2R LADDER DAC's

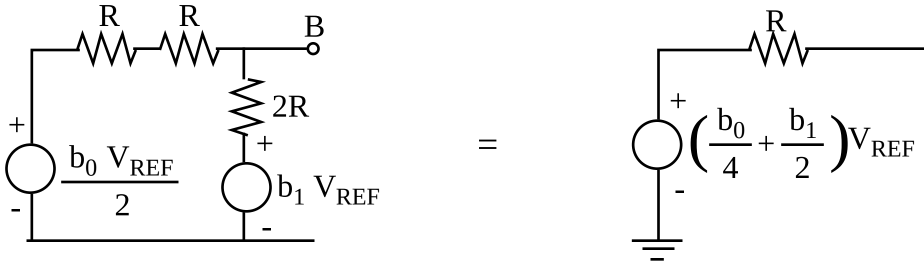
Configuration:



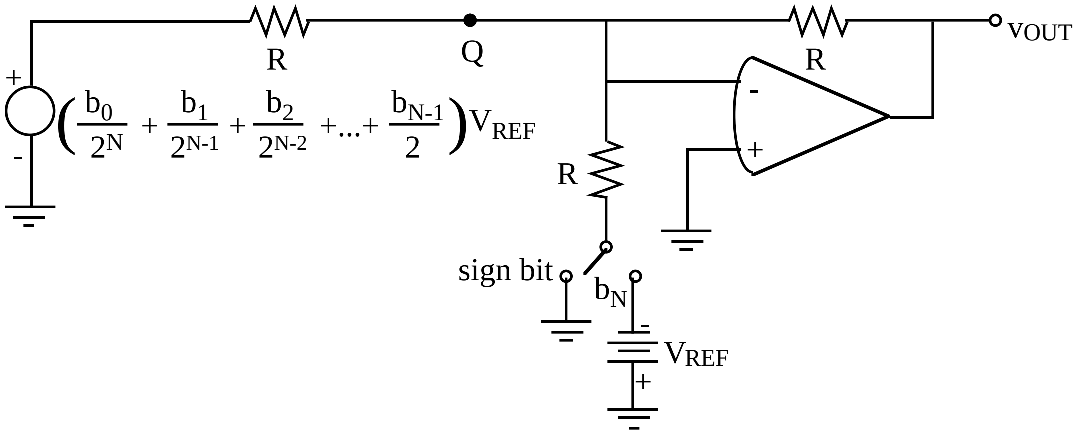
Equivalent circuit at A:



Equivalent circuit at B:

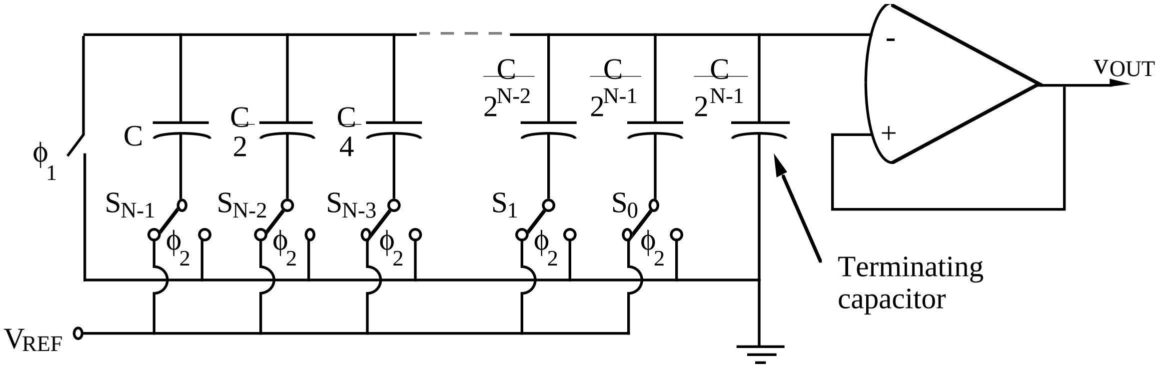


Finally, the equivalent circuit at Q:



X.3 CHARGE SCALING D/A CONVERTER

Binary weighted capacitor array:



Operation:

1.) During ϕ_1, all capacitors are discharged.

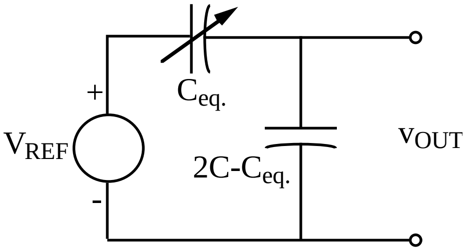
2.) During ϕ_2, capacitors with $b_i = 1$ are connected to V_{REF} and capacitors with $b_i = 0$ are grounded.

3.) The resulting output voltage is,

$$v_{OUT} = V_{REF}\left(\frac{b_{N-1}C}{2C} + \frac{b_{N-2}C/2}{2C} + \frac{b_{N-3}C/4}{2C} + \dots + \frac{b_0 C/(2^{N-1})}{2C}\right)$$

If $C_{eq.}$ is defined as the sum of all capacitances connected to V_{REF}, then

$$v_{OUT} = \left(\frac{C_{eq.}}{2C}\right) V_{REF}$$



Other Versions of the Charge Scaling D/A Converter

Bipolar Operation:

Charge all capacitors to V_{REF}. If $b_i = 1$, connect the capacitor to ground, if $b_i = 0$, connect the capacitor to V_{REF}.

Will require an extra bit to decide whether to connect the capacitors initially to ground or to V_{REF}.

Four-Quadrant Operation:

If V_{REF} can have ±values, then a full, four quadrant DAC can be obtained.

Multiplying DAC:

If V_{REF} is an analog signal (sampled and held), then the output is the product of a digital word and an analog signal and is called a multiplying DAC (MDAC).

Influence of Capacitor Ratio Accurcy on No. of Bits

Use the data of Fig.2.4-2 to estimate the number of bits possible for a charge scaling D/A converter assuming a worst case approach and the worst conditions occur at the midscale (1 = MSB).

The ideal output of the charge scaling DA converter is,

$$\frac{v_{OUT}}{V_{REF}} = \frac{C_{eq.}}{2C}$$

The worst case output of the charge scaling DA converter is,

$$\frac{v'_{OUT}}{V_{REF}} = \frac{C_{eq.(min)}}{\left(2C - C_{eq.}\right)_{(max)} + C_{eq.(min)}}$$

The difference between the ideal output and the worst case output is,

$$\left|\frac{v_{OUT}}{V_{REF}} - \frac{v'_{OUT}}{V_{REF}}\right| = \left|\frac{1}{2} - \frac{C_{eq.(min)}}{(2C - C_{eq.})(max) \pm C_{eq.(min)}}\right|$$

Assuming the worst case condition occurs at midscale, then $C_{eq.} = C$

$$\therefore \left|\frac{v_{OUT}}{V_{REF}} - \frac{v'_{OUT}}{V_{REF}}\right| = \left|\frac{1}{2} - \frac{C_{(min)}}{C_{(max)} - C_{(min)}}\right|$$

If $C_{(max)} = C + 0.5\Delta C$ and $C_{(min)} = C - 0.5\Delta C$, then setting the difference between the ideal and worst case to 0.5LSB gives,

$$\frac{0.5(C_{(max)} \pm C_{(min)}) - C_{(min)}}{C_{(max)} + C_{(min)}} \le 0.5(1/2^N)$$

or

$$C_{(max)} - C_{(min)} \le \frac{1}{2^N}(C_{(max)} + C_{(min)})$$

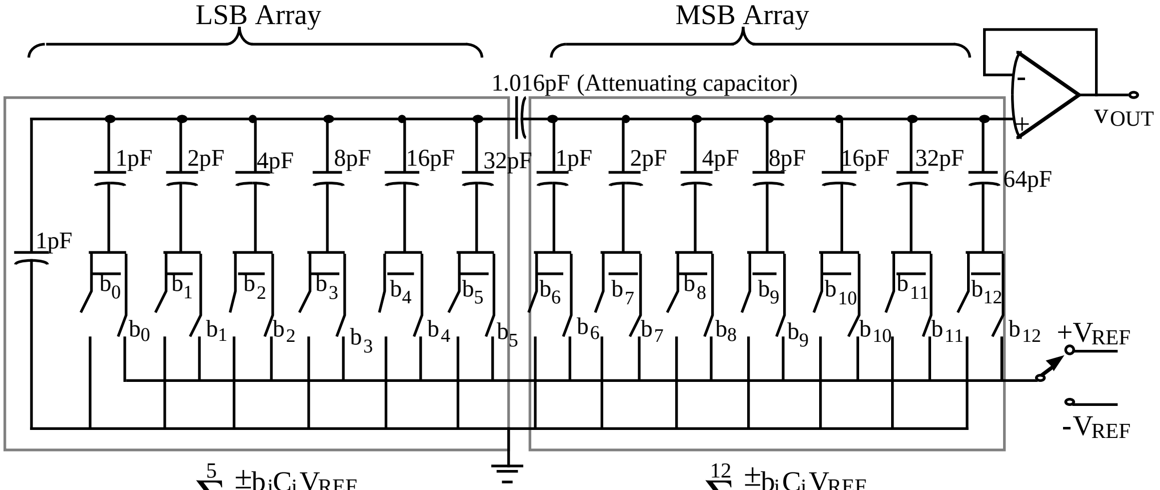
or

$$\Delta C \le \frac{1}{2^N}\, 2C \quad \Rightarrow \quad \left|\frac{\Delta C}{2C}\right| \le 2^{-N} \quad \Rightarrow \quad \left|\frac{\Delta C}{C}\right| \le \frac{1}{2^{N-1}}$$

A 50µm x 50µm unit capacitor gives a relative accuracy of 0.1% and N = 11 bits. It is more appropriate that the relative accuracy is a function of N. For example, if $\Delta C/C \approx 0.001 + 0.0001N$, then N=9 bits.

Increasing the Number of Bits for a Charge Scaling D/A Converter

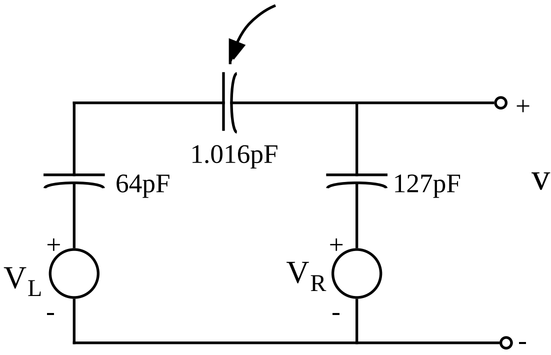
Use a capacitive divider. For example, a 13-bit DAC-



$$V_L = \sum_{i=0}^{5} \frac{\pm b_i C_i V_{REF}}{64} \qquad V_R = \sum_{i=6}^{12} \frac{\pm b_i C_i V_{REF}}{127}$$

An equivalent circuit-

$$\frac{1}{64} + \frac{1}{C} = 1 \;\Rightarrow\; C = \frac{64}{63} \approx 1.016$$



$$v_{OUT} = \frac{\frac{1}{64} + \frac{63}{64}}{\frac{1}{64} + \frac{63}{64} + \frac{1}{127}} V_R + \frac{\frac{1}{127}}{\frac{1}{64} + \frac{63}{64} + \frac{1}{127}} V_L$$

$$= \frac{127}{128} V_R + \frac{1}{128} V_L$$

$$V_R = \sum_{i=6}^{12} \frac{\pm b_i V_{REF} C_i}{127} \quad \text{and } V_L = \sum_{i=0}^{5} \frac{\pm b_i V_{REF} C_i}{64}$$

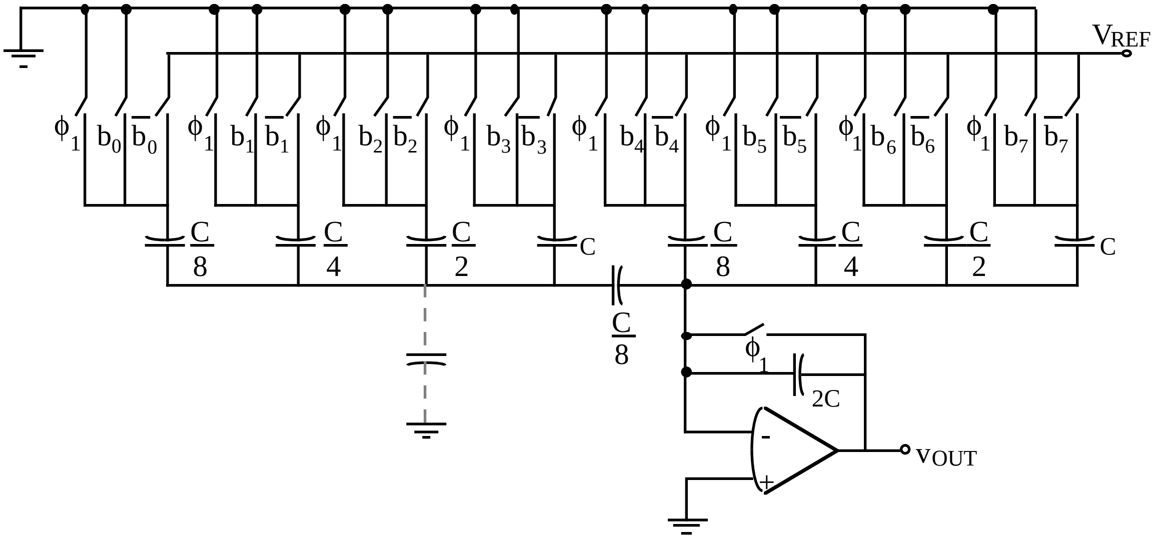
or

$$v_{OUT} = \frac{\pm V_{REF}}{128} \left[\sum_{i=6}^{12} b_i C_i + \sum_{i=0}^{5} \frac{b_i C_i}{64} \right]$$

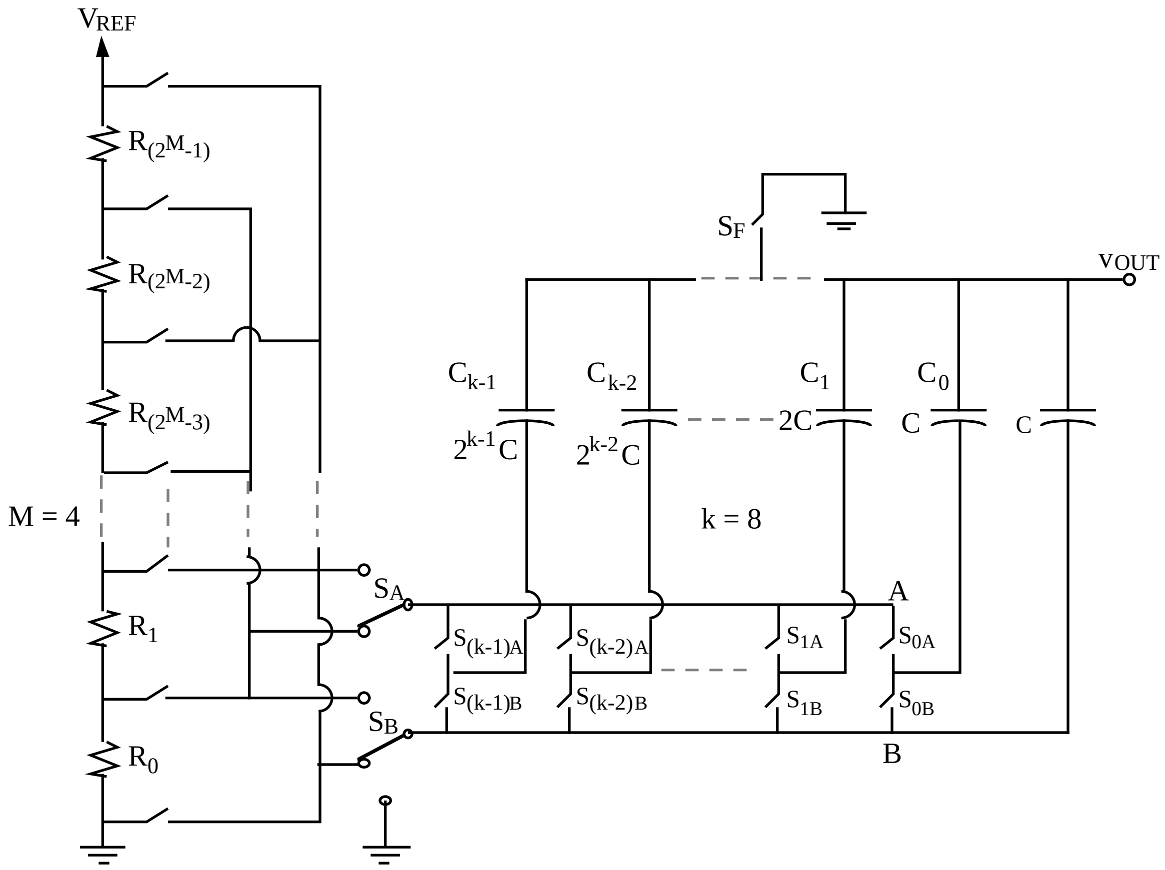
Removal of the Amplifier Input Capacitance Effects

Use the binary weighted capacitors as the input to a charge amplifier.

Example of A Two-Stage Configuration:



X.4 - VOLTAGE SCALING-CHARGE SCALING DAC'S



Advantages:

- Resistor string is inherently monotonic so the first M bits are monotonic.
- Can remove voltage threshold offsets.
- Switching both busses A and B removes switch imperfections.
- Can make tradeoffs in performance between the resistors and capacitors.
- Example with 4 MSB's voltage scaling and 8 LSB's charge scaling:

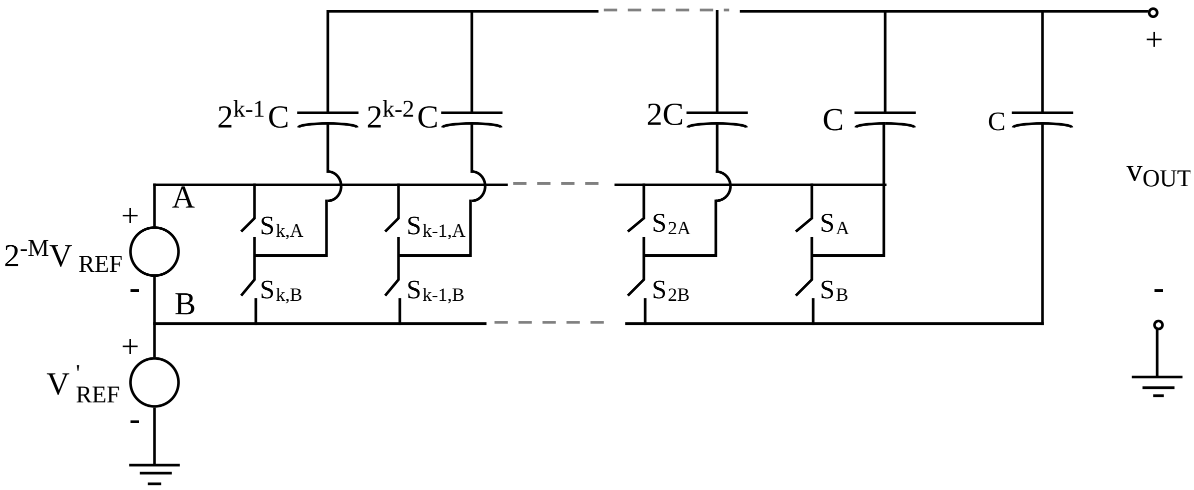
Voltage Scaling, Charge Scaling DAC - Cont'd

Operation:

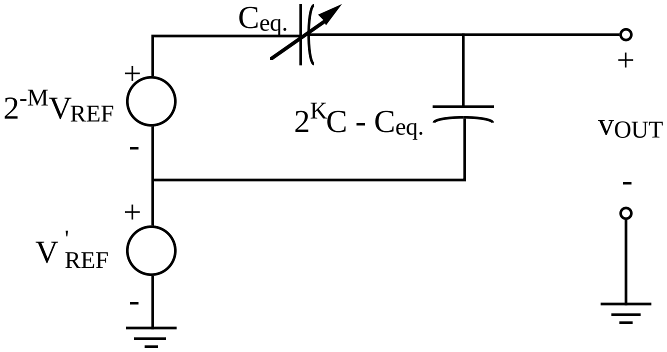
1.) S_F, S_B, and S_{1B} through $S_{k,B}$ are closed discharging all capacitors. If the output of the DAC is applied to any circuit having a nonzero threshold, switch S_B could be connected to this circuit to cancel this threshold effect.

2.) Switch S_F is opened and buses A and B are connected across the resistor whose lower and upper voltage is V'_{REF} and $V'_{REF} + 2^{-M}V_{REF}$ respectively, where

$$V'_{REF} = V_{ref}\left(\frac{b_0}{2^M} + \frac{b_1}{2^{M-1}} + \frac{b_2}{2^{M-2}} + \cdots + \frac{b_{M-1}}{2^1}\right)$$



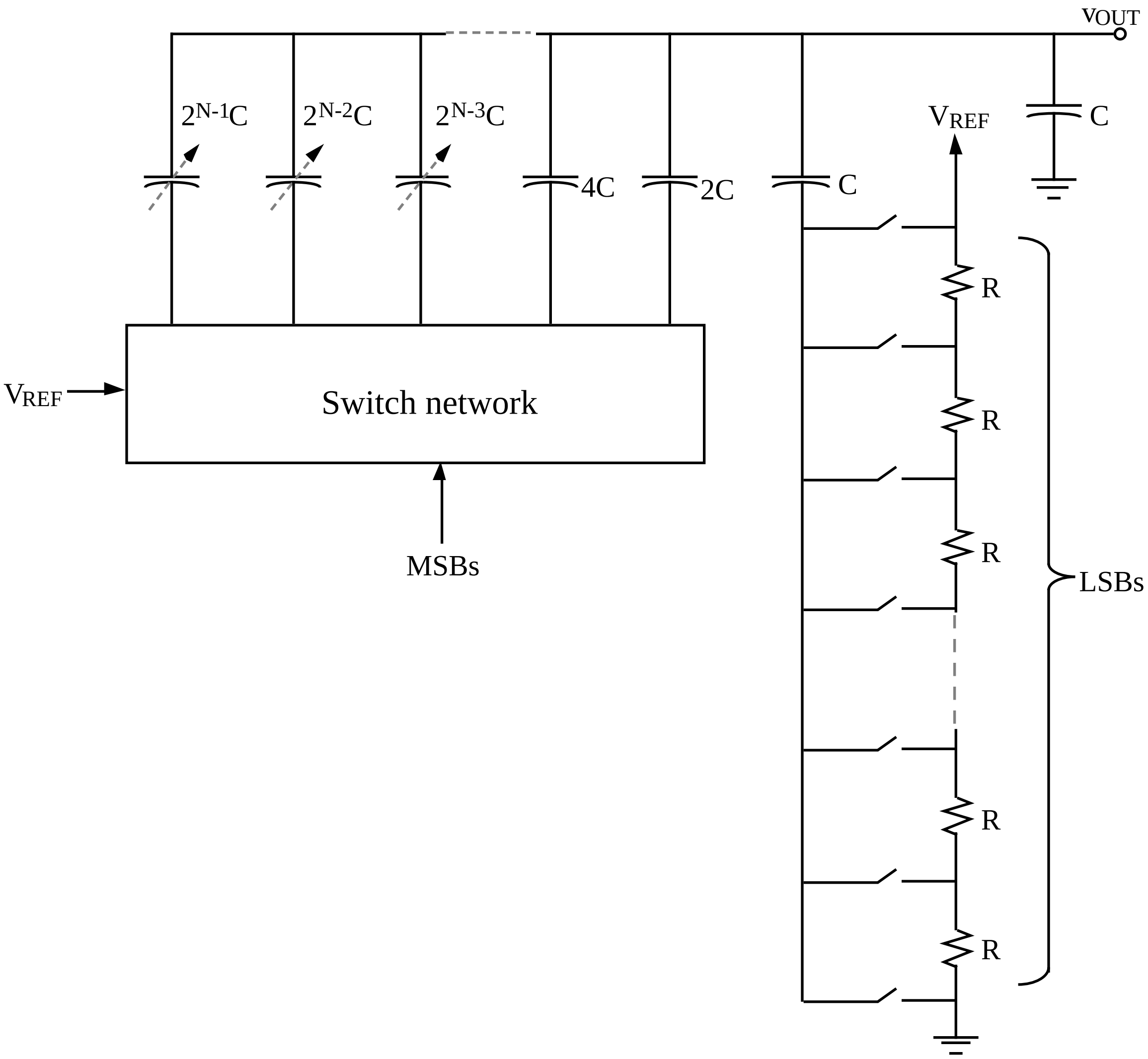
3.) Final step is to determine whether to connect the bottom plates of the capacitors to bus A (b_i=1) or bus B (b_i=0).



$$v_{OUT} = \sum_{i=0}^{M+K-1} b_i 2^{-(M+K-i)} V_{REF}$$

Charge Scaling, Voltage Scaling DAC

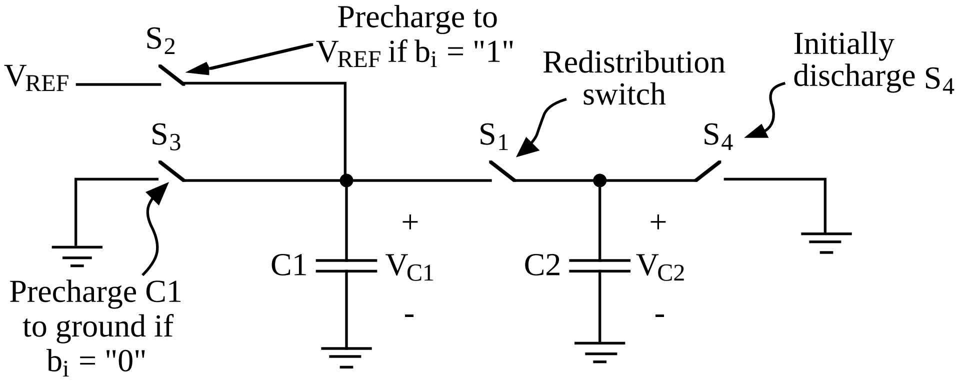
Use capacitors for MSB's and resistors for LSB's



- Resistors must be trimmed for absolute accuracy.
- LSB's are monotonic.

X.5- OTHER TYPES OF D/A CONVERTERS

CHARGE REDISTRIBUTION SERIAL DAC

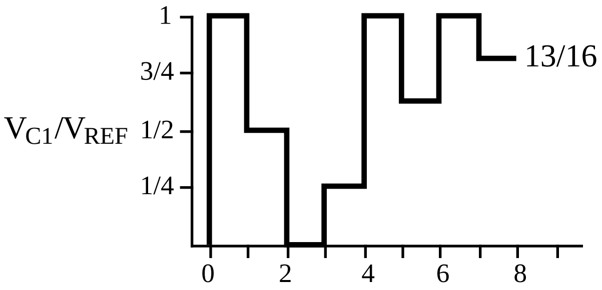


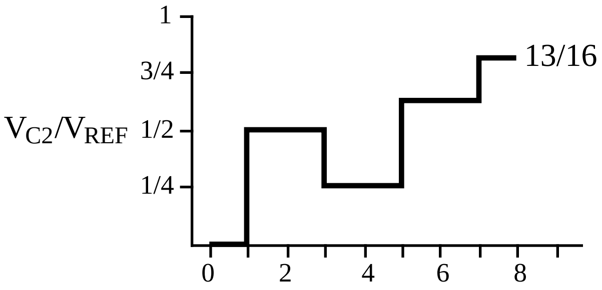
$C1 = C2$
b_0 = LSB
b_1 = NLSB
.
.
.
b_N = MSB

Conversion sequence:

4 Bit D/A Converter

INPUT WORD: 1101





Close S_4: $V_{C2} = 0$

Start with LSB first-

Close S_2 (b_0=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = \frac{V_{REF}}{2} = V_{C2}$

Close S_3 (b_1=0): $V_{C1} = 0$

Close S_1: $V_{C1} = V_{C2} = \frac{V_{REF}}{4}$

Close S_2 (b_2=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = V_{C2} = \frac{5}{8}\ V_{REF}$

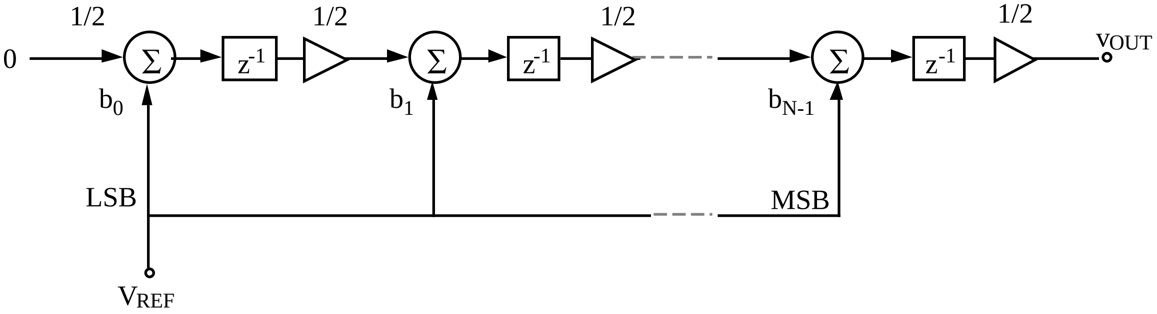
Close S_2 (b_3=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = V_{C2} = \frac{13}{16}\ V_{REF}$

Comments:
- LSB must go first.
- n cycles to make an n-bit D-A conversion.
- Top plate parasitics add error.
- Switch parasitics add error.

ALGORITHMIC SERIAL DAC

Pipeline Approach to Implementing a DAC:



$$v_{OUT}(z) = \left[\frac{b_{N-1}}{2} z^{-1} + \frac{b_{N-2}}{4} z^{-2} + \ldots. + \frac{b_0}{2^N} z^{-N}\right] V_{REF}$$

where $b_i = 1$ or 0

Approaches:

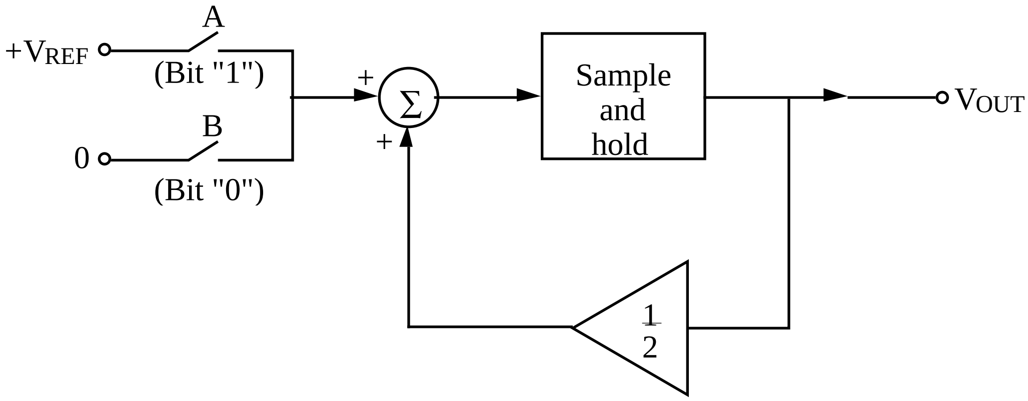
1.) Pipeline with N cascaded stages.

2.) Algorithmic.

$$v_{OUT}(z) = \frac{b_i \, z^{-1} V_{REF}}{1 - 0.5z^{-1}}$$

Example of an Algorithmic DAC Operation

Realization using iterative techniques:



Assume that the digital word is 11001 in the order of MSB to LSB. The steps in the conversion are:

1.) $V_{OUT}(0)$ is zeroed.

2.) LSB = 1, switch A closed,
$V_{OUT}(1) = V_{REF}$.

3.) Next LSB = 0, switch B closed,
$V_{OUT}(2) = 0 + 0.5V_{REF}$
$V_{OUT}(2) = 0.5V_{REF}$.

4.) Next LSB = 0, switch B closed,
$V_{OUT}(3) = 0 + 0.25V_{REF}$
$V_{OUT}(3) = 0.25V_{REF}$.

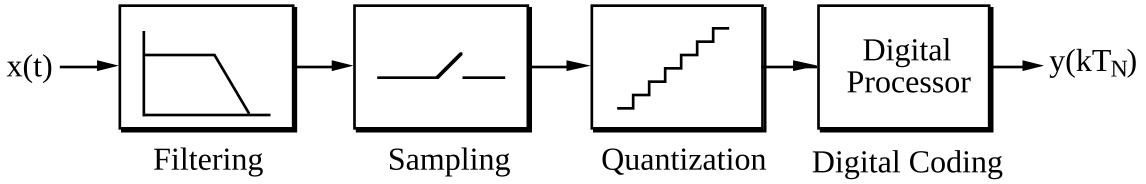
5.) Next LSB = 1, switch A closed,
$V_{OUT}(4) = V_{REF} + (1/8)V_{REF}$
$V_{OUT}(4) = (9/8)V_{REF}$.

6.) Finally, the MSB is 1,
switch A is closed, and
$V_{OUT}(5) = V_{REF} + (9/16)V_{REF}$
$V_{OUT}(5) = (25/16)V_{REF}$

7.) Finally, the MSB+1 is 0 (always last cycle),
switch A is closed, and
$V_{OUT}(6) = (25/32)V_{REF}$

X.6 - CHARACTERIZATION OF ANALOG TO DIGITAL CONVERTERS

General A/D Converter Block Diagram



A/D Converter Types

1.) Serial.

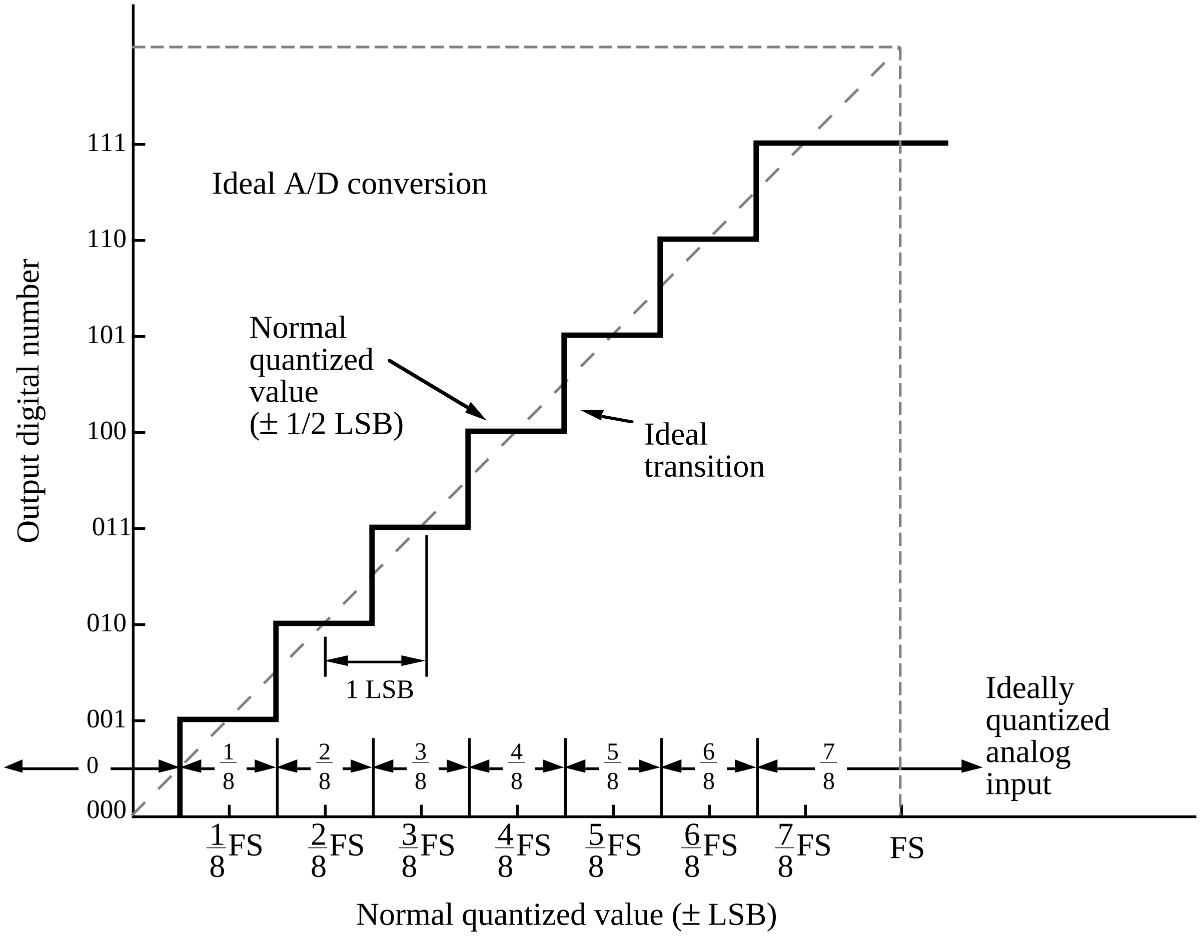
2.) Medium speed.

3.) High speed and high performance.

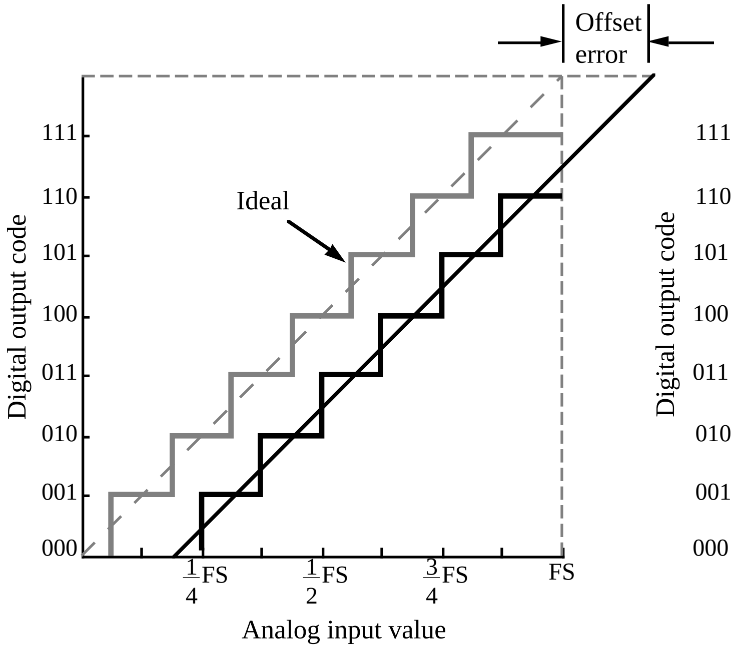
4.) New converters and techniques.

Characterization of A/D Converters

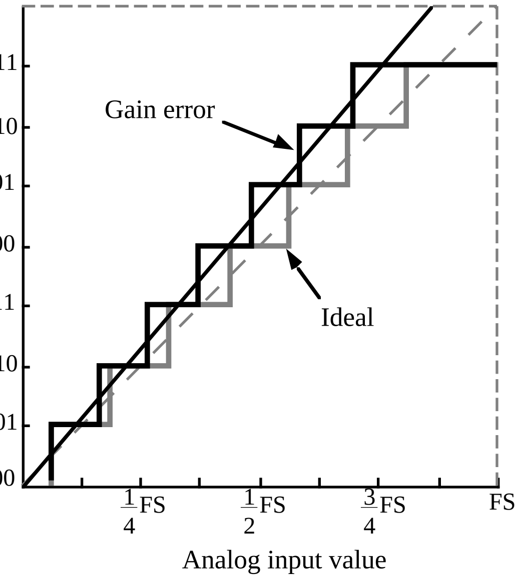
Ideal Input-Output Characteristics for a 3-bit ADC



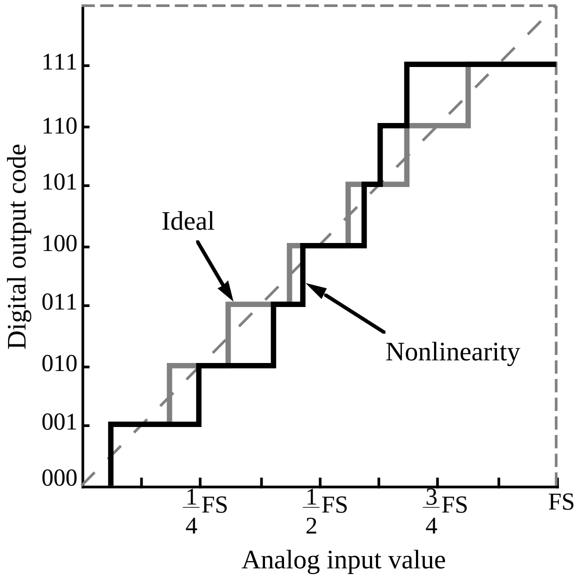
Nonideal Characteristics of A/D Converters



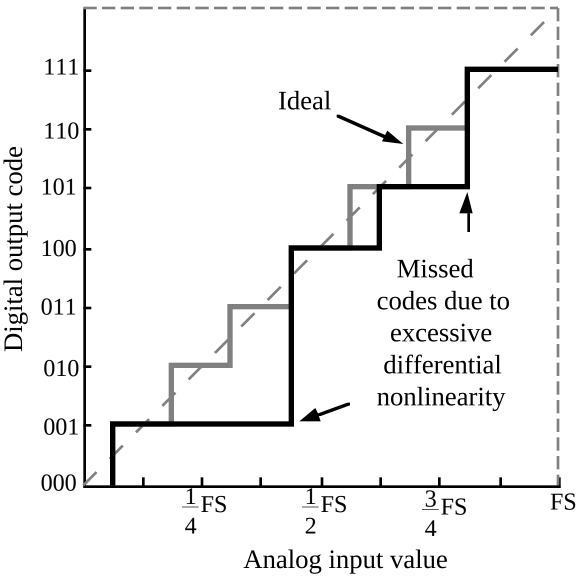
Offset Error



Scale factor (gain) error

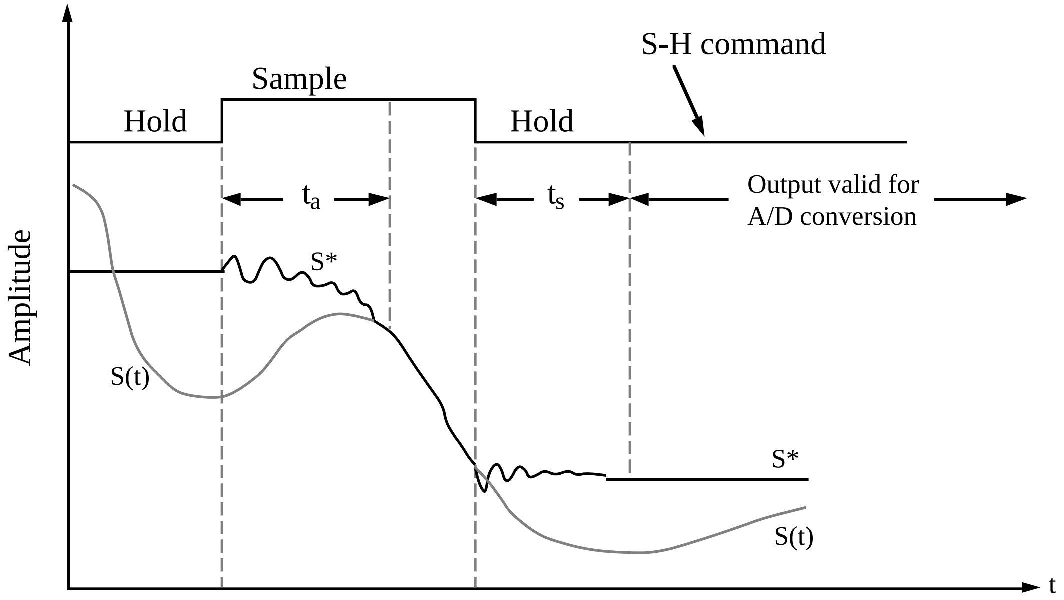


Integral Nonlinearity



Differential Nonlinearity

Sampled Data Aspect of ADC's



$T_{sample} = t_s + t_a$

t_a = acquisition time

t_s = settling time

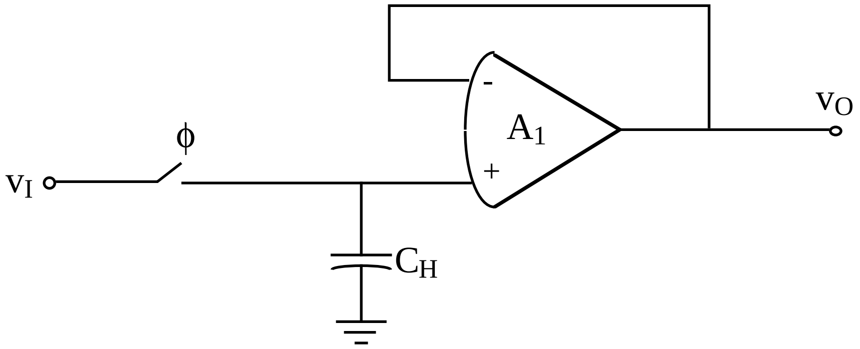
t_{ADC} = time for ADC to convert analog input to digital word.

Conversion time = $t_s + t_a + t_{ADC}$.

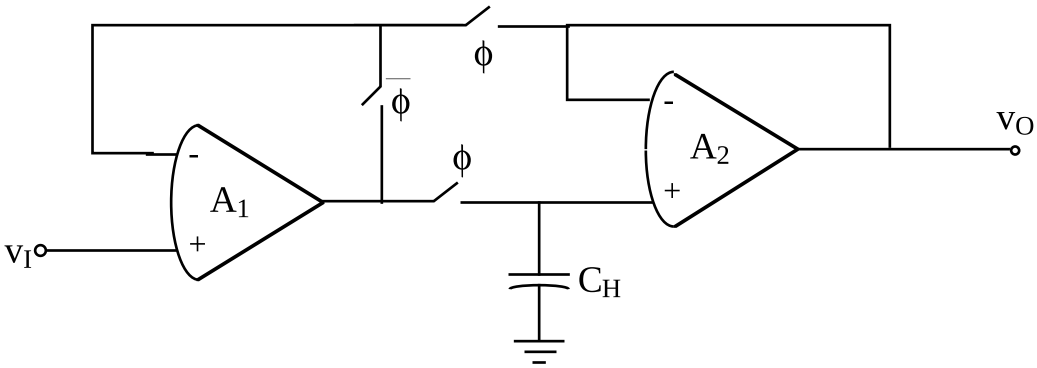
Noise = $\frac{kT}{C}$ V^2 (rms)

Sample and Hold Circuits

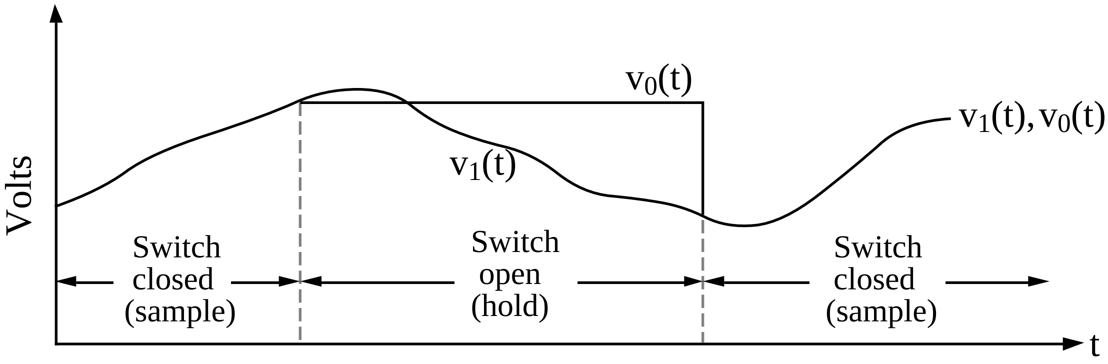
Simple



Improved

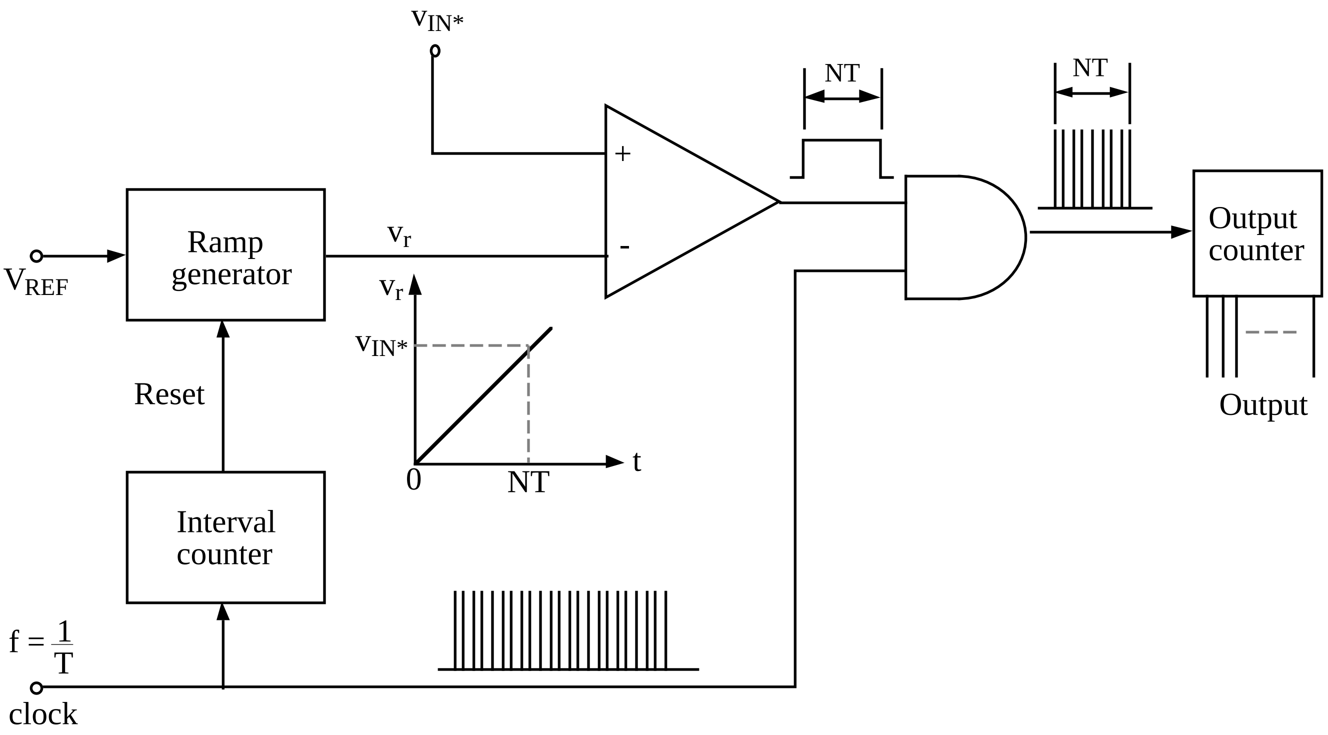


Waveforms



X.7 - SERIAL A/D CONVERTERS

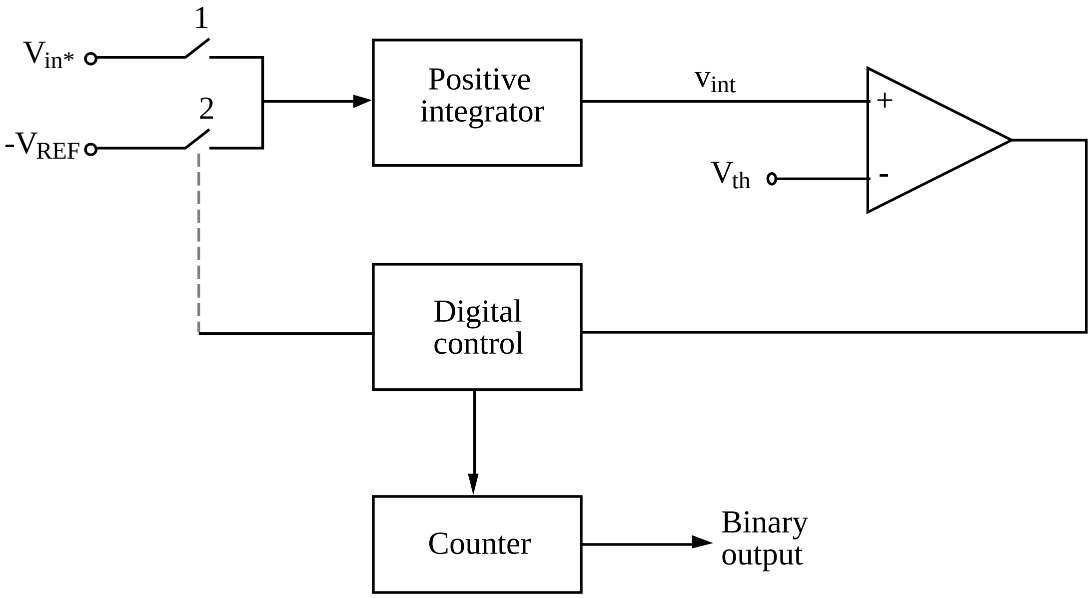
Single-Slope, A/D Converter



- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion times

Dual Slope, A/D Converter

Block Diagram:



Operation:

1.) Initially $v_{int} = 0$ and v_{in} is sampled and held ($V_{in}^* > 0$).

2.) Reset by integrating until $v_{int}(0) = V_{th}$.

3.) Integrate V_{in}^* for N_{ref} clock cycles to get,

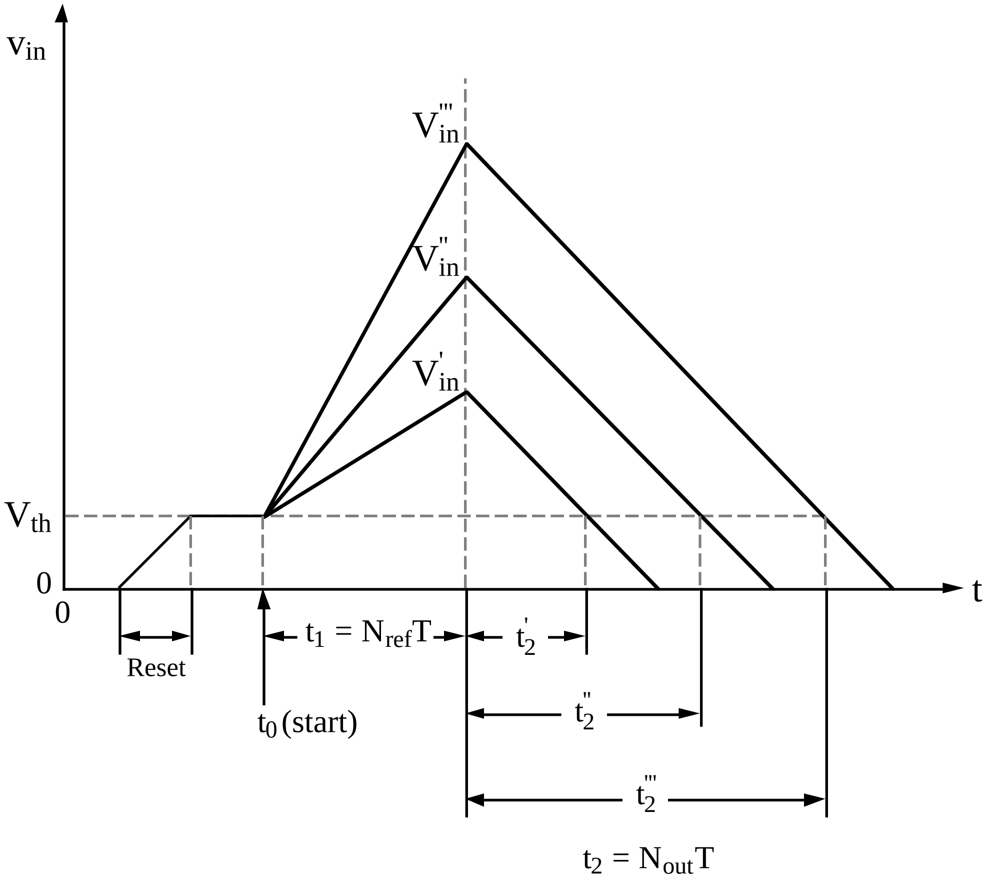
$$v_{int}(t_1) = v_{int}(N_{ref}T) = k\int_0^{N_{ref}T} V_{in}^* \, dt + v_{int}(0) = kN_{ref}TV_{in}^* + V_{th}$$

4.) The Carry Output on the counter is used to switch the integrator from V_{in}^* to $-V_{REF}$. Integrate until v_{int} is equal to V_{th} resulting in

$$v_{int}(t_1 + t_2) = v_{int}(t_1) + k\int_{t_1}^{N_{out}T + t_1} -V_{REF}dt = V_{th}$$

$$\therefore kN_{ref}TV_{in}^* + V_{th} - kV_{REF}N_{out}T = V_{th} \Rightarrow \boxed{V_{REF}\frac{N_{out}}{N_{ref}} = V_{in}^*}$$

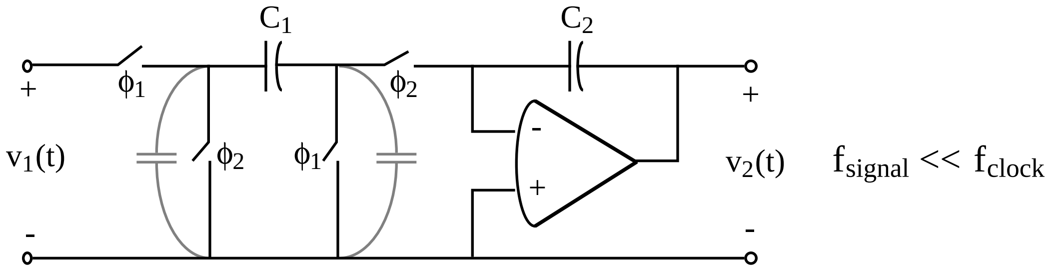
Waveform of the Dual -Slope A/D Converter



- Very accurate method of A/D conversion.
- Requires a long time -2(2^N) T

Switched Capacitor Integrators

Noninverting:



Operation:

Assume non-overlapping clocks ϕ_1 and ϕ_2. During ϕ_1, C_1 is charged to $v_1[(n-1)T]$ giving a charge of $q_1[(n-1)T]$ on C_1. During ϕ_2, the charge across C_1 is added to the charge already on C_2 which is $q_2[(n-1)T]$ resulting in a new charge across C_2 designated as $q_2(nT)$. The charge equation can be written as,

$$q_2(nT) = q_2[(n-1)T] + q_1[(n-1)T]$$

or

$$C_2v_2(nT) = C_2 v_2 [(n-1)T] + C_1 v_1 [(n-1)T]$$

Using z-domain notation gives

$$C_2v_2(z) = C_2z^{-1}v_2(z) + C_1z^{-1}v_1(z)$$

or

$$H(z) = \frac{v_2(z)}{v_1(z)} = \frac{C_1}{C_2}\left[\frac{z^{-1}}{1 - z^{-1}}\right]$$

Replacing z by $e^{j\omega T}$ gives,

$$H(e^{j\omega T}) = \frac{C_1}{C_2}\left[\frac{e^{-j\omega T}}{1 - e^{-j\omega T}}\right] = \frac{C_1}{C_2}\left[\frac{e^{-j\omega\frac{T}{2}}}{e^{j\omega\frac{T}{2}} - e^{-j\omega\frac{T}{2}}}\right]$$

$$= \frac{\omega_o}{j\omega}\underbrace{\left[\frac{(\omega T/2)}{\sin(\omega T/2)}\right]}_{\text{Mag. error}}\underbrace{\exp(-j\omega T/2)}_{\text{Phase error}} \approx \frac{\omega_o}{j\omega} \quad \text{if } f \ll f_c = \frac{1}{T}$$

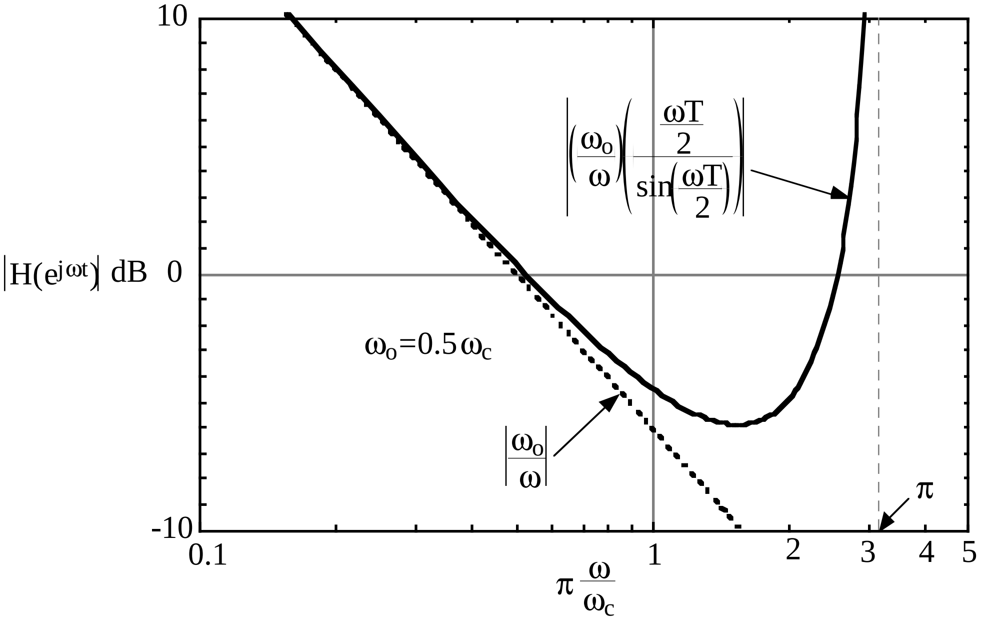
where $\omega_o = C_1/(TC_2)$, $\sin x = \dfrac{e^{jx} - e^{-jx}}{2j}$

Magnitude Plots of the Switched Capacitor Integrator

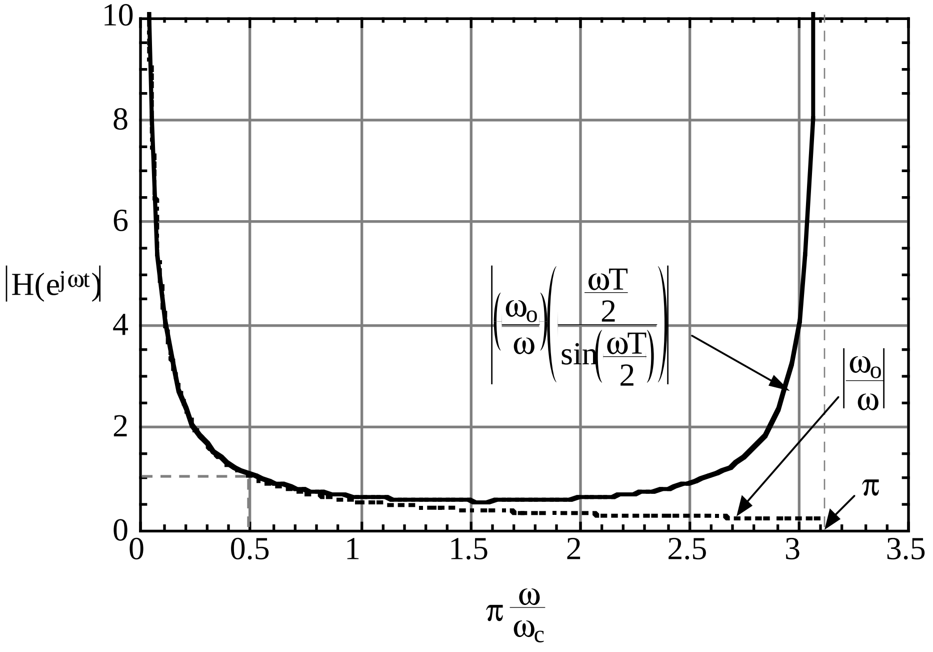
$$\omega_o = \frac{\omega_C}{2\pi}$$

$$\frac{\omega T}{2} = \frac{2\pi f}{2f_C} = \frac{\pi f}{f_C} = \frac{\pi\omega}{\omega_C}$$

Log Plot-

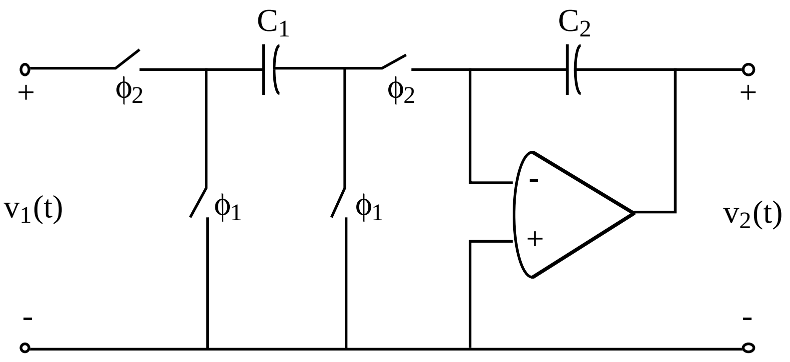


Linear Plot-



Switched Capacitor Integrators - Cont'd

Inverting:

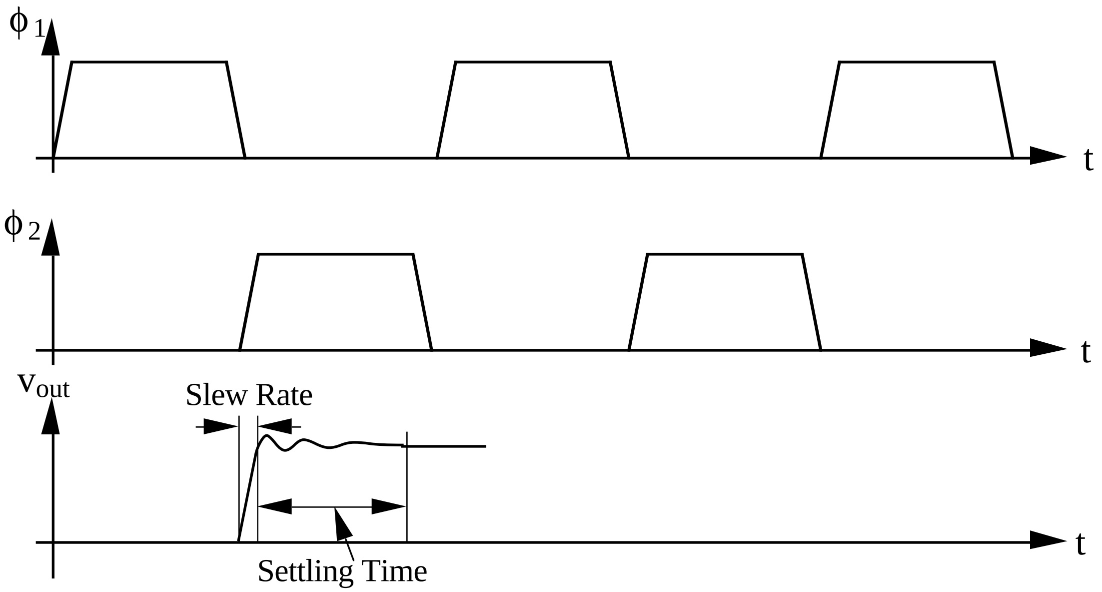


By a similar analysis, one can show that

$$H(e^{j\omega T}) \approx -\frac{\omega_o}{j\omega}\ , \text{ if } f << f_c = 1/T$$

Settling Time and Slew Rate of the Op Amp

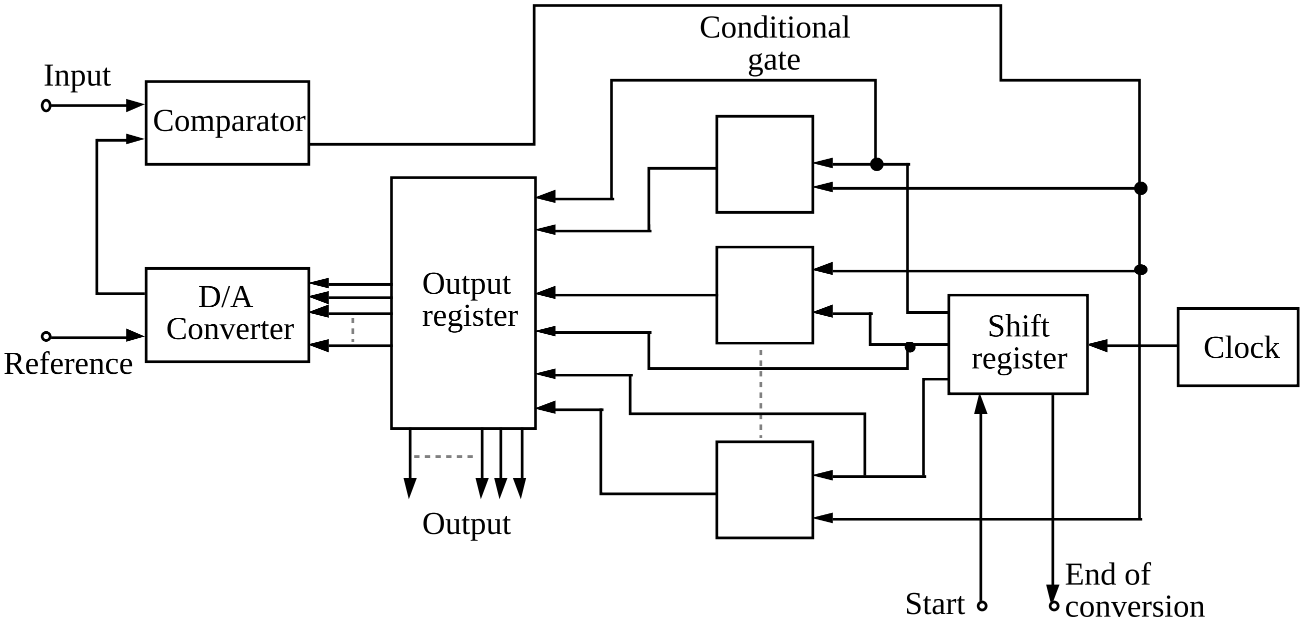
Important when the op amp plus feedback circuit has two or more poles or the op amp has a second pole.



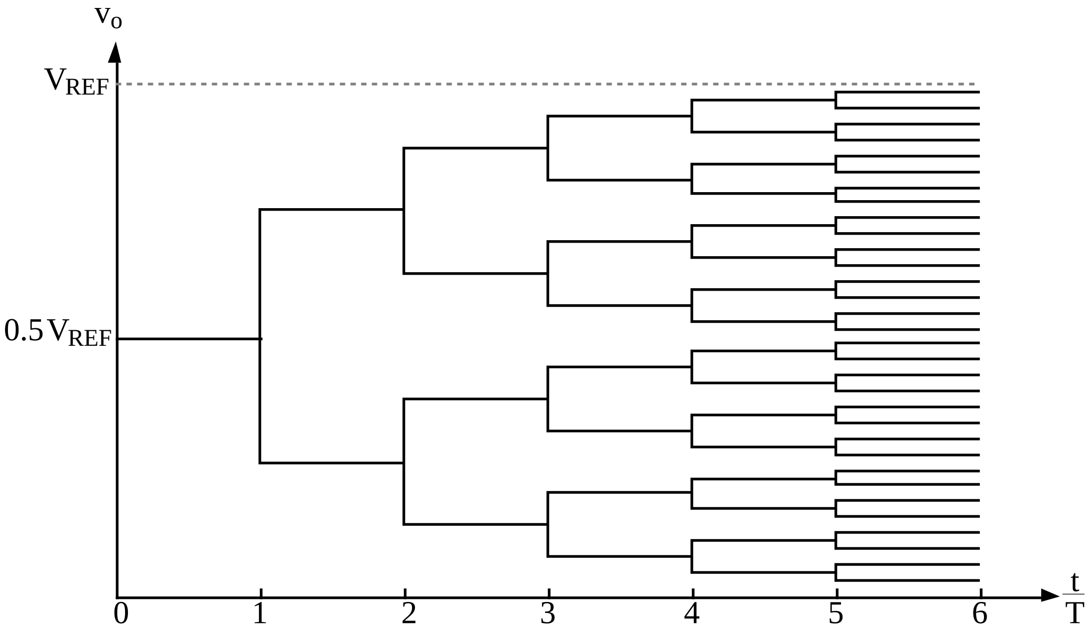
X.8 - MEDIUM SPEED A/D CONVERTERS

Conversion Time ≈ NT

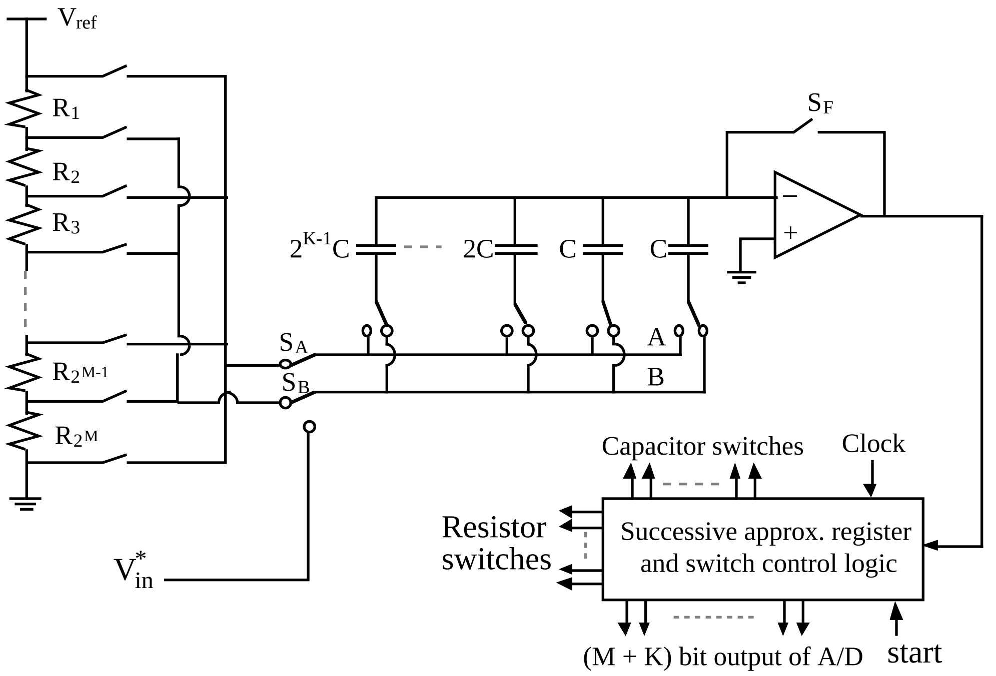
Successive ApproximationArchitecture:



Successive Approximation Process:



A Voltage-Charge Scaling Successive Approximation ADC



Operation:

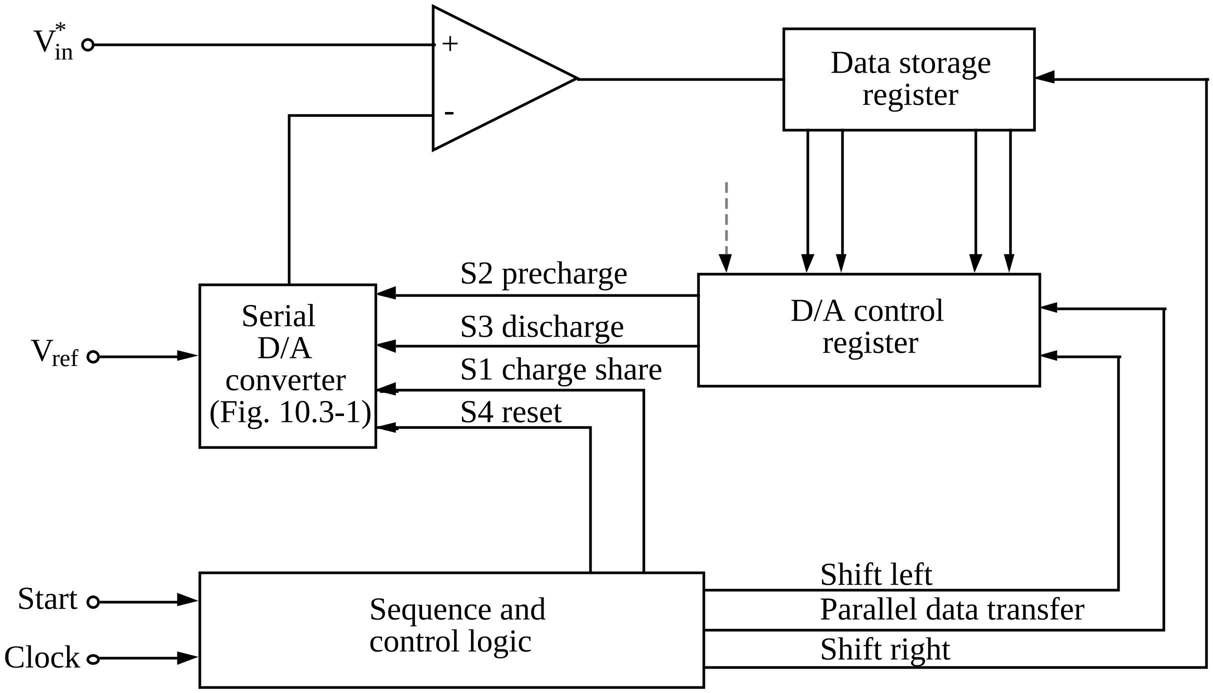
1.) With S_F closed, the bottom plates of all capacitors are connected through switch S_B to V_{in}^*. (Automatically accounts for voltage offsets).

2.) After S_F is opened, a successive approximation search among the resistor string taps to find the resistor segment in which the stored sample lies.

3.) Buses A and B are then connected across this segment and the capacitor bottom plates are switched in a successive approximation sequence until the comparator input voltage converges back to the threshold voltage.

Capable of 12-bit monotonic conversion with a DL of ±0.5LSB within 50µs.

A Successive Approximation ADC using a Serial DAC



Conversion Sequence:

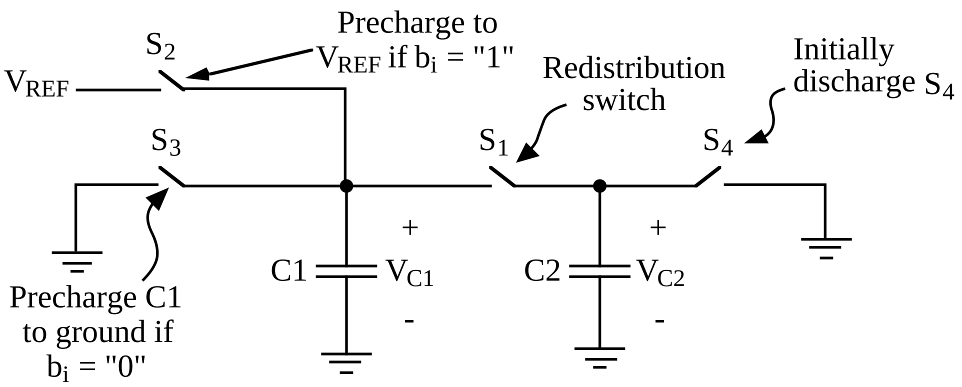
1.) Assume first K MSB's have been decided so that,

$$\text{Digital word} = a_M\frac{1}{2^N} + a_{N-1}\frac{1}{2^{N-1}} + \ldots + a_{N-K+1}\frac{1}{2^{N-K+1}} + .$$

2.) Assume (K + 1)th MSB is 1 and compare this analog output with V_{in}^* to determine a_{N-K}.

3.) Store a_{N-K} in the DATA storage register and contiune.

CHARGE REDISTRIBUTION SERIAL DAC

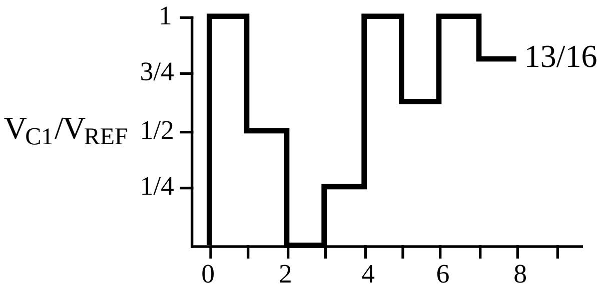


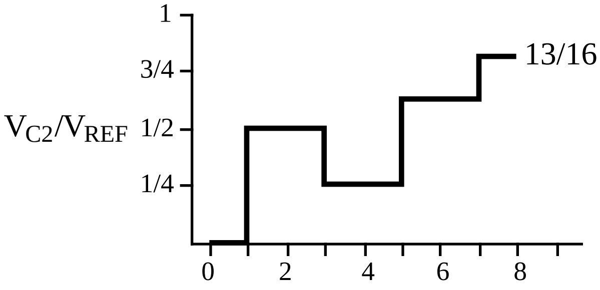
$C1 = C2$
b_0 = LSB
b_1 = NLSB
.
.
.
b_N = MSB

Conversion sequence:

4 Bit D/A Converter

INPUT WORD: 1101





Close S_4: $V_{C2} = 0$

Store with LSB first-

Close S_2 (b_0=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = \frac{V_{REF}}{2} = V_{C2}$

Close S_3 (b_1=0): $V_{C1} = 0$

Close S_1: $V_{C1} = V_{C2} = \frac{V_{REF}}{4}$

Close S_2 (b_2=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = V_{C2} = \frac{5}{8} V_{REF}$

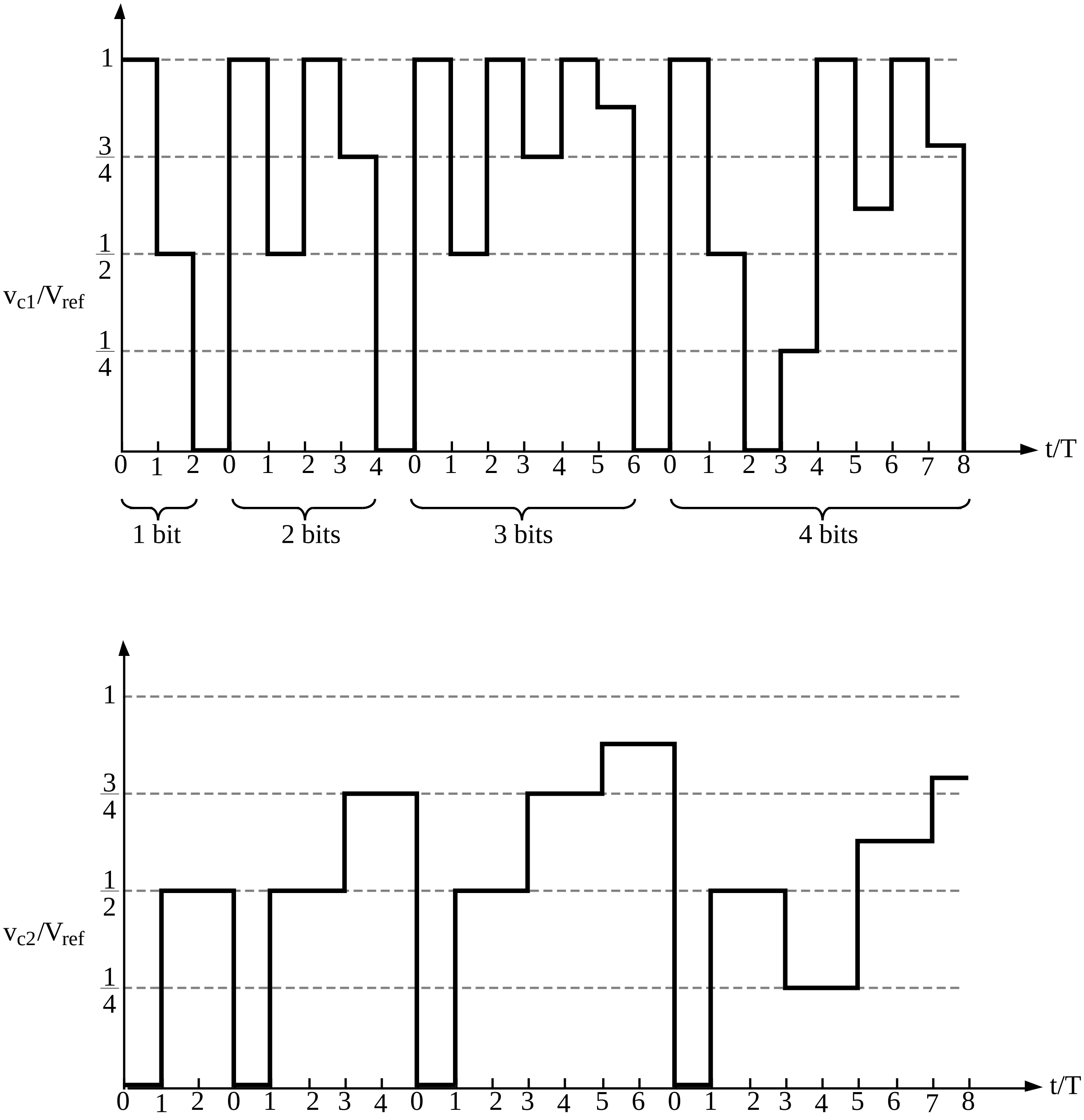
Close S_2 (b_3=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = V_{C2} = \frac{13}{16} V_{REF}$

Comments:

- LSB must go first.
- n cycles to make an n-bit D-A conversion.
- Top plate parasitics add error.
- Switch parasitics add error.

Serial ADC Waveform for an Input of (13/16V_{ref})

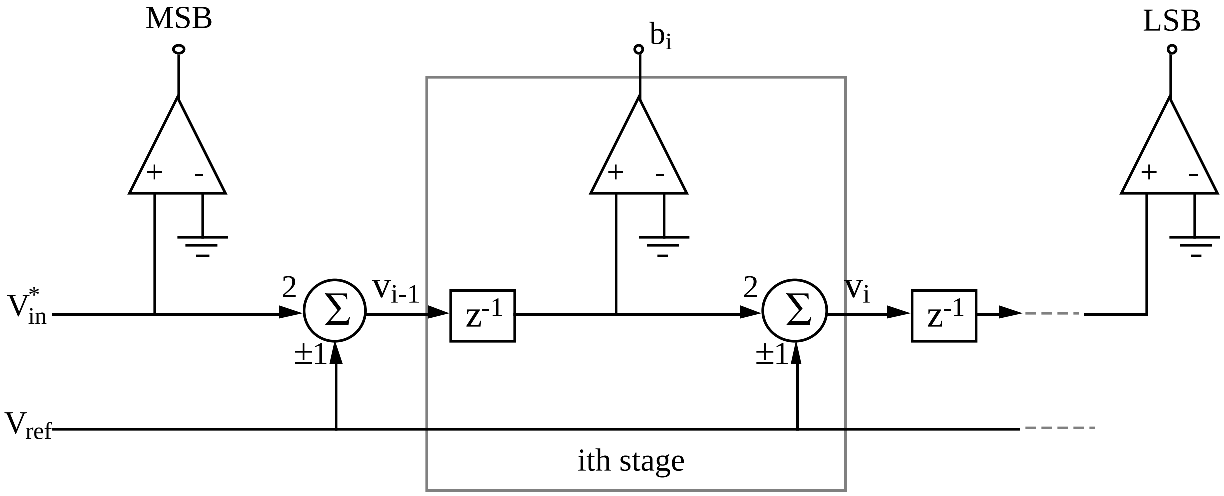


A 1-BIT/PIPE PIPELINE A/D CONVERTER

Single Bit/Stage, N-Stage Pipeline Converter

- Converter in 1 clock cycle using storage registers
- Requires N comparators
- Dependent upon passive component linearity
- Can use error correcting algorithms and self-calibration techniques

<u>Block Diagram of the 1-Bit/Pipe A/D Architecture</u>



$$V_i = 2V_{i-1} - b_iV_{ref} \quad \text{where} \begin{cases} b_i = +1 \text{ if } V_{i-1} > 0 \\ b_i = -1 \text{ if } V_{i-1} < 0 \end{cases}$$

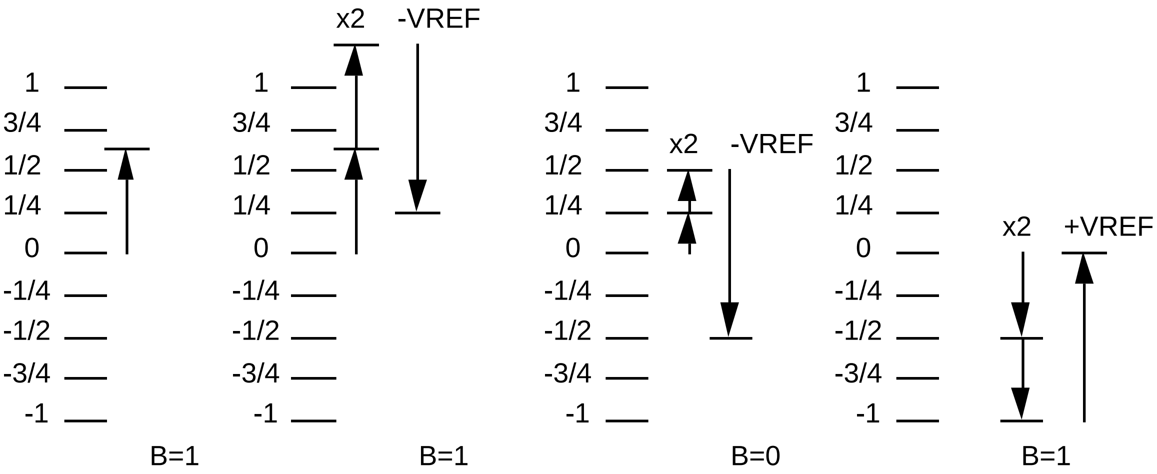
Output of the n-th stage can be written as:

$$V_N = \prod_{i=1}^{N} A_i V_{in} - \left[\sum_{i=1}^{N-1} \left(\prod_{j=i+1}^{N} A_j \right) b_i + b_N \right] V_{ref}$$

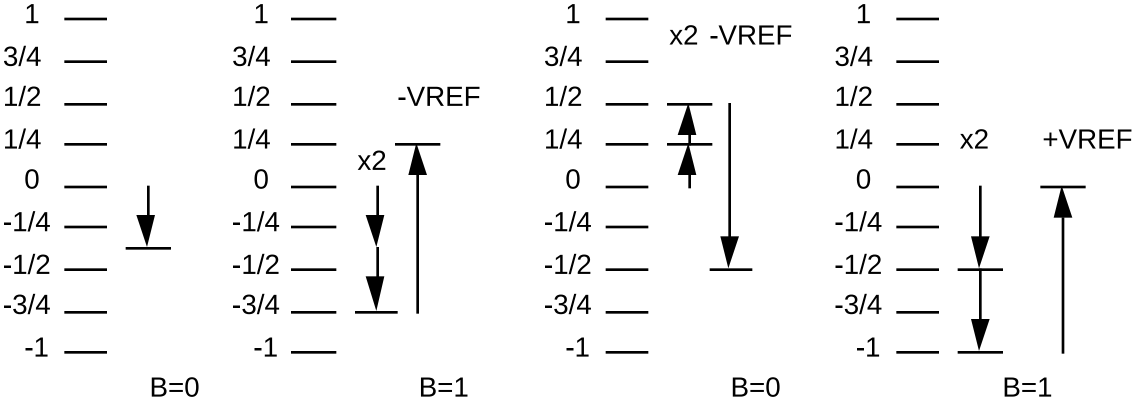
where A_i and b_i are the gain and bit value of the ith stage

Graphical Examples illustrating operation

Example 1

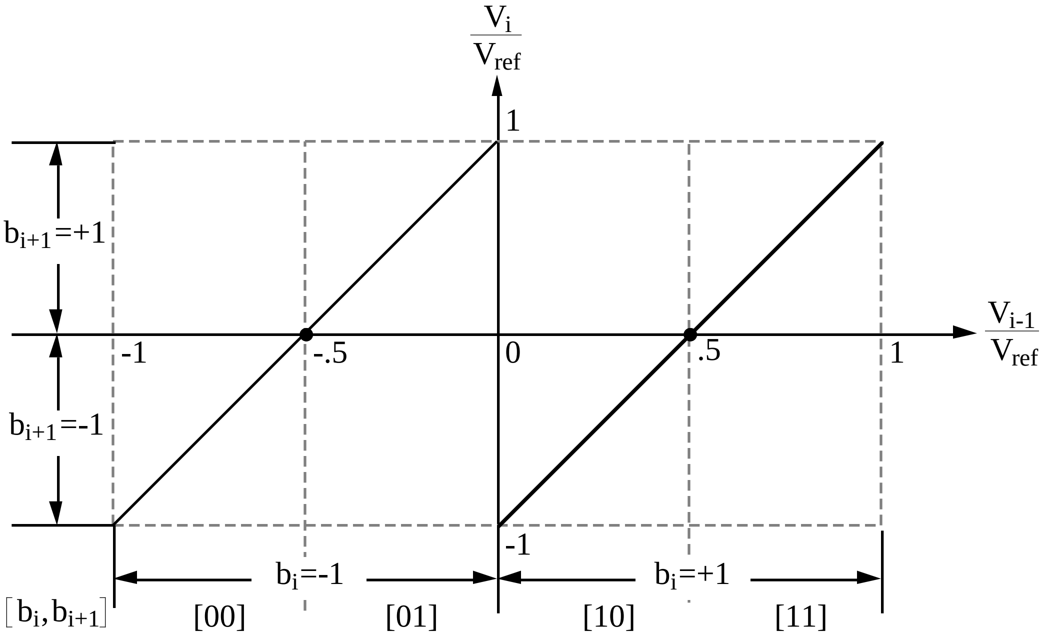


Example 2



IDEAL STAGE PERFORMANCE

ith Stage Plot of: $\frac{V_i}{V_{ref}} = 2\frac{V_{i-1}}{V_{ref}} - b_i$



1.) b_{i+1} must change at 0, and ±0.5V_{ref}. (when V_{i-1}=0 and ±0.5$V_{re\ f}$)

2.) b_i must change at V_i=0.

3.) V_i cannot exceed V_{ref}.

4.) V_i should not be less than V_{ref} when V_{i-1}=±V_{ref}.

IDEAL PERFORMANCE

Example

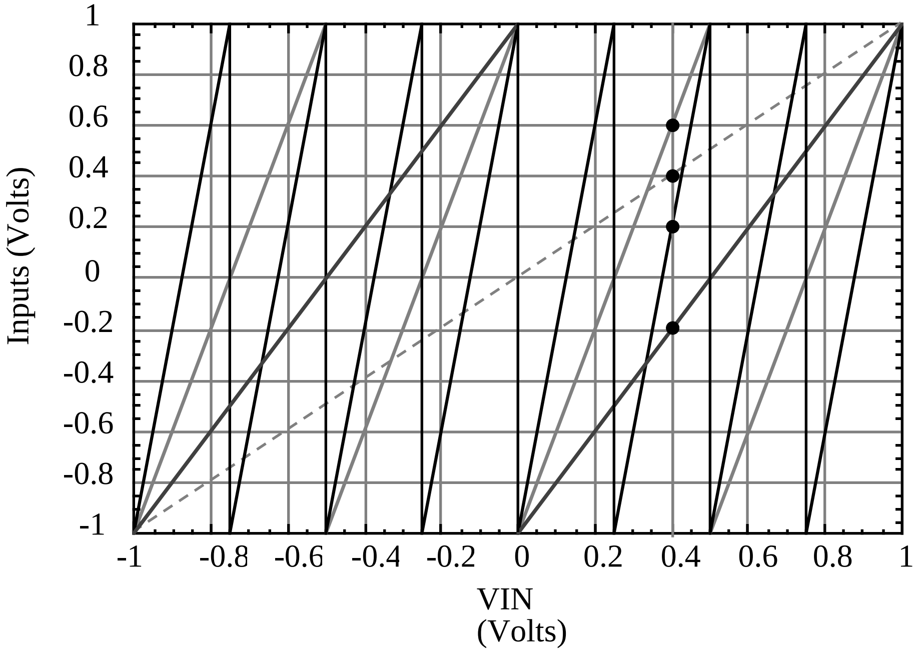
Assume $V_{in}^* = 0.4V$ and $V_{ref} = 1V$

Stage i	Input to the ith stage, V_{i-1}	$V_{i-1} > 0$?	Bit i
1	0.4	Yes	1
2	2(0.4000)-1 = -0.200	No	0
3	2(-0.200)+1 = +0.600	Yes	1
4	2(+0.600)-1 = +0.200	Yes	1

Results for various values ov Vin.

Vin	b(i)	v(i+1)	b(i+1)	v(i+2)	b(i+2)	v(i+3)	b(i+3)	v(i+4)	b(i+4)	v(i+5)
-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
-0.9	-1	-0.8	-1	-0.6	-1	-0.2	-1	0.6	1	0.2
-0.8	-1	-0.6	-1	-0.2	-1	0.6	1	0.2	1	-0.6
-0.7	-1	-0.4	-1	0.2	1	-0.6	-1	-0.2	-1	0.6
-0.6	-1	-0.2	-1	0.6	1	0.2	1	-0.6	-1	-0.2
-0.5	-1	0	1	-1	-1	-1	-1	-1	-1	-1
-0.4	-1	0.2	1	-0.6	-1	-0.2	-1	0.6	1	0.2
-0.3	-1	0.4	1	-0.2	-1	0.6	1	0.2	1	-0.6
-0.2	-1	0.6	1	0.2	1	-0.6	-1	-0.2	-1	0.6
-0.1	-1	0.8	1	0.6	1	0.2	1	-0.6	-1	-0.2
0	1	-1	-1	-1	-1	-1	-1	-1	-1	-1
0.1	1	-0.8	-1	-0.6	-1	-0.2	-1	0.6	1	0.2
0.2	1	-0.6	-1	-0.2	-1	0.6	1	0.2	1	-0.6
0.3	1	-0.4	-1	0.2	1	-0.6	-1	-0.2	-1	0.6
0.4	1	-0.2	-1	0.6	1	0.2	1	-0.6	-1	-0.2
0.5	1	0	1	-1	-1	-1	-1	-1	-1	-1
0.6	1	0.2	1	-0.6	-1	-0.2	-1	0.6	1	0.2
0.7	1	0.4	1	-0.2	-1	0.6	1	0.2	1	-0.6
0.8	1	0.6	1	0.2	1	-0.6	-1	-0.2	-1	0.6
0.9	1	0.8	1	0.6	1	0.2	1	-0.6	-1	-0.2
1	1	1	1	1	1	1	1	1	1	1

Output Voltage for a 4-stage Converter

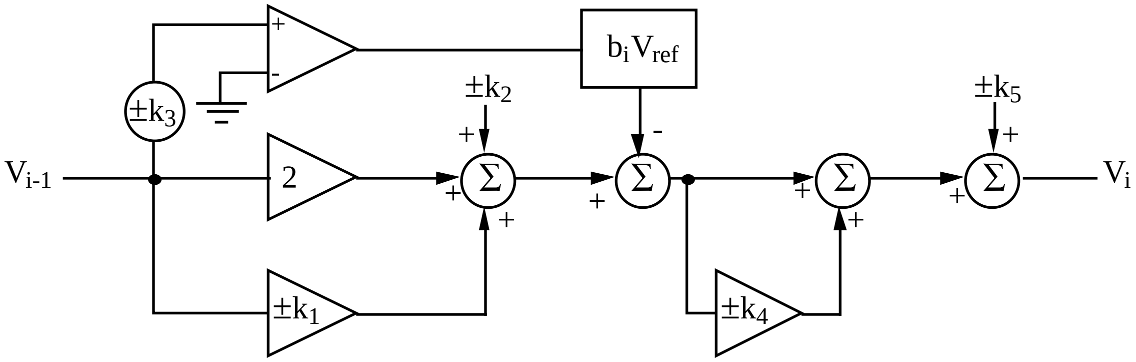


RESOLUTION LIMITS OF THE 1-BIT/STAGE PIPELINE ADC

1st-Order Errors of The 1-Bit/Stage Pipeline ADC

- Gain magnitude and gain matching (k_1)
- Offset of the X2 amplifier and the sample/hold (k_2)
- Comparator offset (k_3)
- Summer magnitude and gain matching (k_4)
- Summer offset (k_5)

Illustration:



$$\boxed{V_i = A_iV_{i-1} + V_{OSi} - b_iA_{si}V_{ref}}$$

where $b_i = \begin{cases} +1 \text{ if } V_{i-1} > \pm k_3 = \pm V_{OCi} \\ -1 \text{ if } V_{i-1} < \pm k_3 = \pm V_{OCi} \end{cases}$

A_i = all gain related errors of the ith stage

V_{OSi} = system offset errors of the ith stage

V_{OCi} = the comparator offset of the ith stage

A_{si} = the gain of the summing junction of the ith stage

Generalization of the First-Order Errors

Extending the ith stage first-order errors to N stages gives:

$$V_N = \prod_{i=1}^{N} A_i V_{in} + \left[\sum_{i=1}^{N-1}\left(\prod_{j=i+1}^{N} A_j\right) V_{OSi} + V_{OSN}\right]$$

$$- V_{ref}\left[\sum_{i=1}^{N-1}\left(\prod_{j=i+1}^{N} A_j\right) A_{si} b_i + A_{sN} b_N\right]$$

Assuming identical errors in each stage gives:

$$V_N = A^N V_{in} + \sum_{i=1}^{N} (A^{N-i}) V_{OS} - V_{ref}\left[\sum_{i=1}^{N} (A^{N-i}) A_s b_i\right]$$

Assuming only the first stage has errors:

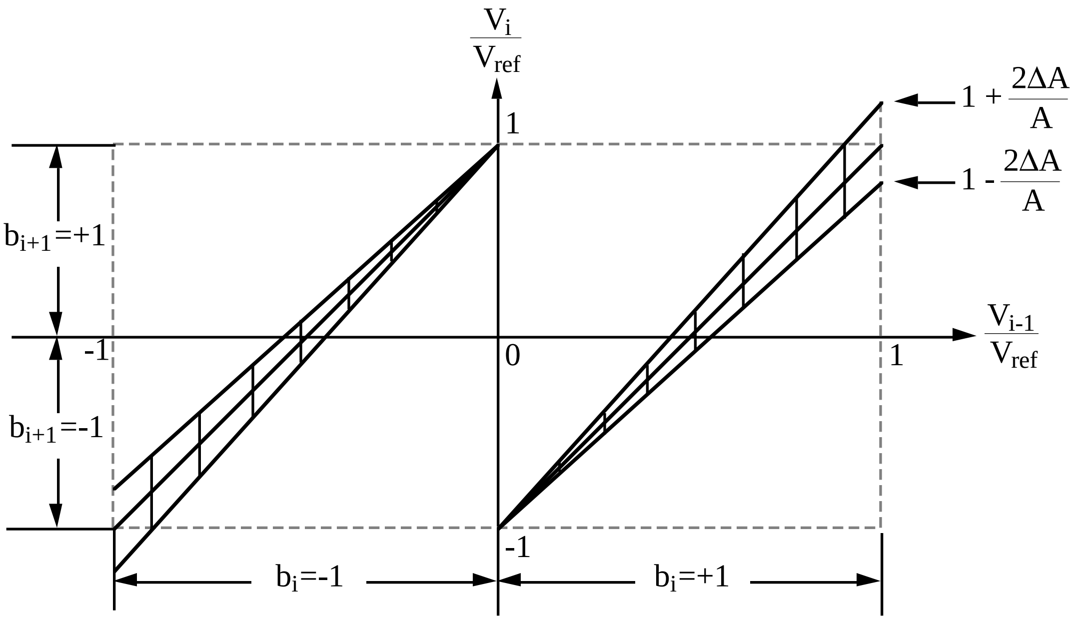
$$V_N = A_1 2^{N-1} V_{in} + 2^{N-1} V_{OS1} - V_{ref} 2^{N-1} A_{s1} b_1 - V_{ref} \sum_{i=2}^{N} (2^{N-i}) b_i$$

Identification of Errors

1. Gain Errors

$$\boxed{2^N(\Delta A/A) < 1} \Rightarrow N=10 \Rightarrow \frac{\Delta A}{A} < \frac{1}{1000}$$

Illustration of gain errors



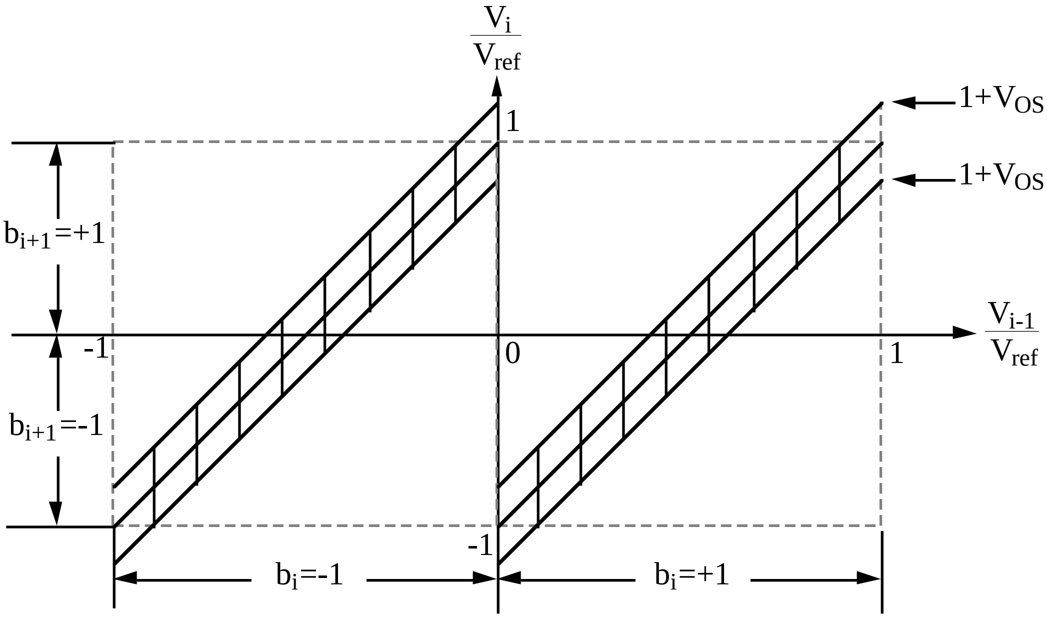
Identification of Errors - Cont'd

2. System Offset Errors

$$\boxed{V_{OS} < \frac{V_{ref}}{2^N}}$$

For N=10 and V_{ref} = 1V, V_{OS} < 1mV

Illustration of system offset error

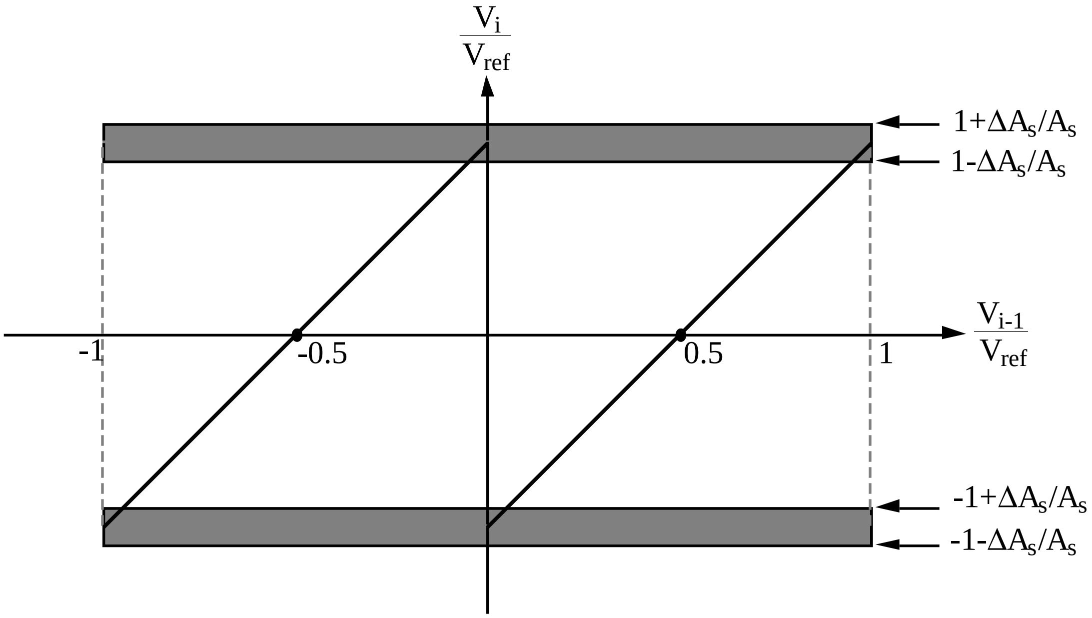


Identification of Errors - Cont'd

3. Summing Gain Error

$$\boxed{\frac{\Delta A_S}{A_S} < \frac{1}{2^N}}$$

For N=10, $\frac{\Delta A}{A} < \frac{1}{1024}$



Identification of Errors - Cont'd

4. Comparator Offset Error

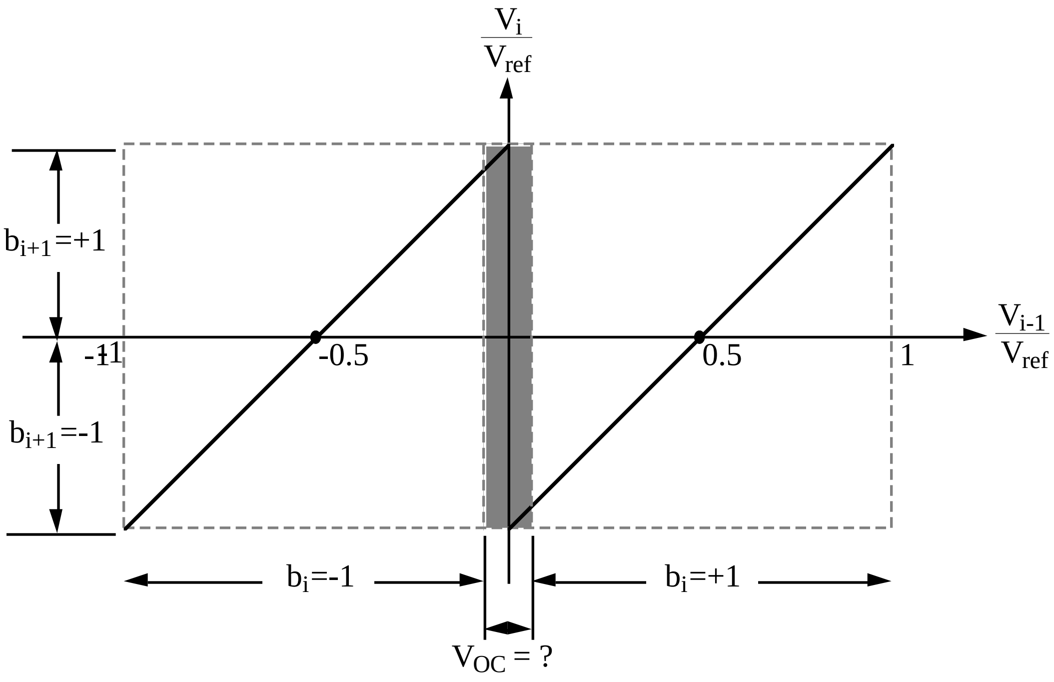
The comparator offset error is any nonzero value of the input to a stage where the stage bit is caused to change. It can be expressed as:

$$V_i = 2V_{i-1} - b_iV_{ref}$$

where

$$b_i = \begin{cases} +1 \text{ if } V_{i-1} > V_{OCi} \\ -1 \text{ if } V_{i-1} < V_{OCi} \end{cases}$$

Illustration of comparator offset error:



SUMMARY

1.) The 1-bit/pipe, pipeline converter which uses standard components including a sample and hold, an amplifier, and a comparator would be capable of realizing at most an 8 or 9 bit converter.

2.) The accuracy of the gains and offset of the first stage of an N-Bit converter must be within 0.5LSB.

3.) The accuracy of the gains and offset of a stage diminishes with the remaining number of stages to the output of the converter.

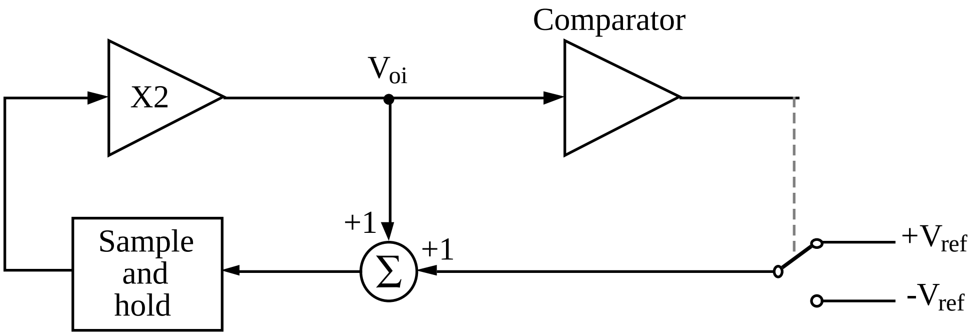
4.) Error correction and self-calibrating techniques are necessary in order to realize the potential resolution capability of the 1-bit/'stage pipeline ADC.

Cyclic Algorithmic A/D Converter

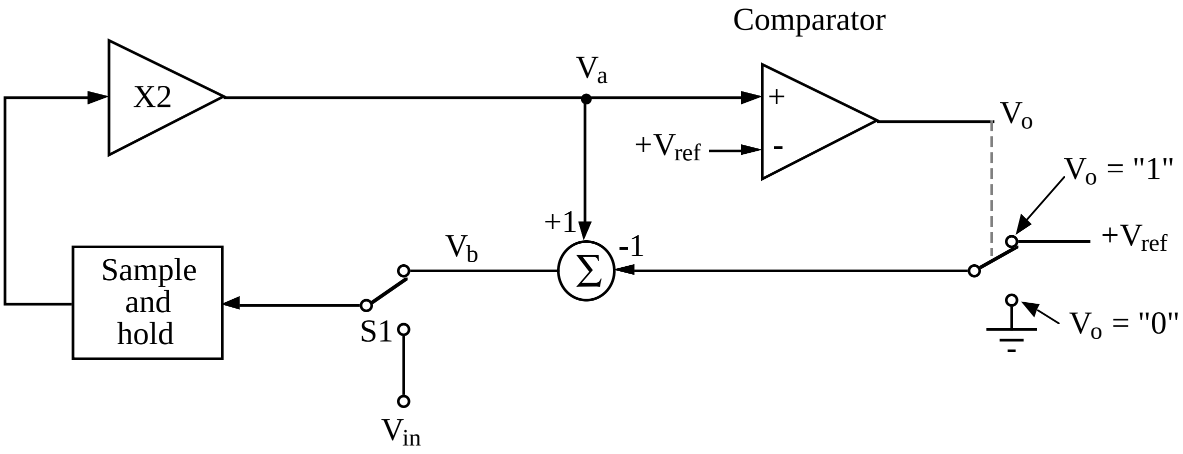
The output of the ith stage of a pipeline A/D converter is

$$V_{oi} = (2V_{o,i-1} - b_i V_{REF})z^{-1}$$

If V_{oi} is stored and feedback to the input, the same stage can be used for the conversion. The configuration is as follows:



Practical implementation:



Algorithmic ADC - Example

Assume that $V_{in}^* = 0.8V_{REF}$. The conversion proceeds as;

1.) $0.8V_{REF}$ is sampled and applied to the X2 amplifier by S1.

2.) $V_a(0)$ is $1.6V_{REF}$ (b_1=1) which causes $-V_{REF}$ to be subtracted from $V_a(0)$ giving

$V_b(0) = 0.6V_{REF}$

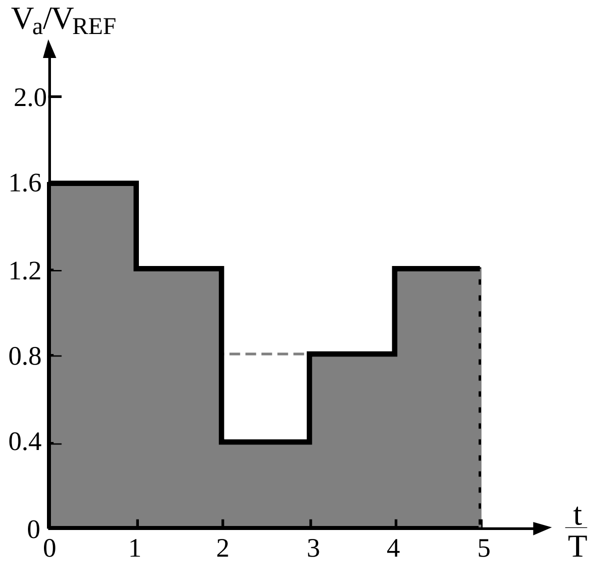
3.) In the next cycle, $V_a(1)$ is $1.2V_{REF}$ (b_2=1) and $V_b(1)$ is $0.2V_{REF}$.

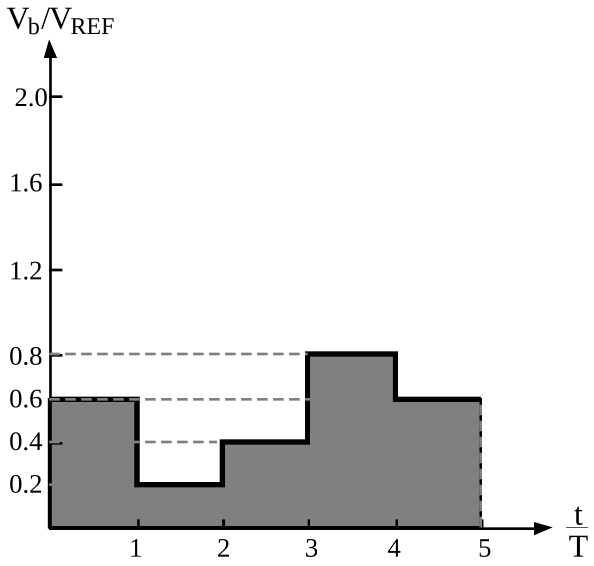
4.) The next cycle gives $V_a(2) = 0.4V_{REF}$ (b_3=0) and $V_b(2)$ is $0.4V_{REF}$.

5.) The next cycle gives $V_a(3) = 0.8V_{REF}$ (b_4=0) and $V_b(3)$ is $0.8V_{REF}$.

6.) Finally, $V_a(4) = 1.6V_{REF}$ (b_5=1) and $V_b(4) = 0.6V_{REF}$.

$\therefore$ The digital word is 11001. ⇒ $V_{analog} = 0.78125V_{REF}$.





Algorithmic A/D Converters-Practical Results

- Only one accurate gain-of-two amplifier required.
- Small area requirements
- Slow conversion time - nT.
- Errors: Finite op amp gain, input offset voltage, charge injection, capacitance voltage dependence.

Practical Converter

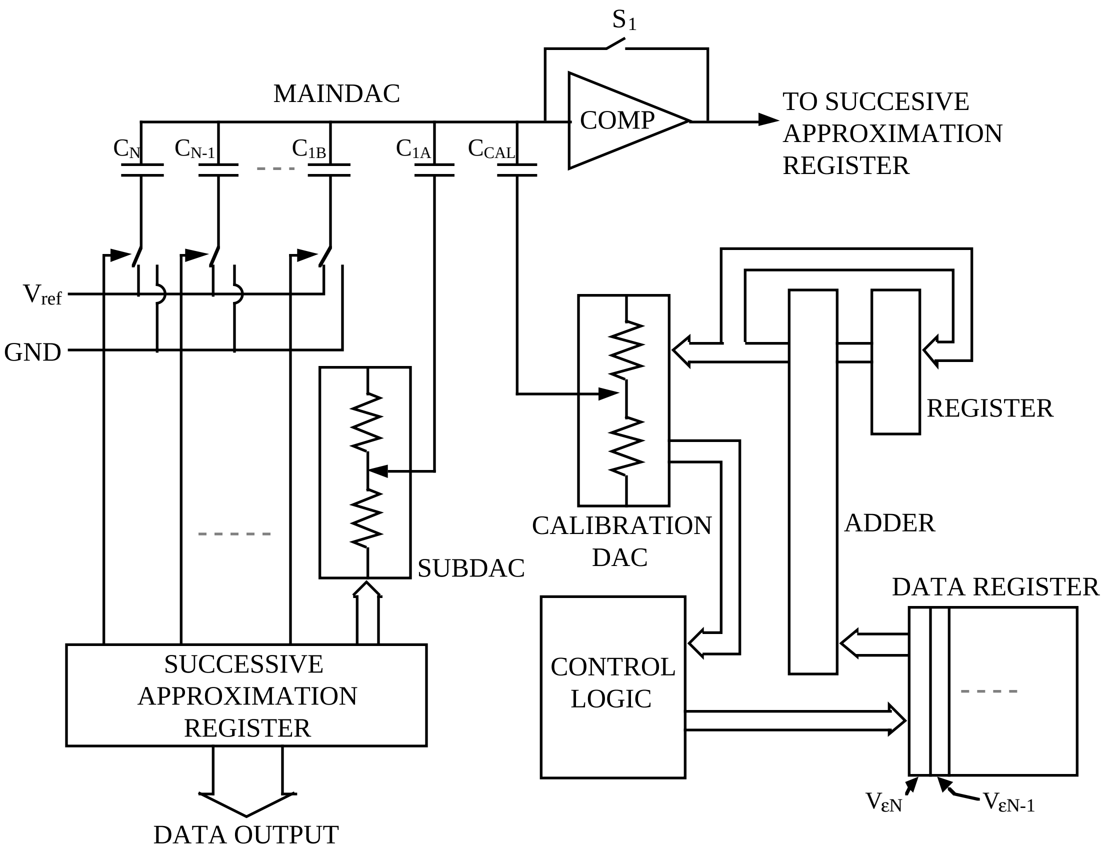
12 Bits

Differential linearity of 0.019% (0.8LSB)

Integral linearity of 0.034% (1.5LSB)

Sample rate of 4KHz.

SELF-CALIBRATING ADC's



Main ADC is an N-bit charge scaling array.

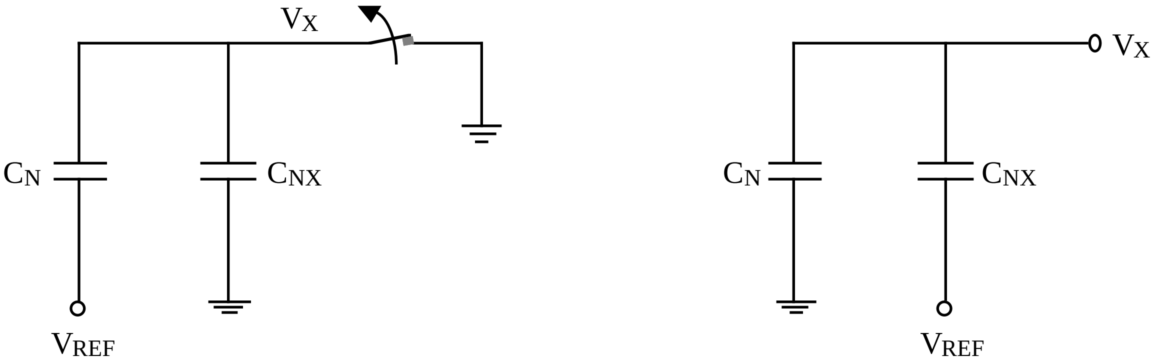
Sub DAC is an M-bit voltage scaling array.

Calibration DAC is an M+2 bit voltage scaling array.

This is an voltage-scaling, charge-scaling A/D converter with (N+M)- bits resolution.

Self-Calibration Procedure

During calibration cycles, the nonlinearity factors caused by capacitor mismatching are calibrated and stored in the data register for use in the following normal conversion cycles. The calibration procedure begins from MSB by connecting C_N to V_{REF} and the remaining capacitors C_{NX} to GND, then exchange the voltage connection as follows:



where $C_{NX} = C_{1B} + C_{1A} + ... + C_{N-1}$

The final voltage V_X after exchanging the voltage connections is

$$V_X = V_{REF} \frac{C_{NX} - C_N}{C_{NX} + C_N}$$

If the capacitor ratio is accurate and $C_{NX} = C_N \Rightarrow V_X = 0$,

otherwise $V_X \neq 0$. This residual voltage V_X is digitized by the calibration DAC. Other less significant bits are calibrated in the same manner.

After all bits are calibrated, the normal successive-approximation conversion cycles occurs. The calibrated data stored in the data register is converted to an analog signal by calibration DAC and is fed to the main DAC by C_{CAL} to compensate the capacitor mismatching error.

Self-Calibrating ADC Performance

Supply voltage ± 5V

Resolution of 16 bits

Linearity of 16 bits

Offset less than 0.25 LSB

Conversion time for 0.5 LSB linearity:

12 μs for 12 Bits

80 μs for 16 Bits.

RMS noise of 40 μV.

Power dissipation of 20 mW (excludes logic)

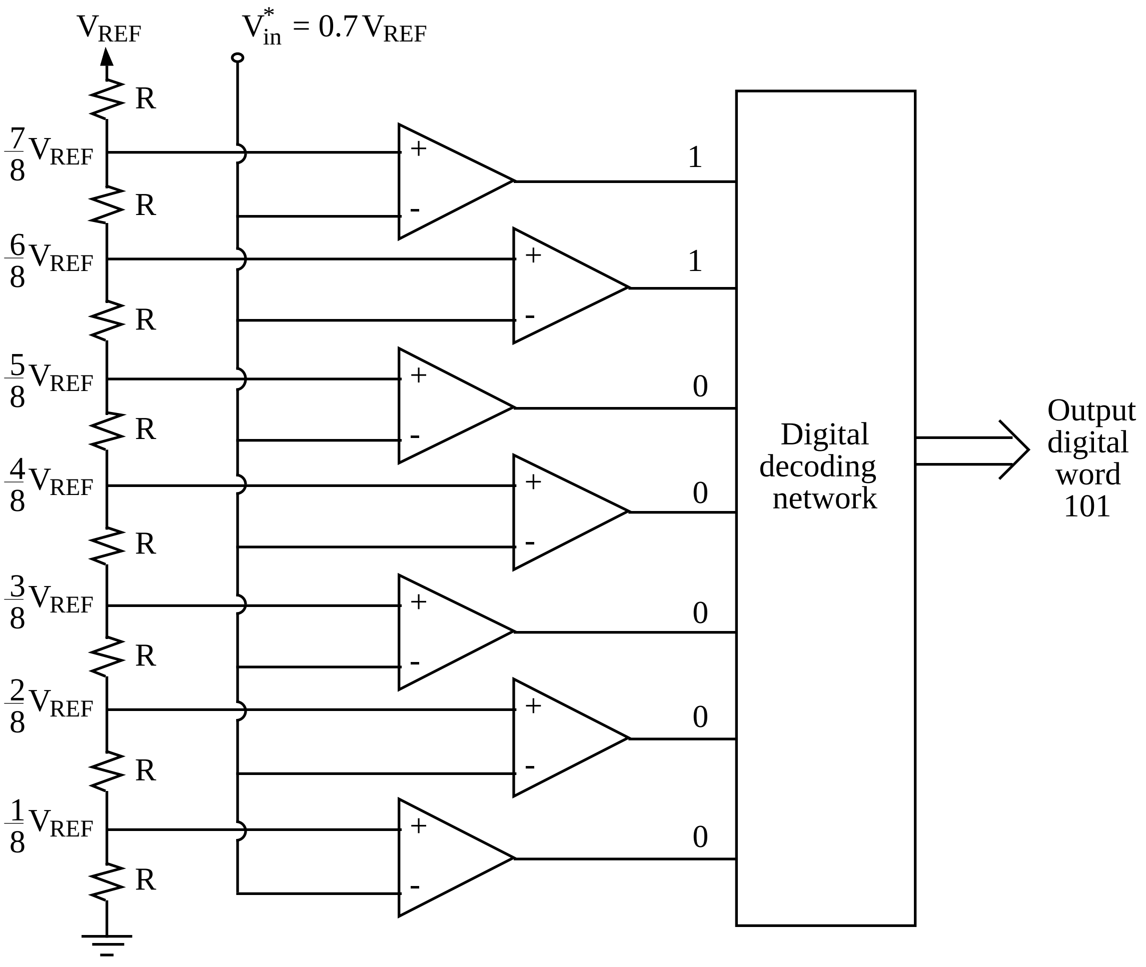
Area of 7.5 mm (excludes logic).

X.9 - HIGH SPEED ADC's

Conversion Time ≈ T (T = clock period)

- Flash or parallel
- Time interleaving
- Pipeline - Multiple Bits
- Pipeline - Single Bit

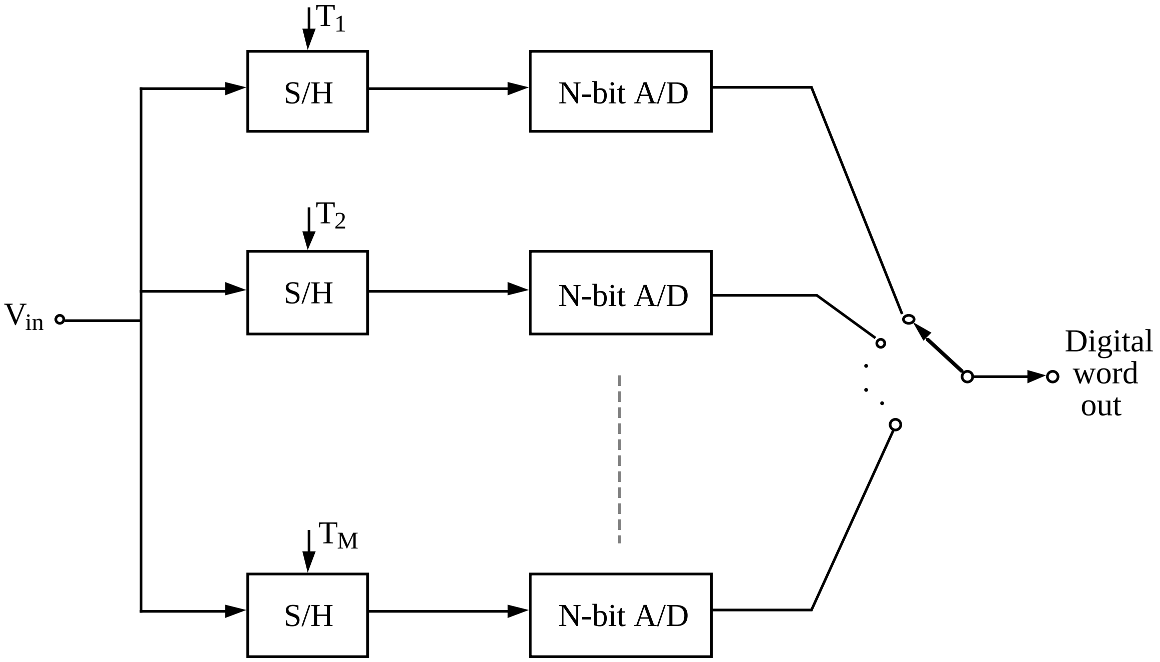
FLASH A/D CONVERTER

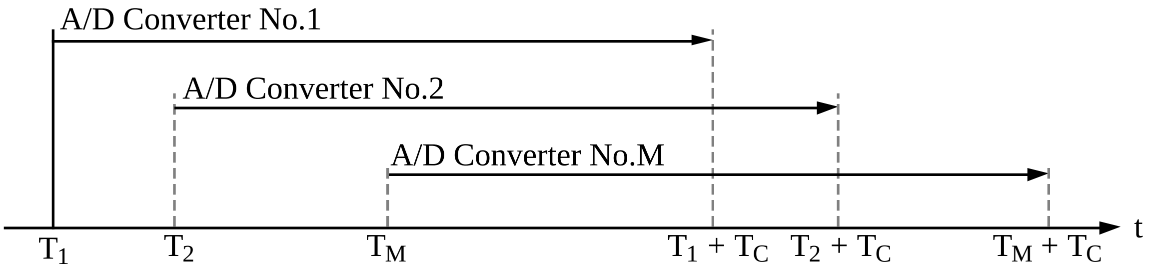


- Fast conversion time, one clock cycle
- Requires 2^N-1 comparators
- Maximum practical bits is 6 or less
- 6 bits at 10 MHz is practical

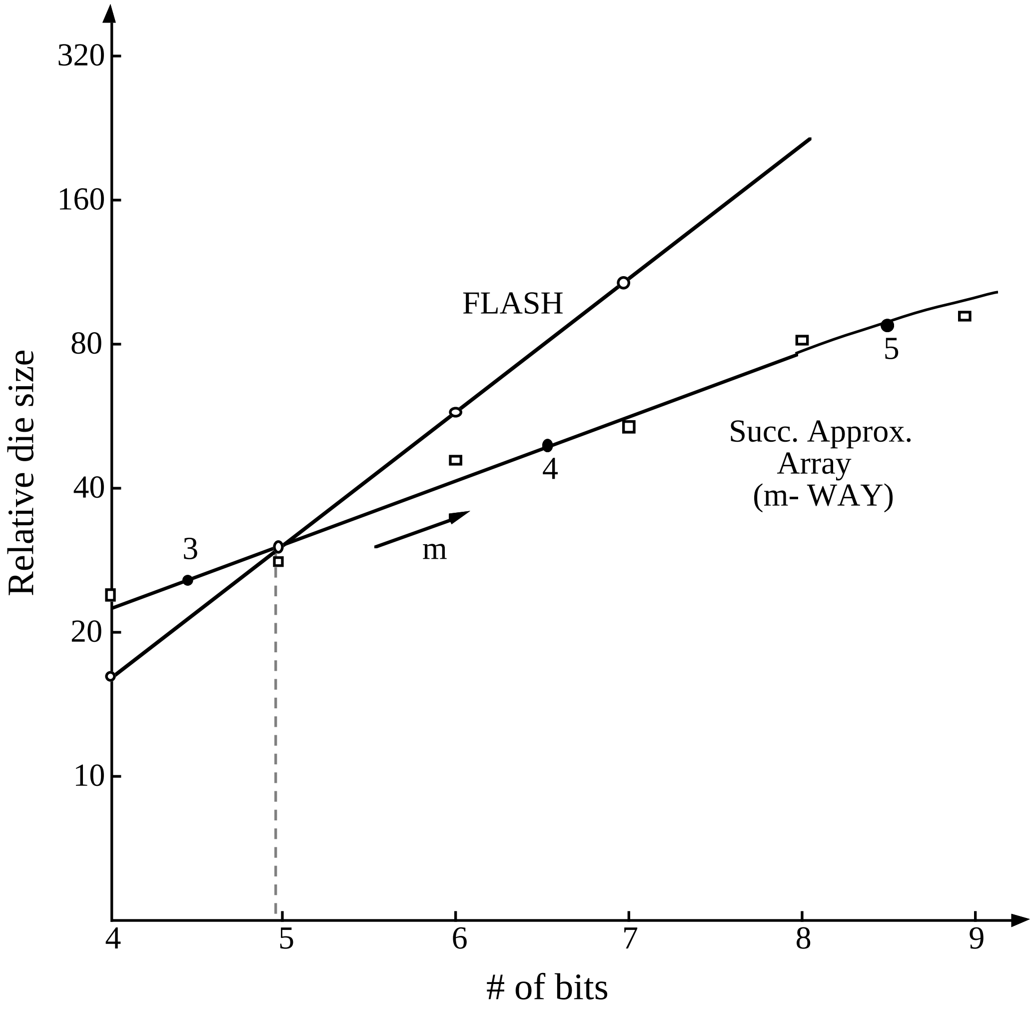
Time-Interleaved A/D Converter Array

Use medium speed, high bit converters in parallel.



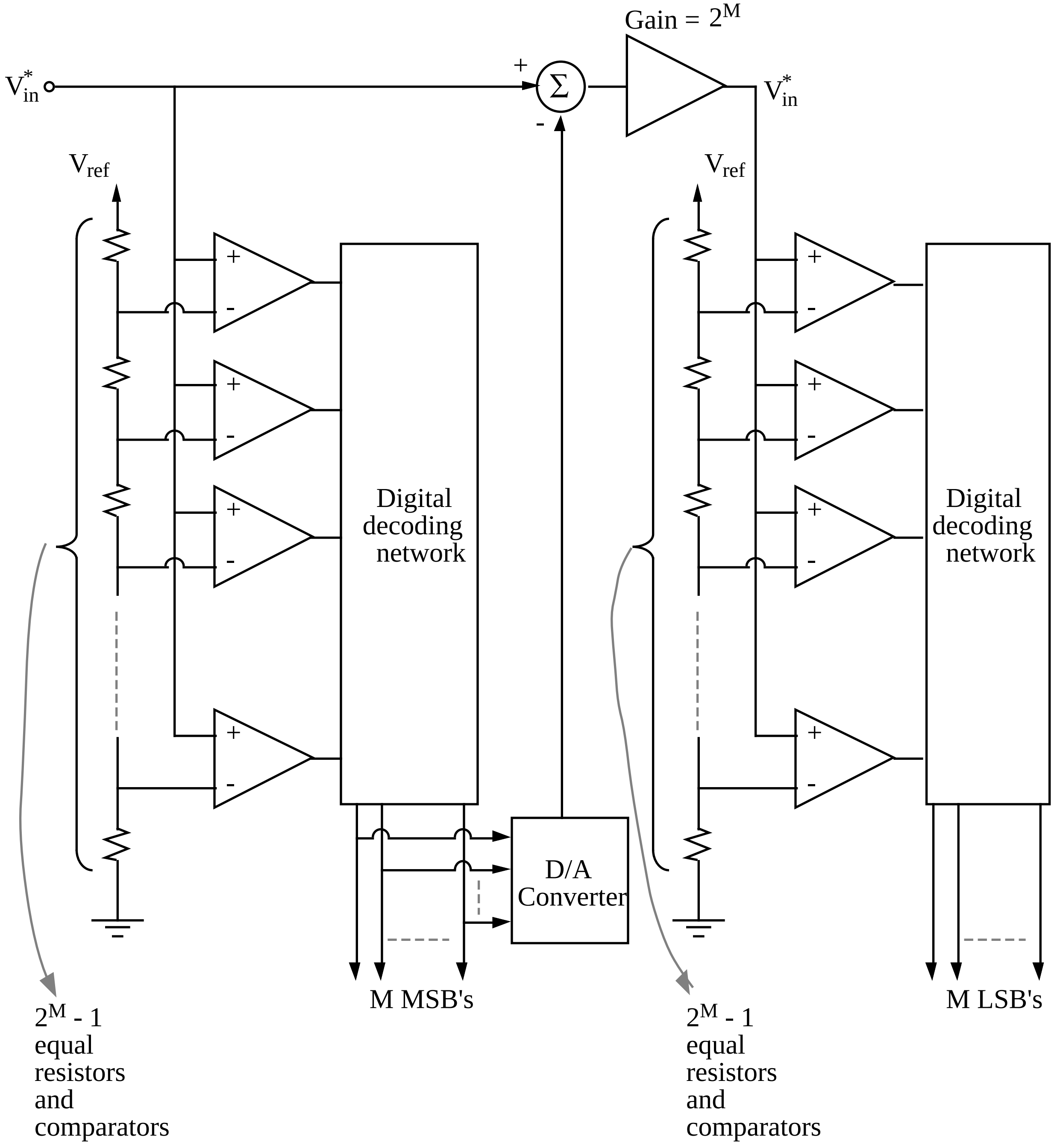


Relative Die Size vs. Number of Bits



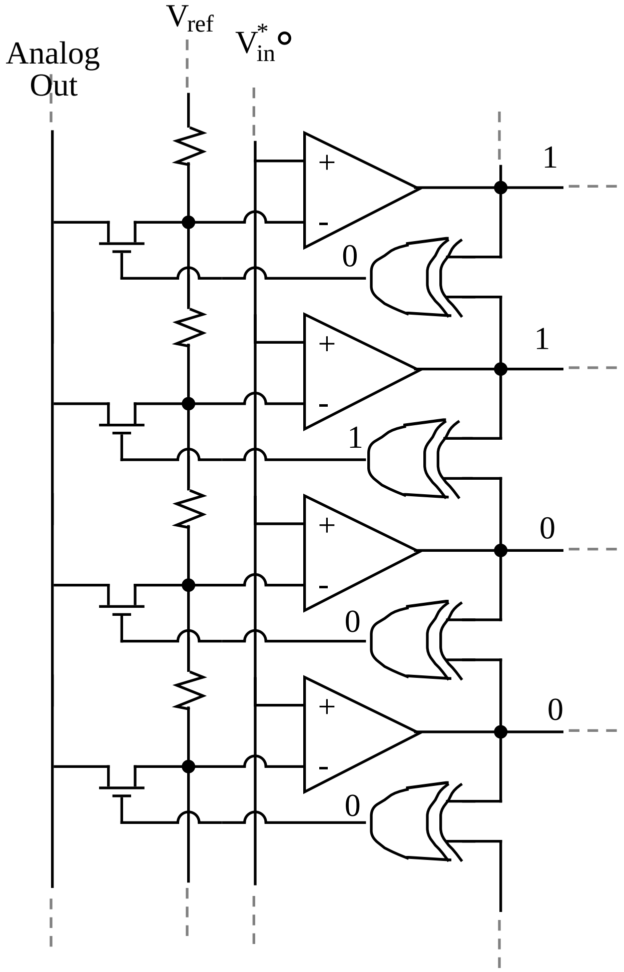
2M-BIT, PARALLEL-CASCADE ADC

- Compromise between speed and area
- 8-bit, 1M Hz.



Conversion of Digital back to Analog for Pipeline Architectures

Use XOR gates to connect to the appropriate point in the resistor divider resulting in the analog output corresponding to the digital output.

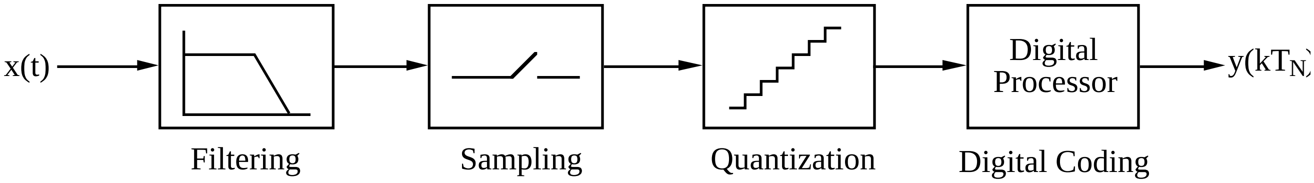


X.10 - OVERSAMPED (Δ-∑) A/D CONVERTER

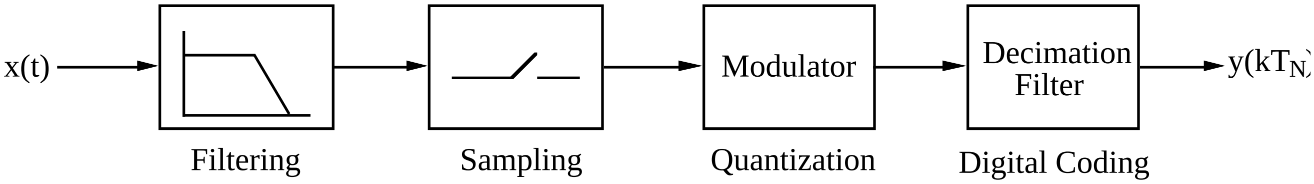
NYQUIST VERSUS OVERSAMPLED A/D CONVERTERS

Oversampling A/D converters use a sampling clock frequency(f_S) much higher than the Nyquist rate(fN).

Conventional Nyquist ADC Block Diagram:



Oversampling ADC Block Diagram



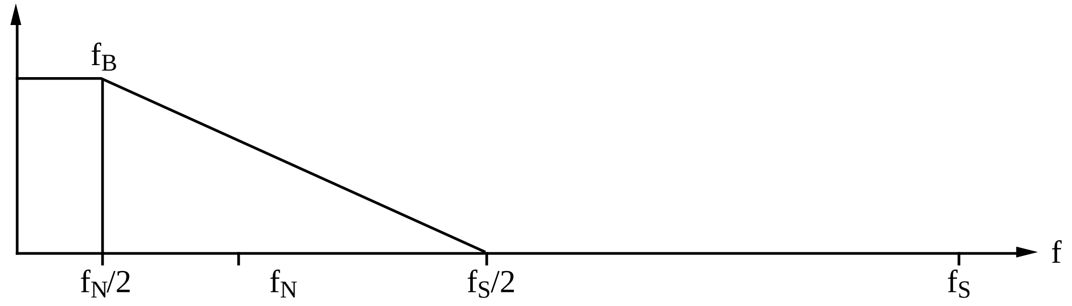
The anti-aliasing filter at the input stage limits the bandwidth of the input signal and prevents the possible aliasing of the following sampling step. The modulator pushes the quantization noise to the higher frequency and leaves only a small fraction of noise energy in the signal band. A digital low pass filter cuts off the high frequency quantization noise. Therefore, the signal to noise ratio is increased.

ANTI-ALIASING FILTER

The anti-aliasing filter of an oversampling ADC requires less effort than that of a conventional ADC. The frequency response of the anti-aliasing filter for the conventional ADC is sharper than the oversampling ADC.

Conventional ADC's Anti-Aliasing Filter

Oversampling ADC's Anti-Aliasing Filter



f_B : Signal Bandwidth
f_N : Nyquist Frequency, $f_N = 2f_B$
f_S : Sampling Frequency and usually $f_S >> f_N$
M : Oversampling ratio, $M = \frac{f_S}{f_N}$

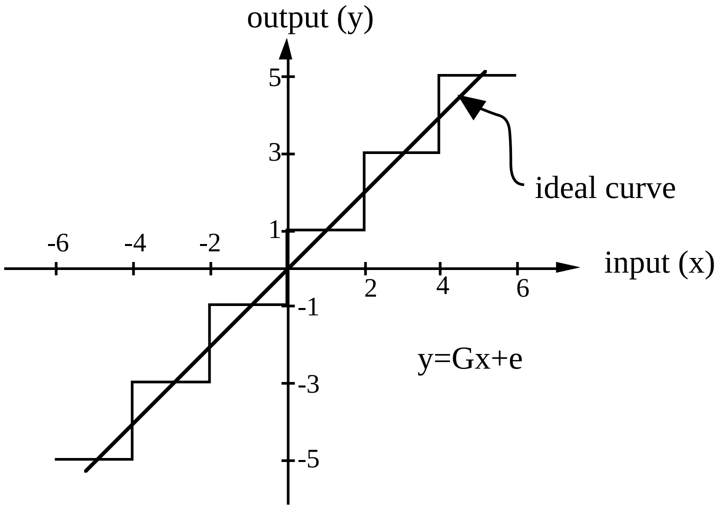
So the analog anti-aliasing filter of an oversampling ADC is less expensive than the conventional ADC. If M is sufficiently large, the analog anti-aliasing filter is simply an RC filter.

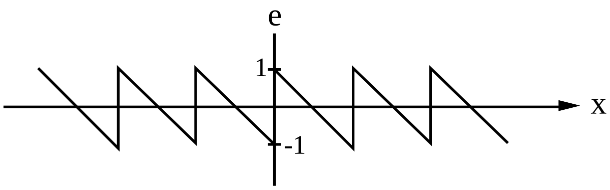
QUANTIZATION

Conventional ADC's Quantization

The resolution of conventional ADCs is determined by the relative accuracy of their analog components. For a higher resolution, self-calibration technique can be adopted to enhance the matching accuracy.

Multilevel Quantizer:





The quantized signal y can be represented by

$$y = Gx + e$$

where,

G = gain of ADC, normally = 1
e = quantization error

Conventional ADC's Quantization - Cont'd

The mean square value of quantization error, e, is

$$e^2_{rms} = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e(x)^2 \, dx = \frac{\Delta^2}{12}$$

where

$$\Delta = \text{the quantization level of an ADC (typically} \frac{VREF}{2^N})$$

When a quantized signal is sampled at f_S (= $1/\tau$), all of its noise power folds into the frequency band from 0 to $f_S/2$. If the noise power is white, then the spectral density of the sampled noise is

$$E(f) = e_{rms}\left(\frac{2}{f_S}\right)^{1/2} = e_{rms}\sqrt{2\tau}$$

where

$$\tau = 1/f_S \quad \text{and} \quad f_S = \text{sampling frequency}$$

The inband noise energy n_o is

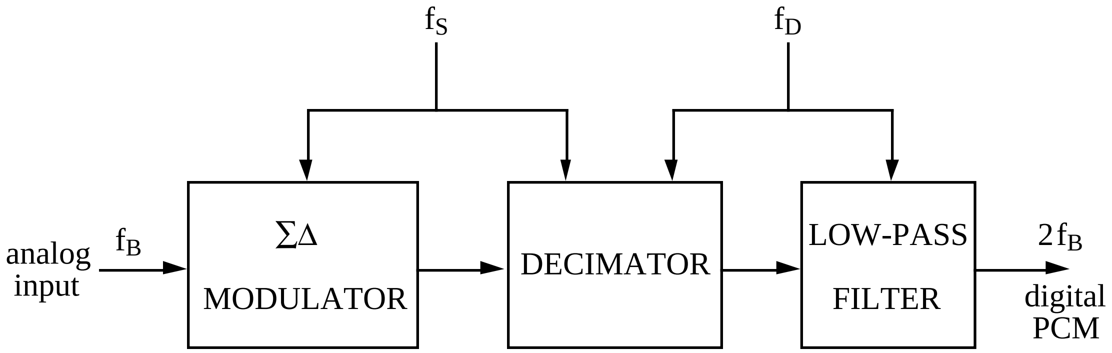
$$n_o^2 = \int_0^{f_B} E^2(f)df = e_{rms}^2 \, (2f_B\tau) = e_{rms}^2 \left(\frac{2f_B}{f_S}\right) = \frac{e_{rms}^2}{M}$$

$$n_o = \frac{e_{rms}}{\sqrt{M}}$$

The oversampling ratio $M = \dfrac{f_S}{2f_B}$

Therefore, each doubling of the sampling frequency decreases the in-band noise energy by 3 dB, and increases the resolution by 0.5 bit. This is not a very efficient method of reducing the inband noise.

OVERSAMPLING ADC



Oversampling ADCs consist of a ΣΔ modulator, a decimator (down-sampler), and a digital low pass filter.

ΣΔ modulator

Also called the noise shaper because it can shape the quantization noise and push majority of the noise to high frequency band. It modulates the analog input signal to a simple digital code, normally is one bit, using a sampling rate much higher the Nyquist rate.

Decimator

Also called the down-sampler because it down samples the high frequency modulator output into a low frequency output.

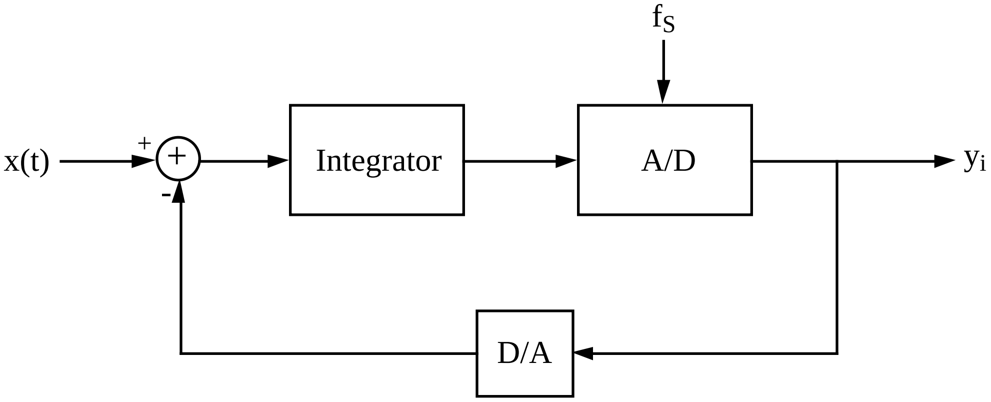
Low-pass filter

Use digital low pass filter to cut off the high frequency quantization noise and preserve the input signal.

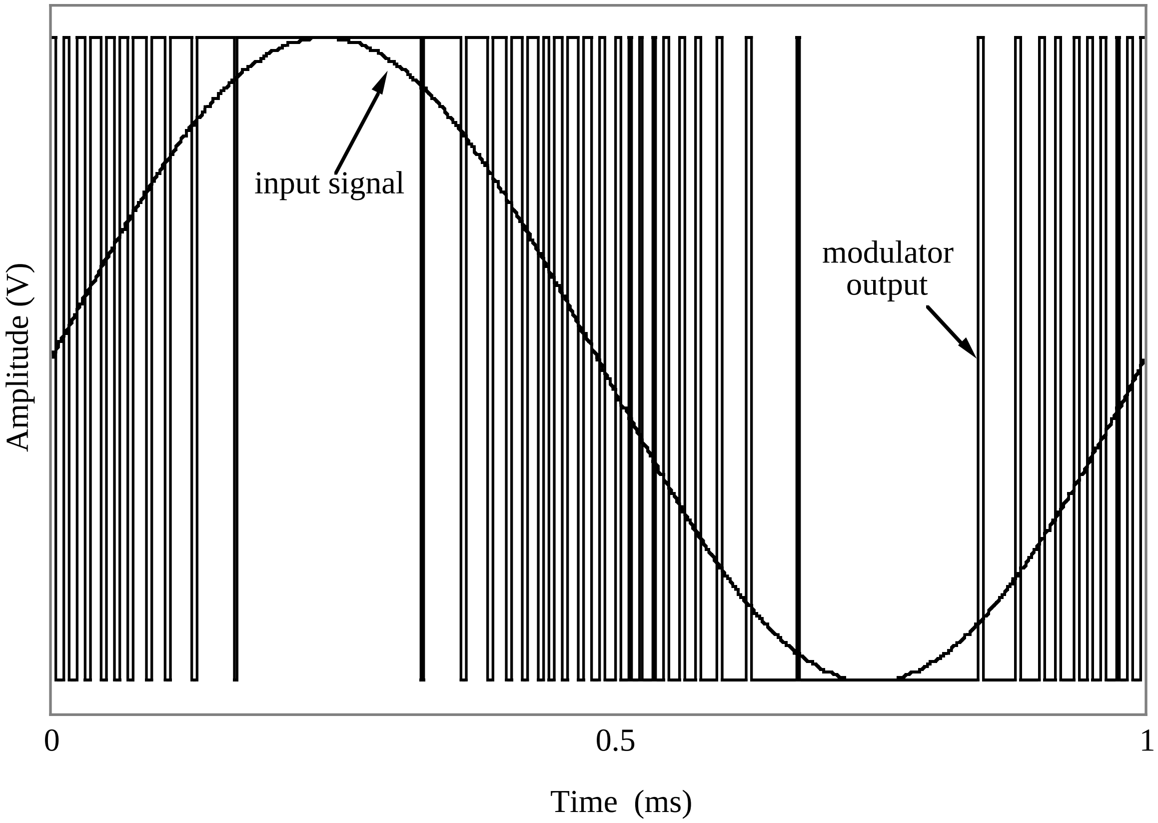
Sigma-Delta (∑Δ) Modulator

First Order ∑Δ Modulator

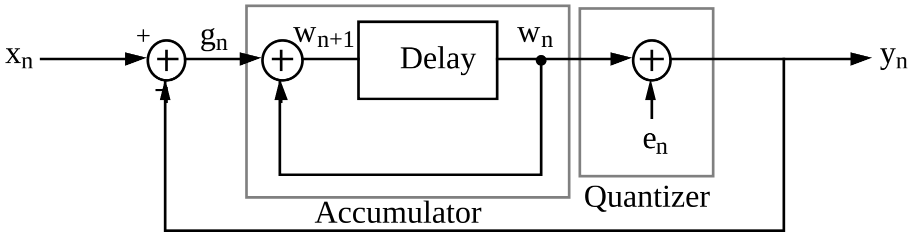
The open loop quantizer in a conventional ADC can be modified by adding a closed loop to become a ∑Δ modulator.



Modulator Output



First-Order ∑Δ Modulator



$$y_n = w_n + e_n$$

(1)

$$w_{n+1} = g_n + w_n = x_n - y_n + w_n$$

$$= x_n -(w_n + e_n) + w_n = x_n - e_n$$

(2)

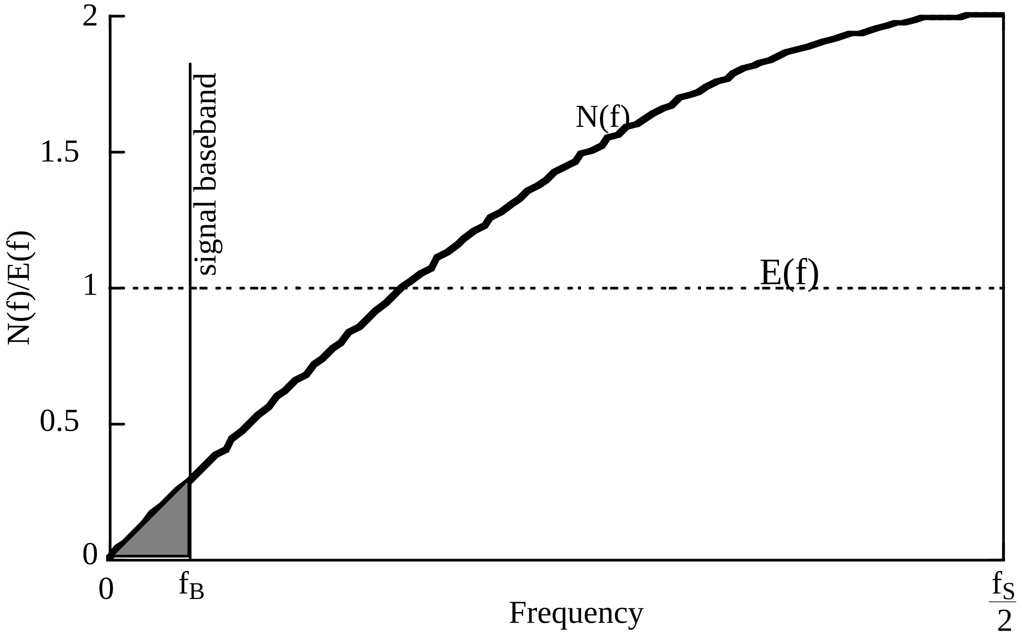
Therefore, $w_n = x_{n-1} - e_{n-1}$, which when substituted into (1) gives

$$y_n = x_{n-1} + (e_n - e_{n-1})$$

The output of ∑Δ modulator y_n is the input signal delayed by one clock cycle x_{n-1}, plus the quantization noise difference $e_n - e_{n-1}$. The modulation noise spectrum density of $e_n - e_{n-1}$ is

$$N(f) = E(f)\left|1 - z^{-1}\right| = E(f)\left|1 - e^{-j\omega\tau}\right| = 2E(f)\sin\left(\frac{\omega\tau}{2}\right) = 2e_{rms}\sqrt{2\tau}\,\sin\left(\frac{\omega\tau}{2}\right)$$

Plot of Noise Spectrum



First Order ∑Δ Modulator-Cont'd

The noise power in the signal band is

$$n_o^2 = \int_0^{f_B} |N(f)|^2 df = \int_0^{f_B} \left(2e_{rms}\sqrt{2\tau}\,\sin\left(\frac{\omega\tau}{2}\right)\right)^2 df$$

$$n_o^2 = \int_0^{f_B} \left(2e_{rms}\sqrt{2\tau}\,(\pi f\tau)\right)^2 df$$

$$\text{where } \sin\left(\frac{\omega\tau}{2}\right) = \sin\left(\frac{2\pi f}{2f_S}\right) = \sin\left(\frac{\pi f}{f_S}\right) \approx \pi f\tau$$

$$\text{if } f_S >> f$$

Therefore,

$$n_o^2 \approx (2\tau)^3\pi^2\, e_{rms}^2 \int_0^{f_B} f^{\,2}\, df = \frac{e_{rms}^2\pi^2(2\tau f_B)^3}{3}$$

$$\text{where , } f_S >> f_B$$

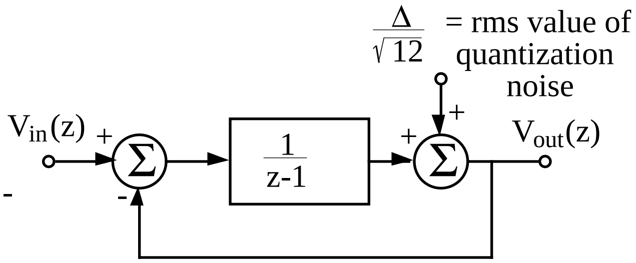
Thus,

$$n_o = e_{rms}\frac{\pi}{\sqrt{3}}\left(2f_B\tau\right)^{3/2} = e_{rms}\frac{\pi}{\sqrt{3}}M^{-3/2}$$

Each doubling of the oversampling ratio reduces the modulation noise by 9 dB and increase the resolution by 1.5 bits.

Oversampling Ratio Required for a First-Order ΔΣ Modulator

A block diagram for a first-order, sigma-delta modulator is shown in the z-domain. Find the magnitude of the output spectral noise with $V_{IN}(z) = 0$ and determine the bandwidth of a 10-bit analog-to-digital converter if the sampling frequency, f_S, is 10 MHz.



Solution

$$V_{out}(z) = e_{rms} + \left(\frac{1}{z-1}\right)[V_{in}(z) - V_{out}(z)]$$

or

$$V_{out}(z) = \left(\frac{z-1}{z}\right) e_{rms} \text{ if } V_{in}(z) = 0 \;\rightarrow\; V_{out}(z) = (1-z^{-1})e_{rms}$$

$$|N(f)| = E(f)\left|1 - e^{-j\omega\tau}\right| = 2E(f)\sin\left(\frac{\omega\tau}{2}\right) = 2\sqrt{\frac{2}{f_S}}\, e_{rms}\sin\left(\frac{\omega\tau}{2}\right)$$

The noise power is found as

$$n_o^2(f) = \int_0^{f_B}|N(f)|^2\, df = \int_0^{f_B}\left(2\sqrt{\frac{2}{f_S}}\, e_{rms}\right)^2 \sin^2\left(\frac{2\pi f\tau}{2}\right) df$$

Let $\sin\left(\frac{2\pi f\tau}{2}\right) \approx \pi f\tau$ if $f_S >> f_B$. Therefore,

$$n_o^2(f) = 4\left(\frac{2}{f_S}\right)e_{rms}^2\,(\pi\tau)^2\int_0^{f_B} f^2\, df = \frac{8\pi^2}{3}\,e_{rms}^2\left(\frac{f_B}{f_S}\right)^3$$

or

$$n_o(f) = \sqrt{\frac{8}{3}}\;\pi\cdot e_{rms}\left(\frac{f_B}{f_S}\right)^{3/2} \le \frac{VREF}{2^{10}}$$

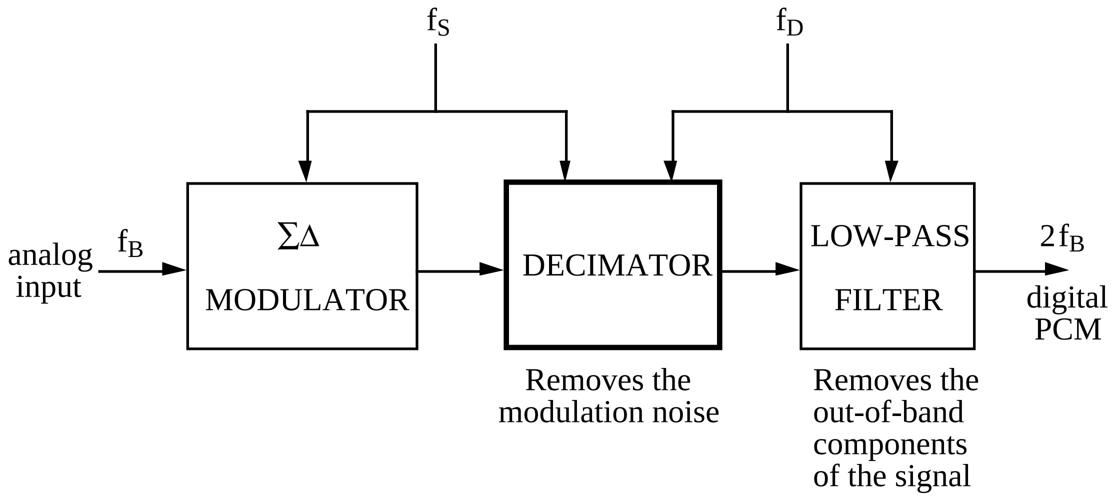
Solving for f_B/f_S gives (using Δ in e_{rms} term is equal to VREF)

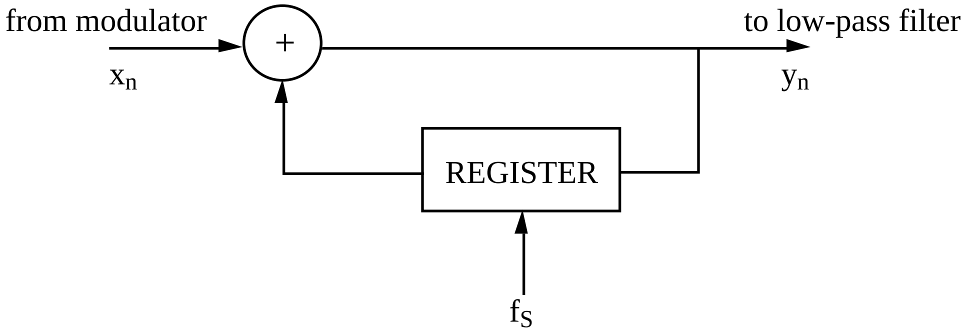
$$\frac{f_B}{f_S} = \left[\left(\frac{\sqrt{12}\sqrt{3}}{\sqrt{8}\,\pi}\right)\frac{1}{2^{10}}\right]^{2/3} = [0.659\text{x}10^{-3}]^{2/3} = 0.007576$$

$$f_B = 0.007576\cdot 10\text{MHz} = 75.76\text{kHz}.$$

Decimator (down-sampling)

The one-bit output from the ∑Δ modulator is at very high frequency, so we need a decimator (or down sampler) to reduce the frequency before going to the digital filter.





$$y_n = \frac{1}{N}\sum_{N=0}^{N} x_n \quad \text{, where } N = \frac{f_S}{f_D} \text{ = down-sampling ratio}$$

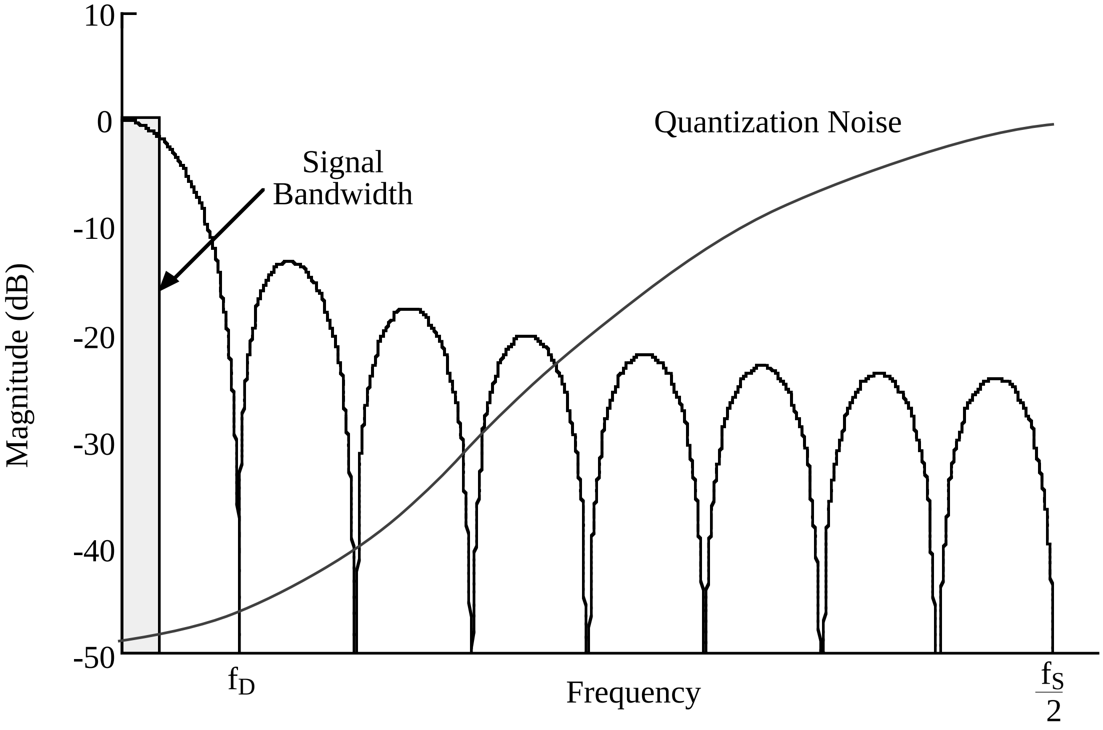
The transfer function of decimator is

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{N}\sum_{i=0}^{N-1} z^{-i} = \frac{1}{N}\,\frac{1 - z^{-N}}{1 - z^{-1}}$$

$$H(e^{j\omega\tau}) = \frac{\mathrm{sinc}(\pi f N\tau)}{\mathrm{sinc}(\pi f\tau)}$$

Frequency Spectrum of the Decimator

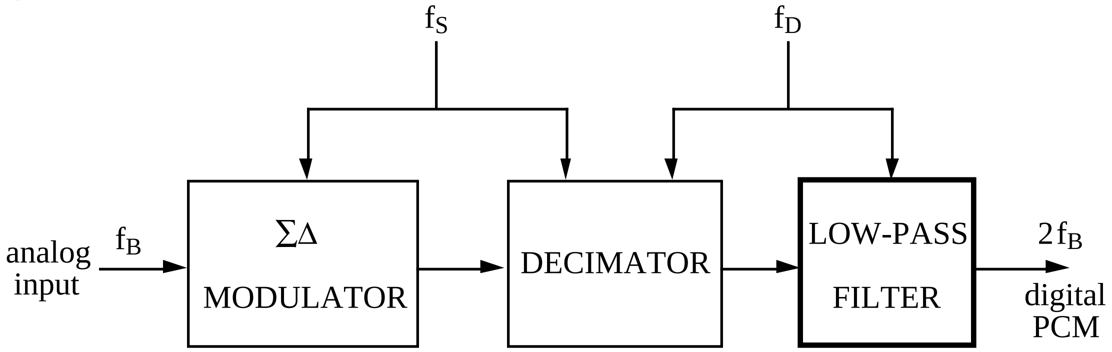
$$H(e^{j\omega\tau}) = \frac{\text{sinc}(\pi fN\tau)}{\text{sinc}(\pi f\tau)}$$



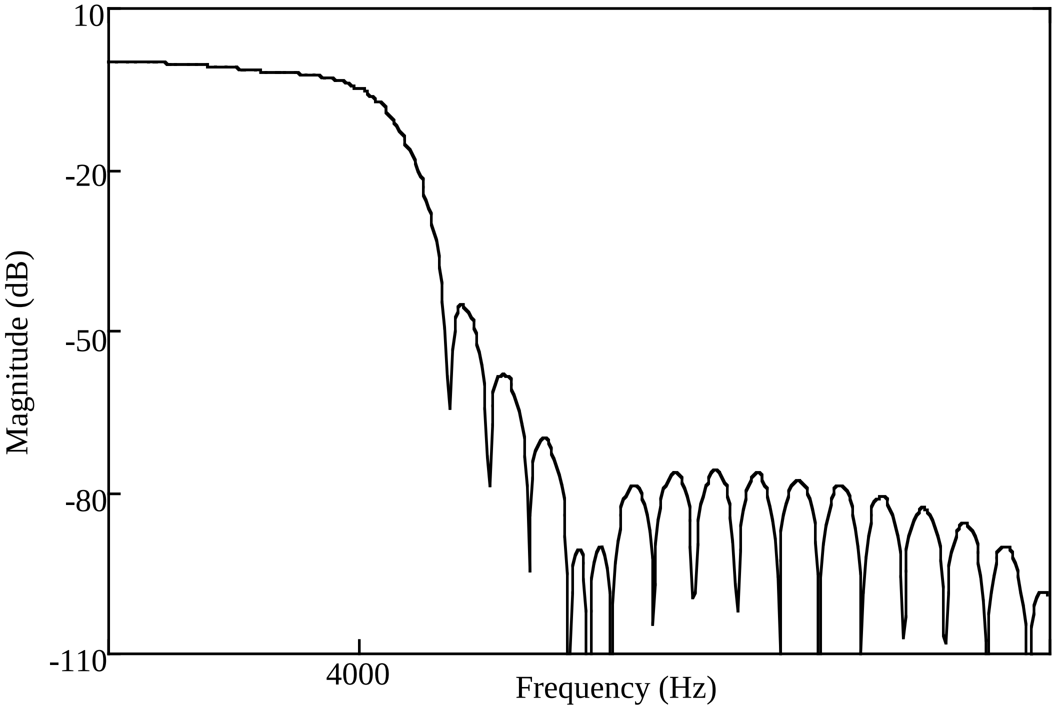
f_D = intermediate decimation frequency

When the modulation noise is sampled at f_D, its components in the vicinity of f_D and the harmonics of f_D fold into the signal band. Therefore, the zeros of the decimation filter must be placed at these frequencies.

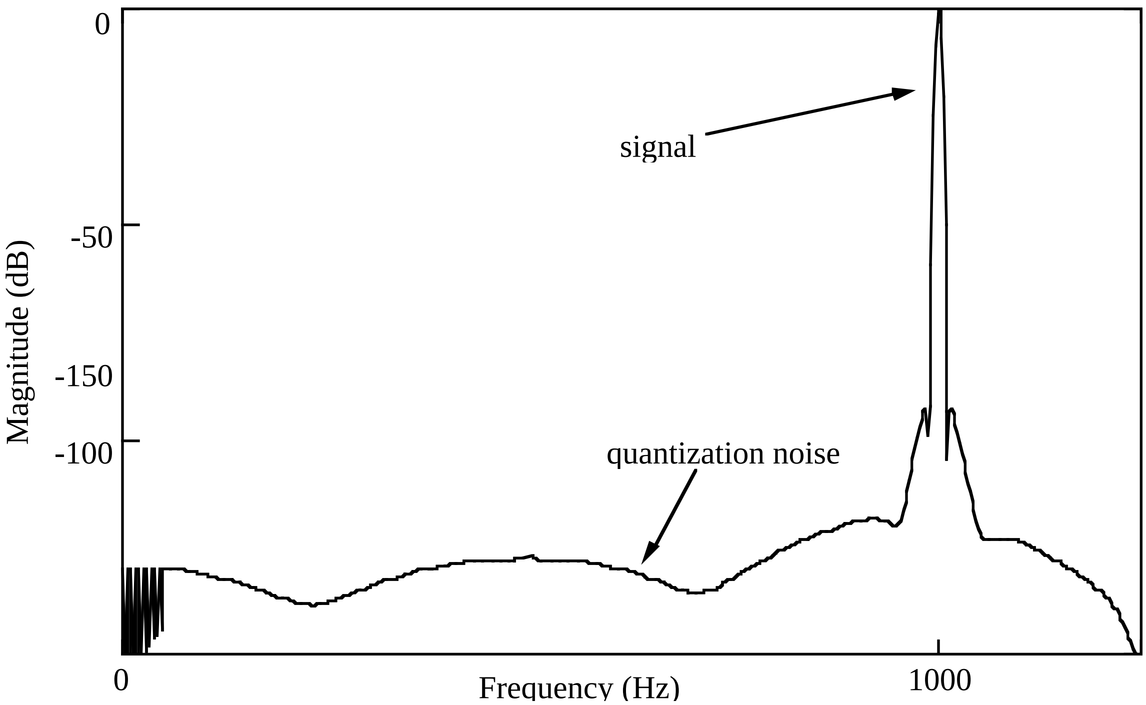
Digital Lowpass Filter



FIR or IIR digital low pass filter



After Digital Low Pass Filtering



Bit resolution

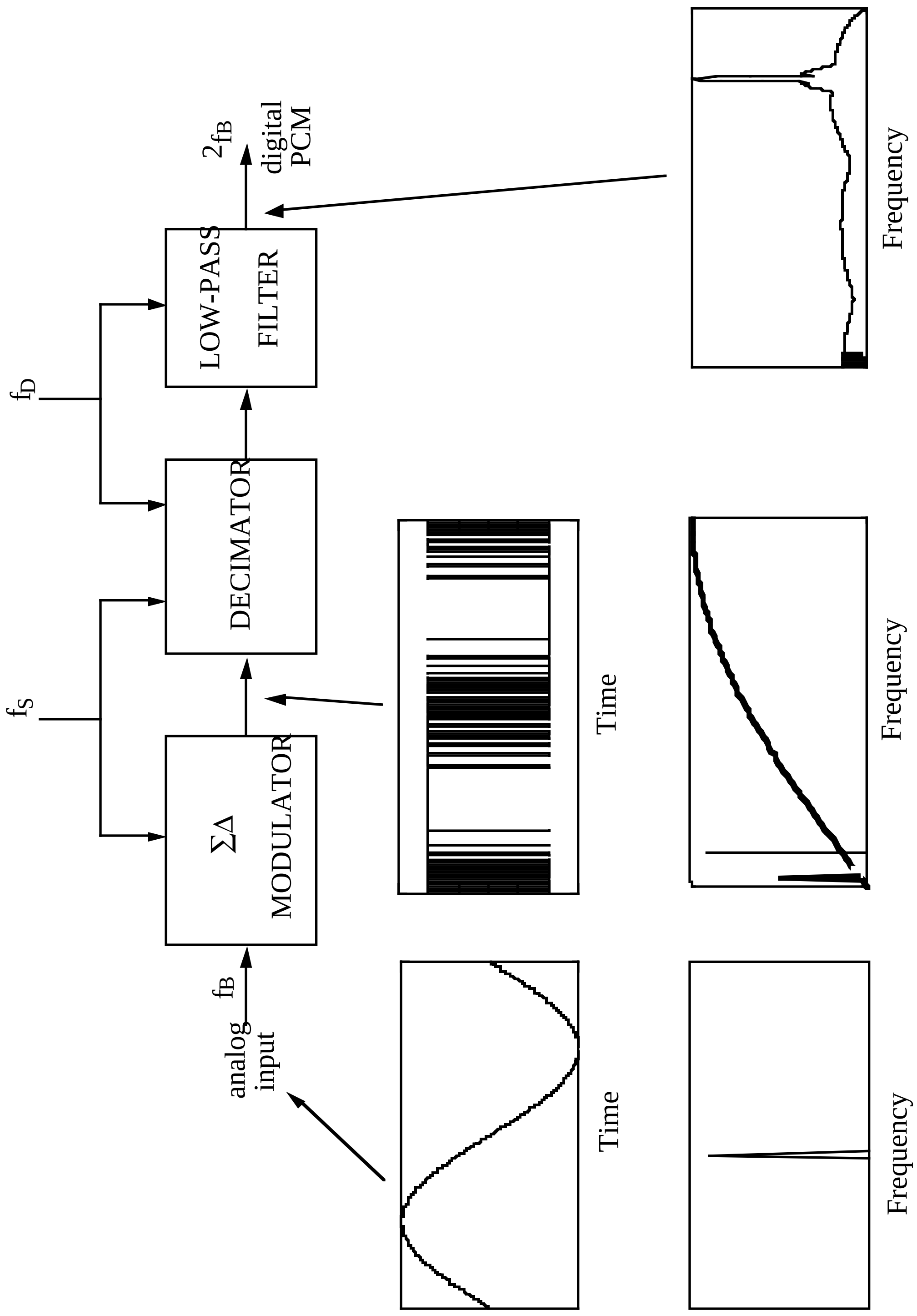
From the frequency response of above diagram, the signal-to-noise ratio (SNR)

$$\mathrm{SNR} = 10\log_{10} \frac{\text{signal}}{\sum_{f=0}^{f_B} \text{noise}(f)} \quad \text{(dB)}$$

and

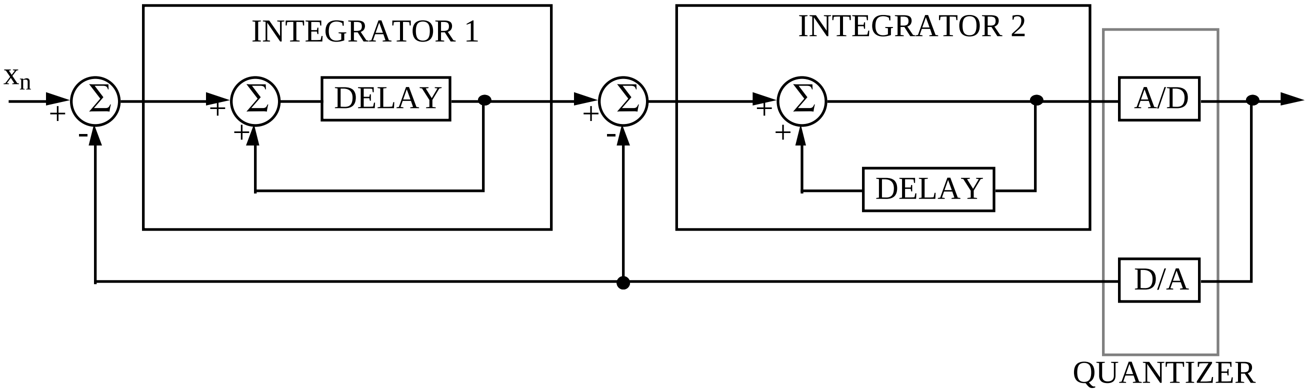
$$\text{Bit resolution (B)} \approx \frac{\mathrm{SNR(db)}}{6\mathrm{dB}}$$

System block in time domain and frequency domain



Second-Order ∑∆ Modulator

Second order ∑∆ modulator can be implemented by cascading two first order ∑∆ modulators.

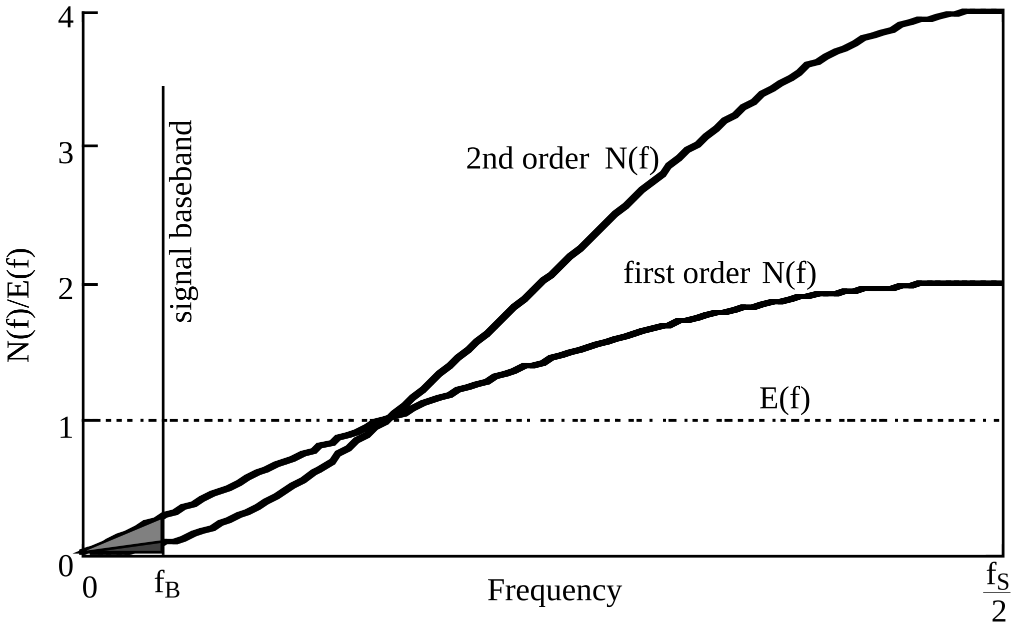


$$y_n = x_{n-1} + (e_n - 2e_{n-1} + e_{n-2})$$

The output of a second order ∑∆ modualtor y_n is the input signal delayed by one clock cycle x_{n-1}, plus the quantization noise difference $e_n - 2e_{n-1} + e_{n-2}$. The modulation noise spectrum density of $e_n - 2e_{n-1} + e_{n-2}$ is

$$N(f) = E(f)\left|1 - z^{-1}\right|^2 = E(f)\left|1 - e^{-j\omega\tau}\right|^2 = 4E(f)\sin^2\left(\frac{\omega\tau}{2}\right)$$

Noise Spectrum



Second-Order ∑∆ Modulator- Cond’d

The noise power in the signal band is

$$n_o = e_{rms}\frac{\pi^2}{\sqrt{5}}\ M^{-5/2} = \sqrt{\frac{\Delta^2}{12}}\frac{\pi^2}{\sqrt{5}}\ M^{-5/2} = \frac{\Delta\pi}{2\sqrt{15}}(M)^{-5/2},\ f_s >> f_o$$

Each doubling of the oversampling ratio reduces the modulation noise by 15 dB and increase the resolution by 2.5 bits.

Higher-Order Σ−∆ Modulators

Let L = the number of loops. The spectral density of the modulation can be written as

$$|N_L(f)| = e_{rms}\sqrt{2\tau}\left[2\sin\left(\frac{\omega\tau}{2}\right)\right]^L$$

The rms noise in the signal band is given approximately by

$$n_o \approx e_{rms}\frac{\pi^L}{\sqrt{2L+1}}(2f_B\tau)^{L+0.5}$$

This noise falls 3(2L+1) dB for every doubling of the sampling rate providing L+0.5 extra bits.

Decimation Filter

A filter function of $\left[\frac{\text{sinc}(\pi f N\tau)}{\text{sinc}(\pi f\tau)}\right]^{L+1}$ is close to being optimum for decimating the signal from an Lth-order ∆−Σ modulator.

Stability

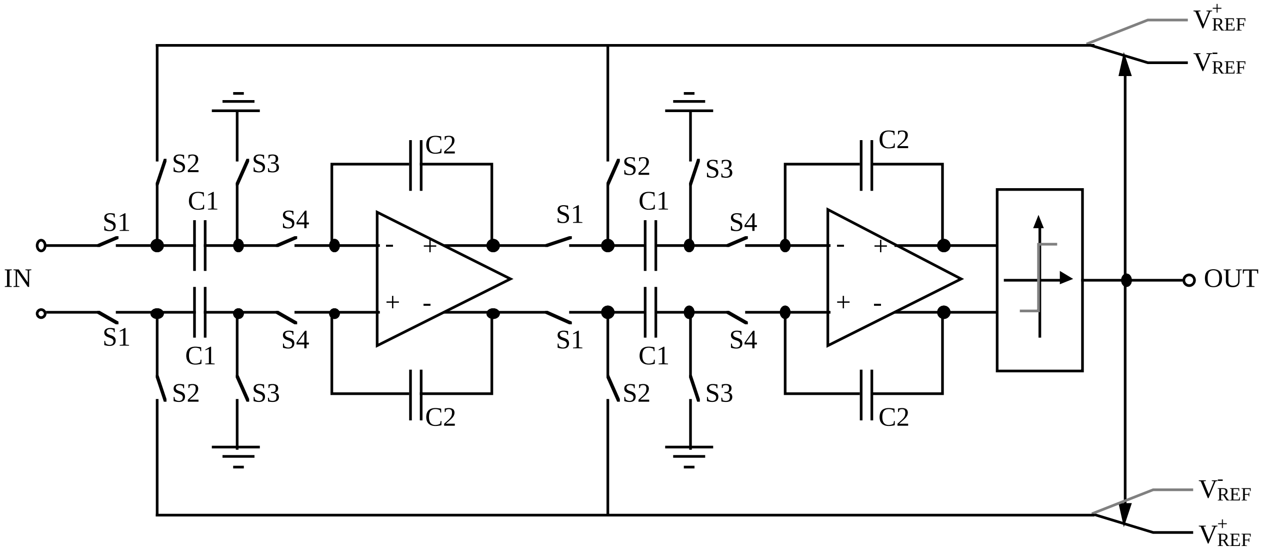
For orders greater than 2, the loop can become unstable. Loop configuration must be used that provide stability for order greater than two.

The modulation noise spectral density of a second-order, 1-bit ΔΣ modulator is given as

$$|N(f)| = \frac{4\Delta}{\sqrt{12}}\sqrt{\frac{2}{fs}}\ \sin^2\left(\frac{\omega t}{4}\right)$$

where Δ is the signal level out of the 1-bit quantizer and $f_S = (1/\tau)$ = the sampling frequency and is 10MHz. Find the signal bandwidth, fB, in Hz if the modulator is to be used in an 18 bit oversampled ADC. Be sure to state any assumption you use in working this problem.

Circuit Implementation of A Second Order ∑∆ Modulator



Fully differential, switched-capacitor integrators can reduce charge injection effect.

Circuit Tolerance of a Second Order ∑∆ Modulator

1. 20% variation of C1/C2 has only a minor impact on performance.
2. The Op Amp gain should be comparable to the oversampling ratio.
3. The unity-gain bandwidth of Op Amp should be at least an order of magnitude greater than the sampling rate.

SOURCES OF ERRORS IN ΣΔ A/D CONVERTERS

1. Quantization in time and amplitude
    - Jitter and hysteresis
2. Linear Errors
    - Gain and delay
3. Nonlinear Errors
    - Harmonic distortion
    - Thermal noise

Comparison of the Various Examples Discussed

Type of Converter	No. of Cycles/ Conversion	No. of Comparators	Dependent on Passive Components	Resolution	Speed	INL/DNL (LSB's)	Area	Power (mW)
Flash	1	2^{N-1}	Yes	Low	High	N/A	Largest	Largest
Two-Step Flash	2	31	Yes	10 bits	5Ms/s	±3/±0.6	54k mils^2	350
Pipeline	1 after initial delay	3	Yes	13 bits	250ks/s	±1.5/±0.5	3600 mils^2	15
Oversampling	64	3	Yes	16 bits	24kHz	91dB	75.3k mils^2	110

X.11 -FUNDAMENTAL LIMITS OF SAMPLING A/D CONVERTERS

kT/C Noise

Assume that the ON resistance of a switch is R and the sampling capacitor is C and that the time to charge the capacitor fully is

$$T = \frac{1}{f_c} \approx 10RC \qquad (1)$$

Set the value of the LSB $\left(= \frac{V_{ref}}{2^N}\right)$ equal to kT/C noise of the switch,

$$\frac{V_{ref}}{2^N} = \sqrt{\frac{kT}{C}} \qquad (2)$$

Solve for C of (1) and substitute into (2) to get

$$\left(\frac{V_{ref}}{2^N}\right)^2 = 10kTRf_c \Rightarrow \quad 2^N\sqrt{f_c} = \frac{V_{ref}}{\sqrt{10kRT}} \qquad (3)$$

Taking the log of both sides of (3) gives

$$N = -1.67 \log(f_c) + 3.3 \log(V_{ref}) - 1.67 \log(10kRT)$$

or

$$\boxed{N = 32.2 + 3.33 \log(V_{ref}) - 1.67 \log(Rf_c)}$$

(At room temperature)

kT/C Noise

Comparison of high-performance, monolithic A/D converters in terms of resolution versus sampling frequency with fundamental limits due to kT/C noise superimposed.

Fundamental Limits of Sampling A/D Converters - Continued

Maximum Sample Rate

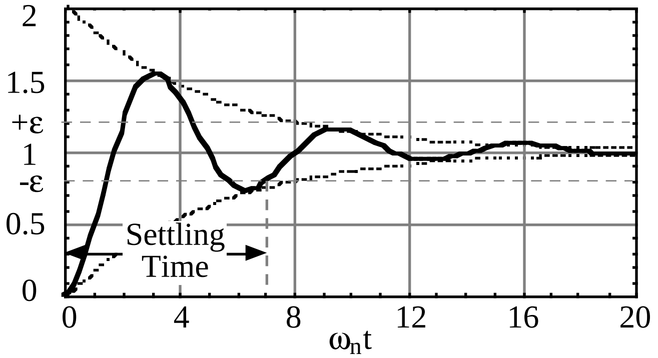
Assume that the maximum sample rate is determined by the time required for the amplifiers and/or sample-hold circuits to settle with the desired accuracy for high resolution. Further assume that the dynamics of these circuits can be modeled by a second-order system with a transfer function of

$$\frac{A(s)}{A(0)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

If $\omega_n \approx GB$ of the circuit and if the system is underdamped, then the step response is given as

$$\frac{v_O(t)}{A(0)} = 1 - \left[\frac{e^{-\zeta GBt}}{\sqrt{1-\zeta^2}}\right] \sin\left(\sqrt{1-\zeta^2}\ GB\cdot t + \phi\right)$$

This response looks like the following,



If we define the error (±ε) in v_O settling to A(0) as the multiplier of the sinusoid, then an expression for the settling time can be derived as

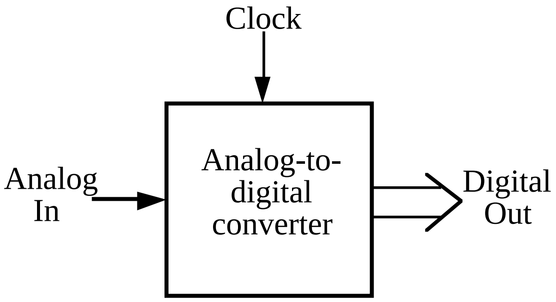
$$t_s = \frac{1}{2\pi\zeta GB}\ \ln\left(\frac{e^{-\zeta GBt}}{\sqrt{1-\zeta^2}}\right) \Rightarrow f_{sample} = \frac{1}{t_s} = \frac{2\pi\zeta GB}{\ln\left(\frac{1}{\varepsilon\sqrt{1-\zeta^2}}\right)}$$

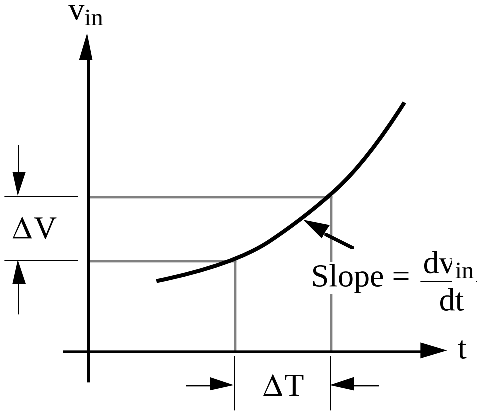
For reasonable values of ζ, f_{sample} can be approximated as

$$\boxed{f_{sample} \approx \frac{\pi GB}{10} = \frac{GB}{3}}$$

Aperature Uncertainty (Jitter)

A problem in all clocked or sampled A/D converters.





$$\Delta V = \text{slope x } \Delta T = \frac{dv_{in}}{dt}\ \Delta T$$

$$\Delta T = \text{Aperature uncertainty} = \frac{\Delta V}{\frac{dV_{in}}{dt}} = \frac{V_{ref}/2^N}{dv_{in}/dt}$$

Assume that $v_{in}(t) = V_p \sin \omega t$

$$\left|\frac{dv_{in}}{dt}\right|_{max} = \omega V_p$$

$$\Delta T = \frac{V_{ref}}{2^N} \text{ x } \frac{1}{\omega V_p} \approx \frac{V_{ref}}{2^N \omega V_{ref}} = \frac{1}{2^N \omega}$$

Therefore, $\Delta T = \frac{1}{2\pi f 2^N} = \frac{1}{\pi f 2^{N+1}}$

Suppose f = 100kHz and N = 8, $\Delta T = \frac{1}{200\pi K x 2^9} = 6.22\text{ns}$

Clock accuracy = $\frac{6.22\text{ns}}{10{,}000\text{ns}} = 0.06\% = \frac{622\text{ppm}}{?}$

X.12 - SUMMARY OF A/D CONVERTERS

Typical Performance Characteristics

A/D Architecture	Typical Performance Characteristics
Serial $\frac{1}{f_c} = 2^N T$	1-100 conversions/sec., 12-14 bit accuracy, requires no element-matching, a stable voltage reference is necessary
Successive Approximation $\frac{1}{f_c} \approx NT$	10,000-100,000 conversions/sec., 8-10 bits of untrimmed or uncalibrated accuracy, 12-14 bits of trimmed or calibrated accuracy
High Speed $T < \frac{1}{f_c} < NT$	1 to 40 megaconversions/sec., 7-9 bits of accuracy, 10-12 bits of accuracy with error correction and other techniques
Oversampling $\frac{1}{f_c} << T$	8,000-600,000 conversions/sec., 12-16 bits accuracy, requires linear integrators but no precision passive components, minimizes noise and offsets

Conclusions

- The best A/D converter depends upon the application
- Both resolution and speed are ultimately limited by the accuracy of the process
- High resolution A/D's will be more oriented toward "signal averaging" type converters, particularly with shorter channel lengths