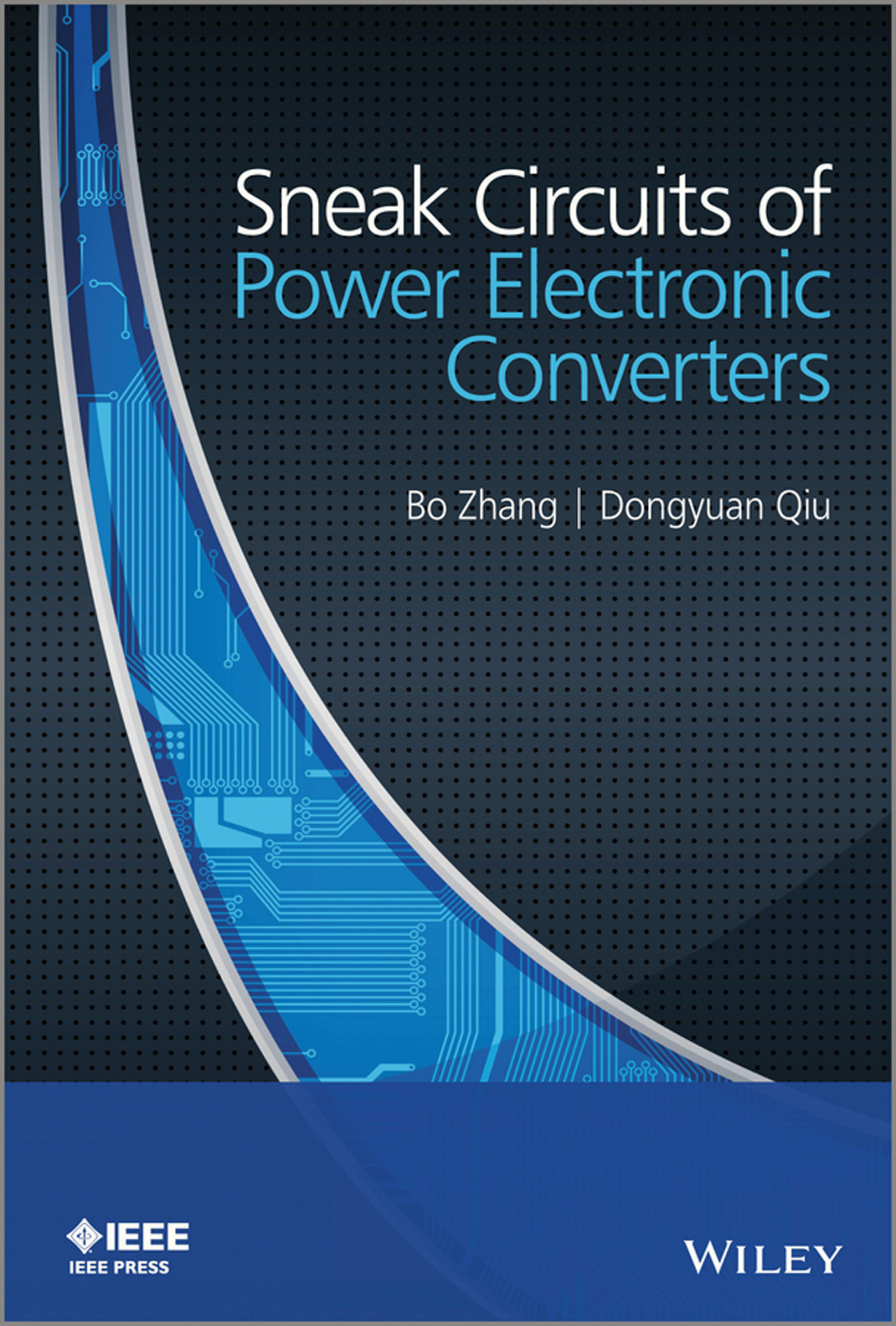
Sneak Circuits of
Power Electronic
Converters
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South China University of Technology, P. R. China

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Contents

Part III ELIMINATION AND APPLICATION OF SNEAK CIRCUITS

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Preface

The so-called 'Sneak Circuit' is defined as an unexpected path or operational status in an electric or electronic circuit due to the limitation or oversight in design. Such sneak circuit can be triggered to operate under certain conditions. Whenever the unwanted or unintended operation corresponding to the sneak circuit emerges, the desired functions are likely to be degraded or inhibited. Undoubtedly, the phenomenon of sneak circuit also exists in power electronic converters, which are artificially designed to convert electric energy. In fact, sneak circuits in power electronic converters are not uncommon. For example, the *discontinuous-conduction mode* (DCM) in DC-DC converters is a type of sneak circuit corresponding to its *continuous-conduction mode* (CCM) counterpart, and vice versa.

However, the phenomenon of sneak circuit was not well-known in the past, largely due to unawareness of their conception in power electronics. In recent decades, power electronics has undergone intense development in many areas of technology. Better functionality, safety, and reliability of the power electronic system have become increasingly important in the present application of power electronics. In view of catastrophic results, which might be caused by the operation of a sneak circuit under certain conditions, it is necessary for power electronic engineers to understand thoroughly the sneak circuit in power electronic converters designed under all possible practical conditions.

The authors' understanding of sneak circuits in power electronic converters came from an accidental experiment on the basic step-down RSC (resonant switched capacitor) converter early in 2004. In that experiment, the control strategy for switches was not changed and only some parameters (i.e., the switching frequency, the load, and the input voltage) were adjusted. It was surprising to observe that the converter changed its status from four normal operating stages to six operating stages, and the adjusting process was completely reversible. Such an observation implied that two unexpected or undersigned operating stages had appeared.

Moreover, when the converter worked in six operating stages, we observed obvious hazards of sneak circuit operation in a basic step-down RSC converter, including decrease in the output voltage and increase in the stress of the inductor current and switched capacitor voltage. Apparently, the six operating stages we observed were an example of a sneak circuit in a basic step-down RSC converter. It could be considered

as the starting point of our study on sneak circuits in power electronic converters, and this book is a periodic summary of our research achievements in this field over the past ten years.

We begin in Chapter 1 as an introduction of sneak circuit, outlining moves onto power electronic converters on sneak circuit phenomena, and an overview of definition, history, and analysis methods for sneak circuits. The following chapters are divided into three parts. The first part, consisting of Chapters 2 to 5, mainly describes sneak circuit phenomena in some typical power electronic converters. In Chapter 2, we present sneak circuit phenomena in families of RSC converters, and derive their expression of output voltage and operational conditions as they were first discovered. In Chapter 3, based on the summary and analysis of CCM and DCM of Buck, Boost, Buck-Boost, Cúk, Sepic, and Zeta DC-DC converters, we argue that DCM can be regarded as a sneak circuit in terms of the definition of these phenomena. In this way, the in-depth understanding on the physical mechanism of the DCM is presented from the viewpoint of a sneak circuit. In Chapter 4, we discuss some sneak circuit phenomena in soft-switching converters, specifically taking the full-bridge ZVS PWM converter, the Buck ZVS multi-resonant converter, and the Buck ZVT PWM converter as examples. The purpose of this chapter is to illustrate that sneak circuit phenomena are more complex and abundant in soft-switching converters due to the existence of the resonant tank. The sneak circuit here must be eliminated, otherwise it will give rise to unpredicted effects on the converters. In Chapter 5, we consider two novel power electronic converters, that is, the Z-source inverter and the synchronous rectifier DC-DC converter. The detailed investigations on these two converters further demonstrate that sneak circuit phenomena inevitably exist in a large number of power electronic converters under certain conditions.

The second part includes Chapters 6 and 7, where we propose some analysis methods, which are used to investigate sneak circuit phenomena in power electronic converters. In Chapter 6, we use graph theory to study sneak circuit paths. Firstly, the adjacency matrix, connection matrix, and switching Boolean matrix are respectively employed to find all circuit paths in the converters. Then, we identify the sneak circuit paths according to the operating principle of power electronic converters. In Chapter 7, we suggest a systematic method for discovering the sneak circuit phenomena in power electronic converters, which is essentially a method of mode analysis of the sneak circuit and can be taken as the complement of Chapter 6.

Chapters 8 and 9 are the last part of this book. In these two chapters, we focus on the guidelines concerning elimination and application of sneak circuits in power electronic converters. In order to eliminate the sneak circuit in power electronic converters, we propose two methods in Chapter 8. One method is to restrict the parameter variation of the converter so that the sneak circuit cannot become active, whereas the other method completely cuts off the circuit path corresponding to the sneak circuit. Since the aim of understanding the sneak circuit is to fully utilize it, this issue is addressed in Chapter 9, where we demonstrate the utilization of a sneak circuit to achieve performance improvement, topological reconfiguration, new function, and fault diagnosis of power electronic converters with specific examples.

We hope this book will help researchers and engineers in power electronics and other related industrial fields to understand that sneak circuits definitely exist in power electronic systems, and further guide them to carry out analysis on the sneak circuit to improve the reliability of power electronic systems at the design stage.

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South China University of Technology
Guangzhou in China
October 2013

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We would also like to thank our former graduate students, Chunfang Zheng, Jianyuan Li, Wenjuan Tu, Lili Qu, Yi Mei, Li Zhang, Yu Dai, Genyun Yi, and Bin Liu, not only for their wonderful work in verifying our conjecture on sneak circuits in power electronic converters, but also for their inquiring minds, which have prompted us to pay attention to many important but easily overlooked problems.

Last, but by no means least, we wish to express our sincere appreciation to the editors of this book, Clarissa Lim and Mingxin Hou, and the staff of John Wiley & Sons for their professional and enthusiastic support of this project.

1

Sneak Circuit and Power Electronic Systems

1.1 Reliability of Power Electronic Systems

Power electronics has already found an important place in modern technology, because it helps to meet the demands of energy, particularly in electrical form and efficient use of electricity. Application of power electronics is expanding exponentially in many areas, from computer power supply to industrial motor control, transportation, energy storage, electric power transmission, and distribution. Nowadays, over 70% of electrical loads are supplied through power electronic systems in the United States and Europe, and almost all electrical and electro-mechanical equipment contains power electronic circuits and/or systems. In the next 5 years, renewable energy systems (wind and solar, etc.) will show a sharp increase throughout the world, the needs of power electronic systems grow rapidly as a result. Therefore, the reliability of these systems should be a concern in its fundamental place in energy conversion and management.

A basic concept in reliability engineering is that part failure may cause system failure, and preventing part failure is effective in preventing system failure. Likewise, in power electronic systems, it is found that many system failures do result from component failures. The main factor affecting reliability at part level is the electrical and thermal stress of a component, such as device voltage, current, temperature, or temperature rise due to power dissipation, since the failure rate of the components will double with a 10°C increase in temperature. In order to achieve good reliability, system designers always apply effective reliability assurance techniques, for example, component derating, and thermal and electrical stress analysis, to manage the levels of component voltage, current, and power dissipation, and keep them well within rating limits.

However, not all system failures are caused by component failure. In some situations, no part has failed, yet the system performs improperly or initiates an

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undesired function. For example, an inadvertent launching of the Redstone rocket on 21 November 1961 resulted from an undetected design error in the electrical path. Such events may cause hazardous and even tragic consequences, which have been proven by many serious accidents in aerospace, navy, nuclear, and military industries in the last century.

A significant cause of such unintended events is named "sneak circuit," which is the unexpected electrical path or logic flow that can produce an undesired result under certain conditions [1]. Opposed to component failure, a sneak circuit happens without any physical failure in the system, causing an undesired effect in that system, although all parts are working within design specifications.

It is well established in reliability engineering that the more parts there are in a system, the more likely it is to fail. Complexity is considered as the main factor that causes sneak circuit, because it is difficult for the designers to have a complete view of the detailed interrelationship between components and functions in a complex system. As a consequence, sneak circuits may exist in a complex system, and produce undesired results or even prevent intended functions from occurring under certain conditions.

Nowadays, power electronic systems are being designed and manufactured with increased complexity to satisfy specific functions. Similar to other systems, the sneak circuit will affect the reliability of the power electronic system as well as part failure. Therefore, sneak circuit situations in different kinds of power electronic converters should be investigated and identified, which will have a positive impact on the reliability of the power electronic system.

1.2 Sneak Circuit

1.2.1 Definition of Sneak Circuit

A sneak circuit is a designed-in current path or signal flow within a system, which inhibits desired functions or causes unwanted functions to occur without a component having failed. Sneak circuits are not the result of component failures, electrostatic, electromagnetic or leakage factors, marginal parametric factors or slightly out-of-tolerance conditions. They are present but not always active conditions inadvertently designed into the system, coded into the software program, or triggered by human error [2].

Based on the definition of a sneak circuit, the sneak conditions may consist of hardware, software, operator actions, or any combinations of these elements. Thus, sneak circuits are a family of design problems, which includes four categories as follows [1]:

1. *Sneak path*:
   unexpected path along which current, energy, or logic sequence flows by an unintended route, resulting in unwanted functions or inhibiting a desired function.

2. *Sneak timing*:
   events occurring in an unexpected or conflicting hardware or logic sequence, which may cause or prevent activation or inhibition of a function at an unexpected time.
3. *Sneak indication*:
   ambiguous or false display of system operating status that may cause the system or operator to take an undesired action.
4. *Sneak label*:
   incorrect or imprecise nomenclature or instructions on system inputs, controls, displays, or buses, which may cause the operator to apply an incorrect stimulus to the system.

1.2.2 Examples of Sneak Circuits

Since the 1960s, many accidents in aerospace, navy, nuclear, military, and modern weapon systems, which caused hazardous and even tragic outcomes, have been found to be the result of sneak circuits. In addition, sneak circuits have also existed in household wiring and automobile electrical systems, which did not perform an intended function or initiated an undesired function. Some examples will be introduced in the following section to explain different types of sneak circuits.

1.2.2.1 Automobile Electrical System

Figure 1.1 shows an example of sneak path found in a mid-1960s automobile electrical circuit [1]. The circuitry design meets the electrical system specification, for example, when the ignition switch is on, power is supplied from the battery to the radio, and if the brake switch is closed, the brake lights receive power from the battery. Also, if the hazard switch (pedal) is on and the ignition switch is off, power will be supplied from the battery to the flasher module causing the brake lights to flash. In summary, all of the design intent had been satisfied.

However, a problem with this circuit design remains hidden. Assuming that the ignition switch is set to "off," the radio is switched to "on" and the hazard switch is enabled, if the brake pedal is depressed, power will be applied to turn the radio on with each flash of the brake lights. The cause of this unintended behavior, a sneak path, is highlighted in Figure 1.1. It is the brake switch (pedal) that provides a current path to the radio and places the radio parallel with the brake lights. In this case, the consequences of the sneak path are not severe; children left in the car by their parents could listen to the radio slowly draining the battery.

1.2.2.2 Household Wiring System

A popular household wiring system in Western European is shown in Figure 1.2a, which is a three-phase 127 V/50 Hz system with an approximately balanced load and

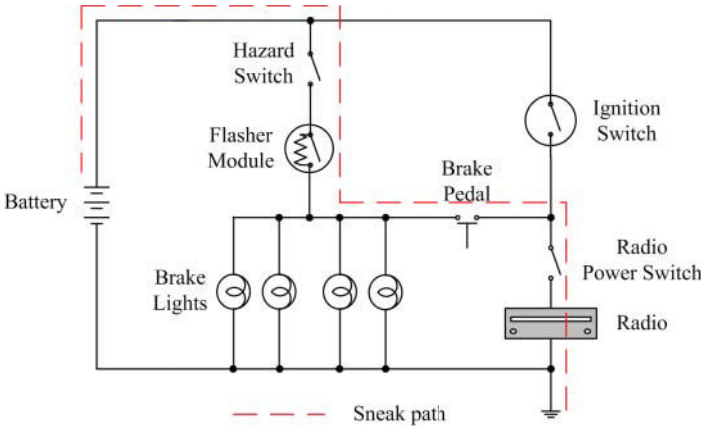

Figure 1.1 An automobile electrical system [1]

no neutral return wire. All devices or appliances are connected between lines and operate at 220 V [3]. If the fuse of phase B blows, a sneak path will appear as in Figure 1.2b, leaving devices in line A–B in series with those in line B–C across 220 V line A–C. Then the lamps on circuit A–B will dim if lamps or bath heater on circuit B–C is on and refrigerator operates erratically when the bath heater is on. Though all devices on circuit A–C work normally as before, phase B has no load, and phases A and C have overload, which will cause the distribution transformer to overheat.

1.2.2.3 A Sudden Acceleration Incident

In one kind of US police van, shown in Figure 1.3, the code 3 control switch activates a roof-mounted blue-light bar and causes brake lights and backup lights to pulse alternately at about 2.4 Hz. Diode (D) is used to prevent brake pedal switch from activating the blue-light bar via an alternating flasher relay. On 4 December 1998, an apparent police van shift lock failure combined with suspected misapplication of the accelerator rather than the brake resulted in sudden acceleration, the death of two pedestrians, and injury of nine [4]. It is found that closing code 3 control switch provides a pulsing path (sneak path) through flasher relay and diode D to disengage the shift lock, allowing the vehicle operator to shift into gear while applying the accelerator rather than the brake.

1.2.2.4 Redstone Rocket Launch Failure

Figure 1.4a shows the Mercury booster firing circuit of the Redstone rocket [3]. In order to satisfy the launching requirements, the motor is ignited by the on-board fire switch, annunciated by the ignition indicator light through an umbilicus, and the motor

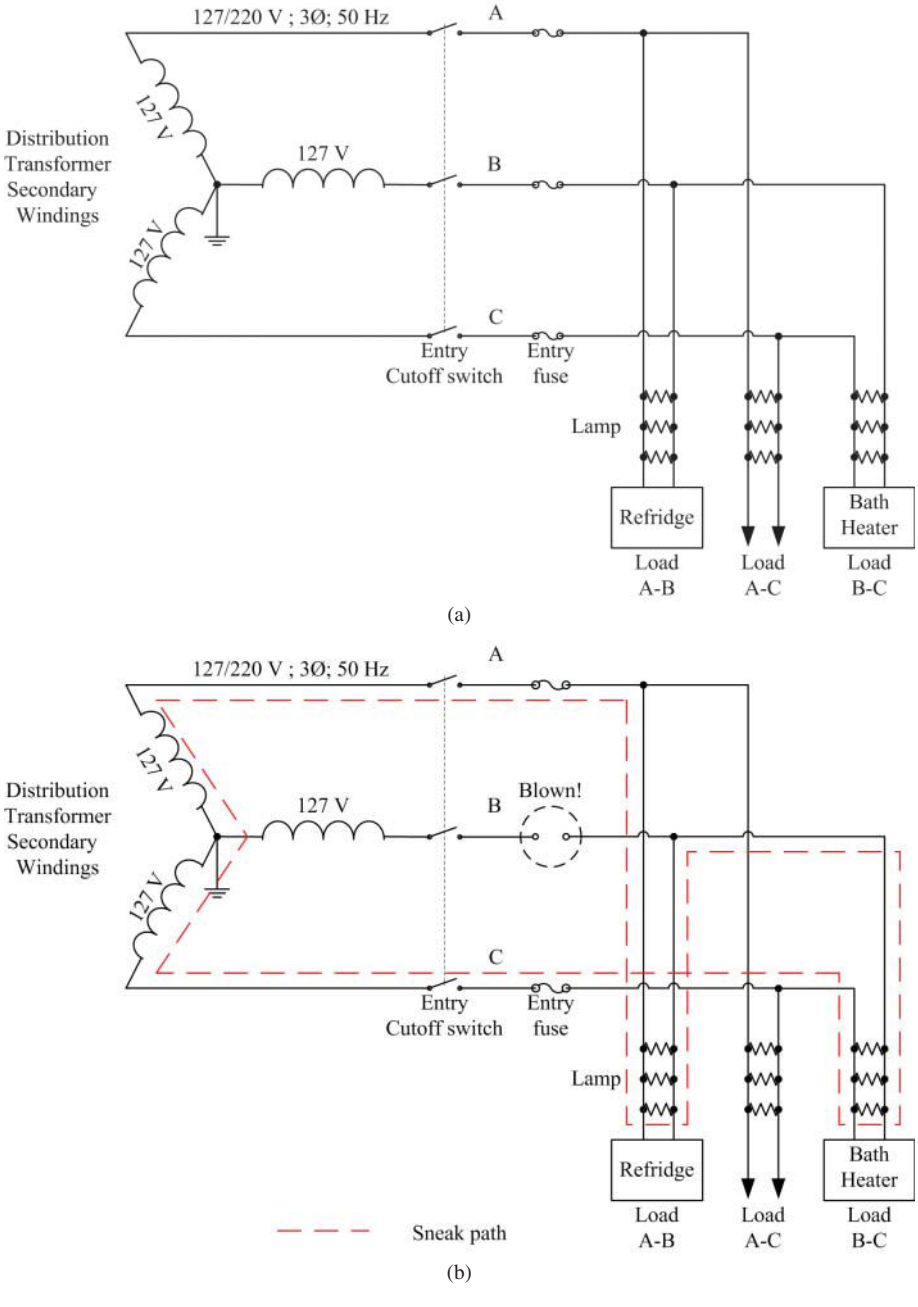

Figure 1.2 A household wiring system [3]: (a) normal operating state; and (b) state with broken fuse

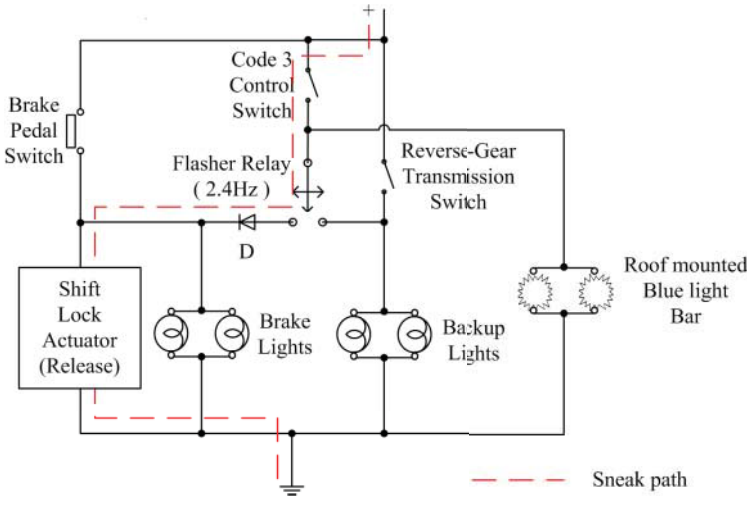

Figure 1.3 Part of control circuit in a police van [3]

ignition coil latches to the on-board power supply (28 V). The on-board motor cutoff coil is energized by an on-board abort switch and latched to the on-board power supply. The abort prior to liftoff is enabled by the pad abort switch and the umbilical connector and tail ground connector are separate for liftoff breakaway. The Redstone rocket had launched successfully 60 times until 21 November 1961. On that day, the Redstone motor fired and began liftoff. After "flight" of a few inches, the motor cut off and the vehicle settled back on the pad. The Mercury capsule jettisoned and impacted 1200 ft away. The rocket was not allowed to be approached until the batteries had been drained down and liquid oxygen evaporated. Fortunately, damage was slight; booster and Mercury capsule were reused later.

This launch failure occurred due to the tail ground connector breaking away 29 ms prior to umbilicus separation, which meant that it was an incident caused by sneak timing. The tail ground connector was disconnected earlier than expected, leaving a current path, as shown in Figure 1.4b, for excitation of the motor cutoff coil through the ignition indicator light and suppressor diode, then the rocket landed back onto its launch pad after lifting just a few inches.

1.2.2.5 Three Mile Island Accident

On 28 March 1979, at the Three Mile Island (TIM) nuclear power plant in the USA, a relief valve solenoid excitation was interpreted as valve position, which resulted in destroying the TIM-2 reactor.

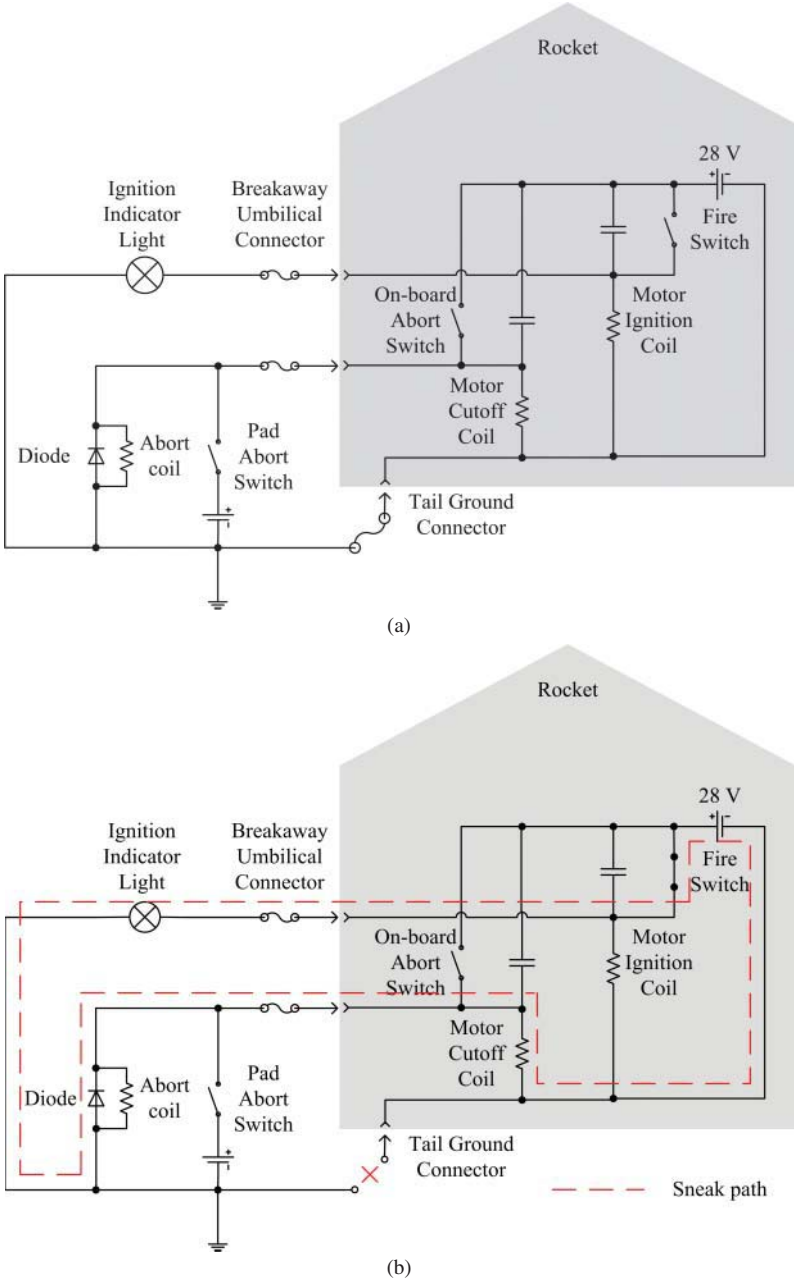

Figure 1.4 The Redstone booster firing circuit [3]; (a) schematics; and (b) sneak circuit path

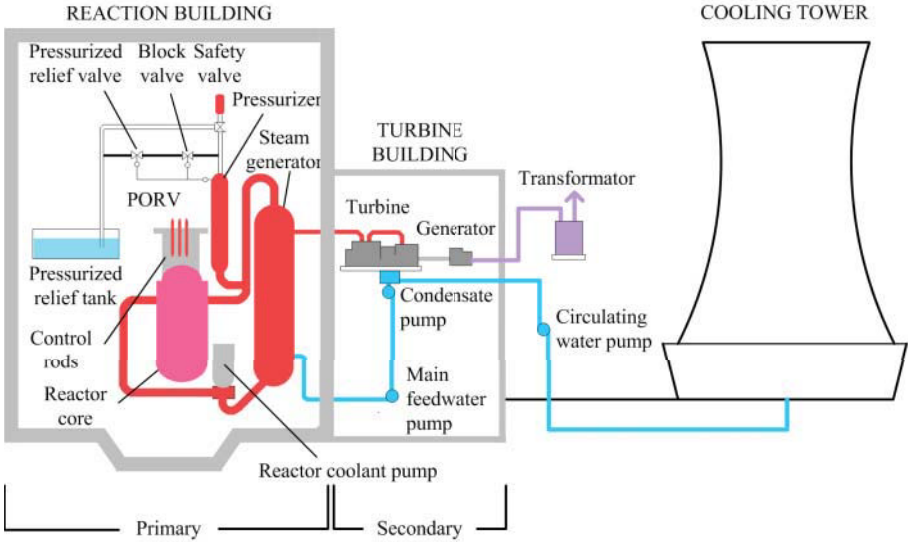

Figure 1.5 The #2 reactor of the Three Mile Island nuclear power plant [5]. (Source: Reproduced by permission of World Nuclear Association.)

The structure of the TIM-2 reactor is shown in Figure 1.5. The accident involved a relatively minor malfunction in the secondary cooling circuit, which caused the temperature in the primary coolant to rise. This in turn caused the reactor to shut down automatically. Within seconds of shutdown, the pilot-operated relief valve (PORV) on the reactor cooling system opened as intended, and at about 10 seconds later it should have closed. But it failed to close and the instrumentation did not indicate the valve's actual position. The operators believed that the relief valve had shut because instruments showed that a "close" signal was sent to the valve. As the valve remained open, so much of the primary coolant drained away that the residual decay heat in the reactor core was not removed and part of the core was melted in the #2 reactor. The core suffered severe damage as a result. Sneak indication has been proved to be the root cause of this accident [6].

1.2.2.6 Morgantown Rapid Transit System

The Morgantown Personal Rapid Transit (PRT) system is a one-of-a-kind people mover system in Morgantown, West Virginia, USA. This system entered operation in 1975 and has operated continually with 98% reliability for over 40 years. Even in such a highly reliable system, a sneak label problem was found [6]. As shown in Figure 1.6, a ganged switch S1, which connected both battery and critical system to the bus, was only labeled as "Battery Disconnect." When the operator disconnected the battery from the bus by turning off switch S1, the critical system was de-energized at the same time.

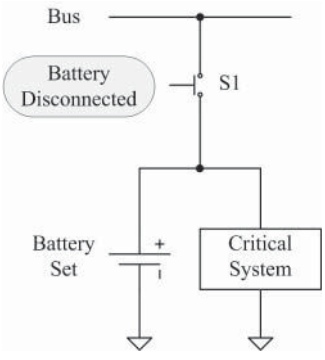

Figure 1.6 An example of a sneak label

1.2.3 Basic Causes of Sneak Circuit

As mentioned above, a sneak circuit is an unintended system path (e.g., wiring, tubing, software interfaces, operator actions, instrumentation, mechanical interlocks) or a latent condition (e.g., timing incompatibility), which is inadvertently introduced into the system. The principle causes of sneak circuits are system complexity, system changes, and user operations [1]:

1. *System complexity*:
   A complex hardware or software system normally requires numerous human interfaces between subsystems that may obscure intended functions or produce unintended functions. Under typical conditions of system design, it is difficult to ensure the understanding of subsystem interactions so completely that no possible variation in the flow of energy or logic, or in the actions of system operators, can fail to be noticed.
2. *System changes*:
   The effects of even minor wiring or software changes to subsystems may be undesired system operations. Because of subsystem interaction, a "fix" or corrective action that seems only minor and of local significance may produce changes in system functions that could not reasonably have been anticipated at the design stage.
3. *User operations*:
   A system that is relatively sneak-free can avoid desired functions, or generate undesired functions if the user employs improper operating methods or procedures. The cause could be simple human error on the part of the operator or inaccurate information supplied to that operator, for example, by a false indicator display or by an incorrectly labeled control.

With respect to all of these types of causes, complexity is the most common factor that will cause the sneak circuit. However, even a simple system may have sneak

circuits as well as the complex one. When systems become more complex, the probability of overlooking potentially undesirable conditions or creating sneak circuits is increased proportionately.

1.3 Sneak Circuit Analysis

1.3.1 Definition of Sneak Circuit Analysis

Sneak circuit analysis (SCA) is a generic term for a group of safety analytical techniques employed to methodically identify sneak circuits in systems, which can lead to anomalous behavior of the system [1, 7]. As described in the last section, a sneak circuit can be caused by inadvertent activation of signals, or the inhibition of signals when they are required to be activated. It can also be caused by the operator controlling the system inappropriately, or wrong information set by the system, such as incorrectly labeled controls or indicators. Therefore, SCA does not look specifically at the effects of component failures, but rather is concerned with the potential effects of latent path or logic flow that may exist in the hardware or software, in operator actions, or in some combination of these elements.

1.3.2 History of Sneak Circuit Analysis

In the past, sneak circuits were often discovered after the unintended effect had been observed in the actual system operation. Detection at this stage in the life cycle not only results in exposing the possibly serious operational effects of the sneak circuit, but may also require a significant expenditure of time and money to correct the problem and to retrofit the existing system. For these reasons, SCA should be developed to assist in the detection of sneak circuit early in system development.

Boeing were the first to develop SCA in the late 1960s, when they were commissioned by the National Aeronautics and Space Administration (NASA) to work on the Apollo and Skylab systems, in order to identify the designed-in conditions that could inhibit desired system functions or lead to catastrophic or otherwise financially costly incidents, such as the Redstone rocket launch failure. At that time, SCA was applied to purely electric circuits, which consisted mainly of discrete components such as relays, resistors, diodes, and vacuum tubes, and so on. Later, SCA was developed further by Boeing to cover computer software and complex designs that integrate hardware and software.

A company named Independent Design Analyses (IDA) has further developed a SCA technique since 1994, and used it to analyze Programmable Logic Devices (PLDs), Complex Programmable Logic Devices (CPLDs), and Application Specific Integrated Circuits (ASICs), and also applied it to software such as Sneak Software Analysis (SSWA). In 1997, the European Space Agency (ESA) published a procedure for implementing SCA, which specifically covered the application of SCA to both

hardware and software. It not only described the basic SCA procedure but also included a process which used the application of "clues" directly to components, to ensure that good design practices had been used throughout the system [8].

1.3.3 Methods of Sneak Circuit Analysis

SCA has been used extensively over the last 50 years as a safety analysis technique to verify the functionality of safety critical systems, and to remove any sneak paths that may have been inadvertently designed into the system. It has been used in various applications of differing complexity and make-up, from early electric circuits involving just discrete components, through analysis of software, to systems combining both software and complex integrated circuits. Among the currently available SCA methods, sneak path analysis, digital SCA, and software sneak path analysis have proved to be particularly useful [1].

1. *Sneak path analysis*:
   Sneak path analysis is a methodical evaluation of all possible electrical paths in a hardware system, which is used primarily to detect sneak circuits in electrical circuits.
   The sneak path analysis process consists of the following steps:
   (i) design elements, such as switches, diodes, and resistors, are converted into data inputs;
   (ii) computer runs path finding programs to identify all possible continuities for each operating mode of interest; and
   (iii) the program outputs are used to employ recognition of topological or functional patterns, with the aid of a rule base (i.e., sneak clues) derived from previous sneak circuit analyses.
2. *Digital sneak circuit analysis*:
   Digital SCA is performed on networks composed of digital functional modules, in which the elements of interest include logic gates, registers, flip-flops, and timers. Unlike sneak path analysis, which seeks to identify undesired paths in hard-wired circuits, digital SCA is concerned primarily with logic errors and inconsistencies, timing races, improper operating modes, and unintended switching patterns.
3. *Software sneak path analysis*:
   Software sneak path analysis examines computer program logic flows through an adaptation of the method used in sneak path analysis of hardware systems. Experience has shown that program flow diagrams containing sneak paths often exhibit similar characteristics.

SCA can be realized by the computer automatically, regardless of which SCA method is performed, and the requirement of collection, processing, and evaluation of detailed system design information is common [9]. The SCA results may be used

to support the activities of a variety of system functions, but its most important use is to aid in the improvement of design reliability prior to product manufacture and test.

1.3.4 Benefits of Sneak Circuit Analysis

SCA aims to identify the latent conditions within a system during the design process, thus SCA can benefit a system in the following ways [1].

1. *Detection of potentially serious system problems*:
   The major benefit of SCA results from the careful examination of a system for problems such as undesired and unintended current or logic paths, out-of-sequence events, false displays, and incorrect function labels. Identification of such anomalies is not the normal result of other analysis methods; generally, it is a unique output of SCA.
2. *Discovery of design oversights*:
   An SCA requires a detailed listing of components, connections, and timing sequences as well as current and signal flows, which gives a good chance of uncovering "design concerns" or possible design oversights. Examples of the types of concerns identified from an SCA, or from further investigation are part over-stressing, single failure point, unnecessary or unusual circuitry or components, lack of transient protection, and component misapplications.
3. *Discovery of documentation errors*:
   The detailed examination of system interfaces and circuitry required by SCA has, in many cases, uncovered drawing and documentation errors that might otherwise have escaped notice until a later stage of the development process.
4. *Reduction in system-change costs*:
   SCA is an analysis tool that can be used for hardware and software systems to identify latent paths, which will cause unwanted functions or inhibit desired functions, assuming all components and codes are functioning properly. Then a significant benefit of SCA is the prediction of these problems before they occur in test or operation. It is obvious that correction is more difficult and more time-consuming when physical changes to the system rather than modifications to drawings are required. Thus, the cost of modifications and redesign will be reduced if the problems are identified early in the development phase.
5. *Improvement to system reliability and safety*:
   The intent of the generally applied reliability and safety analysis is to identify system failures that will result from component failures. While such events certainly contribute a large share of a system's reliability problems, it is now clear that system failures can occur in the absence of part failures. Precluding such events through the use of SCA represents a real improvement in system reliability and safety.

6. *Reduction in testing and analysis requirements*:
   Dependence on extensive and time-consuming testing to detect sneak conditions adds to the cost of the development program and does not necessarily assure that such conditions will be identified. For example, a combination of events that can generate sneak circuits might not occur in a test routine; but a properly conducted SCA is specifically directed toward discovering such unusual conditions.
7. *Benefit to other analysis*:
   Applying SCA in the development phase can complement and facilitate other required analysis. As noted above in the discussion of design oversights, the detailed design review involved in SCA can identify misapplications, over-stressing, and similar problems. Equally important, some of the intermediate results of the SCA can materially assist in the performance of other reliability analysis.

Boeing has applied the SCA technology in over 200 projects for commercial, NASA, Department of Defense, and Boeing customers. In these projects, approaching 5000 sneak circuit problems have been identified and corrected, resulting in cost savings of hundreds of millions of dollars.

1.3.5 Relationship between Sneak Circuit Analysis and other Safety Techniques

The SCA technique differs from other systems analysis techniques in that it is based on identifying designed-in inadvertent modes of operation and is not based on the failed part. The relationship between SCA and other safety techniques are introduced briefly below [9–12].

Hazard and Operability analysis (HAZOP) is a safety technique conducted early in the developing cycle, which aims to identify potential safety hazards within a system caused by a parametric change in the flow of energy, whereas SCA looks for an undesired flow of energy in the form of a sneak path. HAZOP is undertaken using a different approach to SCA. It is performed by applying guide words, one at a time, that describe a non-idealistic behavior, to each of the flows (electrical signals) that are present in the system, in turn, to determine any adverse effects caused by that particular behavior. Guide words considered include both quantitative (e.g., less, more, none) and temporal aspects (e.g., early, late) applied to the flows in the system. SCA is a technique that complements HAZOP, since SCA looks for obscure interactions in the design of a system, whereas HAZOP investigates the effect of changes in the flow between functions in the system.

Functional Failure Analysis (FFA) is another safety technique, which considers the effects of a shortfall in the behavior of a function within the system, so it is performed

at functional level early in the design cycle, usually before the detailed design has been undertaken. FFA considers omission, commission, and invalid operation of the function to determine the possible effects and allow derived safety requirements to be generated to mitigate any potential safety impact. FFA would therefore be undertaken much earlier than SCA, since SCA is generally applied when a significant amount of design detail is available to evaluate, in order to identify sneak paths, as it is not possible to locate all sneak paths just by looking at the proposed functional hierarchy.

Failure Mode and Effect Analysis (FMEA) considers an aspect of system safety analysis that SCA does not cover, that is, it covers the consideration of failures of the system, through only one failure at a time. SCA is not concerned with failure mode analysis, so FMEA is a complementary technique that should be used in addition to SCA. There may be some overlap between these two techniques in what they highlight as problems, particularly from the design concern aspects output of SCA, some of which could lead to actual failures and hence will be caught by an FMEA.

In summary, SCA can be effectively blended with other safety techniques to identify design and fault related problems in a cost-effective manner. System reliability is improved by the combination of different safety techniques.

1.4 Power Electronic System and Sneak Circuit Analysis

SCA has been conducted on hardware and software to identify latent circuits and conditions that inhibit desired functions or cause undesired functions to occur without a component having failed. It has been used extensively over the last 50 years as a safety analysis technique to verify the functionality of safety critical systems and to remove many sneak paths that may have been inadvertently designed into the system. It has been used in various forms to target applications of differing complexity and make-up, from early electric circuits involving just discrete components, through analysis of software only projects, to systems combining both software and complex integrated circuits.

SCA is considered for application on high criticality systems, where undetected design flaws may cause catastrophic events, such as loss of life, critical system failure, or loss of mission. As the power electronic system plays an important role in electric power application, SCA should be carried out in the power electronic system to improve its reliability and safety. However, the power electronic system is one kind of switched-mode system in which the power electronic components are switching on/off under a fixed control sequence, in order to convert the input voltage or current to another form with higher efficiency.

As inductor and/or capacitor are often used as energy storage components in power electronic systems, there will be many electrical current paths in power electronic system, except those from source to ground. On the other hand, since the power electronic component, for example, Power Diode, Power MOSFET (metal oxide semiconductor field effect transistor), IGBT (insulated gate bipolar transistor), and so on, has parasitic

parameters, it is impossible to consider it as an ideal switch only with ON and OFF states, then the current flows in the power electronic system will be more complicated than those in the electrical system. Therefore, the presented SCA methods are not suitable for analyzing the sneak circuit problems in the power electronic system. The sneak circuit phenomena should be studied to investigate the SCA method for the power electronic system.

1.5 Arrangement of this Book

This book starts with an introductory chapter and moves on to power electronic converter topics on sneak circuit phenomena, methods for SCA and application guidelines. The book is organized into three parts, the first of which includes Chapters 2–5 on sneak circuit phenomena of some typical power electronic converters, such as resonant switched capacitor converters, basic non-isolated DC-DC converters, soft-switching converters, Z-source converters, and synchronous converters. The next part, including Chapters 6 and 7, presents three sneak circuit path analysis methods for power electronic converters based on the generalized matrix, adjacency matrix, and Boolean matrix respectively, and one sneak circuit mode analysis method based on mesh combination. The final part, comprising Chapters 8 and 9, focuses on the guidelines concerning elimination and application of sneak circuits in power electronic converters.

This book will help researchers and engineers, in the power electronics field and the related industries, to understand the fact that sneak circuits exist in power electronic systems objectively, and how to carry out SCA at the design stage to improve the reliability of power electronic systems.

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Part One

Sneak Circuit Phenomena

2

Sneak Circuits of Resonant Switched Capacitor Converters

2.1 Introduction

The switched capacitor (SC) converters are one kind of power electronic converters that do not require any inductor or transformer, only using capacitors as the energy storage components [1, 2]. With the advantages of small volume, low weight, high efficiency, and easy integration, SC converters can adapt to the developing trend of power electronics. However, the SC converter has inherent disadvantages of high current stress and EMI (Electro Magnetic Interference) problem [3, 4]. In order to improve the performance of SC converters, a new topology named the resonant switched capacitor (RSC) converter has been proposed, in which an inductor is added in series with the SC [5, 6]. The inserted inductor is very small, mainly used to make up an LC resonant tank with the SC and realize zero-current switching (ZCS) for all switches. Thus, the power dissipation and EMI will be reduced and the advantages of the SC converter will be kept in RSC converters.

Compared with the SC converter, only one component is added in the RSC converter, but it is found that some new circuit paths (i.e., sneak circuits) do exist in RSC converters [7]. In this chapter, different types of sneak circuit phenomena in RSC converters will be introduced and the operating conditions of a sneak circuit will be described in detail.

2.2 Sneak Circuits of Basic RSC Converter

The elementary unit of a RSC converter is composed of two switching devices (S_1 and S_2), two diodes (D_1 and D_2), one SC C_r, and one resonant inductor L_r, as shown in Figure 2.1a. By connecting the four ports of the elementary RSC unit in different

Sneak Circuits of Power Electronic Converters, First Edition. Bo Zhang and Dongyuan Qiu.

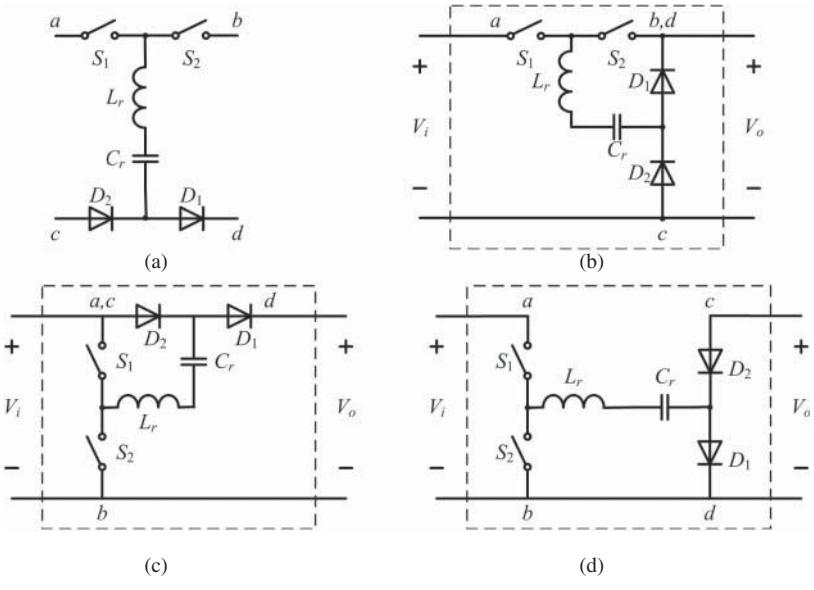


Figure 2.1 Structure of basic RSC units: (a) elementary; (b) step-down; (c) step-up; and (d) inverting

ways, step-down, step-up, and inverting RSC units can be obtained, which are shown in Figure 2.1b–d respectively.

2.2.1 Sneak Circuits of Basic Step-Down RSC Converter

Based on the step-down RSC unit in Figure 2.1b, the basic step-down RSC converter is shown in Figure 2.2. The control switches used in the RSC converter, such as Power MOSFET (metal oxide semiconductor field effect transistor) and IGBT (insulated gate bipolar transistor), have the normal inverse conduction characteristics, then an anti-parallel diode can be added in parallel with the switch.

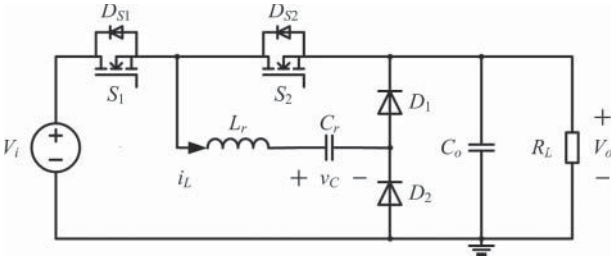


Figure 2.2 Basic step-down RSC converter

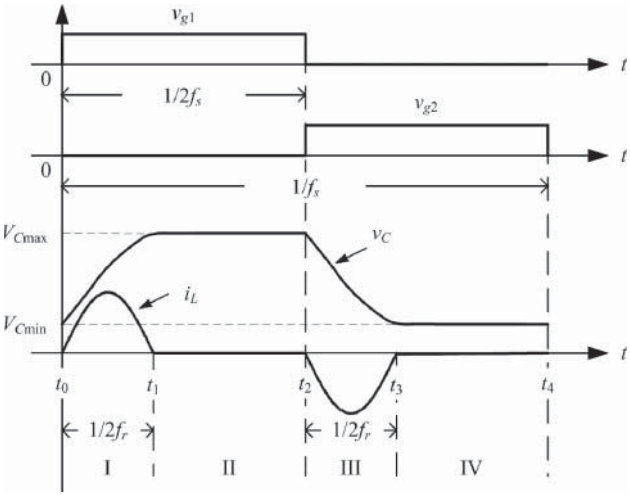


Figure 2.3 Typical waveforms of basic step-down RSC converter in the normal operating mode ($f_s < f_r$)

2.2.1.1 Normal Operating Mode of Basic Step-Down RSC Converter

In the normal operating mode, S_1 and S_2 are turned on in turn with the same duty ratio, and the switching frequency f_s must be smaller than the resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$ (i.e., $f_s < f_r$) to ensure ZCS of switches and diodes. Figure 2.3 shows the typical waveforms of driving signals v_{g1} for S_1 and v_{g2} for S_2, inductor current i_L, and SC voltage v_C.

Assuming that all the components are ideal, both the on-state resistance of the switch and the voltage drop of the diode are ignored, the output capacitor C_o is large enough to obtain a nearly constant instantaneous output voltage V_o. As shown in Figure 2.3, the normal operating process of the basic step-down RSC converter can be divided into four stages, and the corresponding equivalent circuits are demonstrated in Figure 2.4a–c, where stages II and IV are the same.

Stage I (t_0, t_1)

S_1 and D_1 are turned on with zero-current at $t = t_0$, and C_r is charged by input voltage source V_i. Based on Figure 2.4a, the circuit equation of stage I and its solutions are

$$V_i = L_r \frac{di_L}{dt} + v_C + V_o \tag{2.1}$$

$$i_L(t) = \frac{V_i - V_o - v_C(t_0)}{Z_r} \sin \omega_r (t - t_0) \tag{2.2}$$

$$v_C(t) = (V_i - V_o) - (V_i - V_o - v_C(t_0)) \cos \omega_r (t - t_0) \tag{2.3}$$

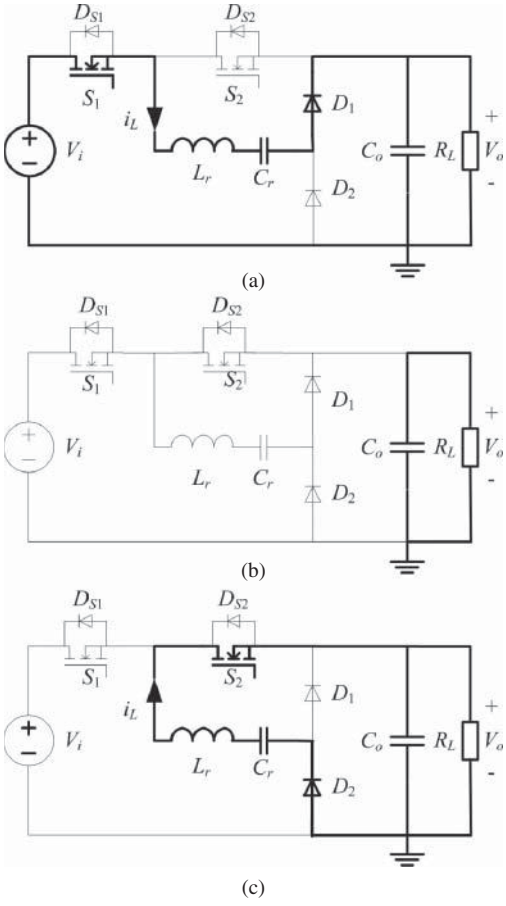


Figure 2.4 Equivalent circuits of basic step-down RSC converter in normal operating mode: (a) equivalent circuit of stage I; (b) equivalent circuit of stage II or IV; and (c) equivalent circuit of stage III

where $v_C(t_0)$ is the value of the SC voltage at t_0, resonant angular frequency $\omega_r = \frac{1}{\sqrt{L_r C_r}}$, and characteristic impedance $Z_r = \sqrt{\frac{L_r}{C_r}}$.

Assuming that $i_L(t) = 0$ at $t = t_1$, at that time the charging process of C_r is finished and v_C increases to its maximum value $V_{C\max}$, which is

$$V_{C\max} = 2V_i - 2V_o - v_C(t_0) \tag{2.4}$$

Stage II (t_1, t_2)

As shown in Figure 2.4b, all the switching components are off because i_L is equal to zero, and v_C remains at its maximum value $V_{C\max}$, that is, $v_C(t_2) = V_{C\max}$. The output capacitor C_o discharges to the load resistor R_L.

Stage III (t_2, t_3)
S_2 and D_2 are turned on with zero-current at $t = t_2$ and C_r is discharged to the load. Based on Figure 2.4c, the circuit equation of stage III and its solutions are

$$L_r \frac{di_L}{dt} + v_C - V_o = 0 \tag{2.5}$$

$$i_L(t) = \frac{V_o - v_C(t_2)}{Z_r} \sin \omega_r (t - t_2) \tag{2.6}$$

$$v_C(t) = V_o - (V_o - v_C(t_2)) \cos \omega_r (t - t_2) \tag{2.7}$$

Similarly, when $t = t_3$, $i_L(t) = 0$, then the discharging process of C_r is finished and v_C decreases to its minimum value $V_{C\min}$, which is

$$V_{C\min} = 2V_o - V_{C\max} \tag{2.8}$$

Stage IV (t_3, t_4)
As all the switching devices are off and v_C is kept at its minimum value $V_{C\min}$, that is, $v_C(t_0) = V_{C\min}$, then, Equation 2.4 becomes

$$V_{C\max} = 2V_i - 2V_o - V_{C\min} \tag{2.9}$$

From Equations 2.8 and 2.9, we obtain

$$V_o = \frac{V_i}{2} \tag{2.10}$$

Equation 2.10 shows that the relationship of input voltage and output voltage of a basic step-down RSC converter in the normal operating mode is fixed and determined by the converter structure only, which is the same as the traditional RC converter.

2.2.1.2 Sneak Circuit Mode of Basic Step-Down RSC Converter

With the same control strategy, if the inductor current i_L does not stop immediately after a half resonant cycle, and keeps resonating to the inverting direction as shown in Figure 2.5, there must be some new current paths appearing in the converter operation [8].

By analyzing the structure of the basic step-down RSC converter in Figure 2.2, it is the anti-parallel diode of the switch (e.g., D_{S1} of S_1 or D_{S2} of S_2), which consists of the freewheeling current path of i_L. As we know, D_{S1} and D_{S2} do not participate in the converter operation in the normal operating mode, therefore the current path with D_{S1} or D_{S2} belongs to the sneak circuit path of the basic step-down RSC converter.

As shown in Figure 2.5, when $f_s < f_r/2$ is selected to ensure ZCS, the operating process of the basic step-down RSC converter includes six stages when the sneak circuit appears, where stages I, II, III, and IV are the same as those in the normal

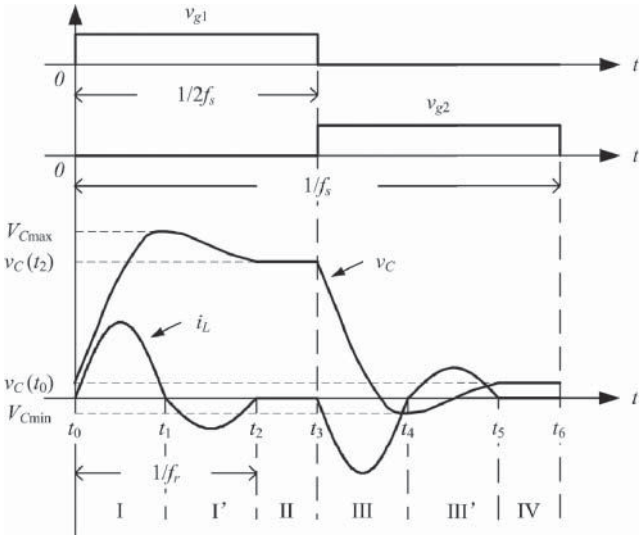


Figure 2.5 Typical waveforms of basic step-down RSC converter in sneak circuit mode ($f_s < f_r/2$)

operating mode; the other two (stages I′ and III′) are with sneak circuit paths and their corresponding equivalent circuits are shown in Figure 2.6a,b respectively.

The operating stages of a basic step-down RSC converter under sneak circuit mode are analyzed as follows:

Stage I (t_0, t_1)

S_1 is turned on, and the operating process is the same as that in normal conditions, and Equations 2.1–2.4 become available.

Stage I′ (t_1, t_2)

As the inductor current i_L continues to resonate in the negative direction, D_1 is inverting biased, but D_{S1} and D_2 are forward biased with zero-current, which means that the energy stored in the SC C_r is fed back to the input power source, and the capacitor voltage v_C drops at this stage. Based on Figure 2.6a, the circuit equation of stage I′ is

$$V_i = L\frac{di_L}{dt} + v_C \tag{2.11}$$

As $i_L(t_1) = 0$ and $v_C(t_1) = V_{C\max}$, the inductor current and the capacitor voltage of this stage can be expressed as

$$i_L(t) = \frac{V_i - V_{C\max}}{Z_r}\sin\omega_r(t - t_1) \tag{2.12}$$

$$v_C(t) = V_i - (V_i - V_{C\max})\cos\omega_r(t - t_1) \tag{2.13}$$

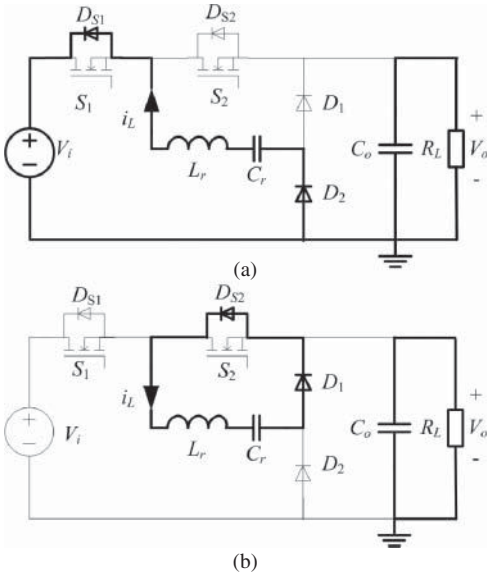


Figure 2.6 Equivalent circuits of basic step-down RSC converter in sneak circuit mode: (a) equivalent circuit of stage I′; and (b) equivalent circuit of stage III′

When $t = t_2$, the resonance process is finished and $i_L(t) = 0$, so the SC voltage is

$$v_C(t_2) = 2V_i - V_{C\max} \tag{2.14}$$

Stage II (t_2, t_3)
All the switching devices are turned off and v_C keeps at $v_C(t_2)$.

Stage III (t_3, t_4)
S_2 is turned on, and the operating process is the same as that in normal conditions, and Equations 2.5–2.7 are still available.

Similar to Equation 2.8, the SC voltage at $t = t_4$ is

$$v_C(t_4) = V_{C\min} = 2V_o - v_C(t_2) = 2(V_o - V_i) + V_{C\max} \tag{2.15}$$

Stage III′ (t_4, t_5)
As the inductor current i_L continues to resonate in the positive direction, D_2 is inverting biased, but D_{S2} and D_1 are forward biased with zero-current, which means that the energy in resonant inductor L_r is transferred to the SC C_r, then v_C rises at this stage. Based on Figure 2.6a, the circuit equation of stage III′ and its solutions are

$$L\frac{di_L}{dt} + v_C = 0 \tag{2.16}$$

$$i_L(t) = \frac{-V_{C\min}}{Z_r} \sin \omega_r (t - t_4) \tag{2.17}$$

$$v_C(t) = \frac{V_{C\min}}{Z_r} \cos \omega_r (t - t_4) \tag{2.18}$$

At $t = t_5$, the resonance is finished and $i_L(t) = 0$, then

$$v_C(t_5) = -V_{C\min} \tag{2.19}$$

Stage IV (t_5, t_6)
All the switching devices are off and v_C remains at $v_C(t_5)$, therefore

$$v_C(t_0) = v_C(t_5) = -V_{C\min} \tag{2.20}$$

Ignoring any power loss and considering energy conservation, the input energy of the power source is equal to the consumed energy of load resistor in one switching cycle, that is

$$V_i \left[\int_{t_0}^{t_1} i_L(t) dt + \int_{t_1}^{t_2} i_L(t) dt \right] = \frac{{V_o}^2}{R_L f_s} \tag{2.21}$$

Substituting Equations 2.2 and 2.12 into the above equation, we obtain

$$V_i[(V_{C\max} - v_C(t_0)) + (v_C(t_2) - V_{C\max})] = \frac{{V_o}^2}{R_L C_r f_s} \tag{2.22}$$

Substituting Equations 2.14 and 2.20 into Equation 2.22, then

$$V_i[2V_i - (V_{C\max} - V_{C\min})] = \frac{{V_o}^2}{R_L C_r f_s} \tag{2.23}$$

Based on Equation 2.15, the relationship between $V_{C\max}$ and $V_{C\min}$ is

$$V_{C\max} - V_{C\min} = 2(V_i - V_o) \tag{2.24}$$

Substituting Equation 2.24 into Equation 2.23, the output voltage is

$$V_o = 2R_L C_r f_s V_i \tag{2.25}$$

It is obvious that the average output voltage of the basic step-down RSC converter in sneak circuit mode is related to converter parameters (such as R_L and C_r) and operating conditions (such as V_i and f_s), which is very different from that in normal mode, thus the sneak circuit leads to an unexpected performance.

2.2.1.3 Sneak Circuit Conditions of Basic Step-Down RSC Converter

The precondition of sneak circuit phenomena is that there is a sneak circuit path existing in the converter. In the basic step-down RSC converter, S_1 and D_1, D_{S1} (the anti-parallel diode of S_1) and D_2 constitute bi-directional current paths for the inductor current i_L. In the normal operating mode, i_L flows through the circuit path with S_1 and

D_1 only. When sneak circuit phenomenon appears, i_L flows through not only the circuit path with S_1 and D_1 but also the one with D_{S1} and D_2. Therefore, the occurrence of the sneak circuit can be derived from the condition that the current flowing through the sneak path is not equal to zero.

Based on the inductor current expressions in stages I′ and III′, that is, Equations 2.12 and 2.17, the sneak circuit will appear when the following equation is satisfied:

$$V_i - V_{C\max} < 0 \text{ and } -V_{C\min} > 0 \tag{2.26}$$

According to Equation 2.24 and combining the above two inequalities, we have

$$2V_o - V_i < 0 \tag{2.27}$$

Substituting Equation 2.25 into Equation 2.27, the sneak circuit condition of a basic step-down RSC converter can be obtained, which is

$$4R_L C_r f_s < 1 \tag{2.28}$$

If some disturbances that make Equation 2.28 satisfied, sneak circuit phenomena will appear. Otherwise, the converter will operate in the desired way.

2.2.1.4 Experimental Verification of Basic Step-Down RSC Converter

In order to verify the above analysis, a prototype of a basic step-down RSC converter is constructed based on Figure 2.1. IRFZ44N is selected for the switch and S3SC4M is selected for the fast recovery diode. The parameters of prototype are L_r = 570 nH, $C_r = 3$ μF, $C_o = 330$ μF, $f_r = 120$ kHz, $f_s = 50$ kHz, and $V_i = 5$ V. Based on Equation 2.28, the sneak circuit condition of the prototype is $R_L < 1.67$ Ω.

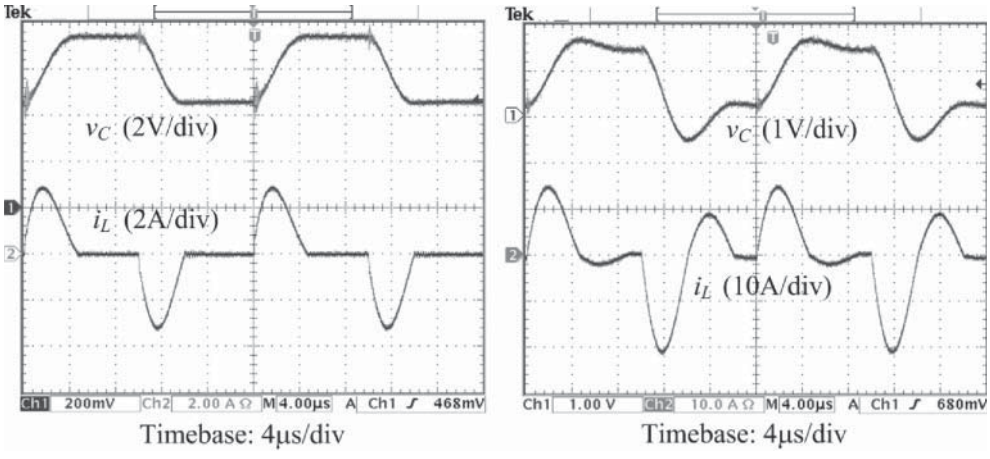
The experimental waveforms of i_L and v_C at $R_L = 6.6$ Ω are shown in Figure 2.7a, which is consistent with the ideal ones in Figure 2.2 and prove that the prototype is working in normal operating mode. When the load is changed to $R_L = 0.4$ Ω, and the experimental waveforms can be obtained as in Figure 2.7b, it is obvious that the sneak circuit phenomena appear and the correctness of sneak circuit conditions has been confirmed.

2.2.2 Sneak Circuits of Basic Step-Up RSC Converter

2.2.2.1 Normal Operating Mode of Basic Step-Up RSC Converter

The basic step-up RSC converter is illustrated in Figure 2.8. As the value of output capacitor C_o is large enough, the output side can be regarded as a DC voltage source V_o. Hence, the waveforms and equivalent circuits of the basic step-up RSC converter in the normal operating mode are shown in Figure 2.9.

Ignoring the loss of devices, the normal operating process of the basic step-up RSC converter can be divided into four stages in the steady state.



(a) (b)

Figure 2.7 Experimental waveforms of basic step-down RSC prototype under different load resistance: (a) $R_L = 6.6\ \Omega$; and (b) $R_L = 0.4\ \Omega$

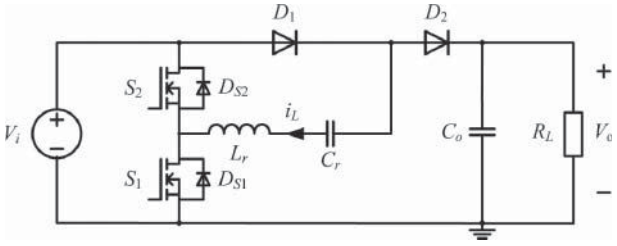


Figure 2.8 Basic step-up RSC converter

Stage I

S_1 and D_1 are turned on with zero-current, SC C_r is charged by the input voltage source V_i, and only the output capacitor C_o provides energy to the load resistor R_L. The input energy to the converter at this stage is

$$E_{i1} = V_i \int_{t_0}^{t_1} i_L(t)dt \tag{2.29}$$

Stage II

At this stage, the inductor current is zero. Meanwhile, all the switching devices are turned off, and C_o keeps discharging to R_L.

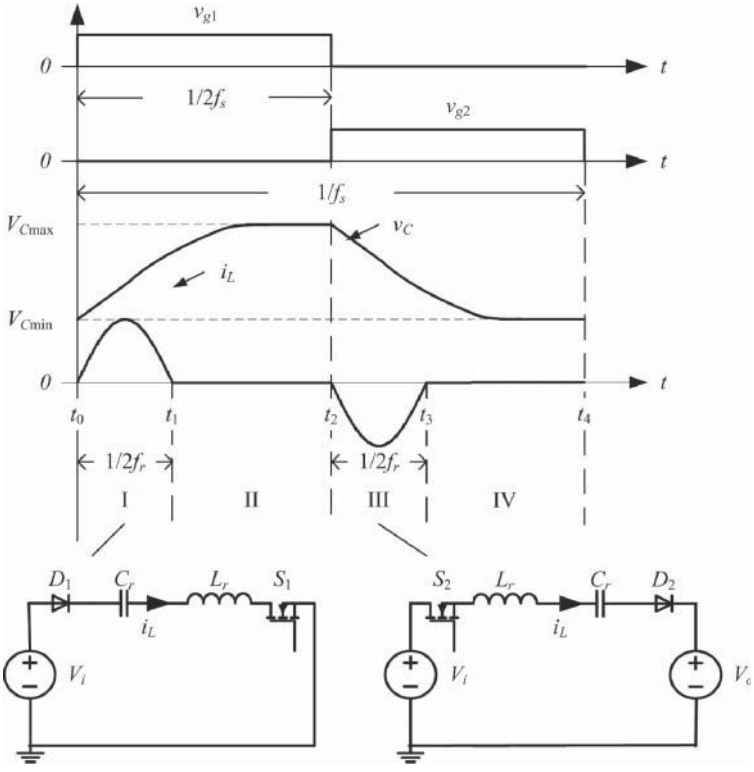


Figure 2.9 Waveforms and equivalent circuits of basic step-up RSC converter in normal operating mode ($f_s < f_r$)

Stage III

S_2 and D_2 are turned on with ZCS, and V_i and C_r provide energy to R_L simultaneously. The input energy to the converter at this stage is

$$E_{i3} = -V_i \int_{t_2}^{t_3} i_L(t)dt \tag{2.30}$$

and the output energy to the load at this stage is

$$E_{o3} = -V_o \int_{t_2}^{t_3} i_L(t)dt \tag{2.31}$$

Stage IV

The operating process is the same as that in Stage II.

As the resonant inductor L_r is in series with the SC C_r, equating the integral of the capacitor current (i.e., i_L) over one switching period to zero yields

$$\int_0^{T_s} i_L(t)dt = \int_{t_0}^{t_1} i_L(t)dt + \int_{t_2}^{t_3} i_L(t)dt = 0 \tag{2.32}$$

Based on the principle of energy conservation, we have

$$E_{i1} + E_{i3} = E_{o3} \tag{2.33}$$

Substituting Equations 2.29–2.32 into Equation 2.33, the average output voltage is

$$V_o = 2V_i \tag{2.34}$$

It is obvious that the output voltage of a basic step-up RSC converter in normal operating mode is fixed and determined by the converter structure only, which is the same as the traditional RC converter.

2.2.2.2 Sneak Circuit Mode of Basic Step-Up RSC Converter

Referring to the sneak circuit phenomena of the basic step-down RSC converter described in Section 2.1.1, the anti-parallel diodes D_{S1} and D_{S2} in the basic step-up RSC converter can also comprise sneak circuit paths, which are shown in Figure 2.10 [9].

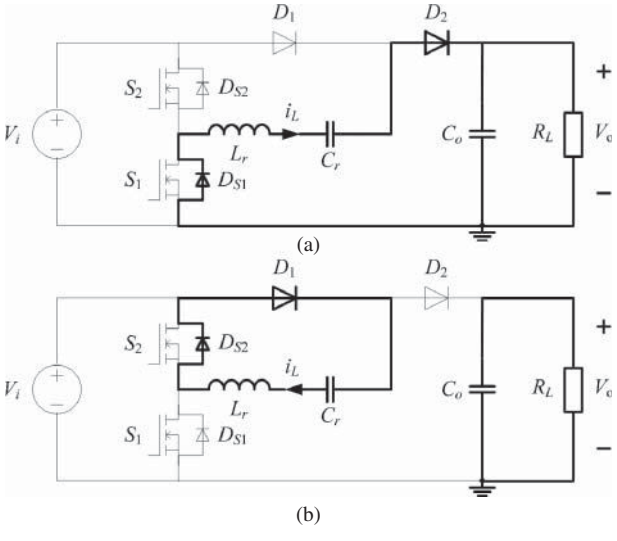


Figure 2.10 Sneak circuit paths of basic step-up RSC converter. (a) Sneak circuit path with D_{S1} and (b) sneak circuit path with D_{S2}

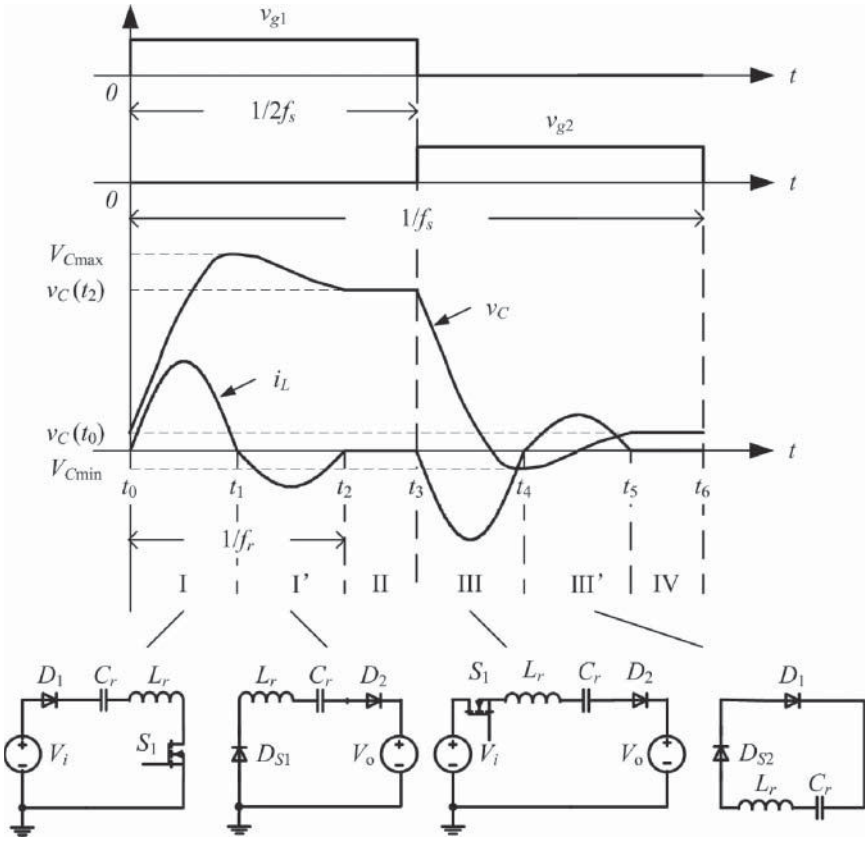


Figure 2.11 Typical waveforms and equivalent circuits of basic step-up RSC converter in sneak circuit mode ($f_s < f_r/2$)

If these two sneak circuit paths participate in the converter operation, then the inductor current i_L can flow bi-directionally. Thus, the typical waveforms and equivalent circuits of a basic step-up RSC converter in sneak circuit mode are shown in Figure 2.11, and the operation process can be divided into six stages.

Stage I (t_0, t_1)

This stage is the same as that in the normal operating mode. The expression of the inductor current is

$$i_L(t) = \frac{V_i - v_C(t_0)}{Z_r} \sin \omega_r (t - t_0) \tag{2.35}$$

Based on the equivalent circuit of stage I and Equation 2.35, the maximum value of the SC voltage can be obtained at the end of this stage, that is

$$V_{C\max} = v_C(t_1) = 2V_i - v_C(t_0) \tag{2.36}$$

Stage I′ (t_1, t_2)
The inductor current keeps resonating in the negative direction, through the circuit path L_r-C_r-D_2-V_o-D_{S1}. The inductor current at this stage is expressed by

$$i_L(t) = \frac{V_o - V_{C\max}}{Z_r} \sin \omega_r (t - t_1) \tag{2.37}$$

Based on the equivalent circuit of stage I′ and Equation 2.37, the SC voltage at the end of this stage is

$$v_C(t_2) = 2V_o - V_{C\max} \tag{2.38}$$

Stage II (t_2, t_3)
This stage is the same as that in normal operating mode, and $v_C(t_3) = v_C(t_2)$.

Stage III (t_3, t_4)
This stage is the same as that in normal operating mode, and the inductor current of this stage can be expressed by

$$i_L(t) = \frac{V_o - V_i - v_C(t_3)}{Z_r} \sin \omega_r (t - t_3) \tag{2.39}$$

Based on the equivalent circuit of stage III and Equation 2.39, the minimum value of the SC voltage can be obtained at the end of this stage, that is

$$V_{C\min} = v_C(t_4) = 2(V_o - V_i) - v_C(t_3) = V_{C\max} - 2V_i \tag{2.40}$$

Stage III′ (t_3, t_4)
The inductor current keeps resonating in the positive direction, through the circuit path L_r-D_{S2}-D_1-C_r. Thus the inductor current of this stage is expressed by

$$i_L(t) = \frac{-V_{C\min}}{Z_r} \sin \omega_r (t - t_4) \tag{2.41}$$

Based on the equivalent circuit of stage III′ and Equation 2.41, the SC voltage at the end of this stage is

$$v_C(t_5) = -V_{C\min} \tag{2.42}$$

Stage IV (t_5, t_6)
This stage is the same as that in normal operating mode, and $v_C(t_0) = v_C(t_5)$.

Due to the energy provided to the load-side during stages I′ and III being equal to that consumed by the load resistor in one switching period, we obtain

$$-\left(V_o \int_{t_1}^{t_2} i_L(t)\, dt + V_o \int_{t_3}^{t_4} i_L(t) dt \right) = \frac{{V_o}^2}{R_L f_s} \tag{2.43}$$

Substituting Equations 2.37 and 2.39 into the above equation, we have

$$2[(V_{C\max} - V_o) + (v_C(t_3) + V_i - V_o)] = \frac{V_o}{R_L C_r f_s} \tag{2.44}$$

Therefore

$$V_o = 2R_L C_r f_s V_i \tag{2.45}$$

From Equation 2.45, the basic step-up RSC converter demonstrates an unexpected characteristic in sneak circuit mode, because its average output voltage V_o no longer remains at $2V_i$, but relates to circuit parameters (such as C_r) and operating conditions (such as R_L, f_s).

2.2.2.3 Sneak Circuit Conditions of Basic Step-Up RSC Converter

Based on the above analysis, it is clear that the paths constituted by D_{S1} and D_1, D_{S2}, and D_2 belong to the sneak circuit paths of a basic step-up RSC converter, then for the sneak circuit conditions, it can be considered that the inductor current of stages I′ and III′ are not equal to zero. From Equations 2.37 and 2.41, we know that $V_o - V_{C\max} < 0$ and $-V_{C\min} > 0$, that is

$$V_o - V_{C\max} < 0 < -V_{C\min} \tag{2.46}$$

Rearranging the above inequality, we have

$$V_{C\max} - V_{C\min} > V_o \tag{2.47}$$

Substituting Equations 2.40 and 2.45 into Equation 2.47, the sneak circuit condition of a basic step-up RSC converter is

$$R_L C_r f_s < 1 \tag{2.48}$$

Therefore, if the circuit parameters and operation conditions of a basic step-up RSC converter do not satisfy Equation 2.48, the converter will operate normally. Otherwise, if there is a disturbance such as load R_L decreasing to satisfy Equation 2.48, then sneak circuit phenomenon will appear.

2.2.2.4 Experimental Verification of Basic Step-Up RSC Converter

To verify the above analysis, a basic step-up RSC prototype is built based on Figure 2.8. IRFZ44N and S3SC4M are selected to be the switch and fast recovery diode respectively. The parameters of prototype are listed as $L_r = 400$ nH, $C_r = 3$ μF, $C_o = 330$ μF, $f_r = 145$ kHz, $f_s = 50$ kHz, and $V_i = 5$ V. Based on Equation 2.48, the sneak circuit condition of the prototype is $R_L < 6.67$ Ω.

The experimental waveforms of inductor current i_L and SC voltage v_C at $R_L = 15$ Ω are shown in Figure 2.12a, from which it is clear that the prototype is working in

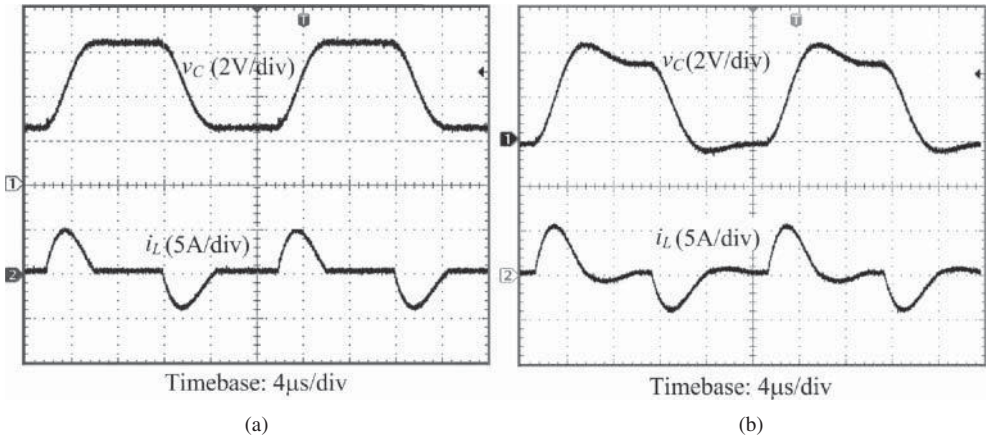


Figure 2.12 Experimental waveforms of basic step-up RSC prototype under different load resistance: (a) $R_L = 15\ \Omega$; and (b) $R_L = 4.7\ \Omega$

normal operating mode. The experimental waveforms at $R_L = 4.7\ \Omega$ are shown in Figure 2.12b, which is different from Figure 2.12a and ensures that the sneak circuit phenomena appear.

Therefore, the experimental results are consistent with the above theoretical analysis. It should be stated that the input power source is not ideal and contains internal resistance, which leads to some difference between experimental waveforms and theoretical waveforms.

2.2.3 Sneak Circuits of Basic Inverting RSC Converter

The basic inverting RSC converter is shown in Figure 2.13, which is one type of RSC converter where its output voltage is negative-polarity with respect to the common terminal of the input voltage. Normally, each switch is turned on for one half-cycle, the typical operating waveforms and equivalent circuits in normal operating mode are shown in Figure 2.14.

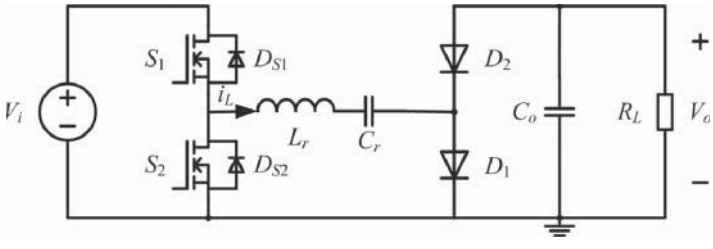


Figure 2.13 Basic inverting RSC converter

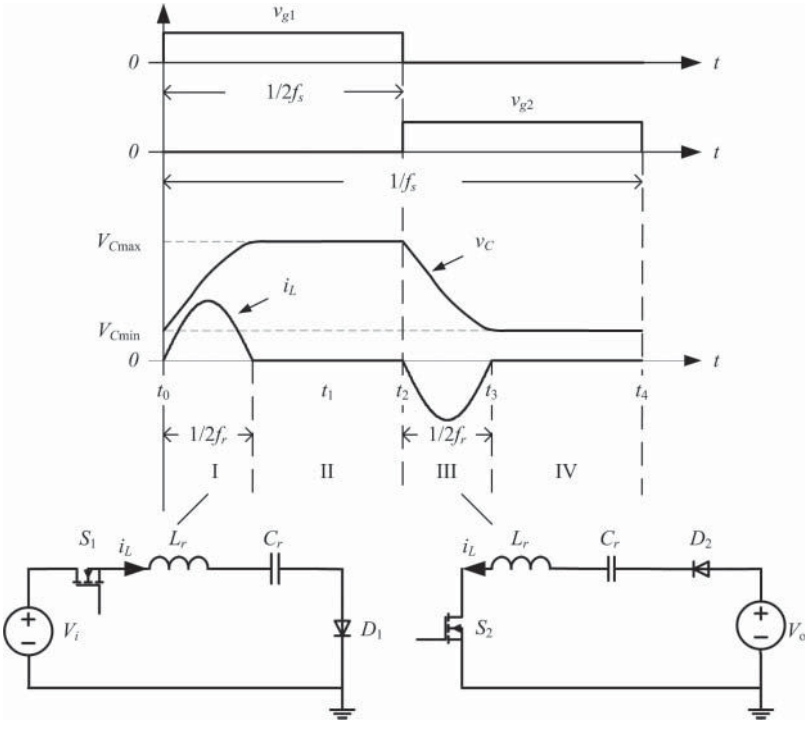


Figure 2.14 Typical waveforms and equivalent circuits of basic inverting RSC converter in normal operating mode ($f_s < f_r$)

It is known that the integral of capacitor current in one switching period equals zero, and from Figure 2.14, we have

$$\int_0^{T_s} i_C(t)dt = \int_{t_0}^{t_1} i_L(t)dt + \int_{t_2}^{t_3} i_L(t)dt = 0 \tag{2.49}$$

Based on the principle of energy conservation, the energy provided by the input voltage source equals that sent to the load, that is

$$V_i \int_{t_0}^{t_1} i_L(t)dt = V_o \int_{t_2}^{t_3} i_L(t)dt \tag{2.50}$$

Combining Equations 2.49 and 2.50, the output voltage is

$$V_o = -V_i \tag{2.51}$$

Consequently, the relationship between input and output voltages of a basic inverting RSC converter in normal operating mode is determined by the converter structure, so any disturbance in the converter parameters or operating conditions has no influence on the output voltage.

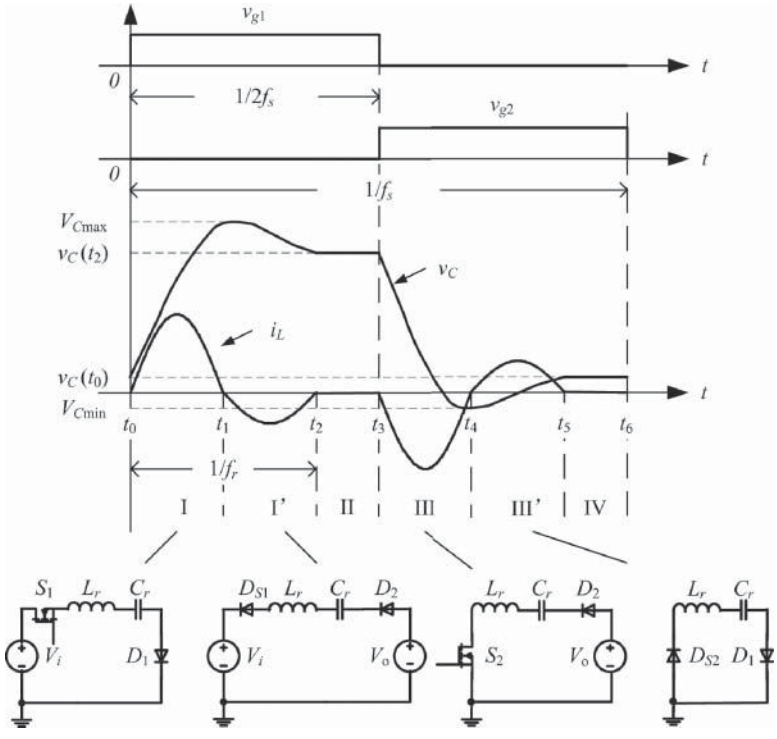


Figure 2.15 Typical waveforms and equivalent circuits of basic inverting RSC converter in sneak circuit mode ($f_s < f_r/2$)

Similar to the basic step-up RSC converter, the anti-parallel diodes D_{S1} and D_{S2} could constitute the sneak circuit paths in the inverting RSC converter, which provide different paths for the inductor current. When these sneak circuit paths participate in converter operation, the typical waveforms and equivalent circuits of a basic inverting RSC converter are as shown in Figure 2.15 [9].

Comparing Figure 2.15 with Figure 2.11, it is found that the equivalent circuits of a basic inverting RSC converter are similar to those of a basic step-up RSC converter when sneak circuits appear. Hence, by using the analytical method of Section 2.1.2, the output voltage of a basic inverting RSC converter in sneak circuit mode is

$$V_o = -2R_L C_r f_s V_i \tag{2.52}$$

Therefore, when sneak circuits appear, the basic inverting RSC converter will demonstrate an unexpected characteristic, and the relationship between input and output voltages no longer keeps constant, but is determined by the circuit parameters (such as C_r) and operating condition (such as R_L and f_s).

Referring to Section 2.1.2, the sneak circuit condition of a basic inverting RSC converter can be derived as

$$2R_L C_r f_s < 1 \tag{2.53}$$

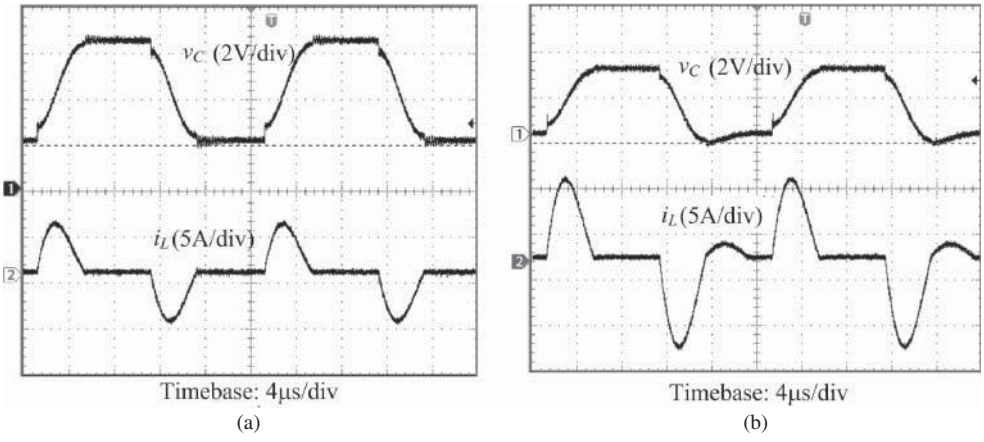


Figure 2.16 Experimental waveforms of basic inverting RSC prototype under different load resistance: (a) $R_L = 4.7\ \Omega$; and (b) $R_L = 1.1\ \Omega$

A prototype of a basic inverting RSC converter was built, in which the components were the same as the basic step-up RSC prototype described in Section 2.1.2. However, the corresponding sneak circuit condition of the basic inverting RSC prototype is $R_L < 3.33\ \Omega$, based on Equation 2.53.

The experimental waveforms of SC voltage v_C and inductor current i_L under different loads are shown in Figure 2.16. It is found that the prototype was working in normal operating mode when $R_L = 4.7\ \Omega$, but in sneak circuit operating mode when $R_L = 1.1\ \Omega$. Thus, the experimental results are consistent with the above theoretical analysis.

2.2.4 Sneak Circuit Performance of Basic RSC Converters

In order to better understand the performance of basic RSC converters, the output voltage expressions in different operating modes and the sneak circuit conditions are synthesized in Table 2.1. It can be concluded that the output voltage in sneak circuit mode is independent of the converter structure, and is closely related to circuit parameters (such as C_r) and operation conditions (such as R_L and f_s). As shown in Figure 2.17, the sneak circuits will lead to an unwanted performance, in which the output voltage of the basic RSC converter is usually lower than that in normal mode.

2.3 Sneak Circuits of High-Order RSC Converter

Since the output voltage of the basic RSC converter is certain in the normal operating mode, the structure of the RSC converter has been modified to meet the requirements of larger ratio of input and output voltages.

Table 2.1 Sneak circuit conditions and output voltage expressions of basic RSC converters ($f_s < f_r$)

Converter type	Output voltage V_o		Sneak circuit condition
	Normal mode	Sneak circuit mode	
Step-down	$V_o = \frac{V_i}{2}$	$V_o = 2R_L C_r f_s V_i$	$R_L C_r f_s < \frac{1}{4}$
Step-up	$V_o = 2V_i$	$V_o = 2R_L C_r f_s V_i$	$R_L C_r f_s < 1$
Inverting	$V_o = -V_i$	$V_o = -2R_L C_r f_s V_i$	$R_L C_r f_s < \frac{1}{2}$

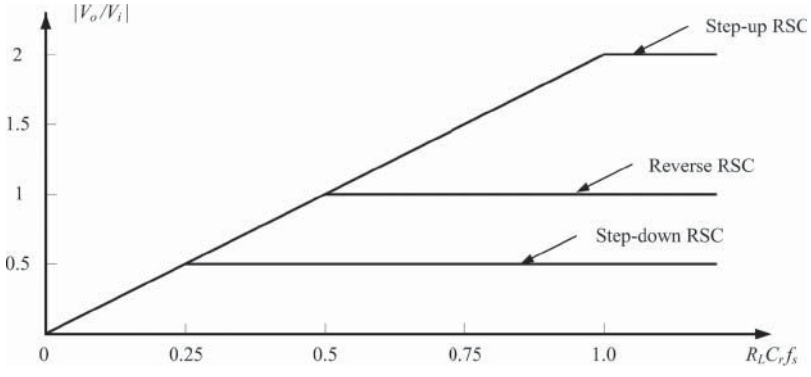


Figure 2.17 $|V_o/V_i|$ versus $R_L C_r f_s$ in basic RSC converters

By connecting capacitors and diodes in series or in parallel, different forms of SC units can be obtained, as shown in Figure 2.18. Commonly, the capacitance of each capacitor is equal, and the order of the SC unit (expressed as n) is defined by the number of independent capacitors in the unit. The operating principle of the SC unit is described by "charging in series and discharging in parallel," that is, when the SC unit is charged, the independent capacitors are connected in series by the diodes between the capacitors, such as D_{i1} in Figure 2.18b and D_{i1} and D_{i2} in Figure 2.18c. When the SC unit is discharged, the independent capacitors are connected in parallel by other diodes, such as D_{p1} and D_{q2} in Figure 2.18b and D_{p1}, D_{p2}, D_{q2}, and D_{q3} in Figure 2.18c.

2.3.1 Sneak Circuits of High-Order Step-Down RSC Converter

2.3.1.1 Normal Operating Mode of High-Order Step-Down RSC Converter

If the SC in the basic step-down RSC converter is replaced by a SC unit with $n-1$ independent capacitors, then a n-order step-down RSC converter can be constructed, as shown in Figure 2.19 [10].

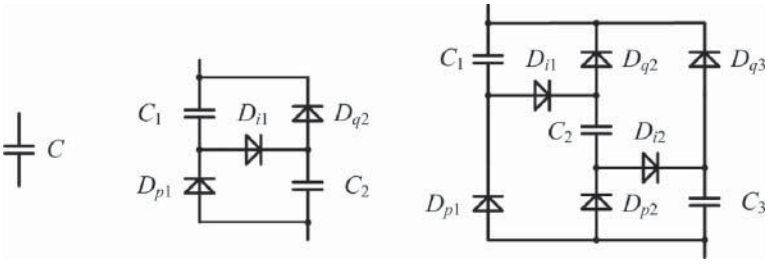


Figure 2.18 SC unit: (a) $n = 1$; (b) $n = 2$; and (c) $n = 3$

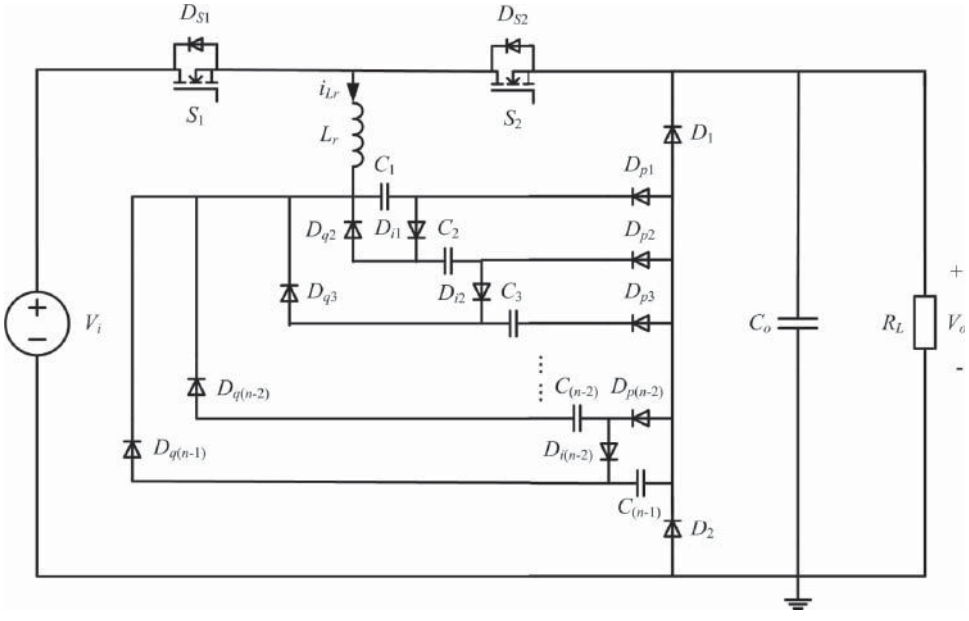


Figure 2.19 n-order step-down RSC converter

When S_1 is turned on, $n-1$ SCs are charged in series by the input voltage source, and the charging resonant frequency is $f_{nr1} = \frac{1}{2\pi}\sqrt{\frac{n-1}{LC}}$. However, when S_2 is turned on, $n-1$ SCs are discharged to the load in parallel, and the discharging resonant frequency is $f_{nr2} = \frac{1}{2\pi}\sqrt{\frac{1}{(n-1)LC}}$. In order to realize ZCS, the switching frequency f_s should be smaller than the lower resonant frequency, that is, $f_s < f_{nr2} < f_{nr1}$.

According to the above operating principle of the high-order step-down RSC converter, the typical waveforms and equivalent circuits in the normal operating mode are obtained, as in Figures 2.20 and 2.21 respectively. The operating process of the converter can be divided into four stages, as all the devices are assumed ideal to simplify the analysis.

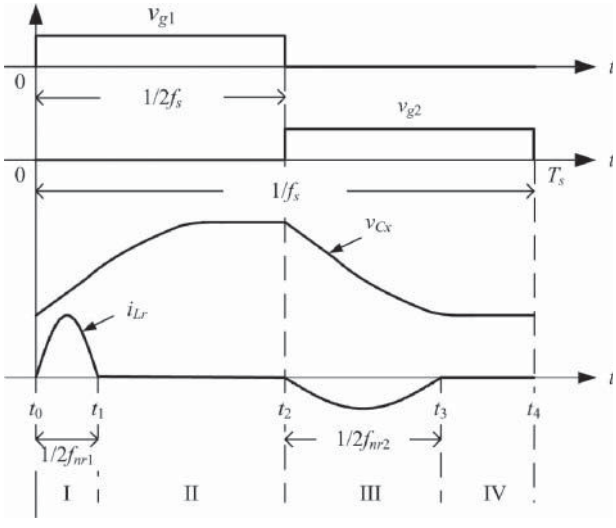


Figure 2.20 Typical waveforms of the *n*-order step-down RSC converter in normal operating mode ($f_s < f_{nr2}$)

Stage I

As shown in Figure 2.21a, S_1 and D_1 are turned on with zero-current at $t = t_0$, and the SCs are charged by V_i in series. Thus the capacitor current is equal to the inductor current, that is, $i_{Cx} = i_{Lr}$, $(x = 1, 2, \ldots, n-1)$. When $t = t_1$, $i_{Lr}(t) = 0$, the capacitor voltage v_{Cx} reaches its maximum value.

The input energy from the voltage source in this stage is

$$E_{i1} = V_i \int_{t_0}^{t_1} i_{Lr}(t)dt \tag{2.54}$$

and the output energy to the load in this stage is

$$E_{o1} = V_o \int_{t_0}^{t_1} i_{Lr}(t)dt \tag{2.55}$$

Stage II

When all the switching devices are turned off, v_{Cx} keeps at its maximum value. Only the output capacitor C_o provides energy to the load resistor R_L.

Stage III

When $t = t_2$, S_2 and D_2 are turned on with zero-current, and the switching capacitors are discharged to the load in parallel, as shown in Figure 2.21b. When $t = t_3$, the capacitor voltage v_{Cx} drops to its minimum value. Based on Kirchhoff's voltage law,

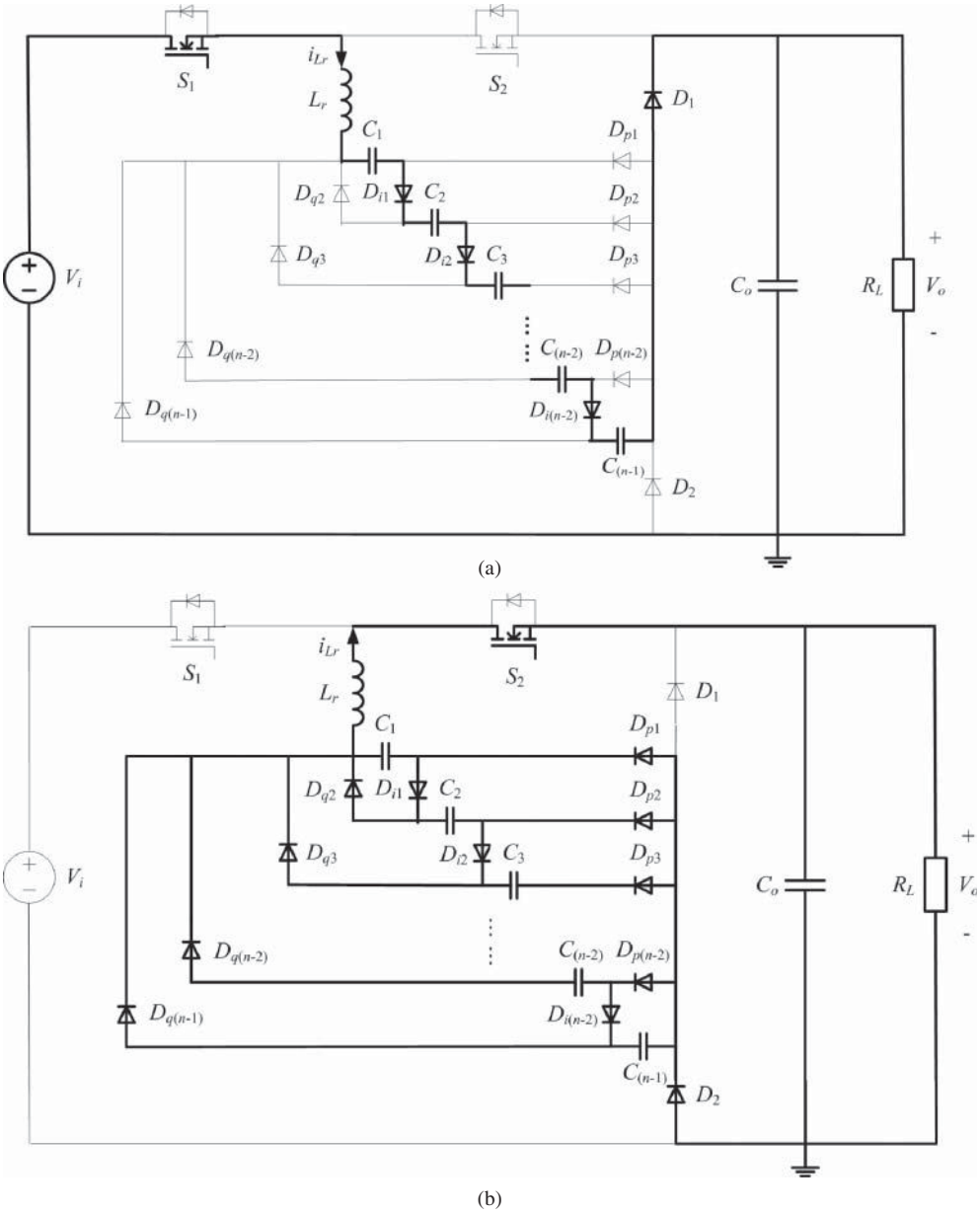


Figure 2.21 Equivalent circuits of the *n*-order step-down RSC converter in normal operating mode: (a) equivalent circuit of stage I; and (b) equivalent circuit of stage III

the state equation for each SC is

$$V_o = L\frac{di_{Lr}}{dt} + v_{Cx} \tag{2.56}$$

Because the capacitance of each SC is selected to be equal, that is, $C_1 = C_2 = \ldots = C_{n-1} = C_r$, the derivation of Equation 2.56 is

$$\frac{di^2_{Lr}(t)}{dt^2} + \frac{i_{Cx}}{C_r} = 0 \tag{2.57}$$

which means that the current flowing in each SC is equal in stage III, and $i_{Cx} = \frac{i_{Lr}}{n-1}$ can be obtained from Figure 2.21b.

The output energy to the load at this stage is

$$E_{o3} = -V_o \int_{t_2}^{t_3} i_{Lr}(t)dt \tag{2.58}$$

Stage IV

The operating process is the same as that in stage II, but v_{Cx} keeps at its minimum value.

According to the integral of the capacitor current over one switching period being zero, the current of capacitor C_1 satisfies

$$\int_{t_0}^{t_1} i_{C1}(t)dt + \int_{t_2}^{t_3} i_{C1}(t)dt = \int_{t_0}^{t_1} i_{Lr}(t)dt + \int_{t_2}^{t_3} \frac{i_{Lr}(t)}{n-1}dt = 0 \tag{2.59}$$

The energy conservation principle yields $E_{i1} = E_{o1} + E_{o3}$, that is

$$V_i \int_{t_0}^{t_1} i_{Lr}(t)dt = V_o \int_{t_0}^{t_1} i_{Lr}(t)dt - V_o \int_{t_2}^{t_3} i_{Lr}(t)dt \tag{2.60}$$

Substituting Equation 2.59 to Equation 2.60 gives

$$V_o = \frac{V_i}{n} \tag{2.61}$$

When the number of SCs in Figure 2.19 is set to $n - 1 = 1$ (i.e., $n = 2$), which means that there is only one SC in the high-order step-down RSC converter, the corresponding output voltage is $V_o = \frac{V_i}{n} = \frac{V_i}{2}$, which is the same as that of the basic step-down RSC converter.

From Equation 2.61, it is obvious that the relationship between input and output voltages of the high-order step-down RSC converter in the normal operating mode is decided by the topology of the converter or the number of SCs, as well as the traditional high-order SC converter [11].

2.3.1.2 Sneak Circuit Mode of High-Order Step-Down RSC Converter

According to the sneak circuit paths in basic RSC converters, the sneak circuit paths of the high-order step-down RSC converter may be composed of the anti-parallel diode of the switch, that is, D_{S1} or D_{S2}, which are illustrated in Figure 2.22 [12].

If the sneak circuits in Figure 2.22a exist, it means that the SCs are discharged to the voltage source in parallel through D_{S1}. As all of the SCs are charged in series by the input voltage through S_1 in stage I, the voltage on every SC at the end of stage I is lower than the input voltage V_i. Therefore, the sneak circuit paths in Figure 2.22a are not in fact available.

If the sneak circuits in Figure 2.22b exist, it means that the SCs are charged in series by the resonant inductor L_r through D_{S2}. This sneak circuit path can appear without any restriction.

The waveforms of inductor current i_{Lr} and capacitor voltage v_{Cx} of a high-order step-down RSC converter in sneak circuit mode are shown in Figure 2.23, where the operating process can be divided into five stages. Among these stages, the equivalent circuits of stages I, II, III, and IV are the same as those of normal operating mode, and the equivalent circuit of stage III′ is shown in Figure 2.22b. In addition, it is found that ZCS can be ensured when the switching frequency is satisfied by $f_s < \frac{f_{nr1}f_{nr2}}{f_{nr1}+f_{nr2}}$.

Though the resonant inductor and SCs construct different series-resonant circuit paths in stages I, III, and III′, the inductor current i_{Lr} and the voltage of each SC v_{cx} can be expressed in the unified form:

$$\begin{cases} i_{Lr}(t) = \dfrac{V_S - V_{C0}}{Z_{nr}} \sin \omega_{nr}(t - t_k) \\ v_{Cx}(t) = \dfrac{V_S - (V_S - V_{C0}) \cos \omega_{nr}(t - t_k)}{k_{nr}} \end{cases} \tag{2.62}$$

where V_S is the equivalent voltage source of the series-resonant circuit, V_{C0} is the equivalent initial value of the SC voltage, ω_{nr} is the equivalent resonant angular frequency, Z_{nr} is the equivalent characteristic impedance, and k_{nr} is a constant related to the SC voltage.

Based on the equivalent circuits of stages I, III, and III′, the definitions of each parameter of Equation 2.62 at different stages are summarized in Table 2.2. According to Equation 2.62 and Table 2.2, the maximum value, minimum value, and initial value of each SC can be deduced as

$$\begin{cases} V_{C\min} = \dfrac{nV_o - V_i}{n-1} \\ V_{C\max} = \dfrac{V_i + (n-2)V_o}{n-1} \\ v_C(t_0) = -V_{C\min} = \dfrac{V_i - nV_o}{n-1} \end{cases} \tag{2.63}$$

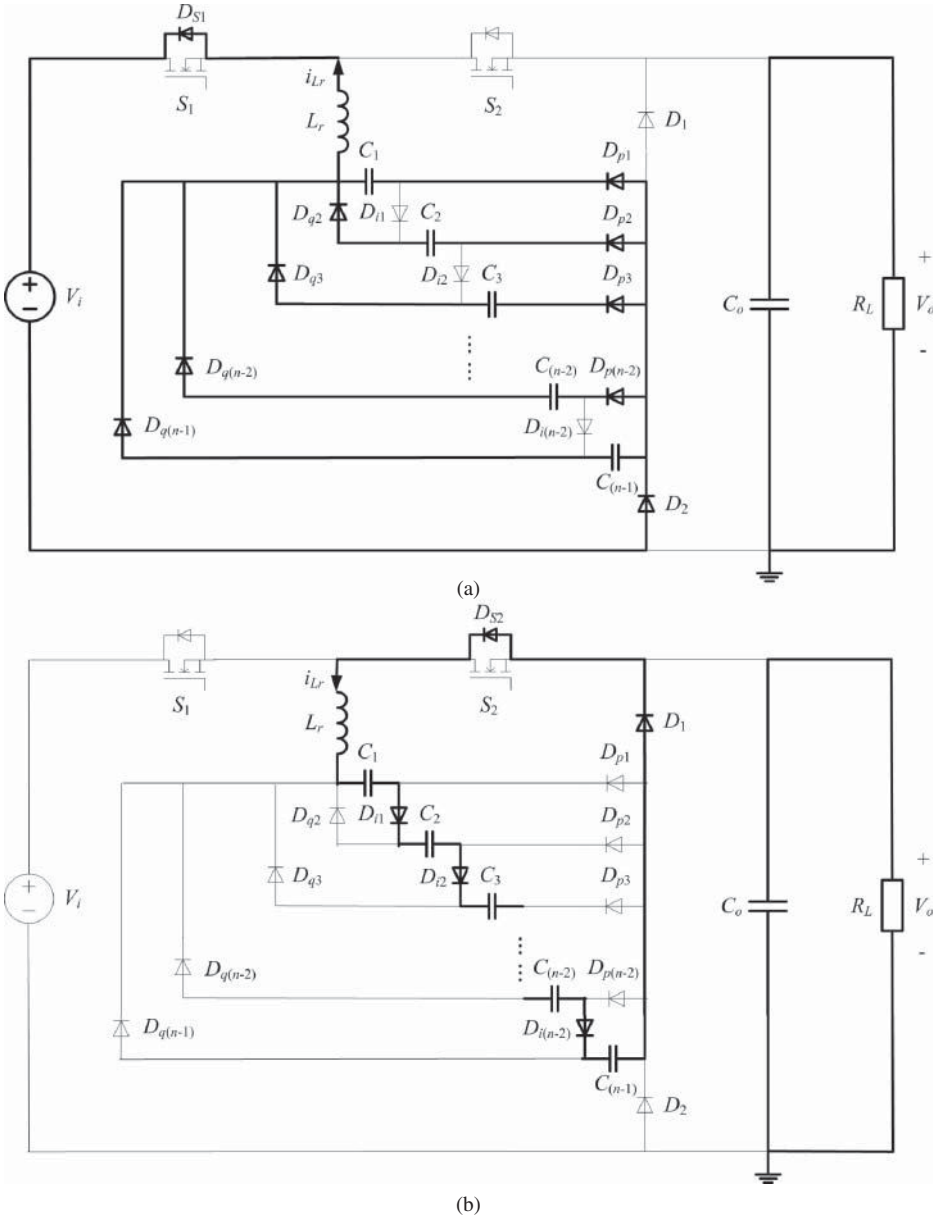


Figure 2.22 Sneak circuit paths in the *n*-order step-down RSC converter: (a) circuit paths when D_{s1} is on; and (b) circuit paths when D_{s2} is on

In the steady state, the energy provided to the output side equals that consumed by the load resistor in one switching cycle, that is

$$V_o \int_{t_0}^{t_1} i_{Lr} dt - V_o \int_{t_2}^{t_3} i_{Lr} dt = \frac{{V_o}^2}{R_L f_s} \tag{2.64}$$

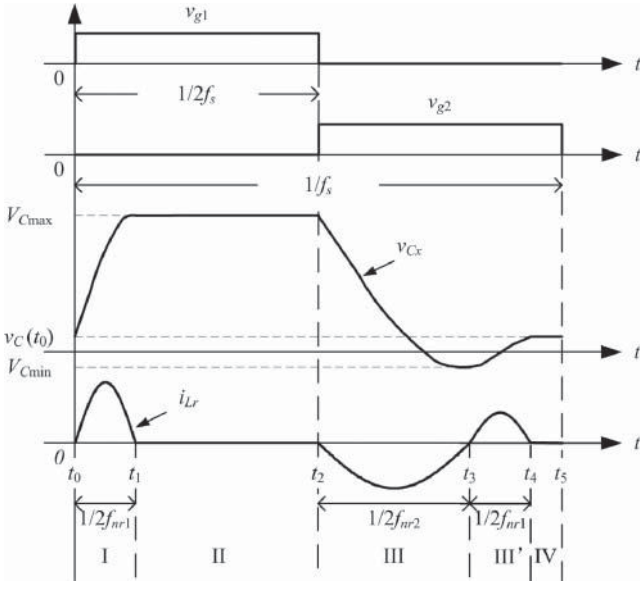


Figure 2.23 Typical waveforms of the *n*-order step-down RSC converter in sneak circuit mode $\left(f_s < \frac{f_{nr1}f_{nr2}}{f_{nr1}+f_{nr2}}\right)$

Table 2.2 Parameters of the *n*-order step-down RSC converter in sneak circuit mode

Stage	I	III	III′
t_k	t_0	t_2	t_3
V_S	$V_i - V_o$	V_o	0
V_{C0}	$(n-1)v_C(t_0)$	$V_{C\max}$	$(n-1)V_{C\min}$
ω_{nr}	$\sqrt{\frac{(n-1)}{L_rC_r}}$	$\sqrt{\frac{1}{(n-1)L_rC_r}}$	$\sqrt{\frac{(n-1)}{L_rC_r}}$
Z_{nr}	$\sqrt{\frac{(n-1)L_r}{C_r}}$	$\sqrt{\frac{L_r}{(n-1)C_r}}$	$\sqrt{\frac{(n-1)L_r}{C_r}}$
k_{nr}	$n-1$	1	$n-1$

Substituting Equations 2.62 and 2.63 into Equation 2.64, the output voltage when the sneak circuit appears can be defined by

$$V_o = 2R_L f_s C_r V_i \tag{2.65}$$

which is in accordance with the output voltage of the basic step-down RSC converter in sneak circuit mode, that is, Equation 2.45.

Referring to the above analysis, the inductor current of stage III′ is not equal to zero when the sneak circuit appears, which means that $-(n-1)V_{C\min} \geq 0$ based on Equation 2.62 and Table 2.2, that is

$$V_{C\min} \leq 0 \tag{2.66}$$

Substituting Equations 2.63 and 2.65 into Equations 2.66,

$$R_L f_s C_r \leq \frac{1}{2n} \tag{2.67}$$

can be obtained as the sneak circuit condition of the high-order step-down RSC converter.

Compared to the sneak circuit condition of the basic step-down RSC converter, that is, Equation 2.28, Equation 2.67 can be considered as a common sneak circuit condition of the step-down RSC converter, where $n = 2$ refers to basic step-down RSC converter.

2.3.1.3 Experimental Verification of Three-order Step-Down RSC Converter

To verify the above analysis, a prototype of a three-order step-down RSC converter ($n = 3$), as shown in Figure 2.24, was built. As the prototype parameters were selected to $L_r = 850$ nH, $C_1 = C_2 = 2.47$ μF, $C_o = 330$ μF, $f_{nr1} = 155$ kHz, $f_{nr2} = 78$ kHz, $f_s = 43$ kHz, and $V_i = 5$V, the sneak circuit condition of the prototype is $R_L < 1.6\ \Omega$ based on Equation 2.67, and the experimental waveforms under different load are shown in Figure 2.25.

When $R_L = 15\ \Omega$, the experimental waveforms of inductor current i_{Lr} and SC voltage v_{C1} shown in Figure 2.23a verify that the prototype is operating in the normal operating mode. Changing the load resistance to $R_L = 0.2\ \Omega$, the experimental waveforms of inductor current, SC currents and diode currents, shown in Figure 2.22b, make it is clear that the sneak circuit phenomena appear at that time. Thus, the correctness of the sneak circuit paths and sneak circuit conditions has been verified.

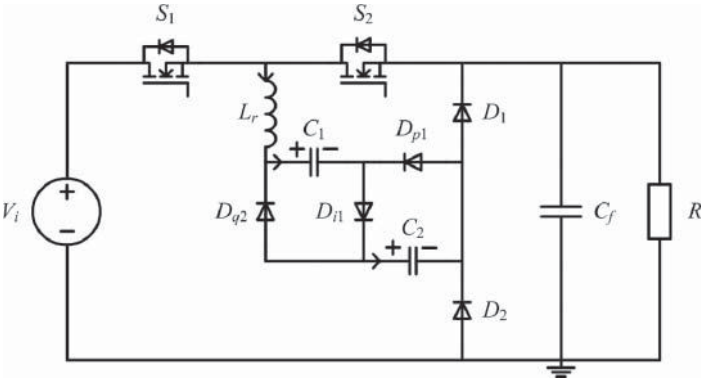


Figure 2.24 The structure of a three-order step-down RSC prototype

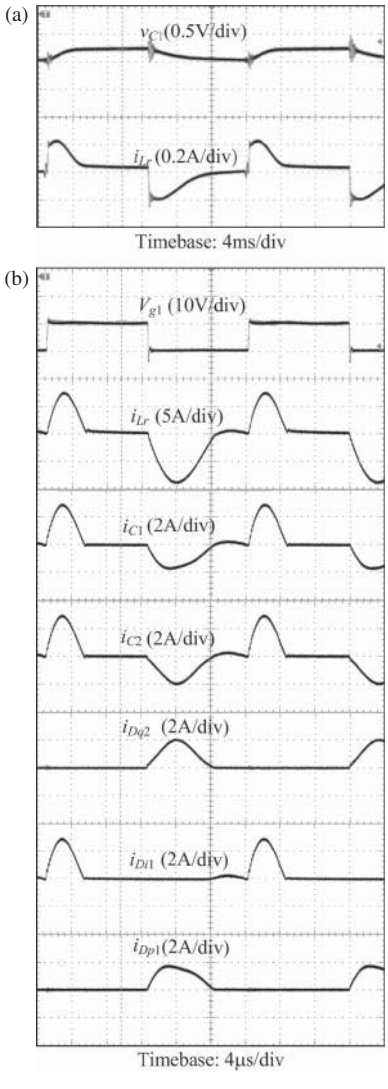


Figure 2.25 Experimental waveforms of a three-order step-down RSC prototype under different load: (a) $R_L = 15\ \Omega$; and (b) $R_L = 0.2\ \Omega$

2.3.2 Sneak Circuits of High-Order Step-Up RSC Converter

2.3.2.1 Normal Operating Mode of High-Order Step-Up RSC Converter

The step-up SC unit can be extracted from the basic step-up RSC converter, as shown in Figure 2.26. If several step-up SC units are connected in the form of the push-pull structure, and replace the step-up SC unit in the basic step-up RSC converter, then the

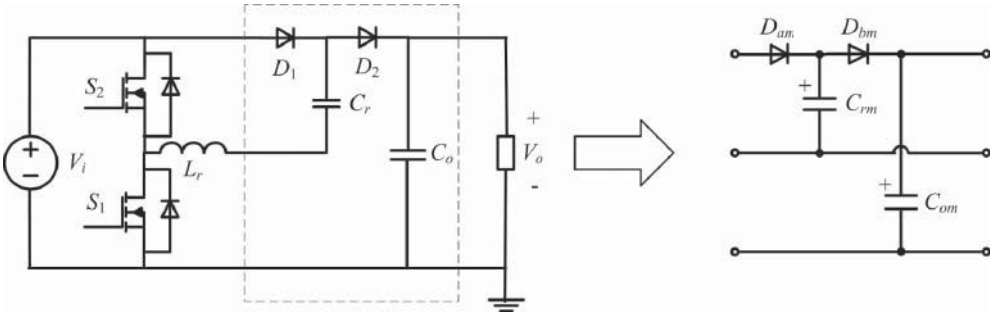


Figure 2.26 Step-up SC unit

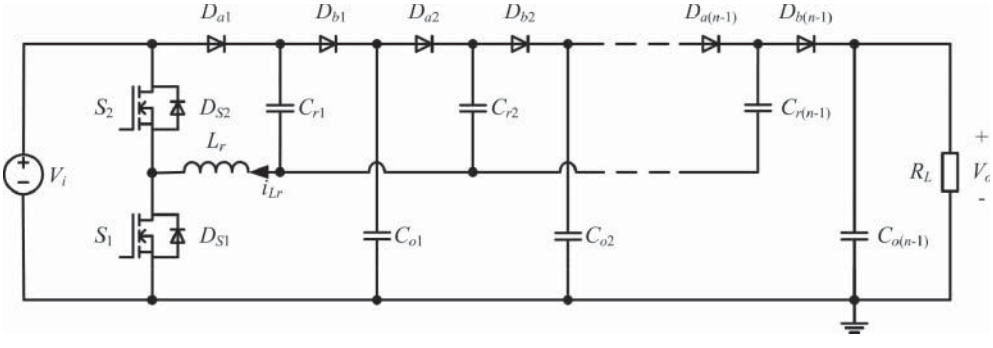


Figure 2.27 n-order step-up RSC converter

high-order step-up RSC converter can be obtained, as in Figure 2.27, in which there are $n-1$ step-up SC units [13].

Based on the principle of ratio equality, S_1 and S_2 are switched on in turn. The normal operating process of a high-order step-up RSC converter can be divided into four stages, and its typical waveforms and equivalent circuits of each stage are shown in Figures 2.28 and 2.29 respectively. To simplify the analysis, it is assumed that all the devices are ideal devices and the capacitance of every SC is equal, that is, $C_{r1} = C_{r2} = \dots\ C_{r(n-1)} = C_r$. In addition, because the output capacitor C_{ox} $(x = 1, 2, \dots, n-1)$ is generally large, the output capacitor voltage is constant, which can be regarded as a DC voltage source, represented by V_{Cox}. Each stage of the n-order step-up RSC converter in normal operating mode is analyzed as follows:

Stage I

S_1, D_{a1}, D_{a2}, … , $D_{a(n-1)}$ are turned on with ZCS. As shown in Figure 2.29a, C_{r1} is charged by V_i, C_{r2} is charged by C_{o1}, C_{r3} is charged by C_{o2}, … , $C_{r(n-1)}$ is charged by $C_{o(n-2)}$, and $C_{o(n-1)}$ supplies energy to the load resistor R_L.

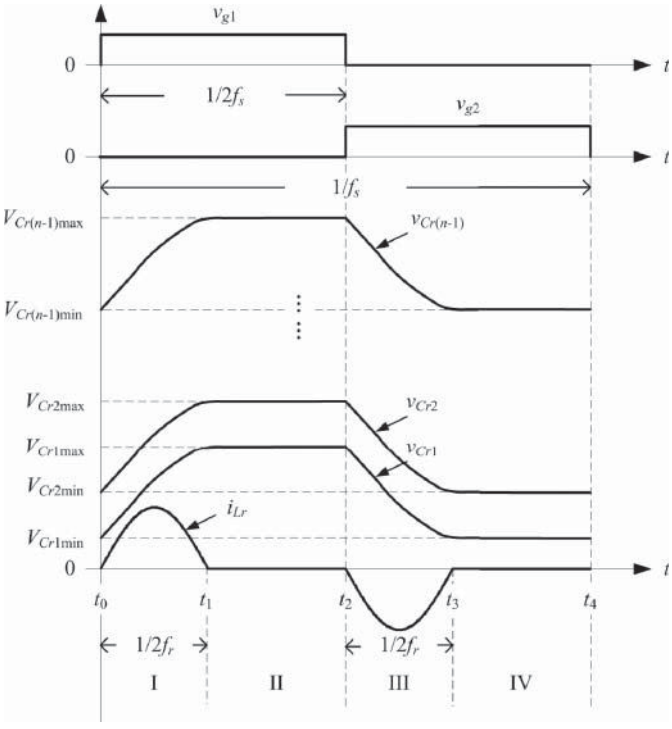


Figure 2.28 Typical waveforms of the n-order step-up RSC converter in normal operating mode ($f_s < f_r$)

At $t = t_1$, $i_{Lr}(t) = 0$, the SC voltage v_{Crx} rises to its maximum value of $V_{Crx\max}$. According to Kirchhoff's voltage law, we obtain

$$\begin{cases} V_i = v_{Cr1} + v_{Lr} \\ V_{Co1} = v_{Cr2} + v_{Lr} \\ \vdots \\ V_{Co(n-2)} = v_{Cr(n-1)} + v_{Lr} \end{cases} \tag{2.68}$$

Differentiating the above equations, we have

$$\begin{cases} \dfrac{dV_i}{dt} = \dfrac{i_{Cr1}}{C} + L\dfrac{d^2 i_{Lr}}{dt} \\ \dfrac{dV_{Co1}}{dt} = \dfrac{i_{Cr2}}{C} + L\dfrac{d^2 i_{Lr}}{dt} \\ \vdots \\ \dfrac{dV_{Co(n-2)}}{dt} = \dfrac{i_{Cr(n-1)}}{C} + L\dfrac{d^2 i_{Lr}}{dt} \end{cases} \tag{2.69}$$

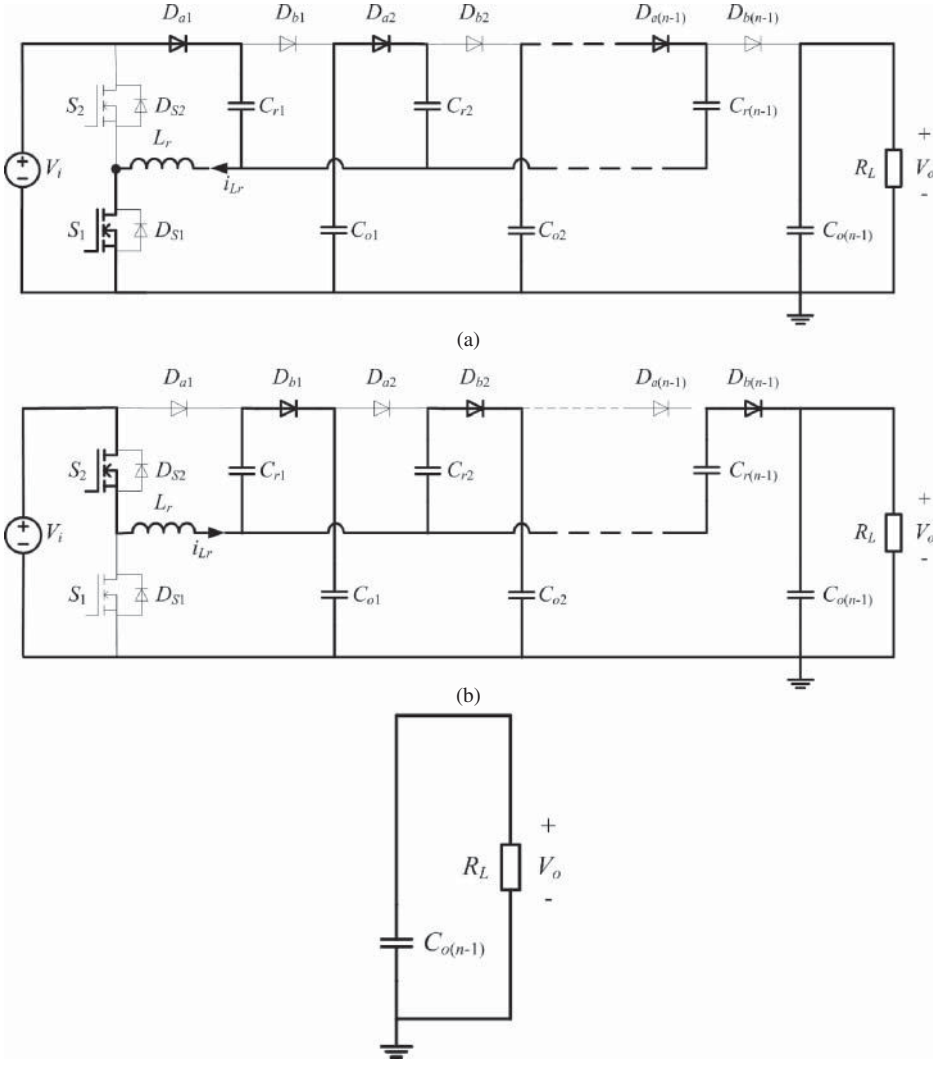


Figure 2.29 Equivalent circuits of the *n*-order step-up RSC converter in normal operating mode: (a) equivalent circuit of stage I; (b) equivalent circuit of stage III; and (c) equivalent circuits of stage II and IV

Assuming that V_{Cox} is approximate to a constant value, and its derivative equates to zero. Therefore, the current flowing through each SC is derived from Equation 2.69, which is

$$i_{Crx} = \frac{i_{Lr}}{n-1} \tag{2.70}$$

Stage II

Since the inductor current i_{Lr} remains at zero, all the switching devices are turned off, v_{Crx} remains at its maximum value, and $C_{o(n-1)}$ discharges to R_L.

Stage III

S_2, D_{b1}, D_{b2}, … , $D_{b(n-1)}$ are also turned on with ZVS (zero voltage switching). As shown in Figure 2.29b, C_{o1} is charged by V_i and C_{r1}, C_{o2} is charged by V_i and C_{r2}, … , $C_{o(n-1)}$ is charged by V_i and $C_{r(n-1)}$. At $t = t_3$, $i_{Lr}(t) = 0$, v_{Crx} decreases to its minimum value of $V_{Crx\min}$.

According to Kirchhoff's voltage law, the circuit equation of stage III can be expressed by

$$V_i = v_{Lr} + v_{Crx} + V_{Cox} \tag{2.71}$$

where $x = 1, 2, \ldots, n-1$. Therefore, Equation 2.70 is still available in stage III.

Stage IV

The converter operation is the same as that in stage II, but v_{Crx} remains at its minimum value. As the integral of capacitor current is zero in one switching cycle, from Equation 2.70, we have

$$\int_{t_0}^{t_1} i_{Crx}dt + \int_{t_2}^{t_3} i_{Crx}dt = \int_{t_0}^{t_1} \frac{i_{Lr}}{n-1}dt + \int_{t_2}^{t_3} \frac{i_{Lr}}{n-1}dt = 0 \tag{2.72}$$

The energy conservation principle yields

$$V_i \int_{t_0}^{t_1} i_{Cr1}dt + V_i \left(-\int_{t_2}^{t_3} i_{Lr}dt \right) = V_o \left(-\int_{t_2}^{t_3} i_{Cr(n-1)}dt \right) \tag{2.73}$$

Substituting Equations 2.70 and 2.72 into Equation 2.73, we obtain

$$V_o = nV_i \tag{2.74}$$

where $n = 2$ refers to the basic step-up RSC converter.

From Equation 2.74, it is known that the relationship between input and output voltages of a high-order step-up RSC converter in normal mode is decided by the converter topology, which is the number of the step-up SC unit.

2.3.2.2 Sneak Circuit Mode of High-order Step-Up RSC Converter

Similar to the basic step-up RSC converter, the sneak circuit paths of a high-order step-up RSC converter include the anti-parallel diode of switch D_{S1} or D_{S2}. Based on Figure 2.27, it is obvious that there are $n-1$ current paths passing through D_{S1}, which are L_r-C_{r1}-D_{b1}-C_{o1}-D_{S1}, L_r-C_{r2}-D_{b2}-C_{o2}-D_{S1}, … , L_r-$C_{r(n-1)}$-$D_{b(n-1)}$-$C_{o(n-1)}$(R_L)-D_{S1},

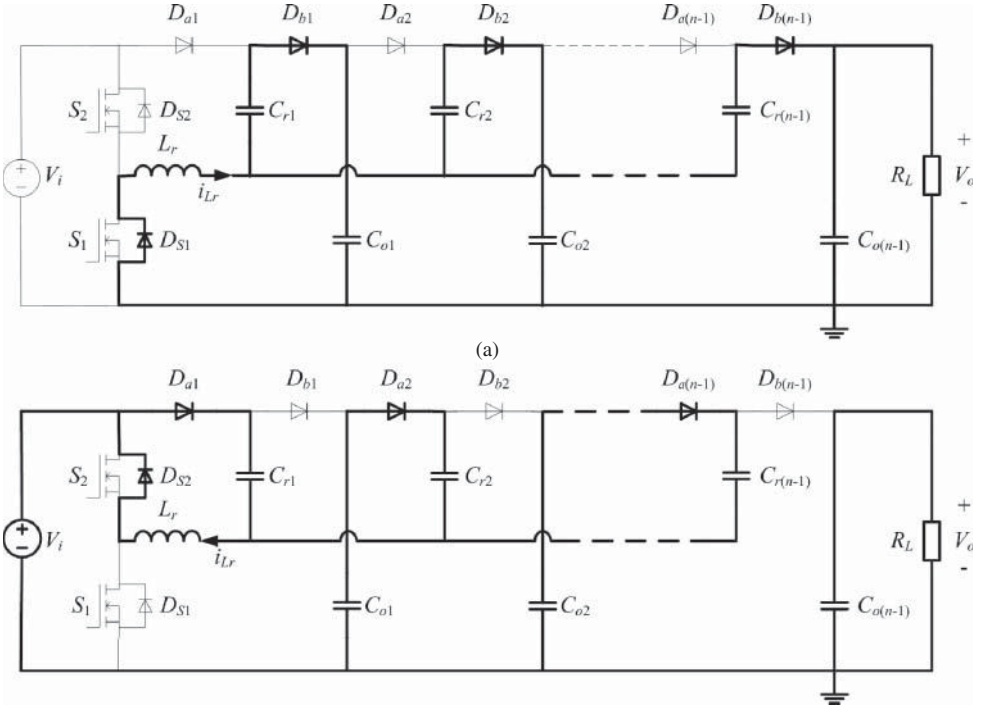


Figure 2.30 Sneak circuit paths of the n-order step-up RSC converter: (a) circuit paths when D_{S1} is on; and (b) circuit paths when D_{S2} is on

highlighted in Figure 2.30a; there are $n-1$ current paths passing through D_{S2} too, which are L_r-D_{S2}-D_{a1}-C_{r1}, L_r-D_{S2}-V_i-C_{o1}-D_{a2}-C_{r2}, L_r-D_{S2}-V_i-C_{o2}-D_{a3}-C_{r3}, … , L_r-D_{S2}-V_i-$C_{o(n-2)}$-$D_{a(n-1)}$-$C_{r(n-1)}$, highlighted in Figure 2.30b [14].

Once the above sneak circuits appear, there will be two more operating stages than the normal mode, and the corresponding waveforms are shown in Figure 2.31. In order to ensure ZCS of all switching components, $f_s < f_r/2$ is selected, then the operating process of the high-order step-up RSC converter in sneak circuit mode will be divided into six stages, and the equivalent circuit of stages I′ and III′ are referred to in Figure 2.30a,b respectively.

Like the analysis method described above, it can be proved that the current flowing through each SC is equal; moreover, Equation 2.70 is still effective at any stage.

Ignoring the dissipation of the switching devices, the energy sent to the load in stages I′ and III is equal to that assumed by the load resistor in one switching period, that is

$$-\left(\int_{t_1}^{t_2}\frac{i_{Lr}}{n-1}dt+\int_{t_3}^{t_4}\frac{i_{Lr}}{n-1}dt\right)=\frac{V_o}{R_L f_s} \tag{2.75}$$

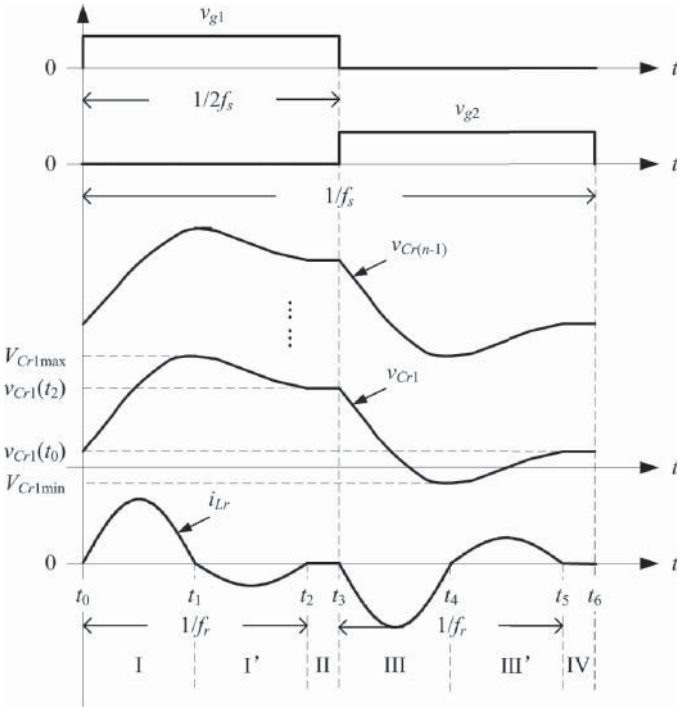


Figure 2.31 Typical waveforms of the *n*-order step-up RSC converter in sneak circuit mode ($f_s < f_r/2$)

Taking C_{r1} as an example, the voltage difference on C_{r1} is defined by

$$\begin{aligned} V_{Cr1\max} - V_{Cr1\min} &= -\frac{1}{C_r}\left(\int_{t_1}^{t_2} i_{Cr1}dt + \int_{t_3}^{t_4} i_{Cr1}dt\right) \\ &= -\frac{1}{C_r}\left(\int_{t_1}^{t_2} \frac{i_{Lr}}{n-1}dt + \int_{t_3}^{t_4} \frac{i_{Lr}}{n-1}dt\right) \end{aligned} \tag{2.76}$$

Substituting Equation 2.76 into Equation 2.75, we have

$$V_{Cr1\max} - V_{Cr1\min} = \frac{V_o}{R_L f_s C_r} \tag{2.77}$$

According to the equivalent circuit of stage I, that is, Figure 2.29a, the voltage of C_{r1} is expressed by

$$v_{Cr1}(t) = V_i - [V_i - v_{Cr1}(t_0)]\cos\omega_n(t - t_0) \tag{2.78}$$

where $\omega_n = \sqrt{\frac{1}{(n-1)L_r C_r}}$ is the resonant angular frequency of the *n*-order step-up RSC converter.

When $t = t_1$,

$$v_{Cr1}(t_1) = V_{Cr1\max} = 2V_i - v_{Cr1}(t_0) \tag{2.79}$$

According to the equivalent circuit of stage III′, Figure 2.30b, the voltage of C_{r1} is expressed by

$$v_{Cr1}(t) = V_{Cr1\min} \cos \omega_n (t - t_4) \tag{2.80}$$

When $t = t_5$,

$$v_{Cr1}(t_5) = v_{Cr1}(t_0) = -V_{Cr1\min} \tag{2.81}$$

Substituting Equations 2.79 and 2.81 into Equation 2.77, we obtain

$$V_o = 2R_L f_s C_r V_i \tag{2.82}$$

When sneak circuits appear in the high-order step-up RSC converter, its output voltage is no longer decided by the converter topology, but relates to circuit parameters or operating conditions instead.

2.3.2.3 Sneak Circuit Conditions of High-Order Step-Up RSC Converter

Referring to the sneak circuit conditions of the basic step-up RSC converter, it is known that when a sneak circuit appears in a high-order step-up RSC converter, the inductor current will not be equal to zero in stages I′ or III′. Again, taking C_{r1} as an example, the expressions of the SC current in stage I′ and III′ are

$$\begin{cases} i_{Cr1}(t) = \dfrac{V_{Co1} - V_{Cr1\max}}{(n-1)Z_n} \sin \omega_n (t - t_1) \\ i_{Cr1}(t) = \dfrac{-V_{Cr1\min}}{(n-1)Z_n} \sin \omega_n (t - t_4) \end{cases} \tag{2.83}$$

where $Z_n = \sqrt{\frac{L_r}{(n-1)C_r}}$ is the characteristic impedance of the n-order step-up RSC converter.

Because $i_{Cr1} = \frac{i_{Lr}}{n-1}$, the sneak circuit conditions can be deduced from Equation 2.83 and Figure 2.31, which are

$$\begin{cases} V_{Co1} - V_{Cr1\max} < 0 \\ V_{Cr1\min} < 0 \end{cases} \tag{2.84}$$

Substituting Equations 2.79 and 2.81 into Equation 2.84, the inequality changes to

$$V_{Co1} < 2V_i \tag{2.85}$$

According to equivalent circuit of stage I in Figure 2.29a, when $t = t_0$, the inductor voltage satisfies

$$v_{Lr}(t_0) = V_i - v_{Cr1}(t_0) = V_{Co1} - v_{Cr2}(t_0) = \cdots = V_{Co(n-2)} - v_{Cr(n-1)}(t_0) \tag{2.86}$$

According to equivalent circuit of stage I′ in Figure 2.30a, when $t = t_1$, the inductor voltage satisfies

$$\begin{aligned} v_{Lr}(t_1) &= V_{Co1} - v_{Cr1}(t_1) = V_{Co2} - v_{Cr2}(t_1) = \cdots = V_{Co(n-2)} - v_{Cr(n-2)}(t_1) \\ &= V_o - v_{Cr(n-1)}(t_1) \end{aligned} \tag{2.87}$$

Subtracting Equation 2.83 from Equation 2.84, we have

$$\begin{aligned} v_{Lr}(t_1) - v_{Lr}(t_0) &= V_i - V_{Co1} - [v_{Cr1}(t_1) - v_{Cr1}(t_0)] \\ &= V_{Co2} - V_{Co1} - [v_{Cr2}(t_1) - v_{Cr2}(t_0)] \\ &= \cdots \\ &= V_o - V_{Co(n-2)} - [v_{Cr(n-2)}(t_1) - v_{Cr(n-1)}(t_0)] \end{aligned} \tag{2.88}$$

As the current flowing through each SC is equal, we have

$$\begin{aligned} v_{Cr1}(t_1) - v_{Cr1}(t_0) &= V_{Cr2}(t_1) - v_{Cr2}(t_0) = \cdots = V_{Cr(n-1)}(t_1) - v_{Cr(n-1)}(t_0) \\ &= \frac{1}{C_r}\int_{t_0}^{t_1} \frac{i_{Lr}(t)}{n-1} dt \end{aligned} \tag{2.89}$$

Therefore,

$$V_i - V_{Co1} = V_{Co1} - V_{Co2} = \cdots = V_{Co(n-2)} - V_{Co(n-1)} = V_o - V_{Co(n-2)} \tag{2.90}$$

Summing up all the equations in Equation 2.90, we have

$$V_{Co1} = V_i + \frac{V_o - V_i}{n-1} \tag{2.91}$$

Substituting Equation 2.91 into Equation 2.85, the sneak circuit condition of high-order step-up RSC converter can be obtained:

$$R_L C_r f_s < \frac{n}{2} \tag{2.92}$$

When $n = 2$, the result of Equation 2.92 is consistent with Equation 2.48, which is the sneak circuit condition of the basic step-up RSC converter. Therefore, Equation 2.92 can be considered as a common sneak circuit condition of step-up RSC converters.

2.3.2.4 Experimental Verification of Three-Order Step-Up RSC Converter

To verify the above analysis, a prototype of a three-order step-up RSC converter ($n = 3$) was built, as shown in Figure 2.32, with parameters of $L_r = 320$ nH, $C_r = 2$ μF, $C_o = 330$ μF, $f_r = 140$ kHz, $f_s = 42$ kHz, and $V_i = 2$V. Based on Equation 2.92, when the load resistance satisfies $R_L < 17.8\ \Omega$, the sneak circuit phenomena will appear. The experimental waveforms of SC voltages and inductor current with $R_L = 22\ \Omega$

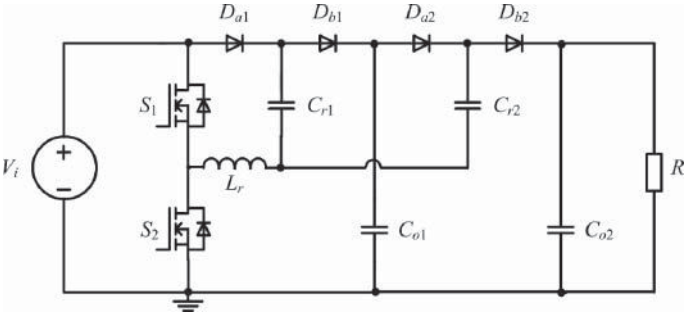


Figure 2.32 The structure of a three-order step-up RSC prototype

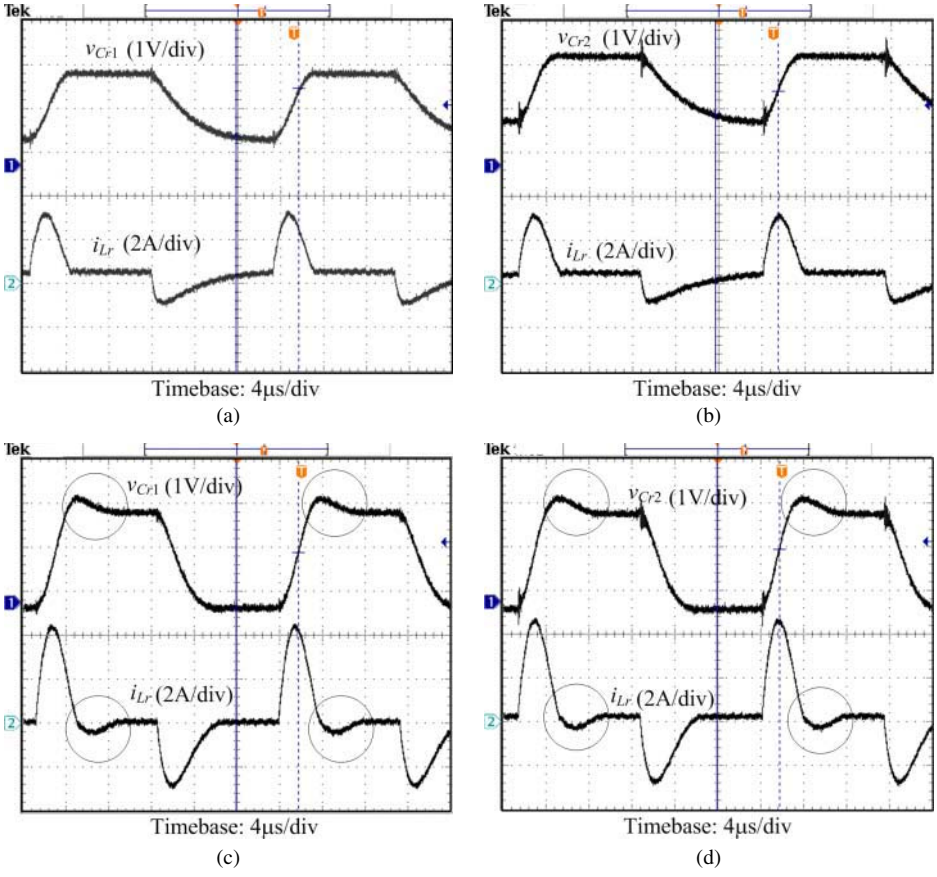


Figure 2.33 Experimental waveforms of a three-order step-up RSC prototype under different load; (a) $R_L = 22\ \Omega$; and (b) $R_L = 8.9\ \Omega$

are shown in Figure 2.33a, which proves that the prototype is working in the normal operating mode.

By reducing the load resistance to $R_L = 8.9\ \Omega$, the sneak circuit phenomena of the prototype can be observed in Figure 2.33b. Because the input power source has certain internal resistance, and the voltage drop of diodes cannot be ignored, there are some differences in stage III′ between experimental waveforms and ideal waveforms.

2.4 Summary

This chapter presented the sneak circuit phenomena in families of RSC converters, and derived the expression of output voltage and the sneak circuit conditions. When the RSC converter is operating in normal mode, the relationship between the input and output voltages are only decided by the converter topology. However, when the sneak circuit appears, the output voltage will be dependent on the circuit parameters and operating conditions, and then the RSC converter will exhibit unexpected behavior. All sneak circuit conditions have been verified by the experimental results, which are useful to restrain the sneak circuit phenomena of RSC converters.

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3

Sneak Circuits of DC-DC Converters

3.1 Introduction

Basic DC-DC converters, such as Buck, Boost, and so on, are generally modeled and analyzed in two distinct operating modes, continuous conduction mode (CCM) and discontinuous conduction mode (DCM), based on the inductor current [1, 2]. In practice, a DC-DC converter is normally designed to operate in one mode to meet certain control functions by selecting the converter parameters (for example, the inductance) in advance. Sometimes the converter will not operate in the desired mode, for example, CCM will switch to DCM, and vice versa. Since the change of operation mode is caused by variation of circuit parameters, such as input voltage, load, or duty ratio, if CCM is regarded as the normal operating mode, then DCM can be considered as the sneak circuit mode of DC-DC converters, according to the definition of the sneak circuit.

In this chapter, six non-isolated DC-DC converters will be analyzed in detail, whereas Sections 3.2–3.4 will study the sneak circuit phenomena and their appearing conditions of the low-order DC-DC converters, which are Buck, Boost, and Buck-boost converters; and Cúk, Sepic, and Zeta converters which belong to the high-order DC-DC converters, will be discussed in Sections 3.6–3.8.

3.2 Buck Converter

3.2.1 CCM of Buck Converter

The schematic diagram of a Buck converter is sketched in Figure 3.1. When a Buck converter operates in CCM, the inductor current flows continuously and is positive. The typical waveforms of switch control signal v_s, inductor current i_L, inductor voltage v_L, and the equivalent circuit of each operating stage are shown in Figure 3.2. During

Sneak Circuits of Power Electronic Converters, First Edition. Bo Zhang and Dongyuan Qiu.

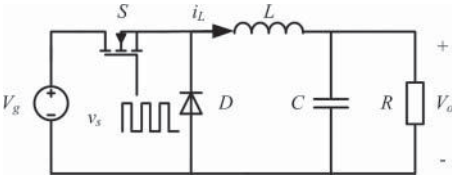


Figure 3.1 Schematic diagram of a Buck converter

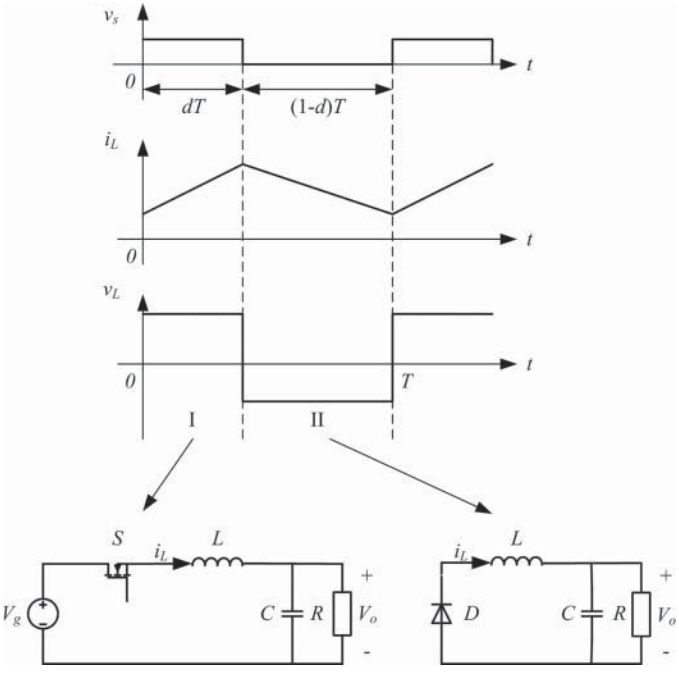


Figure 3.2 Typical waveforms and equivalent circuits of a Buck converter in CCM

the interval when switch S is on, diode D becomes reverse biased, the input voltage source V_g provides energy to load as well as to inductor L, and the inductor voltage satisfies $v_L = V_g - V_o$; During the interval when S is off, the inductor current i_L flows through D, transferring some energy stored in the inductor to the load, and $v_L = -V_o$.

Since the integral of the inductor voltage over one switching period must be zero in the steady state, that is

$$\int_0^T v_L dt = \int_0^{dT} (V_g - V_o)dt + \int_{dT}^T (-V_o)dt = 0 \tag{3.1}$$

Then the average output voltage of the Buck converter is

$$V_o = dV_g \tag{3.2}$$

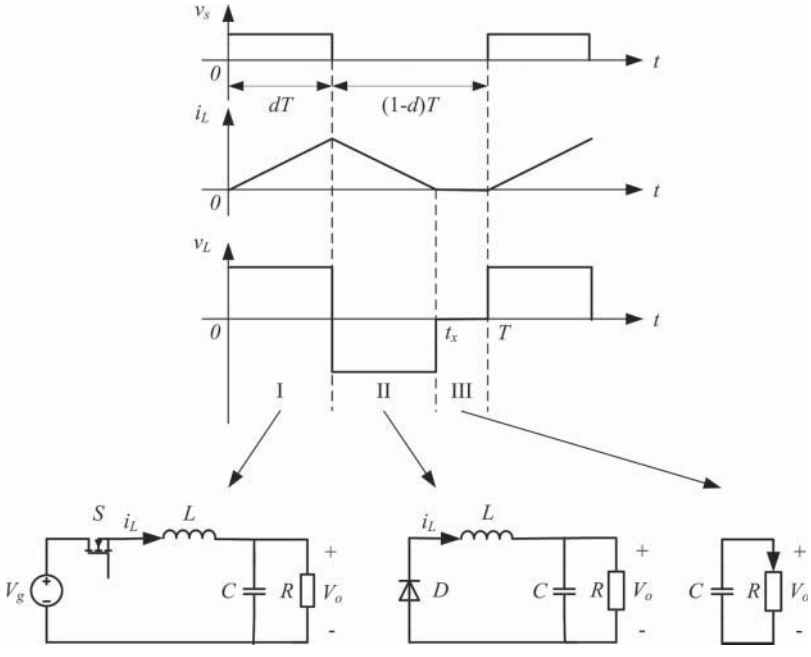


Figure 3.3 Typical waveforms and equivalent circuits of a Buck converter in DCM

where $d = \frac{t_{on}}{T}$ is the duty ratio of switch, t_{on} is the switch-on duration, $T = \frac{1}{f}$ is the switching period, and f is the switching frequency. Therefore, the output voltage varies linearly with the duty ratio of the switch for a given input voltage in CCM, and does not depend on any other circuit parameters.

3.2.2 DCM of Buck Converter

If the inductor current i_L decreases to zero before switch S is turned on, it will result in a discontinuous inductor current; the corresponding waveforms and equivalent circuits are illustrated in Figure 3.3. Comparing Figure 3.3 with Figure 3.2, a new stage, stage III, is added in the converter operation, in which both switch S and diode D are turned off, and the energy to the load resistor is supplied by the output capacitor C alone.

Again, equating the integral of the inductor voltage over one switching period to zero yields

$$\int_0^{dT} (V_g - V_o)dt + \int_{dT}^{t_x} (-V_o)dt = 0 \tag{3.3}$$

where t_x is the time when i_L decreases to zero. The solution of Equation 3.3 is

$$V_o = \frac{dT}{t_x} V_g \tag{3.4}$$

The average inductor current is equal to the average output current I_o, since the average capacitor current is zero in steady state. Then

$$\begin{aligned} I_o = \frac{V_o}{R} &= \frac{1}{T}\left[\int_0^{dT} i_L(t)\,dt + \int_{dT}^{t_x} i_L(t)dt\right] \\ &= \frac{1}{T}\left[\int_0^{dT}\left(\frac{V_g - V_o}{L}t\right)dt + \int_{dT}^{t_x}\left(\frac{V_g}{L}dT - \frac{V_o}{L}t\right)dt\right] \end{aligned} \tag{3.5}$$

Therefore:

$$t_x = \frac{dT + \sqrt{(dT)^2 + \dfrac{8LT}{R}}}{2} \tag{3.6}$$

Substituting Equation 3.6 into Equation 3.4 yields

$$V_o = \frac{2}{1 + \sqrt{1 + \dfrac{8Lf}{d^2R}}}V_g \tag{3.7}$$

It is obviously that the output voltage in DCM depends not only on the duty ratio d, but also other operating condition, such as switching frequency f, load resistance R, and inductance L.

3.2.3 Operating Conditions of Buck Converter

From Figure 3.3, $t_x = T$ is the boundary condition between CCM and DCM, which means that the inductor current i_L decreases to zero at the end of the switch-off period. If t_x is greater than the switching period T, that is, $t_x > T$, then the Buck converter will operate in CCM, and the following equation is satisfied:

$$\frac{R}{2Lf}(1-d) < 1 \tag{3.8}$$

Moreover, the DCM condition of the Buck converter is

$$\frac{R}{2Lf}(1-d) > 1 \tag{3.9}$$

Let $k = \frac{2Lf}{R}$, based on Equations 3.2 and 3.7, so the voltage ratio between input and output voltages of the Buck converter can be concluded as

$$\frac{V_o}{V_g} = \begin{cases} d & (1-d) < k \ \text{ CCM} \\ \dfrac{2d}{d + \sqrt{d^2 + 4k}} & (1-d) > k \ \text{ DCM} \end{cases} \tag{3.10}$$

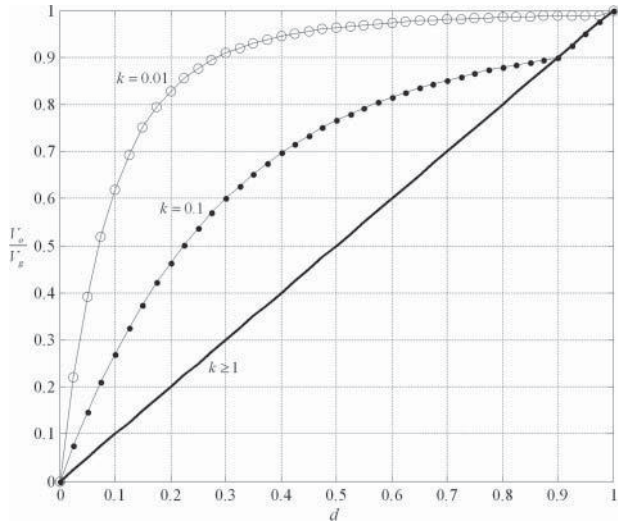


Figure 3.4 Relationship curve of V_o/V_g and duty ratio d of a Buck converter

From Equation 3.10, the Buck converter will operate in CCM, no matter how the duty ratio d changes when $k \geq 1$. Otherwise, when $k < 1$, there are three operating modes, which are:

1. CCM for $1 - d < k < 1$;
2. DCM for $k < 1 - d < 1$; and
3. boundary between DCM and CCM for $k = 1 - d$.

As shown in Figure 3.4, the voltage ratio V_o/V_g is plotted as a function of duty ratio d for various values of k by using Equation 3.10.

Based on the above analysis, the operation mode of the Buck converter will switch between DCM and CCM by varying the values of d, R, L, or f. The circuit path of stage III coincides with the definition of the sneak circuit completely, because it is a current path existing in the converter, and will participate in the circuit operation only when a certain condition (Equation 3.9) is satisfied and causes the output voltage change. Consequently, for a Buck converter, which is set in CCM, DCM can be considered as its sneak circuit mode.

3.3 Boost Converter

3.3.1 CCM of Boost Converter

The schematic diagram of a Boost converter is illustrated in Figure 3.5. When the Boost converter operates in CCM, the corresponding waveforms and equivalent circuits of different operating stages are as illustrated in Figure 3.6. When switch S is

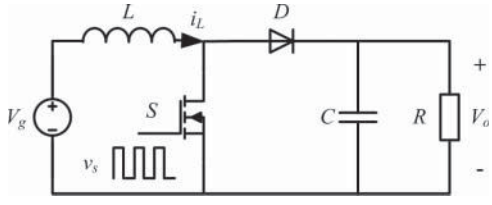


Figure 3.5 Schematic diagram of a Boost converter

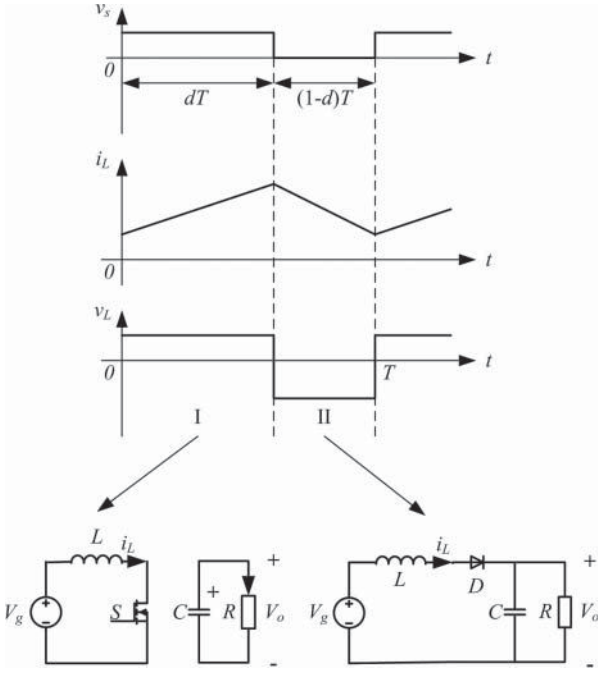


Figure 3.6 Typical waveforms and equivalent circuits of a Boost converter in CCM

turned on, input power source V_g and output capacitor C supply energy to the inductor L and the load resistor R respectively. However, when S is turned off, V_g and L provide energy to the load through diode D simultaneously.

According to the volt-second principle of the inductor, there is

$$\int_0^{dT} V_g dt + \int_{dT}^{T} (V_g - V_o) dt = 0 \tag{3.11}$$

Then the average output voltage of Boost converter in CCM is

$$V_o = \frac{V_g}{1-d} \tag{3.12}$$

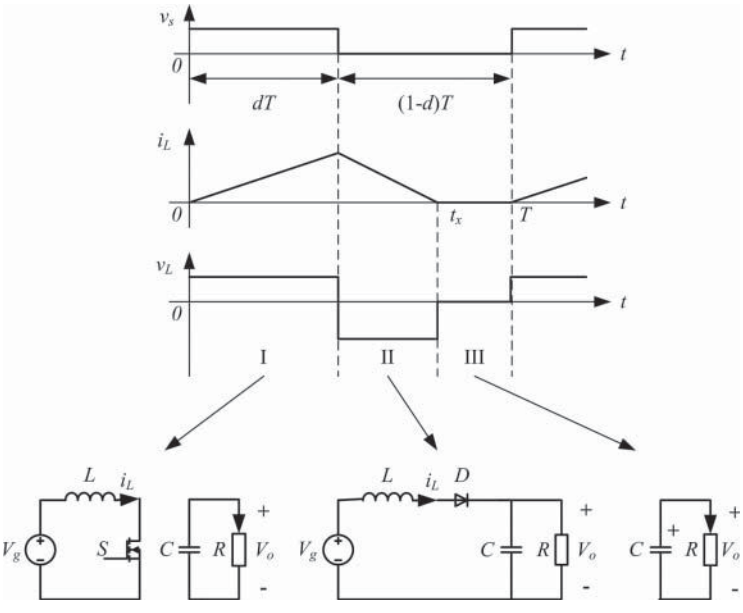


Figure 3.7 Typical waveforms and equivalent circuits of a Boost converter in DCM

3.3.2 DCM of Boost Converter

If the inductor is too small to maintain i_L when S is turned off, then the Boost converter will operate in DCM with a discontinuous inductor current, as shown in Figure 3.7. Compared with CCM (Figure 3.6), stage III in which both switch S and diode D are turned off is added, and meanwhile capacitor C supplies energy to the load resistor R.

According to the volt-second balance of the inductor, the following equation can be obtained

$$\int_0^{dT} V_g dt + \int_{dT}^{t_x} (V_g - V_o) dt = 0 \tag{3.13}$$

where t_x is the time when the inductor current decreases to zero.

The solution for V_o yields

$$V_o = \frac{t_x}{t_x - dT} V_g \tag{3.14}$$

In an ideal situation, the energy supplied by the power source is equal to that consumed by the load resistor in one switching cycle, that is

$$\begin{aligned} \frac{V_o^2}{R} T &= V_g \left[\int_0^{dT} \left(\frac{V_g}{L} t \right) dt + \int_{dT}^{t_x} \left[\frac{V_g}{L} dT - \frac{V_o - V_g}{L} (t - dT) \right] dt \right] \\ &= V_g \left[\int_0^{dT} \left(\frac{V_g}{L} t \right) dt + \int_{dT}^{t_x} \left[\frac{V_g}{L} dT - \frac{V_g dT}{L(t_x - dT)} (t - dT) \right] dt \right] \end{aligned} \tag{3.15}$$

The solution for t_x yields

$$t_x = dT + \frac{L}{Rd} + \sqrt{\frac{2LT}{R} + \left(\frac{L}{Rd}\right)^2} \tag{3.16}$$

Assuming that $k = \frac{2Lf}{R}$, and substituting Equation 3.16 into Equation 3.14, gives the output voltage when the Boost converter operates in DCM, which is

$$V_o = \left(1 + \frac{2d^2}{2d^2 + k + \sqrt{k^2 + 4kd^2}}\right) V_g \tag{3.17}$$

3.3.3 Operating Conditions of Boost Converter

When the Boost converter operates in CCM, t_x should be greater than the switching cycle T, $t_x > T$, therefore the CCM condition of the Boost converter is

$$d(1-d)^2 < k \tag{3.18}$$

Accordingly, the DCM condition of the Boost converter is

$$d(1-d)^2 > k \tag{3.19}$$

The voltage ratio of the Boost converter can be synthesized as

$$\frac{V_o}{V_g} = \begin{cases} \dfrac{1}{1-d} & d(1-d)^2 < k \text{ CCM} \\ 1 + \dfrac{2d^2}{2d^2 + k + \sqrt{k^2 + 4kd^2}} & d(1-d)^2 > k \text{ DCM} \end{cases} \tag{3.20}$$

As the maximum value of $d(1-d)^2$ is 0.148 at $d = 0.33$, the Boost converter will operate in CCM when $k \geq 0.148$. Otherwise, when $k < 0.148$, there are three situations, which are:

1. DCM if $k < d(1-d)^2 < 0.148$;
2. CCM if $d(1-d)^2 < k < 0.148$; and
3. boundary between DCM and CCM, when $k = d(1-d)^2$.

Based on Equation 3.20, the relationship of V_o/V_g and d is sketched in Figure 3.8. As shown in Figure 3.8, the operation mode of the Boost converter can switch between DCM and CCM by varying the value of d, R, L, or f. Similar to the Buck converter, the circuit path of stage III in Figure 3.7 belongs to the sneak circuit path of the Boost converter.

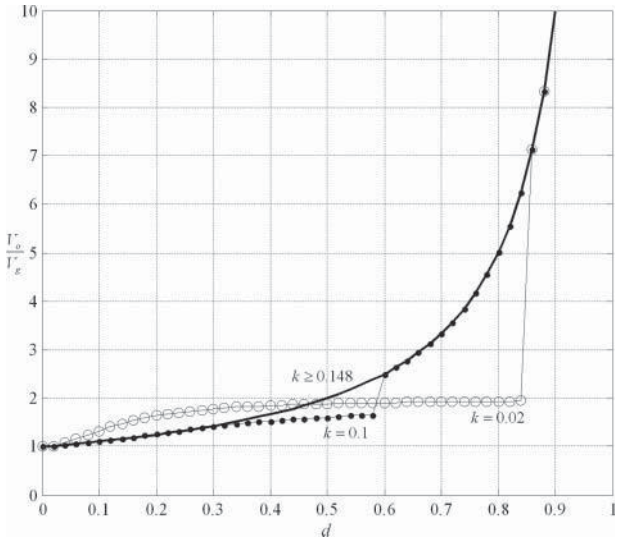


Figure 3.8 Relationship curve of V_o/V_g and duty ratio d of a Boost converter

3.4 Buck-Boost Converter

3.4.1 CCM of Buck-Boost Converter

The schematic diagram of the Buck-boost converter is sketched in Figure 3.9. When the Buck-boost converter operates in CCM with a continuous inductor current, the typical waveforms and equivalent circuits are as shown in Figure 3.10.

When switch S is turned on, inductor L stores energy from the input voltage source V_g and capacitor C supplies energy to the load resistor R respectively. When switch S is turned off, the freewheeling inductor current i_L flows through diode D, then inductor L supplies energy for the load.

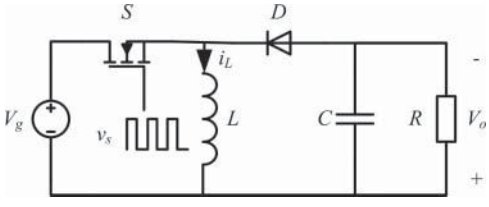


Figure 3.9 Schematic diagram of a Buck-boost converter

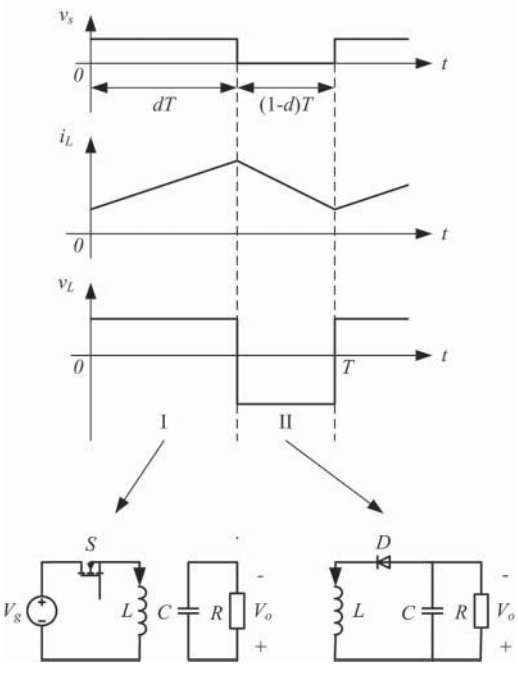


Figure 3.10 Typical waveforms and equivalent circuits of a Buck-boost converter in CCM

According to the volt-second balance principle of the inductor, there is

$$\int_0^{dT} V_g dt + \int_{dT}^{T} (-V_o)\, dt = 0 \tag{3.21}$$

Then we can deduce

$$V_o = \frac{d}{1-d} V_g \tag{3.22}$$

3.4.2 DCM of Buck-Boost Converter

If inductor current i_L decreases to zero before switch S is turned on, the Buck-boost converter will operate in DCM, and the operating waveforms and equivalent circuits are as illustrated in Figure 3.11. Comparing Figure 3.10 with Figure 3.11, in stage III when both S and D are off, only capacitor C supplies energy to the load resistor R.

According to the volt-second balance principle of the inductor, Figure 3.11 illustrates that

$$\int_0^{dT} V_g dt + \int_{dT}^{t_x} (-V_o)\, dt = 0 \tag{3.23}$$

where t_x is the time when the inductor current decreases to zero.

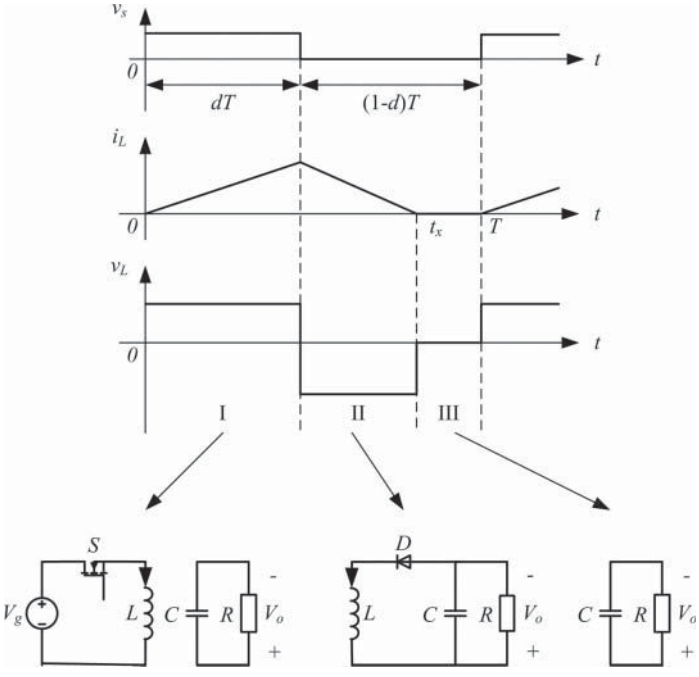


Figure 3.11 Typical waveforms and equivalent circuits of a Buck-boost converter in DCM

The solution of Equation 3.23 for V_o yields

$$V_o = \frac{dT}{t_x - dT} V_g \tag{3.24}$$

According to the principle of energy conservation and the equivalent circuits of the Buck-boost converter, the energy consumed by the load resistor in one switching cycle is supplied by the inductor during the turned-off period, then we obtain

$$V_o \int_{dT}^{t_x} i_L(t)\, dt = \frac{V_o^2}{R} T \tag{3.25}$$

The solution of t_x yields

$$t_x = dT + \sqrt{\frac{2LT}{R}} \tag{3.26}$$

Assuming that $k = \frac{2Lf}{R}$, and substituting Equation 3.26 into Equation 3.24 yields the output voltage when the Buck-boost converter operates in the DCM, that is

$$V_o = \frac{d}{\sqrt{k}} V_g \tag{3.27}$$

3.4.3 Operating Conditions of Buck-Boost Converter

The Buck-boost converter will operate in CCM, when $t_x > T$, or

$$(1-d)^2 < k \tag{3.28}$$

Accordingly,

$$(1-d)^2 > k \tag{3.29}$$

is the DCM condition of the Buck-boost converter.

The voltage ratio of the Buck-boost converter can be summarized as

$$\frac{V_o}{V_g} = \begin{cases} \dfrac{d}{1-d} & (1-d)^2 < k \text{ CCM} \\ \dfrac{d}{\sqrt{k}} & (1-d)^2 > k \quad \text{DCM} \end{cases} \tag{3.30}$$

It is obvious that the operation mode of the Buck-boost converter can switch between DCM and CCM by varying the value of *d, R, L*, and *f*.

When $k \geq 1$, no matter how the duty ratio d changes, the Buck-boost converter will operate in the CCM and the relationship of input and output voltage is only decided by duty ratio d. Otherwise, when $k < 1$, there are three situations, which are:

1. DCM if $k < (1-d)^2 < 1$;
2. CCM if $(1-d)^2 < k < 1$; and
3. boundary between CCM and DCM if $k = (1-d)^2$.

The relationship of V_o/V_g and d based on Equation 3.30 is sketched in Figure 3.12, which proves that the operation mode of the Buck-boost converter can switch between

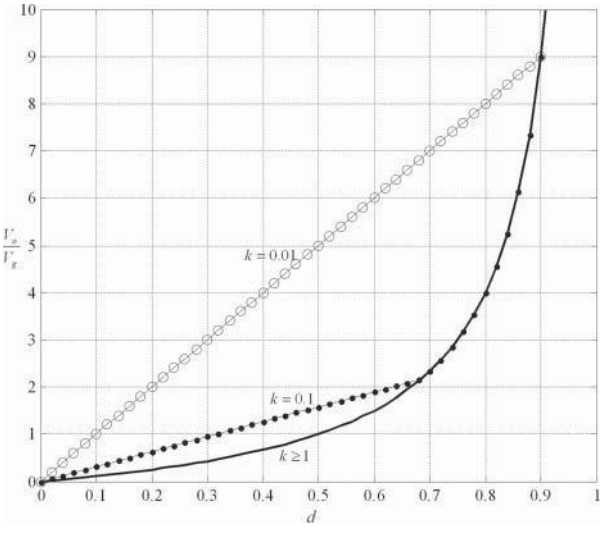


Figure 3.12 Relationship curve of V_o/V_g and duty ratio d of a Buck-boost converter

Table 3.1 Sneak circuit condition and voltage ratio of Buck, Boost, and Buck-boost converters

Converter type	Sneak circuit condition	Input and output voltage ratio V_o/V_g	
		Normal operating mode (CCM)	Sneak circuit mode (DCM)
Buck	$(1-d) > k$	d	$\frac{2d}{d+\sqrt{d^2+4k}}$
Boost	$d(1-d)^2 > k$	$\frac{1}{1-d}$	$1+\frac{2d^2}{2d^2+k+\sqrt{k^2+4kd^2}}$
Buck-boost	$(1-d)^2 > k$	$\frac{d}{1-d}$	$\frac{d}{\sqrt{k}}$

Note: $k = \frac{2Lf}{R}$.

DCM and CCM by varying the value of d and k (i.e., R, L, or f). Similarly, the circuit path in mode III belongs to a sneak circuit path for a Buck-boost converter operating in CCM.

3.5 Sneak Circuit Conditions of Buck, Boost, and Buck-Boost Converters

Synthesizing the above analysis, the sneak circuit conditions and the voltage ratios of Buck, Boost, and Buck-boost converters are summarized in Table 3.1. According to the table, Buck, Boost, or Buck-boost converters can operate in the desired operating mode by choosing appropriate circuit parameters.

3.6 Cúk Converter

3.6.1 Normal Operating Mode of Cúk Converter

A schematic diagram of the Cúk converter is sketched in Figure 3.13. When a Cúk converter operates in its normal operating mode, which means that both inductor

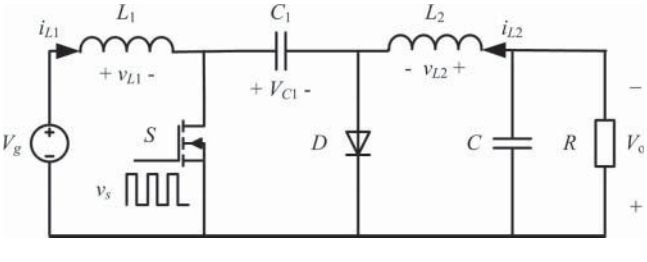


Figure 3.13 Schematic diagram of a Cúk converter

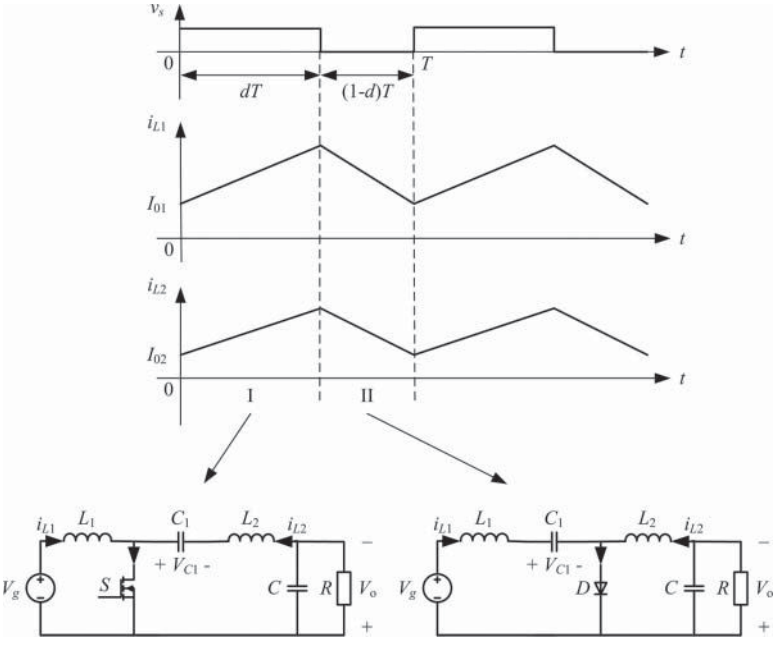


Figure 3.14 Typical waveforms and equivalent circuits of a Cúk converter in normal operating mode

currents are continuous and positive, the corresponding typical waveforms and equivalent circuits are as shown in Figure 3.14.

Referring to Figure 3.14, the operating process of a Cúk converter can be divided into two stages.

Stage I (0, *dT*)

In this stage, switch S is turned on, the inductor current i_{L1} flows through the path L_1-S-V_g, yet the inductor current i_{L2} flows through another path L_2-C_1-S-R(C). At this stage, inductor L_1 stores energy provided by voltage source V_g and capacitor C_1 discharges to inductor L_2 and load simultaneously.

Assuming that the capacitors in the Cúk converter have large capacitance and can be regarded as constant voltage sources, when S is turned on at $t = 0$, $i_{L1} = I_{01} > 0$ and $i_{L2} = I_{02} > 0$ are established in the normal operating mode, then the inductor currents in stage I can be expressed by

$$i_{L1}(t) = \frac{V_g}{L_1}t + I_{01} \tag{3.31}$$

$$i_{L2}(t) = \frac{V_{C1} - V_o}{L_2}t + I_{02} \tag{3.32}$$

Stage II (*dT*, *T*)

At this stage, switch S is turned off and freewheeling diode D is on, i_{L1} flows through the loop L_1-C_1-D-V_g, and i_{L2} flows through the loop L_2-D-$R(C)$. Voltage source V_g and inductor L_1 charge C_1, inductor L_2 supplies energy to load.

Suppose that S is turned off at $t = dT$, based on Equations 3.31 and 3.32, the magnitudes of inductor currents at this moment are $i_{L1}(dT) = \frac{V_g}{L_1}dT + I_{01}$ and $i_{L2}(dT) = \frac{V_{C1}-V_o}{L_2}dT + I_{02}$ respectively. Then the inductor currents at stage II can be expressed as

$$i_{L1}(t) = I_{01} + \frac{V_{C1}}{L_1}dT + \frac{V_g - V_{C1}}{L_1}t \tag{3.33}$$

$$i_{L2}(t) = I_{02} + \frac{V_{C1}}{L_2}dT - \frac{V_o}{L_2}t \tag{3.34}$$

According to the voltage-second balance principle of the inductor, we have the voltage-second balance equations for L_1 and L_2, that is

$$\int_0^{dT} V_g dt + \int_{dT}^{T} (V_g - V_{C1})dt = 0 \tag{3.35}$$

$$\int_0^{dT} V_{C1} - V_o dt + \int_{dT}^{T} (-V_o)dt = 0 \tag{3.36}$$

Based on Equations 3.35 and 3.36, we obtain

$$\begin{cases} V_{C1} = \dfrac{1}{1-d}V_g \\ V_o = \dfrac{d}{1-d}V_g \end{cases} \tag{3.37}$$

Since capacitor and inductor are only energy storing components and do not consume energy in an ideal situation, the energy supplied by the power source is equal to that consumed by the load resistor R in one switching cycle, that is

$$V_g \int_0^T i_{L1}(t)dt = \frac{{V_o}^2}{R}T \tag{3.38}$$

In addition, because inductor L_2 is connected to load in series, the average value of load current is equal to that of i_{L2}, that is

$$\frac{V_o}{R} = \frac{1}{T}\int_0^T i_{L2}(t)\mathrm{d}t \tag{3.39}$$

Combining with the expressions of inductor current and output voltage, and solving Equations 3.38 and 3.39, we obtain

$$I_{01} = \frac{d^2 V_g}{(1-d)^2 R} - \frac{dTV_g}{2L_1} \tag{3.40}$$

$$I_{02} = \frac{dV_g}{(1-d)R} - \frac{dTV_g}{2L_2} \tag{3.41}$$

It is known that $I_{01} > 0$ and $I_{02} > 0$ when the Cúk converter works in normal operating mode, therefore the normal operating condition for Cúk converter is

$$\begin{cases} d > 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d > 1 - 2\beta \end{cases} \tag{3.42}$$

where $\alpha = \frac{L_1 f}{R}$ and $\beta = \frac{L_2 f}{R}$.

3.6.2 Sneak Circuit Phenomena of Cúk Converter

If all of the other operating modes of the Cúk converter, except the normal operating mode shown in Figure 3.14, are regarded as sneak circuit phenomena, there are five kinds of sneak circuit situations in the Cúk converter, according to the inductor current being zero or negative in some of the stages:

1. i_{L2} is always positive and i_{L1} appears negative, and the corresponding waveforms are sketched in Figure 3.15;
2. i_{L1} is always positive and i_{L2} appears negative, and the corresponding waveforms are sketched in Figure 3.16;
3. i_{L2} is always positive, i_{L1} appears negative and satisfies $i_{L1} + i_{L2} = 0$ for some of the time, and the corresponding waveforms are sketched in Figure 3.17;
4. i_{L1} is always positive, i_{L2} appears negative and satisfies $i_{L1} + i_{L2} = 0$ for some of the time, and the corresponding waveforms are sketched in Figure 3.18; and
5. i_{L1} and i_{L2} decrease to zero at the same time, which can be considered as a common DCM, and the corresponding waveforms are sketched in Figure 3.19.

The above five sneak circuit phenomena of a Cúk converter will be analyzed one by one as follows.

3.6.2.1 Sneak Circuit Phenomenon I of Cúk Converter

During the stage when S is turned off and D is turned on, both inductor currents of the Cúk converter decrease. If i_{L1} drops to zero earlier than i_{L2}, and keeps flowing in the negative direction while i_{L2} is still positive, this situation is called sneak circuit

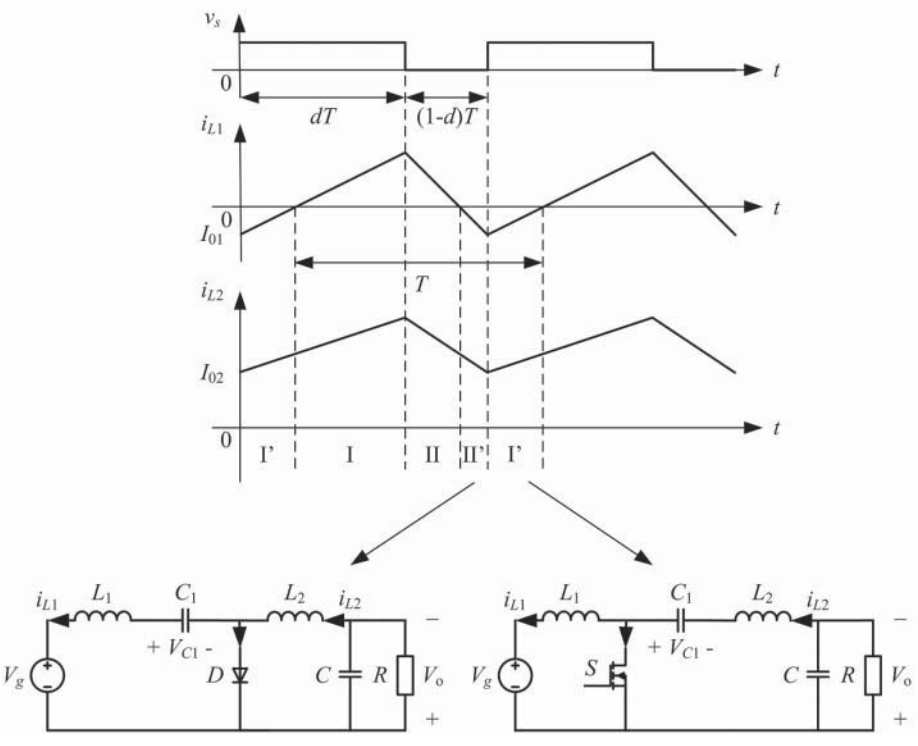


Figure 3.15 Typical waveforms and part of equivalent circuits in a Cúk sneak circuit phenomena I

phenomenon I of the Cúk converter and the resulting waveforms of inductor currents are shown in Figure 3.15. Comparing Figure 3.14 with Figure 3.15, stage I′ and II′ are added in the operating processes of the Cúk converter. As the equivalent circuits of stages I and II are the same as those in the normal operating mode, only the added two stages will be analyzed.

Stage I′

Though $i_{L1} < 0$ and $i_{L2} > 0$ when S is turned on and D is reverse blocking, the equivalent circuit is the same as that of normal stage I and the expressions of two inductor currents are also the same as those of normal stage I, which are Equations 3.31 and 3.32. When i_{L1} increases to greater than zero, the Cúk converter will operate in stage I.

Stage II′

During this stage, S is turned off and D conducts, though $i_{L1} < 0$ and $i_{L2} > 0$, and the equivalent circuit of this stage is still the same as that of stage II. Therefore, the expressions of the two inductor currents are Equations 3.33 and 3.34 of stage II in normal operation.

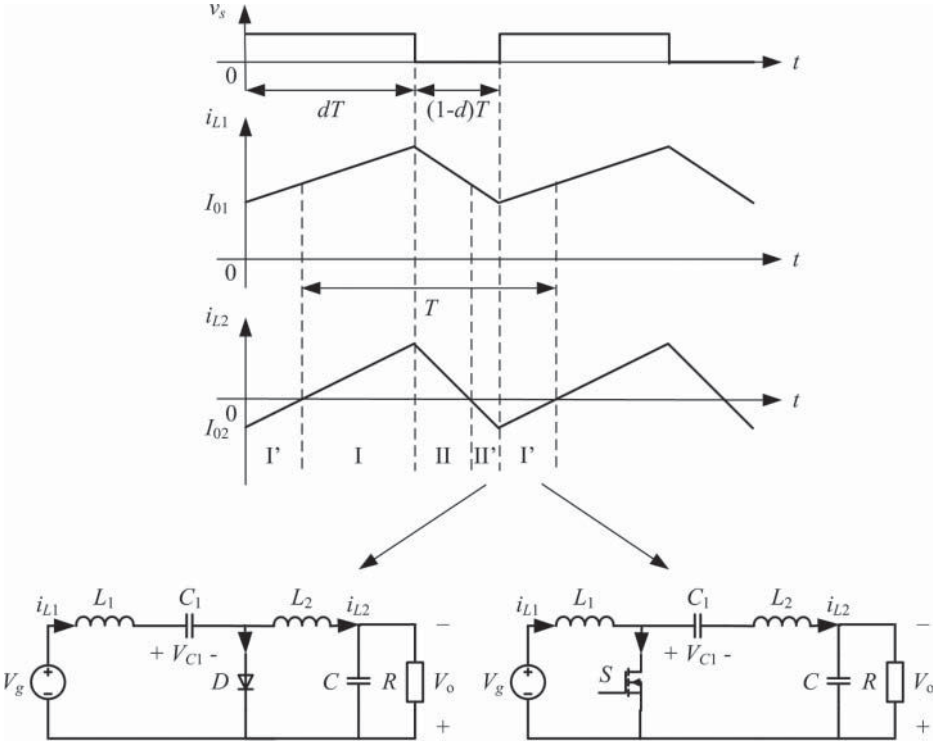


Figure 3.16 Typical waveforms and part of equivalent circuits in a Cúk sneak circuit phenomenon II

According to the inductor's volt-second balance principle and the inductor current expressions, (Equations 3.31–3.34), the output voltage of sneak circuit phenomena I is equal to that of normal operation, that is $V_o = \frac{d}{1-d} V_g$.

When the Cúk converter operates in sneak circuit phenomenon I, it is known that $I_{01} < 0$, $I_{02} > 0$ and $|I_{01}| < |I_{02}|$. Therefore, based on the expressions of I_{01} and I_{02}, that is, Equations 3.40 and 3.41, the resulting condition of sneak circuit phenomenon I yields

$$\begin{cases} d < 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d > 1 - 2\beta \\ d > 1 - \lambda \end{cases} \tag{3.43}$$

where $\lambda = \sqrt{\frac{2L_1 L_2 f}{R(L_1+L_2)}}$.

3.6.2.2 Sneak Circuit Phenomenon II of Cúk Converter

During the stage when S is turned off and D is on, if i_{L2} drops to zero earlier than i_{L1} and then becomes negative while i_{L1} is still larger than zero, then another sneak circuit phenomenon II appears. The typical waveforms of inductor currents in sneak

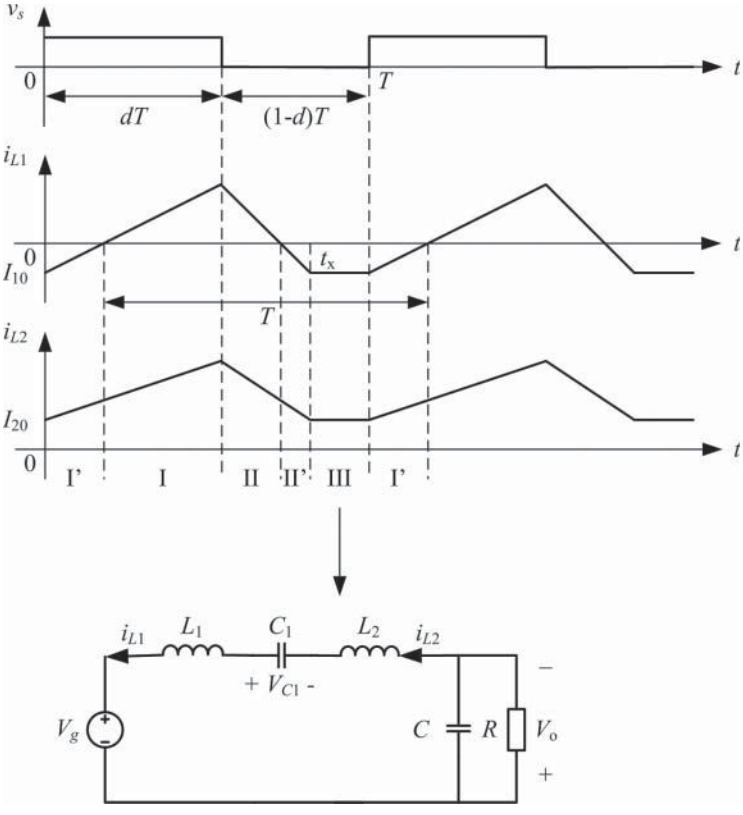


Figure 3.17 Typical waveforms and equivalent circuit of stage III in a Cúk sneak circuit phenomenon III

circuit phenomenon II are sketched in Figure 3.16; obviously, the equivalent circuits of stages I and II are the same as those of normal operating mode in Figure 3.14, while the equivalent circuits of stages I′ and II′ are the same as those of sneak circuit phenomenon I in Figure 3.15.

Similar to the analysis process of sneak circuit phenomenon I, the output voltage of sneak circuit phenomenon II is $V_o = \frac{d}{1-d} V_g$. According to $I_{01} > 0, I_{02} < 0$, and $|I_{01}| > |I_{02}|$, the resulting condition of sneak circuit phenomenon II can be obtained by

$$\begin{cases} d > 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d < 1 - 2\beta \\ d > 1 - \lambda \end{cases} \tag{3.44}$$

3.6.2.3 Sneak Circuit Phenomenon III of Cúk Converter

It is known that both i_{L1} and i_{L2} decrease when S is off and D is on, assuming that i_{L1} drops to zero earlier than i_{L2} and becomes negative while i_{L2} is still greater than zero;

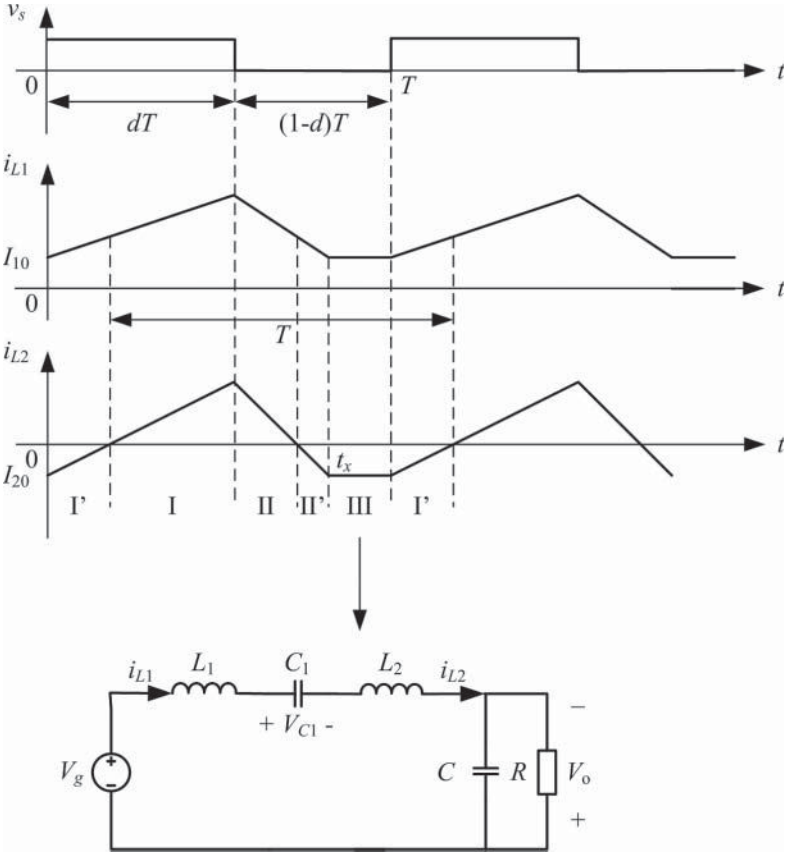


Figure 3.18 Typical waveforms and equivalent circuit of stage III in a Cúk sneak circuit phenomenon IV

if $i_{L1} + i_{L2} = 0$ is satisfied at the moment $t = t_x$, D will be shut down. Since both S and D are in an off-state, the inductor current remains at $i_{L2} = -i_{L1} > 0$, which means that C_1 and load feed back energy to the power source. This situation is called sneak circuit phenomenon III, and the typical waveforms are sketched in Figure 3.17. Compared with sneak circuit phenomenon I, a new stage III is added, which represents both S and D being off at the same time.

Since $i_{L1} = -i_{L2}$, the inductor voltages of stage III when $t \in (t_x, T)$ are

$$v_{L1}(t) = \frac{L_1}{L_1 + L_2}(-V_{C1} + V_g + V_o) \tag{3.45}$$

$$v_{L2}(t) = \frac{L_2}{L_1 + L_2}(V_{C1} - V_g - V_o) \tag{3.46}$$

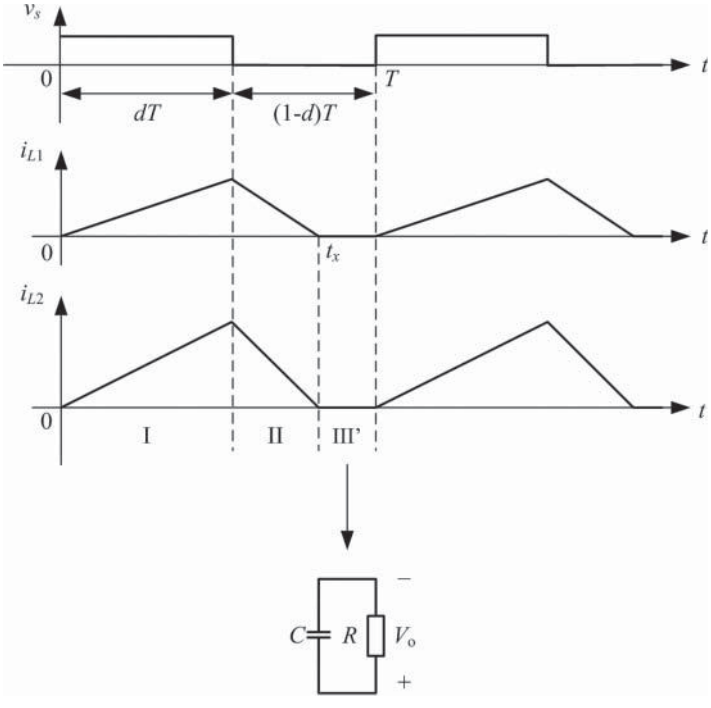


Figure 3.19 Typical waveforms and equivalent circuit of stage III′ in a Cúk sneak circuit phenomenon V

According to the inductor voltage-second balance principle, the inductor voltages of L_1 and L_2 satisfy the following equations respectively:

$$\int_0^{dT} V_g dt + \int_{dT}^{t_x} (V_g - V_{C1}) dt + \int_{t_x}^{T} \frac{L_1(-V_{C1} + V_g + V_o)}{L_1 + L_2} dt = 0 \tag{3.47}$$

$$\int_0^{dT} (V_{C1} - V_o) dt + \int_{dT}^{t_x} (-V_0) dt + \int_{t_x}^{T} \frac{L_2(V_{C1} - V_g - V_o)}{L_1 + L_2} dt = 0 \tag{3.48}$$

Solving these equations yields

$$\begin{cases} V_{C1} = \dfrac{t_x}{t_x - dT} V_g \\ V_o = \dfrac{dT}{t_x - dT} V_g \end{cases} \tag{3.49}$$

Substituting Equation 3.49 into Equations 3.45 and 3.46, $v_{L1} = v_{L2} = 0$ can be deduced. Therefore, i_{L1} and i_{L2} will keep constant in stage III, and $I_{01} = -I_{02} = I_0$ is established.

According to the capacitor ampere-second balance principle, the current flowing through capacitance C_1 meets the following:

$$-\int_0^{dT} i_{L2}(t)dt + \int_{dT}^{t_x} i_{L1}(t)dt + \int_{t_x}^{T} I_0 dt = 0 \tag{3.50}$$

For the energy supplied by L_2 to be equal to that consumed by the load resistor R in one switching cycle, there is

$$V_o \int_0^T i_{L2}(t)\mathrm{d}t = \frac{{V_o}^2}{R} T \tag{3.51}$$

Substituting Equations 3.31–3.34 into Equations 3.50 and 3.51, we have

$$\begin{cases} t_x = dT + \lambda T \\ I_0 = -\dfrac{V_g d\lambda T}{2L_1} + \dfrac{V_g d^2 T}{2L_2} \end{cases} \tag{3.52}$$

Since $I_0 < 0$ and $t_x < T$ are satisfied in sneak circuit phenomenon III, the resulting condition of sneak circuit phenomenon III is

$$\begin{cases} d < \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.53}$$

and the output voltage is

$$V_o = \frac{d}{\lambda} V_g \tag{3.54}$$

3.6.2.4 Sneak Circuit Phenomenon IV of Cúk Converter

If inductor current i_{L2} becomes negative while i_{L1} is still larger than zero, and $i_{L1} + i_{L2} = 0$ is satisfied, the situation is called sneak circuit phenomenon IV, and the typical waveforms are sketched in Figure 3.18.

Similar to the analysis of sneak circuit phenomenon III, the output voltage of the Cúk converter operating in sneak circuit phenomenon IV is $V_o = \frac{d}{\lambda} V_g$. According to $I_0 > 0$ and $t_x < T$, the resulting condition of sneak circuit phenomenon IV is

$$\begin{cases} d > \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.55}$$

3.6.2.5 Sneak Circuit Phenomenon V of Cúk Converter

If i_{L1} and i_{L2} decrease to zero at the same time, then D will be shut down. Since $i_{L1} = i_{L2} = 0$ at this time, a new stage III′ appears in which the capacitor C provides energy for load resistor R. This situation is called sneak circuit phenomenon V, which looks like the traditional DCM of inductor currents, and the typical waveforms are sketched in Figure 3.19.

Since the average value of inductor current i_{L2} is equal to that of the load current, the following equation can be deduced:

$$\frac{V_o}{R} = \frac{1}{T}\int_0^{t_x} i_{L2}(t)dt \tag{3.56}$$

If $I_{02} = 0$, the expression of i_{L2} is

$$i_{L2}(t) = \begin{cases} \dfrac{V_{C1} - V_o}{L_2}t & 0 < t \le dT \\ \dfrac{V_{C1}}{L_2}dT - \dfrac{V_o}{L_2}t & dT < t \le t_x \\ 0 & t_x < t \le T \end{cases} \tag{3.57}$$

As sneak circuit phenomenon V is the special situation of phenomenon III or IV with $I_0 = 0$, the output voltage of sneak circuit phenomenon V is $V_o = \frac{dT}{t_x - dT}V_g$, then substituting Equation 3.57 into Equation 3.56, we obtain

$$t_x = \frac{dT}{2} + \sqrt{\left(\frac{dT}{2}\right)^2 + \frac{2L_2T}{R}} \tag{3.58}$$

and the resulting condition of sneak circuit phenomenon V is

$$\begin{cases} d = \lambda\dfrac{L_2}{L_1} = \lambda\dfrac{\beta}{\alpha} \\ d < 1 - \lambda \end{cases} \tag{3.59}$$

Therefore, the output voltage can be simplified as

$$V_o = \frac{L_2}{L_1}V_g = \frac{d}{\lambda}V_g \tag{3.60}$$

3.6.3 Experimental Verification of Cúk Converter

A Cúk prototype based on Figure 3.13 was built to verify the sneak circuit phenomena. The parameters of the prototype were $V_g = 12$V, $f = 100$ kHz, $L_1 = 440$ μH, $L_2 = 120$ μH, $C_1 = 330$ μF, $C = 180$ μF, and $R = 50$ Ω. Then $\alpha = \frac{L_1 f}{R} = 0.88$, $\beta = \frac{L_2 f}{R} = 0.24$, and $\lambda = \sqrt{\frac{2L_1L_2f}{R(L_1+L_2)}} = 0.614$ could be obtained. According to the above analysis,

the range of duty ratio d in different operating modes of the Cúk converter can be obtained:

1. $d > 0.52$, normal operating mode (CCM), $V_o = \dfrac{d}{1-d}V_g$;
2. $0.386 < d < 0.52$, sneak circuit phenomenon II, $V_o = \dfrac{d}{1-d}V_g$;
3. $0.167 < d < 0.386$, sneak circuit phenomenon IV, $V_o = \dfrac{d}{\lambda}V_g$;
4. $d = 0.167$, sneak circuit phenomenon V (DCM), $V_o = \dfrac{L_2}{L_1}V_g$;
5. $d < 0.167$, sneak circuit phenomenon III, $V_o = \dfrac{d}{\lambda}V_g$.

It is noted that sneak circuit phenomenon I will not appear, because the corresponding condition cannot be satisfied. To set different duty ratio d to make the Cúk converter work in different operating modes, when $d = 0.54$, the prototype should work in normal operating mode and the output voltage should be $V_o = \frac{d}{1-d}V_g = 14.1$ V. The experimental waveforms of driving signal v_s, output voltage V_o, inductor currents i_{L1}, and i_{L2} are shown in Figure 3.20a. Both i_{L1} and i_{L2} are positive as desired, and the output voltage $V_o \approx 14$ V. When $d = 0.23$, the prototype should operate in sneak circuit phenomenon IV, and the output voltage should be $V_o = \frac{d}{\lambda}V_g = 4.5$ V, and the experimental waveforms under $d = 0.23$ are shown in Figure 3.20b, in which i_{L1} is always positive and i_{L2} appears negative and satisfies $i_{L1} + i_{L2} = 0$. When $d = 0.167$, the prototype should operate in sneak circuit phenomenon V (DCM) and output voltage should be $V_o = 3.2$ V. The experimental waveform in Figure 3.20c shows that i_{L1} and i_{L2} decrease to zero at the same time. When $d = 0.075$, the prototype should operate in sneak circuit phenomenon III, and the output voltage should be $V_o = 1.46$ V. The experimental waveforms in Figure 3.20d show that i_{L2} is always positive, i_{L1} appears negative and satisfies $i_{L1} + i_{L2} = 0$. From the above analysis, the experimental results coincide with theoretical analysis, therefore the sneak circuit phenomena of the Cúk converter and corresponding conditions have been verified.

If keeping the duty ratio $d = 0.54$ constant and varying the load resistance R, the Cúk prototype will also work in different operational modes. When $R = 50\ \Omega$, as shown in Figure 3.20a, then $d = 0.54$ belongs to the range of the normal operating mode; when $R = 75\ \Omega$, accordingly $\alpha = \frac{L_1 f}{R} = 0.587$, $\beta = \frac{L_2 f}{R} = 0.16$, and $\lambda = \sqrt{\frac{2\alpha\beta}{\alpha+\beta}} = 0.501$, then $d = 0.54$ is in the range of sneak circuit phenomenon II ($0.499 < d < 0.68$), and the experimental waveforms in Figure 3.21a illustrate that i_{L1} is always positive and part of i_{L2} becomes negative; When $R = 492\ \Omega$, accordingly $\alpha = \frac{L_1 f}{R} = 0.089$, $\beta = \frac{L_2 f}{R} = 0.024$, and $\lambda = \sqrt{\frac{2\alpha\beta}{\alpha+\beta}} = 0.194$, then $d = 0.54$ is in the range of sneak circuit phenomenon IV ($0.052 < d < 0.806$), and the experimental waveforms are shown in Figure 3.21b, in which i_{L1} is always positive, i_{L2} appears negative, and $i_{L1} + i_{L2} = 0$ are satisfied some of the time. The above experimental results demonstrate that the Cúk converter will operate in abnormal operating mode by varying some parameters, that is, the sneak circuit phenomenon will appear.

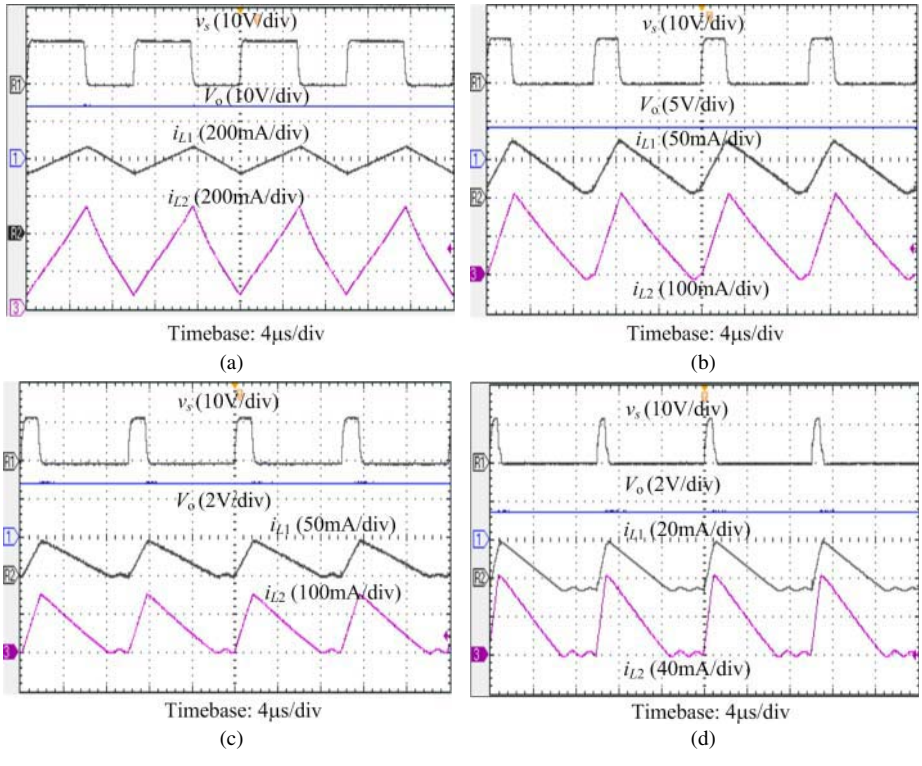


Figure 3.20 Experimental waveforms of a Cúk converter under different duty ratio: (a) $d = 0.54$, normal operating mode; (b) $d = 0.23$, sneak circuit phenomenon IV; (c) $d = 0.167$, sneak circuit phenomenon V (DCM); and (d) $d = 0.075$, sneak circuit phenomenon III

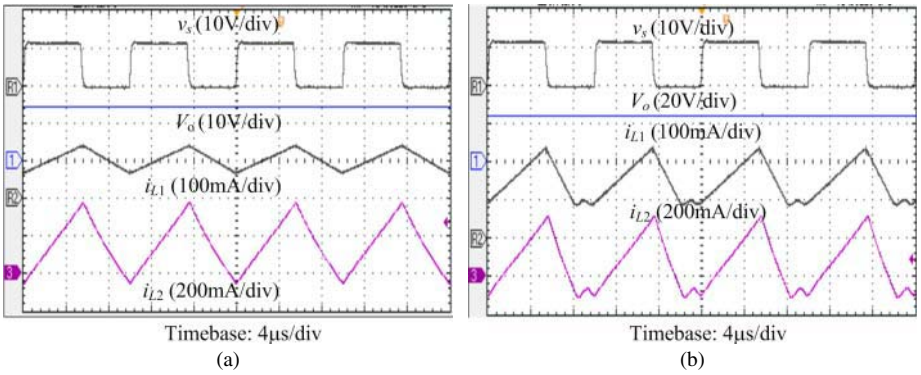


Figure 3.21 Experimental waveforms of a Cúk converter under different load: (a) $R = 75\ \Omega$, sneak circuit phenomenon II and (b) $R = 492\ \Omega$, sneak circuit phenomenon IV

3.7 Sepic Converter

The schematic diagram of a Sepic converter is sketched in Figure 3.22. Similar to analysis of the Cúk converter, the Sepic converter has six modes of operation:

1. *Normal operating mode*: both inductor currents i_{L1} and i_{L2} are constantly positive, as shown in Figure 3.23;
2. *Sneak circuit phenomenon I*: i_{L2} is constantly positive, but i_{L1} appears negative, as shown in Figure 3.24;
3. *Sneak circuit phenomenon II*: i_{L1} is constantly positive, but i_{L2} appears negative, as shown in Figure 3.25;
4. *Sneak circuit phenomenon III*: i_{L2} is always positive, i_{L1} appears negative, and satisfies $i_{L1} + i_{L2} = 0$ for some of the time, as shown in Figure 3.26;
5. *Sneak circuit phenomenon IV*: i_{L1} is constantly positive, i_{L2} appears negative, and satisfies $i_{L1} + i_{L2} = 0$ for some of the time, as shown in Figure 3.27;
6. *Sneak circuit phenomenon V*: i_{L1} and i_{L2} decrease to zero at the same time, that is, DCM, as shown in Figure 3.28.

The characteristic and resulting condition of the Sepic converter in each operating mode are analyzed as follows.

3.7.1 Normal Operating Mode of Sepic Converter

As shown in Figure 3.23, the operating process of a Sepic converter in normal operating mode can be divided into two stages.

Stage I (0, *dT*)

In stage I, switch *S* is turned on, the inductor current i_{L1} flows through the loop V_g-L_1-*S*, while the input voltage source supplies energy for inductor L_1. The inductor current i_{L2} flows through the loop C_1-*S*-L_2, and it is capacitor C_1 which supplies energy for inductor L_2. However, diode *D* is turned off bearing reverse voltage and output capacitor *C* discharges to load resistor *R*.

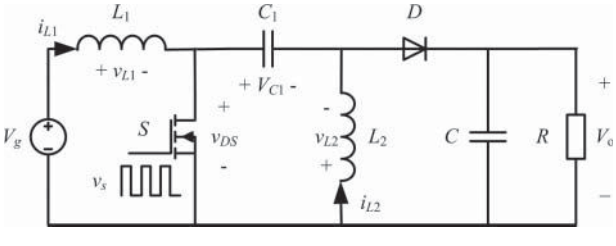


Figure 3.22 Schematic diagram of a Sepic converter

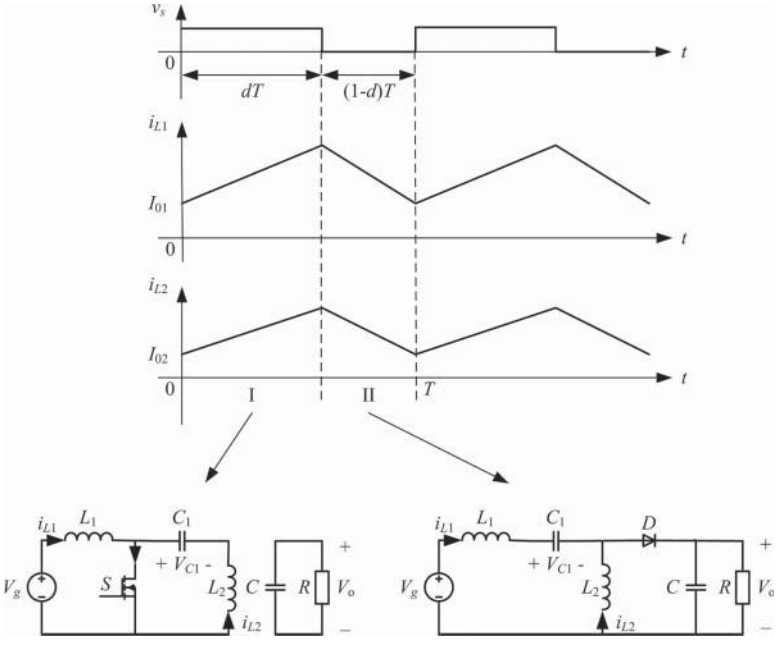


Figure 3.23 Typical waveforms and equivalent circuits of a Sepic converter in normal operating mode

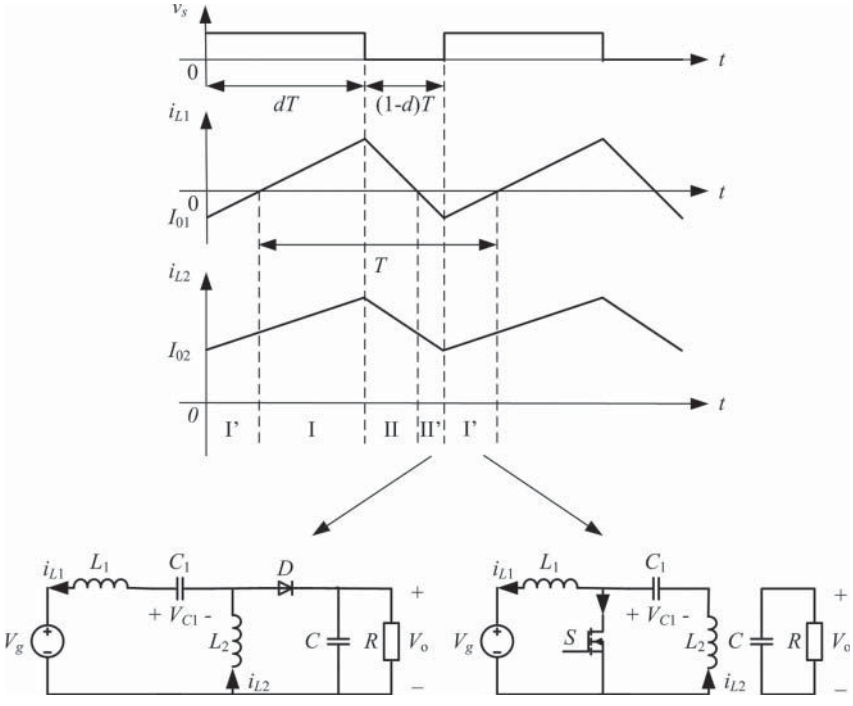


Figure 3.24 Typical waveforms and part of the equivalent circuits in Sepic sneak circuit phenomenon I

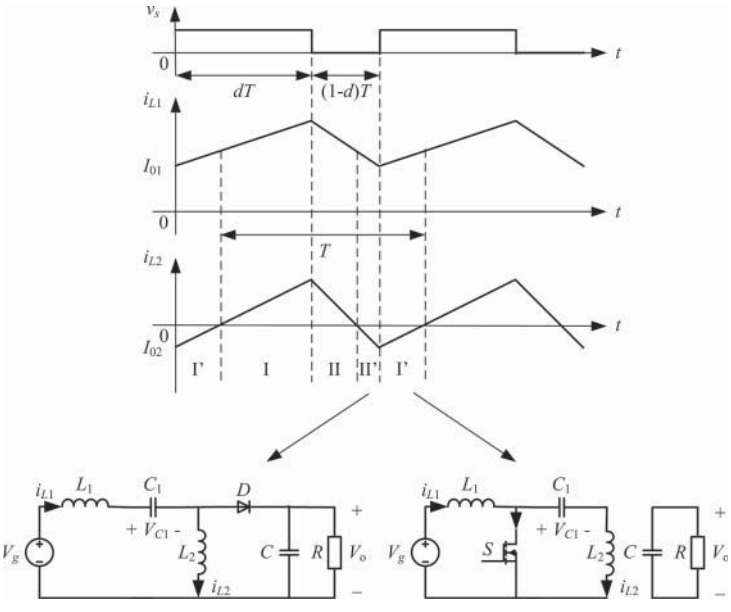


Figure 3.25 Typical waveforms and part of equivalent circuits in Sepic sneak circuit phenomenon II

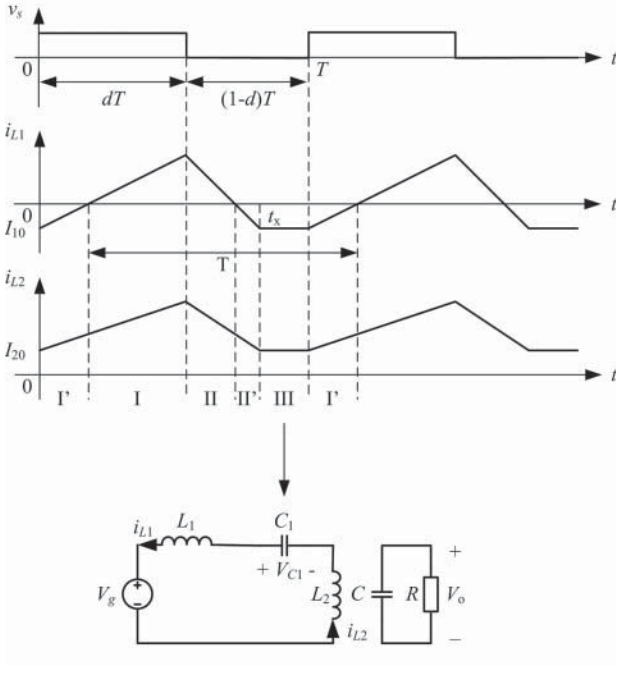


Figure 3.26 Typical waveforms and part of equivalent circuits in Sepic sneak circuit phenomenon III

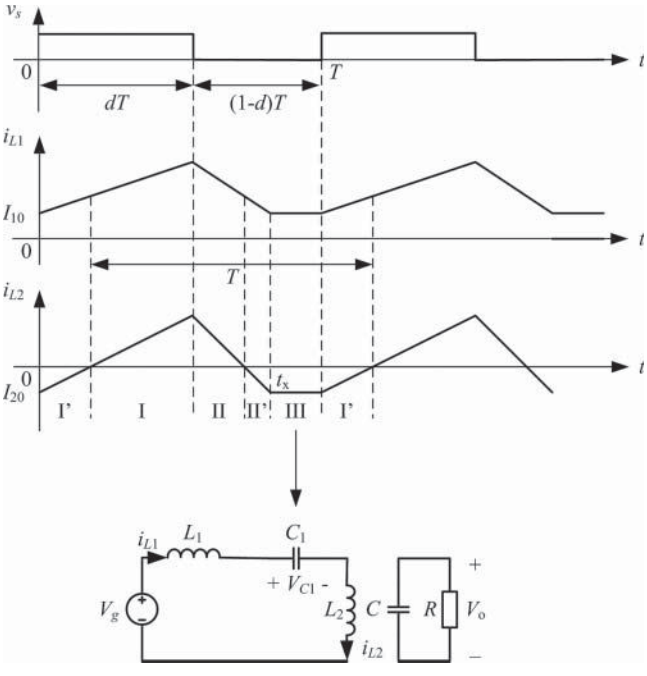


Figure 3.27 Typical waveforms and part of equivalent circuits in Sepic sneak circuit phenomenon IV

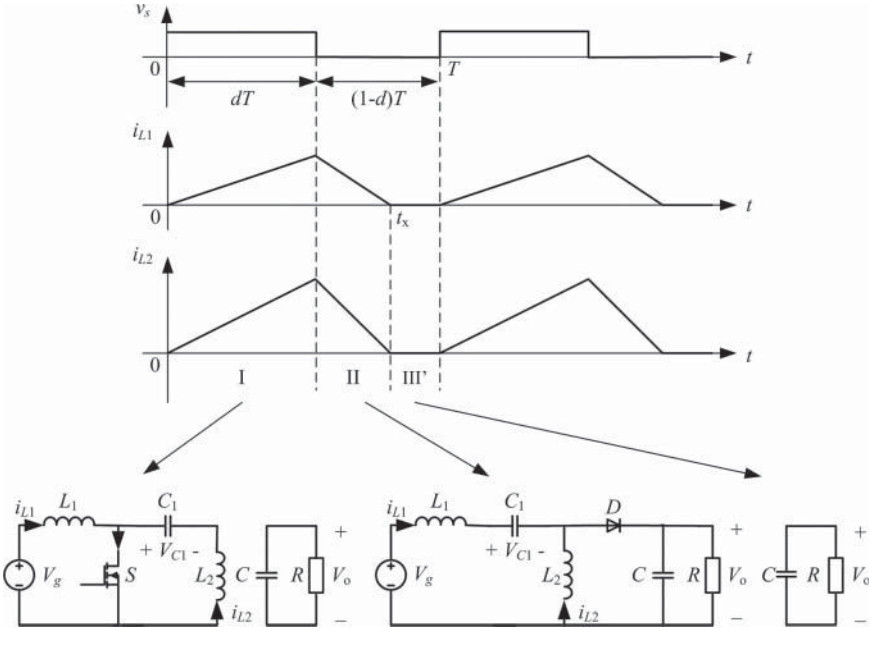


Figure 3.28 Typical waveforms and equivalent circuits in Sepic sneak circuit phenomenon V

Assuming that the capacitances are large enough and the capacitors can be regarded as constant voltage sources, the initial values of i_{L1} and i_{L2} at $t = 0$ are I_{01} and I_{02} respectively. At this stage, the inductor currents can be expressed as

$$i_{L1}(t) = \frac{V_g}{L_1}t + I_{01} \tag{3.61}$$

$$i_{L2}(t) = \frac{V_{C1}}{L_2}t + I_{02} \tag{3.62}$$

Stage II (*dT*, *T*)

In stage II, switch S is turned off and diode D is turned on, then i_{L1} flows through the loop V_g-L_1-C_1-D-$R(C)$ and i_{L2} flows through the loop L_2-D-$R(C)$. In this stage, the input voltage source and inductor L_1 charge capacitor C_1 at the same time, while the input voltage source, inductors L_1 and L_2, supply energy for the load, and the inductor currents can be expressed as

$$i_{L1}(t) = \frac{V_g}{L_1}dT + I_{01} + \frac{V_g - V_{C1} - V_o}{L_1}(t - dT) \tag{3.63}$$

$$i_{L2}(t) = \frac{V_{C1}}{L_2}dT + I_{02} - \frac{V_o}{L_2}(t - dT) \tag{3.64}$$

According to the inductor voltage-second balance principle, the inductor voltages satisfy the following:

$$\int_0^{dT} V_g dt + \int_{dT}^{T} (V_g - V_{C1} - V_o)dt = 0 \tag{3.65}$$

$$\int_0^{dT} V_{C1} dt + \int_{dT}^{T} (-V_o)dt = 0 \tag{3.66}$$

Solving the above equations, we obtain

$$\begin{cases} V_{C1} = V_g \\ V_o = \dfrac{d}{1-d}V_g \end{cases} \tag{3.67}$$

As capacitor and inductor do not consume energy and only store energy in the ideal case, the energy supplied by the input voltage source is equal to that consumed by the load resistor in one switching cycle, that is

$$V_g \int_0^{T} i_{L1}(t)dt = \frac{{V_o}^2}{R}T \tag{3.68}$$

In addition, since inductors L_1 and L_2 supply energy for the load only in stage II, the average value of load current is

$$\frac{V_o}{R} = \frac{1}{T}\int_{dT}^{T} [i_{L1}(t) + i_{L2}(t)]dt \tag{3.69}$$

Combining the expressions of inductor current and output voltage, based on Equations 3.65 and 3.66, we obtain

$$I_{01} = \frac{d^2 V_g}{(1-d)^2 R} - \frac{dTV_g}{2L_1} \tag{3.70}$$

$$I_{02} = \frac{dV_g}{(1-d)R} - \frac{dTV_g}{2L_2} \tag{3.71}$$

When a Sepic converter operates in normal mode, there must be $I_{01} > 0$ and $I_{02} > 0$. Therefore the normal operating condition for a Sepic converter is

$$\begin{cases} d > 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d > 1 - 2\beta \end{cases} \tag{3.72}$$

where $\alpha = \frac{L_1 f}{R}$ and $\beta = \frac{L_2 f}{R}$.

3.7.2 Sneak Circuit Phenomena of Sepic Converter

Because the sneak circuit operating modes of a Sepic converter are similar to those of a Cúk converter, this section will not describe each sneak circuit phenomenon of the Sepic converter in detail. Only the typical operating waveform, equivalent circuit, and the resulting condition will be provided.

3.7.2.1 Sneak Circuit Phenomenon I of Sepic Converter

According to Figure 3.24, when a Sepic converter works in sneak circuit phenomenon I, i_{L1} appears negative and then two new stages I′ and II′ are added. However, the actual operating process of stage I′ is the same as that of normal operating stage I, except the current direction of i_{L1}, and stage II′ is similar to stage II. Therefore, the value of output voltage is still $V_o = \frac{dV_g}{1-d}$.

As we know, $I_{01} < 0$, $I_{02} > 0$ in sneak circuit phenomenon I of a Sepic converter. Moreover, when $i_{L1} < 0$, S or D should be kept on, then $|I_{01}| < |I_{02}|$. Based on the expressions of I_{01} and I_{02}, that is, Equations 3.70 and 3.71, the resulting condition of sneak circuit phenomenon I is

$$\begin{cases} d < 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d > 1 - 2\beta \\ d > 1 - \lambda \end{cases} \tag{3.73}$$

where $\lambda = \sqrt{\frac{2L_1 L_2 f}{R(L_1+L_2)}}$.

3.7.2.2 Sneak Circuit Phenomenon II of Sepic Converter

The typical waveforms of a Sepic converter in sneak circuit phenomenon II are shown in Figure 3.25. Similar to analysis of sneak circuit phenomenon I, the output voltage of sneak circuit phenomenon II equates to $V_o = \frac{d}{1-d}V_g$, and the resulting condition is

$$\begin{cases} d > 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d < 1 - 2\beta \\ d > 1 - \lambda \end{cases} \tag{3.74}$$

3.7.2.3 Sneak Circuit Phenomenon III of Sepic Converter

As shown in Figure 3.26, when a Sepic converter works in sneak circuit phenomenon III, a new stage III is added by comparing with the sneak circuit phenomenon I.

In stage III, since $i_{L1} + i_{L2} = 0$, both S and D are turned off. According to the equivalent circuit of stage III, i_{L1} and i_{L2} keep constant and $I_{01} = -I_{02} = I_0 < 0$. Assume that the Sepic converter enters stage III when $t = t_x$. According to the inductor voltage-second balance principle, the expressions of output voltage and capacitor voltage in sneak circuit phenomenon III are

$$\begin{cases} V_o = \dfrac{dTV_g}{t_x - dT} \\ V_{C1} = V_g \end{cases} \tag{3.75}$$

Combining the inductor current expressions in each operating stage with the energy conservation principle, the following equations can be obtained:

$$\begin{cases} t_x = dT + \lambda T \\ I_0 = -\dfrac{V_g d\lambda T}{2L_1} + \dfrac{V_g d^2 T}{2L_2} \end{cases} \tag{3.76}$$

From Figure 3.26, there must be $I_0 < 0$ and $t_x < T$ when a Sepic converter works in sneak circuit phenomenon III. Therefore, the resulting condition of sneak circuit phenomenon III is

$$\begin{cases} d < \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.77}$$

and the corresponding output voltage is

$$V_o = \frac{d}{\lambda} V_g \tag{3.78}$$

3.7.2.4 Sneak Circuit Phenomenon IV of Sepic Converter

Comparing Figure 3.27 with Figure 3.26, the sneak circuit phenomenon IV of a Sepic converter is similar to the sneak circuit phenomenon III. Therefore, the output voltage in sneak circuit phenomenon IV is still $V_o = \frac{d}{\lambda} V_g$. Since $I_{01} = -I_{02} = I_0 > 0$ in this case, the resulting condition of sneak circuit phenomenon IV is

$$\begin{cases} d > \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.79}$$

3.7.2.5 Sneak Circuit Phenomenon V of Sepic Converter

As shown in Figure 3.28, the sneak circuit phenomenon V of a Sepic converter can be regarded as the special situation of sneak circuit phenomena III and IV when $I_0 = 0$. Therefore, the resulting condition of sneak circuit phenomenon V is

$$\begin{cases} d = \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.80}$$

and the output voltage of sneak circuit phenomenon V equates to $V_o = \frac{d}{\lambda} V_g = \frac{L_2}{L_1} V_g$ based on Equation 3.80.

3.7.3 Experimental Verification of Sepic Converter

Referring to Figure 3.22, a Sepic prototype was built to verify different operating mode of the Sepic converter, and the parameters and operation conditions of the prototype were the same as those of the Cúk converter described in Section 3.6.3. By setting the duty ratio d to 0.08, 0.167, 0.23, and 0.4 respectively, the experimental waveforms of driving signal v_s, switch voltage v_{DS}, output voltage V_o, inductor currents i_{L1} and i_{L2} are sketched in Figure 3.29.

Based on the analysis in Section 3.7.2, the prototype will operate in sneak circuit phenomenon III when $d = 0.08$, V when $d = 0.167$, IV when $d = 0.23$, and II when $d = 0.4$. It is obvious that the experimental results coincide with theoretical analysis very well, therefore the sneak circuit phenomena and the corresponding conditions of the Sepic converter have been verified.

3.8 Zeta Converter

The schematic diagram of a Zeta converter is sketched in Figure 3.30. Similar to the analysis of Cúk and Sepic converters, the Zeta converter has six operating modes, which are

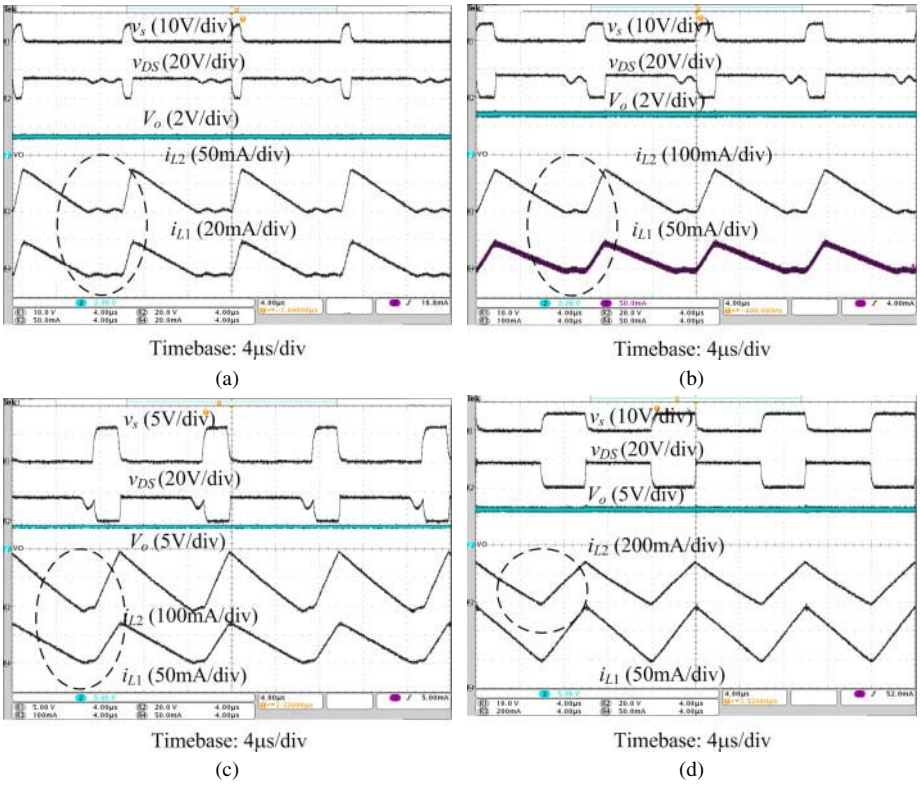


Figure 3.29 Experimental results of a Sepic prototype: (a) $d = 0.08$, sneak circuit phenomenon III; (b) $d = 0.167$, sneak circuit phenomenon V (DCM); (c) $d = 0.23$, sneak circuit phenomenon IV; and (d) $d = 0.4$, sneak circuit phenomenon II

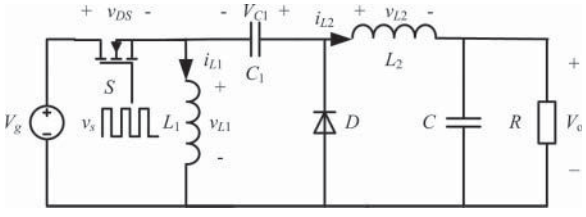


Figure 3.30 Schematic diagram of a Zeta converter

1. *Normal operating mode*: in which both inductor currents i_{L1} and i_{L2} are constantly positive (Figure 3.31);
2. *Sneak circuit phenomenon I*: in which i_{L2} is constantly positive, but i_{L1} appears negative (Figure 3.32);
3. *Sneak circuit phenomenon II*: in which i_{L1} is constantly positive, but i_{L2} appears negative (Figure 3.33);

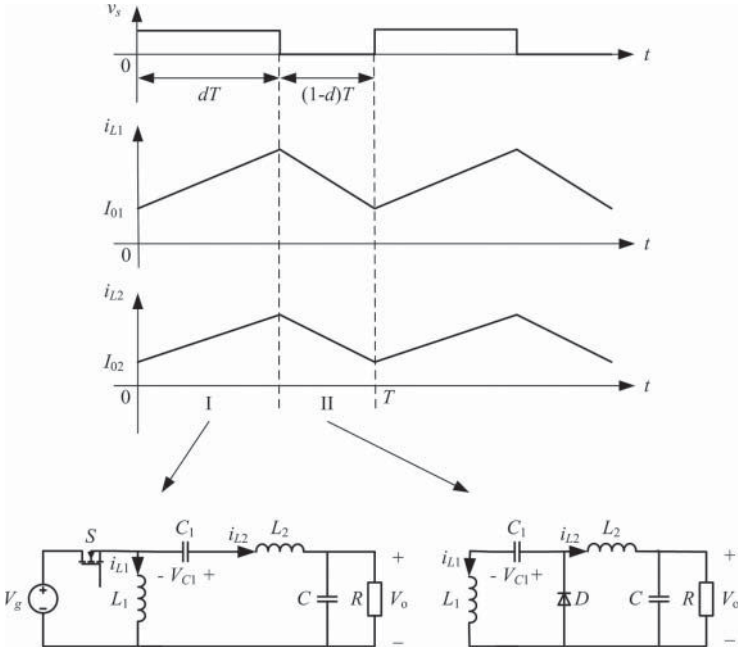


Figure 3.31 Typical waveforms and equivalent circuits of a Zeta converter in normal operating mode

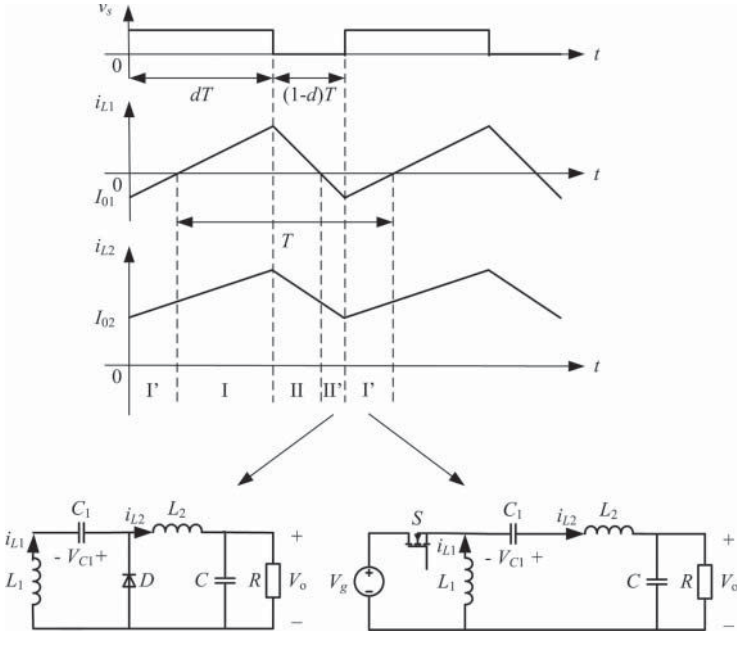


Figure 3.32 Typical waveforms and part of the equivalent circuits in Zeta sneak circuit phenomenon I

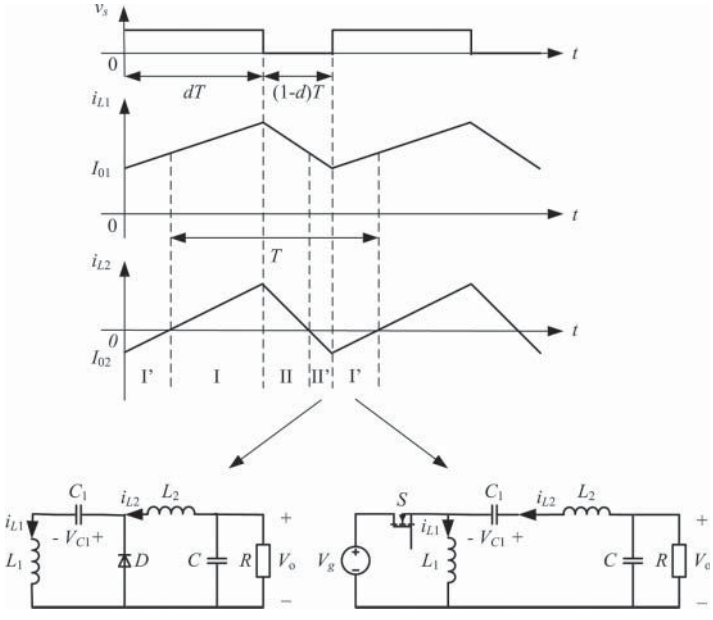


Figure 3.33 Typical waveforms and part of equivalent circuits in Zeta sneak circuit phenomenon II

4. *Sneak circuit phenomenon III*: in which i_{L2} is always positive, i_{L1} appears negative, and satisfies $i_{L1} + i_{L2} = 0$ for some of the time (Figure 3.34);
5. *Sneak circuit phenomenon IV*: in which i_{L1} is constantly positive, i_{L2} appears negative, and satisfies $i_{L1} + i_{L2} = 0$ for some of the time (Figure 3.35);
6. *Sneak circuit phenomenon V*: in which i_{L1} and i_{L2} decrease to zero at the same time, that is, DCM (Figure 3.36).

3.8.1 Normal Operating Mode of Zeta Converter

Referring to Figure 3.30, when switch S is turned on and diode D is turned off because of the reverse voltage, the input voltage source supplies energy for inductor L_1, and supplies energy for inductor L_2 and load with capacitor C_1. However, when switch S is turned off, the inductor currents flows through freewheeling diode D, inductor L_1 charges capacitor C_1, while inductor L_2 supplies energy for the load. Based on the above operating principles of a Zeta converter, the normal operating process of a Zeta converter can be divided into two stages, and its typical waveforms are shown in Figure 3.31.

Stage I (0, *dT*)

As switch S is turned on in stage I, the current loop of i_{L1} is V_g-L_1-S, while V_g-S-C_1-L_2-$R(C)$ is the current loop of i_{L2}. Assuming that I_{01} is the initial value

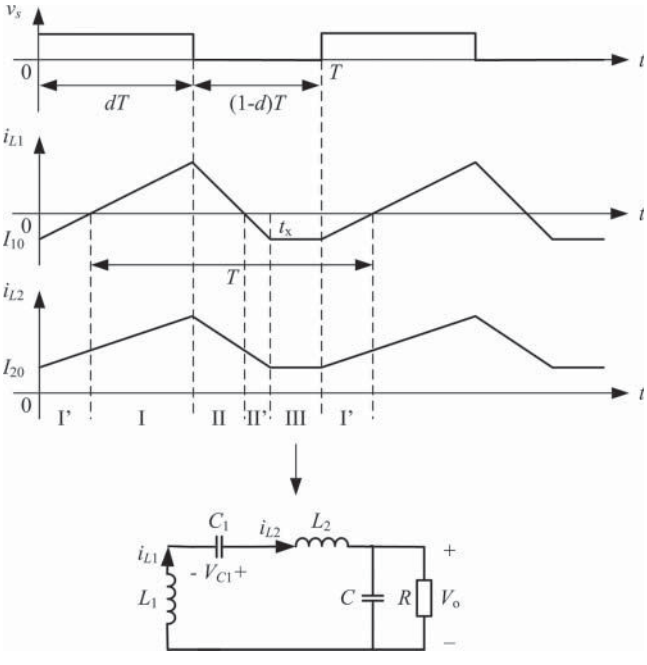


Figure 3.34 Typical waveforms and equivalent circuit of stage III in Zeta sneak circuit phenomenon III

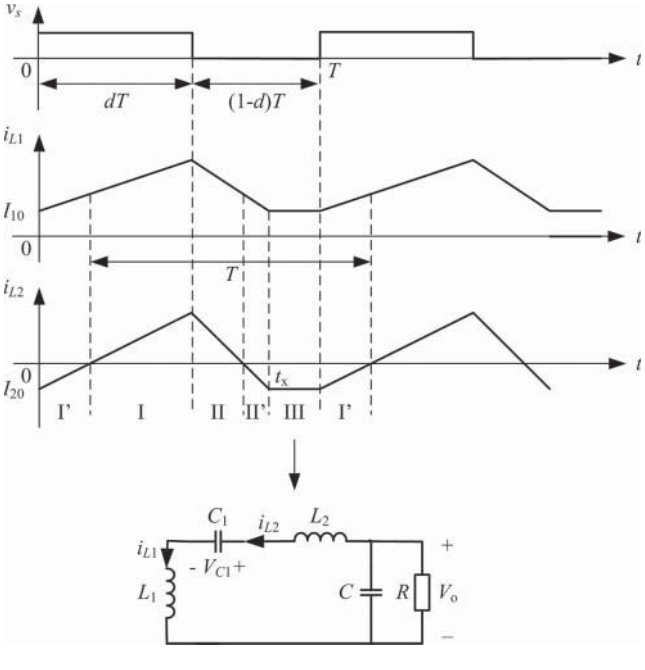


Figure 3.35 Typical waveforms and equivalent circuit of stage III in Zeta sneak circuit phenomenon IV

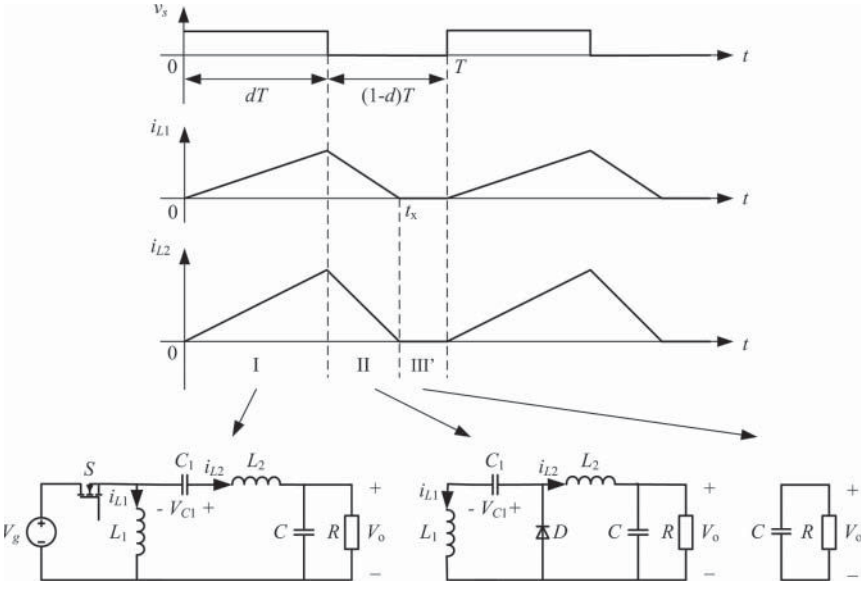


Figure 3.36 Typical waveforms and equivalent circuits in Zeta sneak circuit phenomenon V

of i_{L1} and I_{02} is the initial value of i_{L2}, and the capacitors in the Zeta converter are considered as constant voltage sources, the inductor current in stage I can be expressed as

$$i_{L1}(t) = \frac{V_g}{L_1}t + I_{01} \tag{3.81}$$

$$i_{L2}(t) = \frac{V_g + V_{C1} - V_o}{L_2}t + I_{02} \tag{3.82}$$

Stage II (dT, T)

In stage II, switch S is turned off and diode D is turned on, i_{L1} flows through the loop L_1-D-C_1, and i_{L2} flows through the loop L_2-$R(C)$-D. Then the inductor currents can be expressed as

$$i_{L1}(t) = \frac{V_g}{L_1}dT + I_{01} - \frac{V_{C1}}{L_1}(t - dT) \tag{3.83}$$

$$i_{L2}(t) = \frac{V_g}{L_2}dT + I_{02} - \frac{V_o}{L_2}(t - dT) \tag{3.84}$$

According to inductor voltage-second balance principle, the voltage-second balance equation of L_1 and L_2 can be expressed as the following equations respectively:

$$\int_0^{dT} V_g dt + \int_{dT}^{T} (-V_{C1}) dt = 0 \tag{3.85}$$

$$\int_0^{dT} (V_g + V_{C1} - V_o) dt + \int_{dT}^{T} (-V_o) dt = 0 \tag{3.86}$$

Based on Equations 3.85 and 3.86, we obtain

$$V_o = V_{C1} = \frac{d}{1-d} V_g \tag{3.87}$$

Due to the energy supplied by voltage source being equal to that consumed by the load resistor R in one switching cycle ideally, that is

$$V_g \int_0^{dT} [i_{L1}(t) + i_{L2}(t)] dt = \frac{{V_o}^2}{R} T \tag{3.88}$$

In addition, because the inductor L_2 is connected to the load in series, the average load current is equal to that of i_{L2}, that is

$$\frac{1}{T} \int_0^{T} i_{L2}(t) dt = \frac{V_o}{R} \tag{3.89}$$

Based on Equations 3.81–3.84 and 3.87, the solution of Equations 3.88 and 3.89 yields

$$I_{01} = \frac{d^2 V_g}{(1-d)^2 R} - \frac{dTV_g}{2L_1} \tag{3.90}$$

$$I_{02} = \frac{dV_g}{(1-d)R} - \frac{dTV_g}{2L_2} \tag{3.91}$$

When the Zeta converter operates in normal mode, there must be $I_{01} > 0$ and $I_{02} > 0$. Thus the normal operating condition for a Zeta converter is

$$\begin{cases} d > 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d > 1 - 2\beta \end{cases} \tag{3.92}$$

where $\alpha = \frac{L_1 f}{R}$ and $\beta = \frac{L_2 f}{R}$.

3.8.2 Sneak Circuit Phenomena of Zeta Converter

3.8.2.1 Sneak Circuit Phenomenon I of Zeta Converter

When the inductor current i_{L1} appears negative, two new stages I′ and II′ are added in the operating process. However, the equivalent circuits of stages I′ and II′, which are shown in Figure 3.32, are the same as those of stages I and II in Figure 3.31 respectively. Therefore, the output voltage of sneak circuit phenomenon I will be equal to that of the normal operating mode, that is $V_o = \frac{d}{1-d}V_g$.

In order to ensure S or D being turned on when $i_{L1} < 0$, it is obviously that $I_{01} < 0$, $I_{02} > 0$, and $|I_{01}| < |I_{02}|$, from Figure 3.32. Therefore, according to Equations 3.90 and 3.91, the resulting condition of sneak circuit phenomenon I is

$$\begin{cases} d < 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d > 1 - 2\beta \\ d > 1 - \lambda \end{cases} \tag{3.93}$$

where $\lambda = \sqrt{\frac{2L_1L_2f}{R(L_1+L_2)}}$.

3.8.2.2 Sneak Circuit Phenomenon II of Zeta Converter

The operating waveforms of a Zeta converter in sneak circuit phenomenon II and part of equivalent circuits are shown in Figure 3.33. Similar to the analysis of sneak circuit phenomenon I, the output voltage of sneak circuit phenomenon II is $V_o = \frac{d}{1-d}V_g$ as well, and the resulting condition that satisfies $I_{01} < 0$, $I_{02} > 0$, and $|I_{01}| > |I_{02}|$ is

$$\begin{cases} d > 1 + \alpha - \sqrt{2\alpha + \alpha^2} \\ d < 1 - 2\beta \\ d > 1 - \lambda \end{cases} \tag{3.94}$$

3.8.2.3 Sneak Circuit Phenomenon III of Zeta Converter

Compared with sneak circuit phenomenon I, when i_{L1} becomes negative and is equal to $-i_{L2}$ (i.e., $i_{L1} + i_{L2} = 0$), a new stage III is added, as shown in Figure 3.34. Assuming that the Zeta converter enters stage III when $t = t_x$, both S and D are turned off, and the inductor currents will keep constant, then we have $I_{01} = -I_{02} = I_0$.

According to the inductor voltage-second balance principle, the output voltage of the Zeta converter in sneak circuit phenomenon III is

$$V_o = V_{C1} = \frac{dTV_g}{t_x - dT} \tag{3.95}$$

Combining the inductor current expressions in each operating stage with the ampere-second balance principle of capacitor C_1, the following equations can be

obtained:

$$\begin{cases} t_x = dT + \lambda T \\ I_0 = -\dfrac{V_g d\lambda T}{2L_1} + \dfrac{V_g d^2 T}{2L_2} \end{cases} \tag{3.96}$$

Substituting Equation 3.93 into Equation 3.92 yields the output voltage of sneak circuit phenomenon III, which is

$$V_o = \frac{d}{\lambda} V_g \tag{3.97}$$

From Figure 3.26, it is known that $I_0 < 0$ and $t_x < T$. Therefore, the condition of sneak circuit phenomenon III is

$$\begin{cases} d < \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.98}$$

3.8.2.4 Sneak Circuit Phenomenon IV of Zeta Converter

Comparing sneak circuit phenomenon IV (Figure 3.35) with phenomenon III (Figure 3.34), the only difference between them is the inductor current direction. Thus, the output voltage of sneak circuit phenomenon IV is equal to $V_o = \frac{d}{\lambda} V_g$. When sneak circuit phenomenon IV appears, there is $I_0 > 0$ and $t_x < T$, then the condition of sneak circuit mode IV is

$$\begin{cases} d > \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.99}$$

3.8.2.5 Sneak Circuit Phenomenon V of Zeta Converter

As shown in Figure 3.36, when the Zeta converter operates in the sneak circuit phenomenon V, i_{L1} and i_{L2} will decrease to zero at the same time, which can be regarded as the special situation of sneak circuit phenomena III and IV when $I_0 = 0$.

Therefore, the resulting condition of sneak circuit phenomenon V is

$$\begin{cases} d = \lambda \dfrac{L_2}{L_1} \\ d < 1 - \lambda \end{cases} \tag{3.100}$$

Based on Equations 3.97 and 3.100, the output voltage is defined by $V_o = \frac{d}{\lambda} V_g = \frac{L_2}{L_1} V_g$.

3.8.3 *Experimental Verification of Zeta Converter*

A Zeta prototype is built to verify different operating mode of the Zeta converter based on Figure 3.30. The prototype parameters are $V_g = 12$ V, $f = 100$ kHz, $L_1 = 120$ μH, $L_2 = 440$ μH, $C_1 = 330$ μF, $C = 180$ μF, and $R = 50\ \Omega$, then $\alpha = \frac{L_1 f}{R} = 0.24$, $\beta = \frac{L_2 f}{R} = 0.88$, and $\lambda = \sqrt{\frac{2\alpha\beta}{\alpha+\beta}} = 0.614$ can be obtained. According to the analysis results in above sections, there are only three operating modes in the Zeta prototype, which are:

1. $d > 0.507$, normal operating mode (CCM);
2. $0.386 < d < 0.507$, sneak circuit phenomenon I; and
3. $d < 0.386$, sneak circuit phenomenon III.

Setting the duty ratios d equal to 0.23, 0.4, and 0.51 respectively, the corresponding experimental waveforms of driving signal v_s, switch voltage v_{DS}, and inductor currents i_{L1} and i_{L2} are sketched in Figure 3.37.

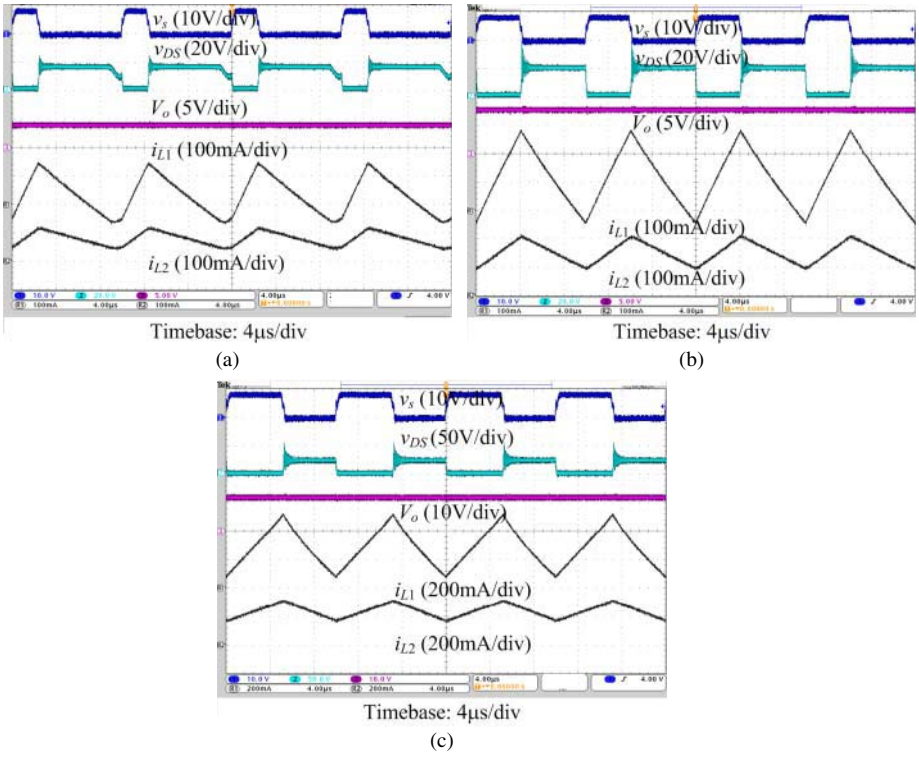
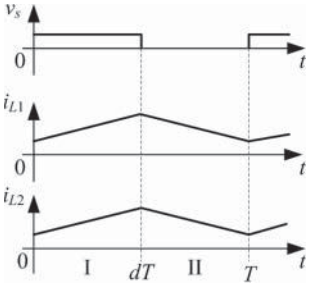
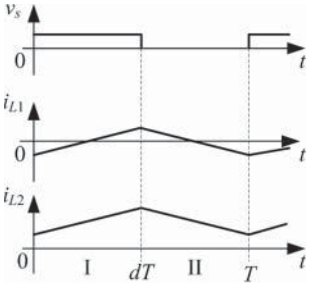
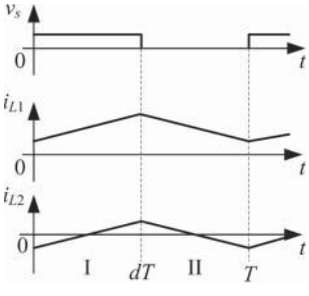
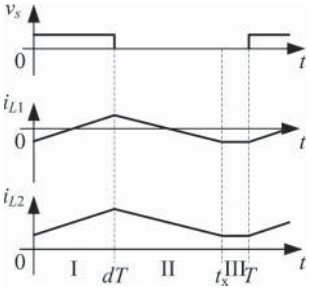


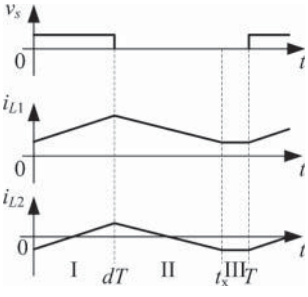
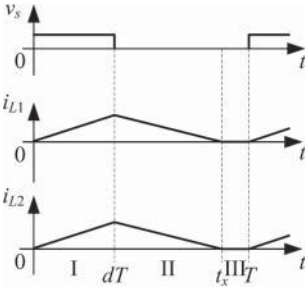
Figure 3.37 Experimental results of a Zeta converter: (a) $d = 0.23$, sneak circuit phenomenon III; (b) $d = 0.4$, sneak circuit phenomenon I; and (c) $d = 0.51$, normal operating mode

Table 3.2 Operating conditions and voltage ratios of Cúk, Sepic, and Zeta converters

Phenomenon	Typical waveform	Voltage ratio V_o/V_g	Operating condition
Normal operating phenomenon (CCM)		$\frac{d}{1-d}$	$\begin{cases} d > 1+\alpha-\sqrt{2\alpha+\alpha^2} \\ d > 1-2\beta \end{cases}$
Sneak circuit phenomenon I		$\frac{d}{1-d}$	$\begin{cases} d < 1+\alpha-\sqrt{2\alpha+\alpha^2} \\ d > 1-2\beta \\ d > 1-\lambda \end{cases}$
Sneak circuit phenomenon II		$\frac{d}{1-d}$	$\begin{cases} d > 1+\alpha-\sqrt{2\alpha+\alpha^2} \\ d < 1-2\beta \\ d > 1-\lambda \end{cases}$
Sneak circuit phenomenon III		$\frac{d}{\lambda}$	$\begin{cases} d < \frac{\lambda\beta}{\alpha} \\ d < 1-\lambda \end{cases}$

(*continued overleaf*)

Table 3.2 (*continued*)

Phenomenon	Typical waveform	Voltage ratio V_o/V_g	Operating condition
Sneak circuit phenomenon IV		d/λ	$\begin{cases} d > \dfrac{\lambda\beta}{\alpha} \\ d < 1-\lambda \end{cases}$
Sneak circuit phenomenon V (DCM)		$\dfrac{L_2}{L_1}$	$\begin{cases} d = \dfrac{\lambda\beta}{\alpha} \\ d < 1-\lambda \end{cases}$

Note: $\alpha = \frac{L_1 f}{R}$, $\beta = \frac{L_2 f}{R}$ and $\lambda = \sqrt{\frac{2L_1L_2f}{R(L_1+L_2)}} = \sqrt{\frac{2\alpha\beta}{\alpha+\beta}}$.

It is clear that the Zeta prototype worked in sneak circuit phenomenon III, I and normal operating mode CCM respectively and the experimental results were coincident with the theoretical analysis, therefore the sneak circuit phenomena and resulting conditions of the Zeta converter have been verified.

3.9 Sneak Circuit Conditions of Cúk, Sepic, and Zeta Converters

By synthesizing the above analysis of Cúk, Sepic, and Zeta converters, it is found that not only their normal operating waveforms but also their sneak circuit phenomena are similar, even their operating conditions and output voltage expressions are the same. Therefore, the operating conditions and voltage ratios between input and output voltages of Cúk, Sepic, and Zeta converters under different modes have been concluded in Table 3.2. According to this table, the sneak circuit phenomena of Cúk, Sepic, or Zeta converters can be mastered, and the undesired operating mode can be avoided by choosing appropriate circuit parameters or operation conditions.

3.10 Summary

The DC-DC converter is a basic power electronic converter. According to the definition of the sneak circuit, this chapter has studied the sneak circuit phenomenon existing in the non-isolated DC-DC converters from a new point of view. If the situation of inductor current being continuous and positive is regarded as CCM or the normal operating mode of the DC-DC converter, the other situations that should be considered are the sneak circuit modes of the DC-DC converter, including DCM. Unlike Buck, Boost, and Buck-boost converters, DCM is not the only sneak circuit phenomenon in Cúk, Sepic, and Zeta converters, because there are two inductors in these high-order converters and the variations of inductor current are more complicated. The sneak circuit phenomena and their resulting conditions of six non-isolated DC-DC converters have been deduced in this chapter, which will lead to a better understanding of the performance of DC-DC converters.

References

[1] Mohan, N., Undelane, T.M. and Robbins, W.P. (2003) *Power Electronics: Converters, Applications, and Design*, 3rd edn, John Wiley & Sons, Ltd, Hoboken, NJ.

[2] Erikcson, R.W. and Maksimovic, D. (2001) *Fundamentals of Power Electronics*, 2nd edn, Kluwer Academic Publishers, Norwell, MA.

4

Sneak Circuits of Soft-Switching Converters

4.1 Introduction

Soft-switching is a technique that makes use of capacitor, inductor, and other components to realize resonance, for reducing the switching losses of switching components and EMI in the power electronic converter. As a result of adding resonant components such as capacitor or inductor into the soft-switching converter, it is certain that the soft-switching converter will have more current paths than the hard-switching converter. Consequently, the sneak circuit phenomena in the soft-switching converter will be more complex than those in the hard-switching converter.

According to the development of the soft-switching technique, the soft-switching converter can be divided into three types, including the quasi-resonant converter, the zero-switching pulse-width modulation (PWM) converter, and the zero-transition PWM converter. In this chapter, the sneak circuit phenomena of several typical soft-switching converters will be introduced.

4.2 Sneak Circuits of Full-Bridge ZVS PWM Converter

Among the DC/DC converters, the Full-bridge (FB) PWM converter is generally used in high-power applications, and the phase-shift technique is often used to control an FB converter, which can make the converter operate in zero voltage switching (ZVS). The basic soft-switching principle of the FB PWM converter is that ZVS of all switching devices can be achieved by the resonance between the leakage inductor of the transformer or the inductor in series with the transformer primary side and the parasitic capacitor of switches. The normal operating mode of the FB ZVS PWM converter will be introduced first.

Sneak Circuits of Power Electronic Converters, First Edition. Bo Zhang and Dongyuan Qiu.

4.2.1 Normal Operating Mode of FB ZVS PWM Converter

A schematic diagram of a conventional FB ZVS PWM converter is shown in Figure 4.1, where D_1 to D_4 is the anti-parallel diodes of switches Q_1 to Q_4, respectively, C_1 to C_4 are the parasitic capacitors or external paralleled capacitors of Q_1 to Q_4, respectively, and L_r represents the total resonant inductor of the leakage inductor of the transformer and the additional inductor in series with the transformer primary side. The fundamental operating principle of the FB ZVS PWM converter is that a pair of switches in each bridge leg conduct complementarily by 180 degrees and the conduction angle of the two bridge legs differ in a fixed phase, where the switching transition of leg Q_1-Q_3 is delayed, that is, phase shifted, with respect to the switching transition of leg Q_2-Q_4. Then leg Q_1-Q_3 becomes known as the lagging leg, and leg Q_2-Q_4 the leading leg. Typical waveforms of an FB ZVS PWM converter under normal operation are shown in Figure 4.2.

The output voltage of an FB ZVS PWM converter can be controlled by duty ratio d of the switches. However, the loss of duty ratio in the secondary side is a common phenomenon in the FB ZVS PWM converter; based on reference [1], the actual output voltage is expressed by

$$V_o = \frac{d_{eff}}{N} V_i \tag{4.1}$$

where d_{eff} is the effective duty ratio in the transformer secondary side. The relationship between the effective duty ratio d_{eff} and the duty ratio d in the transformer primary side is

$$d_{eff} = \frac{d}{1 + \dfrac{4L_r f}{N^2 R_L}} \tag{4.2}$$

where $f = \frac{1}{T}$ is the switching frequency, T is the switching cycle, RL is the load resistance, and N is the turns ratio of the transformer.

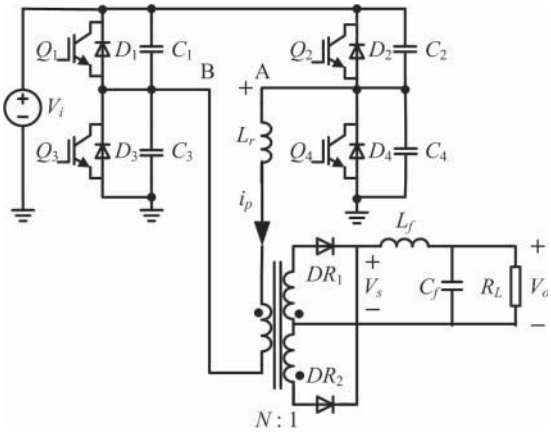


Figure 4.1 Schematic diagram of a FB ZVS PWM converter

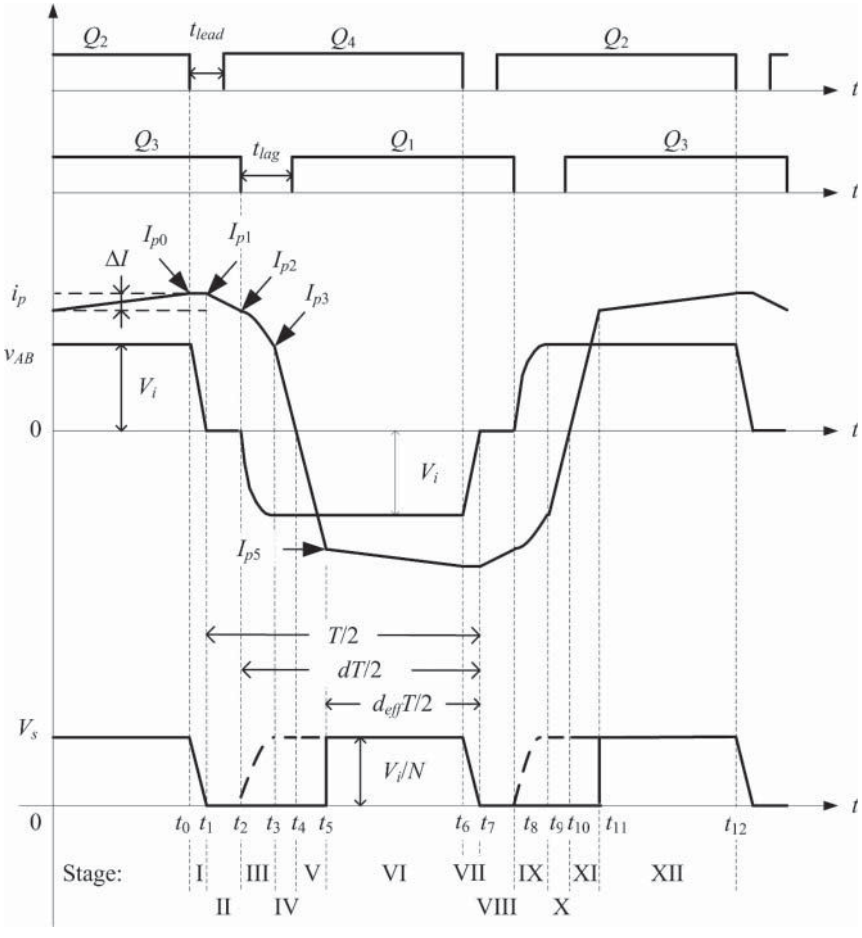


Figure 4.2 Typical waveforms of a FB ZVS PWM converter under normal operation

As shown in Figure 4.2, the normal operating process of an FB ZVS PWM converter can be divided into twelve stages in one switching period T, and the equivalent circuits of the first six stages are illustrated in Figure 4.3.

The analysis of normal operating mode will be described before the following assumptions are made:

1. All elements in the FB ZVS PWM converter are ideal.
2. The paralleled capacitors of switches are defined by $C_1 = C_3 = C_{lag}$ and $C_2 = C_4 = C_{lead}$, but the capacitance between the transformer winding is ignored.
3. The filter inductance L_f satisfies $L_f >> L_r/N^2$.

Before stage I (or when $t < t_0$), Q_2 and Q_3 are conducting, the current of the primary side i_p is positive, the output voltage of FB $v_{AB} = V_i$, the rectifier diode DR_2 is conducting, and the load is supplied by the input voltage source. As shown in Figure 4.2,

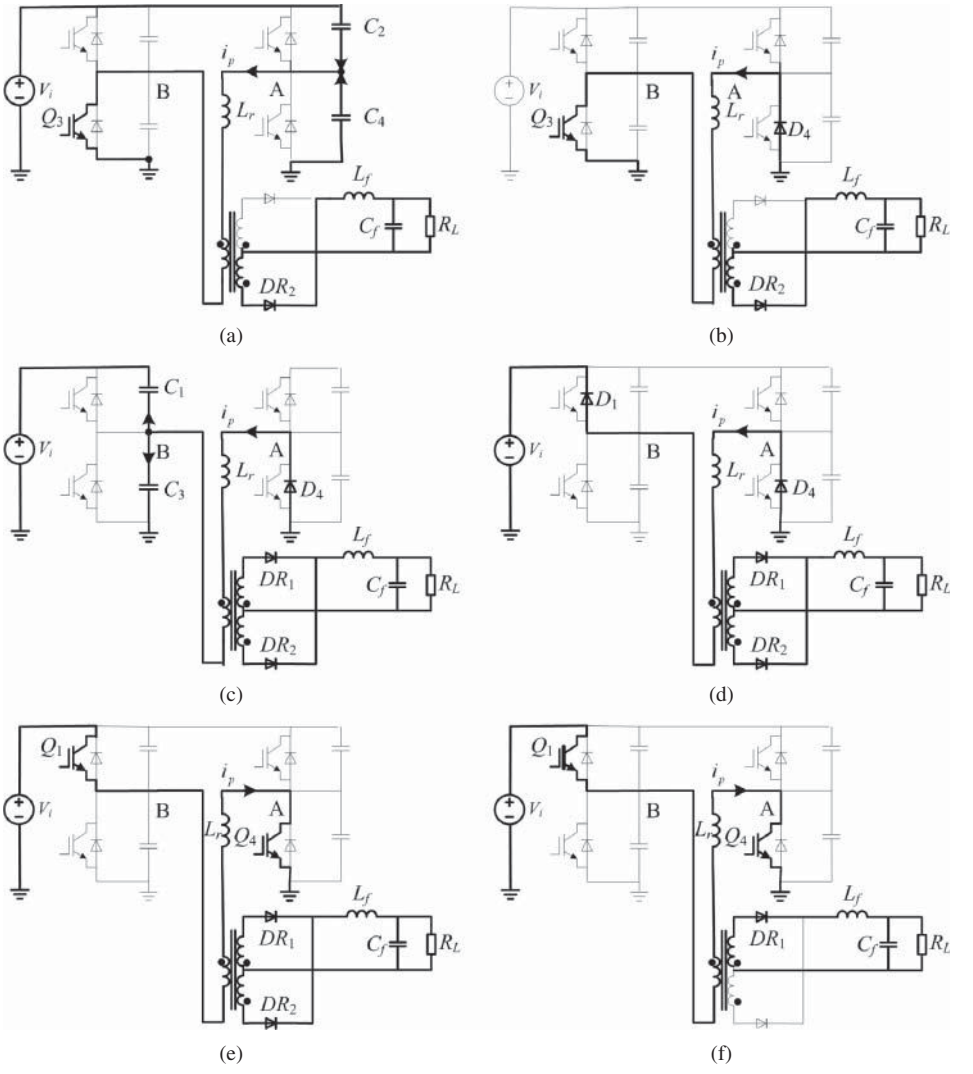


Figure 4.3 Equivalent circuits of the normal operating stages I to VI of a FB ZVS PWM converter: (a) stage I; (b) stage II; (c) stage III; (d) stage IV; (e) stage V; and (f) stage VI

the value of i_p at $t = t_0$ equates to

$$I_{p0} = \frac{I_o}{N} + \frac{\Delta I}{2} \tag{4.3}$$

where $I_o = \frac{V_o}{R_L}$ is the average output current and ΔI is the primary current ripple during the conduction, which can be given by

$$\Delta I = \frac{V_i - NV_o}{L_r + N^2 L_f} \frac{d_{eff} T}{2} \tag{4.4}$$

It is known that $L_f >> L_r/N^2$, so Equation 4.4 can be simplified to

$$\Delta I = \frac{V_i - NV_o}{N^2 L_f} \frac{d_{eff} T}{2} \tag{4.5}$$

In Equation 4.5, ΔI can be regarded as the current ripple of the output filter inductor converting to the primary side.

The analysis of the first six stages are described by the following.

Stage I (t_0, t_1)

Referring to Figure 4.3a, switch Q_2 is turned off at t_0, then the primary current i_p charges the paralleled capacitor C_2 of Q_2 and discharges the paralleled capacitor C_4 of Q_4. v_{C2} will increase from zero and Q_2 can achieve zero-voltage turn-off. $v_{AB} = v_{C4}$ in stage I; meanwhile, as the primary resonant inductor L_r and the filter inductor L_f are connected in series, the total inductance is very large, i_p is approximately constant, and i_p and v_{AB} can be given by

$$i_p(t) = I_{p0} = I_{p1} \tag{4.6}$$

$$v_{AB}(t) = V_i - \frac{I_{p0}}{2C_{lead}}(t - t_0) \tag{4.7}$$

Capacitor voltage v_{C4} (i.e., v_{AB}) decreases from V_i linearly. Assuming that v_{C4} falls to zero at t_1, then D_4, the anti-parallel diode of Q_4, will conduct and stage I will be finished. The duration of stage I is defined by

$$t_1 - t_0 = \frac{2C_{lead} V_i}{I_{p0}} \tag{4.8}$$

Stage II (t_1, t_2)

Referring to Figure 4.3b, Q_4 can be turned on at ZVS after D_4 conducts, because D_4 clamps v_{Q4} to almost zero. Although Q_4 has been turned on, the positive primary current i_p is still running through D_4, and there is no current passing through Q_4. As $v_{AB} = 0$ in stage II, i_p is equal to the filter inductor current converting to the primary side, which is

$$i_p(t) = \frac{1}{N}\left[I_o + \frac{\Delta I}{2} N - \frac{V_o}{L_f}(t - t_1)\right] \tag{4.9}$$

Assuming that Q_3 is turned off at t_2, the primary current i_p at $t = t_2$ can be approximated by

$$I_{p2} = \frac{1}{N}\left[I_o + \frac{\Delta I}{2} N - \frac{V_o}{L_f}\frac{(1-d)\,T}{2}\right] \tag{4.10}$$

The dead time between switches Q_2 and Q_4 of the leading leg, t_{lead}, should be larger than $t_1 - t_0$, to achieve ZVS of Q_4, then should satisfy

$$t_{lead} > \frac{2C_{lead}V_i}{I_{p0}} \tag{4.11}$$

Stage III (t_2, t_3)

Referring to Figure 4.3c, Q_3 is turned off at t_2, and the primary current i_p transfers to C_1 and C_3, where C_1 charges and C_3 discharges. Due to C_3 is the paralleled capacitor of Q_3, v_{Q3} or v_{C3} will rise from zero slowly, then Q_3 can be turned off at ZVS. Since $v_{AB} = -v_{C3}$ in stage III, the secondary voltage of the transformer becomes negative, then the rectifier diode DR_1 conducts too. Both the primary and secondary voltages of the transformer are zero because the secondary windings of the transformer are shorted by DR_1 and DR_2, then the voltage on the filter inductor v_{Lr} is equal to v_{AB}. L_r resonates with C_1 and C_3 during this stage. i_p and v_{C3} can be given by

$$i_p(t) = I_{p2}\cos\omega_1(t - t_2) \tag{4.12}$$

$$v_{C3}(t) = I_{p2}Z_1\sin\omega_1(t - t_2) \tag{4.13}$$

where $Z_1 = \sqrt{\frac{L_r}{2C_{lag}}}$ and $\omega_1 = \frac{1}{\sqrt{2L_rC_{lag}}}$.

Assuming that v_{C3} rises to V_i at t_3, D_1 begins to conduct, and stage III is ended, the duration of stage III is

$$t_3 - t_2 = \frac{\lambda}{\omega_1} \tag{4.14}$$

where $\lambda = \sin^{-1}\frac{V_i}{I_{p2}Z_1}$.

At $t = t_3$, the value of the primary current i_p is

$$I_{p3} = I_{p2}\cos\lambda \tag{4.15}$$

Stage IV (t_3, t_4)

Referring to Figure 4.3d, Q_1 can be turned on at ZVS because its voltage is clamped to almost zero after D_1 conducts. Because i_p is still positive, there is no current passing through Q_1; i_p flows through D_1 and D_3, and the stored energy in the resonant inductor L_r will feed back to the voltage source V_i. Since the voltages of the transformer primary and secondary sides are zero, $v_{AB} = v_{Lr} = -V_i$ in stage IV, and i_p decreases linearly and is expressed by

$$i_p(t) = I_{p3} - \frac{V_i}{L_r}(t - t_3) \tag{4.16}$$

Assuming that i_p falls to zero at t_4, and both D_1 and D_4 are off, then the duration of stage IV is defined by

$$t_4 - t_3 = \frac{I_{p3}L_r}{V_i} = \frac{I_{p2}L_r \cos\lambda}{V_i} \tag{4.17}$$

As shown in Figure 4.2, the time between when Q_3 is shut down and Q_1 is turned on is defined as the dead time of the lagging leg, that is, t_{lag}. Based on the above analysis, in order to achieve ZVS of lagging leg, t_{lag} must satisfy $t_3 - t_2 < t_{lag} < t_4 - t_2$, which is

$$\frac{\lambda}{\omega_1} < t_{lag} < \frac{\lambda}{\omega_1} + \frac{I_{p2}L_r \cos\lambda}{V_i} \tag{4.18}$$

Based on Equation 4.18, there are $t_{lag-\min} = \frac{\lambda}{\omega_1}$ and $t_{lag-\max} = \frac{\lambda}{\omega_1} + \frac{I_{p2}L_r \cos\lambda}{V_i}$.

Stage V (t_4, t_5)

Referring to Figure 4.3e, as i_p is too small to afford the load current, both of the rectifier diodes keep conducting, and the transformer primary and secondary voltages are zero as well as stage IV. Because of $v_{AB} = v_{Lr} = -V_i$, i_p increases linearly reversed and flows through Q_1 and Q_4, which can be given by

$$i_p(t) = -\frac{V_i}{L_r}(t - t_4) \tag{4.19}$$

Assuming that i_p is equal to the load current reflected to the primary side at t_5, we have

$$I_{p5} = -\left(\frac{I_o}{N} - \frac{\Delta I}{2}\right) \tag{4.20}$$

At this moment, DR_2 is off, stage V is ended, and the entire load current will flow through DR_1 only.

Stage VI (t_5, t_6)

Referring to Figure 4.3f, Q_1 and Q_4 keep conducting, the load current is provided by the input voltage source, and i_p can be defined by

$$i_p(t) = I_{p5} - \frac{V_i - NV_o}{N^2 L_f}(t - t_5) \tag{4.21}$$

When Q_4 is turned off at t_6 and stage VI is ended, the FB ZVS PWM converter begins to operate in another half cycle, where the operation of the next six stages are similar to those of stages I to VI.

4.2.2 Zero Voltage Switching Conditions of FB ZVS PWM Converter

In order to achieve ZVS of all switches in the FB PWM converter, there should be enough energy to make the voltage of the parasitic capacitor or external additional capacitor resonate to zero before the switch is turned on, and charge the parasitic capacitor or external additional capacitor of the other switch in the same leg to the input voltage V_i.

During the switching transition between Q_2 and Q_4 on the leading leg, that is, stages I and II, the output filter inductor L_f is in series with the resonant inductor L_r, and the energy stored in L_f and L_r is large enough to achieve ZVS. However, as the secondary side of the transformer is shortened during the switching transition between switches Q_1 and Q_3 on the lagging leg, that is, stages III and IV, only the energy stored in L_r is used to achieve ZVS, which is relatively small. As a result, it is easy to obtain ZVS for switches Q_2 and Q_4 on the leading leg, but difficult for Q_1 and Q_3 on the lagging leg [2].

On the basis of the above analysis, the ZVS conditions of the FB ZVS PWM converter are expressed by

$$\begin{cases} \frac{1}{2}L_r {I_{p2}}^2 > C_{lag} {V_i}^2 \\ t_{lag-\min} < t_{lag} < t_{lag-\max} \\ t_{lead} > \dfrac{2C_{lead}V_i}{I_{p1}} \end{cases} \tag{4.22}$$

Defining the critical current I_{crit} as

$$I_{crit} = V_i \sqrt{\frac{2C_{lag}}{L_r}} \tag{4.23}$$

then the sub-equation $\frac{1}{2}L_r I_{p2}^2 > C_{lag} {V_i}^2$ in Equation 4.22 changes to

$$I_{p2} > I_{crit} \tag{4.24}$$

or the load current should satisfy with

$$I_o > N\left(I_{crit} - \frac{\Delta I}{2}\right) + \frac{V_o}{L_f}\frac{(1-d)T}{2} \tag{4.25}$$

4.2.3 Sneak Circuit Phenomena of FB ZVS PWM Converter

For the FB ZVS PWM converter, if the input voltage V_i or load resistance R_L is changed, or the dead times between switches (t_{lead} or t_{lag}) are not set in a reasonable range, then ZVS may not be realized, and the current will not flow in the presetting paths, or some new current paths will show up, therefore the sneak circuit phenomena will appear.

Based on Equation 4.22, it is clear that the ZVS conditions of the FB ZVS PWM converter can be divided into ZVS time condition and ZVS current condition; no matter which condition is not satisfied, the sneak circuit phenomena will occur. The following sneak circuit analysis will be classified by taking the ZVS current condition into account. Similar to normal operation, only the operating process in the positive half cycle will be analyzed.

4.2.3.1 Sneak Circuit Analysis under the ZVS Current Condition

When the ZVS current condition of the FB ZVS PWM converter, that is, Equation 4.24 is satisfied, there are three kinds of sneak circuit phenomena.

Sneak Circuit Phenomenon I

According to Equations 4.10 and 4.14, when the operating condition of the converter is changed, for example, the load resistance R_L is increased which causes I_{p2} to decrease and $t_{lag-\min}$ to increase, while t_{lead}, t_{lag}, and I_{crit} remain unchanged. When

$$\begin{cases} t_{lag} < t_{lag-\min} \\ I_{p2} > I_{crit} \end{cases} \tag{4.26}$$

is satisfied, Q_1 have to be turned on before stage III is completed (or v_{AB} reaches to $-V_i$), then the zero-voltage turn-on cannot be realized. Furthermore, a new operating stage A will appear after stage III. The equivalent circuit of sneak stage A is shown in Figure 4.4.

As Q_1 is turned on during the resonant process of C_1, C_3, and L_r, v_{C1} will discharge to zero and v_{C3} will charge to V_i immediately. When the sneak stage A is ended, the primary current i_p flows through the freewheeling diodes D_1 and D_4, which is the same as normal stage IV. Then the converter will operate in normal stages IV, V, and VI after sneak stage A. The typical waveforms of sneak circuit phenomenon I are shown in Figure 4.5.

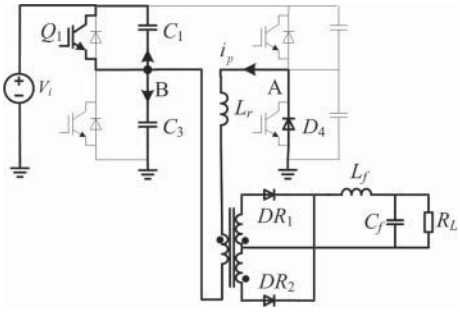


Figure 4.4 Equivalent circuit of sneak stage A

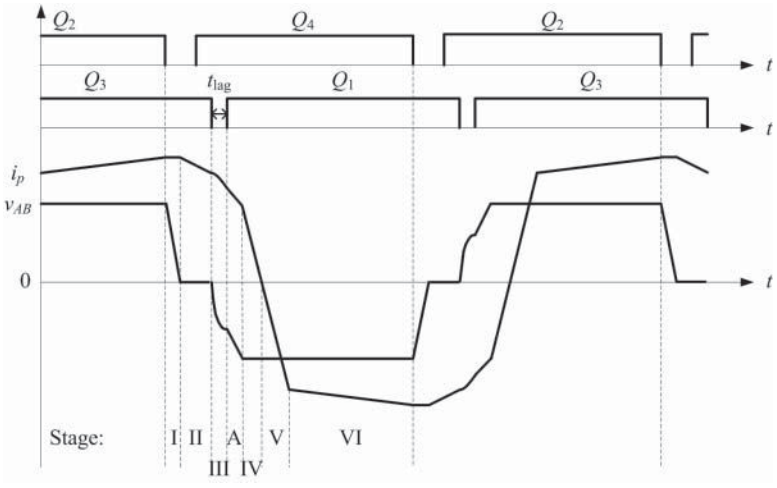


Figure 4.5 Typical waveforms of sneak circuit phenomenon I of a FB ZVS PWM converter

Sneak Circuit Phenomenon II

In the normal operating mode, Q_1 should be turned on during stage IV to achieve ZVS. If $t_{lag} > t_{lag-\max}$ is satisfied, namely Q_1 does not turn on, even if stage IV is finished, then a new operating stage B will appear, whose equivalent circuit is shown in Figure 4.6a.

During sneak stage B, L_r will resonate with C_1 and C_3 again, and as Q_1 is still off, i_p will increase reversed from zero and v_{C3} will decrease. The expressions of i_p and v_{C3} are

$$i_p(t) = -\frac{V_i}{Z_1}\sin\omega_1(t-t_4) \tag{4.27}$$

$$v_{C3}(t) = V_i\cos\omega_1(t-t_4) \tag{4.28}$$

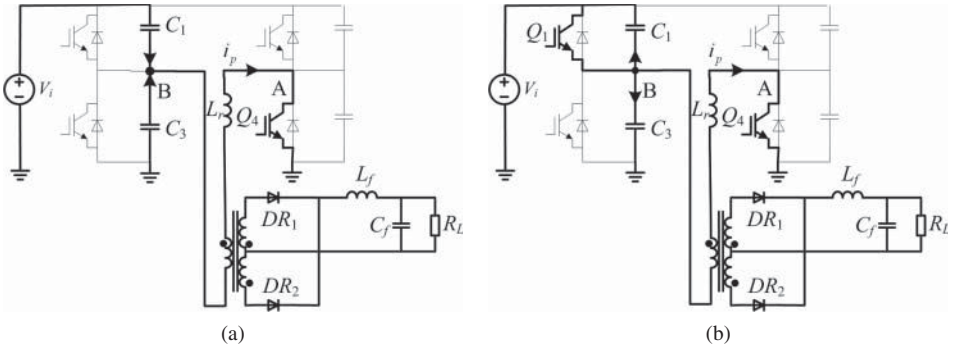


Figure 4.6 Equivalent circuits of sneak stages B and C: (a) sneak stage B; and (b) sneak stage C

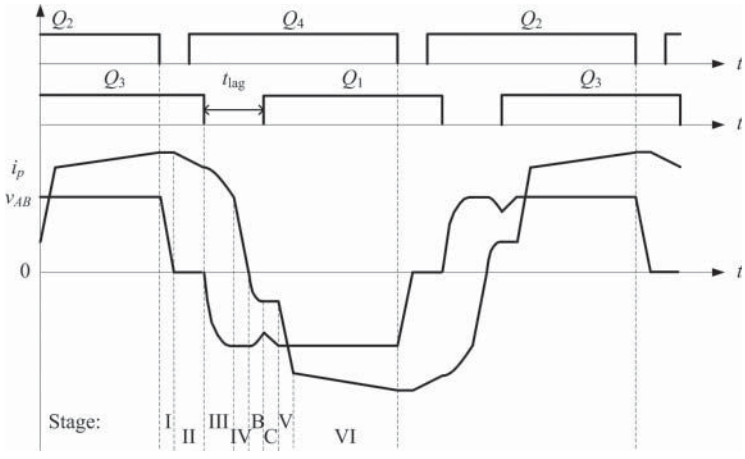


Figure 4.7 Typical waveforms of the sneak circuit phenomenon II of a FB ZVS PWM converter

If Q_1 is not turned on before v_{C3} decreases to zero, then sneak stage B is finished when $v_{C3}(t) = V_i \cos \omega_1 (t - t_4) = 0$, and the maximum duration of sneak stage B is defined by

$$t_{B-\max} = \pi \sqrt{\frac{L_r C_{lag}}{2}} \tag{4.29}$$

If Q_1 is turned on during stage B, that is, the lagging dead time satisfies $t_{lag} < t_{lag-\max} + t_{B-\max}$, then Q_1 will not realize ZVS because v_{C3} does not decrease to zero. Furthermore, a new stage C will show up, as shown in Figure 4.6b.

As Q_1 has been turned on, v_{C1} discharges to zero and v_{C3} rapidly charges to V_i , and i_p remains almost constant because of the existence of resonant inductance L_r. When $v_{AB} = -v_{C3} = -V_i$, the sneak stage C is ended, so the converter will operate in normal stages V and VI.

In summary, the condition of sneak circuit phenomenon II is given by Equation 4.30, and its corresponding typical waveforms are shown as Figure 4.7.

$$\begin{cases} t_{lag-\max} < t_{lag} < t_{lag-\max} + t_{B-\max} \\ I_{p2} > I_{crit} \end{cases} \tag{4.30}$$

Sneak Circuit Phenomenon III

If Q_1 is still off when sneak stage B is over, that is, $t_{lag} > t_{lag-\max} + t_{B-\max}$, then another new stage D will appear, as shown in Figure 4.8.

During sneak stage D, because $v_{C3} = 0$ and $v_{C1} = V_i$, i_p flows through D_3 and Q_4 and remains almost constant, and Q_1 cannot realize zero voltage turn-on. When Q_1 is turned on, the converter will operate in stages C, V, and VI until Q_4 is turned off.

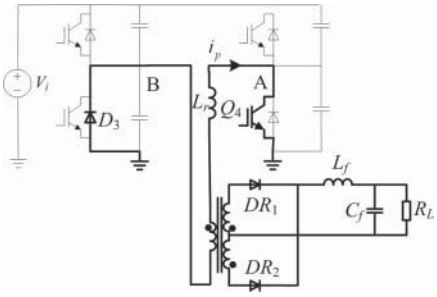


Figure 4.8 Equivalent circuit of the sneak stage D

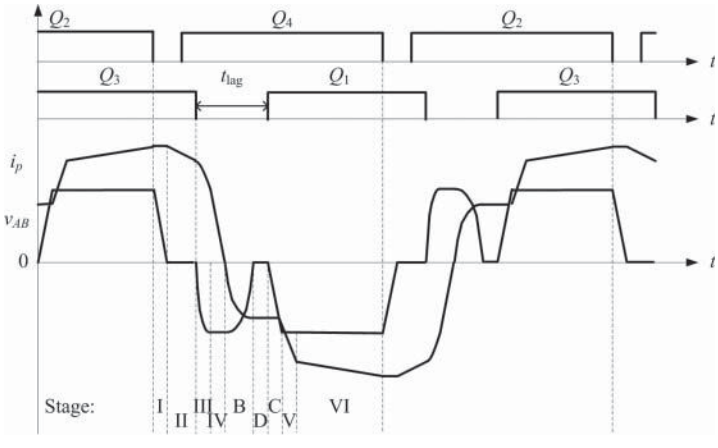


Figure 4.9 Typical waveforms of the sneak circuit phenomenon III of a FB ZVS PWM converter

Based on the above analysis, the condition of sneak circuit phenomenon III can be expressed as

$$\begin{cases} t_{lag} > t_{lag-\max} + t_{B-\max} \\ I_{p2} > I_{crit} \end{cases} \tag{4.31}$$

and the typical waveforms of sneak circuit phenomenon III are shown in Figure 4.9.

4.2.3.2 Sneak Circuit Analysis out of the ZVS Current Condition

When the ZVS current condition of an FB ZVS PWM converter is not satisfied, there are also three kinds of sneak circuit phenomena, which are numbered as IV to VI.

Sneak Circuit Phenomenon IV

If $I_{p2} < I_{crit} = V_i\sqrt{\frac{2C_{lag}}{L_r}}$ is satisfied by changing the converter parameters, such as increasing the load resistance R_L, according to Equation 4.13, the maximum value of

capacitor voltage v_{C3} during normal stage III will be

$$V_{C3} = I_{p2} Z_1 < V_i \tag{4.32}$$

Therefore, it is impossible to realize ZVS of Q_1. If Q_1 is turned on before v_{C3} increases to V_{C3}, this means that the duration of normal operating stage III satisfies $t_{23} < \frac{\pi}{2\omega_1}$, thus

$$\pi \sqrt{\frac{L_r C_{lag}}{2}} = t_{B-\max} \tag{4.33}$$

and the operating process and typical waveforms are similar to those of sneak circuit phenomenon I, but the sneak circuit condition is different. So this situation is called the sneak circuit phenomenon IV, and its condition is expressed as

$$\begin{cases} t_{lag} < t_{B-\max} \\ I_{p2} < I_{crit} \end{cases} \tag{4.34}$$

Sneak Circuit Phenomenon V

If the fixed lagging dead time t_{lag} is longer than $t_{B-\max}$, that is, $t_{lag} > t_{B-\max}$, Q_1 will not be turned on after stage III, then L_r will keep resonant with C_1 and C_3, i_p increases negatively from zero, and v_{C3} begins to decrease, which is the same as the sneak stage B.

Based on Equation 4.29, if Q_1 is turned on before stage B is ended, that is, $t_{lag} < 2t_{B-\max}$, this means that Q_1 is turned on before v_{C3} decreases to zero, and Q_1 cannot be turned on with ZVS. After Q_1 is turned on, the converter will operate at stages C, V, and VI until Q_4 is turned off.

Based on the above analysis, the typical waveforms of sneak circuit phenomenon V are shown in Figure 4.10, and the condition of sneak circuit phenomenon V can be expressed by

$$\begin{cases} t_{B-\max} < t_{lag} < 2t_{B-\max} \\ I_{p2} < I_{crit} \end{cases} \tag{4.35}$$

Sneak Circuit Phenomenon VI

If the fixed lagging dead time satisfies $t_{lag} > 2t_{B-\max}$ when some operating conditions are changed, Q_1 will be turned on after stage B is ended. Similar to sneak circuit phenomenon III, the converter will operate at stages D, C, V, and VI until Q_4 is turned off, thus the typical waveforms of sneak circuit phenomenon VI appear as shown in Figure 4.11.

The condition of sneak circuit phenomenon VI can be expressed by

$$\begin{cases} t_{lag} > 2t_{B-\max} \\ I_{p2} < I_{crit} \end{cases} \tag{4.36}$$

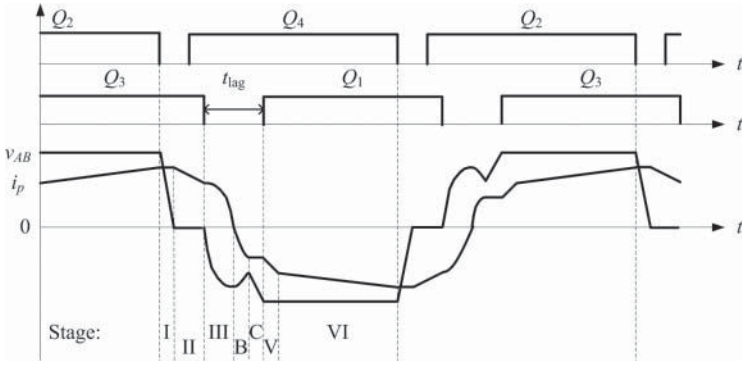


Figure 4.10 Typical waveforms of the sneak circuit phenomenon V of a FB ZVS PWM converter

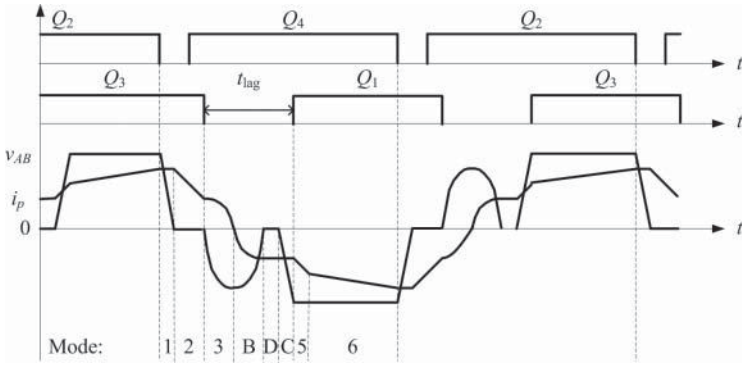


Figure 4.11 Typical waveforms of the sneak circuit phenomenon VI of a FB ZVS PWM converter

4.2.4 Operating Conditions of FB ZVS PWM Converter

As described above, all kinds of operating conditions of the FB ZVS PWM converter, including the normal mode and sneak circuit phenomena, are summarized in Table 4.1.

It is found that the reasonable range of the lagging dead time t_{lag} is related to I_{p2}, which is the value of the primary current i_p at $t = t_2$. Substituting Equations 4.1, 4.2, and 4.5 into Equation 4.10, I_{p2} is defined by

$$I_{p2} = V_o \left[\frac{1}{N} \left(\frac{1}{R_L} + \frac{V_i - NV_o}{4V_i L_f f} - \frac{1}{2L_f f} \right) + \frac{V_o}{V_i} \left(\frac{1}{2L_f f} + \frac{2}{N^2 R_L} \right) \right] \tag{4.37}$$

Therefore, any variation of input voltage V_i, output voltage V_o (or duty ratio d), switching frequency f, or load resistance R_L will change the value of I_{p2}, which may result in sneak circuit phenomenon.

Table 4.1 Operating conditions of an FB ZVS PWM converter

Phenomenon	Current condition	Time condition (t_{lag})	Time condition (t_{lead})
Normal	$I_{p2} > I_{crit}$	$t_{lag-\min} < t_{lag} < t_{lag-\max}$	$t_{lead} > \dfrac{2C_{lead}V_i}{I_{p1}}$
Sneak circuit phenomenon I	$I_{p2} > I_{crit}$	$t_{lag} < t_{lag-\min}$	
Sneak circuit phenomenon II		$t_{lag-\max} < t_{lag} < t_{lag-\max} + t_{B-\max}$	
Sneak circuit phenomenon III		$t_{lag} > t_{lag-\max} + t_{B-\max}$	
Sneak circuit phenomenon IV	$I_{p2} < I_{crit}$	$t_{lag} < t_{B\max}$	
Sneak circuit phenomenon V		$t_{B\max} < t_{lag} < 2t_{B\max}$	
Sneak circuit phenomenon VI		$t_{lag} > 2t_{B\max}$	

Notes: $t_{B-\max} = \pi\sqrt{\frac{L_r C_{lag}}{2}}$, $t_{lag-\min} = \frac{\lambda}{\omega_1}$, $t_{lag-\max} = \frac{\lambda}{\omega_1} + \frac{I_{p2}L_r\cos\lambda}{V_i}$, and $\lambda = \sin^{-1}\frac{V_i}{I_{p2}Z_1}$.

4.2.5 Experimental Verification of FB ZVS PWM Converter

A FB ZVS PWM prototype based on Figure 4.1 has been implemented to demonstrate the sneak circuit phenomena and the corresponding conditions. In the prototype, IRFZ44N and SR506 are selected as switch and diode respectively, the control IC is UC3879 and the driving IC is IR2110, and the other parameters are $C_1 = C_3 = C_{lead} = 15$ nF, $C_2 = C_4 = C_{lag} = 22$ nF, $L_r = 26$ μH, $L_f = 300$ μH, $C_f = 2200$ μF, $f = 24$ kHz, $V_i = 20$ V, $V_o = 4$ V, and $N = 1$. Thus it can be calculated that $Z_1 = \sqrt{\frac{L_r}{2C_{lag}}} = 24.3\ \Omega$, $\omega_1 = \frac{1}{\sqrt{2L_r C_{lag}}} = 9.35 \times 10^5$ (rad/s), $I_{crit} = V_i\sqrt{\frac{2C_{lag}}{L_r}} = 0.82$ A, and $t_{B\max} = \pi\sqrt{\frac{L_r C_{lag}}{2}} = 2.05$ μs. In order to verify all the sneak circuit phenomena of the ZVS FB PWM converter proposed above, three different values of lagging time are selected, and the operating process of the prototype will be observed by varying the load resistance.

4.2.5.1 Experimental Results with the First Lagging Time

When $R_L = 2.7\ \Omega$, it is found that $I_{p2} = 1.42$ A $> I_{crit} = 0.82$ A based on Equation 4.37. It is calculated that $I_{p3} = 1.16$ A, $\lambda = 0.617$ rad/s, $t_{lag-\max} =$

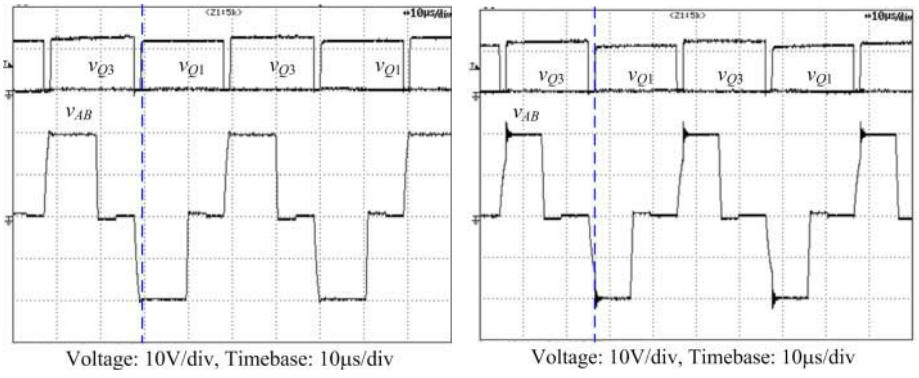


Figure 4.12 Experimental waveforms of a FB ZVS PWM converter when $t_{lag1} = 1.5$ μs: (a) normal operating mode ($R_L = 2.7\ \Omega$); and (b) sneak circuit phenomenon IV ($R_L = 5.3\ \Omega$)

$\frac{\lambda}{\omega_1} + \frac{I_{p2}L_r \cos\lambda}{V_i} = 2.17$ μs, and $t_{lag-\min} = \frac{\lambda}{\omega_1} = 0.66$ μs. By setting the first lagging time $t_{lag1} = 1.5$ μs, that is, $t_{lag-\min} < t_{lag1} < t_{lag-\max}$, the prototype will operate in the normal operating mode according to Table 4.1. Figure 4.12a illustrates the waveforms of driving voltage of switches Q_1 and Q_3 on v_{Q1} and v_{Q3}, and the FB output voltage v_{AB}, which is similar to that in Figure 4.2. The correctness of the theoretical analysis has been verified.

By changing the load resistance to $R_L = 5.3\ \Omega$, it is found that $I_{p2} = 0.67\ \text{A} < I_{crit} = 0.82\ \text{A}$ and $t_{lag1} = 1.5\ \mu\text{s} < t_{B\max} = 2.05\ \mu\text{s}$. The condition of sneak circuit phenomenon IV is satisfied by Table 4.1. The corresponding experimental waveforms are illustrated on Figure 4.12b, which show that v_{AB} begins to decrease when Q_3 is turned off, and Q_1 is turned on before v_{AB} decreases to $-V_i$, but v_{AB} decreases to $-V_i$ very quickly after Q_1 is turned on. Figure 4.12b is similar to the ideal waveforms of sneak circuit phenomenon IV (Figure 4.5), which demonstrates the sneak circuit phenomenon IV and the occurrence of that condition.

4.2.5.2 Experimental Results with the Second Lagging Time

By selecting the load resistance $R_L = 2.5\ \Omega$, it is found that $I_p(t_2) = 1.544\ \text{A} > I_{crit}$, $t_{lag-\min} = 0.5$ μs, and $t_{lag-\max} = 2.3$ μs. The experimental waveforms at the second lagging time $t_{lag2} = 2.2$ μs are illustrated in Figure 4.13a, which show that the prototype is operating in the normal mode, which satisfies the theoretical analysis.

By changing the load to $R_L = 5.7\ \Omega$, it is found that $I_p(t_2) = 0.62\ \text{A} < I_{crit}$ and $t_{B\max} < t_{lag2} = 2.2\ \mu\text{s} < 2t_{B\max}$. According to Table 4.1, the sneak circuit phenomenon V will appear, whose experiment waveforms are illustrated in Figure 4.13b. It is found that v_{AB} does not decrease to $-V_i$ when Q_3 is turned off, then a resonance occurs. v_{AB}

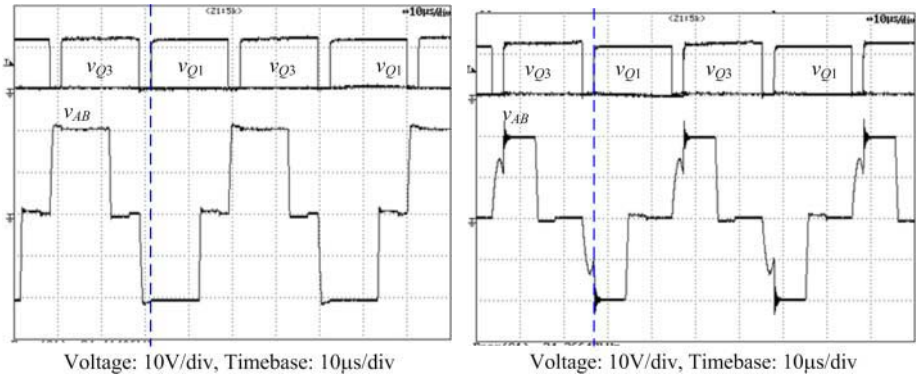


Figure 4.13 Experimental waveforms of a FB ZVS PWM converter when $t_{lag2} = 2.2$ μs: (a) normal operating mode ($R_L = 2.5\ \Omega$); and (b) sneak circuit phenomenon V ($R_L = 5.7\ \Omega$)

decreases to $-V_i$ until Q_1 is turned on, which is similar to the ideal waveform of sneak circuit phenomenon V (Figure 4.10).

4.2.5.3 Experimental Results with the Third Lagging Time

By setting $R_L = 1.2\ \Omega$, it can be achieved that $I_p(t_2) = 3.2\ \text{A} > I_{crit}$, $t_{lag-\min} = 0.28$ μs, and $t_{lag-\max} = 4.3$ μs. By setting the third lagging time to $t_{lag3} = 4.2$ μs, the prototype will operate in the normal mode, as shown in Figure 4.14a.

By changing the load resistance to $R_L = 2.5\ \Omega$, it is found that $I_p(t_2) = 1.544\ \text{A} > I_{crit}$ but $t_{lag-\min} = 0.6$ μs and $t_{lag-\max} = 2.3$ μs. The lagging dead time satisfies the condition of sneak circuit phenomenon II, that is, $t_{B\max} < t_{lag3} = 4.2\ \mu\text{s} < 2t_{B\max}$. The experimental waveforms are illustrated in Figure 4.14b, which show that v_{AB} decreases from zero to $-V_i$ when Q_3 is turned off, and then v_{AB} increases, but Q_1 is turned on before v_{AB} rises to zero, and v_{AB} decreases to $-V_i$ quickly after Q_1 is on. The above process is similar to the ideal waveform of sneak circuit phenomenon II (Figure 4.7), which demonstrates sneak circuit phenomenon II and its occurring condition.

By changing the load resistance to $R_L = 3.3\ \Omega$, it is found that $I_p(t_2) = 1.14\ \text{A} > I_{crit}$, $t_{lag-\min} = 0.86$ μs, and $t_{lag-\max} = 1.89$ μs, thus $t_{lag3} = 4.2\ \mu\text{s} > t_{lag-\max} + t_{B-\max} = 3.94$ μs satisfies the condition of sneak circuit phenomenon III. The corresponding experimental waveforms are illustrated in Figure 4.14c, which is different from Figure 4.14b in that v_{AB} rises to zero before Q_1 is turned on. Therefore, the sneak circuit phenomenon III (Figure 4.9) has been verified.

By increasing the load resistance to $R_L = 8\ \Omega$, it is found that $I_p(t_2) = 0.41\ \text{A} < I_{crit}$ and $t_{lag3} = 4.2\ \mu\text{s} > 2t_{B-\max} = 4.1$ μs, which satisfies the condition of sneak circuit phenomenon VI. The corresponding waveforms are illustrated in Figure 4.14d, in which v_{AB} resonates to zero before Q_1 is turned on, then Q_1 cannot realize ZVS. It

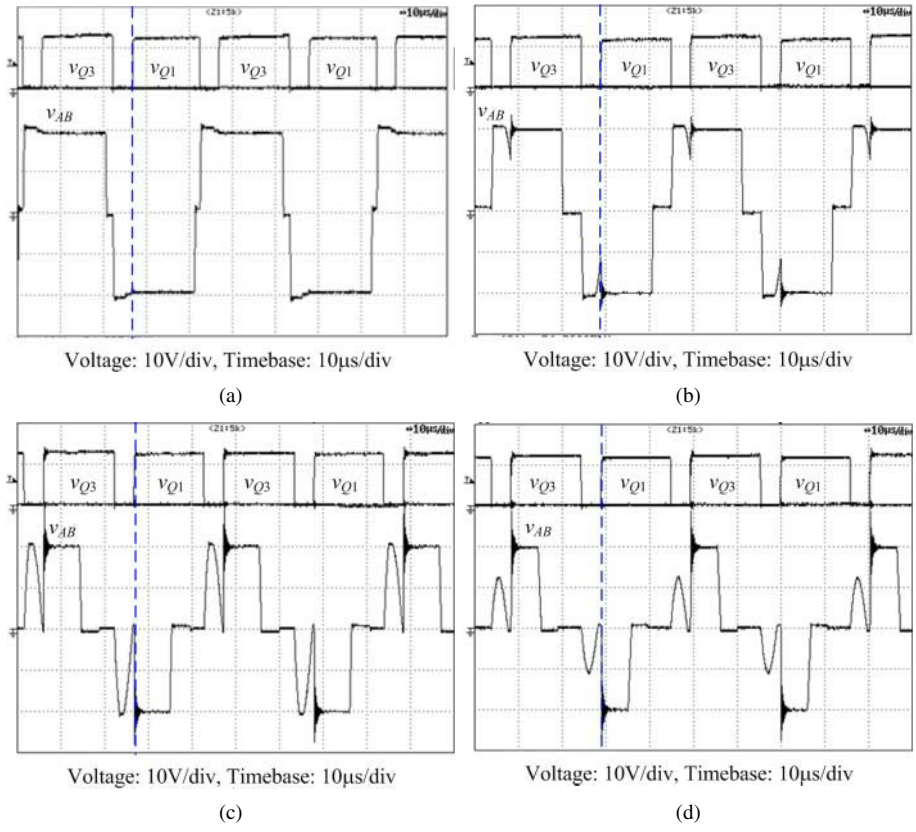


Figure 4.14 Experimental waveforms of a FB ZVS PWM converter when $t_{lag3} = 4.2$ μs: (a) normal operation mode ($R_L = 2.1\ \Omega$); (b) sneak circuit phenomenon II ($R_L = 2.5\ \Omega$); (c) sneak circuit phenomenon III ($R_L = 3.3\ \Omega$); and (d) sneak circuit phenomenon VI ($R_L = 8\ \Omega$)

is clear that sneak circuit phenomenon VI (Figure 4.12) and its appearing conditions have been proven.

Based on Figures 4.12–4.14, all sneak circuit phenomena in the FB ZVS PWM converter, except phenomenon I, have been verified, because $t_{lag-\min}$ is too small and the operating conditions of sneak circuit phenomenon I, that is, $t_{lag} < t_{lag-\min}$, is too hard to be satisfied. It is obvious that ZVS of the lagging leg Q_1 and Q_3 will not be achieved only by varying the load resistance, and different kinds of sneak circuit phenomenon will appear.

4.3 Sneak Circuits of Buck ZVS Multi-Resonant Converter

The quasi-resonant (QR) converter is one of the earliest soft switching converters, in which only one switching component (switch or diode) can achieve soft switching.

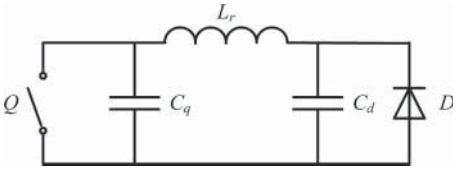


Figure 4.15 Equivalent circuit of an ZV MRS

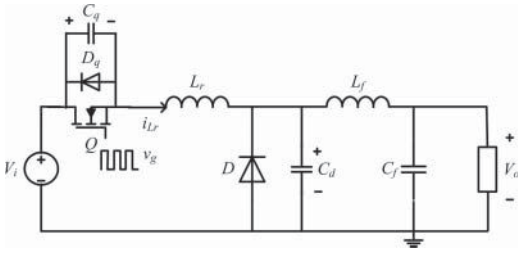


Figure 4.16 Schematic diagram of a Buck ZVS MR converter

In order to realize soft switching of both switch and diode, a multi-resonant (MR) converter is proposed [2]. A zero-voltage multi-resonant switch (ZV MRS) is illustrated in Figure 4.15, where the resonant capacitors C_q and C_d are in parallel with switch Q and diode D respectively. Resonant inductor L_r is connected between C_q and C_d in the type of Π network. In practice, ZV MRS is generally used, because the junction capacitance of switch Q or diode D can be made use of.

Applying the concept of ZV MRS to the Buck converter, a Buck ZVS MR converter can be obtained, as in Figure 4.16, where D_q is the parasitic or anti-parallel diode of Q.

4.3.1 Normal Operating Mode of Buck ZVS MR Converter

Before analyzing the operating principle of the Buck ZVS MR converter, the following assumptions are made.

1. All the components in the Buck ZVS MR converter can be regarded as ideal, that is, all parasitic resistances are zero, and the conduction voltage drop is also zero.
2. The filter inductance is much larger than the resonant inductance, $L_f >> L_r$.
3. The output side can be considered as a constant current source I_o, because the filter inductance is very large.

The typical waveforms of a Buck ZVS MR converter in normal operating mode are illustrated in Figure 4.17. It is found that there are four stages in one switching cycle, and the equivalent circuits of operating stages are shown in Figure 4.18.

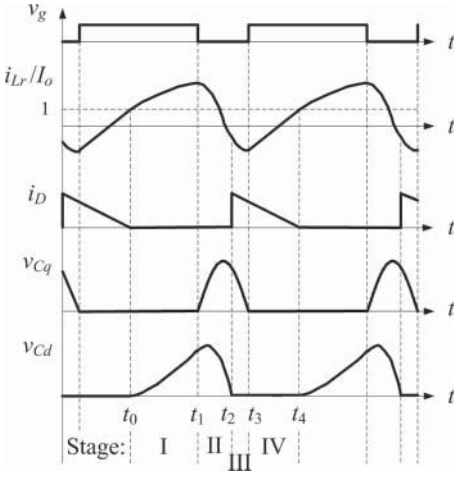


Figure 4.17 Typical waveforms of a Buck ZVS MR converter in normal operating mode

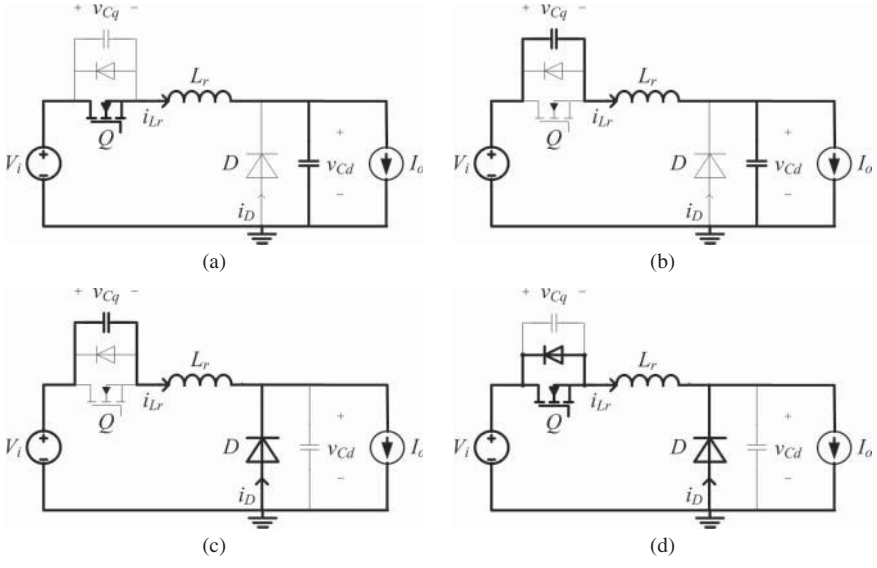


Figure 4.18 Equivalent circuits of a Buck ZVS MR converter in normal operating mode: (a) stage I; (b) stage II; (c) stage III; and (d) stage IV

Stage I (t_0, t_1)

As shown in Figure 4.18a, switch Q is conducting, diode D is reverse biased because v_{Cd} is always positive, and L_r resonates with C_d during stage I.

It is known that the initial conditions of stage I are $i_{Lr}(t_0) = I_o$, $v_{Cq}(t_0) = 0$, and $v_{Cd}(t_0) = 0$, and the expressions of i_{Lr}, v_{Cq}, and v_{Cd} during stage I can be given by

$$i_{Lr}(t) = I_o + \frac{V_i}{Z_{rd}} \sin \omega_{rd}(t - t_0) \tag{4.38}$$

$$v_{Cq}(t) = 0 \tag{4.39}$$

$$v_{Cd}(t) = V_i[1 - \cos \omega_{rd}(t - t_0)] \tag{4.40}$$

where $Z_{rd} = \sqrt{\frac{L_r}{C_d}}$ and $\omega_{rd} = \frac{1}{\sqrt{L_r C_d}}$.

Stage II (t_1, t_2)

As shown in Figure 4.18b, when switch Q is turned off at t_1, C_q and C_d begin resonance with L_r. Q operates in zero-voltage turn-off as the voltage v_{Cq} rises from zero slowly. i_{Lr}, v_{Cq}, and v_{Cd} can be given by

$$\begin{aligned} i_{Lr}(t) = {} & I_{Lr}(t_1) \cos \omega_{rqd}(t - t_1) + \frac{I_o C_q}{C_q + C_d}[1 - \cos \omega_{rqd}(t - t_1)] \\ & + \frac{1}{Z_{rqd}} \left[V_i - V_{Cd}(t_1) \left(1 - \frac{C_q}{C_d} \right) \right] \sin \omega_{rqd}(t - t_1) \end{aligned} \tag{4.41}$$

$$\begin{aligned} v_{Cq}(t) = {} & \frac{I_o}{C_q + C_d}(t - t_1) + \frac{1}{\omega_{rqd}} \left[\frac{I_{Lr}(t_1)}{C_q} - \frac{I_o}{C_q + C_d} \right] \sin \omega_{rqd}(t - t_1) \\ & + \frac{C_d}{C_q + C_d}[V_i - V_{Cd}(t_1)][1 - \cos \omega_{rqd}(t - t_1)] \end{aligned} \tag{4.42}$$

$$\begin{aligned} v_{Cd}(t) = {} & V_{Cd}(t_1) + \frac{C_q}{C_q + C_d}[V_i - V_{Cd}(t_1)][1 - \cos \omega_{rqd}(t - t_1)] \\ & + \frac{1}{\omega_{rqd} C_d} \left[I_{Lr}(t_1) - \frac{C_q I_o}{C_q + C_d} \right] \sin \omega_{rqd}(t - t_1) - \frac{I_o}{C_q + C_d}(t - t_1) \end{aligned} \tag{4.43}$$

where $Z_{rqd} = \sqrt{\frac{L_r}{C_e}}$, $\omega_{rqd} = \frac{1}{\sqrt{L_r C_e}}$, and $C_e = \frac{C_q C_d}{C_q + C_d}$.

Stage II terminates when v_{Cd} reduces to zero at t_2, and diode D turns on under zero-voltage.

Stage III (t_2, t_3)

As shown Figure 4.18c, since switch Q is off and diode D is on, C_q is resonant with L_r. The expressions of i_{Lr}, v_{Cq}, and v_{Cd} during stage III are

$$i_{Lr}(t) = \frac{1}{Z_{rq}}[V_i - V_{Cq}(t_2)] \sin \omega_{rq}(t - t_2) + I_{Lr}(t_2) \cos \omega_{rq}(t - t_2) \tag{4.44}$$

$$v_{Cq}(t) = V_{Cq}(t_2) \cos \omega_{rq}(t - t_2) + Z_{rq} I_{Lr}(t_2) \sin \omega_{rq}(t - t_2) + V_i[1 - \cos \omega_{rq}(t - t_2)] \tag{4.45}$$

$$v_{Cd}(t) = 0 \tag{4.46}$$

where $Z_{rq} = \sqrt{\frac{L_r}{C_q}}$ and $\omega_{rq} = \frac{1}{\sqrt{L_r C_q}}$.

When v_{Cq} decreases to zero at t_3, stage III is ended, and D_q is turned on. As a result, switch Q can be turned on with the zero-voltage condition.

Stage IV (t_3, t_4)

As shown in Figure 4.18d, when the converter enters into stage IV, diodes D and D_q keep conducting as a result of $i_D > I_o$ and $i_{Lr} < 0$. The voltage on the resonant inductor L_r is equal to input voltage V_i, so i_{Lr} will increase linearly. The expressions of i_{Lr}, v_{Cq}, and v_{Cd} during stage IV are

$$i_{Lr}(t) = \frac{V_i}{L_r}(t - t_3) + I_{Lr}(t_3) \tag{4.47}$$

$$v_{Cq}(t) = 0 \tag{4.48}$$

$$v_{Cd}(t) = 0 \tag{4.49}$$

Switch Q should be turned on before i_{Lr} becomes positive, or zero-voltage turn on cannot be achieved. At the moment of t_4, $i_{Lr}(t_4) = I_o$, diode D is turned off naturally and i_{Lr} flows through switch Q, and stage IV is followed by stage I.

Based on the above analysis, except for the operating stage IV, the other three stages operate in resonance, and the resonant frequency varies in every stage because the resonant elements are different. Therefore, this converter is known as a MR converter.

4.3.2 Sneak Circuit Phenomenon of Buck ZVS MR Converter

If circuit parameters or operating conditions of the Buck ZVS MR converter are changed, v_{Cq} reduces to zero before v_{Cd} during stage II, then a new operating stage III′, which is the sneak stage, will appear and its equivalent circuit is illustrated in Figure 4.19. During stage III′, when v_{Cq} reduces to zero at t_2, D_q is turned on, then C_d

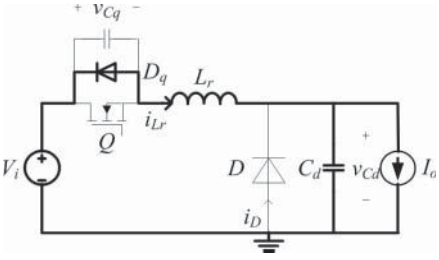


Figure 4.19 Equivalent circuit of the sneak stage in a Buck ZVS MR converter

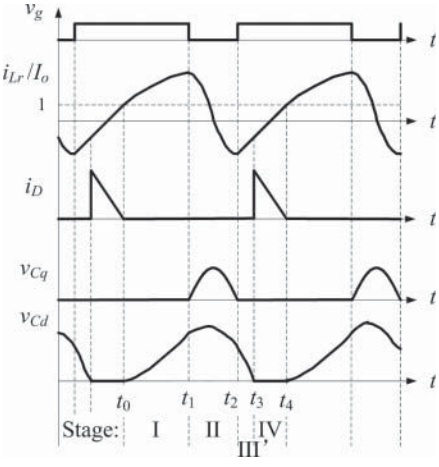


Figure 4.20 Typical waveforms of a Buck ZVS MR converter in sneak circuit mode

will resonate with L_r. When v_{Cd} reduces to zero, stage III′ will finish and the converter will enter the normal operating stage IV. The typical waveforms of the Buck ZVS MR converter in sneak circuit mode are illustrated in Figure 4.20.

Based on Equations 4.42 and 4.43, the sneak circuit conditions at which stage III′ will appear can be expressed as

$$\begin{cases} v_{Cq}(t_2) = 0 \\ v_{Cd}(t_2) > 0 \end{cases} \tag{4.50}$$

where $t_2 - t_1 = (1 - d)T$, d is duty ratio, and T is the switching cycle.

When sneak circuit phenomenon occurs, it is found that both switch Q and diode D can keep zero-voltage turn-on, although the resonant stage is different from normal operation. But the output voltage, the voltage and current stresses of the components may change and have unpredictable influences.

4.3.3 Simulation Verification of Buck ZVS MR Converter

In order to demonstrate the correctness of the above-mentioned analysis, a Buck ZVS MR prototype based on reference [3] was built in PSIM® and the simulation parameters were $V_i = 10$ V, $L_r = 1.36$ μH, $C_s = 13.6$ nF, $C_d = 40.8$ nF, $C_f = 50$ μF, and $L_f = 50$ μH. By changing the switching frequency f_s or load resistance R_L, the driving voltage v_{gs} for switch Q, resonant inductor current i_{Lr}, and resonant capacitor voltages v_{Cq} and v_{Cd}, are illustrated in Figure 4.21, which is consistent with the experimental waveforms in reference [3].

In Figure 4.21a, v_{Cd} reduces to zero earlier than v_{Cq}, which satisfies Figure 4.17. It is obvious that the Buck ZVS MR converter operates in normal operating mode. Figure 4.21b illustrates the critical mode that v_{Cd} and v_{Cq} decrease to zero simultaneously. However, v_{Cq} decreases to zero earlier than v_{Cd} in Figure 4.21c, which is the same as the sneak circuit phenomenon in Figure 4.20.

Comparing Figures 4.21a–c, it is proven that sneak circuit phenomenon will occur by changing the switching frequency or load resistance, which demonstrates the correctness of the above analysis.

4.4 Sneak Circuits of Buck ZVT PWM Converter

In QR converters and MR converters, both resonant inductor and resonant capacitor are involved in the process of energy transfer, and their voltage and current stresses are large as a result. In ZVS PWM converters and ZCS (zero-current switching) PWM converters, resonant inductor is in series with the main power circuit, and the voltage and current stress of switches and resonant devices are also large. In order to overcome the above shortcomings, a zero-voltage-transition (ZVT) converter was proposed in the early 1990s [4]. In this kind of converter, the resonant tank is in parallel with the main switch, and the resonant time is controlled by the auxiliary switch. Thus, the ZVT converter has the following advantages:

1. All of the switching components can achieve ZVS.
2. The main circuit for power transmission does not contain resonant elements. As a result, the voltage and current stresses of the main circuit are relatively small.
3. The constant frequency characteristic of PWM converter can be retained
4. Compared with other kinds of soft switching converters, the range of supply voltage and load resistance in zero switching loss is broadened.

As there is a resonant tank in the ZVT converter, it is likely that sneak circuit paths exist in the ZVT converter. The Buck ZVT PWM converter shown in Figure 4.22 will be used as an example to discuss the sneak circuit phenomena in a ZVT converter.

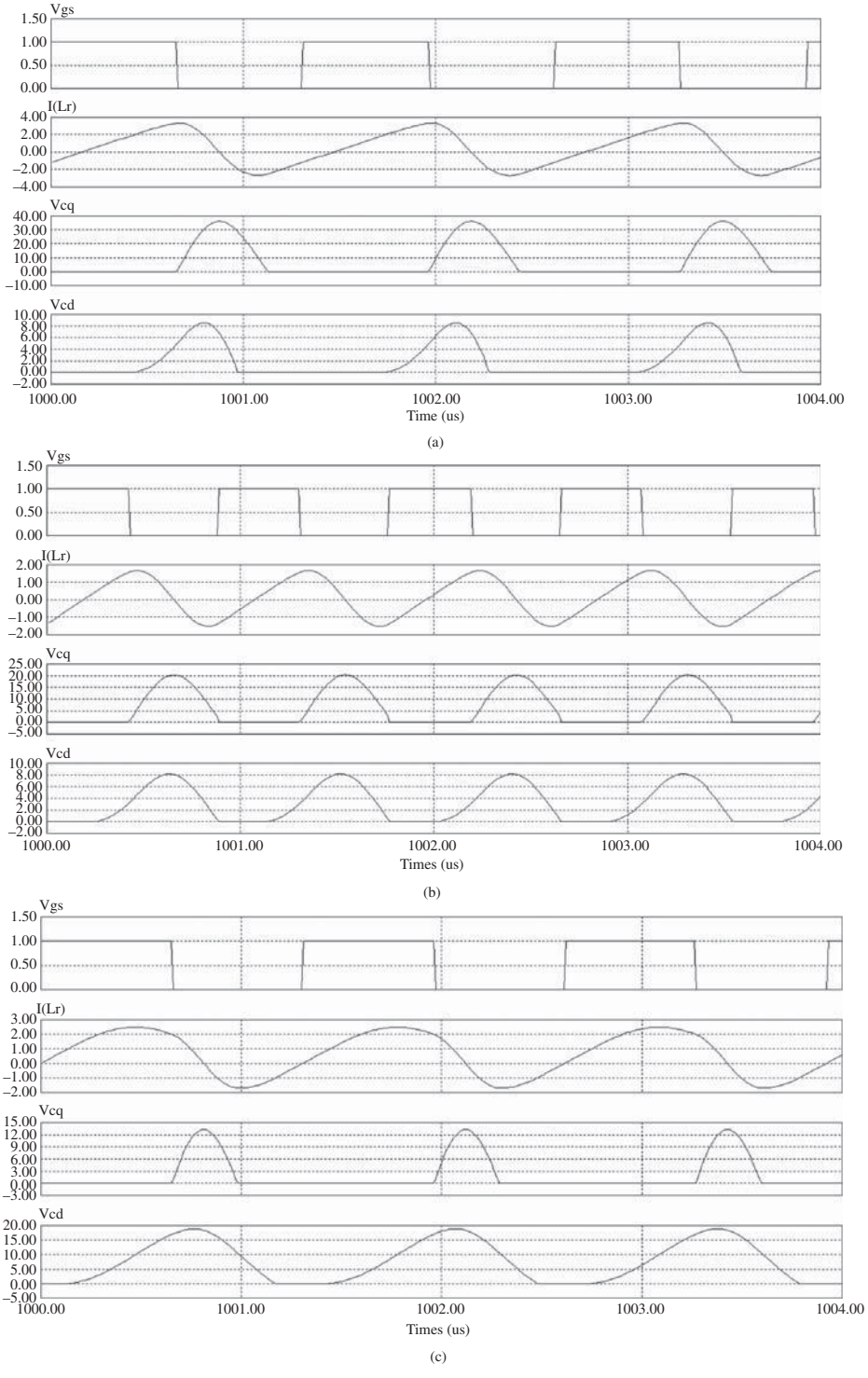


Figure 4.21 Simulation waveforms of a Buck ZVS MR prototype: (a) $f_s = 765$ kHz, $R_L = 1\ \Omega$; (b) $f_s = 1.13$ MHz, $R_L = 10\ \Omega$; and (c) $f_s = 765$ kHz, $R_L = 10\ \Omega$

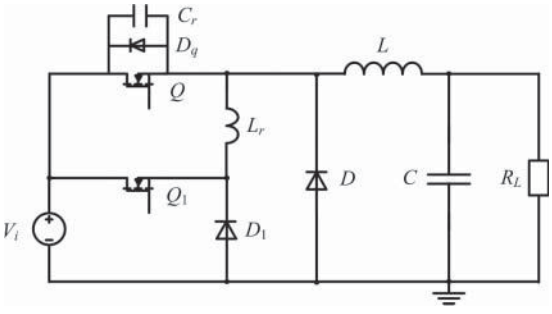


Figure 4.22 Schematic diagram of a Buck ZVT PWM converter

4.4.1 Normal Operating Mode of Buck ZVT PWM Converter

In the Buck ZVT PWM converter, an auxiliary switch Q_1, auxiliary freewheeling diode D_1, and resonant inductor L_r are added with respect to the traditional Buck converter. In addition, resonant capacitor C_r includes the parasitic capacitance of main switch Q, and D_q indicates the anti-parallel diode of switch Q. In order to simplify the analysis, the following assumptions are made.

1. All the components are regarded as ideal ones.
2. The current flowing through filter inductor L can be considered as constant current I_o, because the filter inductance is large enough.
3. The output voltage V_o remains constant, because the output capacitor C is large enough.

The typical operating waveforms of a Buck ZVT PWM converter in normal operating mode are illustrated in Figure 4.23. It is obvious that each switching cycle can be divided into eight stages, whose equivalent circuits are illustrated in Figure 4.24. The brief analysis of various operating stages is described as follows [4].

Stage I (t_0, t_1)

Referring to Figure 4.24a, the main switch Q is turned on and input voltage source V_i provides energy to load through Q.

Stage II (t_1, t_2)

Referring to Figure 4.24b, if Q is turned off at t_1, V_i charges to resonant capacitor C_r, and v_{Cr} increases linearly. Stage II is ended when $v_{Cr} = V_i$.

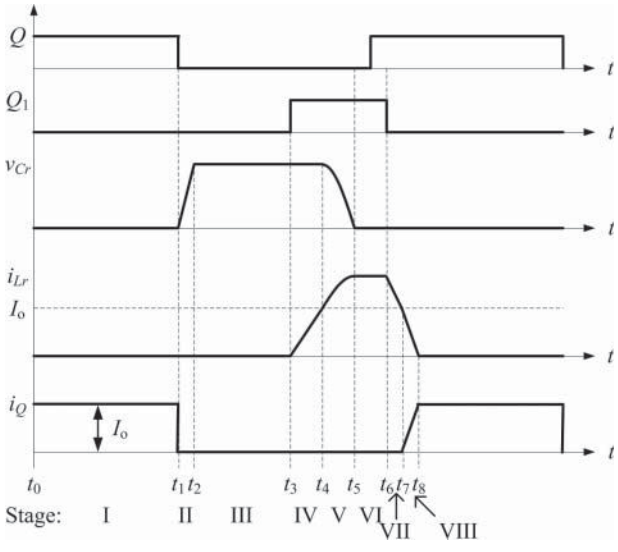


Figure 4.23 Typical waveforms of a Buck ZVT-PWM converter in normal operating mode

Stage III (t_2, t_3)

Referring to Figure 4.24c, as both Q and Q_1 are in the off state, the current flows through the main diode D and $v_{Cr} = V_i$.

Stage IV (t_3, t_4)

Referring to Figure 4.24d, the auxiliary switch Q_1 is turned on at t_3, i_{Lr} increases and i_D decreases linearly to zero, D is turned off and stage IV is finished.

Stage V (t_4, t_5)

Referring to Figure 4.24e, as inductor L_r is resonant with resonant capacitor C_r. When v_{Cr} decreases to zero, D_q is turned on. Then v_{Cr} is clamped to zero, which creates the zero-voltage turn-on condition for Q.

Stage VI (t_5, t_6)

Referring to Figure 4.24f, i_{Lr} remains constant because the voltage across L_r is equal to zero. In this stage, Q can be turned on in zero voltage, but the current will not flow through Q until Q_1 is turned off and i_{Lr} decreases to I_o.

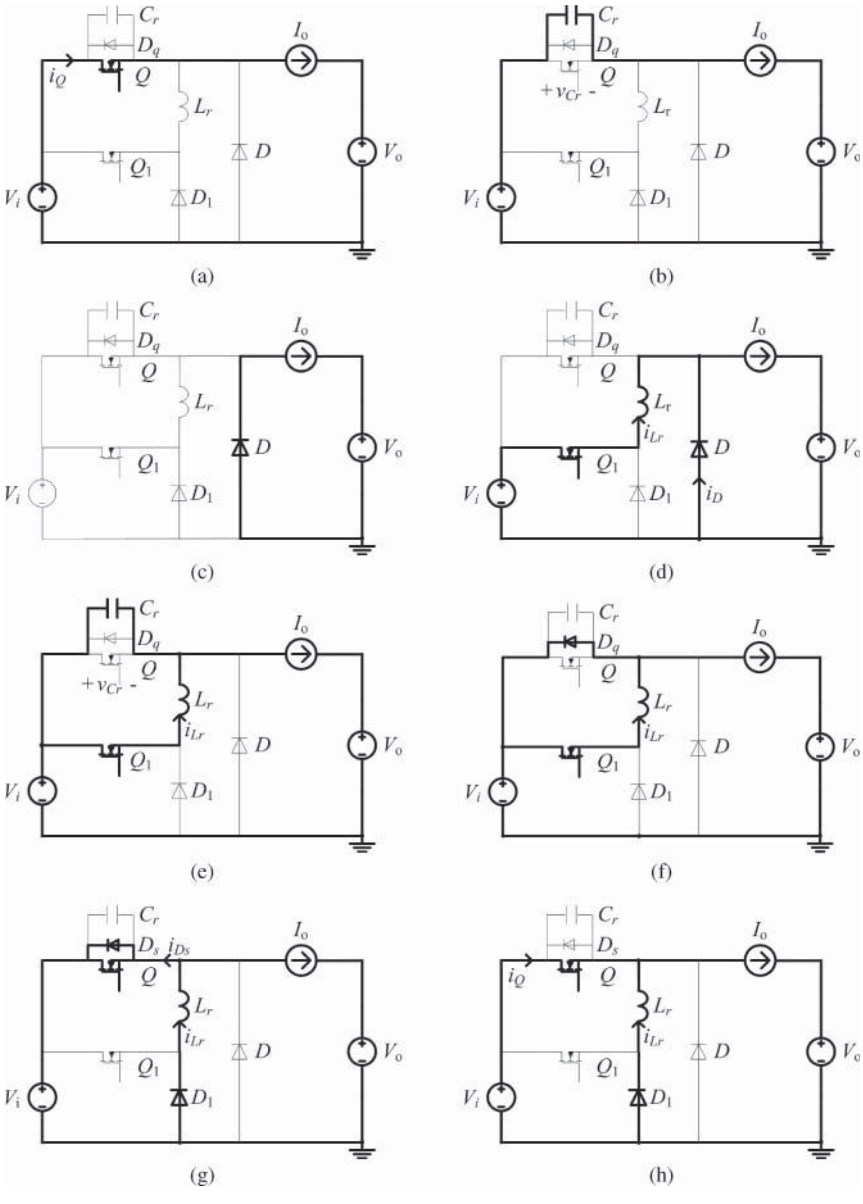


Figure 4.24 Equivalent circuits of a Buck ZVT PWM converter in normal operating mode: (a) stage I; (b) stage II; (c) stage III; (d) stage IV; (e) stage V; (f) stage VI; (g) stage VII; and (h) stage VIII

Stage VII (t_6, t_7)

Referring to Figure 4.24g, if Q_1 is turned off at t_6 and the auxiliary diode D_1 is turned on, which provides a freewheeling path i_{Lr}. i_{Lr} begins to decrease and stage VII is finished until i_{Lr} decreases to I_o.

Stage VIII (t_7, t_8)

Referring to Figure 4.24h, if $i_{Lr} = I_o$ at t_7, i_Q will increase from zero and i_{Lr} will decrease linearly. Stage VIII will terminate until i_{Lr} reduces to zero and one switching cycle is ended.

4.4.2 Sneak Circuit Phenomenon of Buck ZVT PWM Converter

The auxiliary switch Q_1 normally contains parasitic capacitance C_{q1}, and the Buck ZVT PWM converter with parasitic parameters is shown in Figure 4.25 [4]. When the capacitance of C_{q1} cannot be ignored, C_{q1} will construct a new current path with resonant inductor L_r and resonant capacitor C_r, and provide a reverse current path for i_{Lr}. As a result, sneak circuit phenomenon will appear, and the corresponding operation can be described as follows.

Stage (t_0, t_1)

The main switch Q conducts, i_{Lr} equals to zero, and the input voltage source V_i provides energy to load through Q, which is the same as the normal stage I.

Stage (t_1, t_2)

If Q is turned off at t_1, and the auxiliary switch Q_1 is still off at this time, V_i charges to C_r and C_{q1} synchronously and i_{Lr} decreases. The equivalent circuit of this stage,

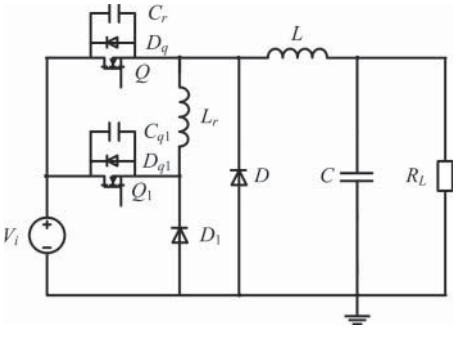


Figure 4.25 Schematic diagram of a Buck ZVT PWM with parasitic parameters

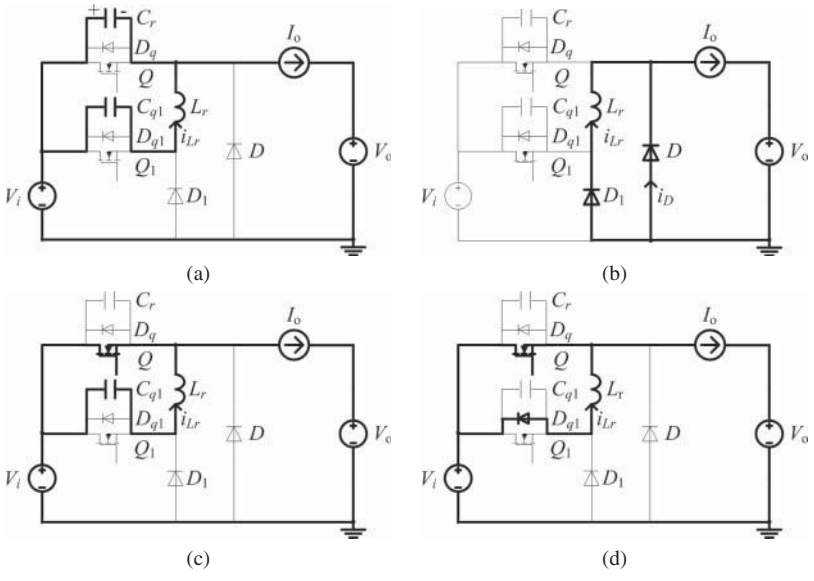


Figure 4.26 Equivalent circuits of the sneak stages in a Buck ZVT PWM converter: (a) stage I′; (b) stage II′; (c) stage III′; and (d) stage IV′

which is named as stage I′, is illustrated in Figure 4.26a. Stage I′ will be finished when v_{Cr} increases to V_i.

Stage (t_2, t_3)

Diode D is turned on when the voltage across it is positive, and then D_1 is also turned on, then the output current flows through D and the series branch D_1 and L_r. The equivalent circuit of this stage, which is named as stage II′, is illustrated in Figure 4.26b. i_{Lr} keeps constant as the voltage across L_r is equal to zero.

Stage (t_3, t_4)

Assuming that Q_1 is turned on at t_3 and D_1 is turned off under negative voltage, this stage is the same as normal stage IV. i_{Lr} increases linearly and i_D decreases linearly, D is turned off when $i_{Lr} = I_o$, and this stage is ended.

Stage (t_4, t_5)

Assuming that D is turned off at t_4, this stage is the same as normal stage V. Resonant inductor L_r is resonant with resonant capacitor C_r, then v_{Cr} decreases and i_{Lr} increases in a sinusoidal way. When v_{Cr} decreases to zero and D_q is turned on, this stage is ended.

Stage (t_5, t_6)

This stage is the same as normal stage VI, in which the main switch Q can achieve zero voltage turn-on.

Stage (t_6, t_7)

Assuming that Q_1 is turned off and D_1 is turned on at t_6, this stage is the same as normal stage VII, which will be terminated when i_{Lr} reduces to I_o.

Stage (t_7, t_8)

This stage is the same as normal stage VIII. i_Q increases from zero linearly and i_{Lr} keeps decreasing at this stage. This stage will be ended when i_{Lr} reduces to zero and D_1 is turned off.

Stage (t_8, t_9)

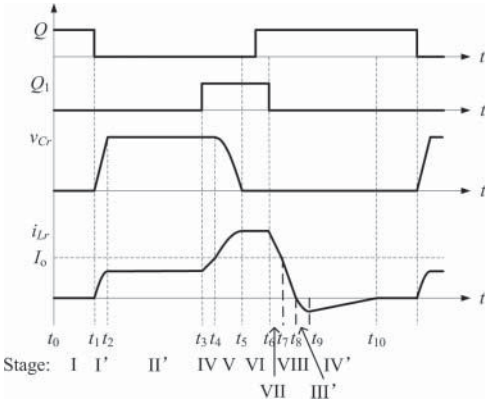
The resonant inductor current i_{Lr} keeps decreasing because L_r resonates with C_{q1}. The equivalent circuit of this stage, which is named as stage III′, is illustrated in Figure 4.26c. This stage will be ended when the voltage on C_{s1} decreases to zero and D_{q1} is turned on.

Stage (t_9, t_{10})

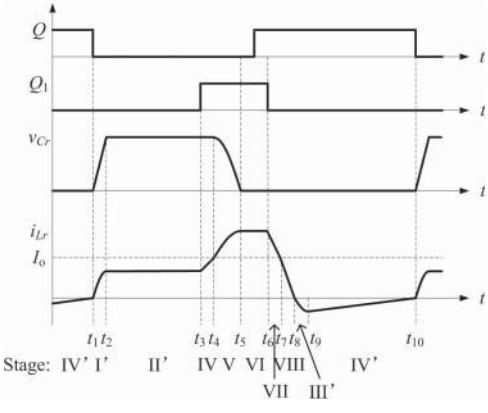
Assuming that D_{q1} is turned on at t_9, the equivalent circuit of this stage, which is named as stage IV′, is illustrated in Figure 4.26d. Because the voltage across L_r is equal to the voltage drop on Q, i_{Lr} increases linearly and this stage ends when i_{Lr} is equal to zero. Then the converter enters stage I again and another operating cycle begins.

The corresponding waveforms are illustrated in Figure 4.27a, in which the resonant inductor current i_{Lr} is discontinuous. If i_{Lr} does not increase to zero before the main switch Q is turned off, stage I will not appear in the operating process, so stage I′ will follow stage IV′ directly and i_{Lr} becomes continuous. The corresponding waveforms are illustrated in Figure 4.27b.

Comparing the waveforms in Figure 4.27 with those in Figure 4.23, the characteristics of the Buck ZVT PWM converter change obviously when the sneak circuit phenomenon occurs. Because the parasitic capacitance of the auxiliary switch Q_1, that is, C_{q1}, cannot be ignored, there is internal commutation during operation, which will increase the conduction loss of the main switch; on the other hand, the turn-on time of D_1 (stage II′) is increased, which will lead to the efficiency drop.



(a)



(b)

Figure 4.27 Typical waveforms of a Buck ZVT-PWM converter in sneak circuit mode: (a) i_{Lr} is discontinuous; and (b) i_{Lr} is continuous

4.4.3 Simulation Verification of Buck ZVT PWM Converter

In order to demonstrate the correctness of the above analysis, a simulation circuit of a Buck ZVT PWM converter was designed in PSIM® based on Figure 4.25. If Power MOSFET IRF460 was selected for the auxiliary switch, then $C_{s1} = 480$ pF and the other parameters were $V_i = 100$ V, $V_o = 50$ V, $L_r = 100$ μH, $C_r = 10$ nF, $C = 100$ μF, $R_L = 25$ Ω, and $f_s = 50$ kHz.

Simulation waveforms are illustrated in Figure 4.28, from top to bottom of the figure, there are driving signal of main switch Q (i.e. v1), driving signal of auxiliary switch Q_1 (i.e. v2), resonant capacitor voltage v_{Cr}, output voltage V_o, and resonant inductor current i_{Lr}. It can be observed that i_{Lr} is continuous, which is the same as that in Figure 4.27b and the correctness of sneak circuit phenomenon is proven.

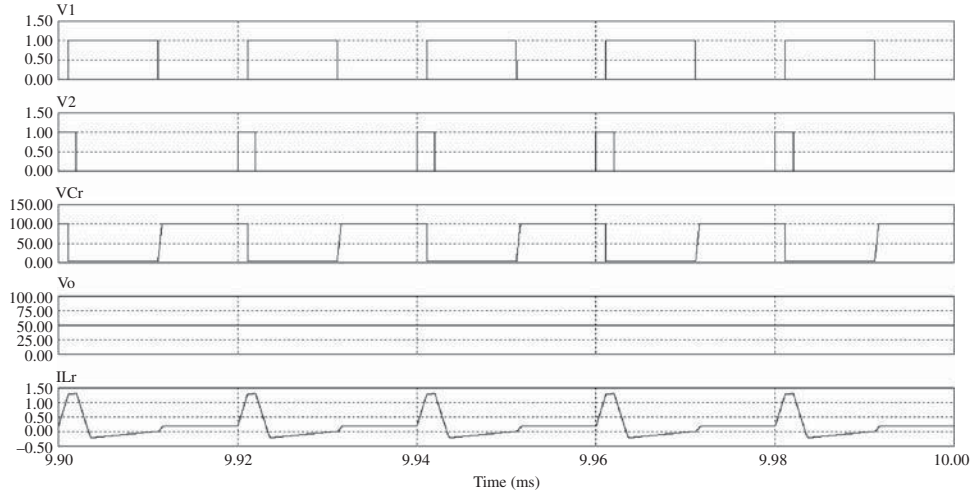


Figure 4.28 Simulation waveforms of a Buck ZVT PWM converter in sneak circuit phenomenon

4.5 Summary

This chapter introduced some sneak circuit phenomena in soft-switching converters, and took FB ZVS PWM converter, Buck ZVS MR converter, and Buck ZVT PWM converter as examples. Compared with the hard-switching converter, it can be concluded that the amount of sneak circuit paths are more and the sneak circuit phenomena are more complex in the soft-switching converters because of the resonant tank. So the sneak circuit phenomenon of soft-switching converters should be avoided, or it will lead to the unpredicted influence on the converter.

References

[1] Sabate, J.A., Vlatkovic, V., Ridely, R. *et al*. (1990) Design considerations for high-power full-bridge ZVS-PWM converter. IEEE Applied Power Electronic Conference Proceeding, pp. 275–284.

[2] Tabisz, W.A. and Lee, F.C. (1989) Zero-voltage-switching multi-resonant technique- a novel approach to improve performance of high-frequency quasi-resonant converters. *IEEE Transactions on Power Electronics*, **4** (4), 450–458.

[3] Tabisz, W.A. and Lee, F.C. (1989) DC analysis and design of zero-voltage-switched multi-resonant converters. IEEE Power Electronics Specialists Conference Proceedings (PESC), pp. 243–251.

[4] Hua, G., Leu, C., Jiang, Y. *et al.* (1994) Novel zero-voltage-transition PWM converters. *IEEE Transactions on Power Electronics*, **9** (2), 213–219.

5

Sneak Circuits of other Power Electronic Converters

5.1 Introduction

Most topologies of power electronic converters are significantly dependent on the inspirations and experiences of designers and there are no rigorous theories or methods to follow, which may lead to some paths or states in the power electronic converter, which are unknown to the designers. The sneak circuit phenomena existed in some common power electronic converters have been described in Chapters 2–4. In this chapter, two new types of power electronic converters, the Z-source inverter and the synchronous rectifier DC-DC converter, will be discussed.

5.2 Sneak Circuits of Z-Source Inverter

The impedance-source (or impedance-fed) power electronic converter (abbreviated as the Z-source converter) is a new type of power electronic converter, which couples the converter (or inverter) to the dc source or load by introducing an impedance network. The general structure of a Z-source converter is presented in Figure 5.1, where the unique impedance network consists of split inductors L_1 and L_2 and capacitors C_1 and C_2 connected in an X-shape [1]. By selecting a suitable control method, the Z-source converter can implement DC-AC, AC-DC, AC-AC, and DC-DC power conversion, and operate in open or short circuit states that cannot be observed in traditional voltage-source and current-source converters. The advantage of the Z-source converter is that it can connect the power source in any form to the converter main circuit, and can provide power for any load. As the power source, main circuit, and load in the Z-source converter are flexible, there are many forms of Z-source converters. In this section, the Z-source inverter is taken as an example to illustrate the sneak circuit phenomenon in the Z-source converter.

Sneak Circuits of Power Electronic Converters, First Edition. Bo Zhang and Dongyuan Qiu.

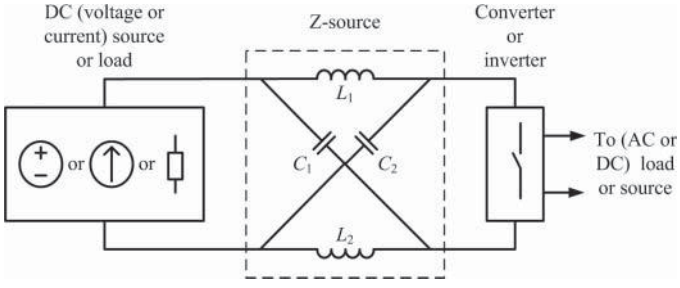


Figure 5.1 General structure of the Z-source converter [1]

5.2.1 Operating Principles of Z-Source Inverter

The schematic diagram of a three-phase Z-source inverter is shown in Figure 5.2, in which the diode *D* is used to prevent the reverse current flowing into the dc source (for example, the fuel-cell). The three-phase inverter can work in both the shoot-through state and the nonshoot-through state of the lower and upper components of the same leg, due to the existence of the Z-source impedance.

Therefore, the inverter bridge will have nine permissible switching states or voltage vectors, including six active states (or status I) when the dc voltage is applied to the load directly, two traditional zero states (or status II) when the load terminals are shorted through either the lower or upper three devices, and one zero vector when the load terminals are shorted, namely is the shoot-through zero state (or status III), which is forbidden in the traditional voltage source inverter [1].

In order to simplify the analysis, the impedance network generally uses the symmetrical structure with $L_1 = L_2$ and $C_1 = C_2$. Then each normal operating mode of the Z-source inverter will be discussed based on the relationships $V_{C1} = V_{C2} = V_C$, $v_{L1} = v_{L2} = v_L$, and $i_{L1} = i_{L2} = i_L$.

Status I

The three-phase inverter bridge is equivalent to a current source I_i when it is in one of the active states. The equivalent circuit of the Z-source inverter is shown in Figure 5.3a, which gives

$$\begin{cases} v_d = V_{DC} \\ v_L = V_{DC} - V_C \\ v_i = V_C - v_L = 2V_C - V_{DC} \\ i_D = 2i_L - I_i \end{cases} \tag{5.1}$$

where V_{DC} is the voltage of input voltage source, V_d is the input voltage of the impedance network, v_i is the output voltage of the impedance network or the input dc voltage of the inverter bridge, and i_D is the diode current.

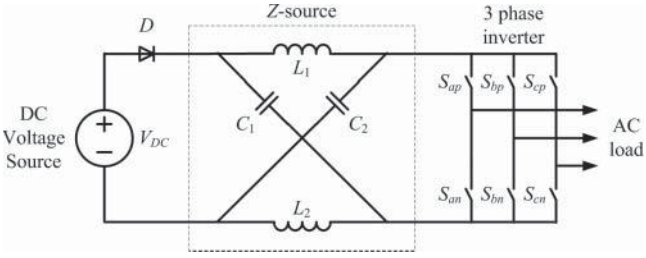
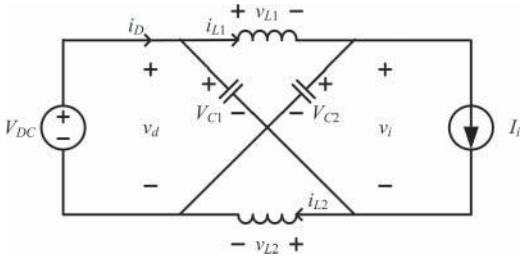


Figure 5.2 Schematic diagram of the three phase Z-source inverter



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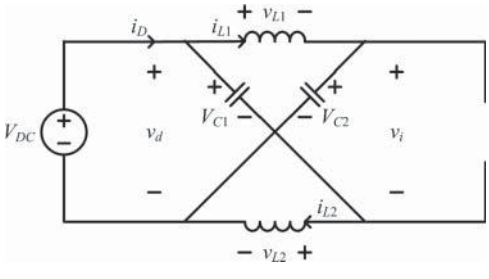
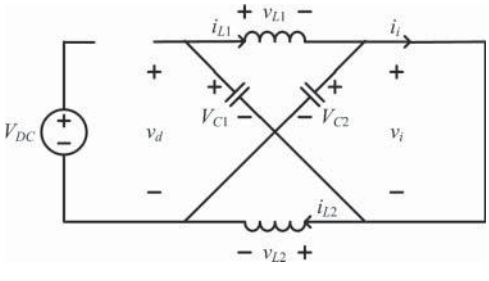


(b)



(c)

Figure 5.3 Equivalent circuits of the Z-source inverter in normal operating mode: (a) status I – inverter's active state; (b) status II – inverter's traditional zero state; and (c) status III – inverter's shoot-through zero state

Status II

The inverter bridge is represented by a current source with zero value or an open circuit when it is in one of the two traditional zero states. The equivalent circuit of the Z-source inverter is shown in Figure 5.3b, which gives

$$\begin{cases} v_d = V_{DC} \\ v_L = V_{DC} - V_C \\ v_i = 2V_C - V_{DC} \\ i_i = 0 \\ i_D = 2i_L \end{cases} \tag{5.2}$$

Status III

The load terminal is equivalent to a short circuit when the inverter bridge is in the shoot-through zero state. Since the capacitor voltage V_C is almost constant and $2V_C > V_{DC}$ based on Equations 5.1 and 5.2, diode D is subject to the reverse voltage and turn off. The equivalent circuit of the Z-source inverter is shown in Figure 5.3c, so we have

$$\begin{cases} v_L = V_C \\ v_d = 2V_C \\ v_i = 0 \\ i_D = 0 \end{cases} \tag{5.3}$$

According to the above analysis, the typical waveforms when the Z-source inverter is in normal operating modes are shown in Figure 5.4, where v_a, v_b, and v_c are the three phase reference voltages respectively, and v_{ps} and v_{ns} are used to control the shoot-through time.

Assuming that in one switching cycle T, the inverter bridge is in the shoot-through zero state (or status III) for an interval of T_0, $D = \frac{T_0}{T}$ is defined as the duty cycle of shoot-through zero state, and the inverter bridge in the nonshoot-through zero state (or statuses I and II) for an interval of T_1, and T_1 satisfies $T_0 + T_1 = T$.

The average voltage of the inductors over one switching cycle T is equal to zero in steady state, and from Equations 5.1–5.3, we have

$$V_C = \frac{1 - D}{1 - 2D} V_{DC} \tag{5.4}$$

According to Equation 5.1, the peak dc-link voltage across the inverter bridge is expressed as $V_{i\max} = 2V_C - V_{DC}$, and substituting it into Equation 5.4 gives

$$V_{i\max} = BV_{DC} \tag{5.5}$$

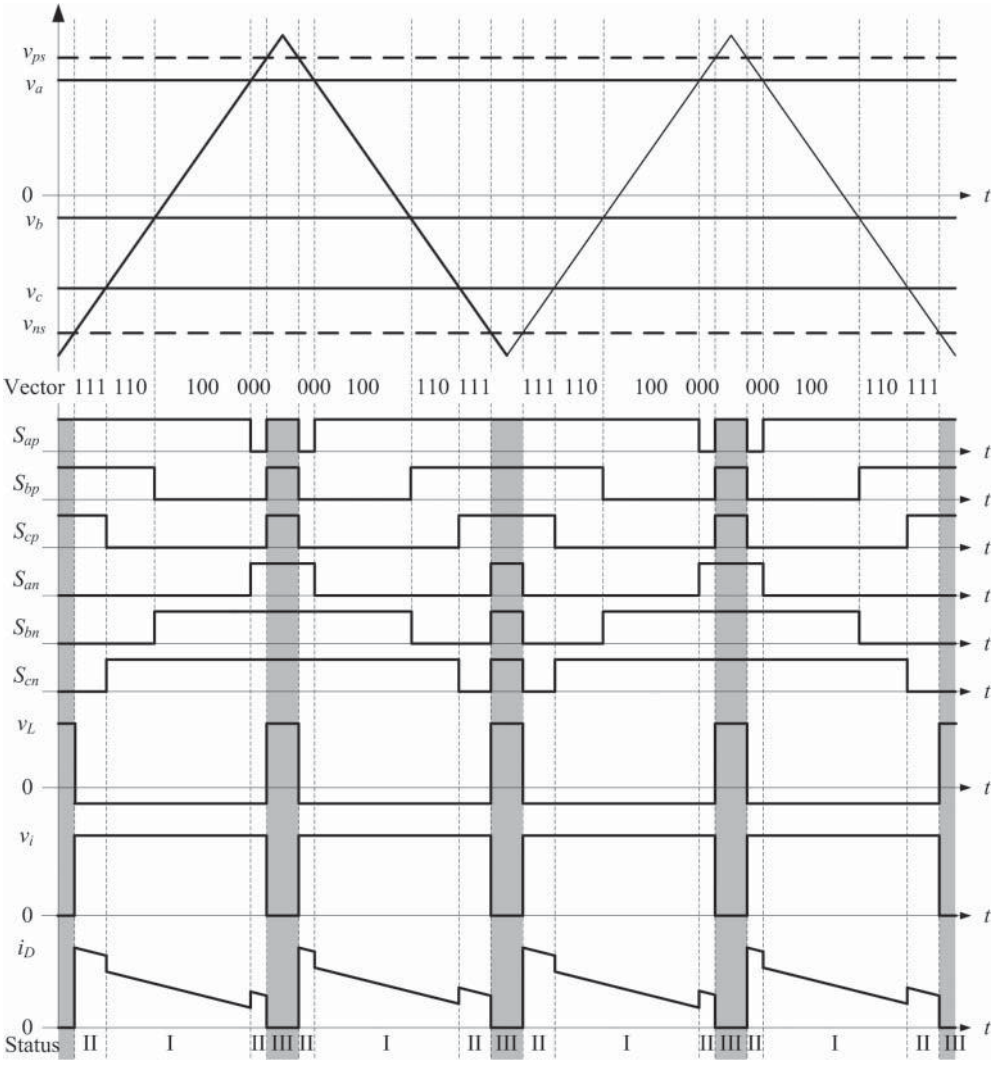


Figure 5.4 Theoretical waveforms of the Z-source inverter in normal operating mode

where $B = \frac{T}{T_1 - T_0} = \frac{1}{1-2D} \geq 1$ is the boost factor resulting from the shoot-through zero state. On the other hand, the output peak phase voltage of the inverter can be expressed as

$$V_{o\max} = M\frac{V_{i\max}}{2} \tag{5.6}$$

where M is the modulation index of inverter, and $M \leq 1$ is normally used in the SPWM (sine pulse-width modulation) and $M \leq 2/3$ in the SVPWM (space vector pulse-width modulation). Substituting Equation 5.5 into Equation 5.6, the output peak

phase voltage can be further expressed by

$$V_{o\max} = \frac{MB}{2} V_{DC} \tag{5.7}$$

Because $MB = (0 \sim \infty)$, Equation 5.7 shows that the output voltage of the Z-source inverter can be step-up or step-down by choosing an appropriate buck-boost factor *MB*.

5.2.2 Sneak Circuits of Z-Source Inverter

Due to the Z-source impedance, the three-phase inverter bridge can operate in active state, traditional zero state, or shoot-through zero state. Considering that diode *D* has two operating states, which are on-state and off-state, the Z-source inverter should have six operating modes according to the combination of two diode states and three inverter states. Except for the three normal operating statuses shown in Figure 5.3, the other three sneak circuit statuses are illustrated in Figure 5.5 respectively.

When the Z-source inverter operates in the sneak circuit status I′, according to Figure 5.5a, $i_D = 0$, we have

$$\begin{cases} v_i = V_C - v_L \\ i_L = I_i/2 \end{cases} \tag{5.8}$$

Since I_i is almost constant, the inductor voltage v_L of L_1 and L_2 is near zero and can be negligible [2], then $v_i = V_C - v_L \approx V_C$. Accordingly, the input dc voltage v_i changes to *Vc* from an original value $2V_C - V_{DC}$, which will make a sudden change and affect the output ac voltage of the inverter.

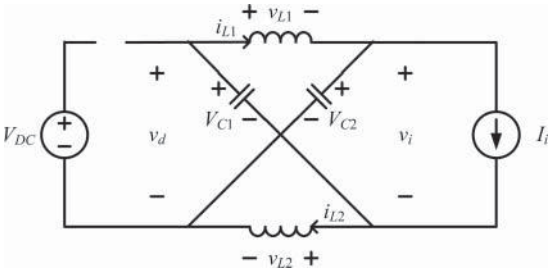
When the Z-source inverter operates in the sneak circuit status II′ shown in Figure 5.5b, $i_D = 0$, $i_L = 0$, and the inverter bridge is in open circuit, then $v_L = 0$ and $v_i = V_C - v_L = V_C$. Since the output voltage of the inverter bridge is a zero vector, the change of input dc-link voltage v_i will not affect the output ac voltage.

When the Z-source inverter operates in the sneak circuit status III′ shown in Figure 5.5c, it must satisfy the following voltage relationship:

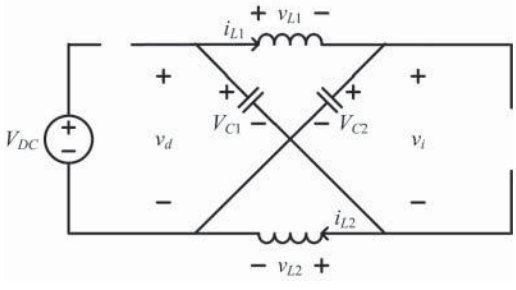
$$\begin{cases} v_L = V_C \\ v_d = V_{DC} = 2V_C \end{cases} \tag{5.9}$$

However, the capacitor voltage V_C satisfies $2V_C > V_{DC}$ in the normal operating mode to ensure a positive dc-link voltage of the inverter bridge (i.e., $v_i > 0$). As the capacitor voltages cannot be changed suddenly, Equation 5.9 is not available, which means that status III′ will not occur.

According to the above analysis, when sneak circuit status I′ occurs, the typical waveforms of the Z-source inverter are as shown in Figure 5.6.



(a)



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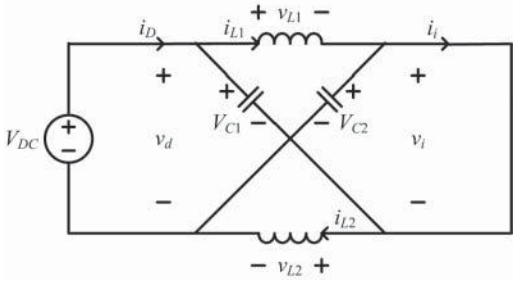


(c)

Figure 5.5 Equivalent circuits of the Z-source inverter in sneak circuit mode: (a) status I′ – inverter's active state and diode's off-state; (b) status II′ – inverter's traditional zero state and diode's off-state; and (c) status III′ – inverter's shoot-through zero state and diode's on-state

The diode current in normal status I can be expressed by $i_D = 2i_L - I_i$, if the inductor current satisfies $i_L \geq \frac{1}{2}I_i$, so $i_D \geq 0$ and the sneak cisrcuit status I′ will not occur.

As the average inductor current is equal to the average input current, according to the energy balance principle, the average value of inductor current I_L can be expressed as

$$I_L = \frac{P}{V_{DC}} = \frac{3V_{o\max}I_{o\max}\cos\phi}{2V_{DC}} \tag{5.10}$$

where $\cos\phi$ is the load power factor and $V_{o\max}$ and $I_{o\max}$ are the peak value of output phase voltage and output phase current, respectively.

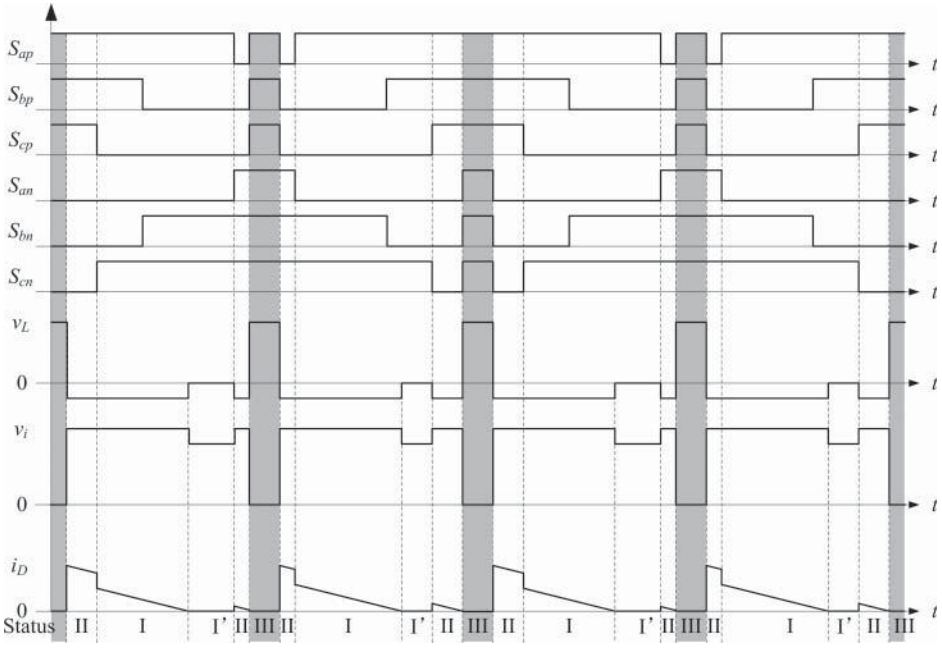


Figure 5.6 Typical waveforms of the Z-source inverter when sneak circuit status occurs

In the normal operating mode, when the Z-source inverter is operating in shoot-through state (operation status III), we have $v_L = V_C$ and the inductor current i_L will increase linearly. According to Figure 5.4, the peak-to-peak value of the inductor current ΔI_L is defined by

$$\Delta I_L = \frac{V_C D}{2Lf_s} \tag{5.11}$$

where f_s is the switching frequency of the inverter. Then the minimum value of inductor current $I_{L\min}$ equates to

$$I_{L\min} = I_L - \frac{1}{2}\Delta I_L \tag{5.12}$$

It is known that the maximum value of the input current $I_{i\max}$ of the inverter bridge is equal to the peak value of the output phase current $I_{o\max}$, thus the normal operating condition of the Z-source inverter can be rewritten as

$$I_{L\min} = I_L - \frac{1}{2}\Delta I_L \geq \frac{1}{2}I_{o\max} \tag{5.13}$$

Substituting Equations 5.4, 5.7, 5.10, and 5.11 into Equation 5.13, we obtain

$$Lf_sM\left(\frac{3}{2}MB\cos\phi - 1\right) \geq D(1-D)|Z| \text{ and } \frac{3}{2}MB\cos\phi - 1 > 0 \tag{5.14}$$

where the magnitude of load impedance Z is $|Z| = |R + j\omega L| = \frac{V_{o\max}}{I_{o\max}}$.

Based on Equation 5.14, if the parameters or operating conditions of a Z-source inverter (i.e., L, Z, M, B, D, f_s, etc.) are selected inappropriately, sneak circuit phenomenon will occur when Equation 5.14 is not established. The diode current will be discontinuous during the period of active states and the input dc voltage of the inverter bridge will drop, which seriously affects the quality of the output ac voltage.

5.2.3 Simulation Verification of Z-Source Inverter

In order to verify the relationship between load impedance and sneak circuit phenomenon in the Z-source inverter, a simulation circuit of the Z-source inverter based on Figure 5.2 was built in PSIM®. The simulation parameters of the impedance network are $C_1 = C_2 = 100$ μF and $L_1 = L_2 = 50$ μH, the modulation factor is $M = 0.9$, the shoot-through duty cycle is $D = 0.15$, the switching frequency is $f_s = 10$ kHz, the output frequency is $f = 50$ Hz, the load power factor is $\cos\phi \approx 1$, and the input voltage is $V_{DC} = 100$ V. It can be calculated from Equation 5.14 that the Z-source inverter will operate in normal situations when the load impedance satisfies $|Z| \leq 3.27\ \Omega$.

By setting the load impedance of each phase to $Z = 3 + j0.314\ \Omega$ (i.e., $|Z| = 3.016\ \Omega$ and $\cos\phi = 0.995$), the simulation waveforms of the input voltage of the inverter bridge v_i, the inductor voltage v_L and the diode current i_D are as shown in Figure 5.7, which are entirely consistent with the normal situation. However, by increasing the load impedance to $Z = 10 + j0.314\ \Omega$ (i.e., $|Z| = 10.005\ \Omega$ and $\cos\phi = 0.999$), with the simulation waveforms of v_i, v_L, and i_D shown in Figure 5.8, it is found that there is a voltage drop in the input dc voltage of the inverter bridge v_i and the peak value of v_i becomes higher than that under normal operating conditions, and the sneak operating status I′ appears.

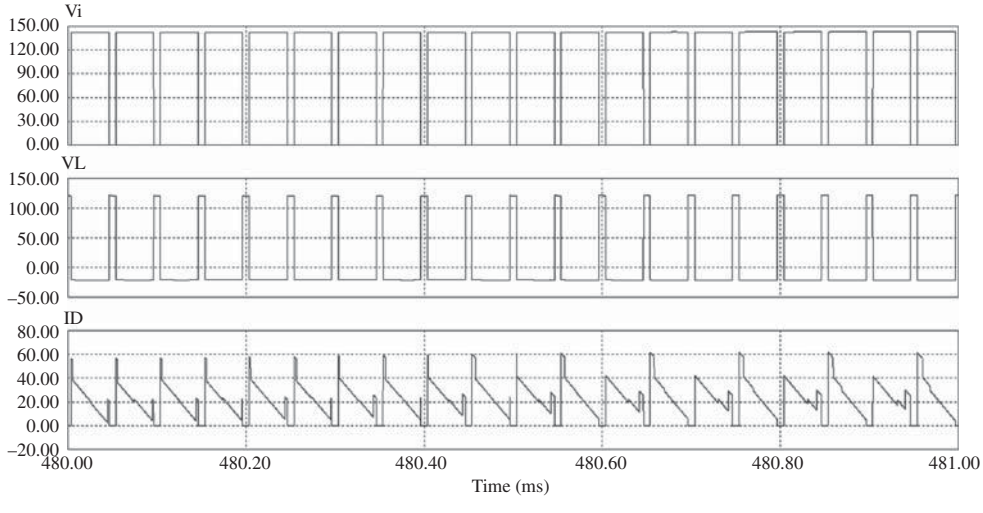


Figure 5.7 Simulation waveforms of Z-source inverter operating when $Z = 3 + j0.314\ \Omega$

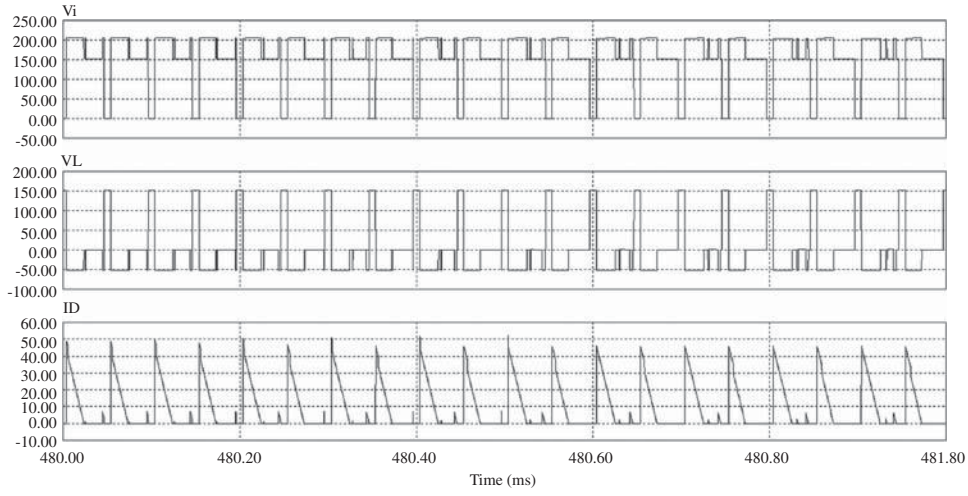


Figure 5.8 Simulation waveforms of Z-source inverter when $Z = 10 + j0.314\ \Omega$

In addition, reference [2] describes some new operating situations in the Z-source inverter under small inductance or low load power factor, which is the same as the sneak circuit phenomenon in Section 5.2.2. Therefore, it can be concluded that sneak circuits really exist in the three-phase Z-source inverter.

5.3 Sneak Circuits of Synchronous DC-DC Converters

The trend in power supplies for CPUs, chipsets, and other portable devices is to reduce the output voltage levels from 5 to 3.3 V, 1.7 V, and lower levels. As the output voltage is reduced, the conduction loss of rectifier diode becomes the main source of power loss in low-voltage power supplies. Unfortunately, what can be done to reduce the forward voltage drop of diodes is limited by the junction contact potential. Schottky diodes having reduced junction potential can be employed; nonetheless, low-voltage power supplies containing diodes still have low efficiency, especially in the case of extra-low output voltage.

Since the channel in the Power MOSFET has the ability to conduct the reverse current, it is possible to replace a diode with a Power MOSFET in some situations, by controlling the Power MOSFET in the on-state when the diode would normally conduct and in the off-state when the rectifier diode would be reverse-biased. The advantage of using a Power MOSFET instead of a rectifier diode is the extra low conduction loss of a Power MOSFET, $I_{rms}^2 R_{on}$, which is defined by its on-resistance R_{on} and the operating RMS current I_{rms}. As the on-resistance can be decreased to a very low value by the design, the conduction loss of the Power MOSFET can be reduced to as low as desired, then the efficiency of the power supply can be increased. Therefore, the solution that replaces the rectifier diodes with Power MOSFETs operated as synchronous rectifiers are widely used in low-voltage power supplies [3].

In synchronous rectifiers, the Power MOSFET will have the same external characteristics of rectifier diode by synchronous control, but the Power MOSFET contains a parasitic capacitor and a body diode, thus there will be some other current paths in the synchronous rectifier, which are different from those in the original diode rectifier, and may bring some new properties to the converter. As the synchronous Buck converter is popular for low-voltage power conversion, because of its high efficiency [4, 5], the following section will use it as an example to illustrate how to analyze the sneak circuits and their occurrence in synchronous converters.

5.3.1 Equivalent Circuit of Synchronous Buck Converter

The synchronous Buck converter can be obtained by replacing the diode in the Buck converter (Figure 3.1) with a Power MOSFET. As shown in Figure 5.9, S_1 is the main switch and S_2 is the synchronous switch, which is controlled by the complement driving signal of S_1.

Normally, a composite switch, as shown in Figure 5.10, is used to represent the structure of a Power MOSFET, when considering the drain-to-source capacitance and body diode of the Power MOSFET. Furthermore, a faster anti-parallel diode or additional capacitor is usually added to improve the performance of the Power MOSFET in some applications. Therefore, the composite switch can be modeled by an ideal bi-directional switch, an anti-parallel ideal diode D_s and a parallel capacitor C_s with a significant drain-to-source capacitance. The equivalent circuit of the synchronous Buck converter with a composite switch model is illustrated in Figure 5.11.

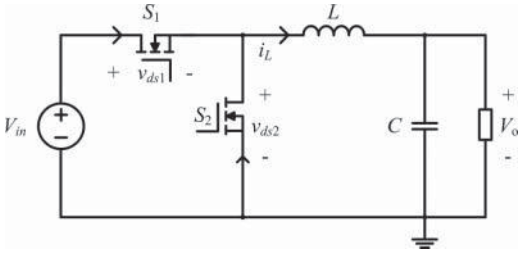


Figure 5.9 Schematic diagram of a synchronous Buck converter

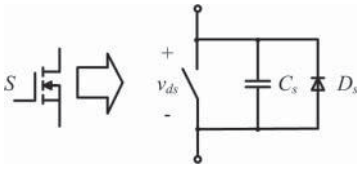


Figure 5.10 Composite switch equivalent to a Power MOSFET

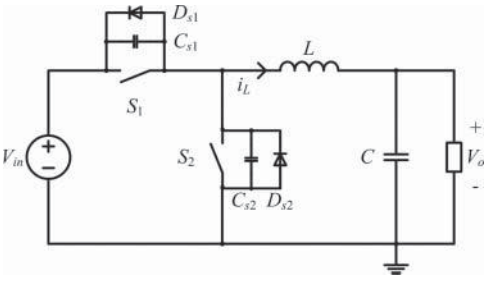


Figure 5.11 Schematic diagram of a synchronous Buck converter with composite switch model

5.3.2 Normal Operating Principle of Synchronous Buck Converter

In general, the conduction of two switches in a synchronous Buck converter is complementary, but certain dead time should be set between two driving signals to prevent simultaneous conduction of the switches. When the inductor current is continuous and positive, according to the equivalent circuit of the synchronous Buck converter in Figure 5.11, its operating process can be described as follows.

Stage I (t_0, t_1)

Main switch S_1 conducts, inductor L subjects to the voltage which is the difference between the input voltage V_{in} and output voltage V_o, then the inductor current i_L increases. At the moment of t_1, S_1 is switched off and stage I is over. The equivalent circuit of this stage is shown in Figure 5.12a.

Stage II (t_1, t_2)

As the inductor current i_L is positive after switching off S_1, it can discharge the parallel parasitic capacitor C_{s2} of the synchronous switch S_2 and charge the parallel parasitic capacitor C_{s1} of the main switch S_1 at the same time. The duration of this stage is extremely short, therefore i_L can be considered as constant and the drain-to-source voltage of S_2 (v_{ds2}) can be regarded as reducing linearly. When v_{ds2} reduces to zero, stage II is over and its equivalent circuit is shown in Figure 5.12b.

Stage III (t_2, t_3)

The anti-parallel diode D_{s2} will be on after v_{ds2} is equal to zero, thus the terminal voltage of S_2 will be clamped to zero, thus providing the zero-voltage turn-on conduction for S_2. The equivalent circuit of stage III is shown in Figure 5.12c.

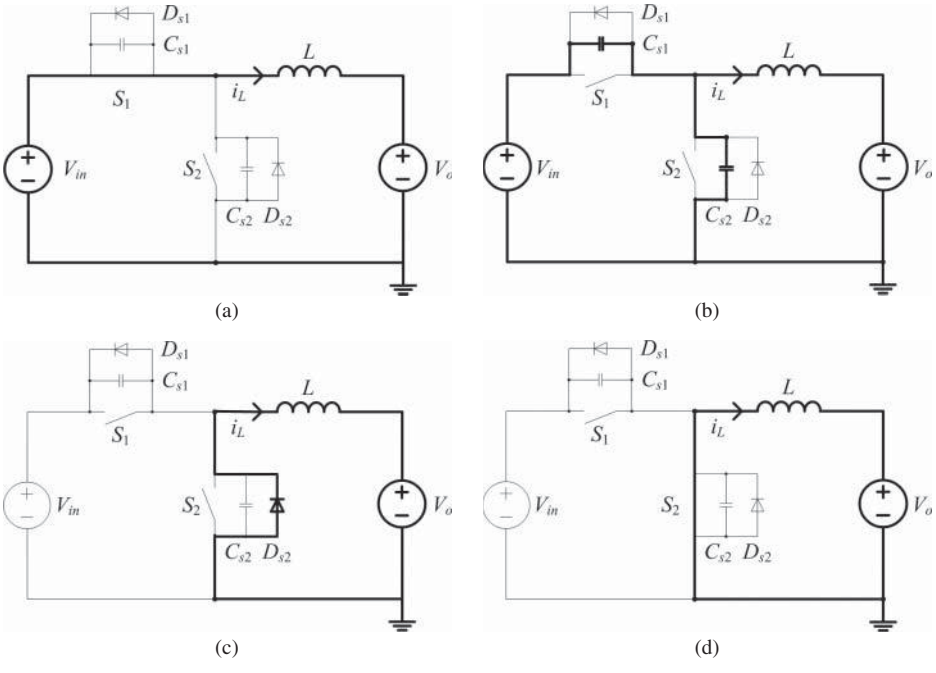


Figure 5.12 Equivalent circuits of a synchronous Buck converter in normal operating mode: (a) stage I; (b) stage II; (c) stage III or V; and (d) stage IV

Stage IV (t_3, t_4)

When S_2 conducts at the moment of t_3, then i_L flows through S_2 continuously and reduces linearly due to the inductor L suffering the reverse output voltage $-V_o$. This stage is ended when S_2 is switched off and the equivalent circuit is shown in Figure 5.12d.

Stage V (t_4, t_5)

The anti-parallel diode D_{s2} of S_2 is freewheeling due to i_L being positive. D_{s2} will not shut down until S_1 is switched on. The equivalent circuit of stage V is the same as that of stage III, that is, Figure 5.12c.

The synchronous Buck converter enters another switching cycle after S_1 is turned on. From the above analysis, typical waveforms of a synchronous Buck converter in normal operating mode are shown in Figure 5.13.

It is obvious that the synchronous switch S_2 can achieve ZVS, since its anti-parallel diode D_{s2} conducts and clamps its terminal voltage to zero before S_2 is switched on. However, the main switch S_1 is still operating in hard-switching state, because the inductor current i_L is still positive and cannot discharge the voltage of C_{s1} to zero after S_2 is turned off.

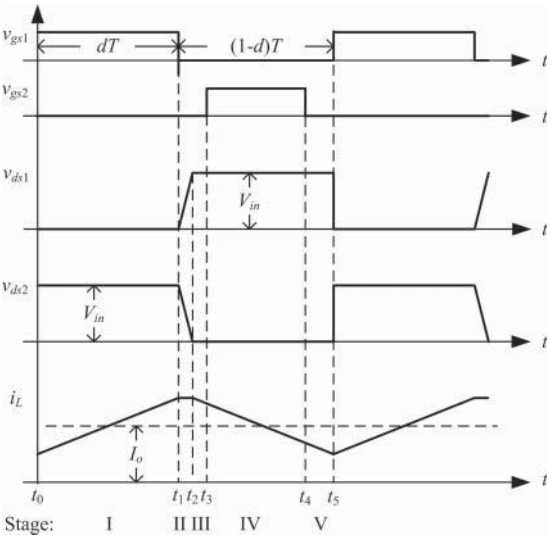


Figure 5.13 Typical waveforms of the synchronous Buck converter in normal operating mode

5.3.3 Sneak Circuits of Synchronous Buck Converter

As Power MOSFET can flow through a bidirectional current, the inductor current i_L will drop to zero and become negative during the on-state of S_2, if the inductor of the synchronous Buck converter is designed relatively small or some operating conditions have changed, thus D_{s1} will conduct to create the zero-voltage turn-on condition of the main switch S_1 [6]. Since the situation that both the main switch S_1 and the synchronous switch S_2 can achieve ZVS only happens in a particular operating condition, it can be regarded as the sneak circuit phenomenon of the synchronous Buck converter according to the definition of sneak circuit. In order to distinguish the case that only S_2 can realize ZVS from that with both switches, the latter is named as the ZVS synchronous Buck converter.

The typical waveforms of the ZVS synchronous Buck converter are illustrated in Figure 5.14, which show that the operating process can be divided into six stages. Among them, stages I to IV are the same as those of the synchronous Buck converter, but stage V′ is different and a new stage VI appears.

Stage V′ (t_4, t_5)

The synchronous switch S_2 is switched off at the moment t_4. As the inductor current i_L is negative, it will charge the parallel parasitic capacitor C_{s2} of S_2 and discharge the parallel parasitic capacitor C_{s1} of S_1, then the drain-to-source voltage of S_1 (v_{ds1}) decreases. When v_{ds1} drops to zero, stage V′ is ended, and its equivalent circuit is shown in Figure 5.15a.

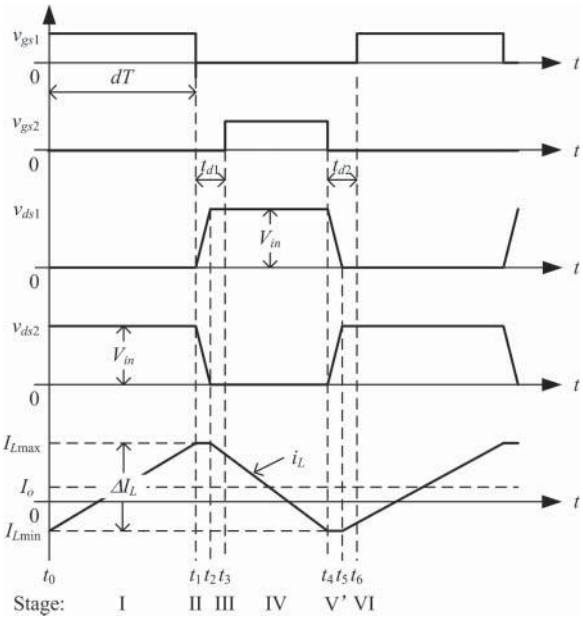
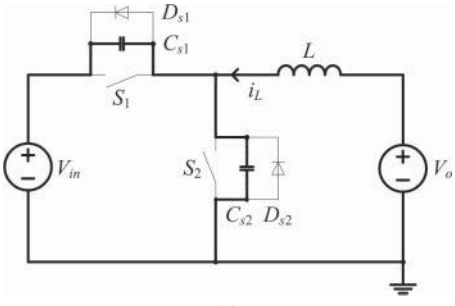
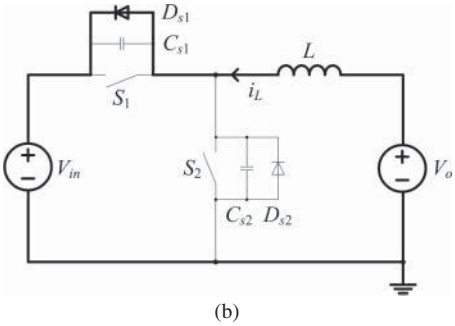


Figure 5.14 Typical waveforms of a ZVS synchronous Buck converter



(a)



(b)

Figure 5.15 Part of equivalent circuits of a ZVS synchronous Buck converter: (a) stage V′; and (b) stage IV

Stage VI (t_5, t_6)

The anti-parallel diode D_{s1} of S_1 conducts when v_{ds1} drops to zero, and the terminal voltage of S_1 is clamped to zero, thus S_1 can also be turned on under zero voltage. As the inductor voltage is positive, i_L begins to increase. This stage is over when S_1 is switched on. The equivalent circuit of stage VI is shown in Figure 5.15b, which belongs to a sneak path of the synchronous Buck converter.

Because both the main switch S_1 and synchronous switch S_2 can achieve zero-voltage turn-on in a ZVS synchronous Buck converter, their turn-on switching loss can be significantly reduced. Besides, due to the fact that anti-parallel capacitors of S_1 and S_2 can keep the voltages across the switches close to zero while the switches are turned off, that the turn-off switching loss is also very small. Thus the efficiency of the ZVS synchronous Buck converter has been further improved.

5.3.4 Sneak Circuit Condition of Synchronous Buck Converter

As the ZVS synchronous Buck converter can be considered as the sneak circuit mode of the synchronous Buck converter, the condition at which the synchronous Buck converter can achieve ZVS should be derived as well as the sneak circuit condition. First, the peak-to-peak value of the inductor current is

$$\Delta I_L = \frac{d(V_{in} - V_o)}{Lf_s} \tag{5.15}$$

where d is the duty ratio of the main switch S_1, and f_s is the switching frequency of the converter. Therefore the maximum and the minimum values of the inductor current are

$$I_{L\max} = I_o + \frac{\Delta I_L}{2} = I_o + \frac{d(V_{in} - V_o)}{2Lf_s} \tag{5.16}$$

$$I_{L\min} = I_o - \frac{\Delta I_L}{2} = I_o - \frac{d(V_{in} - V_o)}{2Lf_s} \tag{5.17}$$

where I_o is the rated output current of the converter.

From the above analysis, only when the minimum inductor current becomes negative, that is, $I_{L\min} < 0$, ZVS of the main switch S_1 in the synchronous Buck converter can be achieved, therefore, according to Equation 5.17, the converter parameters or operating conditions of the synchronous Buck converter should satisfy the following:

$$2Lf_sI_o < d(V_{in} - V_o) \tag{5.18}$$

In addition, the dead time between two switches is also a critical condition for the synchronous Buck converter to achieve ZVS, because sufficient time is required to discharge the parallel capacitor of the switch and make the anti-parallel diode conduct prior to the channel conduction. Since the dead time is relatively short, the inductor

current can be regarded as constant and the capacitor voltage is declining approximately linearly, and the dead times to ensure the ZVS conduction of both switches are

$$t_{d1} = t_3 - t_1 \geq \frac{C_{s2} V_{in}}{I_{L\max}} \quad \text{for} \quad S_2 \tag{5.19}$$

$$t_{d2} = t_6 - t_4 \geq \frac{C_{s1} V_{in}}{I_{L\min}} \quad \text{for} \quad S_1 \tag{5.20}$$

If the parameter condition for ZVS, that is Equation 5.18, has been satisfied, which means that $I_{L\min} < 0$, then the dead time condition for main switch S_1, that is, Equation 5.20, is met with at the same time. Only the dead time condition for synchronous switch S_2, that is, Equation 5.19, should be considered in the synchronous Buck converter to achieve ZVS.

5.3.5 Simulation Verification of Synchronous Buck Converter

According to Figure 5.11, a synchronous Buck converter with composite switch model is built in PSIM® to illustrate the above theoretical analysis. The simulation parameters are input voltage $V_{in} = 48$ V, output voltage $V_o = 19$ V, output current $I_o = 0 \sim 5$ A, switching frequency $f_s = 200$ kHz, inductance $L = 4.5$ μH, and parasitic capacitance $C_{s1} = C_{s2} = 920$ pF when IRFZ44 is selected as the switches. If the dead time between two switches is set to $t_{d1} = t_{d2} = 160$ ns, it is obvious that Equations 5.18–5.20 are satisfied, which means that the converter will operate as the ZVS synchronous Buck converter or the sneak circuit phenomenon will appear.

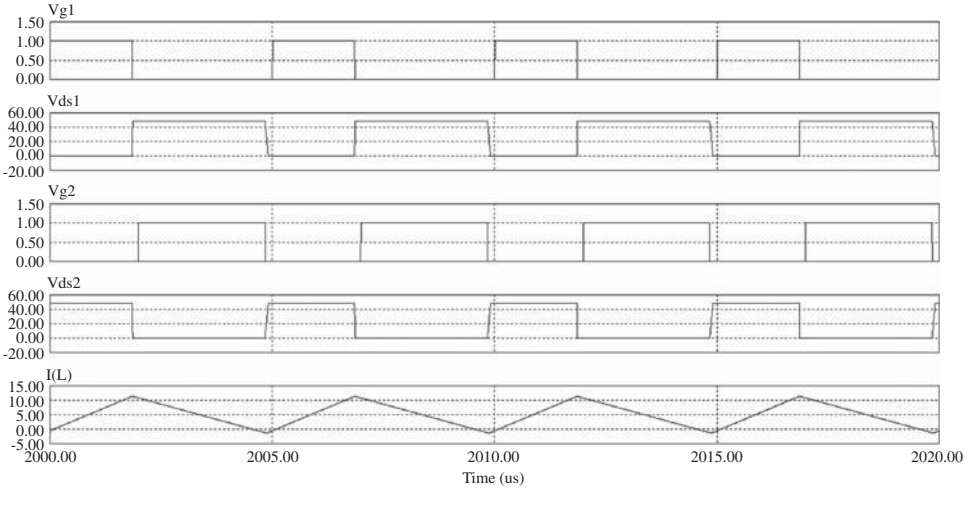


Figure 5.16 Simulation waveforms of a ZVS synchronous Buck converter when $I_o = 5$ A

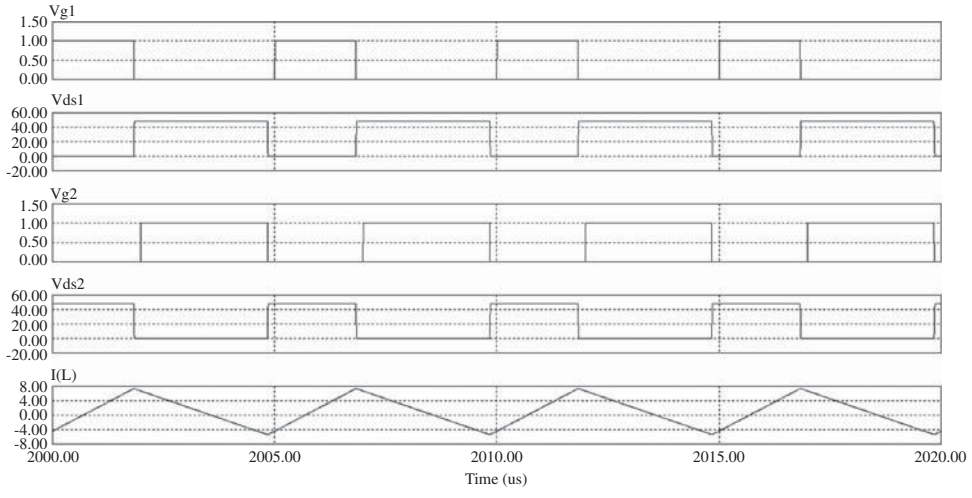


Figure 5.17 Simulation waveforms of a ZVS synchronous Buck converter when $I_o = 1$ A

Figure 5.16 shows the simulation waveforms at full load ($I_o = 5$ A), in which the minimum value of inductor current i_L is less than zero. It is obvious that the drain to source voltage of the switch decreases to zero prior to the driving signal reaching a high level, thus both S_1 and S_2 can achieve ZVS. The simulation waveforms at light load ($I_o = 1$ A) are illustrated in Figure 5.17, from which it is clear that both S_1 and S_2 could operate under ZVS also. Comparing Figure 5.17 with Figure 5.16, the reverse part of the inductor current was enlarged, thus the switches S_1 and S_2 can much easier achieve ZVS under light load than under full load.

Even though the main switch of a synchronous Buck converter can achieve ZVS by making use of the reverse inductor current, other types of synchronous DC-DC converters, such as the synchronous Boost converter, the synchronous Buck-boost converter, the synchronous Flyback converter, and so on, can achieve ZVS by employing the same principles, thus the advantages of the synchronous DC/DC converter could be further promoted. So it is a significant reward to achieve ZVS by using the sneak circuit paths that exist in the synchronous DC-DC converter.

5.4 Summary

This chapter further illustrates the sneak circuits, which are accidentally introduced by the designers in the design process, exist in some novel power electronic. However, the unpredictable affects that are caused by the sneak circuits are not entirely negative, for example, the synchronous DC-DC converters can achieve ZVS by making use of the reverse inductor current path. Consequently, analyzing the sneak circuit and its

efficacy is needed in the converter design process, in order to develop the merits and avoid the drawbacks of sneak circuits.

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Part Two

Sneak Circuit Analysis Methods

6

Sneak Circuit Path Analysis Method for Power Electronic Converters

6.1 Introduction

Sneak circuit phenomena of a variety of power electronic converters were introduced in Chapters 2–5, but most sneak circuit phenomena have been found by experiments or experience. As the power electronic converter contains some switching components, which are switched between on-state and off-state at a high frequency according to certain control rules, the power electronic system is different from conventional electric or electrical systems, and the existing SCA methods cannot be applied to power electronic converters directly. Therefore, a sneak circuit path analysis method, which is suitable for power electronic converters, is required. In this chapter, the topology of a power electronic converter is transferred to a graph based on graph theory, then by using concepts such as the adjacency matrix, connection matrix, and switching Boolean matrix, all of the current paths including the sneak circuit paths existing in the power electronic converter can be found.

6.2 Basic Concepts

In this section, some basic concepts on graph theory, which are useful in sneak circuit path analysis of the power electronic converter, will be briefly introduced based on references [1, 2].

6.2.1 Directed Graph

Abstract graph $G = (V, E)$, or graph G for short, is composed of sets V and E. The elements of the finite set V are the vertices (or nodes, or points) of graph G, and are

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usually expressed by the numbers $1, 2, \ldots, n$. The elements of the finite set E are the edges (or lines) of graph G, and are expressed by the vertex pairs, such as (i, j) or (j, i), where $i, j \in V$, or the edges known as $e_1, e_2, \ldots, e_m$.

The vertex connected to the edge is also known as the endpoint of the edge, edge e and vertex v are associated if vertex v is the endpoint of edge e. Vertices i and j are adjacent if the edge $e_k = (i, j)$ that connects vertices i and j belongs to set E, then these two vertices can be connected by a continuous curve or straight line, and edges e_1 and e_2 are adjacent if e_1 and e_2 have the common endpoint. Obviously, association refers to the relationships among the different elements, such as vertex v and edge e, while adjacency refers to the relationship among the same elements, for example, vertices i and j.

The edge where two endpoints overlap is called the self-loop. If two or more edges are associated with the same endpoint, then these edges are called parallel edges. The graph without a self-loop or parallel edge is called a simple graph. Some common definitions in graphs are listed as follows:

Definition 6.1 Directed graph [1] If the vertex pair (i, j) is ordered, which means that edges (i, j) and (j, i) are the different elements in edge set E, then the corresponding graph is a directed graph (or digraph), otherwise it is an undirected graph. In the directed graph, the direction of the edge is represented by an arrow, for the edge (i, j), vertex i is the starting point, vertex j is the terminal point, and the arrow is pointing from i to j.

Definition 6.2 Edge sequence [1] The finite sequence $\{(i_1, i_2), (i_2, i_3), \ldots, (i_{k-1}, i_k)\}$ in a graph is known as an edge sequence with length $k - 1$, where $k \geq 2$.

Definition 6.3 Path [1] If the vertices $i_1, i_2, \ldots, i_k$ in the edge sequence $\{(i_1, i_2), (i_2, i_3), \ldots, (i_{k-1}, i_k)\}$ are all different, then this edge sequence is called a path with length $k - 1$. The isolated vertex can be considered as a path whose length equals zero.

Definition 6.4 Loop [1] In an edge sequence $\{(i_1, i_2), (i_2, i_3), \ldots, (i_{k-1}, i_k)\}$, if $i_1 = i_k$, and the other vertices $i_1, i_2, \ldots, i_{k-1}$ are all different; this sequence is called a loop with length $k - 1$.

6.2.2 Adjacency Matrix

Definition 6.5 Adjacency matrix If a directed graph, $G = (V, E)$ has n vertices and no parallel edges, and the matrix:

$$\mathbf{A} = [a_{ij}]_{n \times n} \tag{6.1}$$

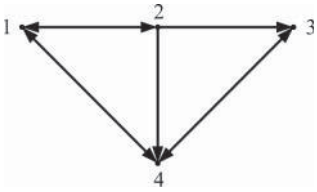


Figure 6.1 A directed graph with four vertices

where

$$a_{ij} = \begin{cases} 1 & \text{if the directed edge } (i,j) \in E \\ 0 & \text{if there is no directed edge between vertices } i \text{ and } j \end{cases} \tag{6.2}$$

and is named as the adjacent matrix of directed graph G.

Assuming that $\mathbf{A}^{(k)}$ is the k-th power of adjacency matrix $\mathbf{A}$, where k is a positive integer, then the element $a_{ij}{}^{(k)}$ of $\mathbf{A}^{(k)}$ is the number of the paths with length k between vertices i and j.

Figure 6.1 is a directed graph with four vertices. According to the Definition 6.5, adjacency matrix $\mathbf{A}$ of Figure 6.1 is expressed by

$$\mathbf{A} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \end{bmatrix} \tag{6.3}$$

then

$$\mathbf{A}^2 = \mathbf{A} \cdot \mathbf{A} = \begin{bmatrix} 2 & 0 & 2 & 1 \\ 1 & 1 & 1 & 2 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 2 \end{bmatrix} = [a_{ij}^{(2)}] \tag{6.4}$$

where

$$a_{ij}^{(2)} = \sum_{k=1,k\neq i,j}^{4} a_{ik} a_{kj} \tag{6.5}$$

It is obvious that $a_{ik} \cdot a_{kj} \neq 0$ if and only if $a_{ik} = a_{kj} = 1$, in other words, there are edges from i to k and from k to j, so the value of $a_{ij}^{(2)}$ is the number of paths with length 2, which start from vertex i and arrive at vertex j. For example, $a_{13}^{(2)} = 2$ indicates that there are two paths with length 2 from vertex 1 to vertex 3. From Figure 6.1, it can be seen that these two paths are $1 \rightarrow 2 \rightarrow 3$ and $1 \rightarrow 4 \rightarrow 3$.

6.2.3 Connection Matrix

Definition 6.6 Connection matrix If a directed graph $G = (V, E)$ has n vertices, then the matrix:

$$\mathbf{C} = [c_{ij}]_{n\times n} \tag{6.6}$$

where

$$c_{ij} = \begin{cases} 1 & i = j \\ 0 & i \neq j \text{ and there is no edge from } i \text{ to } j \\ \sum_{x=1}^{m} e_x & i \neq j \text{ and there are } m \text{ edge from } i \text{ to } j \end{cases} \tag{6.7}$$

and is named as the connection matrix of directed graph G.

The element c_{ij} in connection matrix $\mathbf{C}$ represents the directed paths from vertex i to j, namely without passing through any other vertex. Assuming that matrix $\mathbf{C}^{(k)}$ is the k-th power of connection matrix $\mathbf{C}$, where k is a positive integer, the element in $\mathbf{C}^2 = \mathbf{C} \times \mathbf{C}$ is defined by $c_{ij}^{(2)} = \sum_{k=1,k\neq i,j}^{n} c_{ik}c_{kj}$. If $c_{ik}c_{kj} \neq 0$, which indicates there are paths between vertices i and k, k and j, then a path is formed between vertices i and j via vertex k. So the matrix $\mathbf{C}^2$ contains the path information of any vertex pair through one vertex in graph G. Similarly, the matrix $\mathbf{C}^3 = \mathbf{C} \times \mathbf{C} \times \mathbf{C} = \mathbf{C}^2 \times \mathbf{C}$ contains the path information of any vertex pair through two or less than two vertices in graph G, the matrix $\mathbf{C}^4 = \mathbf{C} \times \mathbf{C} \times \mathbf{C} \times \mathbf{C} = \mathbf{C}^3 \times \mathbf{C}$ contains the path information of any vertex pair through three or less than three vertices in graph G, and the matrix $\mathbf{C}^{(n-1)} = \mathbf{C} \times \mathbf{C} \times \mathbf{C} \times \cdots \times \mathbf{C} = \mathbf{C}^{(n-2)} \times \mathbf{C}$ contains the path information of any vertex pair through $n-2$ or less than $n-2$ vertices in graph G. Therefore, all the paths in graph G can be obtained by calculating the matrix $\mathbf{C}^{(n-1)}$.

The undirected graph shown in Figure 6.2 is an example showing how to use the connection matrix $\mathbf{C}$ to obtain all paths in the graph. As there are four vertices in Figure 6.2, matrix $\mathbf{C}^3$ needs to be calculated.

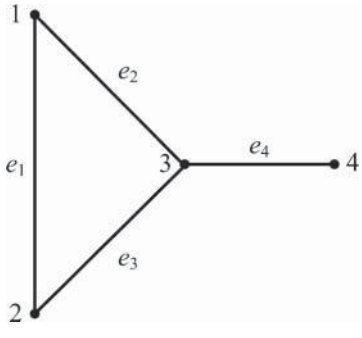


Figure 6.2 An undirected graph with four vertices

According to Definition 6.6, the connection matrix $\mathbf{C}$ corresponding to Figure 6.2 is

$$\mathbf{C} = \begin{bmatrix} 1 & e_1 & e_2 & 0 \\ e_1 & 1 & e_3 & 0 \\ e_2 & e_3 & 1 & e_4 \\ 0 & 0 & e_4 & 1 \end{bmatrix} \tag{6.8}$$

Then

$$\begin{aligned} \mathbf{C}^2 &= \begin{bmatrix} 1 & e_1 & e_2 & 0 \\ e_1 & 1 & e_3 & 0 \\ e_2 & e_3 & 1 & e_4 \\ 0 & 0 & e_4 & 1 \end{bmatrix} \begin{bmatrix} 1 & e_1 & e_2 & 0 \\ e_1 & 1 & e_3 & 0 \\ e_2 & e_3 & 1 & e_4 \\ 0 & 0 & e_4 & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1 + e_1e_1 + e_2e_2 & e_1 + e_1 + e_2e_3 & e_2 + e_2 + e_1e_3 & e_2e_4 \\ e_1 + e_1 + e_2e_3 & 1 + e_1e_1 + e_3e_3 & e_3 + e_3 + e_1e_2 & e_3e_4 \\ e_2 + e_2 + e_1e_3 & e_3 + e_3 + e_1e_2 & 1 + e_2e_2 + e_3e_3 + e_4e_4 & e_4 + e_4 \\ e_2e_4 & e_3e_4 & e_4 + e_4 & 1 + e_4e_4 \end{bmatrix} \end{aligned} \tag{6.9}$$

According to the definition of element c_{ij} in the connection matrix, the operation rules of edge can be obtained as follows:

$$\begin{aligned} 1 + e_i &= 1 \\ e_i + e_i &= e_i \\ e_ie_i &= e_i \\ e_i + e_ie_j &= e_i(1 + e_j) = e_i \end{aligned} \tag{6.10}$$

Then, Equation 6.9 can be simplified to

$$\mathbf{C}^2 = \begin{bmatrix} 1 & e_1 + e_2e_3 & e_2 + e_1e_3 & e_2e_4 \\ e_1 + e_2e_3 & 1 & e_3 + e_1e_2 & e_3e_4 \\ e_2 + e_1e_3 & e_3 + e_1e_2 & 1 & e_4 \\ e_2e_4 & e_3e_4 & e_4 & 1 \end{bmatrix} \tag{6.11}$$

Similarly,

$$\mathbf{C}^3 = \begin{bmatrix} 1 & e_1 + e_2e_3 & e_2 + e_1e_3 & e_2e_4 + e_1e_3e_4 \\ e_1 + e_2e_3 & 1 & e_3 + e_1e_2 & e_3e_4 + e_1e_2e_4 \\ e_2 + e_1e_3 & e_3 + e_1e_2 & 1 & e_4 \\ e_2e_4 + e_1e_3e_4 & e_3e_4 + e_1e_2e_4 & e_4 & 1 \end{bmatrix} \tag{6.12}$$

From Figure 6.2, there are $\frac{n(n-1)}{2} = 6$ pairs of vertices in the graph, and the paths between vertex pair (1, 2) are e_1, e_2e_3, those between vertex pair (1, 3) are e_2, e_1e_3, those between vertex pair (1, 4) are e_2e_4, $e_1e_3e_4$, those between vertex pair (2, 3) are e_3, e_1e_2, those between vertex pair (2, 4) are e_3e_4, $e_1e_2e_4$, and the path between vertex pair (3, 4) is e_4. It is found that the elements in $\mathbf{C}^3$, that is Equation 6.12, which represents the paths of any vertex pair through two or less than two vertices, is entirely consistent with the information in Figure 6.2.

6.2.4 Switching Function and Transfer Matrix

Definition 6.7 Switching function For graph G, assume that the number of total paths between vertices i and j is L, and each path is represented by $P_{ij}^{(k)}$, where $k = 1, 2, \ldots, L$. If $\pi_{ij}^{(k)}$ is defined as the continuous product of all edges in path $P_{ij}^{(k)}$, then

$$f_{ij} = \begin{cases} \sum_{k=1}^{L} \pi_{ij}^{(k)} & i \neq j \\ 1 & i = j \end{cases} \tag{6.13}$$

which is called the switching function between vertices i and j of graph G.

Definition 6.8 Transfer matrix For a graph G with n vertices, the matrix

$$\mathbf{F} = (f_{ij})_{n\times n} \tag{6.14}$$

is called the transfer matrix of the graph G. From these definitions, it is known that the switching function represents paths between two specified vertices, and the transfer matrix represents the paths between any two vertices, therefore all paths existing in the graph can be obtained by the transfer matrix.

However, when the scale of a graph is relatively large, there are so many vertices in the graph that it is difficult and complicated to find all the paths manually. According to the definition of the connection matrix $\mathbf{C}$, the switching function and transfer matrix can be obtained by the following theorems:

Theorem 6.1 For a graph G with n vertices, assuming that its connection matrix is $\mathbf{C}$, then its transfer matrix $\mathbf{F}$ can be expressed by

$$\mathbf{F} = \mathbf{C}^{(n-1)} \tag{6.15}$$

Theorem 6.2 Assuming that Δ_{ij} is the cofactor of element (i, j) in connection matrix $\mathbf{C}$, then the switching function f_{ij} between vertices i and j can be expressed by

$$f_{ij} = |\det \Delta_{ij}| \tag{6.16}$$

It is known that a loop is a special path, but according to the definition of a switching function, only the paths between two different vertices can be calculated by Theorem 6.2. In Reference [3], it is proven that the loops in a graph can be obtained by the determinant of connection matrix.

Theorem 6.3 Assuming that the connection matrix of graph G is $\mathbf{C}$, then the absolute value of the determinant of connection matrix $\mathbf{C}$ is defined as the generalized switching function:

$$f_{loop} = |\det \mathbf{C}| \tag{6.17}$$

Taking the graph with four vertices in Figure 6.2 as an example that explains Theorems 6.1–6.3, based on Theorem 6.1 and Equation 6.12, the transfer matrix of Figure 6.2 is

$$\mathbf{F} = \mathbf{C}^3 = \begin{bmatrix} 1 & e_1 + e_2e_3 & e_2 + e_1e_3 & e_2e_4 + e_1e_3e_4 \\ e_1 + e_2e_3 & 1 & e_3 + e_1e_2 & e_3e_4 + e_1e_2e_4 \\ e_2 + e_1e_3 & e_3 + e_1e_2 & 1 & e_4 \\ e_2e_4 + e_1e_3e_4 & e_3e_4 + e_1e_2e_4 & e_4 & 1 \end{bmatrix} \tag{6.18}$$

If we want to obtain the paths between vertices 1 and 4 only, there is no need to calculate the transfer matrix **F**, but only the switching function f_{14}. According to Theorem 6.2:

$$f_{14} = |\det \Delta_{14}| = \begin{vmatrix} e_1 & 1 & e_3 \\ e_2 & e_3 & 1 \\ 0 & 0 & e_4 \end{vmatrix} = e_1e_3e_4 + e_2e_4 \tag{6.19}$$

which is the same as the element c_{14} in Equation 6.18.

According to Theorem 6.3, the generalized switching function of Figure 6.2 is

$$f_{loop} = |\det \mathbf{C}| = \begin{vmatrix} 1 & e_1 & e_2 & 0 \\ e_1 & 1 & e_3 & 0 \\ e_2 & e_3 & 1 & e_4 \\ 0 & 0 & e_4 & 1 \end{vmatrix} = 1 + e_4^2 + e_3^2 + e_2^2 + e_1^2 + e_1^2e_4^2 + 2e_1e_3e_2 \tag{6.20}$$

It is obvious that the results in Equation 6.20 represent all possible loops in Figure 6.2. As, all edges in Figure 6.2 are bi-directional, the squared terms belong to a special loop that passes through the same edge. Therefore, the generalized switching function is useful in calculating the loops in the graph.

6.2.5 Switching Network and Switching Boolean Matrix

Definition 6.9 Switching network The ideal switch can be considered as a two-terminal component with "on" and "off" states. Thus, a network, which is composed of ideal switches only, is called the switching network. Assuming that the ideal switch is an edge and its terminal is a vertex, then the switching network can be regarded as an undirected graph G_N.

Definition 6.10 Switching Boolean matrix As the Boolean variable x can be used to indicate the state of the switch in the switching network, where $x = 1$ when the switch is turned on and $x = 0$ when the switch is turned off, the connection matrix of the switching network or the undirected graph G_N can be transformed into the switching Boolean matrix **B**.

Obviously, if and only if all the Boolean variables in path $P_{ij}^{(k)}$ are equal to 1, that is $\pi_{ij}^{(k)} = 1$, then path $P_{ij}^{(k)}$ is established. Thus, the switching function f_{ij} of the switching network G_N is also known as the Boolean function, and Boolean algebra should be used to process the switching function.

Boolean algebra is a mathematical system $(\beta, +, \cdot)$, which consists of a non-empty set β and two binary operators "+" (ADDITION) and "·" (MULTIPLICATION) based on β. The Boolean algorithm can be concluded as follows:

1. Operators "+" and "·" are exchangeable, that is for $a, b \in \beta$, there are $a + b = b + a$ and $a \cdot b = b \cdot a$.
2. Operators "+" and "·" satisfy the distributive law, that is for $a, b, c \in \beta$, there are $a + (b \cdot c) = (a + b) \cdot (a + c)$ and $a \cdot (b \cdot c) = a \cdot b + a \cdot c$.
3. For operators "+" and "·," if one of the operating elements is 0 or 1, then for $\alpha \in \beta$, there are $a + 0 = a$ and $a \cdot 1 = a$.
4. For each element $\alpha \in \beta$, there always exists another element $\overline{\alpha} \in \beta$, which is called the complementary element of a, and satisfies $a + \overline{a} = 1$ and $a \cdot \overline{a} = 0$.

Based on the above Boolean algorithm, the switching function of the switching network can be calculated. A switching network in Figure 6.3 is an example that explains the calculation process of the switching function. Based on Figure 6.3 and Definition 6.7, the switching function between vertices 1 and 4 is

$$f_{14} = x_1x_3x_7 + x_2x_4x_8 + x_1x_5x_8 + x_2x_6x_7 + x_1x_3x_6x_4x_8 + x_2x_4x_5x_3x_7 + x_2x_6x_3x_5x_8 + x_1x_5x_4x_6x_7 \tag{6.21}$$

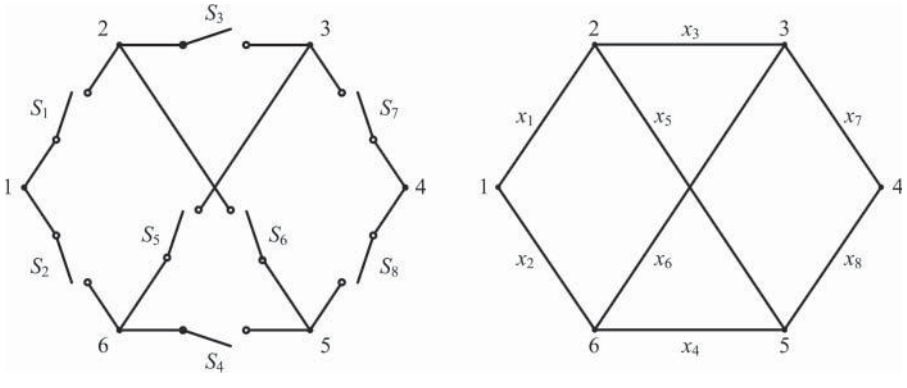


Figure 6.3 A switching network and its undirected graph: (a) switching network; and (b) undirected graph

The Boolean variable corresponding to the switch's state can be independent or associated with other switches, if the Boolean variables in Figure 6.3 are assumed to be

$$x_1 = x, x_2 = \bar{x}, x_3 = \bar{y}, x_4 = \bar{y}, x_5 = x, x_6 = x, x_7 = \bar{z}, x_8 = z \tag{6.22}$$

where *x, y, z* are independent Boolean variables. Then Equation 6.21 is changed to

$$f_{14} = x\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + xyz + x\bar{y}y\bar{y}z + \bar{x}\bar{y}y\bar{y}\bar{z} + xy\bar{y}y\bar{z} + \bar{x}y\bar{y}yz \tag{6.23}$$

According to the Boolean algorithm, Equation 6.23 can be simplified as

$$f_{14} = x\bar{y}\bar{z} + \bar{x}\bar{y}z + xyz + \bar{x}y\bar{z} \tag{6.24}$$

If all the switching variables in the switching network are independent, which means that all switches can be controlled respectively, then the switching network can be named a simple contacting network.

6.3 Sneak Circuit Path Analysis Based on Adjacency Matrix

6.3.1 Directed Graph and Adjacency Matrix of Power Electronic Converter

A power electronic converter generally consists of power supplies, inductors, capacitors, resistors, switching components, and so on. The control circuit, which is connected to the control terminal of three-terminal controllable components such as SCR (semiconductor controlled rectifier), GTO (gate-turn-off thyristor), Power MOSFET IGBT, is always mutually isolated with the main circuit of the converter. The structure of the control circuit will be different because of the control function, so the sneak circuit path analysis of the power electronic converter will be limited to the main circuit only and the control circuit will not be considered. As a result, the three-terminal controllable switch can be simplified to a component with two terminals, as well as the Power diode. If the power source in the power electronic converter is considered as a special component with a bi-directional current, then a given power electronic converter can be transferred to a directed graph.

The directed graph $G = (V, E)$ of a power electronic converter is composed of two finite sets V and E, where the element of vertex set V represents the intersection of components or a terminal of the component in the power electronic converter, which is named by number, the element of edge set E is the component in the converter named by the component symbol, while the direction of the edge is determined by the current direction of the component on the edge. For the edge with power supply, inductor, capacitor, resistor, or the switching component with inverse conduction

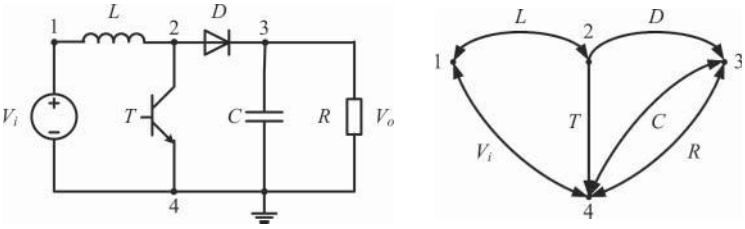


Figure 6.4 Boost converter and its directed graph: (a) vertex definition; and (b) directed graph

properties, it can be indicated by a two-way arrow, because the component current can flow bi-directionally. For the edge with the diode or the switching component without inverse conduction properties, it can be indicated by a uni-directional arrow, which points to the possible flowing direction of the component current.

A Boost converter is taken as an example to explain how to establish the directed graph of a power electronic converter. The schematic diagram of a Boost converter is shown in Figure 6.4a, by defining the components in the converter as the edge and the intersections of the components as the vertices, there are four vertices in the Boost converter.

By considering the component current direction as the edge direction, the directed graph of the Boost converter can be obtained as shown in Figure 6.4b.

According to the definition of an adjacency matrix, the adjacency matrix of a Boost converter is

$$\mathbf{A} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \end{bmatrix} \tag{6.25}$$

Based on Equation 6.25, it is known that $a_{12} = 1$, $a_{23} = 1$, $a_{34} = 1$, and $a_{41} = 1$, so we have $a_{12} \times a_{23} \times a_{34} \times a_{41} = 1$, which means that the vertex sequence 1-2-3-4 represents one current path in the Boost converter. But the vertex sequence 4-3-2-1 is an invalid current path, because diode D is a uni-directional branch and $a_{32} = 0$. Therefore, all the current paths in the power electronic converter can be described by a group of vertex sequences and obtained from the adjacency matrix.

6.3.2 Searching Algorithms

By considering the power electronic converter as a graph, then searching the current paths in the power electronic converter is equivalent to the graph traversal. The common algorithms for graph traversal include breadth-first search and depth-first search.

6.3.2.1 Breadth-First Search Algorithm

The process of the Breadth-first search algorithm can be described by the following steps:

1. Start from any vertex in the graph, such as vertex *i*.
2. Visit the vertices adjacent to vertex *i* in turn.
3. Start from these adjacent vertices respectively, and visit their adjacent in turn.
4. Repeat step (3) until there is no adjacent vertex that has not been visited.
5. If there are vertices that have not been visited in the graph, choose one of them as a starting point. Repeat steps (2) to (4) described above, until all vertices of the graph have been visited.

During the visiting process, if vertices *i* and *j* are adjacent, and vertex *i* is visited before vertex *j*, then all adjacent vertices of *i* must be visited before those of *j*.

A graphic process of the Breadth-first search algorithm is shown in Figure 6.5, where the arrows represent the searching direction, and the numbers beside the arrows are the searching order. By setting vertex A as the starting point, according to the Breadth-first search algorithm, the visiting order of vertices is A-B-E-D-C-G-F-H-I.

6.3.2.2 Depth-First Search Algorithm

The Depth-first search algorithm is different from the Breadth-first search algorithm in its searching routes. It starts from a vertex, and searches the vertices that can be

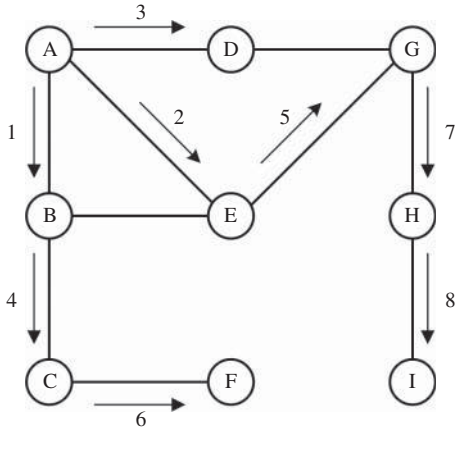


Figure 6.5 Sketch map of breadth-first search process

reached as far as possible along a path emitting from that vertex, until there is no unvisited vertices in that path, then reverses back and continues to search other new vertices. Then, the process of the Depth-first search is described as follows:

1. Start from any vertex in the graph, such as vertex *i*.
2. Search for the adjacent vertices that have not been visited, and select one to visit.
3. Repeat step (2) until the vertex being visited has no unvisited adjacent vertices.
4. Back to the prior vertex that has been visited, select one of its unvisited adjacent vertices and visit. Repeat step (3).
5. If there are vertices in the graph that have not been visited, select one of them as the starting point and repeat steps (2) to (4), until all of the vertices in the graph have been visited.

Taking the graph in Figure 6.5 as an example, the searching process of the Depth-first search algorithm is shown in Figure 6.6, where the solid arrows represent the forward visiting direction, the dotted arrows are the backward visiting direction, and the numbers beside the arrows are the searching order. By setting vertex A as the starting point, according to the Depth-first search algorithm described above, the visiting order of vertices is A-B-C-F-E-G-D-H-I, which is different from the order in Figure 6.5.

Comparing the searching process of the above two algorithms, it is found that the Breadth-first search algorithm has small time complexity but large space complexity, so it is suitable for a graph with small vertices depth; however, the Depth-first search algorithm has large time complexity, but small space complexity, so it is suitable for a graph with large vertices depth. On the other hand, the Depth-first search algorithm traverses the graph by paths, which is suitable for searching current paths in power electronic converters.

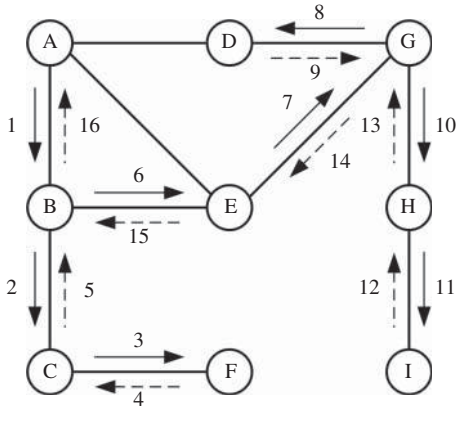


Figure 6.6 Sketch map of depth-first search process

6.3.3 Current Path Search in Power Electronic Converter

Based on the above analysis, all possible current paths in a power electronic converter can be found by using the adjacent matrix and the Depth-first search algorithm. However, according to the basic circuit principles, there must exist at least one voltage source or current source in the current path, thus only the paths with voltage or current source belong to the available current paths.

In a power electronic converter, the power supply and energy storage component, such as inductor or capacitor, can be considered as the typical power elements, thus the two terminals of the power element can be set as the start point and the target point when searching for the current paths. Therefore, all current paths in a power electronic converter can be obtained by searching for the paths between two endpoints of every power element. But if one power element is connected in series with another power element, then a same current path will be searched out twice, thus some modifications should be made in the current searching method.

A basic step-down RSC converter is an example explaining how to search for the current paths. The vertex definition and the directed graph of the basic step-down RSC converter are shown in Figure 6.7.

It is clear that there are three power elements, which are voltage source V_i, resonant tank L_r-C_r, and output capacitor C_o respectively. Since vertices 1 and 5 are the positive and negative points of the voltage source respectively, a current path with vertex sequence 1-2-4-3-5 is obtained by searching for paths between vertices 1 and 5. As vertices 4 and 2 are the terminals of the resonant tank L_r-C_r, a current path with vertex sequence 4-3-5-1-2 can be found. Although the start point and the target point of the above two paths are different, they are, in fact, the same path. In order to avoid redundancy, the power element will be considered as an open circuit after its path searching work is finished, then this power element will not appear in the paths when searching for the next power element.

Therefore, in the basic step-down RSC converter, the power elements will be numbered at first, for example, as the voltage source V_i is #1, the resonant tank L_r-C_r is #2, and the output capacitor C_o is #3. Then the current paths of each power element

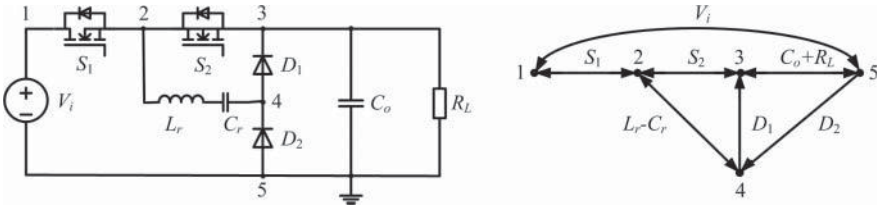


Figure 6.7 Basic step-down RSC converter and its directed graph: (a) vertex definition; and (b) directed graph

will be searched in turn. When the searching work for power element #1 has finished, power element #1 should be an open circuit, which means that the related elements in the adjacency matrix will be set to zero, that is, $a_{15} = a_{51} = 0$. In the following searching process, the paths that pass through power element #1 will not appear. Thus the repeated current path will be effectively prevented in the path searching results; on the other hand, the searching speed will be improved greatly.

6.3.4 Sneak Circuit Path Judgment in Power Electronic Converter

After finding out all possible current paths in a power electronic converter, some criteria should be used to judge the current paths. If a current path is neither an invalid current path nor a normal current path, then it belongs to the sneak circuit path.

The invalid current path refers to the path that will not be allowed in the operation of power electronic converter. In the basic step-down RSC converter shown in Figure 6.7, the control strategy of switches S_1 and S_2 is complementary, therefore the path including vertex sequence 1-2-3 or 3-2-1 is invalid, because both switches are on at the same time. After eliminating the invalid current paths, the rest of the possible current paths are the effective ones.

The normal current paths are the paths that will show up during normal operation of the converter. Comparing the effective current paths with the normal operating paths, the effective current path that is different from any normal path is the sneak current path. During path comparison, the vertex order of the current path to be judged may not be the same as that of the normal path, for example, the vertex order of path 1-2-4-3-5 and that of 4-3-5-1-2 appear different in Figure 6.7, but they are the same path in essence. In order to improve the efficiency and accuracy of path comparison, the vertex shift function, which ensures the current flow and the vertex order of the path remain unchanged, can be used. If the path to be judged has the same start and target vertices and the same vertex sequence as the normal path, then this path belongs to a normal path, not a sneak circuit path.

6.3.5 Sneak Circuit Path Analysis Software Based on Adjacency Matrix

According to the sneak circuit path searching method of the power electronic converter described above, the "sneak circuit path analysis software based on adjacency matrix" has been developed, and its flow chart is shown in Figure 6.8. At first, input the relevant information of power electronic converter, then call the path searching subroutine to find out all current paths in the power converter. Next call the path judgment subroutine to eliminate the invalid paths and normal paths and finally output the sneak circuit paths.

Because a vertex will not appear repeatedly in a current path, and only the paths between the start and target vertices of power element need to be searched, three recursive conditions will be set up in the path searching subroutine:

1. The searched adjacent vertex does not exist in the temporary saved path.
2. The searched adjacency vertex is not the target point.
3. There are some adjacent vertices that are not visited.

Based on the above conditions, the flow chart of the path searching subroutine is illustrated in Figure 6.9.

The main function of the path judgment subroutine is to compare the searched current path with the invalid current path criteria first; if it is not consistent with any invalid criteria, then compare it with all normal current paths successively. If it is different from all normal operating paths, it can be concluded that this path is a sneak circuit path. The procedure of the path judgment subroutine is shown in Figure 6.10.

The three-order step-down RSC converter is selected as an example to explain the feasibility of "sneak circuit path analysis software based on adjacency matrix." The vertex definition of the three-order step-down RSC converter is illustrated in Figure 6.11, and the corresponding adjacency matrix is expressed by

$$\mathbf{A} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{6.26}$$

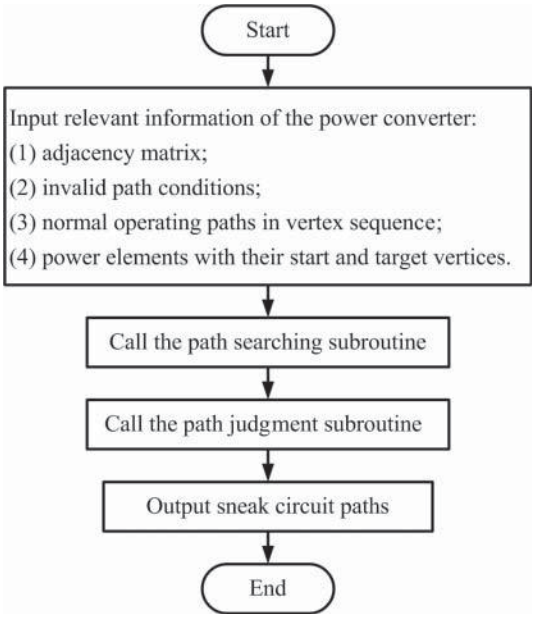


Figure 6.8 Flow chart of sneak circuit path analysis software based on adjacency matrix

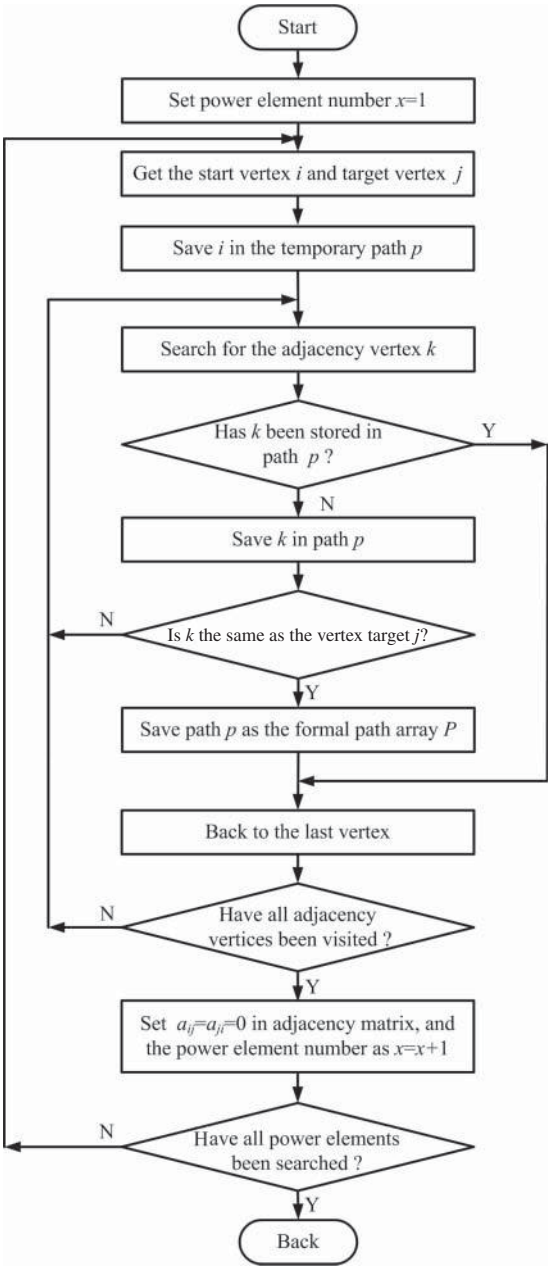


Figure 6.9 Flow chart of current path searching subroutine

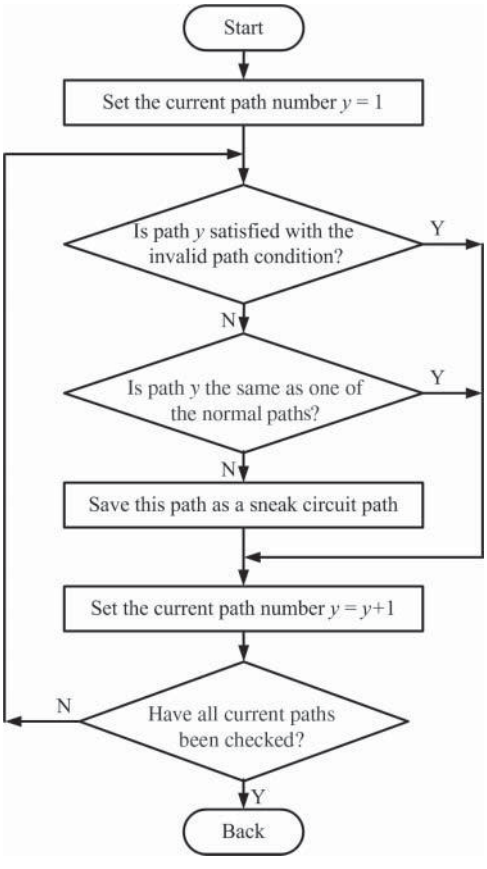


Figure 6.10 Flow chart of path judgment subroutine

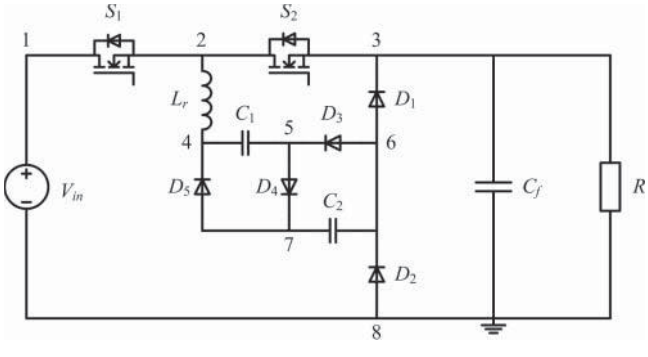


Figure 6.11 Vertex definition of a three-order step-down RSC converter

It is found that there are five power elements in a three-order step-down RSC converter and their terminals are 1 and 8 for V_{in}, 2 and 4 for L_r, 4 and 5 for C_1, 7 and 6 for C_2, and 3 and 8 for C_f, respectively. As all of the power elements can flow in a bi-directional current, there will be ten pairs of vertices needing to be searched. According to the operating principle of the three-order step-down RSC converter, there are four kinds of invalid current path, which are 1-2-3, 3-2-1, 4-3-2, and 4-2-1, and three normal current paths, which are 1-2-4-5-7-6-3-8, 4-2-3-8-6-5, and 7-4-2-3-8-6.

Input all the above information into the developed software, and four sneak circuit paths will be obtained, which are 2-3-8-6-5-7-4, 4-5-7-6-3-2, 5-7-4, and 6-5-7. Combined with Figure 6.11, it is found that the software results are the same as the experimental results in Section 2.3.1.3.

6.4 Sneak Circuit Path Analysis Based on Connection Matrix

6.4.1 Generalized Connection Matrix of Power Electronic Converter

After transferring the main circuit of the power electronic converter into a directed graph, if the edge of the graph is named by the components on the edge, that is, element symbols, then the connection matrix of the power electronic converter is called the generalized connection matrix $\mathbf{C}'$, where its matrix element c'_{ij} is defined by

$$c'_{ij} = \begin{cases} 1, & \text{for } i = j \\ 0, & \text{for } i \neq j, \text{and there is no current path between } i \text{ and } j \\ \text{element symbol}, & \text{for } i \neq j, \text{and there are current paths between } i \text{ and } j \end{cases} \tag{6.27}$$

Referring to the directed graph of the Boost converter in Figure 6.4b, the corresponding generalized connection matrix is

$$\mathbf{C}' = \begin{bmatrix} 1 & L & 0 & V_i \\ L & 1 & D & T \\ 0 & 0 & 1 & (R+C) \\ V_i & 0 & (R+C) & 1 \end{bmatrix} \tag{6.28}$$

As the current path must be a loop in the circuit, then based on Theorem 6.3, all possible current loops in a power electronic converter can be found by calculating the determinant of the generalized connection matrix $\mathbf{C}'$. Thus, the generalized switching function of a Boost converter is

$$\begin{aligned} f_{loop} &= |\det \mathbf{C}'| \\ &= 1 - R^2 - 2RC - C^2 - L^2 + V_i LDR + V_i LDC + V_i LT + L^2R^2 + 2L^2RC + L^2C^2 \end{aligned} \tag{6.29}$$

It is found that there are some terms with squared components in Equation 6.29. The term with two or more powers can be considered as one kind of special loop in graph theory, but in fact the current cannot pass through the same component repeatedly, so the terms with two or more powers must be eliminated from the generalized switching function. In addition, as each term in the generalized switching function represents a current loop of power electronic converter, the coefficient of the term only means the number is the same term in the determinant calculation results and should be unitized in the final results. Therefore, Equation 6.29 is rewritten as

$$f_{loop} = RC + V_iLDR + V_iLDC + V_iLT \tag{6.30}$$

From Equation 6.30, it is found that there are four current loops in the Boost converter, and their equivalent circuits are shown in Figure 6.12. Referring to the analysis of the Boost converter in Section 3.3, the loops in Figure 6.12 can form different operating modes of the Boost converter, where normal operating mode (continuous conduction mode (CCM)) includes loops $V_iLT + RC$ and loops $V_iLDC + V_iLDR$, while the sneak circuit operating mode (discontinuous conduction mode (DCM)) includes loops $V_iLT + RC$, loops $V_iLDC + V_iLDR$, and loop RC. So it is possible to use a generalized switching function to indicate all current loops in a power electronic converter.

6.4.2 *Identification of False Current Loop*

The current loop found by the generalized switching function is a combination of components in the power electronic converter according to the edge direction in essence.

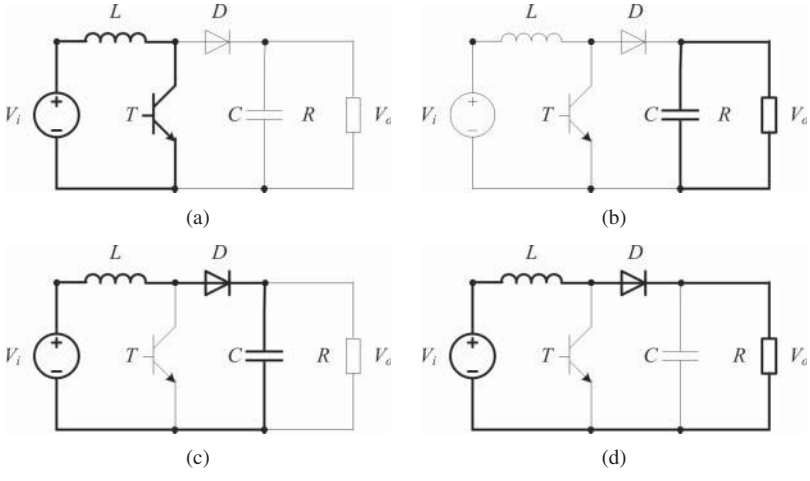


Figure 6.12 Current loops in the Boost converter: (a) V_iLT; (b) RC; (c) V_iLDC; and (d) V_iLDR

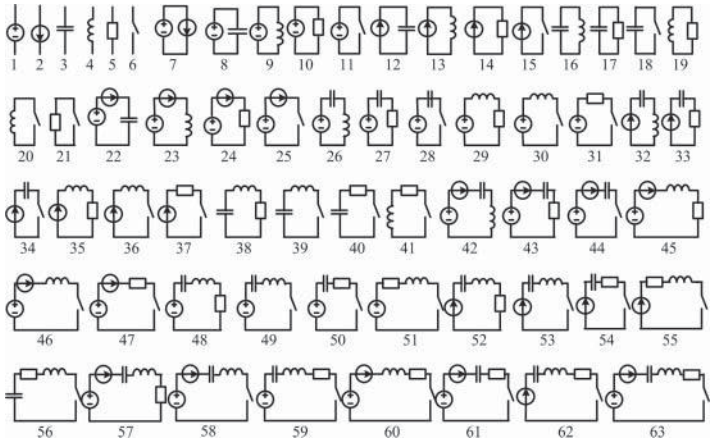


Figure 6.13 Basic current loops in a power electronic converter

Obviously, there will be some false current loops in the calculation results, which are unacceptable or impossible during the operation of the power electronic converter.

It is known that the main circuit of a power electronic converter generally includes voltage source, current source, switching components, capacitor, inductor, resistor, transformer, and so on. A transformer can be considered as a combination of voltage source, inductor, capacitor, and resistor according to its equivalent circuit, voltage source, current source, capacitor, inductor, resistor, and switch belonging to the basic components of the power electronic converter. By combining the above six basic components, there are $C_6^1 + C_6^2 + C_6^3 + C_6^4 + C_6^5 + C_6^6 = 63$ kinds of basic current loops in a power electronic converter, which are shown in Figure 6.13.

According to Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) [4], the 63 kinds of basic current loops in Figure 6.13 have been verified one by one, to distinguish false current loops and effective current loops. The principles in identifying the false current paths are listed as follows:

1. A single component cannot constitute a current loop. Thus basic current loops 1–6 are false.
2. The single voltage source, capacitor, inductor, or resistor cannot be shortened by a switch, while the single current source cannot be opened by a switch. Thus, basic current loops 11, 15, 18, 20, and 21 are false.
3. If there is a current source existing in the current loop, the current direction should be consistent with the direction of that current source. For the basic current loop that includes the current source, for example, loops 7, 12–15, 22–25, 32–37, 42–47, 52–55, 57, 58, and 60–63, if its current direction is different from the current source, then the corresponding basic loop is false.
4. If the voltage source or capacitor supplies energy to the resistor only, the current should flow from the positive point to the negative point of the voltage source or

capacitor. It is found that there are four kinds of basic current loops, that is, 10, 17, 31, and 40, belonging to this case, so if its current direction is from the negative terminal to the positive one, then this loop is the false current loop.

Except for the above circuit principles, the operating principles of the power electronic converter should also be used to identify the false current loops in the calculation results of generalized switching functions as well. After all false loops have been eliminated by both circuit principle and converter operating principle, the remaining current loops belong to the effective ones. The effective current loops, which are used to realize the intended function of the power electronic converter, are the normal current loops, while the rest of effective current loops are the sneak circuit loops.

6.4.3 Example

In this section, the three-order step-up RSC converter is taken as an example to explain how to obtain the sneak circuit loops based on a generalized switching function [5]. The vertices definition of the three-order step-up RSC converter is shown in Figure 6.14a, and the equivalent directed graph is shown in Figure 6.14b, in which the arrow indicates the current direction of the component.

According to the definition of the generalized connection matrix of the power electronic converter, the generalized connection matrix of the three-order step-up RSC

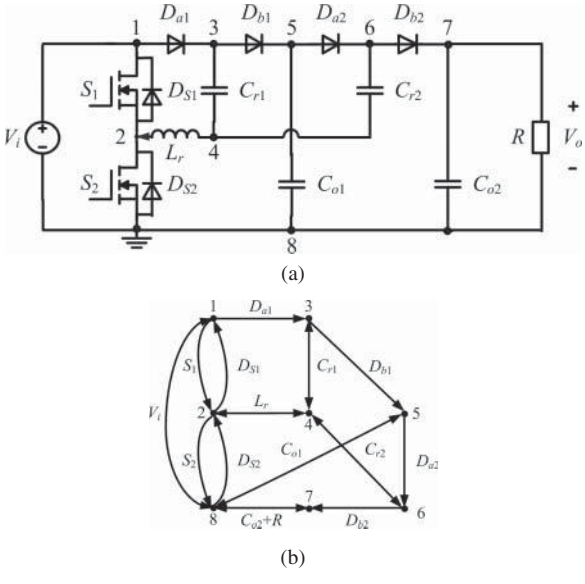


Figure 6.14 Three-order step-up RSC converter and its directed graph: (a) vertex definition; and (b) directed graph

converter is

$$\mathbf{C}' = \begin{bmatrix} 1 & S_1 & D_{a1} & 0 & 0 & 0 & 0 & V_i \\ D_{S1} & 1 & 0 & L_r & 0 & 0 & 0 & S_2 \\ 0 & 0 & 1 & C_{r1} & D_{b1} & 0 & 0 & 0 \\ 0 & L_r & C_{r1} & 1 & 0 & C_{r2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & D_{a2} & 0 & C_{o1} \\ 0 & 0 & 0 & C_{r2} & 0 & 1 & D_{b2} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & C_{o2}+R \\ V_i & D_{S2} & 0 & 0 & C_{o1} & 0 & C_{o2}+R & 1 \end{bmatrix} \tag{6.31}$$

Then all possible current loops of the three-order step-up RSC converter can be obtained by calculating the generalized switching function, which are listed as follows:

No 1. $C_{r2}*D_{a2}*D_{b1}*C_{r1}*S_1*D_{S1}$
No 2. $C_{o1}*D_{b1}*D_{a1}*V_i$
No 3. $C_{o2}*R$
No 4. $D_{s2}*S_2$
No 5. $L_r*C_{r2}*C_{o2}*D_{b2}*S_1*V_i$
No 6. $L_r*C_{r2}*C_{o2}*D_{b2}*D_{s2}$
No 7. $L_r*C_{r2}*R*D_{b2}*S_1*V_i$
No 8. $L_r*C_{r2}*R*D_{b2}*D_{s2}$
No 9. $L_r*C_{o1}*D_{b1}*C_{r1}*D_{s2}$
No 10. $L_r*C_{o1}*D_{b1}*C_{r1}*S_1*V_i$
No 11. $L_r*D_{a2}*C_{o1}*D_{b2}*C_{r1}*D_{a1}*D_{S1}*C_{o2}$
No 12. $L_r*D_{a2}*D_{b1}*D_{a1}*D_{S1}*C_{r2}*C_{o2}*R$
No 13. $D_{a2}*D_{b1}*D_{a1}*D_{S1}*C_{o2}*D_{b2}*D_{s2}$
No 14. $D_{a2}*D_{b1}*D_{a1}*D_{S1}*R*D_{b2}*D_{s2}$
No 15. $C_{r1}*D_{a1}*D_{S1}*L_r*C_{o2}*R$
No 16. $C_{r2}*C_{o2}*D_{b2}*C_{r1}*D_{a1}*V_i$
No 17. $C_{r2}*R*D_{b2}*C_{r1}*D_{a1}*V_i$
No 18. $C_{r2}*D_{a2}*D_{b1}*C_{r1}*S_1*D_{S1}*C_{o2}*R$
No 19. $C_{r2}*D_{a2}*D_{b1}*C_{r1}*C_{o2}*R$
No 20. $S_1*D_{S1}*C_{o2}*R$
No 21. $L_r*D_{a2}*C_{o1}*D_{b2}*C_{r1}*D_{a1}*D_{S1}*R$
No 22. $D_{a2}*C_{o1}*D_{b2}*S_1*D_{S1}*C_{o2}$
No 23. $D_{a2}*C_{o1}*D_{b2}*S_1*D_{S1}*R$
No 24. $D_{a2}*C_{o1}*D_{b2}*C_{o2}$
No 25. $D_{a2}*C_{o1}*D_{b2}*R$
No 26. $L_r*C_{r2}*D_{a2}*C_{o1}*S_2$
No 27. $L_r*C_{r2}*D_{a2}*C_{o1}*V_i*D_{S1}$
No 28. $D_{a2}*D_{b1}*D_{a1}*V_i*D_{b2}*C_{o2}$
No 29. $D_{a2}*D_{b1}*D_{a1}*V_i*D_{b2}*R$
No 30. $L_r*C_{r2}*D_{a2}*D_{b1}*D_{a1}*V_i*S_2$

No 31. C_{r1}*D_{a1}*V_i*L_r*S_2
No 32. C_{r2}*D_{s2}*D_{b2}*C_{r1}*D_{a1}*D_{S1}*C_{o2}
No 33. C_{r2}*D_{s2}*D_{b2}*C_{r1}*D_{a1}*D_{S1}*R
No 34. D_{a2}*D_{b1}*C_{r1}*D_{s2}*D_{b2}*L_r*C_{o2}
No 35. D_{a2}*D_{b1}*C_{r1}*D_{s2}*D_{b2}*L_r*R
No 36. C_{r2}*D_{a2}*D_{b1}*C_{r1}*D_{s2}*S_2
No 37. C_{r2}*D_{a2}*D_{b1}*C_{r1}*D_{s2}*V_i*D_{S1}
No 38. D_{a2}*D_{b1}*C_{r1}*S_1*V_i*D_{b2}*L_r*C_{o2}
No 39. D_{a2}*D_{b1}*C_{r1}*S_1*V_i*D_{b2}*L_r*R
No 40. C_{r2}*D_{a2}*D_{b1}*C_{r1}*S_1*V_i*S_2
No 41. S_1*V_i*S_2
No 42. D_{s2}*V_i*D_{S1} D_{s2}*C_{o1}*D_{b1}*D_{a1}*D_{S1}
No 43. L_r*D_{a2}*D_{b1}*D_{a1}*D_{S1}*C_{r2}
No 44. S_1*D_{S1}
No 45. C_{r1}*D_{a1}*D_{S1}*L_r
No 46. C_{r2}*D_{a2}*D_{b1}*C_{r1}

According to the circuit principle and the operating principles of the three-order step-up RSC converter, among the above 46 current loops, those required to be eliminated include:

1. D_{S1} is the body diode or anti-parallel diode of S_1, and cannot conduct while S_1 is in the on-state. So the loops including D_{S1} and S_1, or D_{S2} and S_2 need to be eliminated.
2. Voltage source V_i will be shortened if S_1 and S_2 conduct at the same time. Thus the loops including S_1 and S_2, or D_{S1} and D_{S2} need to be eliminated.
3. D_{a1} and D_{b1} will make capacitor C_{o1} and voltage source V_i short circuit if they conduct at the same time. Similarly, D_{b1} and D_{a2}, D_{a1} and D_{b2}, D_{a2} and D_{b2} should not be conducted at the same time. Therefore, loops including D_{a1} and D_{b1}, D_{b1} and D_{a2}, D_{a1} and D_{b2}, or D_{a2} and D_{b2} need to be eliminated.

Therefore, it is concluded that there remain 11 effective current loops, which are:

1. No 3. C_{o2}*R
2. No 5. L_r*C_{r2}*C_{o2}*D_{b2}*S_1*V_i
3. No 6. L_r*C_{r2}*C_{o2}*D_{b2}*D_{s2}
4. No 7. L_r*C_{r2}*R*D_{b2}*S_1*V_i
5. No 8. L_r*C_{r2}*R*D_{b2}*D_{s2}
6. No 9. L_r*C_{o1}*D_{b1}*C_{r1}*D_{s2}
7. No 10. L_r*C_{o1}*D_{b1}*C_{r1}*S_1*V_i
8. No 26. L_r*C_{r2}*D_{a2}*C_{o1}*S_2
9. No 27. L_r*C_{r2}*D_{a2}*C_{o1}*V_i*D_{S1}
10. No 31. C_{r1}*D_{a1}*V_i*L_r*S_2
11. No 45. C_{r1}*D_{a1}*D_{S1}*L_r

The equivalent circuits of the effective current loops are shown in Figure 6.15, while Figure 6.15b is made up of loops No. 5 and No. 7, and Figure 6.15c is made up of loops No. 6 and No. 8.

Compared with the equivalent circuits of the high-order step-up RSC converter in normal operating mode, it is found that stage I in Figure 2.29 is composed of Figure 6.15f,h, stage III is composed of Figure 6.15b,e, and stage II or IV is Figure 6.15a. The rest of effective current loops are sneak circuit loops, where Figure 6.15c,d are consistent with Figure 2.30a, and Figure 6.15g,i are consistent with Figure 2.30b. It is obvious that the sneak circuit loop analysis method based on the connection matrix is practicable.

6.4.4 Sneak Circuit Loop Analysis Software Based on Connection Matrix

From the example in Section 6.4.3, all effective current loops in a power electronic converter, including the normal operating loops and the sneak circuit loops, can be found by calculating the generalized switching function. If all steps in the sneak circuit loop analysis process are carried out manually, including defining the generalized connection matrix, eliminating the false current loops, identifying the normal operating loops, and determining the sneak circuit loops, then it will be a huge amount of work for the power electronic converter with a large number of vertices, and it is also easy to make mistakes. Thus, software should be developed to realize the sneak circuit loop analysis method automatically.

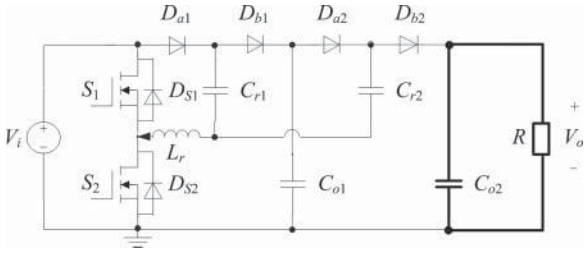
The flow chart of "sneak circuit loop analysis software based on generalized connection matrix" is shown in Figure 6.16.

Firstly, the schematic diagram of the power electronic converter should be established by the specialized software, for example, Altium Designer®. Then the generalized connection matrix of the power electronic converter can be obtained by transferring the net information produced by Altium Designer®. Next, all possible current loops in the power electronic converter can be obtained by calculating the generalized switching function. Based on the operating principle of the power electronic converter, the false loops can be eliminated and the effective current loops will remain. Finally, the sneak circuit loops can be found by comparing the effective loops with the normal operating loops.

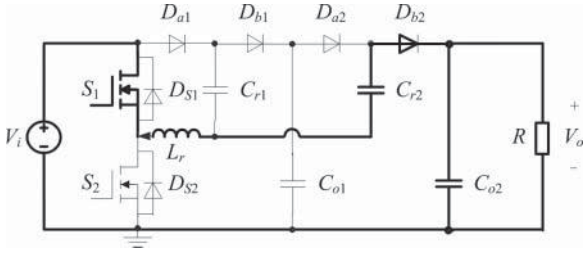
6.5 Sneak Circuit Path Analysis Based on Switching Boolean Matrix

6.5.1 Switching Boolean Matrix of Power Electronic Converter

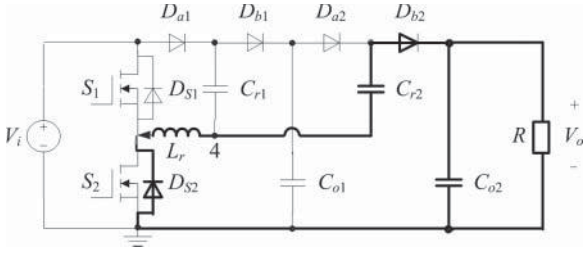
It is known that the topology of a power electronic converter is composed of branches, which contain power supplies, inductors, capacitors, resistors, and



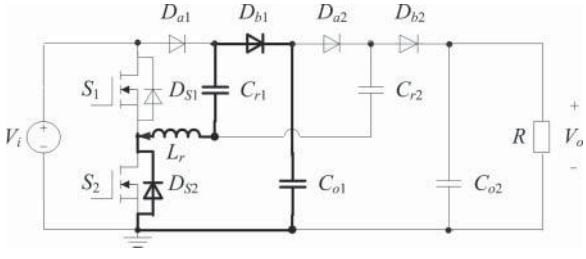
(a)



(b)

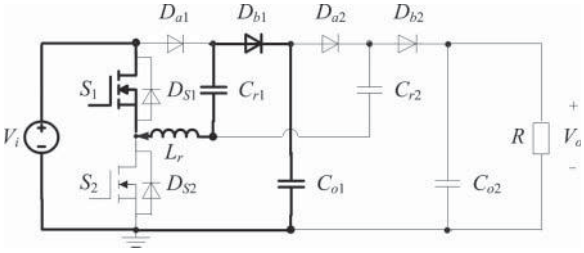


(c)



(d)

Figure 6.15 Effective current loops of three-order step-up RSC converter: (a) C_{o2}*R; (b) L_r*C_{r2}*D_{b2}*S_1*V_i*(C_{o2}+R); (c) L_r*C_{r2} *D_{b2}*D_{s2}*(C_{o2}+R); (d) L_r*C_{o1}*D_{b1}*C_{r1}*D_{s2}; (e) L_r*C_{o1}*D_{b1}*C_{r1}*S_1*V_i; (f) L_r*C_{r2}*D_{a2}*C_{o1}*S_2; (g) L_r*C_{r2}*D_{a2}*C_{o1}*V_i*D_{s1}; (h) C_{r1}*D_{a1}*V_i*L_r*S_2; and (i) C_{r1}*D_{a1}*D_{s1}*L_r



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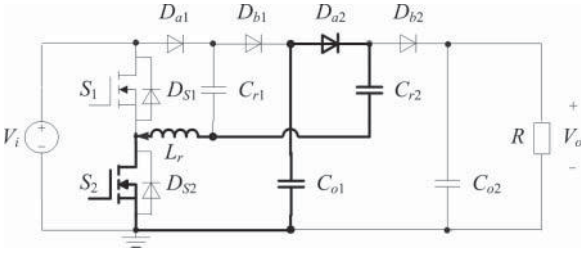

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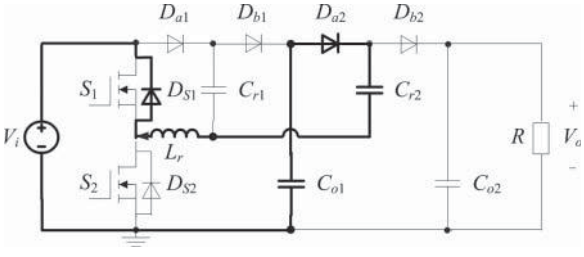

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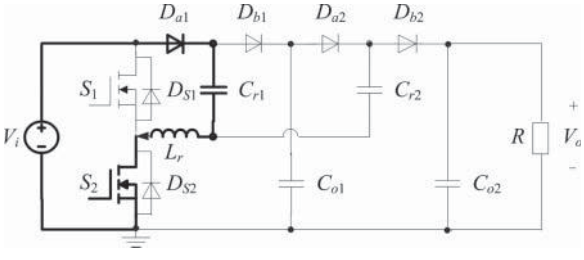

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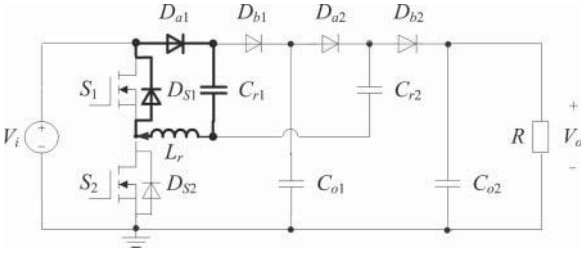

(i)

Figure 6.15 (*continued*)

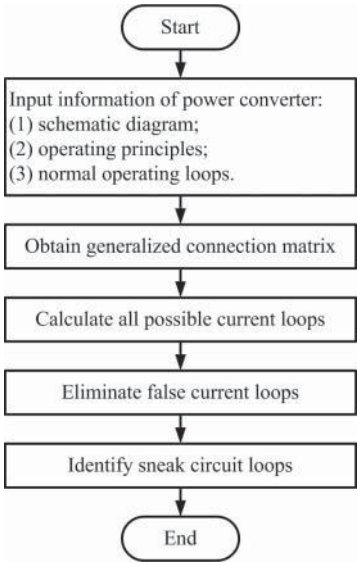

Figure 6.16 Flow chart of sneak circuit loop analysis software based on the connection matrix

switching components, and so on. Generally, the branches in a power electronic converter can be divided into three kinds as follows:

1. For the branch that contains the switching component only, it can be regarded as the switching branch, and its value is dependent on the state of the switch within it, where "1" means switch on and "0" means switch off.
2. For the branch that contains only power supply and/or resistor, it can be regarded as the non-switching branch. This kind of branch can be considered as always being in the on-state from an electrical point of view, then its value can be marked as "1."
3. For the branch that contains energy storage components such as inductor and capacitor, it can be regarded as the generalized switching branch, because its property is related to the energy storage function of the component in the branch. If the stored energy in the branch has been released completely, and its stored energy becomes zero, then the state of the branch can be represented by "0"; if the stored energy in the branch is not equal to zero, then the state of the branch can be represented by "1." If the stored energy is always greater than zero because of the function of the energy storage component, such as the filter capacitor, then the state of this branch can be defined by "1," just like the non-switching branch.

If a power electronic converter contains N switching branches or generalized switching branches and M non-switching branches, then there will be 2^N kinds of branch state combinations at most, which can be expressed by a Boolean matrix

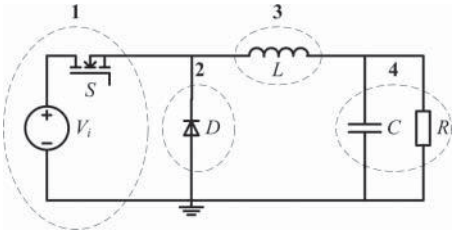

Figure 6.17 Branch definition of a Buck converter

with 2^N rows and $N + M$ columns. This matrix is known as the complete switching Boolean matrix $\mathbf{B_f}$ of a power electronic converter.

The Buck converter is taken as an example to describe how to establish the complete switching Boolean matrix of a power electronic converter. As we know, there are six components in the Buck converter, where the voltage source V_i is in series with switch S, then V_i and S can be considered as a switching branch, diode D also belongs to the switching branch, inductor L is used to transfer energy, so it can be considered as a generalized switching branch, and filter capacitor C and load R can be combined into a non-switching branch. Therefore, there are three switching branches and a non-switching branch in the Buck converter in total, and commonly the switching branches should be numbered first. Then the branches of switch S (and voltage source V_i), diode D, inductor L, and capacitor C (and load R) are numbered as 1 to 4, respectively, which are shown in Figure 6.17.

Due to the Buck converter having three switching branches and one non-switch branch, and the non-switching branch is always in the conducting state, the Buck converter has eight kinds of switching states. Thus the complete switching Boolean matrix of the Buck converter is given by

$$\mathbf{B_f} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \tag{6.32}$$

In theory, every row vector of the complete switching Boolean matrix $\mathbf{B_f}$ corresponds to one of the switching states of a power electronic converter. However, some switching states, which do not coincide with the operating principles of the power electronic converter or the circuit principle, will not appear, so the row vectors including any invalid switching states should be deleted. After the invalid row vectors

are removed from the complete switching Boolean matrix, the rest of the row vectors correspond to the actual switching states of the power electronic converter, and they can compose of a new Boolean matrix, named as the valid switching Boolean matrix $\mathbf{B_a}$.

For the Buck converter, according to the basic circuit principle, the voltage source V_i cannot be in short circuit, which means that branches 1 and 2 should not be in the on-state at the same time. However, as the function of switch S is to provide an energy storage path for inductor L and the function of diode D is to provide an energy releasing path for inductor L, this means that the states of branch 3 should be "1", while the state of branch 1 or 2 is "1."

Therefore, after removing the invalid row vectors in the complete switching Boolean matrix, the valid switching Boolean matrix of a Buck converter is

$$\mathbf{B_a} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \end{bmatrix} \tag{6.33}$$

The equivalent circuits that are corresponding to row vectors in Equation 6.33 are shown in Figure 6.18. Referring to Section 3.2, all operating modes in a Buck converter can be described correctly by the switching Boolean matrix, that is, Equation 6.33.

The Boolean matrix, which is used to express the switching states under normal operating condition, is known as the normal switching Boolean matrix $\mathbf{B_n}$. If the valid switching Boolean matrix $\mathbf{B_a}$ is the same as the normal switching Boolean matrix $\mathbf{B_n}$, there is no sneak circuit in the power electronic converter. If the row number of the valid switching Boolean matrix $\mathbf{B_a}$ is larger than that of the normal switching Boolean matrix $\mathbf{B_n}$, it means that there are some sneak switching states existing in the power electronic converter, and the sneak switching Boolean matrix $\mathbf{B_s}$ can be obtained by eliminating the normal row vectors in the valid switching Boolean matrix $\mathbf{B_a}$.

According to Section 3.2.1, CCM is considered as the normal operating mode of the Buck converter, so the normal switching Boolean matrix of a Buck converter is

$$\mathbf{B_n} = \begin{bmatrix} 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 \end{bmatrix} \tag{6.34}$$

Comparing Equation 6.33 with Equation 6.34, the sneak switching Boolean matrix of the Buck converter can be expressed by

$$\mathbf{B_s} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{6.35}$$

and its corresponding switching state is that branches 1–3 are all off and branch 4 is on, which is consistent with DCM, that is, the sneak circuit phenomenon of the Buck converter described in Section 3.2.2.

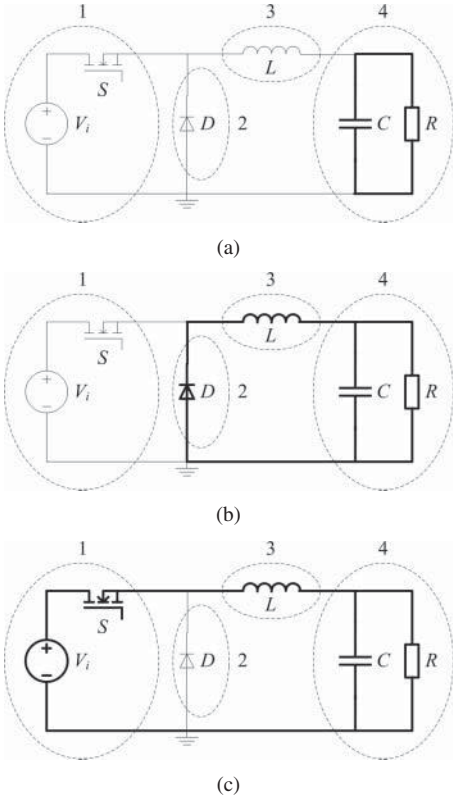

Figure 6.18 Equivalent circuits of the valid switching Boolean matrix of a Buck converter: (a) [0 0 0 1]; (b) [0 1 1 1]; and (c) [1 0 1 1]

6.5.2 Invalid Switching Vector Criteria

According to the above analysis, the valid switching Boolean matrix is derived from the complete switching Boolean matrix by eliminating the invalid row vectors, then it is important to establish some criteria to judge whether the row vector in the complete switching Boolean matrix is invalid or not.

It is clear that the switching state, which does not meet the operating principle of a power electronic converter or basic circuit principle, is defined as the invalid row vector; normally the invalid row vector criteria include the following four kinds:

1. *Short circuit criteria*: If the switching state corresponding to the row vector makes the voltage source or capacitor short circuit, this row vector belongs to the invalid row vector.
2. *Conducting direction criteria*: As power switches and power diodes are semiconductor components, their current direction or conduction direction is unique. If the

conducting switching branches in one row vector cannot constitute a current path, then the corresponding row vector is invalid.
3. *Switching constraint criteria*: For the switching component which has specific constraint condition, if its switching states are inconsistent with the conduction condition, the corresponding row vector is invalid.
4. *Substring criteria*: For the power electronic converter with multiple switching components, if part of the switching components that are turned on cannot constitute a current path, the corresponding row vector is invalid, which can be defined by the substring criteria.

In the complete Boolean matrix of a power electronic converter, if a row vector $x = (x_1, x_2, \ldots, x_n)$ with non-zero switching state is the substring of another row vector $y = (y_1, y_2, \ldots, y_n)$ with non-zero switching state, that is, the row vector x satisfies the following equation, then the row vector x is invalid:

$$\sum_{i=1}^{n} x_i = 1 \quad \text{and } x_i \le y_i \tag{6.36}$$

For the Buck converter, based on its operating principle, the invalid switching vector criteria can be expressed by the following Boolean equations:

$$\begin{aligned} b_{i1} b_{i2} &= 1 \\ b_{i1} \overline{b}_{i3} &= 1 \\ b_{i2} \overline{b}_{i3} &= 1 \\ \overline{b}_{i1} \overline{b}_{i2} b_{i3} &= 1 \end{aligned} \tag{6.37}$$

where $i = 1, 2, \ldots, 8$.

If the row elements in the complete switching Boolean matrix $\mathbf{B_f}$, that is, Equation 6.32, satisfy with any formula in Equation 6.37, then the corresponding row vector is invalid. For example, the second row vector $\begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix}$ in Equation 6.32 should be eliminated because $\overline{b}_{i1} \overline{b}_{i2} b_{i3} = 1$ is established.

6.5.3 Example

The three-order step-up RSC converter is again selected as an example, to describe the sneak circuit path analysis process based on the switching Boolean matrix.

Firstly, the branches in the three-order step-up RSC converter should be defined. As the state of non-switching branch remains at "1" and will not change during the converter operation, the columns according to the non-switching branches can be deleted from the switching Boolean matrixes, in order to reduce the matrix dimension and simplify the matrix calculation. In the three-order step-up RSC converter, the branches with resonant inductor L_r and switching capacitors C_{r1}, C_{o1}, C_{r2}, and

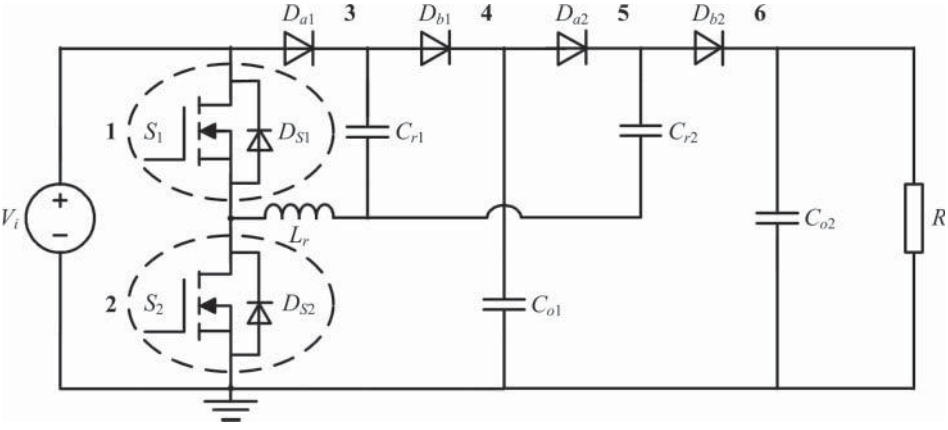

Figure 6.19 Branch definition diagram of a three-order step-up RSC converter

C_{o2} can be defined as the non-switching branches based on their function in the converter. Thus, only the switching branches in the three-order step-up RSC converter will be numbered, as shown in Figure 6.19. The switching branches with switch S_1 (including its anti-parallel diode D_{s1}), S_2 (including its anti-parallel diode D_{s1}), diode D_{a1}, D_{b1}, D_{a2}, and D_{b2} are defined as branches 1 to 6 respectively. The corresponding complete switching Boolean matrix becomes a 64×6 matrix:

$$\mathbf{B_f} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ 1 & 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \tag{6.38}$$

According to the operating principle of the three-order step-up RSC converter, switches S_1 and S_2 conduct half of the switching period in turn, so the row vector in which both branches 1 and 2 are on or off at the same time is invalid.

According to the short circuit criteria, if D_{a1} and D_{b1}, D_{b1} and D_{a2}, D_{a2} and D_{b2}, or D_{a1} and D_{b2} conduct at the same time, the voltage source or capacitor will be shorted,

then the row vector in which branches 3 and 4 (4 and 5, 5 and 6, or 6 and 3) are on at the same time is also invalid. Therefore, the Boolean expressions corresponding to the above invalid criteria are

$$\begin{aligned} b_{i1}b_{i2} &= 1 \\ \overline{b}_{i1}\overline{b}_{i2} &= 1 \\ b_{i3}b_{i4} &= 1 \\ b_{i4}b_{i5} &= 1 \\ b_{i5}b_{i6} &= 1 \\ b_{i6}b_{i3} &= 1 \end{aligned} \tag{6.39}$$

where $i = 1, 2, \ldots, 64$.

The valid switching Boolean matrix of the three-order step-up RSC converter can be obtained by removing the row vectors that meet with Equations 6.36 and 6.39 from the complete switching Boolean matrix, that is, Equation 6.38, which is

$$\mathbf{B_a} = \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{6.40}$$

Referring to the normal operating condition of the three-order step-up RSC converter in Section 6.4.3, there are two normal switching states; one is the branches 2, 3, and 5 being on at same time and the other is branches 1, 4, and 6 being on at same time. Then the corresponding normal switching Boolean matrix is given by

$$\mathbf{B_n} = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 & 1 \end{bmatrix} \tag{6.41}$$

and the Boolean expressions used to describe the normal operating condition of three-order step-up RSC converter are

$$\begin{aligned} b_{i1}\overline{b}_{i2}\overline{b}_{i3}b_{i4}\overline{b}_{i5}b_{i6} &= 1 \\ \overline{b}_{i1}b_{i2}b_{i3}\overline{b}_{i4}b_{i5}\overline{b}_{i6} &= 1 \end{aligned} \tag{6.42}$$

The sneak switching Boolean matrix can be derived by removing the row vectors in $\mathbf{B_a}$, which satisfy Equation 6.42, that is:

$$\mathbf{B_s} = \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{6.43}$$

From Equation 6.43, it is clear that there are two sneak switching states in the three-order step-up RSC converter. One is the branches 2, 4, and 6 conducting at same

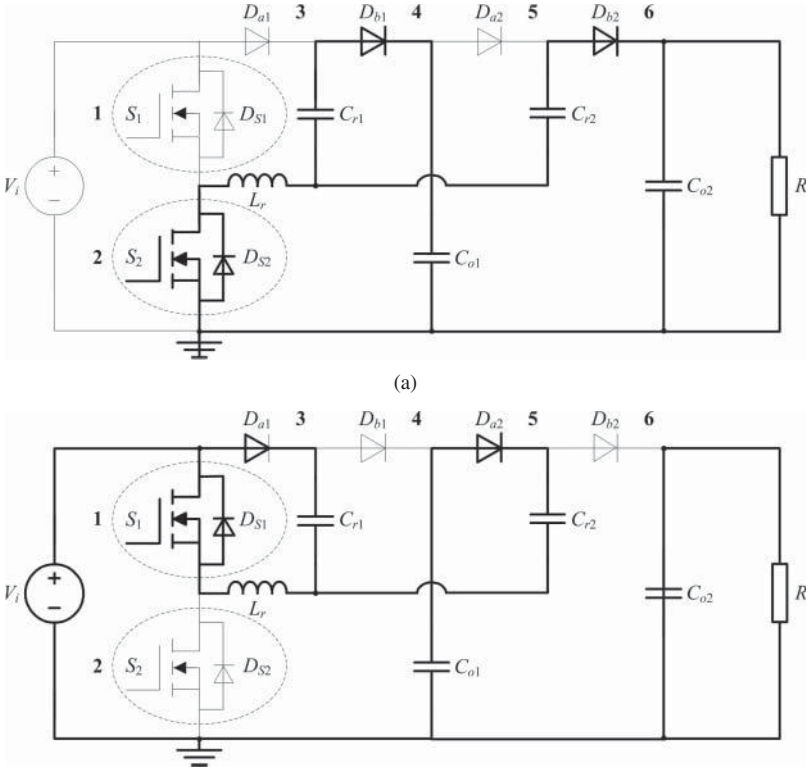

Figure 6.20 Equivalent circuits of the sneak switching Boolean matrix of a three-order step-up RSC converter: (a) [0 1 0 1 0 1]; and (b) [1 0 1 0 1 0]

time and the other is branches 1, 3, and 5 conducting at same time, and the row vectors in $\mathbf{B_s}$ can be transferred to the equivalent circuits shown in Figure 6.20. It is obvious that the sneak circuit path analysis result based on the switching Boolean matrix is consistent with that of the generalized connection matrix, and the sneak circuit paths existing in the converter can be identified directly from the sneak switching Boolean matrix.

6.5.4 Sneak Circuit Path Analysis Software Based on Switching Boolean Matrix

As mentioned above, the basic idea of the sneak circuit path analysis method based on the switching Boolean matrix is to obtain the sneak switching Boolean matrix by eliminating the invalid and normal row vectors from the complete switching Boolean matrix, then transforming the sneak switching Boolean matrix to equivalent circuits, which are the sneak circuits in the power electronic converter.

When there are only a few switching branches in the power electronic converter, the dimension of a complete switching Boolean matrix is small and the sneak circuit analysis can be realized manually, such as with the Buck converter. However, if the number of switching branches is large, it is impossible to check the property of the row vector in the complete switching Boolean matrix one by one. As the invalid and normal switching states can be identified by the Boolean operations, the sneak circuit can be analyzed by the computer, and the flow chart of "sneak circuit path analysis software" based on the switching Boolean matrix is shown in Figure 6.21, which includes the following four steps:

1. According to schematics of the power electronic converter, define the switching branches and establish the complete Boolean switching matrix. If there are N switching branches, then the complete Boolean switching matrix will be an $N \times N$ matrix, like Equation 6.44.
2. Based on the operating principle of the analyzed power electronic converter and basic circuit principle, establish the invalid row vector criteria and the normal operating conditions in the form of Boolean expression.

$$\mathbf{B_f} = \begin{bmatrix} 0 & 0 & \cdots & \cdots & 0 & 0 \\ 0 & 0 & \cdots & \cdots & 0 & 1 \\ 0 & 0 & \cdots & \cdots & 1 & 0 \\ 0 & 0 & \cdots & \cdots & 1 & 1 \\ 0 & 0 & \cdots & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & 1 & \cdots & \cdots & 1 & 1 \\ 1 & 1 & \cdots & \cdots & 0 & 0 \\ 1 & 1 & \cdots & \cdots & 0 & 1 \\ 1 & 1 & \cdots & \cdots & 1 & 0 \\ 1 & 1 & \cdots & \cdots & 1 & 1 \end{bmatrix}_{N \times N} \tag{6.44}$$

3. Check each row vector in the complete Boolean switching matrix, and if the row vector meets with any Boolean expression established in step (2), then it should be eliminated, and the remaining row vectors will constitute the sneak switching Boolean matrix.
4. If the sneak switching Boolean matrix is empty, this means that no sneak circuit exists in the analyzed power electronic converter; if not, the sneak circuits can be obtained by transforming the row vectors of the sneak switching Boolean matrix based on the branch definition of the power electronic converter.

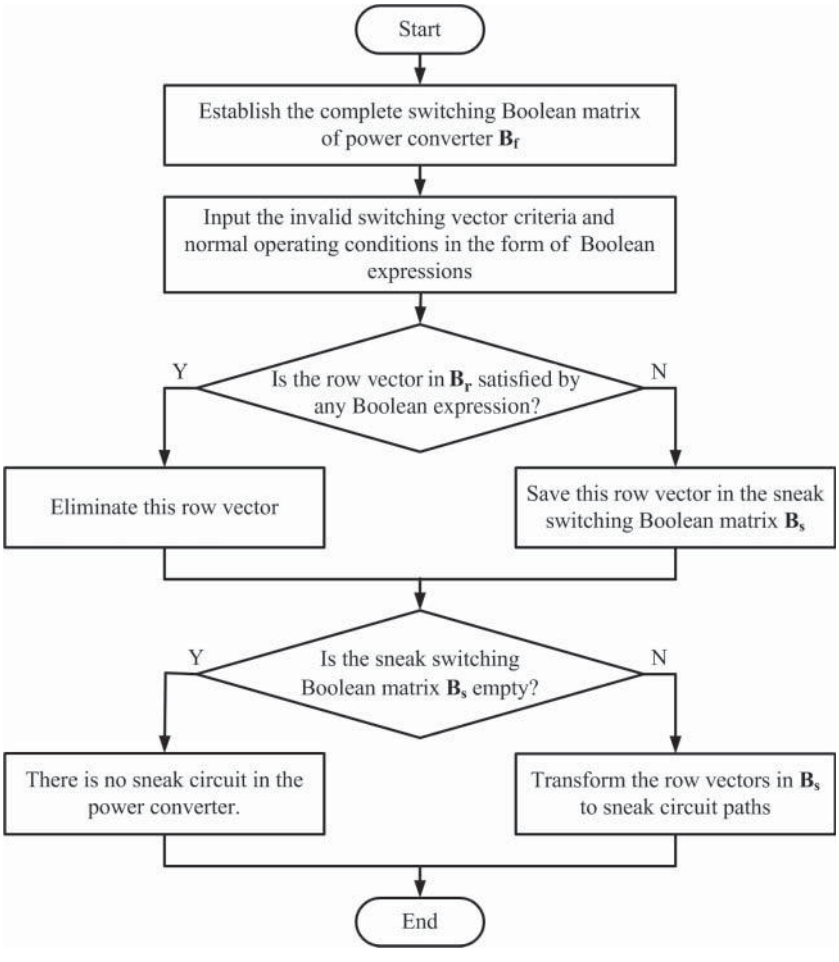

Figure 6.21 Flow chart of sneak circuit analysis software based on the switching Boolean matrix

6.6 Comparison of Three Sneak Circuit Path Analysis Methods

This chapter proposes three sneak circuit path analysis methods of the power electronic converter based on adjacency matrix, connection matrix, and switching Boolean matrix respectively. The differences among these three methods are concluded as follows:

1. The way to describe the topology structure of the power electronic converter is different, with the methods based on the adjacency matrix and the connection matrix needing to know both the relationship between vertices and the direction of edge or the property of the component. The method based on the switching Boolean matrix

only focuses on the property of the branch or component, ignoring the connection between branches.
2. The form of sneak circuit analysis result is different, and the results based on the adjacency matrix are several vertex sequences, which need to be changed to current paths according to the schematic diagram of the power electronic converter. The results based on the connection matrix are some strings with a component name, which are equivalent to the current paths. The results based on the switching Boolean matrix is a switching vector, which can be converted to the equivalent circuits based on the branch definition of the power electronic converter.

The common point among these three sneak circuit path analysis methods is that the normal operating information of the power electronic converter and some invalid criteria should be obtained in advance, and the correctness of sneak circuit analysis results depends on the completeness of the normal operating information or the invalid criteria.

6.7 Summary

Based on graph theory, this chapter introduces three sneak circuit path analysis methods by using adjacency matrix, connection matrix, and switching Boolean matrix respectively. These methods can find all of the current paths existing in the power electronic converter, and then identify the sneak circuit paths according to the operating principles of the power electronic converter. The advantage of the proposed sneak circuit path analysis methods is that all of them can be realized by the computer automatically, thus the sneak circuit analysis of the power electronic converter can be achieved easily.

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7

Sneak Circuit Mode Analysis Method for Power Electronic Converters

7.1 Introduction

According to the definition of a sneak circuit in power electronic converters and sneak circuit phenomena described in Chapters 2–5, the occurrence of sneak circuit phenomenon is due to the current flowing through the sneak circuit paths, and the essence of the phenomenon is a sneak circuit operating mode differing from the normal operating mode. All sneak circuit paths existing in power electronic converters can be found by the sneak circuit path analysis method that was introduced in Chapter 6. But the basic operating unit of the power electronic converter is the equivalent circuit or sub-circuit at every operating stage. Different operating units or sub-circuits are switched in a fixed order during each switching cycle according to the designed control strategy, which constitute the operating mode of the power electronic converter. So it is difficult to know the route of sneak circuit operation or sneak circuit phenomenon of the power electronic converter will be, even if sneak circuit paths in the power electronic converter has been discovered.

This chapter intends to discover all of the operating units or sub-circuits that may exist in the power electronic converter by using some basic graph algorithms [1–3], and then obtains all operating modes in the power electronic converter by assembling the operating units based on the operating principles of the power electronic converter and the switch control strategy. Thereby the sneak circuit phenomenon or sneak circuit mode in a power electronic converter can be predicted by identifying the normal operating mode from the available operating modes. In this chapter, the Cúk converter is taken as an example, to prove the feasibility of the proposed sneak circuit mode analysis method.

Sneak Circuits of Power Electronic Converters, First Edition. Bo Zhang and Dongyuan Qiu.

7.2 Mesh Combination Analytical Method

This chapter will analyze the sneak circuit modes of a power electronic converter based on graph theory, as well as Chapter 6, but the power electronic converter will be considered as a graph made up of several meshes, not paths. Thus, according to the basic graph algorithms, any operating unit or sub-circuit of the power electronic converter is composed by connecting different meshes into the piece or sub-graph.

7.2.1 Mesh and Connecting Piece

According to the basic definition of a graph in Section 6.2, the mesh and connecting piece are defined as follows [1]:

Definition 7.1 Mesh [1] The loop that does not contain an internal loop with an edge is called a mesh, and the vertex on the loop of the mesh is called the mesh element.

Definition 7.2 Connectivity [1] The graph is called connected, if there is a path between each pair of vertices in the graph. Intuitively, the unbroken expanse of the graph is called the connected graph.

Definition 7.3 Connecting piece [1] The connected sub-graph, which has the maximum edge number, is called a connecting piece or simply called a piece.

7.2.2 Basic Graph Algorithms

In set theory, there are four types of binary operation, which are AND, INTERSECTION, DIFFERENCE, and RING SUM, indicated by $\cup$, $\cap$, $-$, and $\oplus$ respectively. The definition of the above four operations are listed as follows:

Definition 7.4 AND operation [1] If S_1 and S_2 are two sets, then the AND operation between S_1 and S_2 (i.e., $S_1 \cup S_2$) represents the set that includes all the elements only in S_1 or S_2 and the common elements in S_1 and S_2.

Similarly, if $G_1(V_1, E_1)$ and $G_2(V_2, E_2)$ are two sub-graphs of graph $G(V, E)$, then $G_1 \cup G_2$ represents a sub-graph of G, the corresponding vertex set is $V_1 \cup V_2$, and the edge set is $E_1 \cup E_2$.

Definition 7.5 INTERSECTION operation [1] If S_1 and S_2 are two sets, then the INTERSECTION operation between S_1 and S_2 (i.e., $S_1 \cap S_2$) represents the set that includes all the common elements in S_1 and S_2.

Obviously, $G_1 \cap G_2$ is a sub-graph of G, the corresponding vertex set is $V_1 \cap V_2$, and the edge set is $E_1 \cap E_2$.

Definition 7.6 DIFFERENT operation [1] If S_1 and S_2 are two sets, then the DIFFERENT operation between S_1 and S_2 (i.e., $S_1 - S_2$) represents the set that includes all the elements only in S_1 and not in S_2.

Definition 7.7 RING SUM operation [1] If S_1 and S_2 are two sets, then the RING SUM operation between S_1 and S_2 (i.e., $S_1 \oplus S_2$) represents the set that includes all the elements, except the common elements of S_1 and S_2.

The RING SUM operation is also called the symmetric difference, because it is the difference between the AND operation and the INTERSECTION operation of S_1 and S_2, that is, $S_1 \oplus S_2 = (S_1 \cup S_2) - (S_1 \cap S_2)$.

Inference 7.1 Mesh Combination If there is no common element in S_1 and S_2, the RING SUM operation results of S_1 and S_2 are consistent with the AND operation result. Similarly, if G_1 and G_2 are two sub-graphs of G without any isolated vertices, then $G_1 + G_2$ is the sub-graph that contains all the edges in G_1 and G_2, while $G_1 \oplus G_2$ is the sub-graph that contains all the edges in G_1 and G_2, except the common edges of G_1 and G_2.

It is clear from the above definitions that only AND and RING SUM operations are needed to compose the meshes into connected pieces.

7.2.3 Mesh Combination Method

An undirected graph containing four meshes is shown in Figure 7.1. If the mesh is represented by the edges of the mesh, then the meshes in Figure 7.1 are defined by $G_1 = \{e_4, e_5\}$, $G_2 = \{e_1, e_3, e_5\}$, $G_3 = \{e_2, e_3, e_6\}$, $G_4 = \{e_6, e_7\}$ respectively.

Based on Definitions 7.4 and 7.7, the AND and RING SUM operation results of meshes G_2 and G_3 are $G_2 \cup G_3 = \{e_1, e_2, e_3, e_5, e_6\}$ and $G_2 \oplus G_3 = \{e_1, e_2, e_5, e_6\}$. The corresponding calculation results are shown in Figure 7.2.

Theorem 7.1 For a graph G with N meshes, if K meshes ($K \leq N$) in graph G are selected, then there will be $K - 1$ operators between the K meshes. If the $K - 1$ operators are restricted to AND and RING SUM operations, then the number of mesh combinations is

$$M_K = C_{K-1}^0 + C_{K-1}^1 + \cdots + C_{K-1}^{K-1} \tag{7.1}$$

For instance, take three meshes G_1, G_2, and G_4 for operation, that is, $K = 3$, then the number of mesh combinations is $M_3 = C_2^0 + C_2^1 + C_2^2 = 4$ according to Theorem 7.1.

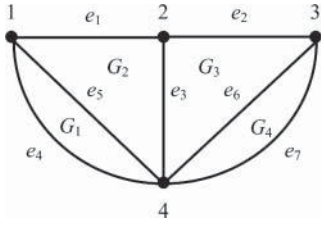


Figure 7.1 An undirected graph with four meshes

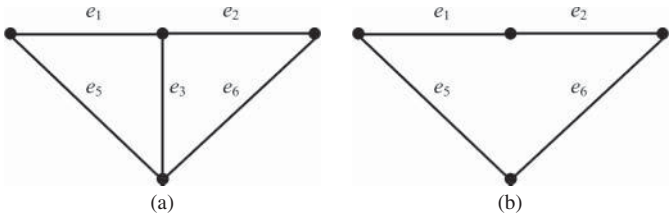


Figure 7.2 Calculation results of G_2 and G_3: (a) $G_2 \cup G_3$; and (b) $G_2 \oplus G_3$

The mesh combination results are $G_1 \cup G_2 \cup G_4$, $G_1 \cup G_2 \oplus G_4$, $G_1 \oplus G_2 \cup G_4$, and $G_1 \oplus G_2 \oplus G_4$, as shown in Figure 7.3.

Figure 7.3 shows that $G_1 \cup G_2 \cup G_4 = G_1 \cup G_2 \oplus G_4$ and $G_1 \oplus G_2 \cup G_4 = G_1 \oplus G_2 \oplus G_4$, because there is no common edge or element in G_1 and G_4. The correctness of Inference 7.1 has been proved.

Theorem 7.2 For a graph G with N meshes, the maximum number of mesh combinations is

$$M_{\max} = \sum_{K=1}^{N} C_N^K \cdot M_K \tag{7.2}$$

It is know that $N = 4$ in Figure 7.1, so the maximum number of mesh combinations is $M_{\max} = 40$. Based on Inference 7.1, some calculation results of Equation 7.2 will be repeated, such as $G_1 \cup G_2 \cup G_4$, $G_1 \cup G_2 \oplus G_4$, $G_1 \oplus G_2 \cup G_4$ and $G_1 \oplus G_2 \oplus G_4$ in Figure 7.3. Then the actual mesh combination results will be less than 40, so we need to find a way to remove the duplicate mesh combination results.

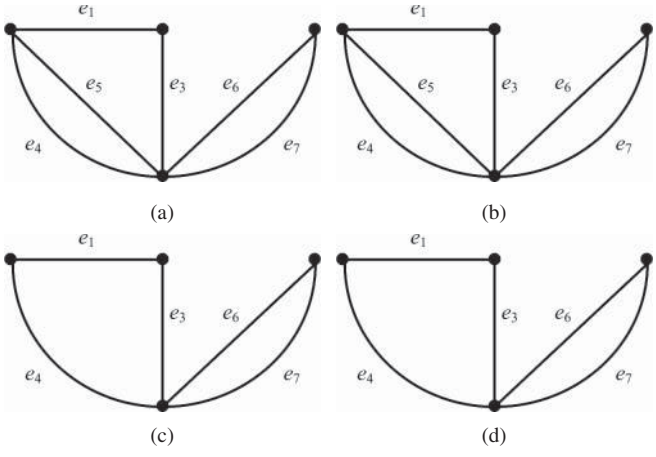
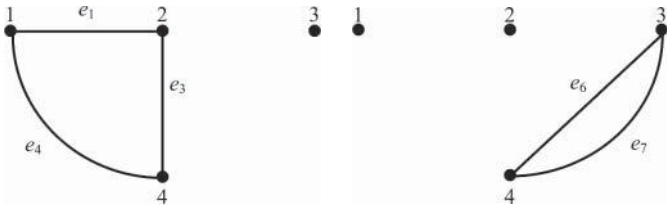


Figure 7.3 Calculation results of G_1, G_2, and G_4: (a) $G_1 \cup G_2 \cup G_4$; (b) $G_1 \cup G_2 \oplus G_4$; (c) $G_1 \oplus G_2 \cup G_4$; and (d) $G_1 \oplus G_2 \oplus G_4$



(a) (b)

Figure 7.4 Connecting pieces among G_1, G_2, and G_4: (a) $G_1 \oplus G_2$; and (b) G_4

Theorem 7.3 For a graph G with N meshes, the number of ways to take K meshes from the total N meshes in graph G is C_N^K. If there are h_i meshes that have no common element in the i-th way ($i = 1, 2, 3, \ldots, C_N^K$), then the number of the connecting piece is h_i, which is defined by

$$h_i = K - l_i \tag{7.3}$$

where l_i is the number of common edges among h_i meshes. In Figure 7.1, assuming that $K = 3$ and G_1, G_2, and G_4 are selected, since the common edge of G_1, G_2, and G_4 is e_5, that is, $l_i = 1$, the number of connecting pieces among them is $h_i = 2$, which are $G_1 \oplus G_2$ and G_4 respectively, as shown in Figure 7.4.

Theorem 7.4 Taking h_i connecting pieces for AND and RING SUM operations, there are $h_i - 1$ operators and 2^{h_i-1} kinds of combination methods. Because the results of AND operation between the connecting pieces are the same to those of the RING SUM operation based on Inference 7.1, the recurrence rate of the operation result among h_i connecting pieces is

$$B_i = \frac{2^{h_i-1} - 1}{2^{h_i-1}} \tag{7.4}$$

Therefore, in the mesh combination result of the ith K meshes, the number of repeated mesh combinations is

$$B_i M_K = \frac{2^{h_i-1} - 1}{2^{h_i-1}} \left(C_{K-1}^0 + C_{K-1}^1 + \cdots + C_{K-1}^{K-1} \right) \tag{7.5}$$

Based on Equations 7.4 and 7.5, the recurrence rate of the connecting pieces when $h_i = 2$ is $B_i = \frac{1}{2}$, and the number of the repeated combinations of the mesh when $M_K = 4$ is $B_i M_K = \frac{1}{2} \times 4 = 2$, which is verified by the results in Figure 7.3.

Theorem 7.5 For a graph G with N meshes, the largest number of mesh combinations is $M_{\max}$, so the number of repeated mesh combinations that need to be eliminated is

$$M_T = \sum_{K=1}^{N} \sum_{i=1}^{C_N^K} B_i M_K \tag{7.6}$$

so the number of non-repeated mesh combinations is

$$M = M_{\max} - M_T = \sum_{K=1}^{N} \left(C_N^K - \sum_{i=1}^{C_N^K} \frac{2^{h_i-1} - 1}{2^{h_i-1}} \right) \left(C_{K-1}^0 + C_{K-1}^1 + \cdots + C_{K-1}^{K-1} \right) \quad (7.7)$$

7.3 Sneak Operating Unit Analytical Method

For power electronic converters, a sub-circuit in accord with the certain turn-on and turn-off control sequence of switching component is called the operating unit. If a power electronic converter is converted to a graph, then the sub-circuit corresponding to the operating unit might be equivalent to a sub-graph. Based on the mesh combination method in Section 7.2, the non-repeated mesh combinations obtained are equal to the sub-graphs, that is, the possible operating units in power electronic converters.

According to Theorem 7.5, if a power electronic converter has M non-repeated mesh combinations, this means that this converter contains a maximum of M sub-circuits or operating units. In these M operating units, the one that does not meet the circuit principle or the operating principle of the converter belongs to the invalid operating unit, and should be eliminated according to the constraint conditions of operating modes. After removing the invalid operating units, those remaining are called the effective operating units. In the effective operating modes, those corresponding to normal operating conditions belong to normal operating units, and the others are named as sneak operating units.

The Cúk converter is selected as an example to explain how to use mesh combination algorithms to obtain effective operating units, normal operating units, and sneak operating units.

7.3.1 Mesh Combination Results of Cúk Converter

According to the schematic diagram, the Cúk converter can be considered to be made up of four meshes, G_1, G_2, G_3, and G_4, which are shown in Figure 7.5. If the components of the Cúk converter are used to represent the mesh elements, then the meshes in the Cúk converter are expressed by

$$\begin{aligned} G_1 &= \{V_i,\ L_1,\ S\} \\ G_2 &= \{S,\ C_1,\ D\} \\ G_3 &= \{D,\ C,\ L_2\} \\ G_3 &= \{C,\ R\} \end{aligned} \quad (7.8)$$

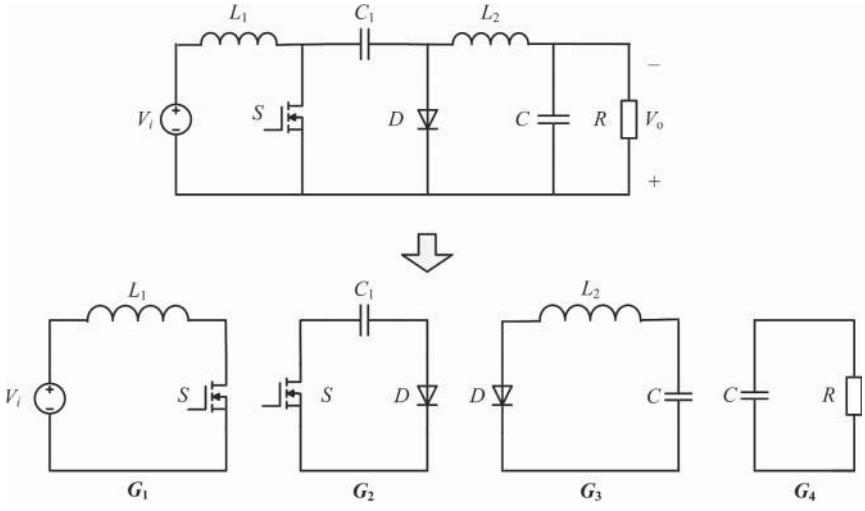


Figure 7.5 The Cúk converter and its meshes

According to the AND and RING SUM operations, and Theorems 7.3 and 7.4, the mesh combination results of a Cúk converter, including the number of connecting pieces h_i and the repetition rate B_i under various mesh combinations, are listed in Table 7.1.

It is known that the mesh number of a Cúk converter is $N = 4$; according to Theorem 7.5, the maximum number of mesh combination results in a Cúk converter is $M_{\max} = 40$. Based on Equation 7.7 and Table 7.1, the repeated mesh combination results that need to be eliminated are $M_T = 7$, then the number of non-repeated mesh combination results or actual sub-circuits in a Cúk converter is $M = 33$. The corresponding equivalent circuits of 33 non-repeated mesh combination results are shown in Table 7.2.

7.3.2 Effective Operating Units of Cúk Converter

In order to eliminate the invalid sub-circuits in the above 33 mesh combination results, the constraint conditions of a Cúk converter should be built by considering the basic circuit principle and the operating principle of the Cúk converter [4–7]:

1. Switch S and diode D cannot be turned on simultaneously, otherwise it will cause capacitor C_1 to be short circuit.
2. The currents flow to L_1 and L_2 should be zero or non-zero at the same time.
3. Because the capacitance of C is large enough, the capacitor C is always in parallel with load resistor R.

Table 7.1 Mesh combination results of the Cúk converter

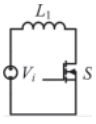
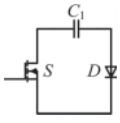
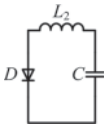
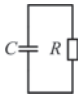
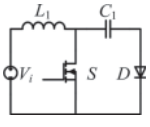
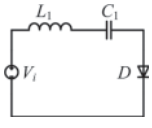
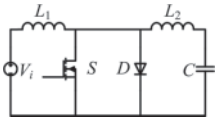
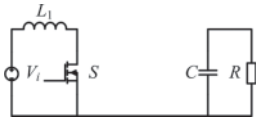
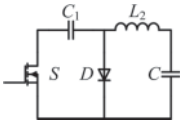
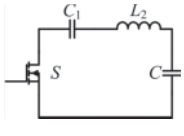
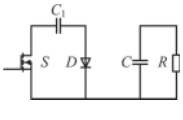
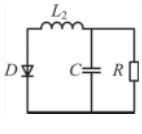
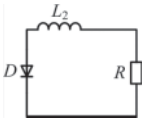
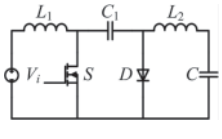
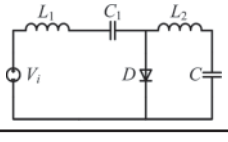
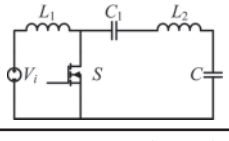
K	The selected mesh	Mesh calculation results	M_K	l_i	h_i	B_i
1	G_1	G_1	1	0	1	0
	G_2	G_2		0	1	0
	G_3	G_3		0	1	0
	G_4	G_4		0	1	0
2	G_1, G_2	$G_1 \cup G_2, G_1 \oplus G_2$	2	1	1	0
	G_1, G_3	$G_1 \cup G_3, G_1 \oplus G_3$		0	2	1/2
	G_1, G_4	$G_1 \cup G_4, G_1 \oplus G_4$		0	2	1/2
	G_2, G_3	$G_2 \cup G_3, G_2 \oplus G_3$		1	1	0
	G_2, G_4	$G_2 \cup G_4, G_2 \oplus G_4$		0	2	1/2
	G_3, G_4	$G_3 \cup G_4, G_3 \oplus G_4$		1	1	0
3	G_1, G_2, G_3	$G_1 \cup G_2 \cup G_3, G_1 \oplus G_2 \cup G_3,$ $G_1 \cup G_2 \oplus G_3, G_1 \oplus G_2 \oplus G_3$	4	2	1	0
	G_1, G_2, G_4	$G_1 \cup G_2 \cup G_4, G_1 \cup G_2 \oplus G_4,$ $G_1 \oplus G_2 \cup G_4, G_1 \oplus G_2 \oplus G_4$		1	2	1/2
	G_1, G_3, G_4	$G_1 \cup G_3 \cup G_4, G_1 \oplus G_3 \cup G_4,$ $G_1 \cup G_3 \oplus G_4, G_1 \oplus G_3 \oplus G_4$		1	2	1/2
	G_2, G_3, G_4	$G_2 \cup G_3 \cup G_4, G_2 \oplus G_3 \cup G_4,$ $G_2 \cup G_3 \oplus G_4, G_2 \oplus G_3 \oplus G_4$		2	1	0
4	G_1, G_2, G_3, G_4	$G_1 \cup G_2 \cup G_3 \cup G_4,$ $G_1 \oplus G_2 \cup G_3 \cup G_4,$ $G_1 \cup G_2 \oplus G_3 \cup G_4,$ $G_1 \cup G_2 \cup G_3 \oplus G_4,$ $G_1 \oplus G_2 \oplus G_3 \cup G_4,$ $G_1 \oplus G_2 \cup G_3 \oplus G_4,$ $G_1 \cup G_2 \oplus G_3 \oplus G_4,$ $G_1 \oplus G_2 \oplus G_3 \oplus G_4$	8	3	1	0

The above constraint conditions can be transformed to equations of mesh elements, which are

$$\begin{aligned} S \cdot D &= 1 \\ L_1 \oplus L_2 &= 1 \\ C \cdot R &= 0 \end{aligned} \tag{7.9}$$

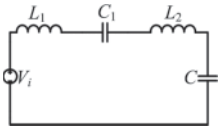
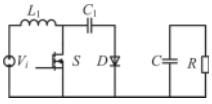
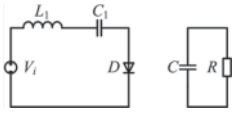
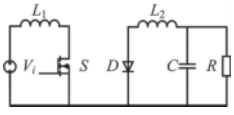
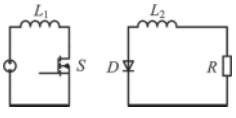
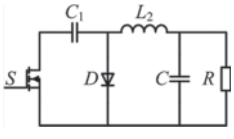
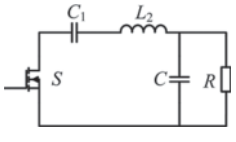
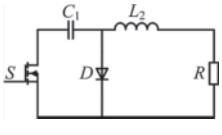
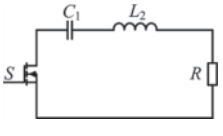
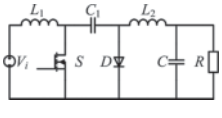
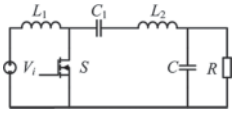
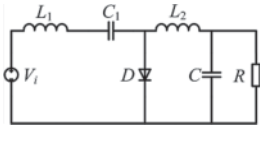
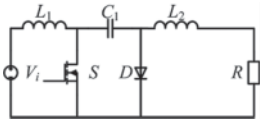
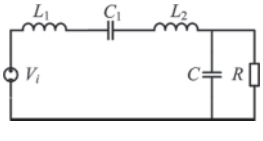
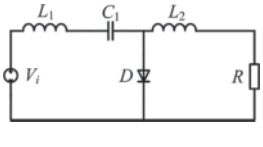
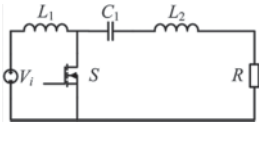
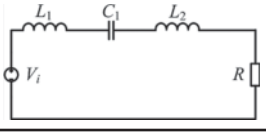
If the mesh elements in one mesh combination result satisfy at least one of the conditions in Equation 7.9, then the related sub-circuit or operating state is invalid. For example, the mesh combination result No. 1 in Table 7.2 (i.e. G_1) is invalid, because the mesh elements in $G_1 = \{V_i, L_1, S\}$, satisfy $L_1 \oplus L_2 = 1$ and $C \cdot R = 0$. Taking the

Table 7.2 Equivalent circuits of mesh combination results in the Cúk converter

No.	Mesh combination result	Equivalent circuit	No.	Mesh combination result	Equivalent circuit
1	G_1		2	G_2	
3	G_3		4	G_4	
5	$G_1 \cup G_2$		6	$G_1 \oplus G_2$	
7	$G_1 \cup G_3$ or $G_1 \oplus G_3$		8	$G_1 \cup G_4$ or $G_1 \oplus G_4$	
9	$G_2 \cup G_3$		10	$G_2 \oplus G_3$	
11	$G_2 \cup G_4$ or $G_2 \oplus G_4$		12	$G_3 \cup G_4$	
13	$G_3 \oplus G_4$		14	$G_1 \cup G_2 \cup G_3$	
15	$G_1 \oplus G_2 \cup G_3$		16	$G_1 \cup G_2 \oplus G_3$	

(*continued overleaf*)

Table 7.2 (*continued*)

No.	Mesh combination result	Equivalent circuit	No.	Mesh combination result	Equivalent circuit
17	$G_1 \oplus G_2 \oplus G_3$		18	$G_1 \cup G_2 \cup G_4$ or $G_1 \cup G_2 \oplus G_4$	
19	$G_1 \oplus G_2 \cup G_4$ or $G_1 \oplus G_2 \oplus G_4$		20	$G_1 \cup G_3 \cup G_4$ or $G_1 \oplus G_3 \cup G_4$	
21	$G_1 \cup G_3 \oplus G_4$ or $G_1 \oplus G_3 \oplus G_4$		22	$G_2 \cup G_3 \cup G_4$	
23	$G_2 \oplus G_3 \cup G_4$		24	$G_2 \cup G_3 \oplus G_4$	
25	$G_2 \oplus G_3 \oplus G_4$		26	$G_1 \cup G_2 \cup G_3 \cup G_4$	
27	$G_1 \cup G_2 \oplus G_3 \cup G_4$		28	$G_1 \oplus G_2 \cup G_3 \cup G_4$	
29	$G_1 \cup G_2 \cup G_3 \oplus G_4$		30	$G_1 \oplus G_2 \oplus G_3 \cup G_4$	
31	$G_1 \oplus G_2 \cup G_3 \oplus G_4$		32	$G_1 \cup G_2 \oplus G_3 \oplus G_4$	
33	$G_1 \oplus G_2 \oplus G_3 \oplus G_4$				

mesh combination result #5 as another example, its corresponding mesh set $G_1 \cup G_2 = \{V_i, L_1, S, C_1, D\}$ satisfies all three conditions in Equation 7.9, so it also needs to be eliminated. Similarly, by judging the 33 mesh combination results in Table 7.2 one by one, we eliminate the invalid sub-circuits, then the effective operating units of the Cúk converter can be obtained, which are:

1. G_4 (Mesh combination result #4);
2. $G_1 \cup G_2 \oplus G_3 \cup G_4$ (Mesh combination result #27);
3. $G_1 \cup G_2 \oplus G_3 \cup G_4$ (Mesh combination result #28);
4. $G_1 \oplus G_2 \oplus G_3 \cup G_4$ (Mesh combination result #30).

7.3.3 Sneak Operating Units of Cúk Converter

Referring to the normal operating mode of the Cúk converter in Section 3.6.1, it is known that two effective operating units $G_1 \cup G_2 \oplus G_3 \cup G_4$ and $G_1 \oplus G_2 \cup G_3 \cup G_4$ belong to the normal operating modes, which correspond to when switch S or diode D is on respectively, and their equivalent circuits are shown in Figure 7.6. Then the remaining two effective operating units $G_1 \oplus G_2 \oplus G_3 \cup G_4$ and G_4 belong to the sneak operating units, of which the equivalent circuits are shown in Figure 7.7.

The above analysis shows that all the operating units of a Cúk converter can be found accurately by using the mesh combination method, then the invalid operating ones can be eliminated according to the operating principle of the Cúk converter. Finally, the sneak operating units can be distinguished by comparing the effective operating units

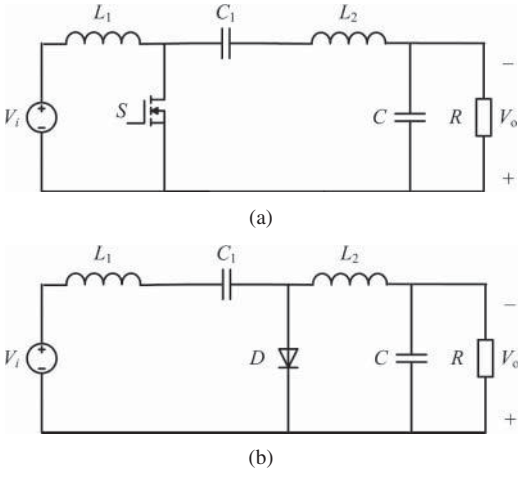


Figure 7.6 Equivalent circuits of normal operating units of the Cúk converter: (a) normal operating unit 1 $-G_1 \cup G_2 \oplus G_3 \cup G_4$; and (b) normal operating unit 2 $-G_1 \oplus G_2 \cup G_3 \cup G_4$

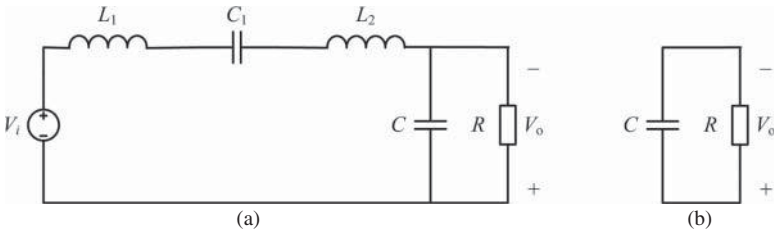


Figure 7.7 Equivalent circuits of sneak operating units of the Cúk converter: (a) sneak operating unit 1 $-G_1 \oplus G_2 \oplus G_3 \cup G_4$; and (b) sneak operating unit 2 $-G_4$

with the normal ones. As there are sneak operating units in a Cúk converter, it may contain sneak circuit phenomenon.

7.4 Sneak Circuit Operating Mode Analytical Method

It is well known that the switching components in the power electronic converter are turned on or off according to a certain control strategy, so the power electronic converter will operate in different operating units in one switching cycle. Then the combination of operating units in a fixed order constitutes the operating mode of the power electronic converter. Apparently, any operating mode of a power electronic converter is the orderly arranged results of effective operating units.

As all the effective operating units can be obtained by using the mesh combination method described in Section 7.3, all the operating modes can be found by combining the effective operating units with the control strategy. Defining the designed or desired operating mode of the power electronic converter is the normal operating mode, then the corresponding operating units in the normal operating mode are the normal operating units, and the corresponding current directions in the normal operating mode are the normal current directions. Therefore, the operating mode, which differs from the normal operating modes, is known as the sneak circuit operating mode, and sneak circuit phenomenon will occur when the power electronic converter works in the sneak circuit operating mode.

If the current direction of the component is not taken into account and only the form of sub-circuit is considered, then the operating mode containing any sneak operating unit is called the sneak circuit phenomenon caused by variations of topology. If the current direction of the component is taken into account, as well as the form of sub-circuit, then the operating mode contains a current direction different from the normal operating conditions, and is called the sneak circuit phenomenon caused by change in current direction.

This section continues to takes the Cúk converter as an example, to illustrate how to analyze sneak circuit operating modes of the power electronic converter in two aspects; one is variation of topology and the other is change of current direction.

7.4.1 *Sneak Circuit Phenomenon of Cúk Converter Caused by Variations of Topology*

Theorem 7.6 For a power electronic converter with J switching components S_1, $S_2, \ldots, S_J$, the sub-circuit satisfying the control sequence of switching components is called the operating mode. Thus, there is only one control sequence if all of the J switches are controllable; there are 2^E kinds of control sequence if E switches among the J switches (i.e. $E<=J$) are uncontrollable, and each uncontrollable switch only has on and off conditions.

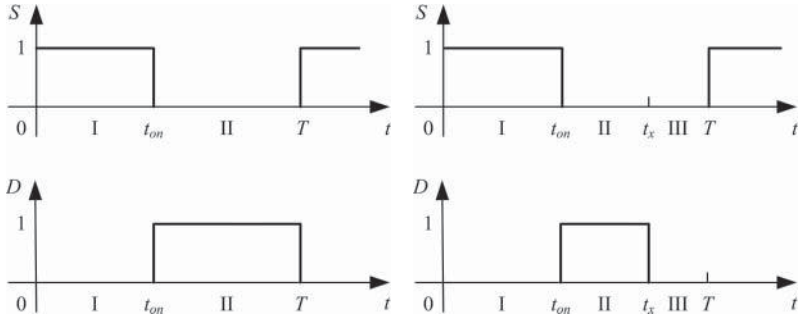
The Cúk converter has two switching components, which are switch S and diode D, and D is an uncontrollable component, so it has 2^1 kinds of control sequences. If "1" indicates that the switching component is on, and "0" indicates that it is off, and it is known that the operating state which satisfies $S \cdot D = 1$ (i.e., $SD = 11$) is invalid, then the Cúk converter has three operating states, that is, $SD = 10$, $SD = 01$, and $SD = 00$. Then the above three switch states can comprise two kinds of switch control sequences in the Cúk converter, as shown in Figure 7.8.

Each switching cycle under switch control sequence 1 contains two switch states, where the duration of $SD = 10$ is t_{on} or stage I, and the duration of $SD = 01$ is $T - t_{on}$ or stage II. Each switching cycle under switch control sequence 2 contains three switch states, there is one more state than control sequence 1, and the duration of $SD = 01$ is $t_x - t_{on}$ or stage II, and the duration of $SD = 00$ is $T - t_x$ or stage III.

Comparing the effective operating units to the on-off state of switches in the Cúk converter, the results are shown in Table 7.3.

Referring to the on-off state control sequences in Figure 7.8 and the effective operating units in Table 7.3, the operating modes of the Cúk converter can be obtained as follows:

1. Operating mode with the operating units in Figure 7.6a,b, which is the normal operating mode by referring to the normal operating principle of the Cúk converter described in Section 3.6.1;



(a) (b)

Figure 7.8 Switch control sequences of the Cúk converter: (a) sequence 1; and (b) sequence 2

Table 7.3 Relationships between switch state and operating unit of the Cúk converter

Stage	State		Effective operating unit	Figure number
	S	*D*		
I	1	0	Normal operating unit 1	Figure 7.6a
II	0	1	Normal operating unit 2	Figure 7.6b
III	0	0	Sneak operating unit 1	Figure 7.7a
			Sneak operating unit 2	Figure 7.7b

2. operating mode with the operating units in Figures 7.6a,b and 7.7a, which is the sneak circuit operating mode 1 containing sneak circuit operating unit 1;
3. operating mode with the operating units in Figures 7.6a,b and 7.7b, which is the sneak circuit operating mode 2 containing sneak circuit operating unit 2.

The equivalent circuits of the above three operating modes are illustrated in Figure 7.9. It is obvious that all of the operating modes of the Cúk converter can be derived by combining the effective operating units with the switch control sequence, thus the sneak circuit operating mode with sneak operating units can be distinguished from the normal operating mode.

7.4.2 Sneak Circuit Phenomenon of Cúk Converter Caused by Changing of Current Direction

It is known that the currents of power source, inductor, capacitor, resistor, and switch with reverse conducting properties can flow bi-directionally, while the currents of diode and switch without reverse conducting properties flow in only one direction. In the analysis of sneak circuit operating modes when considering the current direction, the effective operating unit of a power electronic converter can be classified according to the direction of the current flow in the mesh.

Taking the normal operating unit 1 in Figure 7.6a as an example, it contains three independent meshes G_1, $G_2 \oplus G_3$, and G_4. Among these meshes, G_4 is a mesh without any switching component and only consists of passive devices, so G_4 can be simplified as a branch, and it is unnecessary to discuss the current direction inside G_4. Therefore, only meshes G_1 and $G_2 \oplus G_3$ need to be considered when investigating the mesh current direction of normal operating unit 1.

If the current direction of G_1 and $G_2 \oplus G_3$ are considered respectively, according to the unilateral conductivity of switch S, the direction of mesh current, which is represented by the inductor current i_{L1} or i_{L2}, is shown in Figure 7.10a. Referring to the normal operating condition of the Cúk converter in Section 3.6.1, the current direction 1 in Figure 7.10a is the normal current direction and is also defined as the positive direction of inductor currents, that is, $i_{L1} > 0$ and $i_{L2} > 0$.

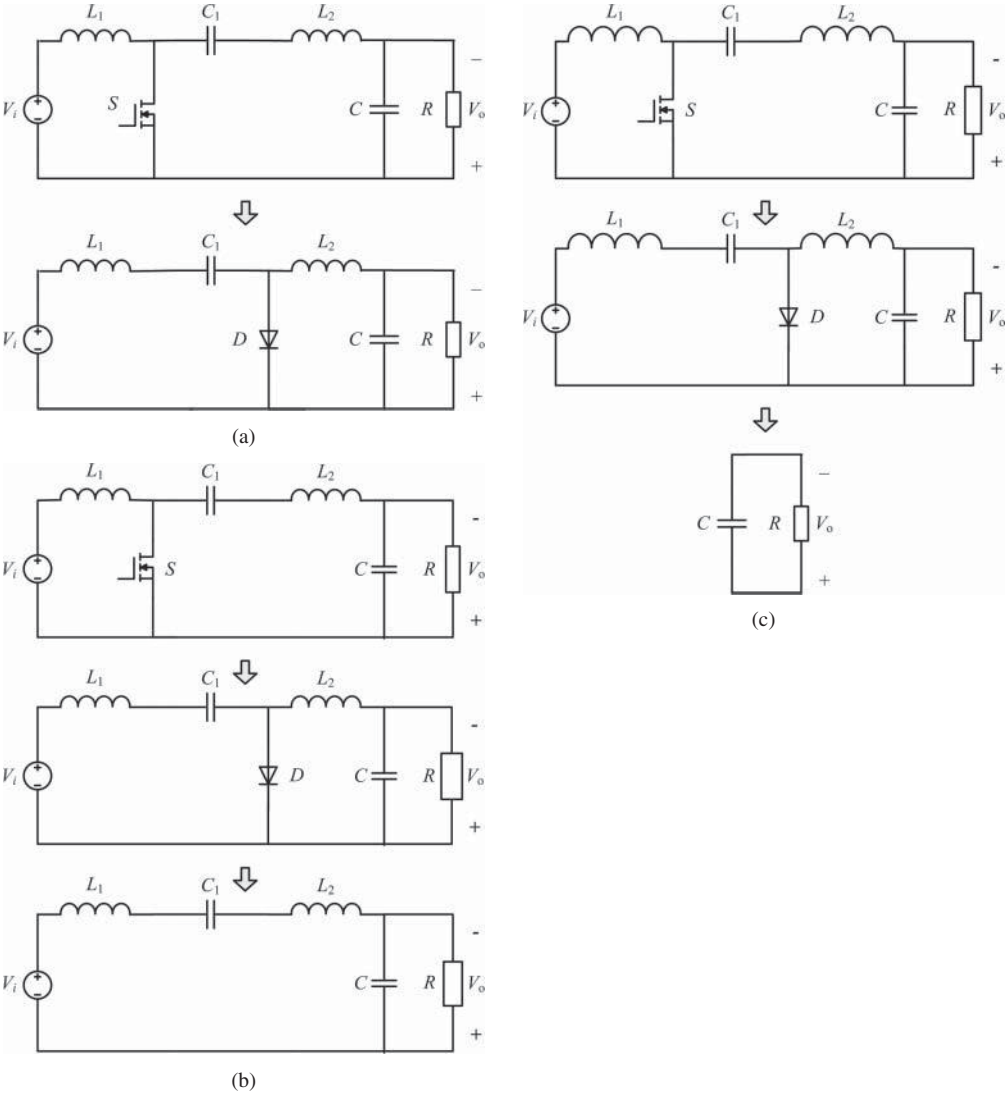


Figure 7.9 Equivalent circuits of operating modes of the Cúk converter: (a) normal operating mode; (b) sneak circuit operating mode 1; and (c) sneak circuit operating mode 2

If merging G_1 and $G_2 \oplus G_3$ into a connecting piece $G_1 \cup G_2 \oplus G_3$ and considering the current direction from the point of view of the connecting piece, as long as the current of switch S (i_S) satisfies $i_S = i_{L1} + i_{L2} > 0$, then one of the inductor currents can be reversed, since the inductor current can flow bi-directionally, but both inductor currents i_{L1} and i_{L2} cannot be negative simultaneously. Thus, another two kinds of current direction of normal operating unit 1 can be derived, such as the current

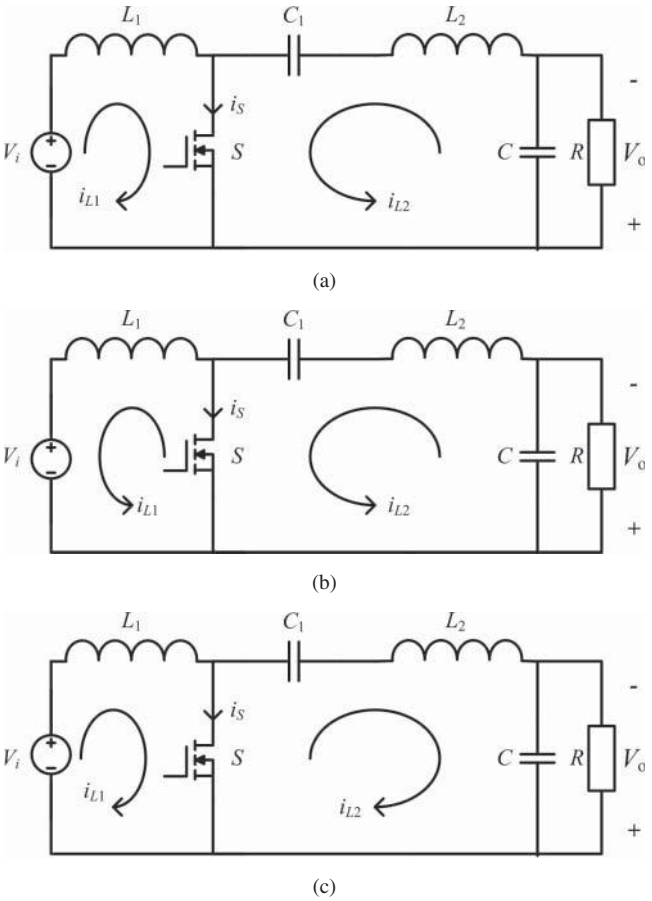


Figure 7.10 Current directions of normal operating unit 1 of the Cúk converter when $i_S = i_{L1} + i_{L2} > 0$: (a) current direction 1, $i_{L1} > 0$ and $i_{L2} > 0$; (b) current direction 2, $i_{L1} < 0$ and $i_{L2} > 0$; and (c) current direction 3, $i_{L1} > 0$ and $i_{L2} < 0$

direction 2 ($i_{L1} < 0$ and $i_{L2} > 0$) shown in Figure 7.10b and the current direction 3 ($i_{L1} > 0$ and $i_{L2} < 0$) shown in Figure 7.10c.

Similarly, the mesh current direction of normal operating unit 2 can be obtained, which shows that there are three kinds of current direction if the diode current i_D satisfying $i_D = i_{L1} + i_{L2} > 0$. As shown in Figure 7.11, the current direction 1 in Figure 7.11a is the normal current direction of the Cúk converter ($i_{L1} > 0$ and $i_{L2} > 0$), and the other two current directions are the current direction 2 ($i_{L1} < 0$ and $i_{L2} > 0$) in Figure 7.11b and the current direction 3 ($i_{L1} > 0$ and $i_{L2} < 0$) in Figure 7.11c.

The sneak operating unit 1 in Figure 7.7a contains two independent meshes $G_1 \oplus G_2 \oplus G_3$ and G_4. Since there is no uni-directional component in mesh

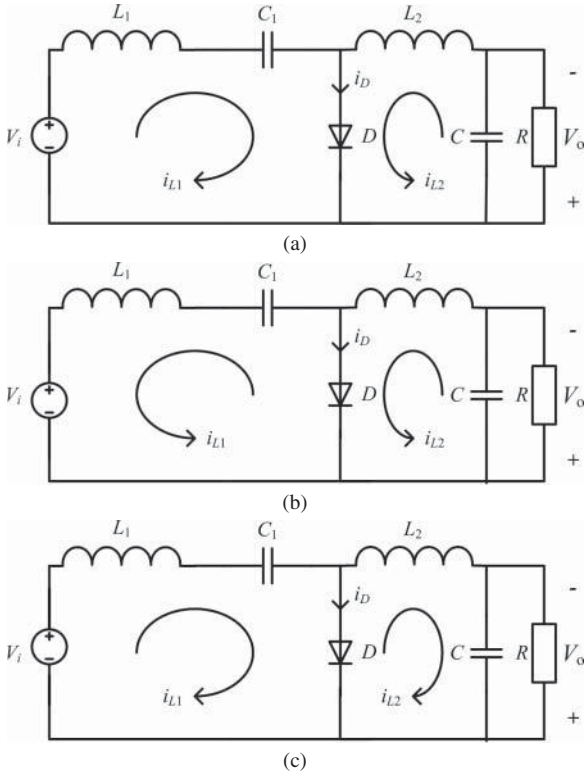
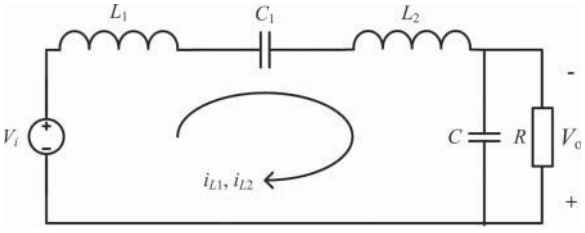


Figure 7.11 Current directions of normal operating unit 2 of the Cúk converter when $i_D = i_{L1} + i_{L2} > 0$: (a) current direction 1, $i_{L1} > 0$ and $i_{L2} > 0$; (b) current direction 2, $i_{L1} < 0$ and $i_{L2} > 0$; and (c) current direction 3, $i_{L1} > 0$ and $i_{L2} < 0$

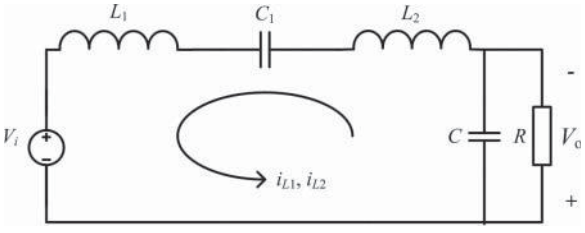
$G_1 \oplus G_2 \oplus G_3$, the mesh current can flow bi-directionally, as shown in Figure 7.12a,b. It is noted that inductor L_1 and inductor L_2 are connected in series, and $i_{L1} + i_{L2} = 0$ should be satisfied when the Cúk converter operates in sneak operating unit 1.

For the sneak operating unit 2 in Figure 7.7b, as there is only one independent mesh G_4, as described above, there is no need to classify its current direction. When the Cúk converter operates in sneak operating unit 2, both of the induction currents are zero, that is, $i_{L1} = i_{L2} = 0$.

As shown in Figures 7.10–7.12, the current direction in some operating units of the Cúk converter is not unique, so the current direction should be considered when combining the operating units in operating mode. As we know, the inductor current cannot change suddenly, so the direction of the inductor current will remain unchanged during the switching moment between two operating units. Therefore, the possible current directions in each operating mode of the Cúk converter are listed in Table 7.4.



(a)



(b)

Figure 7.12 Current directions of sneak operating unit 1 of the Cúk converter when $i_{L1} + i_{L2} = 0$: (a) current direction 1, $i_{L1} > 0$ and $i_{L2} < 0$; and (b) current direction 2, $i_{L1} < 0$ and $i_{L2} > 0$

From Table 7.4, it is found that if the current direction of the normal operating unit is different from the normal current direction defined in Figures 7.10a and 7.11a, according to the definition of sneak circuit operating mode considering the changing of current direction, even the operating mode with only normal operating units should be considered as sneak circuit phenomena. Therefore, besides operating mode No. 1 in Table 7.4 belonging to normal operation, the other five operating modes are all sneak circuit phenomena.

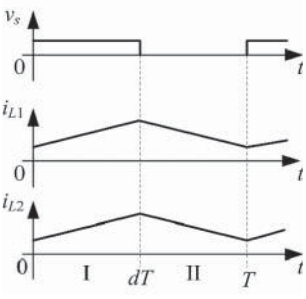
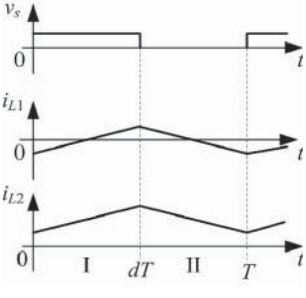
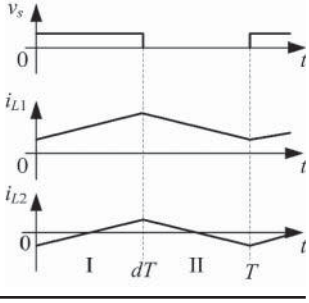
7.5 Results of Sneak Circuit Mode Analysis Method on Cúk Converter

According to the inductor current direction in different operating modes of the Cúk converter shown in Table 7.4, typical waveforms of the inductor current in every operating mode are gathered in Table 7.5, which are completely consistent with the normal operating phenomenon and five kinds of sneak circuit phenomena of the Cúk converter in Section 3.6.2. It is obvious that the feasibility of the sneak circuit mode analysis method presented in this chapter has been verified.

Table 7.4 Inductor current directions in the Cúk converter

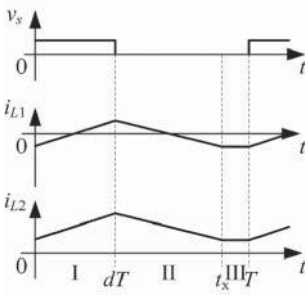
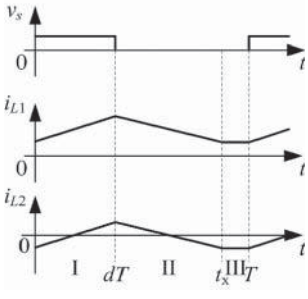
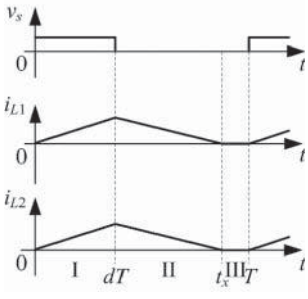
Operating mode	Inductor current direction						Operating mode No.
	Stage I		Stage II		Stage III		
Normal operating mode or Figure 7.9a	Normal operating unit 1 or Figure 7.6a	$i_{L1} > 0, i_{L2} > 0$ or Figure 7.10a	Normal operating unit 2 or Figure 7.6b	$i_{L1} > 0, i_{L2} > 0$ or Figure 7.11a	–		1
		$i_{L2} > 0$ or Figure 7.10a,b		$i_{L2} > 0$ or Figure 7.11a,b	–		2
		$i_{L1} > 0$ or Figure 7.10a,c		$i_{L1} > 0$ or Figure 7.11a,c	–		3
Sneak circuit operating mode 1 or Figure 7.9b	Normal operating unit 1 or Figure 7.6a	$i_{L2} > 0$ or Figure 7.10a,b	Normal operating unit 2 or Figure 7.6b	$i_{L2} > 0$ or Figure 7.11a,b	Sneak operating unit 1 or Figure 7.7a	$i_{L1} < 0$, $i_{L2} > 0$, and $i_{L1} + i_{L2} = 0$ or Figure 7.12a	4
		$i_{L1} > 0$ or Figure 7.10a,c		$i_{L1} > 0$ or Figure 7.11a,c		$i_{L1} > 0$, $i_{L2} < 0$, and $i_{L1} + i_{L2} = 0$ or Figure 7.12b	5
Sneak circuit operating mode 2 or Figure 7.9c	Normal operating unit 1 or Figure 7.6a	$i_{L1} > 0, i_{L2} > 0$ or Figure 7.10a	Normal operating unit 2 or Figure 7.6b	$i_{L1} > 0, i_{L2} > 0$ or Figure 7.11a	Sneak operating unit 2 or Figure 7.7b	$i_{L1} = i_{L2} = 0$	6

Table 7.5 Sneak circuit operating modes of the Cúk converter

Stage			Phenomenon	Typical waveforms
I	II	III		
Normal operating unit 1 or Figure 7.6a	Normal operating unit 2 or Figure 7.6b	–	Normal operating condition (CCM)	
			Sneak circuit phenomenon I	
			Sneak circuit phenomenon II	

(*continued overleaf*)

Table 7.5 (*continued*)

Stage			Phenomenon	Typical waveforms
I	II	III		
Normal operating unit 1 or Figure 7.6a	Normal operating unit 2 or Figure 7.6b	Sneak operating unit 1 or Figure 7.7a	Sneak circuit phenomenon III	
			Sneak circuit phenomenon IV	
Normal operating unit 1 or Figure 7.6a	Normal operating unit 2 or Figure 7.6b	Sneak operating unit 2 or Figure 7.7b	Sneak circuit phenomenon V (DCM)	

CCM, continuous conduction mode and DCM, discontinuous conduction mode.

7.6 Summary

This chapter converts the power electronic converter to a graph, searches for the effective operating unit or actual sub-circuit of the power electronic converter by using the mesh combination algorithms of graph theory, obtains all operating modes of the power electronic converter by taking the on-off control strategy into account, and

derives the typical waveforms in sneak circuit operating modes by considering the current direction.

The sneak circuit mode analysis method presented in this chapter is a systematic method to discover the sneak circuit phenomena in power electronic converters. It is an effective complement to the sneak circuit path analysis methods in Chapter 6. The proposed sneak circuit mode method can realize sneak circuit analysis of power electronic converters accurately, and can be extended to all kinds of power electronic converters in the future.

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Part Three

Elimination and Application of Sneak Circuits

8

Elimination of Sneak Circuits in Power Electronic Converters

8.1 Introduction

Based on the definition of a sneak circuit, the sneak circuit of a power electronic converter is a current path hidden in that converter, which will appear when a specific parameter condition is satisfied. As a result, the operating stages increase or change and the energy balance under normal operating mode is destroyed, which will lead to changes of the converter's characteristics and so the desired performance of the converter cannot be achieved. Thus, sneak circuits should be eliminated in the power electronic converter.

Apparently, the emergence of sneak circuits should satisfy two conditions. Firstly, there must be potential paths existing in the power electronic converter; if not, the sneak circuit phenomenon will not occur. Secondly, sneak circuits will appear on specific operating parameters, but if the converter parameters are designed appropriately or the converter's operating conditions are set within normal ranges, then sneak circuit phenomenon cannot occur. Chapters 2–5 demonstrated the sneak circuit phenomena in some typical power electronic converters, and proved the correctness of the above sneak circuit conditions. Therefore, in order to eliminate sneak circuits in power electronic converters, two methods can be used based on the conditions under which sneak circuit appear. One is parameter design, which can avoid the emergence of a sneak circuit through reasonable design and make the converter work in the normal operating mode. The other is topology improvement, which can cut off the sneak circuit paths by changing the converter topology based on the characteristics of the sneak circuit path.

Although the second method can eliminate the hazard of sneak circuits thoroughly, it may bring about new sneak circuit paths or influence the performance of converter after changing its topology. So selecting the suitable method to eliminate sneak

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circuits should take into consideration the practical situation of converter. The method of parameter design can be selected for the converter which has the identified sneak circuit condition, but for the converter which does not have clear sneak circuit conditions, the method of topology improvement will be a better choice.

This chapter will demonstrate how to eliminate sneak circuits by taking the (RSC) converters, Z-source inverters, and Buck (ZVT) (PWM) converter as examples, which can be used as a reference for other power electronic converters.

8.2 Sneak Circuit Elimination for RSC Converters

8.2.1 Parameter Design Principle

Chapter 2 introduced the normal operating mode and sneak circuit operating mode of RSC converters in detail and derived the sneak circuit conditions. The characteristics of basic RSC converters under different modes are summarized in Table 8.1.

The expressions of output voltage, inductor current stress, and capacitor voltage stress illustrated in Table 8.1 can be used to calculate their specific values after the converter parameters are known. By considering the operating conditions of basic RSC converters, the results of operating characteristics under different operating modes are listed in Table 8.2. Compared with the normal operating mode, the sneak circuit mode leads to a lower output voltage and increases the current and voltage stresses of the components, which will adversely influence the converter.

For high-order step-down and step-up RSC converters, their sneak circuit conditions are concluded in Equations 2.67 and 2.88 respectively, and the sneak circuit influence is similar to that of basic RSC converters. As the RSC converters have identified sneak circuit conditions, reasonable parameters can be selected or operating conditions can be restricted to ensure the RSC converter operates under normal operating mode and avoids the emergence of a sneak circuit.

Table 8.1 Characteristics of basic RSC converters under different operating conditions

RSC converter type	Normal operating mode			Sneak circuit mode		
	V_o	$I_{L\max}$	$V_{C\max}$	V_o	$I_{L\max}$	$V_{C\max}$
Step-down	$\frac{V_i}{2}$	$\frac{V_i}{8R_LC_rf_sZ_r}$	$\frac{V_i}{2}\left(1+\frac{1}{4R_LC_rf_s}\right)$	$2R_LC_rf_sV_i$	$\frac{V_i}{2Z_r}$	$V_i\left(\frac{3}{2}-2R_LC_rf_s\right)$
Step-up	$2V_i$	$\frac{V_i}{R_LC_rf_sZ_r}$	$V_i\left(1+\frac{1}{R_LC_rf_s}\right)$	$2R_LC_rf_sV_i$	$\frac{V_i}{Z_r}$	$2V_i$
Inverting	$-V_i$	$\frac{V_i}{2R_LC_rf_sZ_r}$	$V_i\left(1+\frac{1}{2R_LC_rf_s}\right)$	$-2R_LC_rf_sV_i$	$\frac{V_i}{Z_r}$	$2V_i$

Table 8.2 Comparison of operating conditions and characteristics of basic RSC converters

RSC converter	Mode	Condition	V_o	$I_{L\max}$	$V_{C\max}$
Step-down	Normal	$R_L C_r f_s \geq \frac{1}{4}$	$\frac{V_i}{2}$	$\leq \frac{V_i}{2Z_r}$	$\leq V_i$
	Sneak circuit	$R_L C_r f_s < \frac{1}{4}$	$< \frac{V_i}{2}$	$\frac{V_i}{2Z_r}$	$> V_i$
Step-up	Normal	$R_L C_r f_s \geq 1$	$2V_i$	$\leq \frac{V_i}{Z_r}$	$\leq 2V_i$
	Sneak circuit	$R_L C_r f_s < 1$	$< 2V_i$	$\frac{V_i}{Z_r}$	$2V_i$
Inverting	Normal	$R_L C_r f_s \geq \frac{1}{2}$	$-V_i$	$\leq \frac{V_i}{Z_r}$	$\leq 2V_i$
	Sneak circuit	$R_L C_r f_s < \frac{1}{2}$	$< -V_i$	$\frac{V_i}{Z_r}$	$2V_i$

8.2.2 Topology Improvement Scheme

Based on the sneak circuit analysis of various RSC converters described in Chapter 2, the common feature of the sneak circuit paths in RSC converters is that the parasitic diode (or anti-parallel diode) of the power switch conducts and then offers a reversed current path for the resonant inductor current. The sneak circuit path can be eliminated by cutting off the reversed current path formed by the parasitic diode. It is found that the sneak circuit path is different from the normal operating paths in RSC converters, thus a diode can be added in series with the power switch to ensure that the resonant inductor current cannot pass through the power switch in the reverse direction. Figure 8.1 illustrates the power switch structure before and after improvement.

By replacing the original power switch in Figure 8.1a by the improved power switch in Figure 8.1b, an improved RSC converter can obtained, as in Figure 8.2. Compared

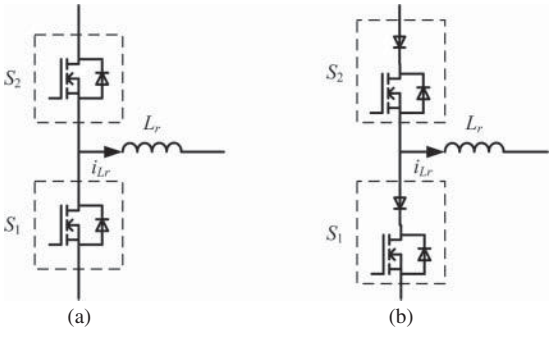
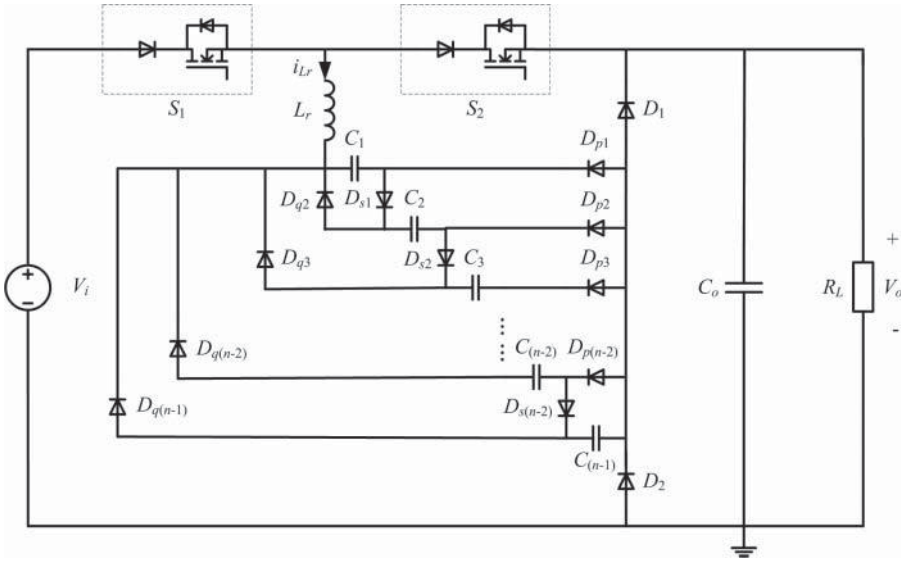
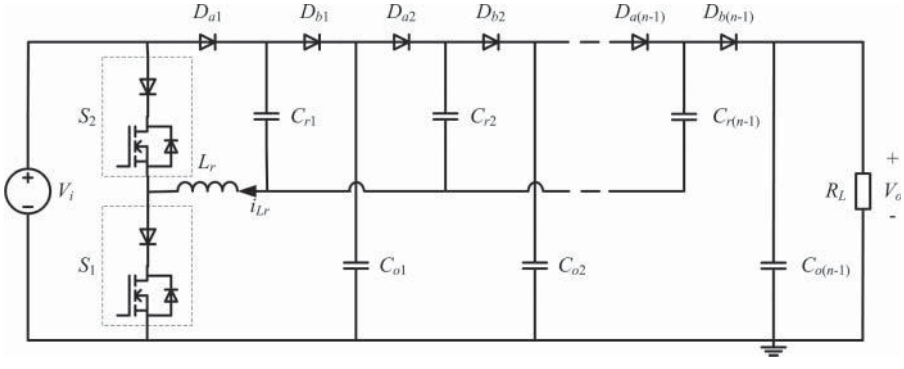


Figure 8.1 Structure of the power switch in the RSC converters: (a) before improvement; and (b) after improvement



(a)

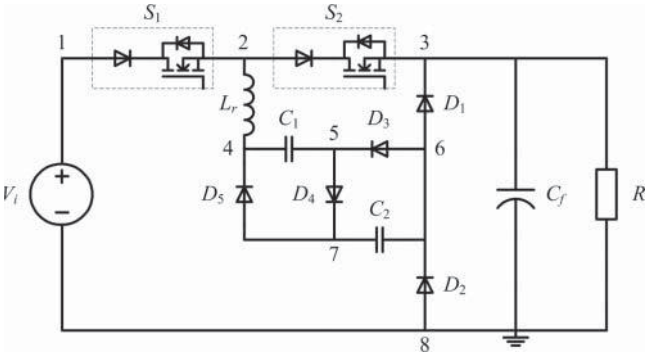


(b)

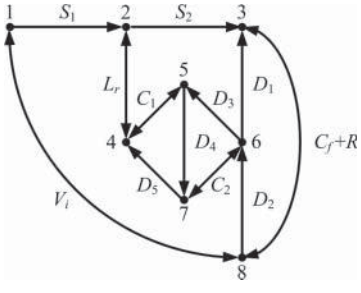
Figure 8.2 The topology of improved RSC converters: (a) high-order step-down; and (b) high-order step-up

with the traditional high-order RSC converters in Figures 2.19 and 2.27, two diodes are added, which ensure that the improved RSC converter operate under normal operating mode, even if the converter parameters satisfy the sneak circuit conditions, but the hardware cost and the power loss will increase. Furthermore, the improved topology needs to be evaluated to ensure that all the previous sneak circuit paths have been cut off and no new sneak circuit will occur.

A three-order step-down RSC converter and a three-order step-up RSC converter are used to demonstrate the feasibility of the above topology improvement scheme, by using the generalized connection matrix [1, 2].



(a)



(b)

Figure 8.3 The improved three-order step-down RSC converter: (a) circuit diagram; and (b) directed graph

8.2.3 Examples

8.2.3.1 The Improved Three-order Step-Down RSC Converter

According to Figure 8.2a, the circuit diagram of the improved three-order step-down RSC converter is illustrated in Figure 8.3a, and Figure 8.3b is the directed graph of the improved converter.

Based on the definition of a generalized connection matrix of a power electronic converter, the generalized connection matrix of Figure 8.3b is

$$\mathbf{C}' = \begin{bmatrix} 1 & S_1 & 0 & 0 & 0 & 0 & 0 & V_i \\ 0 & 1 & S_2 & L_r & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & C_f + R \\ 0 & L_r & 0 & 1 & C_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_1 & 1 & 0 & D_4 & 0 \\ 0 & 0 & D_1 & 0 & D_3 & 1 & C_2 & 0 \\ 0 & 0 & 0 & D_5 & 0 & C_2 & 1 & 0 \\ V_i & 0 & C_f + R & 0 & 0 & D_2 & 0 & 1 \end{bmatrix} \tag{8.1}$$

The switching function of Equation 8.1 can be calculated as

$$\begin{aligned} F = {} & D_4 * D_5 * C_1 + C_f * S_2 * S_1 * V_i + R * S_2 * S_1 * V_i + C_f * R + D_2 * D_5 * \\ & C_2 * S_2 * L_r * C_f + C_2 * D_3 * D_4 + D_2 * D_1 * C_f + D_2 * D_1 * R + D_4 * \\ & D_5 * C_1 * C_f * R + D_4 * D_5 * C_1 * C_f * S_2 * S_1 * V_i + D_4 * D_5 * C_1 * R * \\ & S_2 * S_1 * V_i + C_2 * D_3 * D_4 * C_f * R + C_2 * D_3 * D_4 * C_f * S_2 * S_1 * V_i \\ & + C_2 * D_3 * D_4 * R * S_2 * S_1 * V_i + D_2 * D_3 * C_1 * S_2 * L_r * C_f + D_2 * \\ & D_3 * C_1 * S_2 * L_r * R + D_2 * D_5 * C_2 * S_2 * L_r * R + D_2 * D_5 * D_3 * D_4 * \\ & S_2 * L_r * C_f + D_2 * D_5 * D_3 * D_4 * S_2 * L_r * R + D_2 * D_5 * D_1 * C_f * D_4 * \\ & C_1 + D_2 * D_5 * D_1 * R * D_4 * C_1 + C_2 * L_r * S_1 * V_i * D_1 * C_f * D_4 * \\ & C_1 + C_2 * L_r * S_1 * V_i * D_1 * R * D_4 * C_1 \end{aligned} \tag{8.2}$$

According to the operating principle of the high-order step-down RSC converter, the invalid current loops in Equation 8.2 can be deleted, which include both S_1 and S_2, both D_1 and D_2, both D_4 and D_5, and both D_3 and D_4 turning on simultaneously. Then, the remaining effective current loops are expressed by

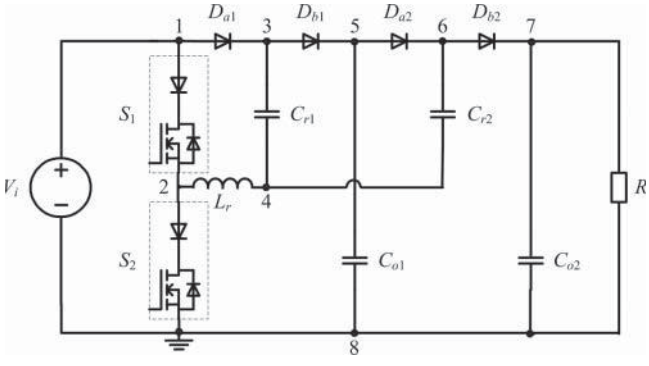
$$\begin{aligned} F_a = {} & D_2 * D_5 * C_2 * S_2 * L_r * C_f + D_2 * D_5 * C_2 * S_2 * L_r * R + D_2 * D_3 * \\ & C_1 * S_2 * L_r * C_f + D_2 * D_3 * C_1 * S_2 * L_r * R + C_2 * L_r * S_1 V_i * \\ & D_1 * C_f * D_4 * C_1 + C_2 * L_r ** S_1 * V_i * D_1 * R * D_4 * C_1 + C_f * R \end{aligned} \tag{8.3}$$

It is found that the current loops in Equation 8.3 are the same as those in which C_1 and C_2 are charging in series and C_1 and C_2 are discharging in parallel, therefore, there is no sneak circuit path in the improved three-order step-down RSC converter and the converter can operate normally under any conditions.

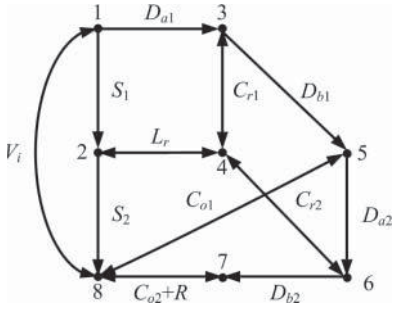
8.2.3.2 The Improved Three-order Step-Up RSC Converter

Similarly, the improved three-order step-up RSC converter and its directed graph are illustrated in Figure 8.4a,b respectively. The corresponding generalized connection matrix of Figure 8.4b is defined by

$$C' = \begin{bmatrix} 1 & S_1 & D_{a1} & 0 & 0 & 0 & 0 & V_i \\ 0 & 1 & 0 & L_r & 0 & 0 & 0 & S_2 \\ 0 & 0 & 1 & C_{r1} & D_{b1} & 0 & 0 & 0 \\ 0 & L_r & C_{r1} & 1 & 0 & C_{r2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & D_{a2} & 0 & C_{o1} \\ 0 & 0 & 0 & C_{r2} & 0 & 1 & D_{b2} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & C_{o2} + R \\ V_i & 0 & 0 & 0 & C_{o1} & 0 & C_{o2} + R & 1 \end{bmatrix} \tag{8.4}$$



(a)



(b)

Figure 8.4 The improved three-order step-up RSC converter: (a) circuit diagram; and (b) directed graph

and the result of switching function is

$$
\begin{aligned}
F = {} & C_{o1} * D_{b1} * D_{a1} * V_i + C_{o2} * R + L_r * C_{r2} * C_{o2} * D_{b2} * S_1 * V_i + L_r * C_{r2} * \\
& R * D_{b2} * S_1 * V_i + L_r * C_{o1} * D_{b1} * C_{r1} * S_1 * V_i + C_{r2} * C_{o2} * D_{b2} * C_{r1} * \\
& D_{a1} * V_i + C_{r2} * R * D_{b2} * C_{r1} * D_{a1} * V_i + C_{r2} * D_{a2} * D_{b1} * C_{r1} * C_{o2} * R \\
& + D_{a2} * C_{o1} * D_{b2} * C_{o2} + D_{a2} * C_{o1} * D_{b2} * R + L_r * C_{r2} * D_{a2} * C_{o1} * S_2 \\
& + D_{a2} * D_{b1} * D_{a1} * V_i * D_{b2} * C_{o2} + D_{a2} * D_{b1} * D_{a1} * V_i * D_{b2} * R + L_r * \\
& C_{r2} * D_{a2} * D_{b1} * D_{a1} * V_i * S_2 + C_{r1} * D_{a1} * V_i * L_r * S_2 + D_{a2} * D_{b1} * C_{r1} \\
& * S_1 * V_i * D_{b2} * L_r * C_{o2} + D_{a2} * D_{b1} * C_{r1} * S_1 * V_i * D_{b2} * L_r * R + C_{r2} \\
& * D_{a2} * D_{b1} * C_{r1} * S_1 * V_i * S_2 + S_1 * V_i * S_2 + C_{r2} * D_{a2} * D_{b1} * C_{r1}
\end{aligned}
\tag{8.5}
$$

According to the operating principle of a high-order step-up RSC converter, the invalid current loops that include S_1S_2, $D_{a1}D_{b1}$, $D_{b1}D_{a2}$, $D_{a1}D_{b2}$, $D_{a2}D_{b2}$, or $D_{a1}D_{b2}$

should be deleted, then the effective current loops are concluded by

$$F_a = \mathrm{Co2} * \mathrm{R} + \mathrm{Lr} * \mathrm{Cr2} * \mathrm{Co2} * \mathrm{Db2} * \mathrm{S1} * \mathrm{Vi} + \mathrm{Lr} * \mathrm{Cr2} * \mathrm{R} * \mathrm{Db2} * \mathrm{S1} * \mathrm{Vi} + \mathrm{Lr} * \mathrm{Co1} * \mathrm{Db1} * \mathrm{Cr1} * \mathrm{S1} * \mathrm{Vi} + \mathrm{Lr} * \mathrm{Cr2} * \mathrm{Da2} * \mathrm{Co1} * \mathrm{S2} + \mathrm{Cr1} * \mathrm{Da1} * \mathrm{Vi} * \mathrm{Lr} * \mathrm{S2} \quad (8.6)$$

Compared with the effective current loops of the original three-order step-up RSC converter in Section 6.4.3, the terms in Equation 8.6, that is, all of the current loops existing in the improved three-order step-up RSC converter belong to those under normal operating mode, which proves that there is no sneak circuit path in the improved three-order step-up RSC converter. Thus, the scheme of adding a diode in series with the power switch makes it feasible to remove the sneak circuit paths from RSC converters completely.

8.3 Sneak Circuit Elimination for Z-Source Inverter

8.3.1 Restricted Operating Conditions

It is known from the sneak circuit analysis of Z-source inverter described in Section 5.2.2, that if the converter parameters or operating conditions, such as load impedance |Z|, inductance L, modulation ratio M, step-up factor B, duty cycle of shoot-through zero state D, switching frequency f_s, and so on, are selected to satisfy the following equation, then the sneak circuit phenomenon in which the diode current becomes discontinuous during the non-zero vector will appear [3]:

$$Lf_sM\left(\frac{3}{2}MB\cos\phi - 1\right) < D(D-1)|Z| \text{ or } \frac{3}{2}MB\cos\phi - 1 \le 0 \quad (8.7)$$

Therefore, the Z-source inverter has a specific sneak circuit condition, whereby restricting the operating conditions of a Z-source inverter to make Equation 8.7 invalid, means that the sneak circuit phenomenon of a Z-source inverter will not appear.

8.3.2 Topology Improvement

If diode D is off when the Z-source inverter operates in the non-zero vector, the DC voltage source V_{DC} will not connect to the Z impedance network, which means that the sneak circuit phenomenon occurs. Therefore, if there is a circuit path that connects the DC voltage source V_{DC} with the Z impedance network during the non-zero vector, the sneak circuit phenomenon will disappear.

As the three-phase inverter in the Z-source inverter has six controllable switches and nine switching states, it is impossible to describe various switching states of a Z-source inverter by the adjacent matrix or generalized adjacency matrix. However,

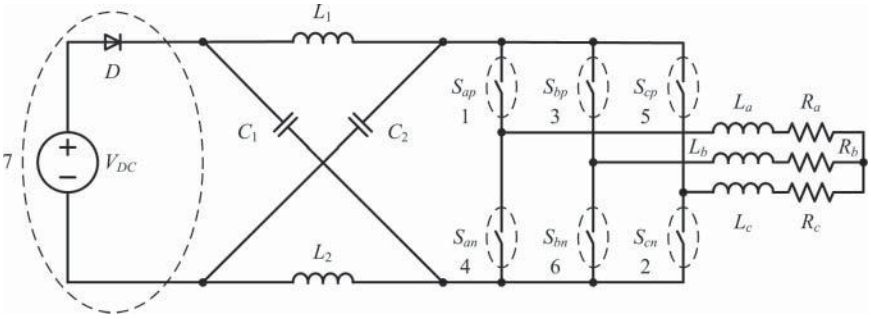


Figure 8.5 Switching branch definition of the Z-source inverter

if the switch is represented by a switching branch, in which "1" is on behalf of the on-state and "0" is on behalf of the off-state, then all kinds of switching states in the Z-source inverter can be described clearly by the switching Boolean matrix. The definition of the switching branches in the Z-source inverter is shown in Figure 8.5, where only the switching branches are defined, because the impedance network and the load belong to the non-switching branches, which are continuously in the on-state. In Figure 8.5, switching branches 1–6 are numbered according to the conducting order of the six bridges in the three-phase inverter; in addition, diode D and V_{DC} are defined as the no. 7 switching branch.

According to three kinds of normal operating status in the Z-source inverter presented in Section 5.2.1, the normal switching Boolean matrix $\mathbf{B_n}$ can be expressed by

$$\mathbf{B_n} = \begin{array}{c} \begin{matrix} S_{ap} & S_{cn} & S_{bp} & S_{an} & S_{cp} & S_{bn} & D \end{matrix} \\ \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 0 \end{bmatrix} \end{array} \begin{matrix} (1) \\ (2) \\ (3) \\ (4) \\ (5) \\ (6) \\ (7) \\ (8) \\ (9) \end{matrix} \tag{8.8}$$

where row vectors (1) to (6) correspond to six active vectors of normal operating status I, row vectors (7) and (8) correspond to two traditional zero vectors of status II, and row (9) corresponds to the shoot-through zero vector of status III, which is restricted to the case of a three-phase short-circuit at the same time.

Based on the sneak circuit analysis of the Z-source inverter in Section 5.2.2, only the sneak circuit status I′ in Figure 5.5a is available, and diode D will turn off when the diode current i_D or input current decreases to zero during the non-zero vectors.

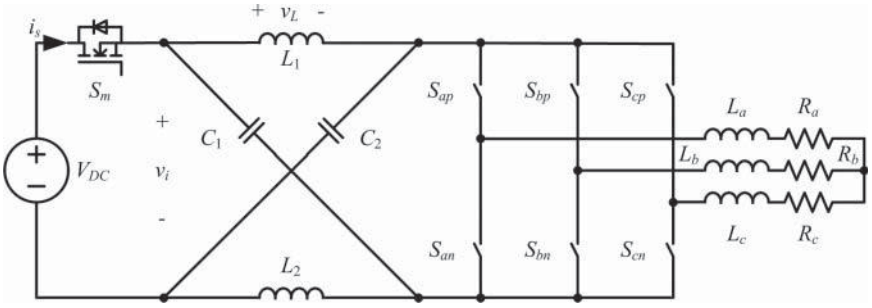


Figure 8.6 The improved Z-source inverter

Therefore, the sneak circuit can be avoided if the voltage source V_{DC} is always connected to the Z-source impedance, except during the shoot-through zero state.

If the diode D is substituted by a fully controlled power switch, which has a reverse conducting property (i.e., Power MOSFET), then the input current or the original diode current i_D can flow in a bi-directional way. Even when the input current decreases to zero and becomes reversed, the switch can provide a backward path for the current by its control signal or anti-parallel diode. Therefore, the improved Z-source inverter with power switch S_m instead of diode D is illustrated in Figure 8.6. We need to design the control method of switch S_m, in which switch S_m must be turned on in the active or traditional zero states, but turned off in the shoot-through zero state.

According to the normal switching Boolean matrix of the Z-source inverter in Equation 8.8, the on-state of switch S_m is defined by

$$b_{i7} = \begin{cases} b_{i1}b_{i2}\overline{b}_{i3}\overline{b}_{i4}\overline{b}_{i5}b_{i6} \\ b_{i1}b_{i2}b_{i3}\overline{b}_{i4}\overline{b}_{i5}\overline{b}_{i6} \\ \overline{b}_{i1}b_{i2}b_{i3}b_{i4}\overline{b}_{i5}\overline{b}_{i6} \\ \overline{b}_{i1}\overline{b}_{i2}b_{i3}b_{i4}b_{i5}\overline{b}_{i6} \\ \overline{b}_{i1}\overline{b}_{i2}\overline{b}_{i3}b_{i4}b_{i5}b_{i6} \\ b_{i1}\overline{b}_{i2}\overline{b}_{i3}\overline{b}_{i4}b_{i5}b_{i6} \\ b_{i1}\overline{b}_{i2}b_{i3}\overline{b}_{i4}b_{i5}\overline{b}_{i6} \\ \overline{b}_{i1}b_{i2}\overline{b}_{i3}b_{i4}\overline{b}_{i5}b_{i6} \end{cases} = 1 \tag{8.9}$$

where $b_{i7} = b_{i1}b_{i2}\overline{b}_{i3}\overline{b}_{i4}\overline{b}_{i5}b_{i6} = 1$ is derived from row vector (1) of the normal switching Boolean matrix $\mathbf{B_n}$, which indicates that switch S_m should be turned on when S_{ap}, S_{bn}, and S_{cn} are on (i.e., $b_{i1} = b_{i2} = b_{i6} = 1$) and S_{an}, S_{bp}, and S_{cp} are off (i.e., $b_{i3} = b_{i4} = b_{i5} = 0$). Similarly, other sub-equations in Equation 8.9 are derived from row vectors (2) to (8) of Equation 8.8. Therefore, Equation 8.9 corresponds to the six active states and two traditional zero states of the Z-source inverter, in which the

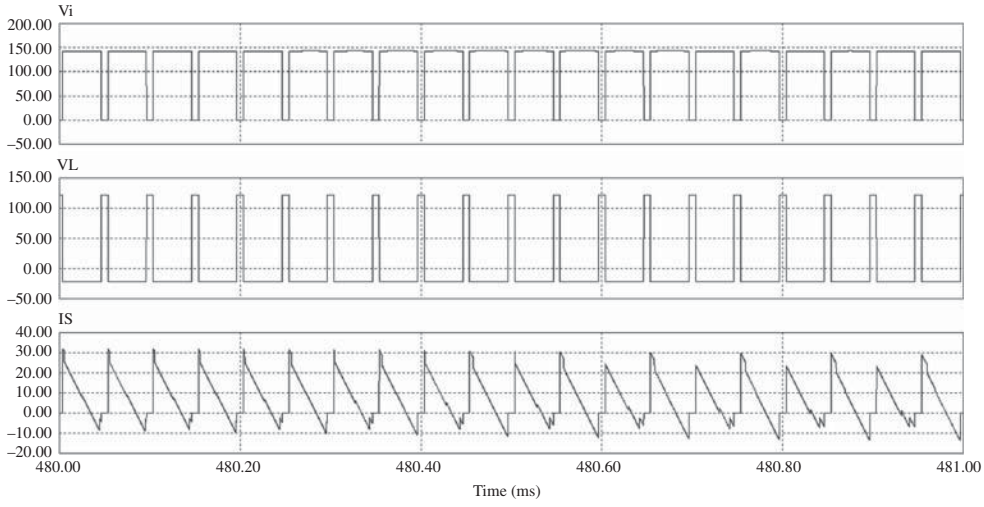


Figure 8.7 Simulation results of the improved Z-source inverter with $Z = 10 + j0.314\Omega$

switch S_m should be turned on. When Equation 8.9 is not satisfied, $b_{i7} = 0$, which means that the switch S_m should be turned off. Therefore, the driving signal of switch S_m can be generated by the driving signals of a three-phase inverter.

When the simulation parameters of the improved Z-source prototype are the same as those in Section 5.2.3, which are the Z-source impedance with $C_1 = C_2 = 100$ μF and $L_1 = L_2 = 50$ μH, the modulation factor $M = 0.9$, the duty cycle of shoot-through zero vector $D = 0.15$, the switching frequency $f_s = 10$ kHz, the output frequency $f = 50$ Hz, the input voltage $V_{DC} = 100$ V, the load $Z = 10 + j0.314\ \Omega$, and the load power factor $\cos\phi = 0.999$, the simulation results of the improved Z-source inverter in PSIM® are the as shown in Figure 8.7. As the sneak circuit condition of the traditional Z-source inverter, that is, Equation 8.7, has been satisfied, the sneak circuit phenomenon will appear in the traditional Z-source inverter, which is shown in Figure 5.8.

Comparing Figure 8.7 with Figure 5.8, it can be seen that there is no distortion in both the inverter input voltage v_i and the inductor voltage v_L, and they are consistent with the normal operating situation illustrated in Figure 5.7. The only difference between Figures 8.7 and 5.7 is that the input current or the switch current i_s are bi-directional. Therefore, the improvement scheme for the Z-source inverter presented in Figure 8.6 has been proven to be reasonable.

8.4 Sneak Circuit Elimination for Buck ZVT PWM Converter

The Buck ZVT PWM converter is a soft-switching converter with superior performance; however, according to the analysis in Section 4.4, sneak circuit phenomenon

will affect the soft-switching performance of the Buck ZVT PWM converter, so the sneak circuit should be eliminated to keep the converter operating under the desired conditions [4].

It is found that the sneak circuit paths of the Buck ZVT PWM converter are caused by the paralleled capacitor of the auxiliary switch, but this capacitor belongs to the parasitic component of the power switch and exists objectively, On the other hand, its capacitance is decided by factors of the switch, such as current, voltage, material, craft, and so on. So it is impossible to eliminate the sneak circuit by restricting the value of parasitic capacitance or removing the parasitic capacitor. Only the method of topology improvement can be adopted in the Buck ZVT PWM converter.

By comparing the sneak circuit phenomenon with the normal operating mode of the Buck ZVT PWM converter in Section 4.4, it is clear that the resonant inductor current flows in reverse when a sneak circuit appears. As a result, the current-circulation loss will increase and the efficiency of the converter will decrease. On the other hand, as the inductor current flows through the anti-paralleled diode of the auxiliary switch, then the reverse recovery characteristic of diode will lead to some distortions. Therefore, the target of topology improvement is to cut off the reverse current path of the resonant current.

8.4.1 Topology Improving Scheme I

According to the above analysis, one of the improving schemes for the Buck ZVT PWM converter is to change the characteristics of the resonant current path from bi-directional to uni-directional by adding a diode D_L in series with the resonant inductor L_r, which ensures that the inductor current flows only in the forward direction.

In order to verify the feasibility of the above scheme, the switching Boolean matrix is used to analyze the effective current paths existing in the improved Buck ZVT PWM converter. Because both the main switch and the auxiliary switch can be regarded as the composite switches with a capacitor and an anti-parallel diode, three different switching branches are required to describe a composite switch. The schematic diagram of an improved Buck ZVT PWM converter I with switching branch definition is illustrated in Figure 8.8.

As there are nine switching branches in the improved Buck ZVT PWM converter I, the corresponding complete switching Boolean matrix will be a $2^9 \times 9$ matrix. Based on the principle of a Buck ZVT PWM converter, the criteria to delete the invalid switching vectors are listed as follows:

1. *Switching constraint criteria*: only one switch branch can be turned on among the three branches in the composite switch. Thus the cases that more than one switching branches in the main composite switch (S, D_s, and C_r) or the auxiliary composite switch (S_1, D_{s1}, and C_{s1}) are turned on simultaneously are invalid.

2. *Short circuit criteria*: the invalid cases include that main composite switch (S, D_s, or C_r) is turned on with the main diode D simultaneously, or auxiliary composite switch (S_1, D_{s1}, or C_{s1}) is turned on with the auxiliary diode D_1 simultaneously.
3. *Conducting direction criteria*: the case that S and S_1, D and D_1, D_L and S, D or D_{s1} are on at the same time belongs to the invalid vector.
4. *Substring criteria*: the case that S_1 (or C_{s1}) and D_1 are off when D_L conducts is invalid.

By removing the invalid row vectors in the complete switching Boolean matrix, the remaining row vectors will be the effective ones, and compose of the valid switching Boolean matrix, that is

$$\mathbf{B_a} = \begin{matrix} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \end{matrix} \begin{matrix} S & D_s & C_r & S_1 & D_{s1} & C_{s1} & D_1 & D & D_L & (L_r) \end{matrix} \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \end{bmatrix} \tag{8.10}$$

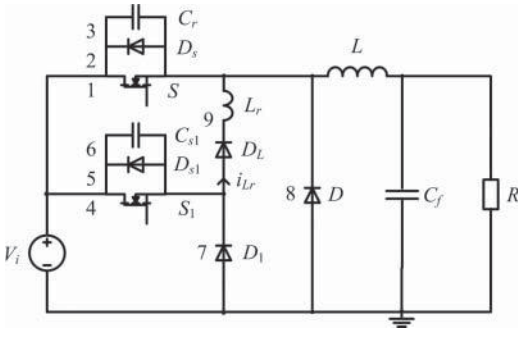


Figure 8.8 Switching branch definition of improved Buck ZVT PWM converter I

According to the definition of switching branches in Figure 8.8, each row vector in the valid switching Boolean matrix $\mathbf{B_a}$ that is Equation 8.10, represents a current path, so there are 14 current paths in the improved Buck ZVT PWM converter I, which are illustrated in Figure 8.9.

Contrasting the 14 current paths in Figure 8.9 with the normal operating mode of the original Buck ZVT PWM converter in Figure 4.24, there is no new current path and reverse inductor current path in the improved Buck ZVT PWM converter I. Therefore, the improving scheme I, which added a diode in series with a resonant inductor, is feasible.

8.4.2 Topology Improving Scheme II

It is known that the purpose of topology improvement for a Buck ZVT PWM converter is to eliminate the opposite inductor current path. According to the schematic diagram of the Buck ZVT PWM converter with a parasitic capacitor in Figure 4.25, the reverse inductor current must pass through D_{s1} or C_{s1} in the auxiliary switch. If the auxiliary switch S_1 becomes uni-directional, then the sneak current path will be cut off. Therefore, another improved Buck ZVT PWM converter, in which a diode D_2 is inserted in series with the auxiliary switch S_1, is shown in Figure 8.10.

In this section, a generalized connection matrix is used to demonstrate the feasibility of the improved Buck ZVT PWM converter II, and corresponding to the directed graph in Figure 8.11, the generalized connection matrix of the improved Buck ZVT PWM converter II is defined by

$$\mathbf{C}' = \begin{bmatrix} 1 & C_r + S & C_{s1} + S_1 & 0 & V_i \\ C_r + D_s & 1 & L_r & L & 0 \\ 0 & L_r & 1 & 0 & 0 \\ 0 & L & 0 & 1 & C_f + R \\ V_i & D & D_1 & C_f + R & 1 \end{bmatrix} \tag{8.11}$$

and the switching function F can be obtained by

$$\begin{aligned} F = {} & \mathrm{C_r} * \mathrm{L_r} * \mathrm{C_{s1}} + \mathrm{C_r} * \mathrm{L_r} * \mathrm{S_1} + \mathrm{D_s} * \mathrm{D} * \mathrm{V_i} + \mathrm{D} * \mathrm{L} * \mathrm{C_f} + \mathrm{D} * \mathrm{L} * \mathrm{R} \\ & + \mathrm{D_s} * \mathrm{L_r} * \mathrm{S_1} + \mathrm{D_s} * \mathrm{L_r} * \mathrm{C_{s1}} + \mathrm{C_r} * \mathrm{D} * \mathrm{V_i} + \mathrm{D_s} * \mathrm{L_r} * \mathrm{C_{s1}} * \mathrm{C_f} * \mathrm{R} \\ & + \mathrm{C_f} * \mathrm{R} + \mathrm{L_r} * \mathrm{D_1} * \mathrm{L} * \mathrm{C_f} + \mathrm{L_r} * \mathrm{D_1} * \mathrm{L} * \mathrm{R} + \mathrm{C_r} * \mathrm{S} * \mathrm{C_f} * \mathrm{R} + \mathrm{C_r} * \\ & \mathrm{L_r} * \mathrm{D_1} * \mathrm{V_i} + \mathrm{C_r} * \mathrm{L} * \mathrm{V_i} * \mathrm{C_f} + \mathrm{C_r} * \mathrm{L} * \mathrm{V_i} * \mathrm{R} + \mathrm{D_s} * \mathrm{C_r} * \mathrm{C_f} * \mathrm{R} \\ & + \mathrm{D_s} * \mathrm{S} * \mathrm{C_f} * \mathrm{R} + \mathrm{D_s} * \mathrm{L_r} * \mathrm{D_1} * \mathrm{V_i} + \mathrm{D_s} * \mathrm{L} * \mathrm{V_i} * \mathrm{C_f} + \mathrm{D_s} * \mathrm{L} * \\ & \mathrm{V_i} * \mathrm{R} + \mathrm{C_r} * \mathrm{S} + \mathrm{D_s} * \mathrm{C_r} + \mathrm{D_s} * \mathrm{S} + \mathrm{C_r} * \mathrm{L_r} * \mathrm{C_{s1}} * \mathrm{C_f} * \mathrm{R} + \mathrm{C_r} * \\ & \mathrm{L_r} * \mathrm{S_1} * \mathrm{C_f} * \mathrm{R} + \mathrm{D_s} * \mathrm{L_r} * \mathrm{S_1} * \mathrm{C_f} * \mathrm{R} + \mathrm{V_i} * \mathrm{L} * \mathrm{S} * \mathrm{C_f} + \mathrm{V_i} * \mathrm{L} * \\ & \mathrm{S} * \mathrm{R} + \mathrm{C_{s1}} * \mathrm{L} * \mathrm{L_r} * \mathrm{V_i} * \mathrm{C_f} + \mathrm{C_{s1}} * \mathrm{L} * \mathrm{L_r} * \mathrm{V_i} * \mathrm{R} + \mathrm{V_i} * \mathrm{L_r} * \mathrm{L} * \\ & \mathrm{S_1} * \mathrm{C_f} + \mathrm{V_i} * \mathrm{L_r} * \mathrm{L} * \mathrm{S_1} * \mathrm{R} \end{aligned} \tag{8.12}$$

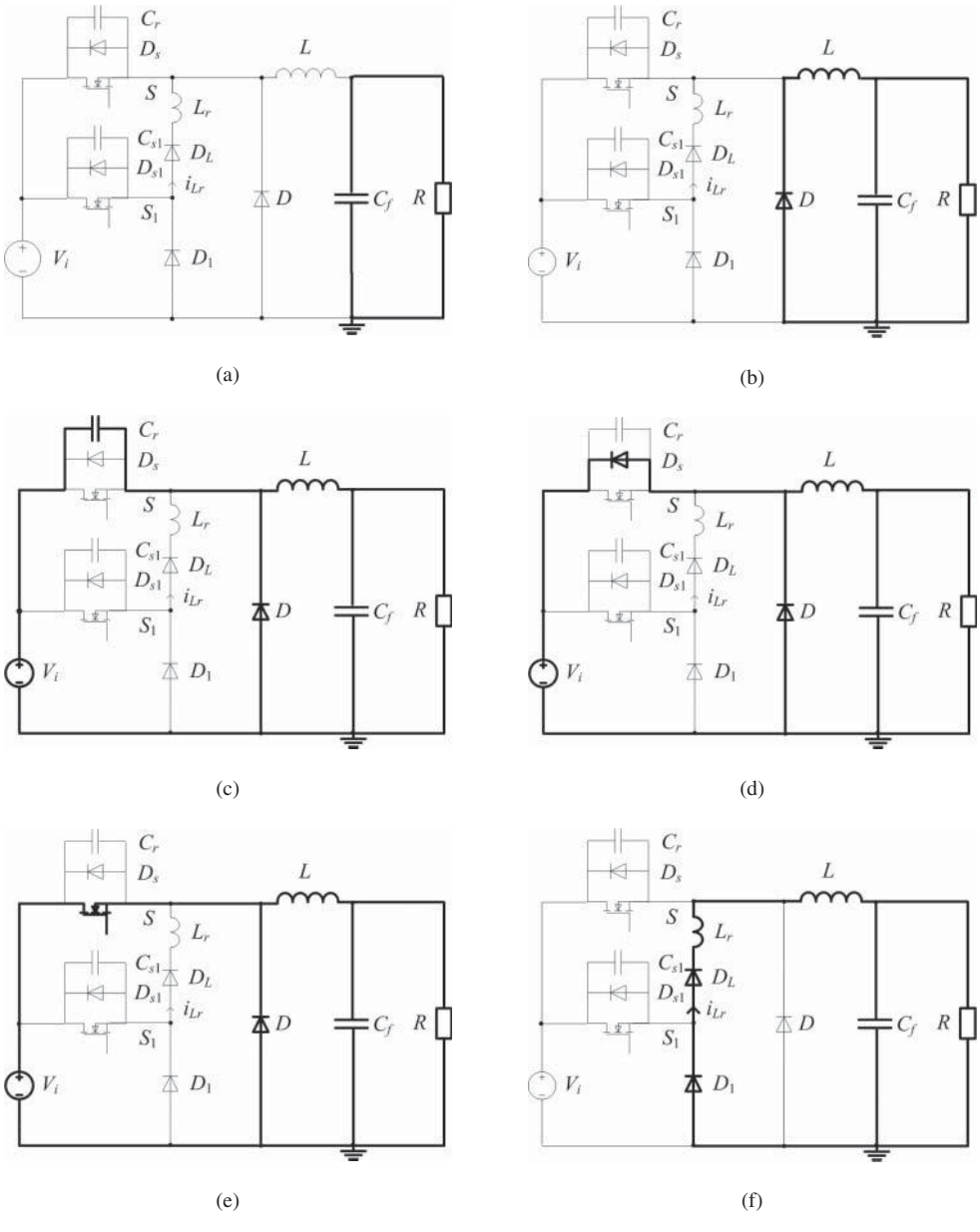


Figure 8.9 Effective current paths in the improved Buck ZVT PWM converter I: (a) [0 0 0 0 0 0 0 0 0 0]; (b) [0 0 0 0 0 0 0 0 1 0]; (c) [0 0 1 0 0 0 0 0 0 0]; (d) [0 1 0 0 0 0 0 0 0 0]; (e) [1 0 0 0 0 0 0 0 0 0]; (f) [0 0 0 0 0 0 1 0 1]; (g) [0 0 0 0 0 1 0 0 1]; (h) [0 0 0 1 0 0 0 0 1]; (i) [0 0 1 0 0 0 1 0 1]; (j) [0 0 1 0 0 1 0 0 1]; (k) [0 0 1 1 0 0 0 0 1]; (l) [0 1 0 0 0 0 1 0 1]; (m) [0 1 0 1 0 0 0 0 1]; and (n) [0 1 0 0 0 1 0 0 1]

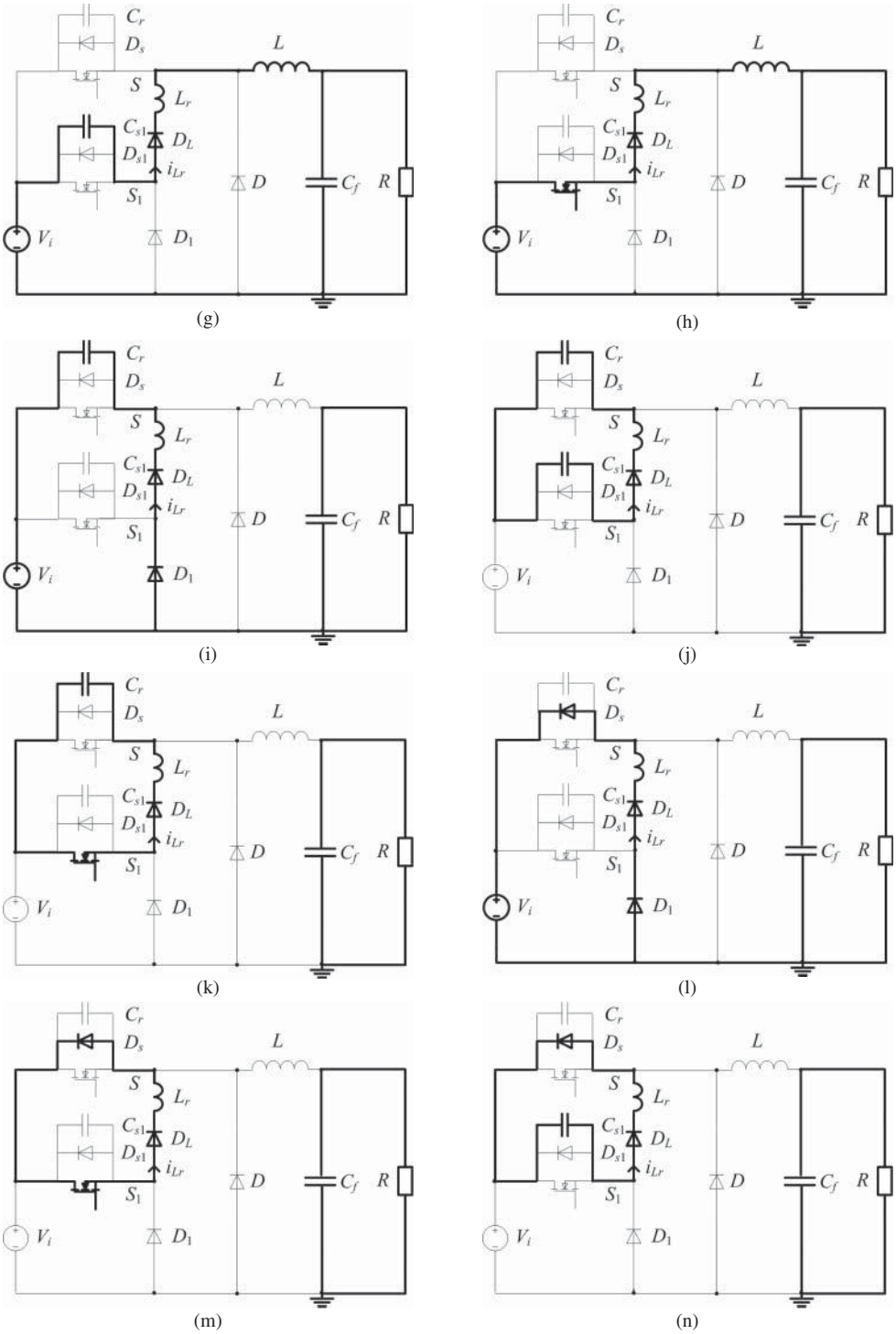


Figure 8.9 (*continued*)

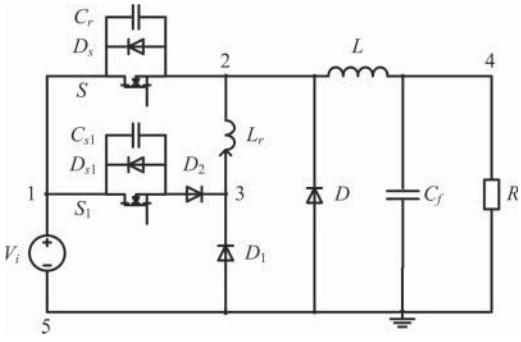


Figure 8.10 The improved Buck ZVT PWM converter II

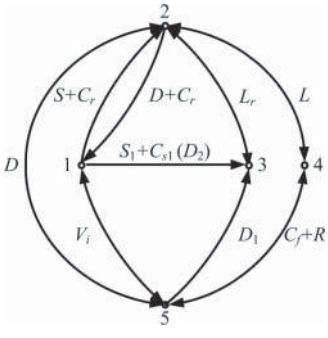


Figure 8.11 Directed graph of the improved Buck ZVT PWM converter II

According to the operating principle of the Buck ZVT PWM converter and circuit theory, the false current loop can be deleted and all effective current loops are contained in the following equation:

$$\begin{aligned} F_a = {} & C_r * L_r * C_{s1} + C_r * L_r * S_1 + D * L * (C_f + R) + D_s * L_r * S_1 \\ & + D_s * L_r * C_{s1} + C_f * R + L_r * D_1 * L * (C_f + R) + C_r * L_r * D_1 * \\ & V_i + C_r * L * V_i * (C_f + R) + D_s * L_r * D_1 * V_i + D_s * L * V_i * \\ & (C_f + R) + V_i * L * S * (C_f + R) + C_{s1} * L * L_r * V_i * (C_f + R) \\ & + V_i * L_r * L * S_1 * (C_f + R) \end{aligned} \tag{8.13}$$

Compared with Figure 8.9, 14 terms in Equation 8.13 are consistent with the effective current paths of the improving scheme I, which demonstrates that the improving scheme II is also feasible.

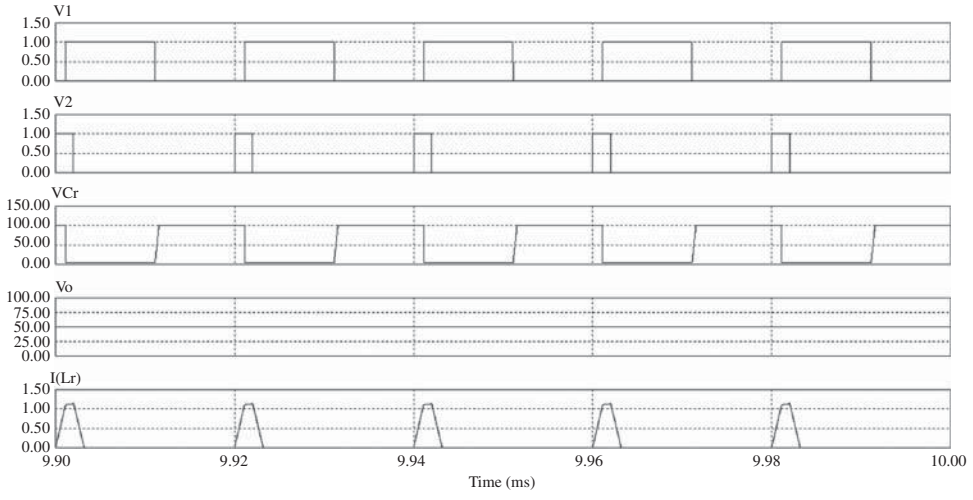


Figure 8.12 Simulation waveforms of the improved Buck ZVT PWM converter

8.4.3 Simulation Verification

The correctness of the above improving schemes will be verified by PSIM®. The simulation parameters of the improved Buck ZVT PWM converter are the same as those in Section 4.4.3, and a fast recovery diode DSE130-10A is selected as the inserted diode. The simulation waveforms are shown in Figure 8.12, which include the driving signal of the main switch S (v_1), the driving signal of the auxiliary switch S_1 (v_2), the resonant capacitor voltage v_{Cr}, the output voltage V_o and the resonant inductor current i_{Lr}. It is found that there is no difference in the simulation results between improving schemes I and II, which means that the effect of sneak circuit elimination of the two schemes are the same.

Compared with the simulation results of the original Buck ZVT PWM converter in Figure 4.28, the resonant inductor current i_{Lr} remains positive, which is consistent with the normal operating mode, and the correctness of topology improvement for the Buck ZVT PWM converter has been verified.

8.5 Summary

In order to eliminate the sneak circuit in power electronics converters, this chapter proposes two methods. One is to restrict the converter parameters or operating conditions in an appropriate range, which do not satisfy sneak circuit condition. The other is to improve the converter's topology in order to cut off the sneak circuit paths completely. The RSC converter, Z-source inverter, and Buck ZVT PWM converter have been selected as examples to demonstrate the sneak circuit elimination in the power electronic converter. It is proven that the proposed methods can eliminate the sneak

circuit effectively and ensure the power electronic converter operates in the designed way or normal operating mode, which can be applied to other power electronic converters with sneak circuit problems.

References

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[4] Hua, G., Leu, C., Jiang, Y. *et al.* (1994) Novel zero-voltage-transition PWM converters. *IEEE Transactions on Power Electronics*, **9** (2), 213–219.

9

Application of Sneak Circuits in Power Electronic Converters

9.1 Introduction

This book has mainly focused on the sneak circuit phenomena in different kinds of power electronics converters, analyzed the undesired effects of sneak circuits on converter performance, then introduced some methods to search for and eliminate sneak circuits. In fact, the existing circuit paths may have a positive effect in a power electronic converter, if they can be taken advantage of, such as those in the synchronous DC-DC converters described in Chapter 5. This chapter will discuss how to improve converter performance, reconstruct converter topology, and design new functions of the converter without increasing the hardware cost, by making use of the sneak circuit. In addition, the sneak circuit path analysis method will be applied to diagnosis faults in the power electronic converter.

9.2 Improvement of Power Electronic Converter Based on Sneak Circuits

In order to improve the converter performance by taking advantage of sneak circuit paths, the main idea is to insert some sneak circuit paths into the normal operating process. Therefore, it is important to choose a useful sneak circuit path and to combine it with the normal operating paths. This section will attempt to improve the soft-switching characteristic of the Boost zero-current-transition (ZCT) pulse width modulation (PWM) converter, by inserting some sneak circuit paths into the operating process of the converter.

9.2.1 Operating Principle of Boost ZCT PWM Converter

The ZCT PWM converter is a soft-switching converter that uses an auxiliary circuit to realize zero-current switching (ZCS). A Boost ZCT PWM converter is shown in

Sneak Circuits of Power Electronic Converters, First Edition. Bo Zhang and Dongyuan Qiu.

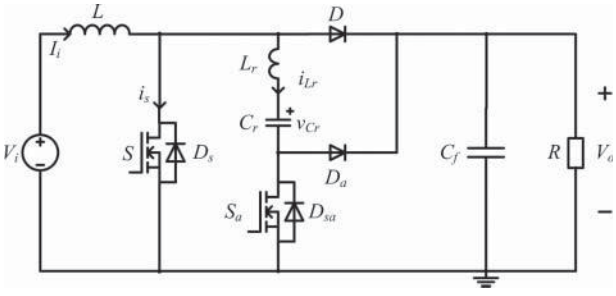


Figure 9.1 Schematic diagram of a Boost ZCT PWM converter

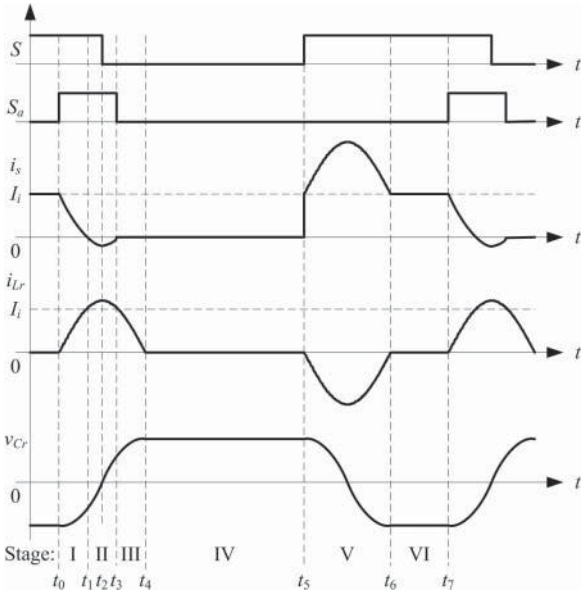


Figure 9.2 Typical waveforms of a Boost ZCT PWM converter

Figure 9.1, and the difference between this converter and the traditional Boost converter in Figure 3.5 is the additional auxiliary circuit, which includes resonant inductor L_r, resonant capacitor C_r, auxiliary switch S_a, and auxiliary freewheeling diode D_a [1]. The auxiliary switch S_a is only turned on before the main switch S is about to be turned off, in order to make the current of the main switch decrease to zero, thus the typical operating waveform of the Boost ZCT PWM converter is as shown in Figure 9.2.

The corresponding process of the Boost ZCT PWM converter can be divided into six operating stages, and their equivalent circuits are given in Figure 9.3. The following

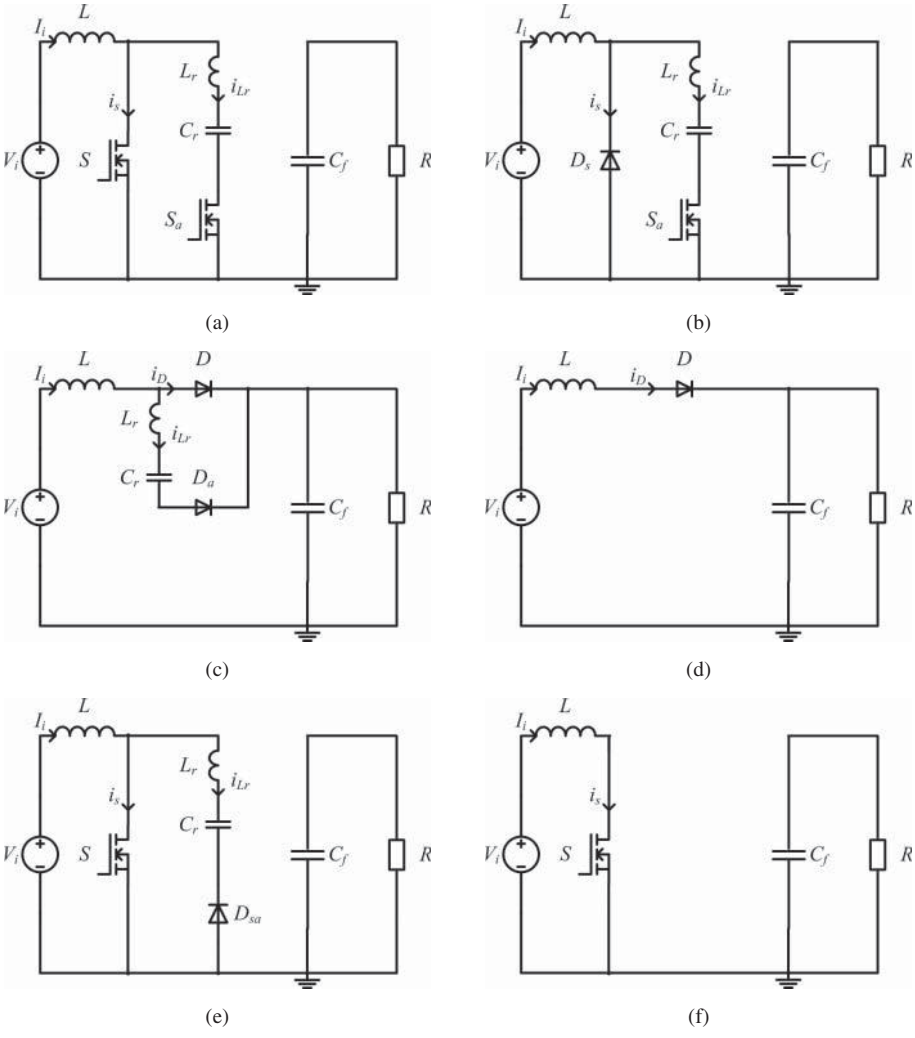


Figure 9.3 Equivalent circuits of Boost ZCT-PWM converter in normal operation: (a) stage I; (b) stage II; (c) stage III; (d) stage IV; (e) stage V; and (f) stage VI

assumptions should be taken into account before introducing the operating process:

1. All the switches and diodes are ideal devices.
2. The inductance L is large enough to keep the input current I_i almost invariable in one switching cycle.
3. The capacitance of output capacitor C_f is large enough to keep the output voltage V_o almost constant in one switching cycle.

The brief analysis of various operating stages is provided as follows.

Stage I (t_0, t_1)

Prior to t_0, the main switch S is conducting, and the resonant capacitor, C_r, is charged reversely to a certain negative voltage. At t_0, the auxiliary switch S_a is turned on and the resonant inductor L_r and resonant capacitor C_r starts to resonate. Then C_r discharges in reverse, while the resonant inductor current i_{Lr} increases in a forward direction. At the same time, the main switch current i_s decreases in a sinusoidal way. When $t = t_1$, i_s decreases to zero and i_{Lr} rises to the input current I_i, stage I is ended, and its equivalent circuit is as shown in Figure 9.3a.

Stage II (t_1, t_3)

During the time period (t_1, t_3), L_r and C_r remain resonant. As i_{Lr} keeps rising and becomes larger than I_i, the anti-paralleled diode of the main switch S, D_s, is turned on and the condition of zero-current turn-off for S is created. When $t = t_2$, C_r discharges to zero. Owing to $t_2 - t_0 = \frac{T_r}{4}$, in which $T_r = 2\pi\sqrt{L_r C_r}$ is the resonant cycle of L_r and C_r, the time to turn off the main switch S should be set at t_2.

During the time period (t_2, t_3), L_r and C_r remain resonant, i_{Lr} starts to decrease, and v_{Cr} rises from zero. When $t = t_3$, i_{Lr} decreases to I_i, $i_s = 0$ then D_s is shut down, and the auxiliary switch S_a should be turned off at the same time. Then stage II is over and its equivalent circuit is as shown in Figure 9.3b.

Stage III (t_3, t_4)

Because both switches S and S_a are turned off, diode D and auxiliary diode D_a will conduct to provide freewheeling paths for the input current I_i and resonant inductor current i_{Lr}. The resonance of L_r and C_r continues and i_{Lr} keeps decreasing. Assuming that L_r and C_r complete half of a resonant cycle at t_4, i_{Lr} decreases to zero and D_a is off. Stage III is over and its equivalent circuit is as shown in Figure 9.3c.

Stage IV (t_4, t_5)

As shown in Figure 9.3d, this stage is identical to that of a traditional Boost converter when S is turned off and D is on.

Stage V (t_5, t_6)

When $t = t_5$, S is turned on so D is off, and the input current I_i is transferred from S to D directly. At the same time, L_r and C_r start to resonate through S and D_{sa}, which is the anti-parallel diode of the auxiliary switch S_a. At the moment of t_6, L_r and C_r

complete half a resonant cycle, that is, $t_6 - t_5 = \frac{T_r}{2}$, i_{Lr} equals to zero then D_{sa} is off, stage V is over, and its equivalent circuit is as shown in Figure 9.3e.

Stage VI (t_6, t_7)

This stage is identical to that of the traditional Boost converter when S is turned on. The equivalent circuit is shown in Figure 9.3f. At the moment of t_7, S_a is turned on, then another switching cycle begins.

From the above analysis, it is obvious that the Boost ZCT-PWM converter can realize zero-current turn-off of the main switch S and zero-current turn-on of auxiliary switch S_a. But when S is turned on, there is current I_i flowing through it, which is hard-switching and will bring about the reversed recovering problems of diode D. In addition, S_a is turned off with hard-switching. Therefore, the switching loss of the Boost ZCT-PWM converter is relatively large and so it is desirable to achieve zero-current turning-on and turning-off of the two switches.

9.2.2 Sneak Circuit Paths of Boost ZCT PWM Converter

Before using sneak circuit paths to improve converter performance, the sneak circuit paths existing in the converter should be found. The following section will analyze the sneak circuit paths in the Boost ZCT PWM converter by using the switching Boolean matrix. The definition of all switching branches is shown in Figure 9.4, where the main switch S (including its anti-parallel diode D_s), diode D, auxiliary switch S_a (including its anti-parallel diode D_{sa}), and auxiliary diode D_a are defined as switching branches 1–4 respectively. As the state of the generalized switching branch L_r-C_r is related to the switching branches 2 and 4, it can be regarded as a non-switching branch, and all non-switching branches need not be numbered in order to simplify the analysis.

According to the circuit principle and operating principle of the Boost ZCT PWM converter, S and D, S_a and D_a, S and D_s, S_a, and D_{sa} cannot be turned on at the same

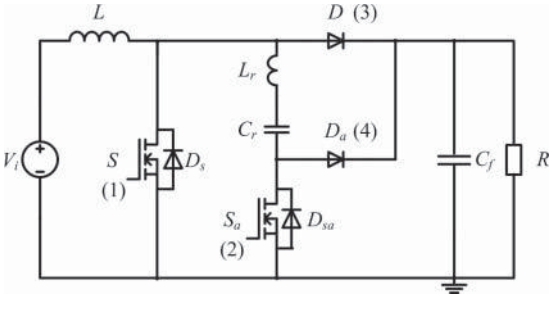


Figure 9.4 Switching branch definition of a Boost ZCT PWM converter

time. In addition, the switches with different current directions cannot be turned on at the same time. Combined with the above switching constraint conditions, the valid switching Boolean matrix $\mathbf{B_a}$ of the Boost ZCT PWM converter can be obtained, which is

$$\mathbf{B_a} = \begin{array}{c} \begin{matrix} S & S_a & D & D_a \end{matrix} \\ \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 \end{bmatrix} \end{array} \tag{9.1}$$

According to the definition of the switching branch and the equivalent circuits of normal operating stages shown in Figure 9.3, the normal switching Boolean matrix $\mathbf{B_n}$ of the Boost ZCT PWM converter is

$$\mathbf{B_n} = \begin{array}{c} \begin{matrix} S & S_a & D & D_a \end{matrix} \\ \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \end{bmatrix} \end{array} \tag{9.2}$$

Comparing Equation 9.1 with Equation 9.2, the sneak switching Boolean matrix $\mathbf{B_s}$ of the Boost ZCT PWM converter is

$$\mathbf{B_s} = \begin{array}{c} \begin{matrix} S & S_a & D & D_a \end{matrix} \\ \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix} \end{array} \tag{9.3}$$

By transferring the row vector in $\mathbf{B_s}$ to the equivalent circuit, there will be five sneak circuit stages in the Boost ZCT PWM converter, and their equivalent circuits are shown in the Figure 9.5.

9.2.3 The Improved Control Method of Boost ZCT PWM Converter

In order to achieve zero-current turn-on of the main switch S in the Boost ZCT PWM converter, the input current I_i must be transferred to the parallel branch of S before the

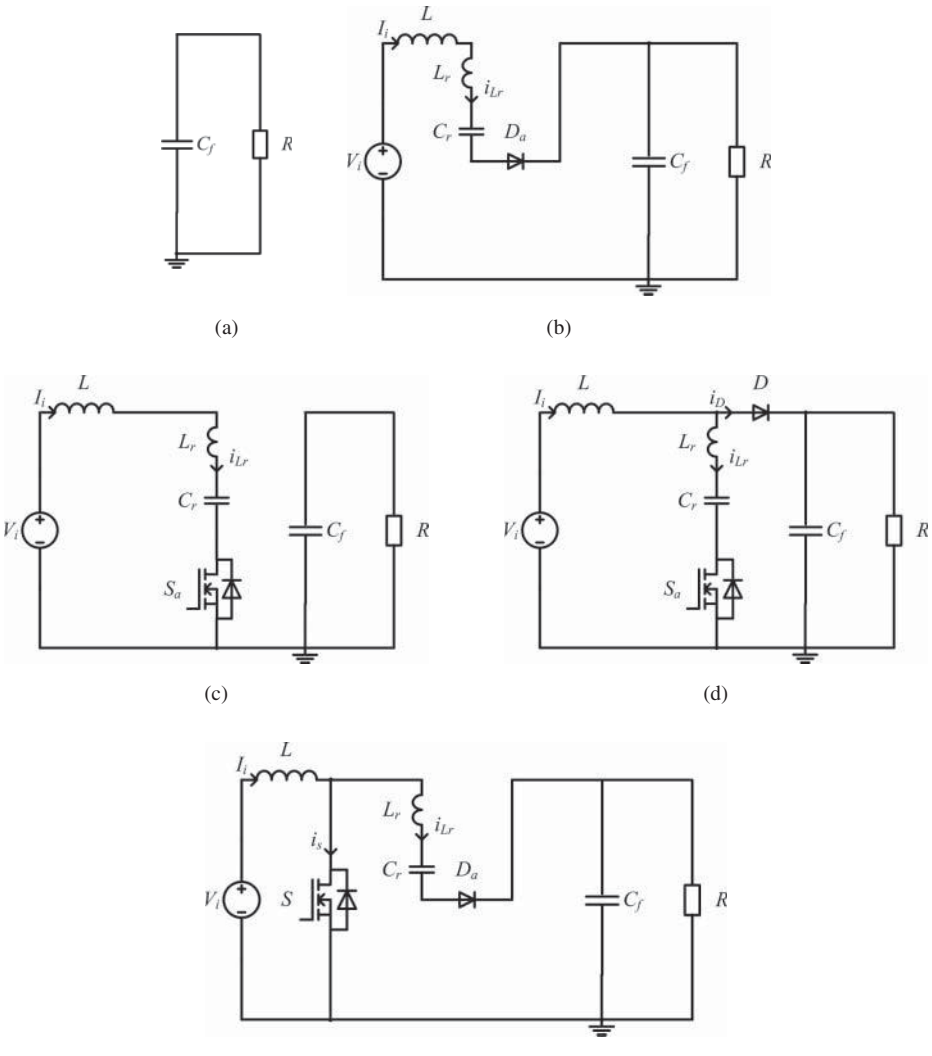


Figure 9.5 Sneak circuits in Boost ZCT PWM converter: (a) stage I′[0 0 0 0]; (b) stage II′ [0 0 0 1; (c) stage III′ [0 1 0 0]; (d) stage IV′ [0 1 1 0]; and (e) stage V′ [1 0 0 1]

main diode D is off. Therefore, similar to achieving the zero-current turn-off of the main switch S, the auxiliary switch S_a should be turned on before the main switch S is turned on.

In the same way, the zero-current turn-off of the auxiliary switch S_a can be achieved when the resonant inductor current i_{Lr} flows diversely through D_{sa}, the anti-parallel diode of S_a, but there should be a current path for i_{Lr} to flow through D_{sa}. Based on the existing current paths in Figures 9.3 and 9.5, it is found that the sneak circuit path in

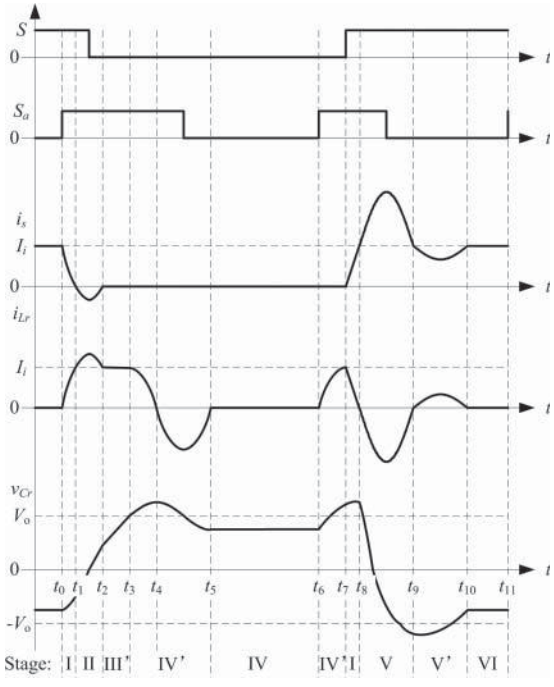


Figure 9.6 Typical waveforms of a Boost ZCT PWM converter with improved control sequence

Figure 9.5d can satisfy the above requirement. Therefore, delaying the turn-off time of S_a can make i_{Lr} resonate to zero and then flow through D_{sa} in reverse.

According to the above analysis, the improved control method for a Boost ZCT PWM converter is to make the auxiliary switch S_a turn on and off twice in one switching cycle and extend the on-state time of auxiliary switch S_a. The corresponding waveforms with the improved control sequence are shown in the Figure 9.6 [2]. The operating process can be divided into 10 stages, which are described as follows.

Stage (t_0, t_1)

The main switch S conducts before t_0, and the auxiliary switch S_a is turned on at the time t_0. This stage is the same as the normal stage I in Figure 9.3a.

Stage (t_1, t_2)

In this stage, L_r and C_r remain resonant, the anti-parallel diode D_s conducts due to $i_s < 0$, then S can be turned off with zero-current. This stage is the same as the normal stage II in Figure 9.3b.

Stage (t_2, t_3)

Because S and D_s have been turned off but S_a still conducts, the resonant current i_{Lr} is constant and equal to the input current I_i, while the resonant capacitor voltage v_{Cr} rises linearly. It is found that the equivalent circuit of this stage is the same as that of sneak stage III′ in Figure 9.5c.

Stage (t_3, t_5)

Assuming that when $t = t_3$, v_{Cr} rises to the output voltage V_o and the main diode D is turned on, L_r and C_r resonate again and i_{Lr} decreases, while the diode current i_D increases. When $t = t_4$, i_{Lr} decreases to zero and then flows in reverse through D_{sa}, thus the zero-current turn-off of S_a can be achieved. When $t = t_5$, half of a resonant cycle is completed, i_{Lr} resonates to zero, and D_{sa} is turned off then this stage is over, and its equivalent circuit is the same as that of sneak stage IV′ in Figure 9.5d.

Stage (t_5, t_6)

In this stage, S is turned off and D conducts, which is the same as the normal stage IV in Figure 9.3d.

Stage (t_6, t_7)

When $t = t_6$, the auxiliary switch S_a is turned on again, and L_r and C_r become resonant. Meanwhile, i_{Lr} increases and i_D decreases. This stage is the same as the normal stage IV in Figure 9.5d.

Stage (t_7, t_8)

Assuming that i_D decreases to zero and i_{Lr} increases to I_i at t_7, if S is turned on at this moment, zero-current turn-on of the main switch S can be achieved. After S is turned on, i_s increases and i_{Lr} decreases. When $t = t_8$, i_{Lr} decreases to zero and this stage is ended, whose equivalent circuit is the same as the normal stage I in Figure 9.3a.

Stage (t_8, t_9)

During this stage, as i_{Lr} flows reversely through D_{sa}, the zero-current turning off of S_a can be achieved. When L_r and C_r finish half a resonance cycle, i_{Lr} resonates to zero again and then D_{sa} is off, this stage is over, and its equivalent circuit is the same as the normal stage V in Figure 9.3e.

Stage (t_9, t_{10})

Owing to the fact that the resonant capacitor C_r is charged in reverse to less than $-V_o$, the auxiliary diode D_a will be turned on and provides a positive current path for i_{Lr}. When $t = t_{10}$, L_r and C_r finish another half resonant cycle, i_{Lr} is back to zero again, and D_{sa} becomes off. This stage is over and its equivalent circuit is the same as the sneak stage V' in Figure 9.5e.

Stage (t_{10}, t_{11})

In this stage, the main switch S is turned on and the main diode D is turned off, which is the same as normal operating mode VI in Figure 9.3f. Assuming that the auxiliary switch S_a is turned on at t_{11}, another switching cycle begins.

Synthesizing the above analysis, it is known that both of the main and auxiliary switches can achieve zero-current turn on and turn off, thus switching loss of the Boost ZCT PWM converter can be reduced significantly by changing the control sequence and inserting some sneak stages into the operating process. Therefore, making reasonably good use of the sneak circuit path can contribute to improving the performance of a power electronic converter.

9.3 Reconstruction of Power Electronic Converter Based on Sneak Circuits

Topology determines the basic performance and operating characteristics of a power electronic converter. For decades, scholars and engineers have invented a large number of topologies for converters such as the Cúk converter, resonant converter, soft-switching converter, multi-level converter, Z-source converter, and so on, which have greatly improved the level and quality of electric energy transformation, promoted further development of power electronic technology.

However, it is found that the invention of any kind of power electronic converter largely depends on the inventors' academic attainment and practical experience, as a systematic topology construction method for power electronic converters is still unformed. Furthermore, many typical power electronic converters also need further improvement and optimization in practical application. For this reason, researchers usually adopt a try and test method, modify the original topology by adding, deleting, or removing some components or units, and then testing the performance of the modified topology. The process of topology reconstruction will be repeated many times until the performance of the converter meets with the desired requirements. Obviously, there is no systematic topological modification method to follow.

Therefore, this section will make use of the sneak circuit path analysis method introduced in Chapter 6, and realize the topology reconstruction of a power electronic converter based on understanding the functions of the effective paths. The Boost ZCT

PWM converter is also taken as an example, to illustrate how to reconstruct a modified converter based on sneak circuits.

9.3.1 Structure of Boost ZCT PWM Converter

All of the effective current paths of a Boost ZCT PWM converter can be expressed by the valid switching Boolean matrix $\mathbf{B_a}$ in Equation 9.1, where it is found that the elements of column 2 and column 4 in $\mathbf{B_a}$ are symmetrical. By exchanging column 2 and column 4, a new Boolean matrix $\mathbf{B_{an}}$, which has the same row vector as $\mathbf{B_a}$ in Equation 9.1, can be expressed by the following:

$$\mathbf{B_{an}} = \begin{matrix} 1 & 2 & 3 & 4 \end{matrix} \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 \end{bmatrix} = \begin{matrix} 1 & 4 & 3 & 2 \end{matrix} \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix} \tag{9.4}$$

In order to transform the new Boolean matrix $\mathbf{B_{an}}$ in Equation 9.4 to a schematic diagram of power electronic converter, the component on branch 2 (S_a) and that on branch 14 (D_a) of the original Boost ZCT PWM converter should be exchanged and the other branches kept unchanged. The modified topology of Boost ZCT PWM converter is illustrated in Figure 9.7, where diode D_x substitutes for the original auxiliary switch S_a and the conducting direction of D_x is consistent with the anti-parallel diode of S_a; switch S_x substitutes for the original auxiliary diode D_a and the anti-parallel diode of S_x keeps the same conducting direction of D_a.

The modified converter in Figure 9.7 and the original converter in Figure 9.1 have the same row vectors or switching states, therefore the modified Boost ZCT PWM converter may keep the original function of the Boost ZCT PWM converter.

9.3.2 Performance of the Modified Boost ZCT PWM Converter

Based on the improved control method for the Boost ZCT PWM converter described in Section 9.2.3, the auxiliary switch S_x needs to be turned on before the main switch S is turned on and turned off, in order to ensure ZCS of the main switch S. Due to the

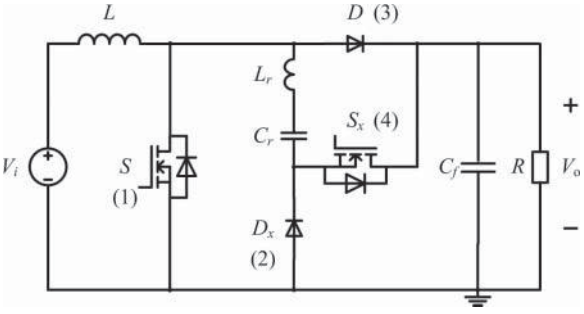


Figure 9.7 Schematic diagram of the modified Boost ZCT PWM converter

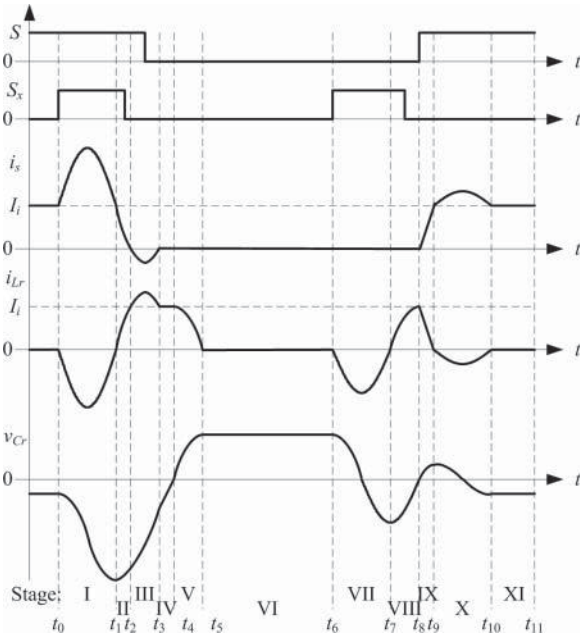


Figure 9.8 Typical waveforms of the modified Boost ZCT PWM converter

converter structure having been changed, the turn-off time of S_x should be designed according to the actual operating conditions.

The typical waveforms of the modified Boost ZCT PWM converter are shown in Figure 9.8 [2], where there are 11 operating stages in one switching cycle, and the equivalent circuit of each stage is shown in Figure 9.9.

The operating process of the modified Boost ZCT PWM converter can be described as follows.

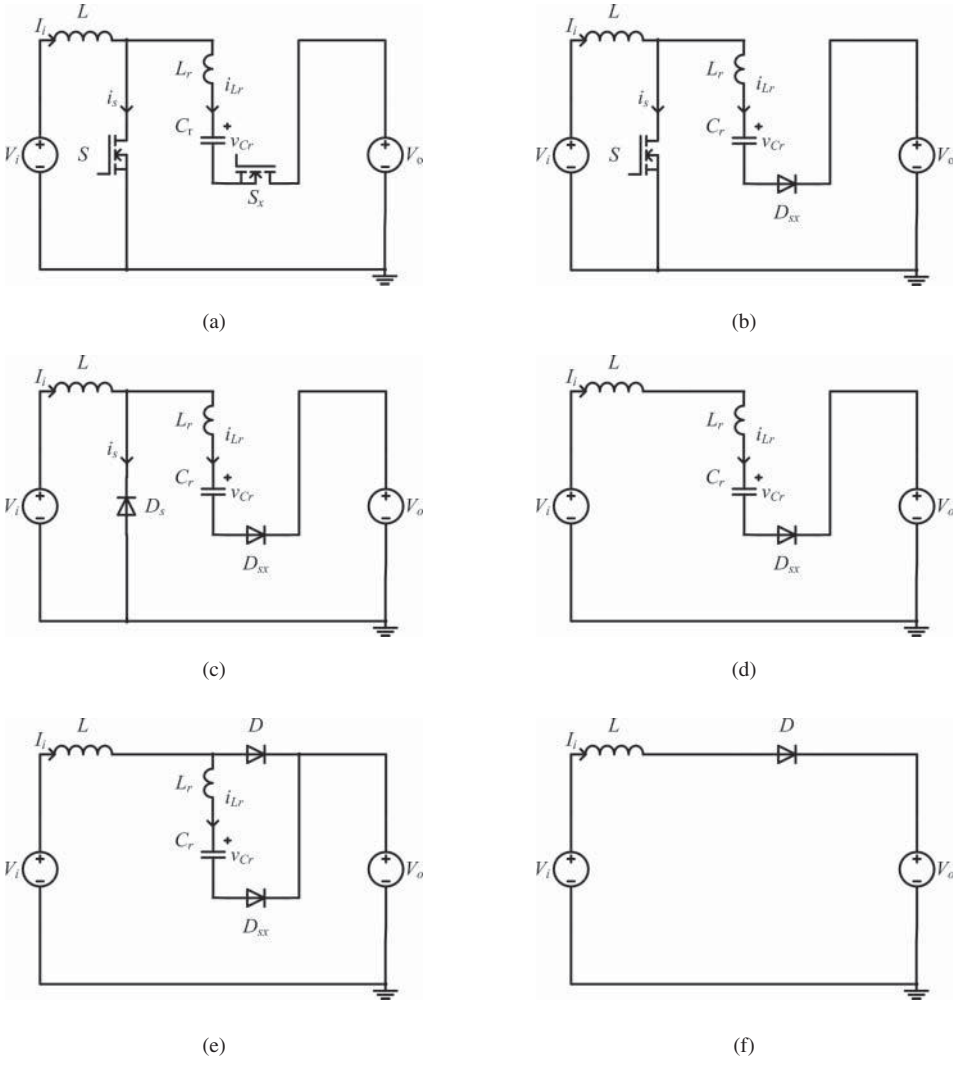
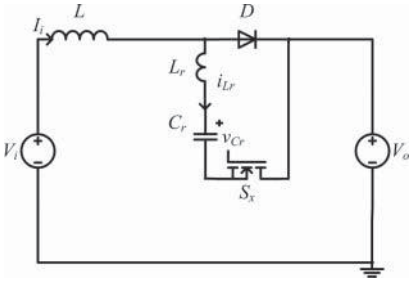


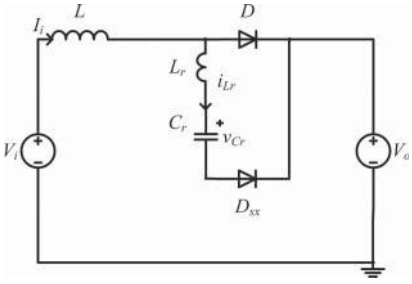
Figure 9.9 Equivalent circuits of the modified Boost ZCT PWM converter: (a) stage I; (b) stage II; (c) stage III; (d) stage IV; (e) stage V; (f) stage VI; (g) stage VII; (h) stage VIII; (i) stage IX; (j) stage X; and (k) stage XI

Stage I (t_0, t_1)

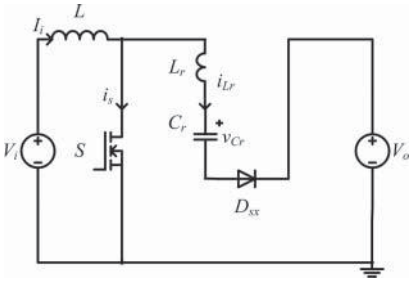
Before stage I, S is on and D is off, the resonant branch does not work, and v_{Cr} is kept at a certain negative value. At the time of t_0, S_x is turned on, and L_r and C_r are in resonance through S and S_x. Since the output voltage V_o is added on the resonant branch directly, i_{Lr} increases from zero in the negative direction, C_r is charged reversely, and



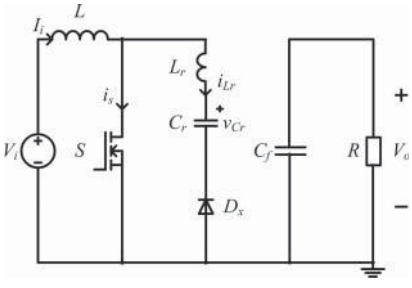
(g)



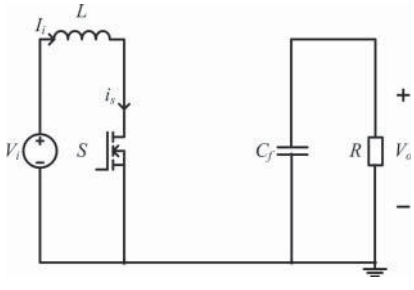
(h)



(i)



(j)



(k)

Figure 9.9 (*continued*)

i_s increases from I_i. After half of a resonant cycle, when $t = t_1$, this stage is ended and its equivalent circuit is as shown in Figure 9.9a.

Stage II (t_1, t_2)

L_r and C_r continue to resonate, while C_r discharges, i_{Lr} increases positively from zero and flows through D_{sx} and the anti-parallel diode of auxiliary switch S_x. Then S_x can be turned off under zero current after t_1. Assuming that $i_{Lr} = I_i$ and $i_s = 0$ at t_2, this stage is ended and its equivalent circuit is as shown in Figure 9.9b.

Stage III (t_2, t_3)

In this stage, L_r and C_r remain resonant, but i_{Lr} increases from I_i and i_s increases negatively. Then D_s, the anti-parallel diode of main switch S conducts and clamps the main switch at zero voltage. When $t = t_3$, i_s resonates to zero again and D_s will be shut down, thus S should be turned off with zero current in this stage. The equivalent circuit of stage III is as shown in Figure 9.9c.

Stage IV (t_3, t_4)

Because D is still in the off state, input current I_i flows through the resonant branch, that is, $i_{Lr} = I_i$. Then C_r will discharge linearly, and assuming that $v_{Cr} = 0$ at t_4, D becomes conducting. The equivalent circuit of stage IV is as shown in Figure 9.9d.

Stage V (t_4, t_5)

In this stage, D is on, i_{Lr} continues to decrease until it falls to zero, then D_{sx} becomes turned off. The equivalent circuit of this stage is as shown in Figure 9.9e.

Stage VI (t_5, t_6)

The auxiliary circuit stops working as D_{sx} is shut down, and the equivalent circuit of stage VI is as shown in Figure 9.9f.

Stage VII (t_6, t_7)

In order to achieve zero-current turn-on of main switch S, the auxiliary switch S_x is turned on again at t_6. As i_{Lr} is equal to zero during stage VI, S_x is turned on under zero current conditions. When S_x is on, L_r and C_r begins resonance through D and S_x, and after half a resonant cycle, this stage is terminated and i_{Lr} resonates to zero again. The corresponding equivalent circuit is shown in Figure 9.9g.

Stage VIII (t_7, t_8)

L_r and C_r continue to resonate, i_{Lr} becomes positive and flows through D_{sx}, then zero current and zero voltage turn-off of S_x can be realized after t_7. The current passing through diode D will decrease as i_{Lr} increases, when $i_{Lr} = I_i$ at t_8, the diode current reduces to zero, then D is off. The equivalent circuit of stage VIII is shown in Figure 9.9h.

Stage IX (t_8, t_9)

If S is turned on at t_8, because the inductor current cannot change suddenly, the main switch S realizes zero-current turn-on. After S conducts, i_{Lr} declines rapidly down to zero at t_9, D_{sx} will be off, and stage IX is over, the equivalent circuit of which is shown in Figure 9.9i.

Stage X (t_9, t_{10})

As v_{Cr} is positive at t_9, L_r and C_r continue to resonate, and i_{Lr} flows reversely through D_x and S. When $t = t_{10}$, i_{Lr} resonates to zero, D_x turns off, and this stage is ended, and the equivalent circuit is shown as in Figure 9.9j.

Stage XI (t_{10}, t_{11})

This stage is consistent with the conventional Boost converter when S is on, and its equivalent circuit is as shown in Figure 9.9k. As the resonant branch does not work in stage XI, i_{Lr} is zero, then S_x will be turned on to begin another switching cycle under zero current conditions.

From the above operating process of the modified Boost ZCT PWM converter, it is clear that this converter cannot only realize ZCS of the main switch and auxiliary switch, but also has the advantage that the peak current of auxiliary switch (i.e., i_{Lr}) is relatively small and the switch time of the auxiliary switch is easy to control, and so on [2]. These results show that the topology reconstruction method, by making use of the sneak circuit path analysis method, is feasible, and the good performance of the original converter can be retained.

9.4 New Functions of Power Electronic Converter Based on Sneak Circuits

When a power electronic converter operates in the sneak circuit mode, the sneak circuit phenomenon is not entirely detrimental, such as the zero voltage switching (ZVS) synchronous Buck converter in Chapter 5. In this section, the Cúk converter will be taken as an example to illustrate how to design a new function – power factor correction (PFC), by using its sneak circuit operating modes automatically.

9.4.1 PFC Principle of Cúk Converter

Before designing the new functions of a Cúk converter, the properties of the converter in different operating modes should be analyzed.

9.4.1.1 Normal Operating Mode

For the normal operating mode illustrated in Figure 7.9a, based on Equations 3.31–3.34 and 3.37, the output voltage of the Cúk converter is $V_o = \frac{d}{1-d}V_g$ and the expressions of inductor currents in stage I ($0 \le t < dT$) are

$$i_{L1-1}(t) = I_{01} + \frac{V_g}{L_1}t \tag{9.5}$$

$$i_{L2-1}(t) = I_{02} + \frac{V_g}{L_2}t \tag{9.6}$$

where $I_{01} = \frac{d^2V_g}{(1-d)^2R} - \frac{dTV_g}{2L_1}$, $I_{02} = \frac{dV_g}{(1-d)R} - \frac{dTV_g}{2L_2}$ and $T = 1/f$ is the switching cycle.

The inductor currents in stage II ($dT \le t < T$) are

$$i_{L1-1}(t) = I_{01} + \frac{V_g}{L_1}\frac{d(T-t)}{(1-d)} \tag{9.7}$$

$$i_{L2-1}(t) = I_{02} + \frac{V_g}{L_2}\frac{d(T-t)}{(1-d)}, \tag{9.8}$$

then, the average inductor currents in normal operating mode are

$$\begin{aligned} I_{L1-1} &= \frac{1}{T}\left(\int_0^{dT} i_{L1-1}(t)\,dt + \int_{dT}^{T} i_{L1-1}(t)dt\right) \\ &= \frac{1}{T}\left(\int_0^{dT}\left[I_{01} + \frac{V_g}{L_1}t\right]dt + \int_{dT}^{T}\left[I_{01} + \frac{V_g}{L_1}\frac{d(T-t)}{(1-d)}\right]dt\right) \\ &= \left(\frac{d}{1-d}\right)^2\frac{V_g}{R} \end{aligned} \tag{9.9}$$

$$\begin{aligned} I_{L2-1} &= \frac{1}{T}\left(\int_0^{dT} i_{L2-1}(t)\,dt + \int_{dT}^{T} i_{L2-1}(t)dt\right) \\ &= \frac{1}{T}\left(\int_0^{dT}\left[I_{02} + \frac{V_g}{L_2}t\right]dt + \int_{dT}^{T}\left[I_{02} + \frac{V_g}{L_2}\frac{d(T-t)}{(1-d)}\right]dt\right) \\ &= \left(\frac{d}{1-d}\right)\frac{V_g}{R} \\ &= \frac{V_o}{R} \end{aligned} \tag{9.10}$$

9.4.1.2 Sneak Circuit Operating Mode 1

For the sneak circuit operating mode 1 illustrated in Figure 7.9b, based on Equations 3.31–3.34, 3.49, 3.52, and 3.54, the output voltage changes to $V_o = \frac{d}{\lambda}V_g$, in which

$\lambda = \sqrt{\frac{2L_1L_2f}{R(L_1+L_2)}}$, and the inductor currents in stage I ($0 \le t < dT$) are

$$i_{L1-2}(t) = I_0 + \frac{V_g}{L_1}t \tag{9.11}$$

$$i_{L2-2}(t) = -I_0 + \frac{V_g}{L_2}t \tag{9.12}$$

The inductor currents in stage II ($dT \le t < t_x$) are

$$i_{L1-2}(t) = I_0 + \frac{V_g}{L_1}\frac{dT(t_x - t)}{t_x - dT} \tag{9.13}$$

$$i_{L2-2}(t) = -I_0 + \frac{V_g}{L_2}\frac{dT(t_x - t)}{t_x - dT} \tag{9.14}$$

While the expression of the inductor currents in stage III ($t_x \le t < T$) are

$$i_{L1-2}(t) = I_0 \tag{9.15}$$

$$i_{L2-2}(t) = -I_0 \tag{9.16}$$

where $I_0 = \frac{V_g dT}{2}\left(\frac{d}{L_2} - \frac{\lambda}{L_1}\right)$ and $t_x = dT + \lambda T$, then, the average inductor currents in sneak circuit operating mode 1 are

$$\begin{aligned} I_{L1-2} &= \frac{1}{T}\left(\int_0^{dT} i_{L1-2}(t)\,dt + \int_{dT}^{t_x} i_{L1-2}(t)dt + \int_{t_x}^{T} i_{L1-2}(t)dt\right) \\ &= \frac{1}{T}\left(\int_0^{dT}\left[I_0 + \frac{V_g}{L_1}t\right]dt + \int_{dT}^{t_x}\left[I_0 + \frac{V_g}{L_1}\frac{dT\,(t_x - t)}{t_x - dT}\right]dt + \int_{t_x}^{T} I_0 dt\right) \\ &= V_g d^2 T\frac{L_1 + L_2}{2L_1L_2} \end{aligned} \tag{9.17}$$

$$\begin{aligned} I_{L2-2} &= \frac{1}{T}\left(\int_0^{dT} i_{L2-2}(t)\,dt + \int_{dT}^{t_x} i_{L2-2}(t)dt + \int_{t_x}^{T} i_{L2-2}(t)dt\right) \\ &= \frac{1}{T}\left(\int_0^{dT}\left[-I_0 + \frac{V_g}{L_2}t\right]dt + \int_{dT}^{t_x}\left[-I_0 + \frac{V_g}{L_2}\frac{dT\,(t_x - t)}{t_x - dT}\right]dt + \int_{t_x}^{T}(-I_0)dt\right) \\ &= V_g d\lambda T\frac{L_1 + L_2}{2L_1L_2} \\ &= V_o\lambda^2 T\frac{L_1 + L_2}{2L_1L_2} \\ &= \frac{V_o}{R} \end{aligned} \tag{9.18}$$

9.4.1.3 Sneak Circuit Operating Mode 2

For the sneak circuit operating mode 2 illustrated in Figure 7.9c, due to $I_o = 0$, the inductor current expressions change to

$$i_{L1-3}(t) = \begin{cases} \dfrac{V_g}{L_1} t & 0 \le t < dT \\ \dfrac{V_g}{L_1} \dfrac{dT\,(t_x - t)}{t_x - dT} & dT \le t < t_x \\ 0 & t_x \le t < T \end{cases} \tag{9.19}$$

$$i_{L2-3}(t) = \begin{cases} \dfrac{V_g}{L_2} t & 0 \le t < dT \\ \dfrac{V_g}{L_2} \dfrac{dT\,(t_x - t)}{t_x - dT} & dT \le t < t_x \\ 0 & t_x \le t < T \end{cases} \tag{9.20}$$

When $d = \lambda \frac{L_2}{L_1}$, the Cúk converter will work in sneak circuit operating mode 2 and the output voltage is $V_o = \frac{L_2}{L_1} V_g$, the average inductor currents in this mode are

$$I_{L1-3} = \frac{V_g}{2L_1} dt_x = \frac{V_g}{R} \left(\frac{L_2}{L_1} \right)^2 \tag{9.21}$$

$$I_{L2-3} = \frac{V_g}{2L_2} dt_x = \frac{V_g}{R} \frac{L_2}{L_1} = \frac{V_o}{R} \tag{9.22}$$

Synthesizing Sections 3.6 and 7.5 and the results of the average inductor currents presented above, the properties of the Cúk converter operating in different modes are illustrated in Table 9.1. According to the structure of the Cúk converter, it is known that the average value of the input current of the converter is equal to that of inductor current I_{L1}, and the average value of output current is equal to that of the inductor current I_{L2}.

Table 9.1 shows that whichever operating mode the Cúk converter works in, its average value of input current I_{L1} is always proportional to the input voltage V_g when the circuit parameters and operating conditions are determined. Therefore, the Cúk converter can realize the function that the input current follows the input voltage automatically without any current control loop. At this moment, the power factor of the Cúk converter is theoretically a unit, which means that this converter inherently has ideal PFC properties.

Further research shows that due to the average input current equal to $I_{L1} = \left(\frac{d}{1-d} \right)^2 \frac{V_g}{R}$ in normal operating mode, even if the duty cycle d of the Cúk converter remains constant, I_{L1} cannot follow the input voltage V_g linearly when the load resistance R changes. While in sneak circuit operating mode 1, the average input

Table 9.1 The properties of a Cúk converter under different operating modes

Operating mode	Phenomenon	Average input current (I_{L1})	Average output current (I_{L2})	Output voltage V_o	The range of d
Normal operating mode	Normal operation Sneak circuit phenomenon I Sneak circuit phenomenon II	$\left(\frac{d}{1-d}\right)^2\frac{V_g}{R}$	$\frac{V_o}{R}$	$\frac{d}{1-d}V_g$	$d > 1-\lambda$
Sneak circuit operating mode 1	Sneak circuit phenomenon III Sneak circuit phenomenon IV	$V_g d^2 T\frac{L_1+L_2}{2L_1L_2}$		$\frac{d}{\lambda}V_g$	$d < 1-\lambda$
Sneak circuit operating mode 2	Sneak circuit phenomenon V	$\left(\frac{L_2}{L_1}\right)^2\frac{V_g}{R}$		$\frac{L_2}{L_1}V_g$	$d=\lambda\frac{L_2}{L_1}<1-\lambda$

Note: $\lambda = \sqrt{\frac{2L_1L_2f}{R(L_1+L_2)}}$.

current is $I_{L1} = V_g d^2 T\frac{L_1+L_2}{2L_1L_2}$, which is not related to the load R, therefore it can ensure that I_{L1} can follow V_g linearly with a fixed d. Although the duty cycle d in sneak circuit operating mode 2 is not related to the average input current $I_{L1} = \frac{V_g}{R}\left(\frac{L_2}{L_1}\right)^2$, the relationship between I_{L1} and V_g is also influenced by the load R. Comparing these three operating modes of the Cúk converter, the sneak circuit operating mode 1 is most suitable to realize PFC function.

Therefore, if the Cúk converter works in sneak circuit operating mode 1 and the duty cycle d is set to a fixed value, the PFC function, which means that the input current follows the input voltage, can be realized automatically without any input current control.

9.4.2 PFC Implementation of Cúk Converter

According to the above analysis, the schematic diagram of a Cúk PFC converter based on sneak circuit is illustrated in Figure 9.10, where v_{in} is the input ac voltage and v_s is the drive voltage of switch S, which determines the duty cycle d.

From Table 7.4, it is known that when the Cúk converter works in sneak circuit operating mode 1, the inductor current can be divided into two situations. One is that inductor current i_{L2} is always greater than zero; and the other is that inductor current i_{L1} is also always greater than zero. Because i_{L1} is equivalent to the input current of the Cúk converter, in order to ensure i_{L1} is consistent with the rectified input voltage

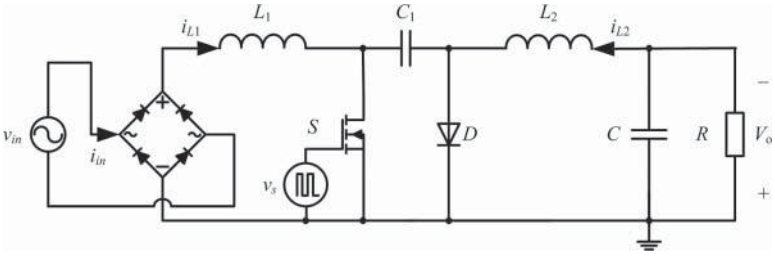


Figure 9.10 A Cúk PFC converter based on a sneak circuit

$|v_{in}|$, the converter should work under the conditions that i_{L1} is always positive, that is, with sneak circuit phenomenon IV, as illustrated in Table 7.5. Referring to Equation 3.55, the operating conditions of a Cúk PFC converter should be

$$\lambda\frac{L_2}{L_1} < d < 1-\lambda \tag{9.23}$$

The corresponding range of output voltage is

$$\frac{L_2}{L_1}V_{in} < V_o = \frac{d}{\lambda}V_{in} < \frac{1-\lambda}{\lambda}V_{in} \tag{9.24}$$

where V_{in} is the root-mean-square (RMS) value of the input voltage.

The proposed Cúk PFC converter in Figure 9.10 will be verified by simulation results in PSIM®. The simulation parameters are $v_{in} = 220\sqrt{2}\sin(100\pi t)$, $L_1 = 2.4$ mH, $L_2 = 0.15$ mH, $C_1 = 0.82$ μF, $C = 330$ μF, $R = 100\ \Omega$, $f = 50$ kHz, and $\lambda = 0.3757$. According to Equation 9.23, the range of the duty cycle is $0.023 < d < 0.625$. The open-loop control is used and $d = 0.3$ is set, thus $V_o = \frac{d}{\lambda}V_{in} = 175$ V. The simulation results are illustrated in Figure 9.11, which show that the phases of input voltage v_{in} and input current i_{in} of the ac side are almost the same and the shape of i_{in} is approximate to sine waves. The inductor current i_{L1} is always greater than zero and the output voltage V_o is 175 V, which is well consistent with the analytical value. At this moment, PF = 0.991, and the total harmonic distortion (THD) value of the input current i_{in} is THD = 13%, which verifies the feasibility of the designed Cúk PFC converter.

From the simulation results, the Cúk PFC converter has the following merits, when compared to the traditional Boost PFC converter:

1. The input current follows the input voltage automatically, so the PFC function can be achieved without any current loop control. The control circuit of the Cúk PFC converter is relatively simple, as only fixed duty cycle and switching frequency are needed.
2. The output voltage is larger than the input voltage in the Boost PFC converter, while the Cúk PFC converter can boost or buck the output voltage only by selecting the suitable circuit parameters and its output voltage range is relatively wide.

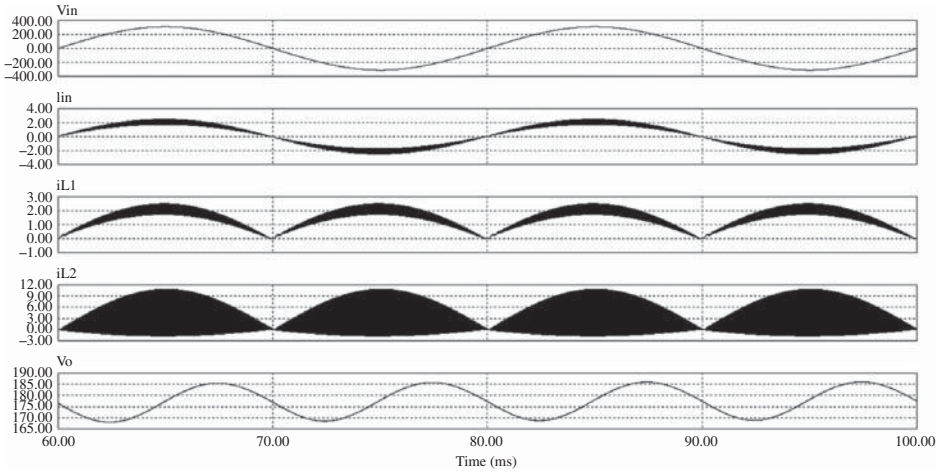


Figure 9.11 Simulation waveforms of a Cúk PFC converter

3. The switch *S* operates with zero-current turn-on and the diode *D* operates with zero-current turn-off in the Cúk PFC converter, based on the sneak circuit, which will reduce the switching loss.
4. The ripple of the input current in the Cúk PFC converter is small, so it is suitable for the situation that has the higher requirement of the current ripple.

In addition, the idea that uses the sneak circuit to realize the PFC function can also be applied to isolate the Cúk converter and Sepic converter [3]. The isolated Cúk PFC converter and Sepic PFC converter have more advantages, such as that the power supply can be isolated from the load and the range of the ratio between input voltage and output voltage is wider.

In short, based on the nature characteristics of the sneak circuit, some new functions of a power electronic converter will be realized when the converter operates in sneak circuit mode. This means that sneak circuits can be made good use of under certain conditions.

9.5 Fault Analysis of Power Electronic Converter Based on Sneak Circuits

The failure of the power electronic converter often refers to the failure of the main circuit, and 90% of failures are due to the damage of the switching components, such as short circuit or open circuit. When a sneak circuit occurs, it looks like a short-circuit or open-circuit of some switching components, and causes the converter topology to change. Thus it is possible to apply the sneak circuit path analysis method to fault diagnosis and fault identification of the power electronic converter.

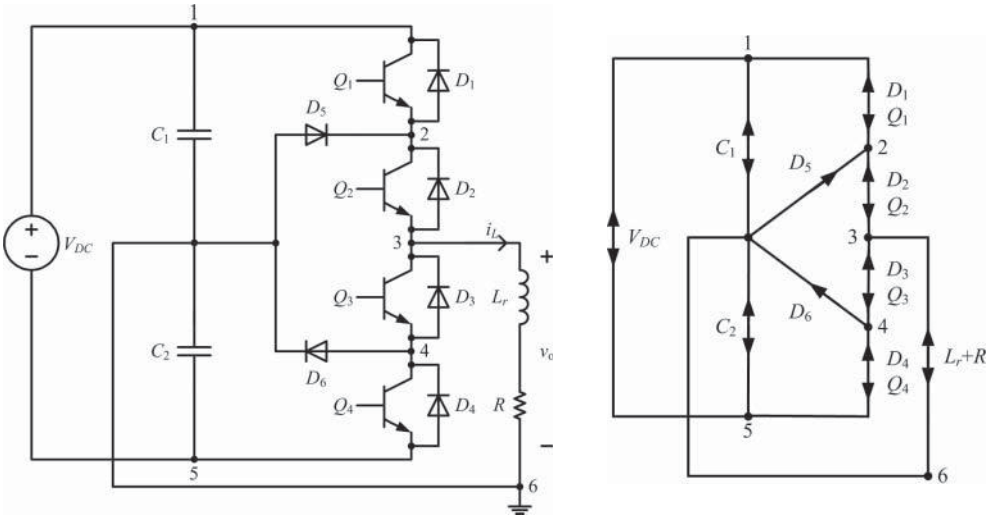


Figure 9.12 Diode-clamped three-level HB inverter and its directed graph: (a) schematic diagram; and (b) directed graph

The next section will take a diode-clamped three-level half-bridge (HB) inverter as an example, extract typical fault characteristics by using the directed graph and adjacency matrix of power electronic converter, and then realize fault analysis.

9.5.1 Adjacency Matrix of Diode-Clamped Three-Level HB Inverter

A schematic diagram of the diode-clamped three-level HB inverter is shown in Figure 9.12a. Referring to the definition of a directed graph of the power electronic converter in Section 6.3.1, the intersection of components in the converter can be defined as a vertex, and each component can be defined as an edge, and the direction of the edge is determined by the current characteristics of the components. Thus, the directed graph of the diode-clamped three-level half bridge inverter is shown in Figure 9.12b.

According to Figure 9.12b, the adjacency matrix of the diode-clamped three-level HB inverter is

$$\mathbf{A} = \begin{bmatrix} 0 & x & 0 & 0 & 1 & 1 \\ 1 & 0 & x & 0 & 0 & 0 \\ 0 & 1 & 0 & x & 0 & 1 \\ 0 & 0 & 1 & 0 & x & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.25}$$

where symbol x is used to represent the switching component in the adjacency matrix, and the value of x is decided by the state of the switch, $x = 1$ when the switch is turned on, and $x = 0$ when the switch is shut down.

When a short circuit failure occurs in the converter, two vertices that are connected to the failed edge will coincide. By assuming that the component between vertices i and j is short-circuit, then the value of the elements in row i of the original adjacency matrix changes to $r_i' = r_i \oplus r_j$, and the value of the elements in column i changes to $c_i' = c_i \oplus c_j$. By deleting the jth row and jth column of the original adjacency matrix, and ensuring that the elements on the diagonal of the adjacency matrix always remain at zero, that is, $a_{ii}' = 0$, then the modified adjacency matrix corresponds to short-circuit failure.

Assuming that the switch Q_1 in Figure 9.12a is short-circuited, vertex 1 and vertex 2 in Figure 9.12b coincide, and Equation 9.25 becomes

$$\mathbf{A}_{\mathrm{Q_1\text{-}S}} = \begin{bmatrix} 0 & x & 0 & 1 & 1 \\ 1 & 0 & x & 0 & 1 \\ 0 & 1 & 0 & x & 1 \\ 1 & 0 & 1 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.26}$$

When a component becomes open-circuit, the edge with the open-circuit component is disconnected. Assuming that the component between vertices i and j is an open circuit, if the corresponding edge is a one-way side edge from i to j, then set $a_{ij}' = 0$; if the edge is bi-directional, then set $a_{ij}' = a_{ji}' = 0$, and keeping the other elements unchanged, the modified adjacency matrix corresponds to the open circuit is obtained.

Assuming that diode D_5 in Figure 9.12a is an open circuit, the one-way edge from vertex 2 to vertex 6 in Figure 9.12b is disconnected, and Equation 9.25 becomes

$$\mathbf{A}_{\mathrm{D_5\text{-}O}} = \begin{bmatrix} 0 & x & 0 & 0 & 1 & 1 \\ 1 & 0 & x & 0 & 0 & 0 \\ 0 & 1 & 0 & x & 0 & 1 \\ 0 & 0 & 1 & 0 & x & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.27}$$

Based on the above method, the adjacency matrix corresponding to component failure can be obtained. According to the definition of adjacency matrix of a power electronic converter, the current path in the power electronic converter is determined by the product of adjacency matrix elements. If

$$a_{i,j} \cdot a_{j,k} \ \ldots \ a_{m,n} \cdot a_{n,i} = 1 \tag{9.28}$$

then the vertex sequence $i - j - k - \cdots - m - n$ comprises a current path. Because the current does not flow through the duplicate vertex or edge, the path obtained by Equation 9.28 will not contain the same vertices.

Therefore, all paths under normal operating mode can be obtained according to the normal adjacency matrix, and the paths under fault conditions can be obtained according to the failure adjacency matrix. Comparing the normal paths with the fault paths, the variation of some electrical parameters can be derived, thus the criteria of fault diagnosis can be obtained.

9.5.2 *Electrical Characteristics of Diode-Clamped Three-Level HB Inverter*

During the operating process of a power electronic converter, the failure probability of switching components is the largest, because the switch or diode operates at a high switching frequency and withstands a certain amount of voltage and current stress. As an instantaneous and very high current usually appears after a short-circuit failure, the over-current protection circuit in the power electronic converter will take action immediately, and clear system faults. However, the open circuit of switching components often leads to distortion of the output waveforms, therefore it is necessary to diagnose which component is malfunctioning.

It is found that there are four power switches and six diodes in the diode-clamped three-level HB inverter. As there are ten kinds of single component open-circuit faults and one normal operating mode, at least four electrical variables are needed to determine the above eleven conditions. Generally, the output voltage v_o, the load current i_L, the voltage across Q_1 in the upper leg v_{Q1}, and the voltage across Q_4 in the lower leg v_{Q4}, are selected to be monitored, among them, v_o and i_L are used to judge the operating mode, and v_{Q1} and v_{Q4} are used to judge the fault location.

According to the operating principle of the diode-clamped three-level HB inverter, there are six operating statuses under normal operating mode, which are listed in Table 9.2.

Taking status I as an example, Q_1 and Q_2 are conducting, which means $a_{12} = 1$, $a_{23} = 1$, $a_{34} = 0$, and $a_{45} = 0$, and the corresponding adjacency matrix becomes

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.29}$$

From Equation 9.29, $a_{12} \times a_{23} \times a_{36} \times a_{61} = 1$, thus the current path corresponding to status I is 1-2-3-6, and the values of electrical variables can be obtained by analyzing the path, which are $v_o = v_{36} = v_{16} = \frac{V_{DC}}{2}$, $i_L > 0$, $v_{Q1} = v_{12} = 0$, and $v_{Q4} = v_{45} = \frac{v_{35}}{2} = \frac{v_{15}}{2} = \frac{V_{DC}}{2}$. Similarly, the current paths and variable values of statuses II to VI can be achieved and are listed in Table 9.2.

Table 9.2 Current paths and electrical variables of a diode-clamped three-level HB inverter under normal operating mode

Status	Conducting component	Current path	Electrical variables			
			v_o	i_L	v_{Q1}	v_{Q4}
I	Q_1, Q_2	1-2-3-6	$\frac{V_{DC}}{2}$	>0	0	$\frac{V_{DC}}{2}$
II	D_1, D_2	3-2-1-6	$\frac{V_{DC}}{2}$	<0	0	$\frac{V_{DC}}{2}$
III	D_5, Q_2, Q_3	2-3-6	0	>0	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$
IV	D_6, Q_2, Q_3	3-4-6	0	<0	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$
V	D_3, D_4	5-4-3-6	$-\frac{V_{DC}}{2}$	>0	$\frac{V_{DC}}{2}$	0
VI	Q_3, Q_4	3-4-5-6	$-\frac{V_{DC}}{2}$	<0	$\frac{V_{DC}}{2}$	0

9.5.3 Failure Criterion of Diode-Clamped Three-Level HB Inverter

This section will discuss how to obtain the failure criteria by using the adjacency matrix and realize fault diagnosis, when one and only one switching component is in open-circuit.

9.5.3.1 Q_1 Open-Circuit

Assuming that Q_1 is an open circuit, status I is selected for fault diagnosis, because Q_1 only conducts in status I under normal conditions. When Q_1 is an open circuit, the fault adjacency matrix of status I is

$$\mathbf{A}_{1\text{-}Q_1\text{-}O} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.30}$$

Due to $a_{12} = 0$, the original current path 1-2-3-6 does not exist. According to the direction of the inductor current i_L, $a_{23} \times a_{36} \times a_{62} = 1$, which means that a new current path 2-3-6 emerges and makes the load short circuit, then $v_o = 0$. i_L will flow through D_5 and Q_2, and $v_{Q1} = v_{12} = v_{13} = v_{16} = \frac{V_{DC}}{2}$. In status I, as Q_3, Q_4, and D_6

are all shut down, then $v_{Q4} = v_{45} = \frac{2}{3}v_{35} = \frac{2}{3}v_{65} = \frac{V_{DC}}{3}$. Even if i_L is equal to zero when Q_1 has been open, no current path exists in status I, so $v_0 = 0$, $v_{Q1} = \frac{V_{DC}}{2}$, and $V_{Q4} = \frac{V_{DC}}{3}$ as well.

9.5.3.2 Q_2 Open-Circuit

Assuming that Q_2 is an open-circuit, Q_2 conducts in statuses I and III, and D_5 conducts only in status III, it is not suitable to select status III for fault diagnosis of Q_2. The fault adjacency matrix of status I when Q_2 is an open-circuit is

$$\mathbf{A}_{1\text{-}Q_2\text{-}O} = \begin{bmatrix} 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.31}$$

The original current path 1-2-3-6 in status I does not exist based on Equation 9.31. If $i_L > 0$ when the fault occurs, the inductor current i_L will flow through the current path 5-4-3-6, then $v_o = v_{36} = v_{56} = -\frac{V_{DC}}{2}$, $v_{Q1} = v_{12} = 0$, and $v_{Q4} = v_{45} = 0$. But if $i_L = 0$ at this moment, there will be no current path, $v_o = 0$, $v_{Q1} = v_{12} = 0$, and $v_{Q4} = \frac{V_{DC}}{3}$, because Q_1 is on and Q_3, Q_4, D_6 are all turned off.

9.5.3.3 D_6 Open-Circuit

Assuming that D_6 is an open-circuit, that is, $a_{46} = 0$. Because D_6 conducts only in status IV under normal conditions, the fault adjacency matrix of status IV when D_6 is an open-circuit becomes

$$\mathbf{A}_{4\text{-}D_6\text{-}O} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.32}$$

The original current path 3-4-6 in status IV does not exist due to $a_{46} = 0$. If $i_L < 0$ when D_6 is broken, a new current path 3-2-1-6 will appear, and then $v_o = v_{16} = \frac{V_{DC}}{2}$ and $v_{Q1} = 0$, because Q_3 is conducting during status IV, $v_{Q4} = v_{15} = V_{DC}$. But if $i_L = 0$ at the same moment, no current path exists, then $v_o = 0$ and $v_{Q1} = v_{Q4} = \frac{V_{DC}}{2}$ owing to $a_{23} = 0$ and $a_{34} = 0$.

9.5.3.4 D_1 Open-Circuit

Assuming that D_1 is an open-circuit, that is, $a_{21} = 0$, the adjacency matrix of status II turns out to be

$$\mathbf{A}_{2\text{-}D_1\text{-}O} = \begin{bmatrix} 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 1 & 0 \end{bmatrix} \tag{9.33}$$

The original current path 3-2-1-6 in status II no longer exists, there is no freewheeling path for the inductor current, and i_L will suddenly drop to zero and a transient high voltage will be generated. Q_1 or Q_3 will break down as a result, which belongs to a cascading failure, instead of the single component failure discussed here.

9.5.3.5 Single Component Open-Circuit Criterion

Similarly, the failure criteria of other components in a diode-clamped three-level half bridge inverter can be deduced and summarized, as in Table 9.3. Based on this table,

Table 9.3 Single component open-circuit criterion in a diode-clamped three-level HB inverter

Failure component	Status	Working path	Electrical variables			
			v_o	i_L	v_{Q1}	v_{Q4}
Q_1	I	2-3-6	0	≥ 0	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{3}$
Q_2	I	5-4-3-6	$-\frac{V_{DC}}{2}$	> 0	0	0
	I		0	0	0	$\frac{V_{DC}}{3}$
Q_3	VI	3-2-1-6	$\frac{V_{DC}}{2}$	< 0	0	0
	VI		0	0	$\frac{V_{DC}}{3}$	0
Q_4	VI	3-4-6	0	≤ 0	$\frac{V_{DC}}{3}$	$\frac{V_{DC}}{2}$
D_5	III	5-4-3-6	$-\frac{V_{DC}}{2}$	> 0	V_{DC}	0
	III		0	0	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$
D_6	IV	3-2-1-6	$\frac{V_{DC}}{2}$	< 0	0	V_{DC}
	IV		0	0	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$

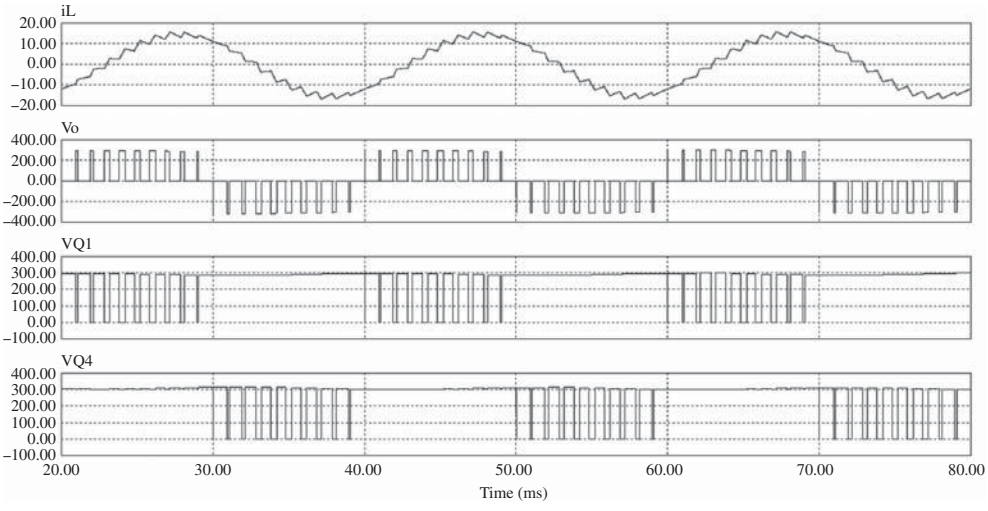


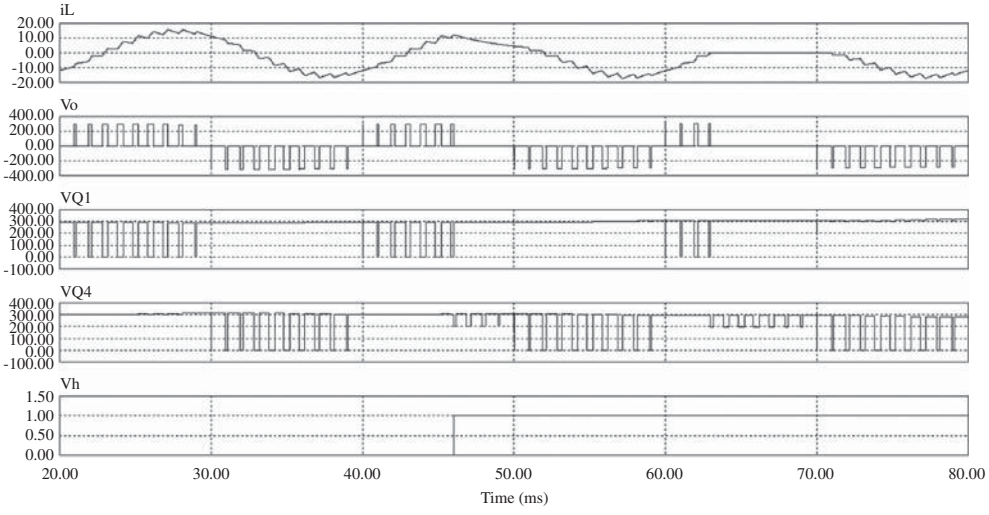
Figure 9.13 Simulation waveforms of a diode-clamped three-level HB inverter under normal operating mode

the open-circuit fault diagnosis and fault location of four switches and two clamping diodes in the inverter can be realized only by monitoring four electrical variables.

In accordance with the method described above, the characteristics of electrical variables under other kinds of component failure can be obtained, thus a structural fault diagnosis method based on the adjacency matrix of a power electronic converter is formed. This method can extract the fault features and produce the fault diagnostic results quickly and accurately by computation, so it will be useful especially for complex power electronic system.

9.5.4 Simulation Verification of Diode-Clamped Three-Level HB Inverter

In this section, the correctness of the proposed fault diagnosis method is verified in PSIM®, the simulation parameters are $V_{DC} = 600\,\text{V}$, $L_r = 20\,\text{mH}$, $R = 5\,\Omega$, and $C_1 = C_2 = 3300\,\mu\text{F}$, modulation frequency is $f = 50\,\text{Hz}$, modulation ratio is $m = 0.8$, and switching frequency is $f_s = 1\,\text{kHz}$. The simulation waveforms of i_L, v_o, v_{Q1}, and v_{Q4} under normal operating mode are shown in Figure 9.13, which is consistent with the analysis results of Table 9.2. Figure 9.14 shows the simulation results while Q_1, Q_2, Q_3, Q_4, D_5, or D_6 is an open circuit respectively, in which v_h illustrates the open-circuit time. Figure 9.14 has proved the correctness of Table 9.3, therefore, according to the values of i_L, v_o, $v_{Q1,}$ and v_{Q4} under specific statuses, the component which is an open-circuit can be judged, and the feasibility of failure diagnosis based on adjacency matrix has been verified.



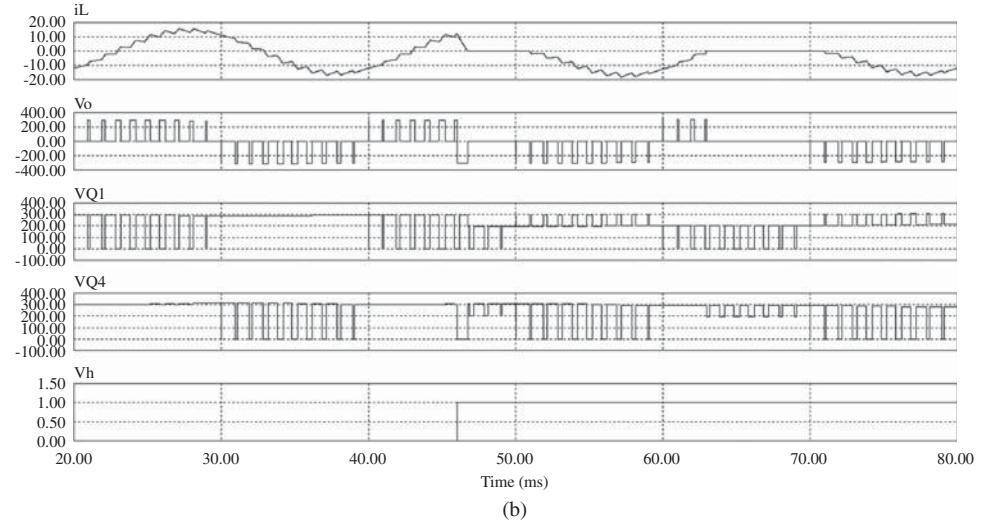
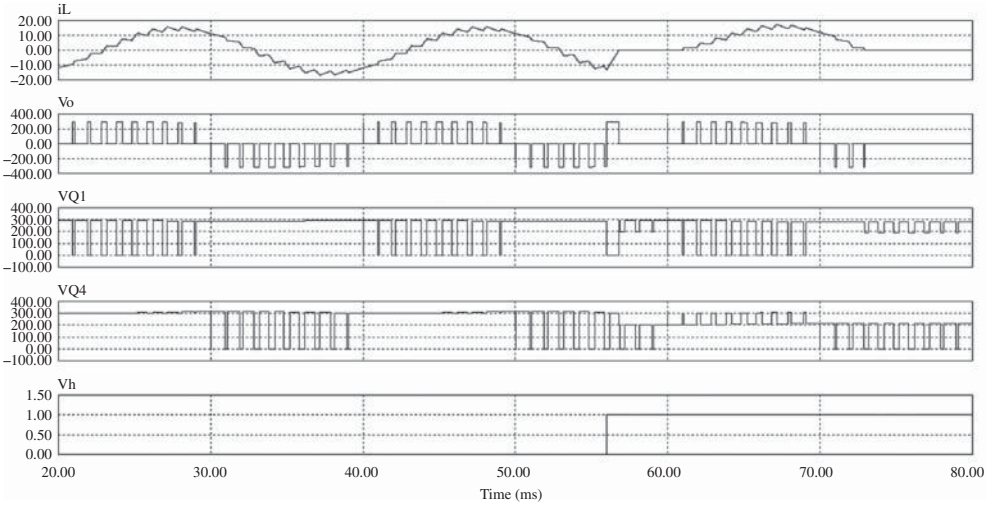


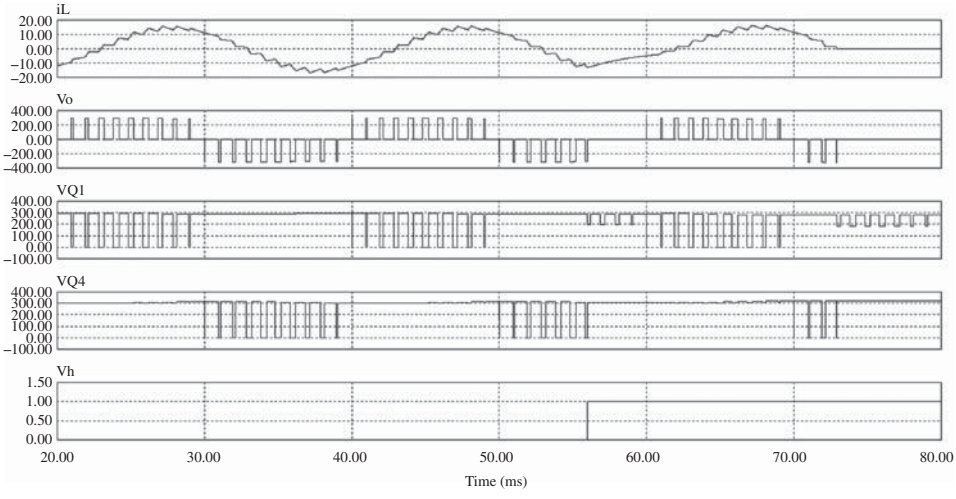
Figure 9.14 Simulation waveforms of diode-clamped three-level HB inverter when a different component is open-circuit: (a) Q_1 is open-circuit; (b) Q_2 is open-circuit; (c) Q_3 is open-circuit; (d) Q_4 is open-circuit; (e) D_5 is open-circuit; and (f) D_6 is open-circuit

9.6 Summary

Sneak circuits are electrical paths that objectively exist in power electronic converters, although they do not participate in converter operation under normal operating conditions. The performance of a power electronic converter can be improved or new functions can be realized by purposefully inserting sneak circuit paths during the



(c)

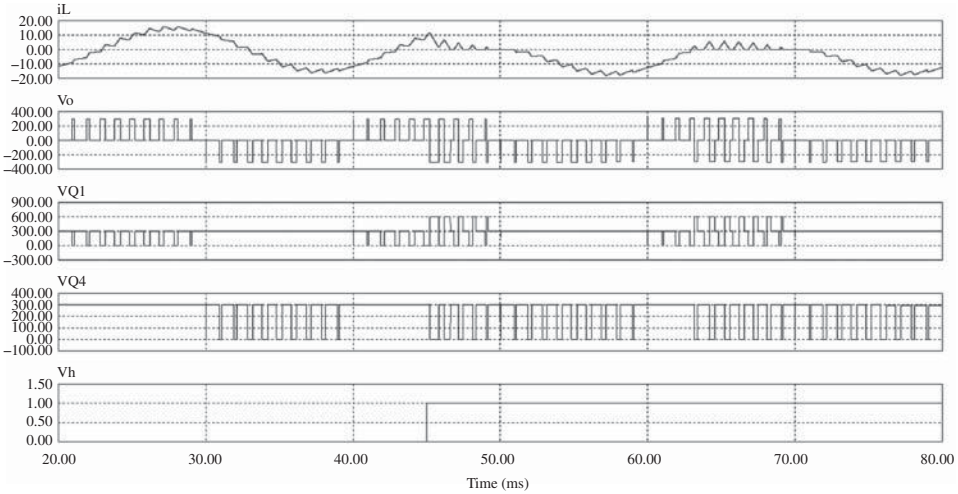


(d)

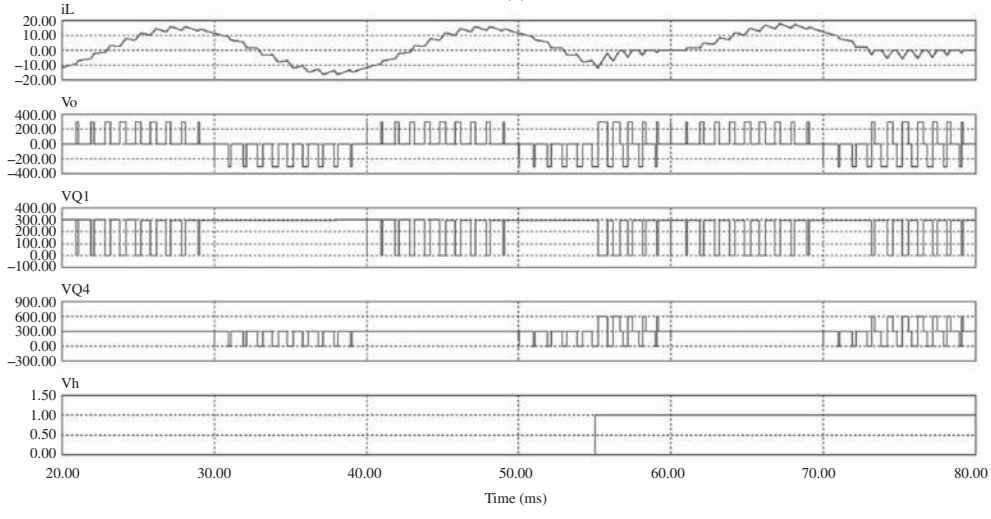
Figure 9.14 (*continued*)

normal operating process. On the other hand, the proposed sneak circuit path analysis method will contribute to a further understanding of topological structures and operating mechanisms of power electronic converters, also providing a reference for topology reconstruction and failure diagnosis of power electronic converters.

This chapter introduces how to make use of sneak circuits to improve the converter performance, realize topology reconfiguration, design new functions, and diagnose



(e)



(f)

Figure 9.14 (*continued*)

some faults of the power electronic converter concretely with some examples, which is conducive to promoting the use of sneak circuits and analysis methods in power electronic converters.

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Index

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