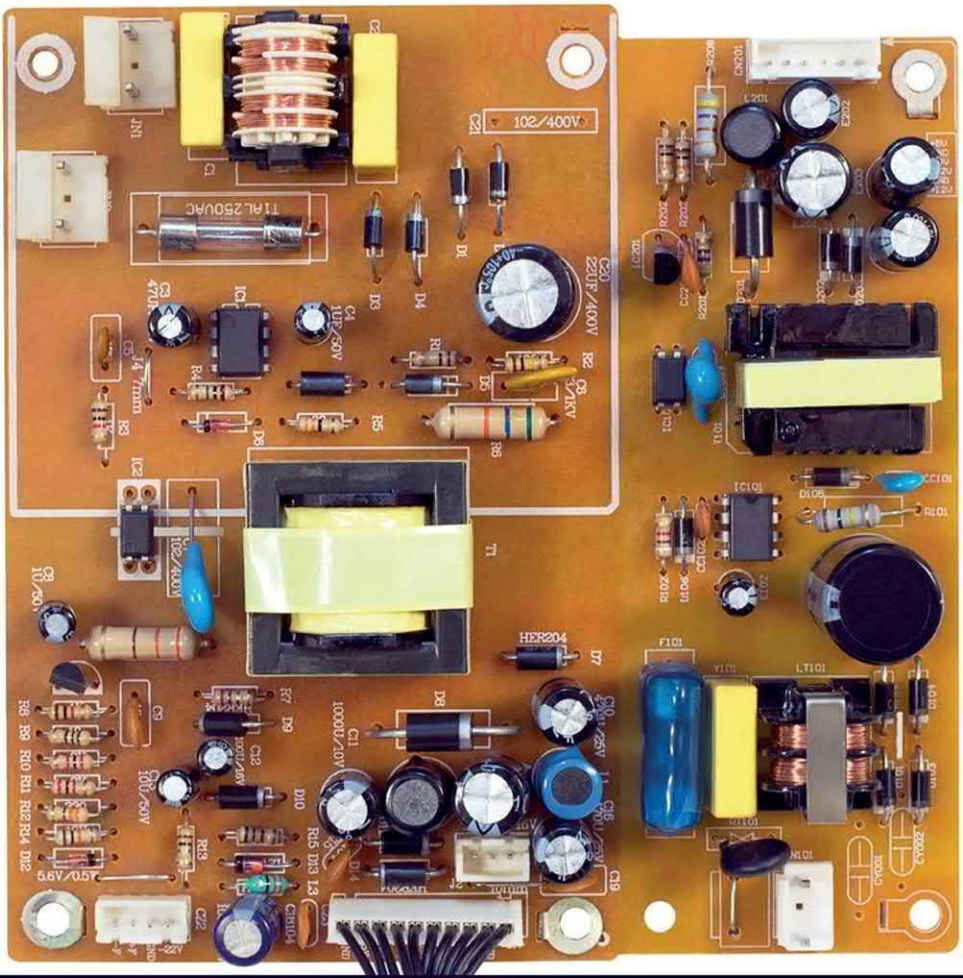


# SIMULATION OF POWER ELECTRONICS CONVERTERS USING PLECS®

FARZIN ASADI
KEI EGUCHI

# Simulation of Power Electronics Converters Using PLECS®

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# Dedication

**In loving memory of my mother, Khorshid Tahmasebi (1950-2019), always on my mind, forever in my heart.**

**Farzin Asadi**

**Dedicated to my lovely family.**

**Kei Eguchi**

# Preface

Power electronic systems are widely used today to provide power processing for applications ranging from computing and communications to medical electronics, appliance control, transportation, and high-power transmission. The associated power levels range from milliwatts to megawatts.

Modeling and simulation are essential ingredients of the analysis and design process in power electronics. They help a design engineer gain an increased understanding of circuit operation. With this knowledge the designer can, for a given set of specifications, choose a topology, select appropriate circuit component types and values, estimate circuit performance, and complete the design by ensuring that the circuit performance will meet specifications even with the anticipated variations in operating conditions and circuit component values.

Power electronics systems are nonlinear variable structure systems. They involve passive components such as resistors, capacitors, and inductors, semiconductor switches such as thyristors and MOSFETs, and circuits for control. The analysis and design of such systems presents significant challenges. Fortunately, increased availability of powerful computer and simulation programs makes the analysis/design process much easier.

PLECS® (Piecewise Linear Electrical Circuit Simulation) is one of the modern circuit simulators developed by Plexim® (www.plexim.com). Using PLECS, simulation of power electronics converters can be done easily in a user-friendly environment. PLECS has a rich component library. Its library contains electrical components (resistors, inductors, capacitors, semiconductor switches, OP-AMPs, electrical machines, etc.), magnetic components (magnetic cores, air gap, winding, mmf source, etc.), thermal components (heat sink, thermal resistor/capacitor, thermometer, etc.), mechanical components (force/speed/position sensor, mass, spring, mechanical loads, etc.). PLECS simulation runs quite fast, as well. PLECS has another nice aspect: the trial version of PLECS can be used free of charge for period of 1 month.

PLECS comes in two versions: standalone and Simulink® versions. Standalone version uses its own solver and it can run independently. Simulink version (as the name suggests) runs under the Simulink program and uses the Simulink solver. The Simulink version has a big advantage: when you use the Simulink version of PLECS, you can use all the Simulink blocks in your simulations. This can simplify the simulation considerably. For example, when you want to simulate a power electronics converter, which uses fuzzy logic controller, there is

no need to implement the controller block from ground up. You simply use the ready-to-use fuzzy logic controller block of Simulink.

This book tries to show you how simple you can simulate the power electronics converter circuits in PLECS environment. The prerequisite for this book is a first course on power electronics. The studied examples are selected among the most basic circuits of power electronics. All the details are shown, so you can follow the examples easily. It is highly recommended to do some hand calculations for the given examples and compare the results with the one produced by PLECS. Try to find the source of discrepancy if hand analysis and simulation results are not the same. This helps you to learn the concepts deeply. For instance, the voltage drop of diodes is neglected in hand analysis. So, the hand analysis result (which ignores the voltage drop of diodes) and simulation result (which considers the voltage drop of diodes) are not the same.

We want to acknowledge the Plexim for providing the access to PLECS during the writing of this book. We hope that this book will be useful to the readers, and we welcome comments on the book. Enjoy the world of PLECS!

**Farzin Asadi**
**Kei Eguchi**

Chapter 1

# Brief introduction to PLECS

## Chapter Outline



## Introduction

This chapter gives you a brief introduction about the PLECS and this book.

## 1.1 What is PLECS?

PLECS (Piecewise Linear Electrical Circuit Simulation) is a software tool for system-level simulation of electrical circuits developed by Plexim [1].

Working with PLECS is quite easy. It has a powerful component library to let you simulate almost every circuit. Your simulation can contain electrical blocks (for instance, semiconductor switch), thermal blocks (for instance, heat sink), magnetic blocks (for instance, a magnetic core), control blocks (for instance, PI controller) and mechanical blocks (for instance, gearbox). Fig. 1.1 shows the available libraries inside the PLECS. We will study these libraries in future chapters. PLECS do the simulations quite fast as well.

PLECS comes in two versions:

- Standalone version,
- Simulink® version.

As the name suggests, the standalone version works independently. You can run it without MATLAB®/Simulink. Simulink version of PLECS uses the Simulink solver as its solver, while the standalone version uses GNU Octave as its numerical engine in place of Simulink. When you work with the Simulink version, all the MATLAB/Simulink blocks are accessible to you. So, you have the power of Simulink behind you.

Plexim provides a free trial version of PLECS, which can be downloaded from https://www.plexim.com/trial. You can use it for a period of 30 days (Fig. 1.2).

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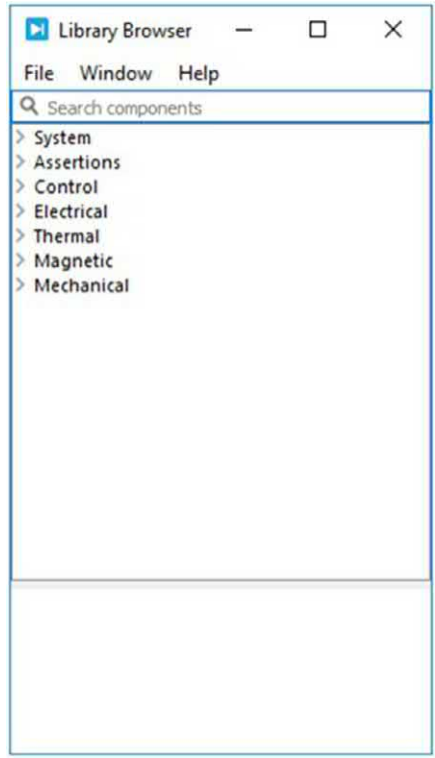


**FIG. 1.1** PLECS Library Browser.

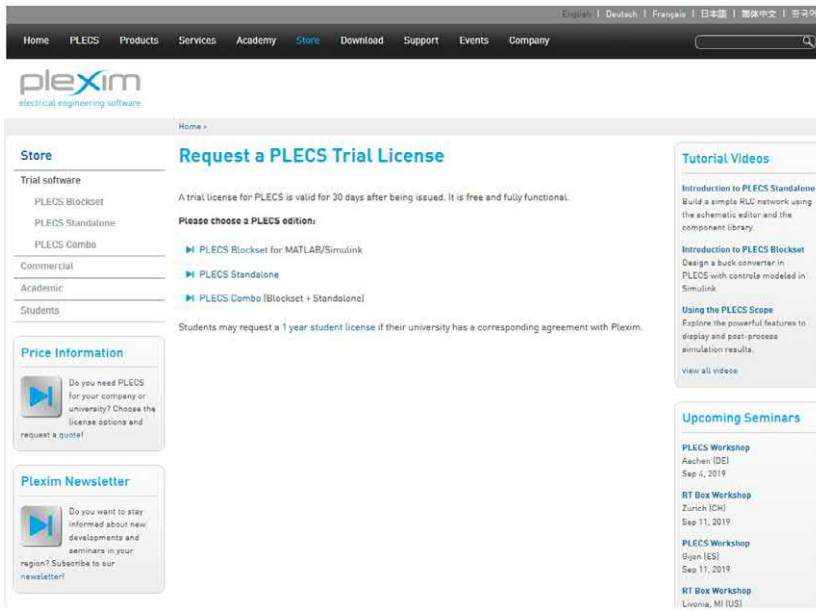


**FIG. 1.2** https://www.plexim.com/trial.

## 1.2 What is this book?

This book tries to teach you how simply you can simulate a power electronics converter in PLECS. We strongly suggest you to turn on your computer and regenerate the book examples. Here is a quick review of future chapters:

Chapter 2 shows you the basic skills required to simulate any type of circuits in PLECS. This chapter makes the basis for Chapter 3.

Chapter 3 studies simulation of different power electronics converters. It is a good idea to do some pencil-and-paper analysis for the examples given in this chapter and compare the results with the ones given by PLECS.

Chapter 4 does not gives you fish but teaches you fishing! We suggest you some ways to learn more about the world of circuit simulation using PLECS.

## References

[1] PLECS user manual available online at, https://www.plexim.com/download/documentation.

## Further reading

[2] Allmeling, J.H., Hammer, W.P. (July 27, 1999). PLECS—piece-wise linear electrical circuit simulation for Simulink. Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. Vol. 1: 355–360.

Chapter 2

# Basics of circuit simulation with PLECS

## Chapter outline



## Introduction

This chapter studies the fundamental skills one must have when using PLECS standalone to simulate circuits. We show the required techniques using simple circuits such as resistive voltage divider and first-order RC circuit. No power converter is studied in this chapter. Power converter circuits are studied in Chapter 3.

## 2.1 Example 2.1: Resistive voltage divider

In this example, we analyze the simple circuit shown in Fig. 2.1. We want to find the resistor R2's voltage and the current drawn from the 10-V source. Using basic circuit theory, one can find the answer easily,

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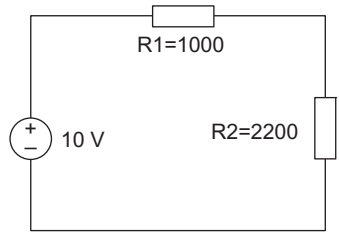


**FIG. 2.1** Schematic of example 1.

$V_{R2} = \frac{2200}{2200+1000} \times 10\,\text{V} = 6.87\,\text{V}$ and $I = \frac{10}{1000+2200} = 3.12\,\text{mA}$. We want to obtain these results using PLECS.

### 2.1.1 Preparing the simulation

After running the standalone version of PLECS, windows shown in Figs. 2.2 and 2.3 appear. We use the window shown in Fig. 2.3 to select the blocks that are required to the simulation.

In order to open a new model, click on "New model" as shown in Fig. 2.4. You can make a new model by clicking the File menu and selecting the "New model" in the Library Browser window as well.

PLECS open a new window for you. Circuit diagrams are drawn in this window (Fig. 2.5).

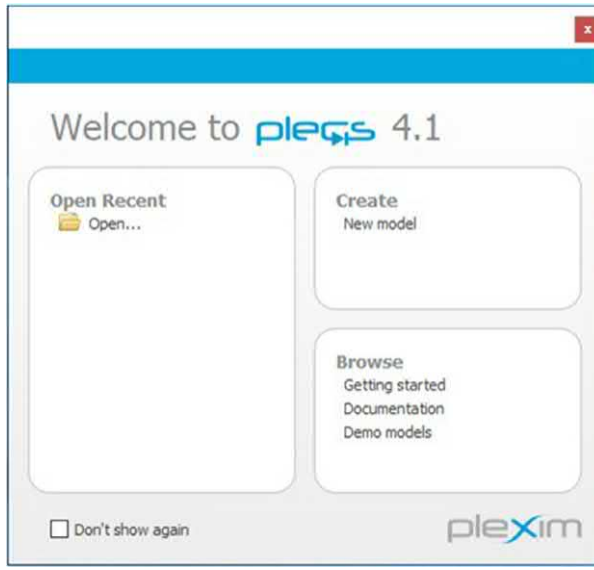


**FIG. 2.2** PLECS start page.

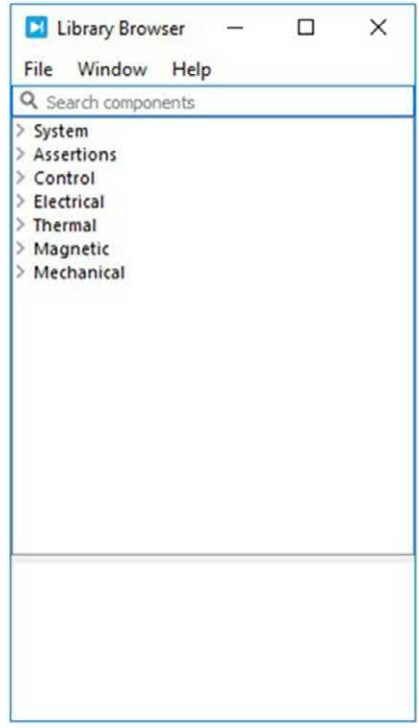


**FIG. 2.3** PLECS Library Browser.

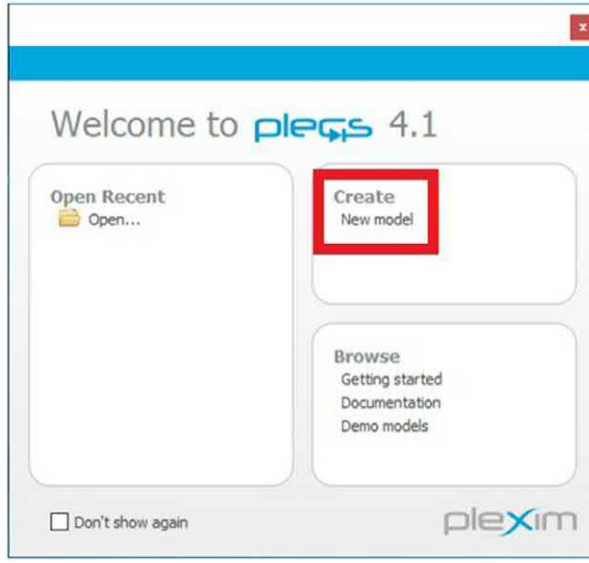


**FIG. 2.4** Creating a new model.


**FIG. 2.5** Schematic editor window.

It is a good practice to save the simulation file before starting drawing the schematic (Fig. 2.6). To do this, use the File > Save menu to save the file.

We use the name of firstCircuit for this simulation. PLECS save the files with .plecs extension (Fig. 2.7).

Use the Library Browser window to drag and drop the block named Voltage Source DC to the working area (Fig. 2.8).

After drag and drop, working area look likes that shown in Fig. 2.9.

Use the Library Browser to add a resistor to the schematic (Figs. 2.10 and 2.11).

You can rotate the resistor R1 by clicking on it and pressing the Ctrl+R on your keyboard (Fig. 2.12).

As another method, you can rotate R1 by right clicking on it selecting the Rotate (Fig. 2.13).

Add another resistor to the schematic (Fig. 2.14).

Next step is connecting the parts together. When you bring the mouse pointer near to the parts terminals, mouse pointer changes to a "+" sign. You push down the mouse left button at the source terminal and release it at the desired destination terminal (Fig. 2.15).

We can now set the components values. To do this, double click on the component and enter the desired value. When you check the small box behind the input text boxes, PLECS shows the value entered to that text box in the schematic. For example, if we check the small box behind the Voltage: box (see Fig. 2.16), we will see the schematic shown in Fig. 2.17.

We set the values of remaining parts (Figs. 2.18 and 2.19). After setting the components values, schematic looks like that shown in Fig. 2.20.

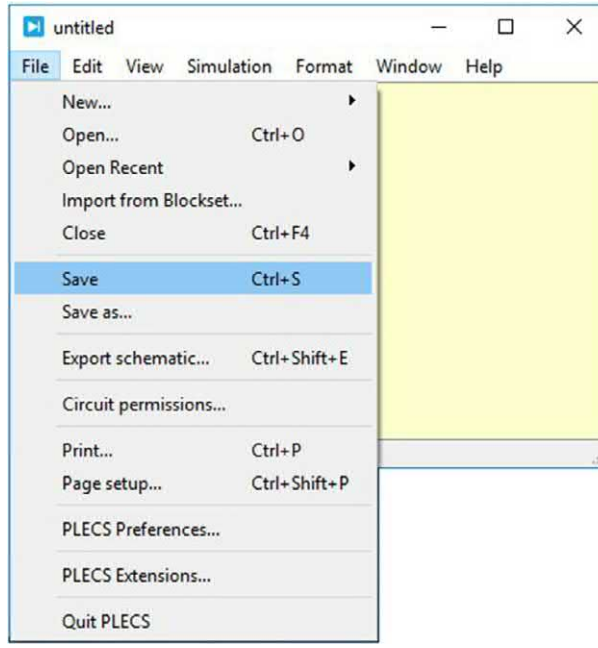


**FIG. 2.6** Saving the schematic.

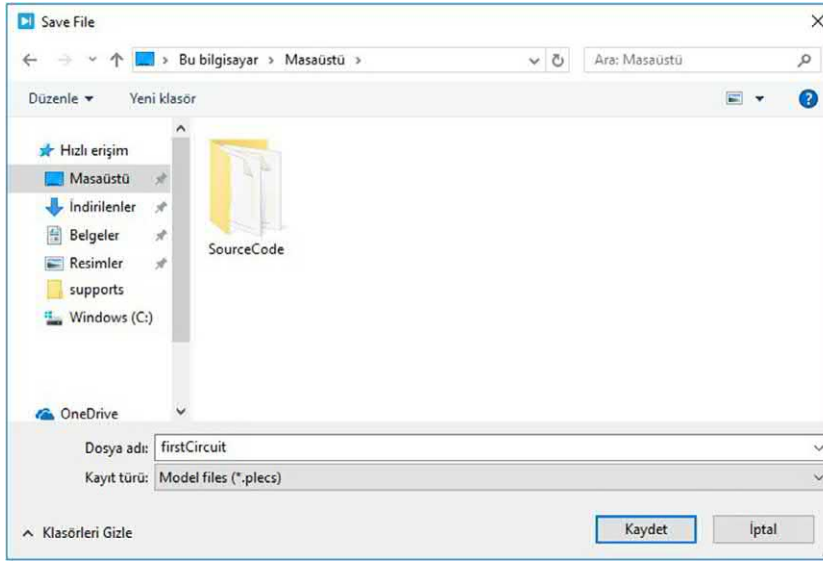


**FIG. 2.7** Specifying a path for saving the simulation file.

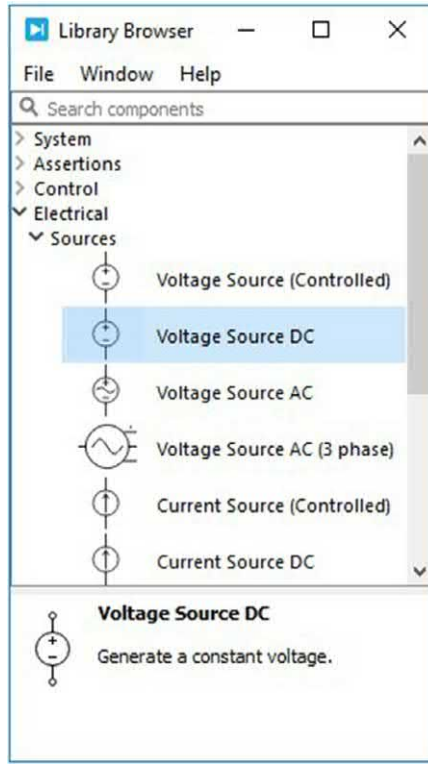


**FIG. 2.8** DC voltage source block.

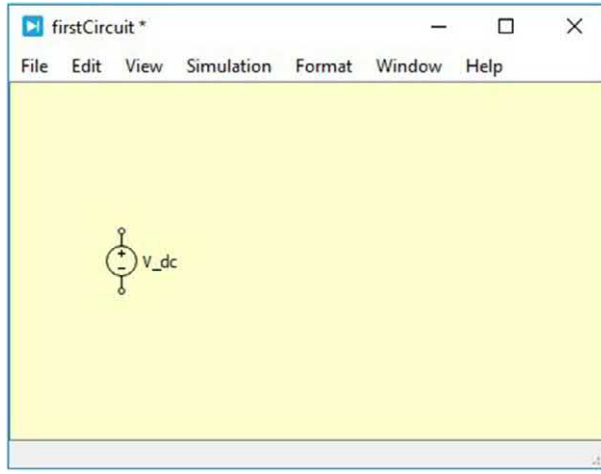


**FIG. 2.9** Placing the voltage source to the schematic.

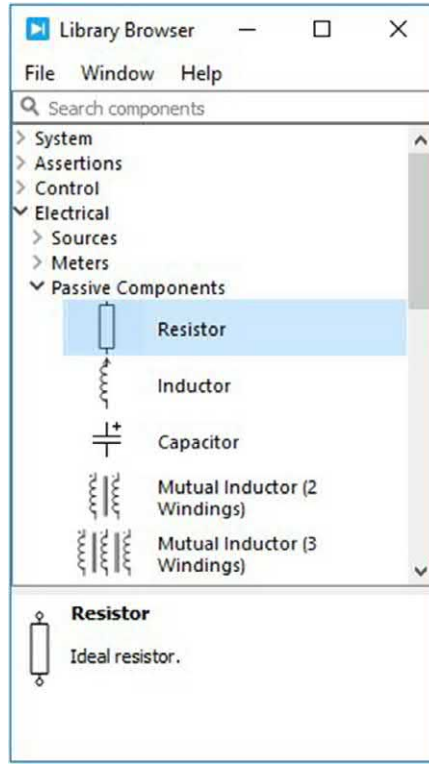


**FIG. 2.10** Resistor block.

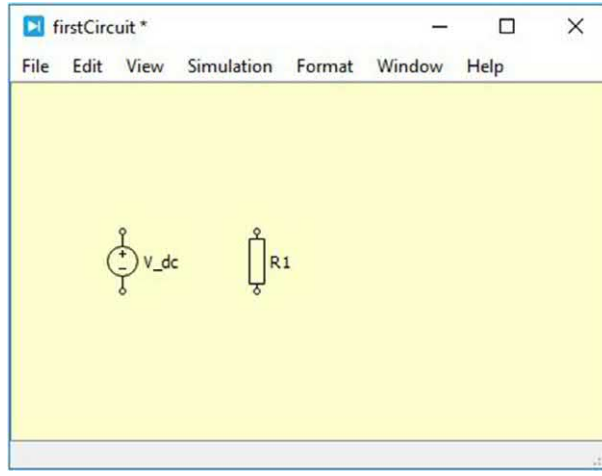


**FIG. 2.11** Placing the resistor block on the schematic.

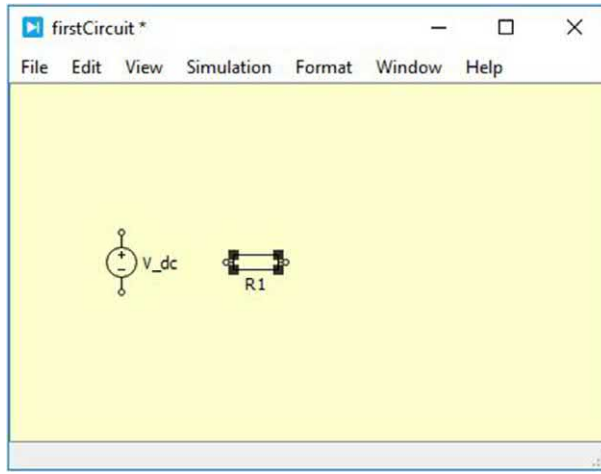


**FIG. 2.12** Rotating the resistor.

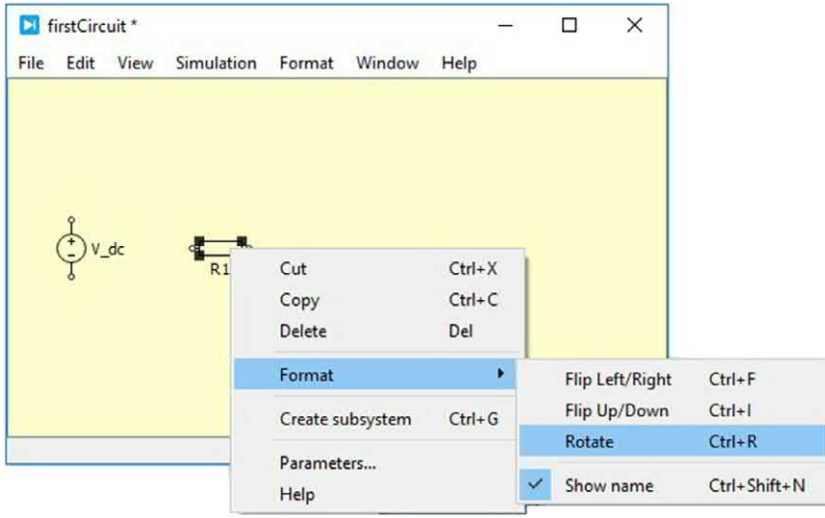


**FIG. 2.13** Rotating the resistor.

In order to measure the output voltage, we must add a voltmeter to the schematic (Figs. 2.21 and 2.22).

Output of voltmeter must be connected to a display to see the waveform. We use a scope block to observe the resistor R2 voltage (Figs. 2.23 and 2.24).

You can ground the circuit by adding a "Electrical Ground" block to your schematic. It is a good practice to use the Electrical Ground block in all of your simulations. "Electrical Ground" can be found in the system menu (Fig. 2.25).

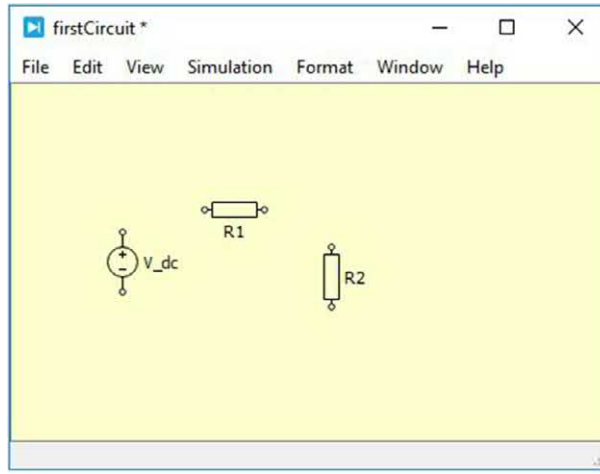


**FIG. 2.14** Placing the resistor R2 on the schematic editor.

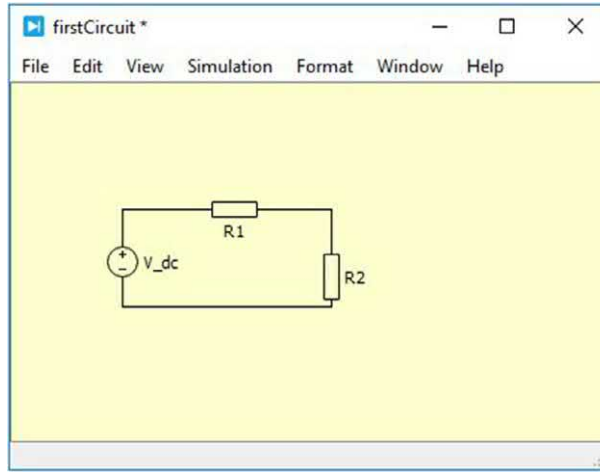


**FIG. 2.15** Connecting the parts together.

Assume that you forgot the place of "Electrical Ground" block. PLECS contains hundreds of blocks and it is not possible to memorize each blocks place. You can use the "Search components" box of Library Browser. Just type name of the block you need. For example, if you forgot the "Electrical Ground," place just type "ground" in the "Search components" box and press the Enter key on your keyboard (Fig. 2.26).

After adding the "Electrical Ground," schematic looks like that shown in Fig. 2.27.

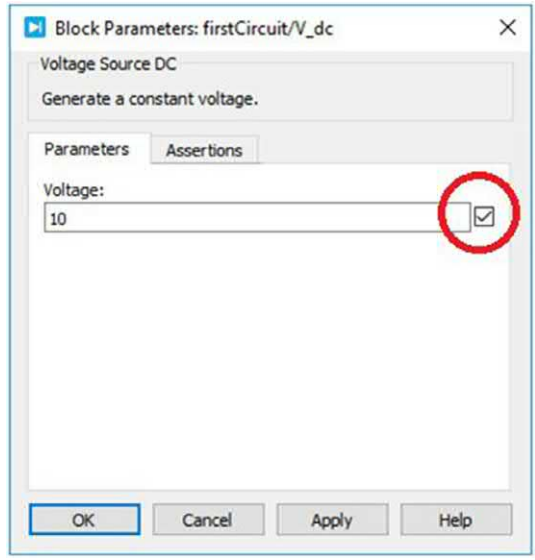


**FIG. 2.16** If you check the small box behind the textboxes, PLECS shows that value on the schematic.

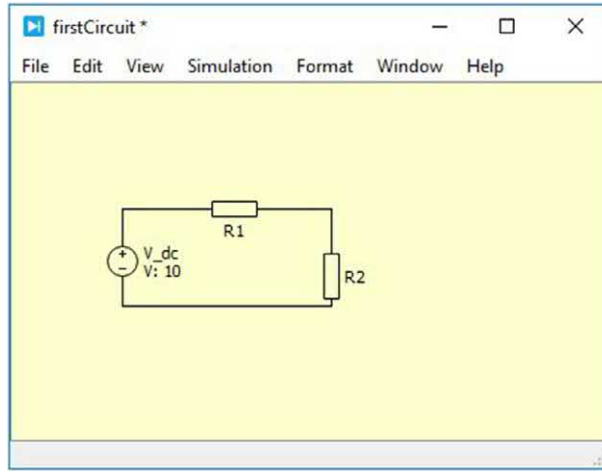


**FIG. 2.17** PLECS shows the DC voltage source value (10 V) on the schematic.

Our schematic is ready for simulation now. Before simulating the schematic, we must do some settings (Fig. 2.28). For instance we must tell PLECS to use which type of solver, how accurate results must be, simulation length, etc. These types of settings are done with the aid of "Simulation parameters…"

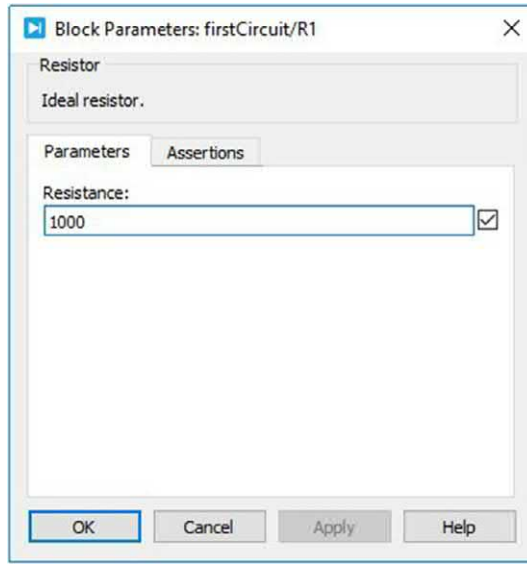


**FIG. 2.18** Specifying the value of resistor R1.

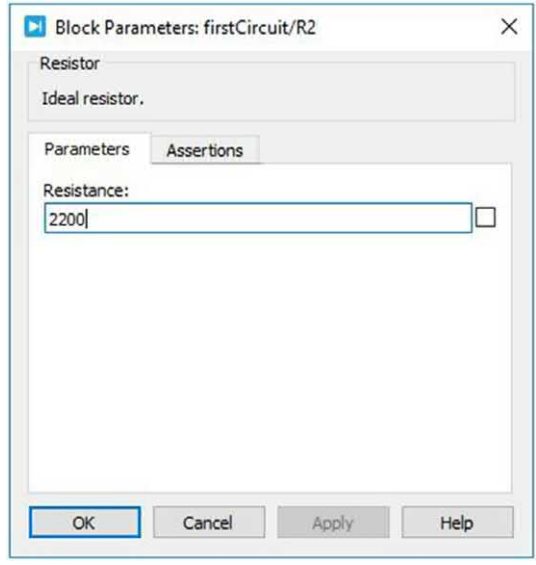


**FIG. 2.19** Specifying the value of resistor R2.

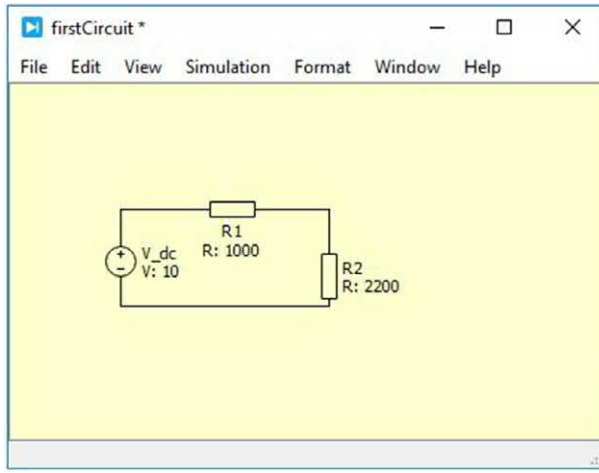


**FIG. 2.20** Schematic editor after specifying the parameter values.

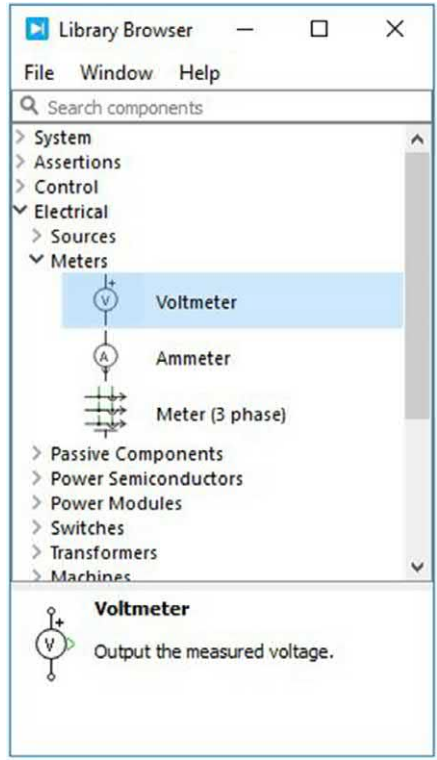


**FIG. 2.21** Voltmeter block.

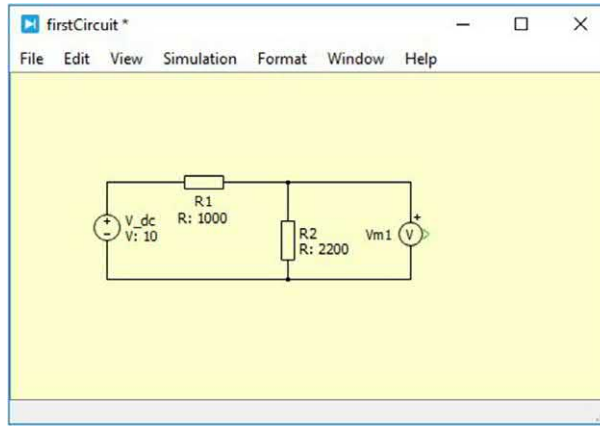


**FIG. 2.22** Connecting the voltmeter to the circuit.

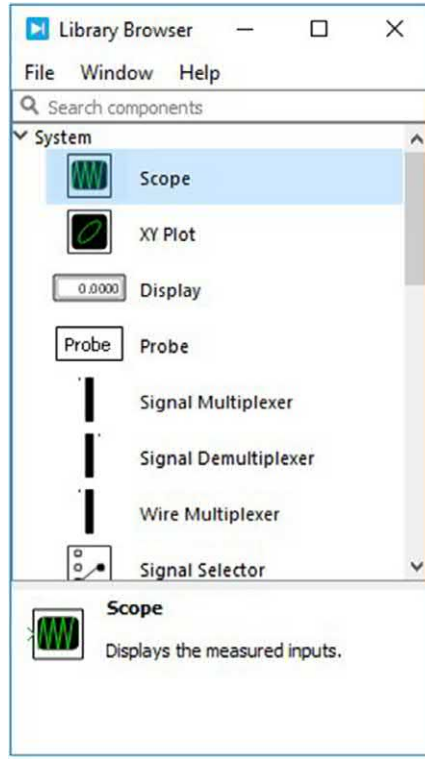


**FIG. 2.23** Scope block.

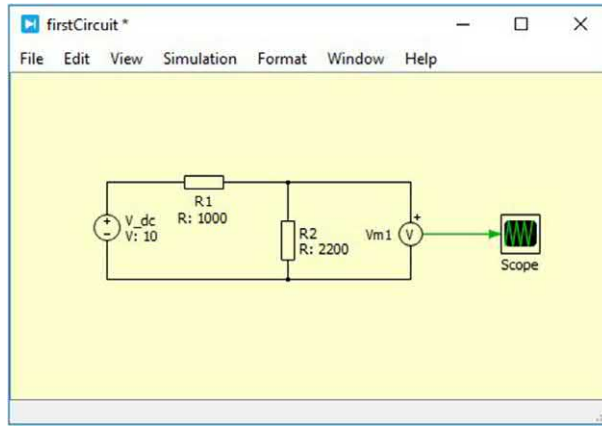


**FIG. 2.24** Connecting the scope block to the output of voltmeter.

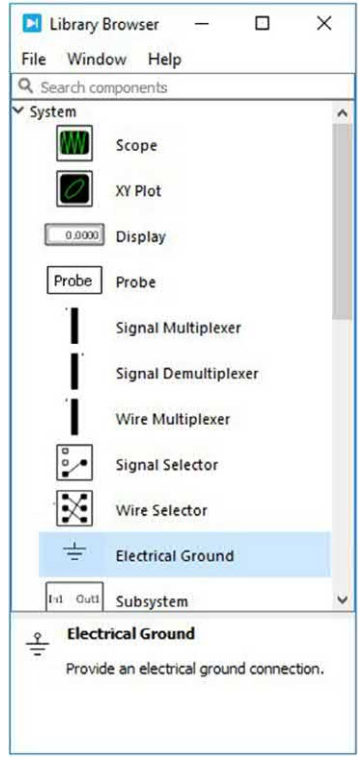


**FIG. 2.25** Electrical Ground block.

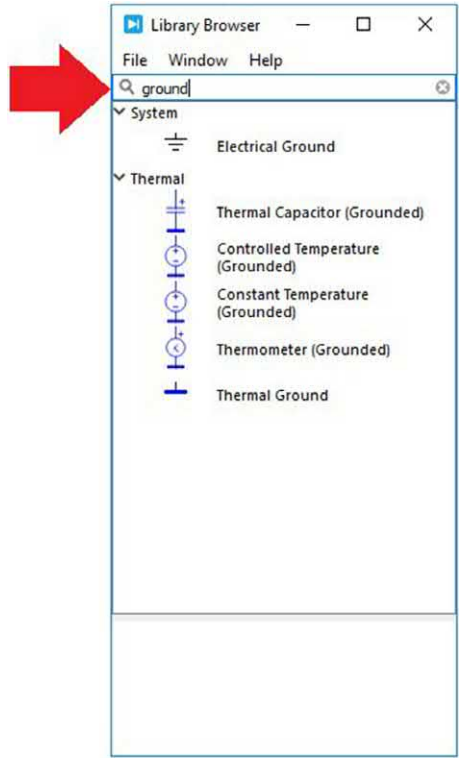


**FIG. 2.26** Searching for block.

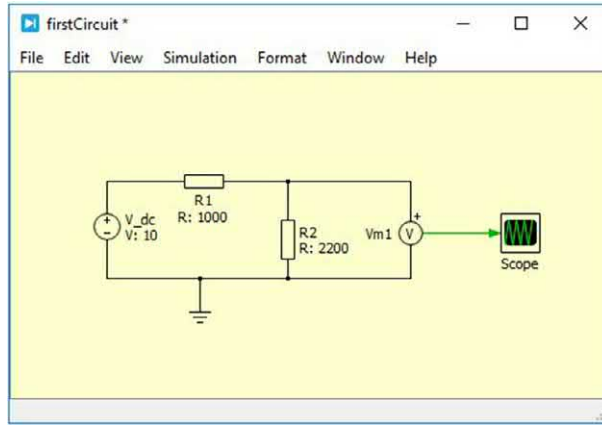


**FIG. 2.27** Grounding the circuit.

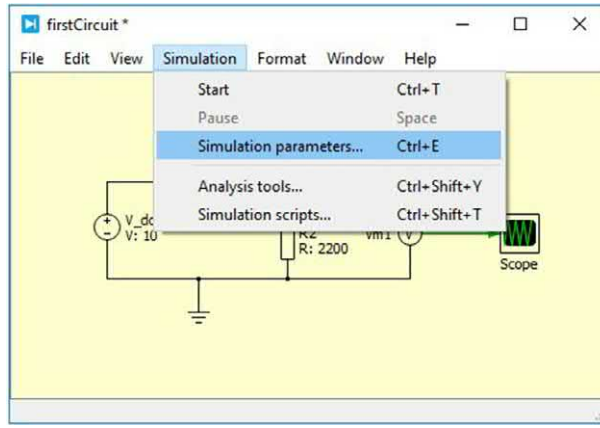


**FIG. 2.28** Simulation parameter is used to specify the simulation setting (i.e., stop time, solver type, max step size, etc.).

In this example, we want to ask PLECS to simulate the circuit for an interval of length 1 s. To do this, after clicking the "Simulation parameter," we set the "Stop time:" box to 1.0 as shown in Fig. 2.29. Leave the other settings unchanged.

To simulate the schematic, click on "Start" or press the Ctrl + T on your keyboard (Fig. 2.30).

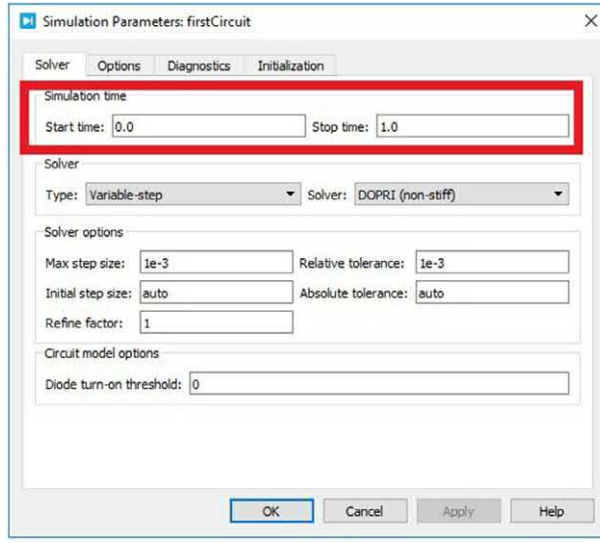


**FIG. 2.29** Simulation Parameter window.

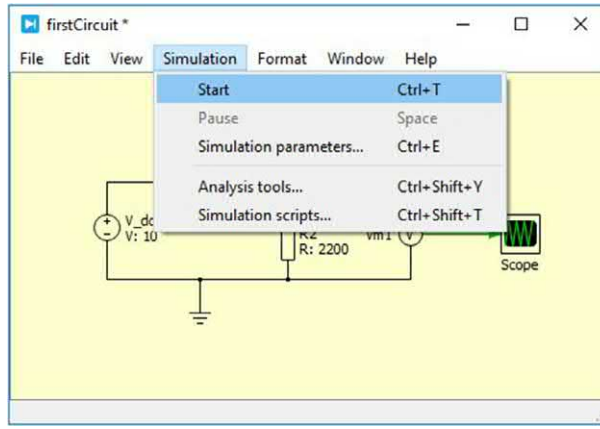


**FIG. 2.30** Starting the simulation can be done by clicking the Start.

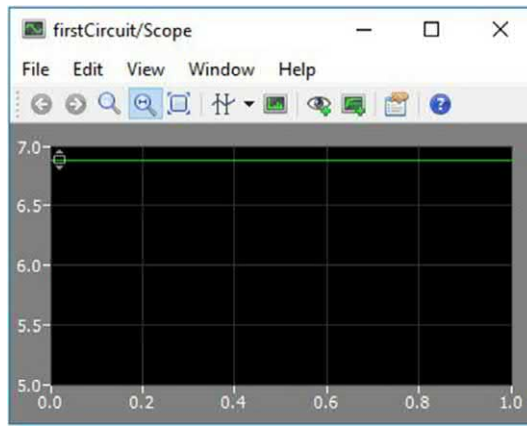


**FIG. 2.31** Simulation result (R2 voltage).

To see the resistor R2 voltage, double click the scope block. Fig. 2.31 shows the result.

### 2.1.2 Adding title to the scope

As shown in Fig. 2.31, axes have no titles. In order to add titles to the scope, click on "Scope parameters" icon. After clicking the icon, the window shown in Fig. 2.32 will appears.

Go to the "Plot 1" tab (Fig. 2.33).

Enter the desired title and axis label into the "Title:" and "Axis label:" boxes (Fig. 2.34). After clicking the "OK" button, PLECS adds the entered texts to the graph (Figs. 2.35 and 2.36).

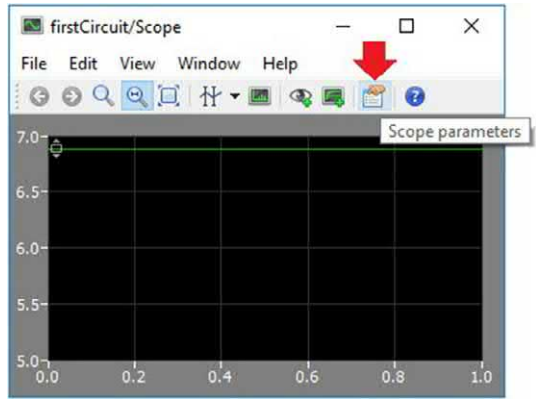


**FIG. 2.32** Scope parameters icon.

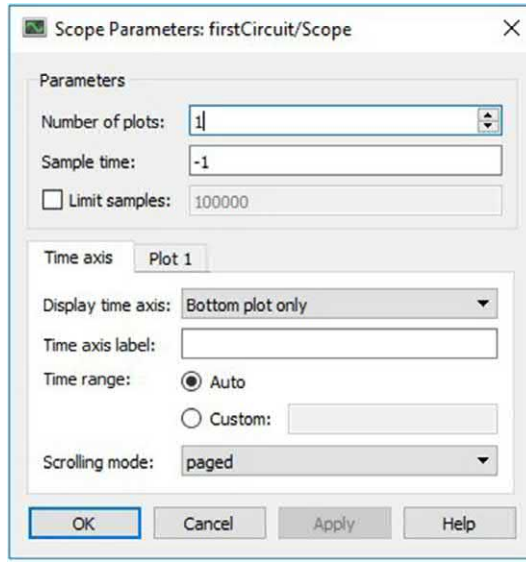


**FIG. 2.33** Scope parameters window.

### 2.1.3 Setting the axis limits

You can set the axis lower/upper bound by double clicking on them. For example, if we double click on the Y axis, the windows shown in Fig. 2.37 appears, which lets us to enter the lower and upper value for the Y axis.

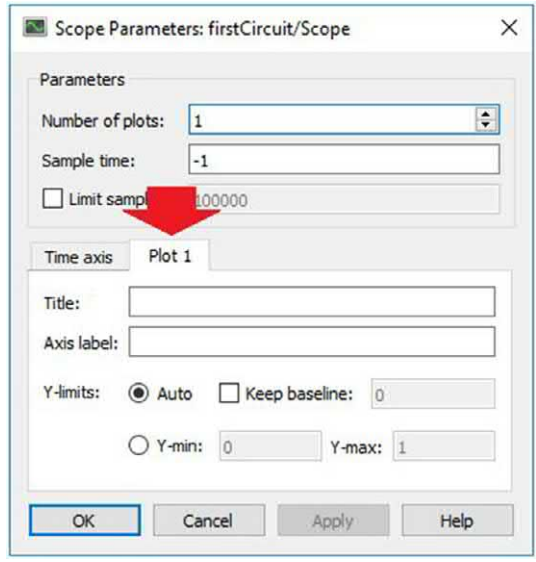


**FIG. 2.34** Plot 1 tab of Scope parameters window.

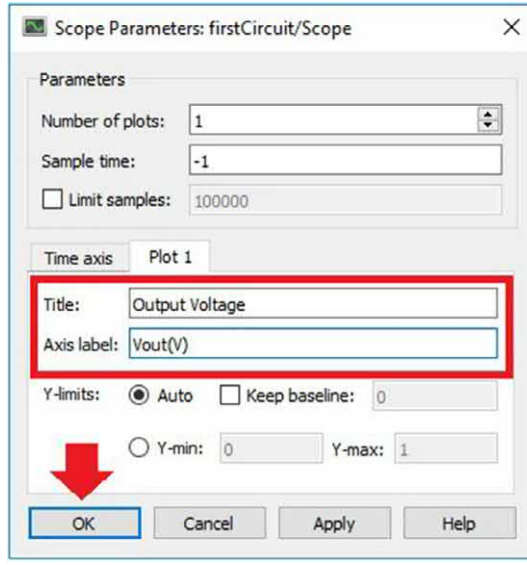


**FIG. 2.35** Specifying the desired title and axis label.

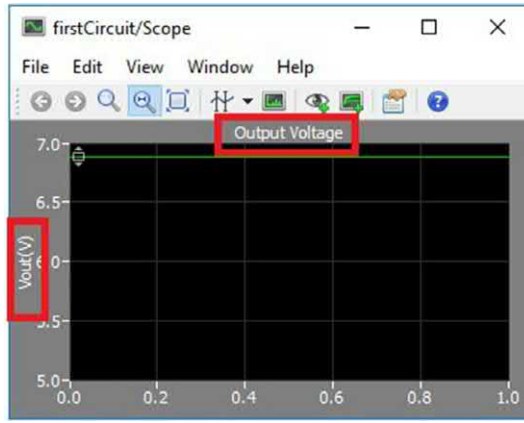


**FIG. 2.36** Specified labels are shown on the scope.

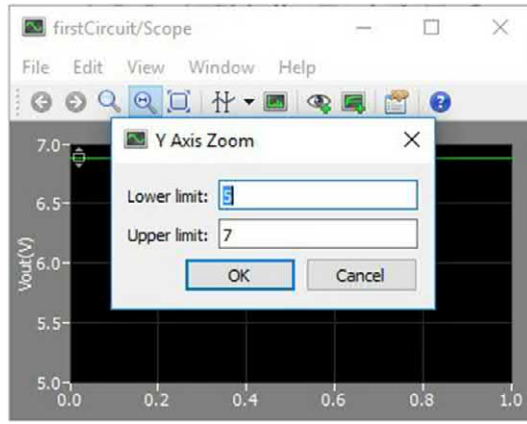


**FIG. 2.37** Y-Axis Zoom window.

### 2.1.4 Change the properties of the shown waveform

You can change the properties of the waveform shown in the scope by right clicking on the scope screen and select the "Edit curve properties." (Figs. 2.38 and 2.39)

### 2.1.5 Reading the values using cursors

You can read the waveform values easily with the cursors (Fig. 2.40).

After clicking the cursors, two cursors are added to the scope. You can bring them to the desired places (Fig. 2.41).

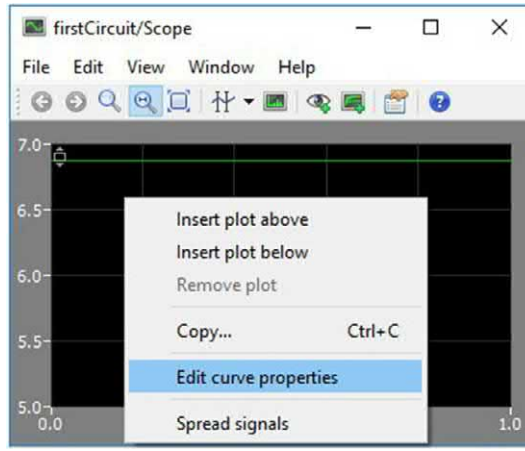


**FIG. 2.38** "Edit curve properties" is used to specify the desired curve properties.

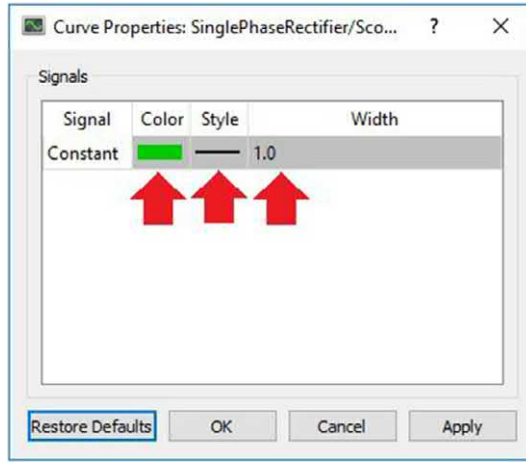


**FIG. 2.39** Specifying the desired curve properties.

Using cursors one can measure the time difference between two cursors, minimum/maximum/average/RMS/THD of waveform captured between two cursors. To do such measurements, you must click the small triangle behind the cursors icon. After clicking the small triangle, a menu will appear (Fig. 2.42).

For example, assume that we want to find the time difference between the two cursors. We must click the "Delta" (see Fig. 2.43) to find the time difference. After clicking the "Delta," PLECS shows the time difference.

Note the lock icon shown in Fig. 2.43. It is an open lock meaning that you can slide each cursor independently (Fig. 2.44).

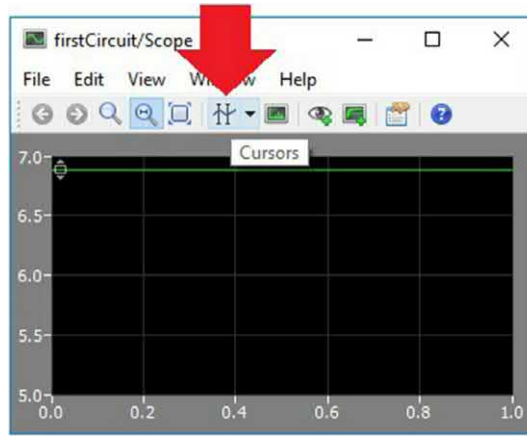


**FIG. 2.40** Cursor icon.

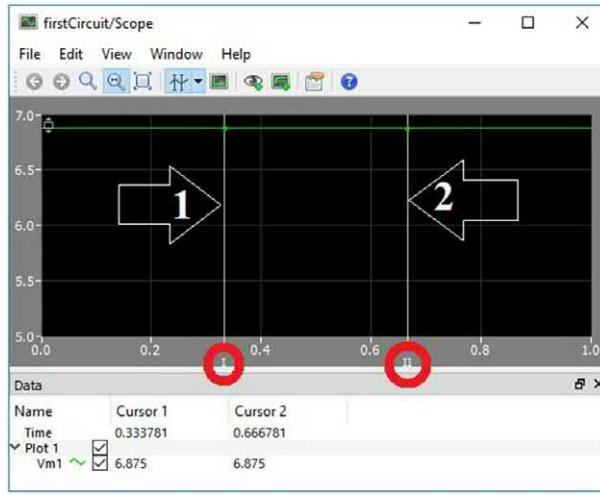


**FIG. 2.41** After clicking the cursor icon, 2 cursors are appear.

If you click on the lock icon it will change to a close lock. In this case, you can slide either of cursors, but the other one moves as well, i.e., two cursors are dependent. The difference between two cursors is constant and (in this example) is equal to 0.333 s (Fig. 2.45).

### 2.1.6 Zoom in/out

Use the magnifier icon to zoom in/out the waveform shown in the scope (Fig. 2.46).

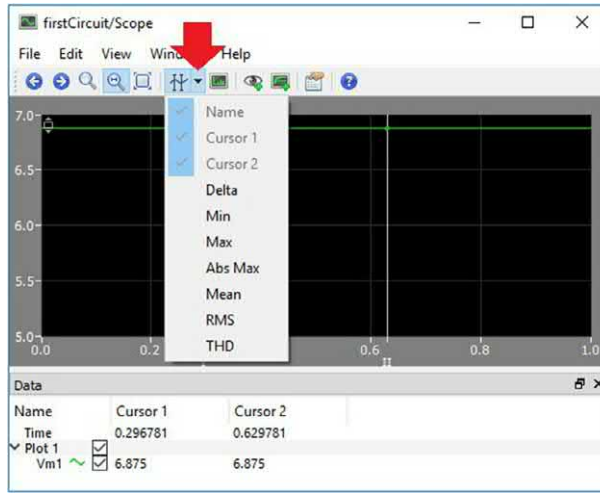


**FIG. 2.42** Menu appeared after clicking the small triangle.

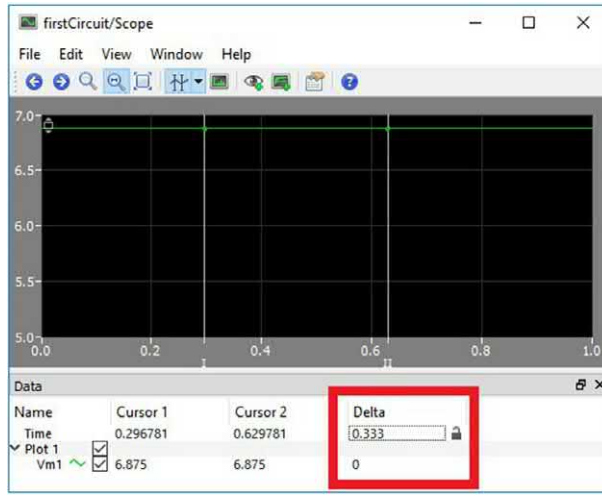


**FIG. 2.43** Difference (both time difference and voltage difference) is calculated and shown on the Data window.

For example if you want to see the [0.4 S, 0.6 S] time interval with more detail, use the  icon. After clicking the  icon, left click around the 0.4 S and move the mouse pointer toward the 0.6 S. After reaching the desired destination, release the mouse button. After releasing the mouse button, PLECS zoom into the selected region (Figs. 2.47 and 2.48).

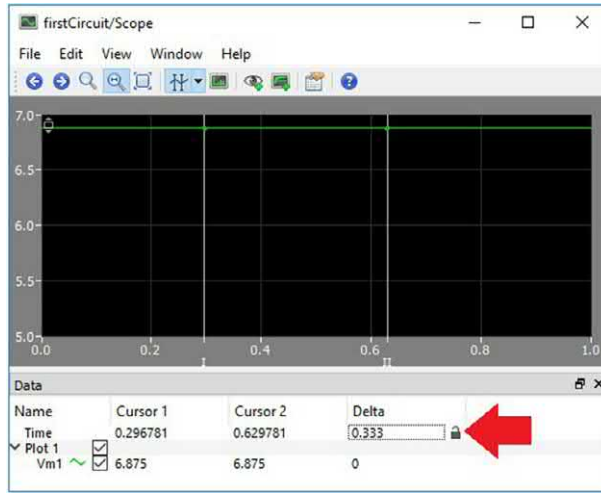


**FIG. 2.44** Open lock.

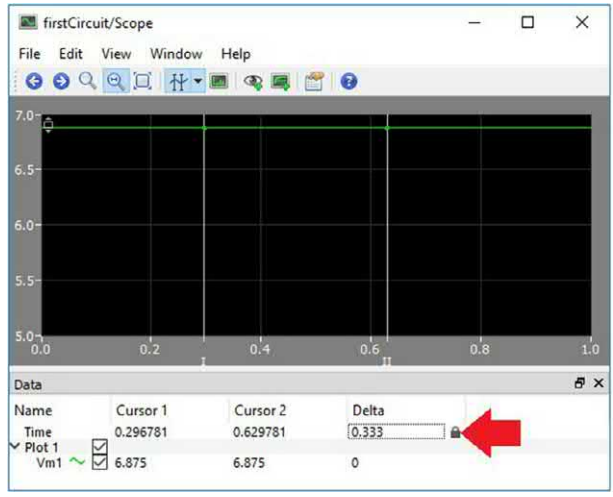


**FIG. 2.45** Closed lock.

Application of  icon is not limited to horizontal zooming. You can use it to do vertical zooming as well (Figs. 2.49 and 2.50).

PLECS memorizes the settings of scope each time you do zooming. Use the  and  icons to move between different views. For example, if you do zooming and you are not happy with the new view, you can return to previous view simply by clicking on the return icon (  ) (Fig. 2.51).

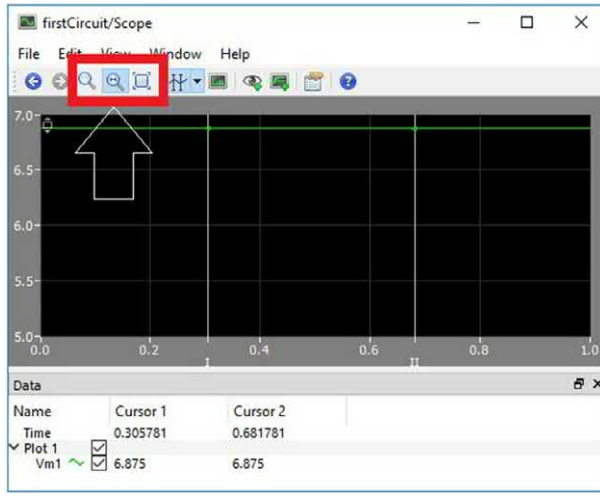


**FIG. 2.46** Zoom icons.

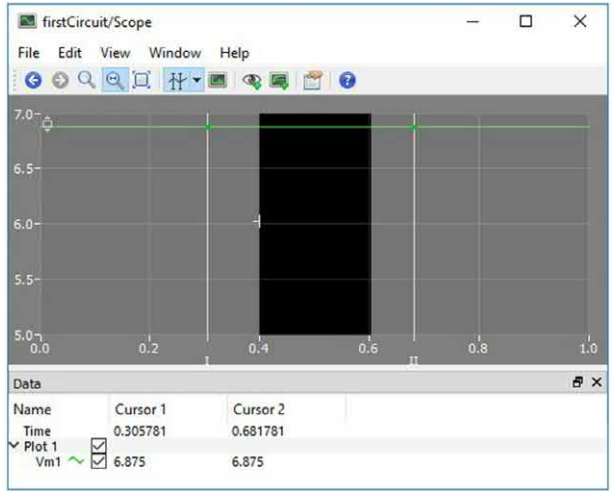


**FIG. 2.47** Selecting the 0.4–0.6 s interval.

### 2.1.7 Exporting the scope block waveforms

You can simply export the waveform shown in the scope by clicking "Export" and select the desired format (Fig. 2.52).

If you want to write a report and show the obtained waveforms, use the "as Bitmap…". It makes a .bmp file for you, which you can put it easily into your report. After clicking the "as Bitmap…," the window shown in Fig. 2.53 will

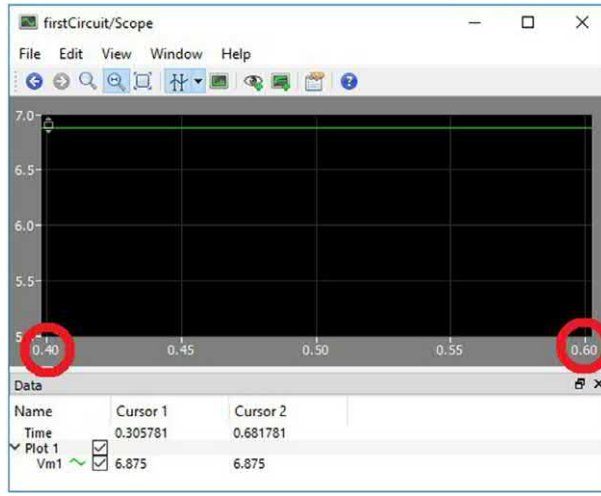


**FIG. 2.48** PLECS zoom into the selected region.

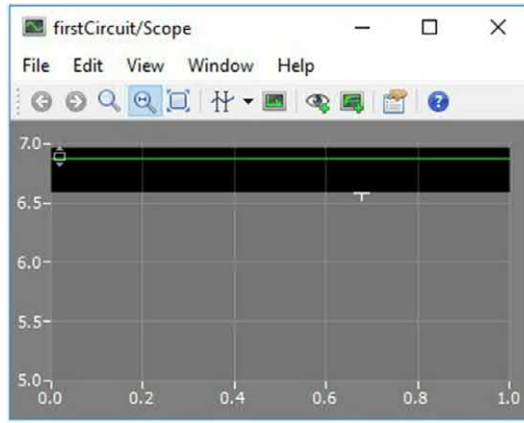


**FIG. 2.49** Zooming the Y axis.

appear. Enter the desired width and height into the "Width" and "Height" boxes. Use the "Image settings" section to set the produced image quality. Generally, "Resolution (dpi): 72" and "Quality (0-100): 80" is good for most applications, but you can increase them at the cost of produced larger file. For instance, while "Resolution (dpi): 72" and "Quality (0 – 100): 80" produces only 8 KB, "Resolution (dpi): 600" and "Quality (0–100): 80" produces a 152-KB file.

You can copy the waveform shown in the scope into the Windows clipboard. This capability is useful when you want to edit the obtained waveform in a graphic software. In order to copy the waveform into the clipboard, click The "Copy…" (Fig. 2.54).

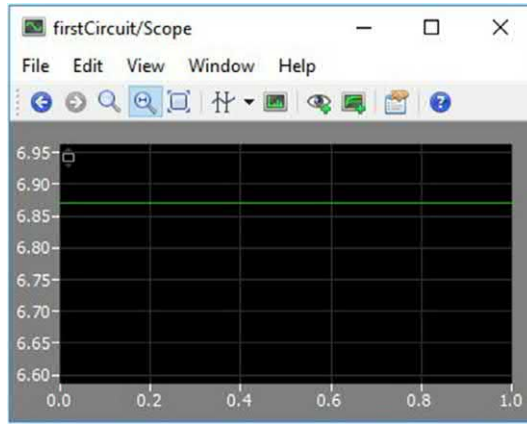


**FIG. 2.50** Zoomed Y axis.

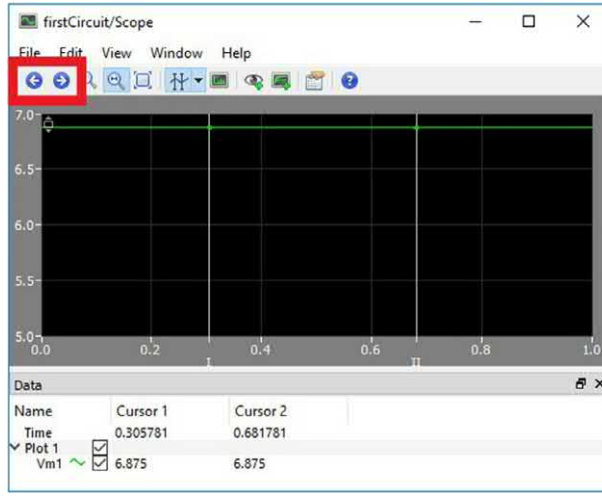


**FIG. 2.51** Using the arrows, you can move between the different views.

After clicking the "Edit…," the window shown in Fig. 2.55 will appear. Do the desired settings and click on the "Copy to Clipboard" button.

### 2.1.8 Exporting the drawn schematic

You can export the drawn schematic easily with the "Export schematic…" (Fig. 2.56).

After clicking the "Export schematic…," the window shown in Fig. 2.57 will appear. Select the desired resolution and press the "OK" button. After

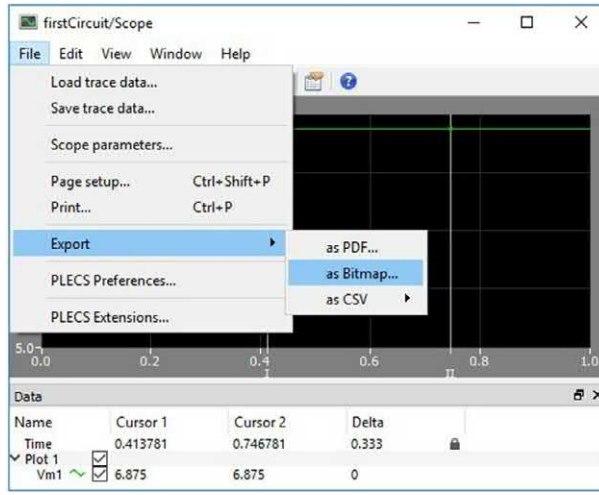


**FIG. 2.52** Exporting the scope graphs as Bitmap(.bmp) file.

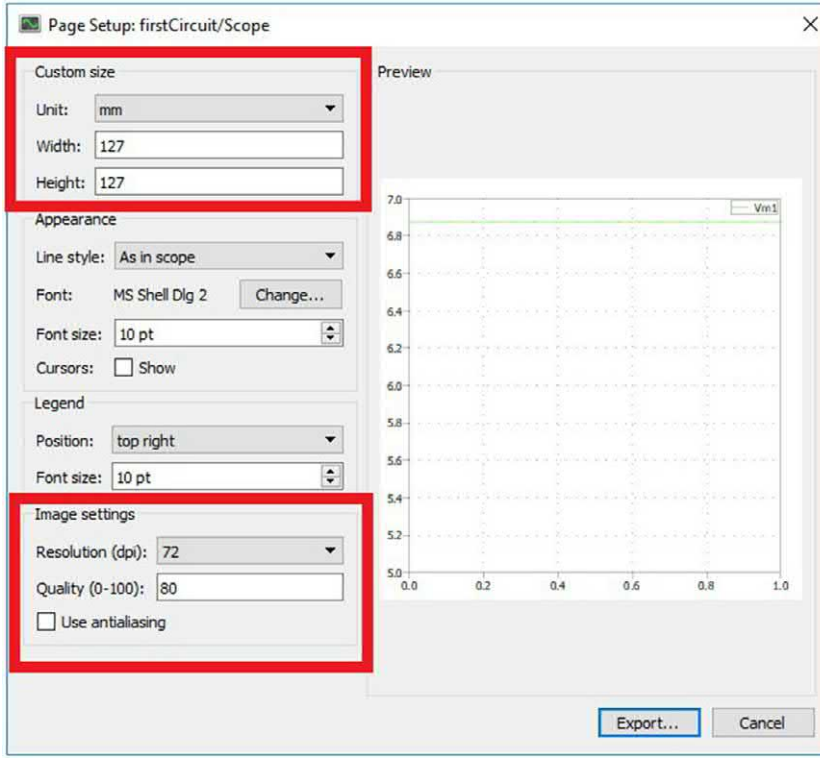


**FIG. 2.53** Page Setup window.

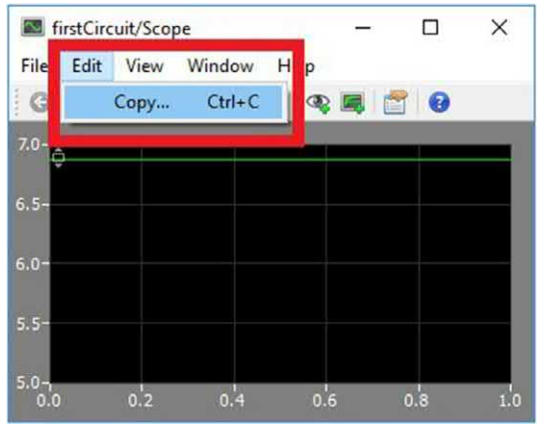


**FIG. 2.54** Copying the scope graphs into the Windows clipboard.

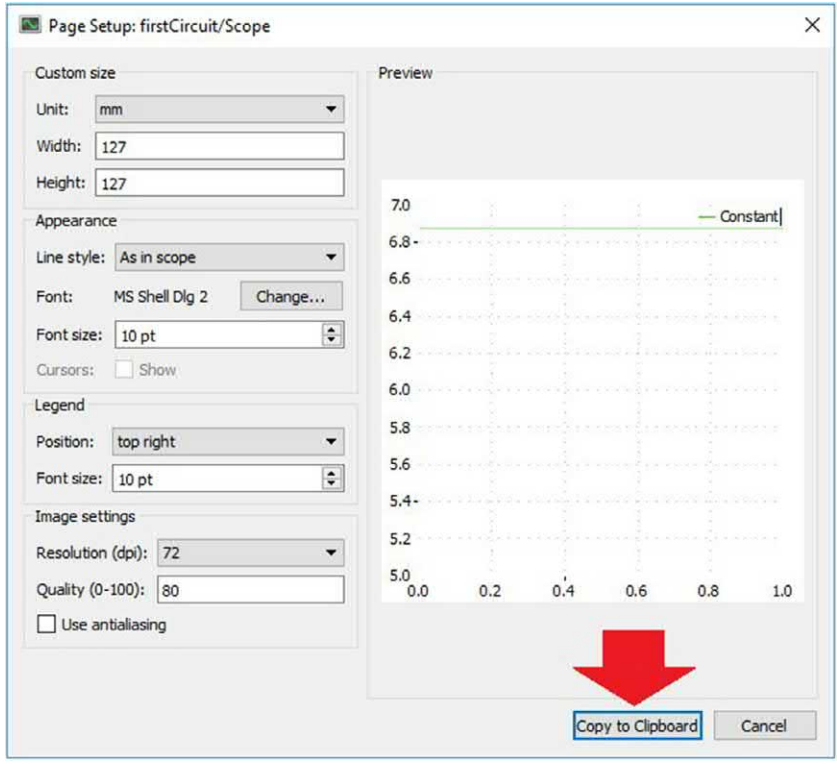


**FIG. 2.55** Page Setup window.

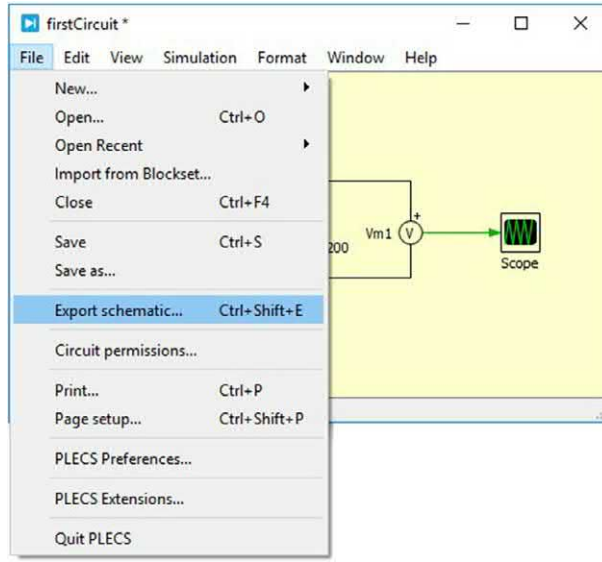


**FIG. 2.56** Exporting the schematic as graphic file.

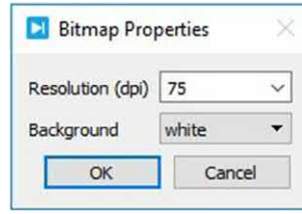


**FIG. 2.57** Bitmap Properties window.

pressing the "OK" button, you must specify a place to save the file. Exported schematic is shown in Fig. 2.58. You can use the exported graphic file for the purpose of documentation.

You can even copy the schematic to Windows clipboard. To do this, use the "Copy as image." You can paste the image in the graphical or word processor software (Fig. 2.59).

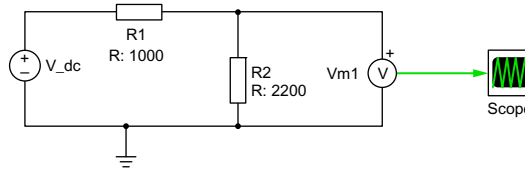


**FIG. 2.58** Exported graphic file.

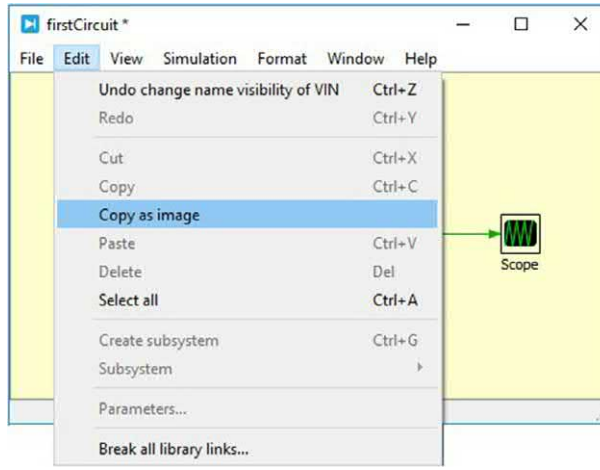


**FIG. 2.59** Copying the schematic into the Windows clipboard.

### 2.1.9 Display block

DC quantities can be displayed easily with the aid of "Display" block (Figs. 2.60 and 2.61).

### 2.1.10 Changing the block names

Selection of meaningful names for components is an important issue since it simplifies the understanding of circuit. You can change the default components names easily by double clicking on their name and writing the new name (Figs. 2.62 and 2.63).

### 2.1.11 Hiding the block names

You can ask PLECS not to show the component name if you prefer to do so. To hide the component name, simply right click on the component and uncheck the "Show name." After unchecking the "Show name," the components name will be hidden (Figs. 2.64 and 2.65).

### 2.1.12 Adding text to the schematic

You can add text to the schematic by double clicking on the schematic and writing the desired text into the appeared box (Fig. 2.66).

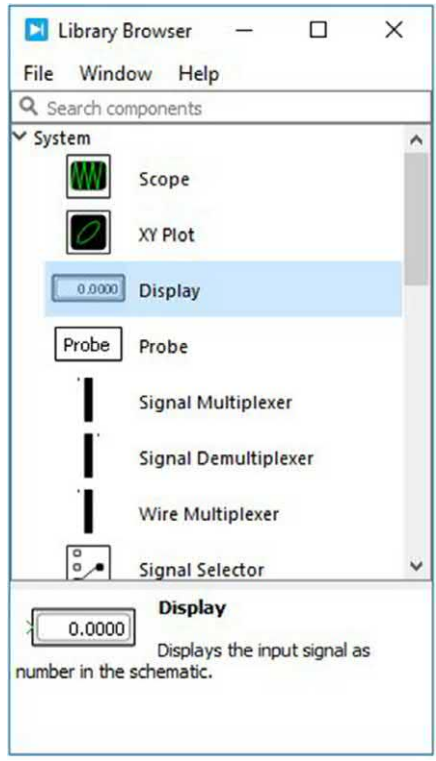


**FIG. 2.60** Display block.

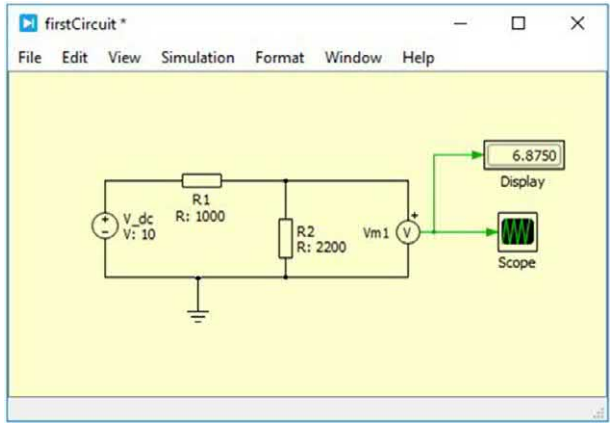


**FIG. 2.61** Adding the display block to the schematic.

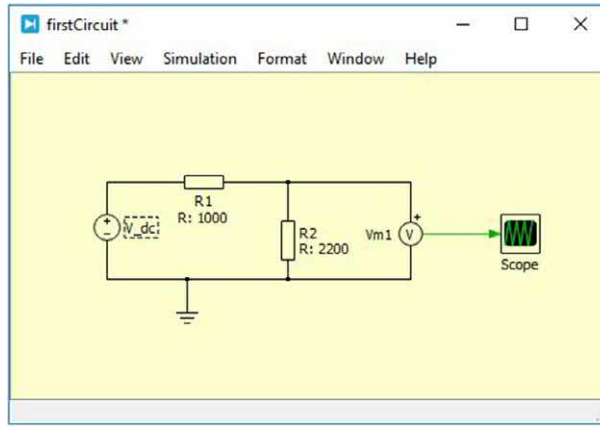


**FIG. 2.62** Renaming the components.

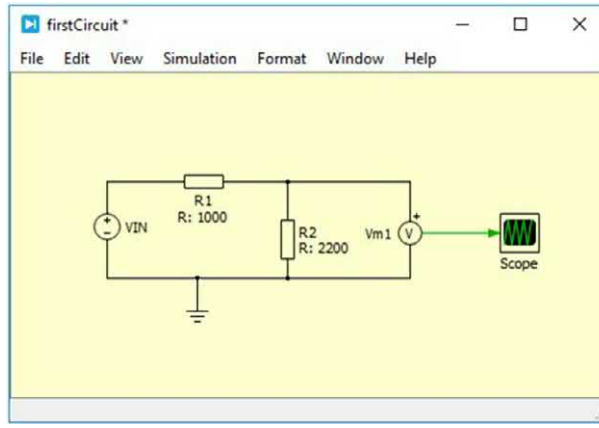


**FIG. 2.63** Schematic with new names.

### 2.1.13 Ammeter block

You can add an ammeter to the circuit in order to see the circuit current. To do so, first click on the wire connecting the source to the resistor R1. Press the keyboard "Delete" key to remove that wire (Figs. 2.67 and 2.68).

After wire has been removed, add an ammeter in its place. Connect the output port of ammeter to a scope in order to see the waveform (Figs. 2.69–2.71).

It is a good practice to select meaningful names for scopes. This makes the understanding of circuit easy. You can change the scope labels easily by double clicking on the current label ("Scope" and "Scope1" in Fig. 2.72) and writing the new label in the opened box.

If we run the simulation we obtain the result shown in Fig. 2.73.

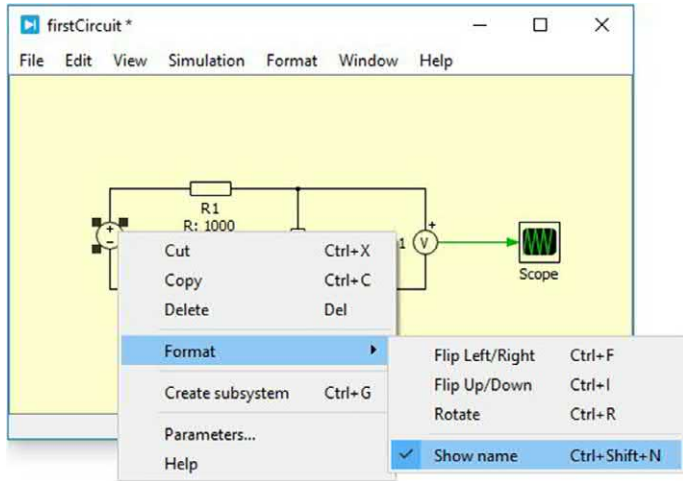


**FIG. 2.64** Show/hide the block names.

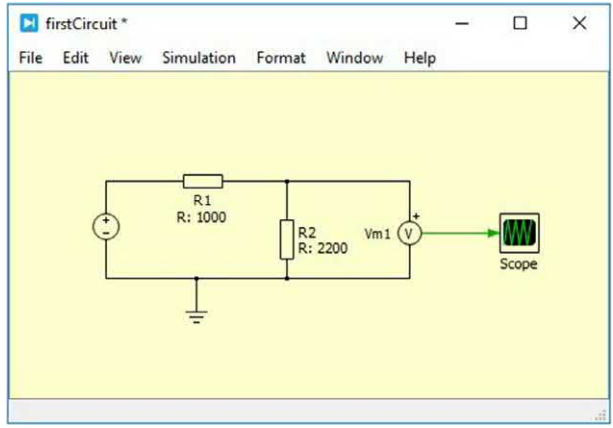


**FIG. 2.65** Input source name is hided.

If we use the icon, we can obtain a closer look of the current waveform. As expected, result is 3.12 mA (Fig. 2.74).

### 2.1.14 Wire colors

Power electronics converters are composed of a power circuit and a control algorithm. PLECS shows the power circuit components in black and control (or measurement) signals in green (Fig. 2.75).

You cannot connect components designed for power circuit to control (or measurement) signals (Fig. 2.76).

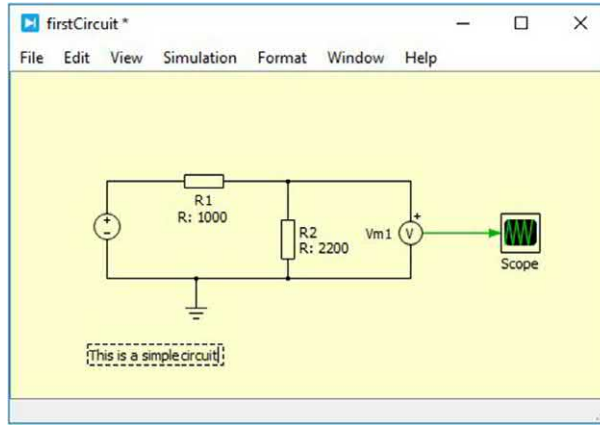


**FIG. 2.66** Adding text to the schematic.

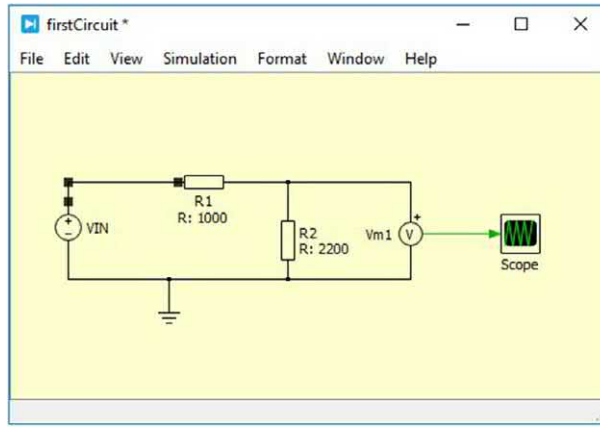


**FIG. 2.67** You can select a wire by clicking on it.

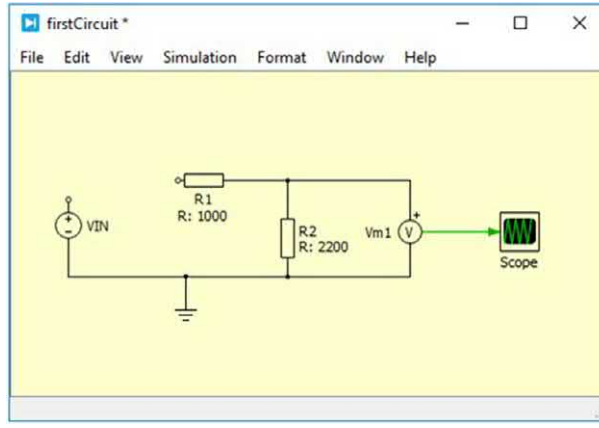


**FIG. 2.68** Remove the selected wire by pressing the Delete key on keyboard.

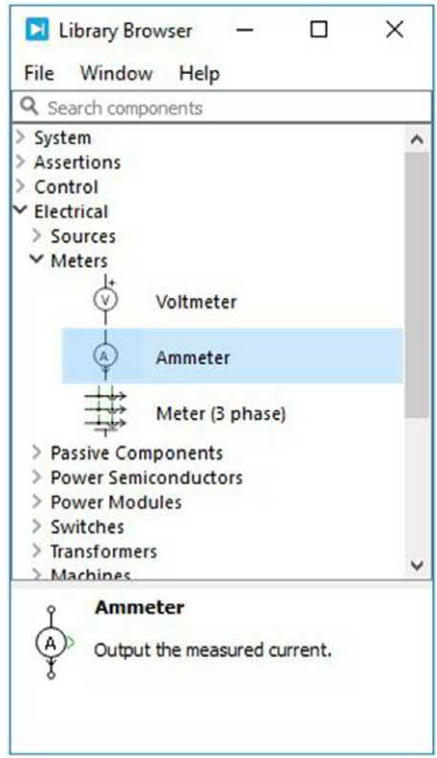


**FIG. 2.69** Ammeter block.

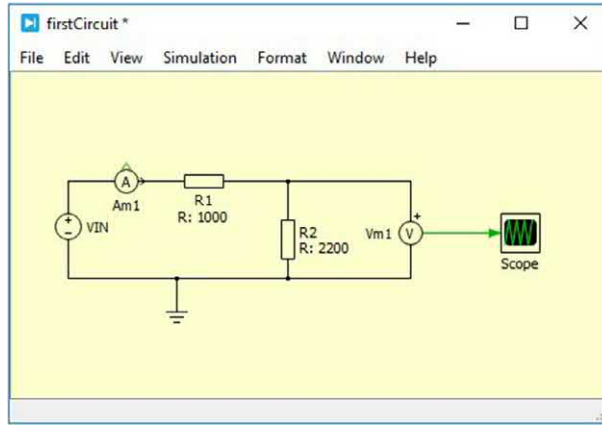


**FIG. 2.70** Adding an ammeter block to the schematic.

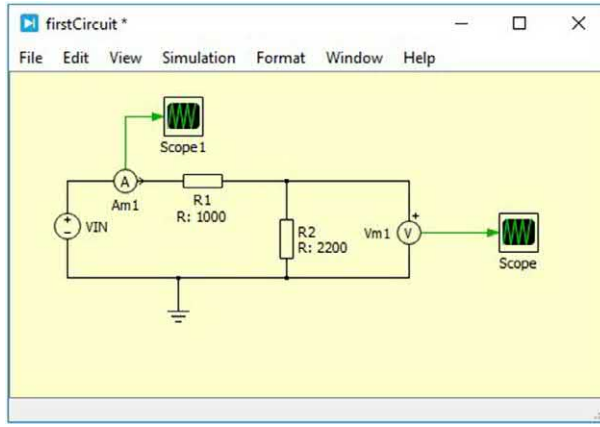


**FIG. 2.71** Connecting the ammeter block to the Scope 1 block.

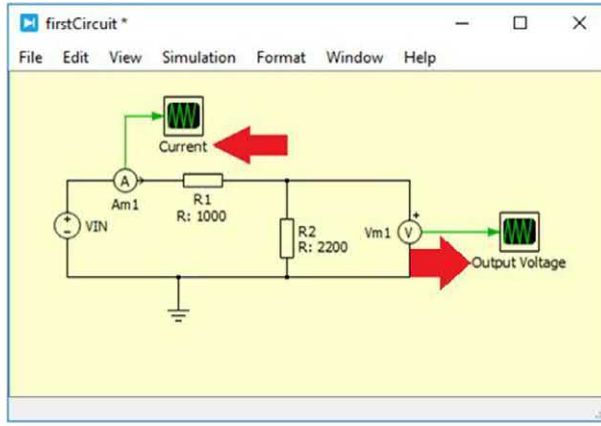


**FIG. 2.72** Renaming the scopes.

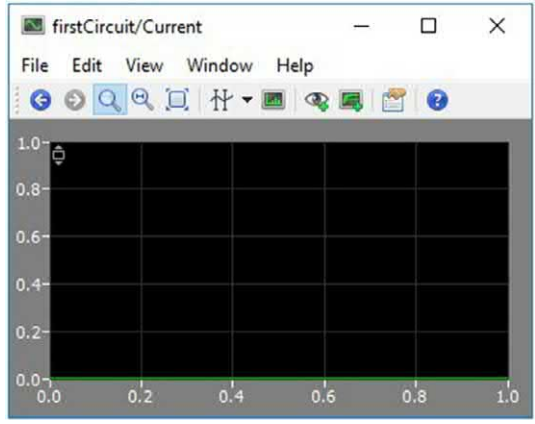


**FIG. 2.73** Current scope waveform.

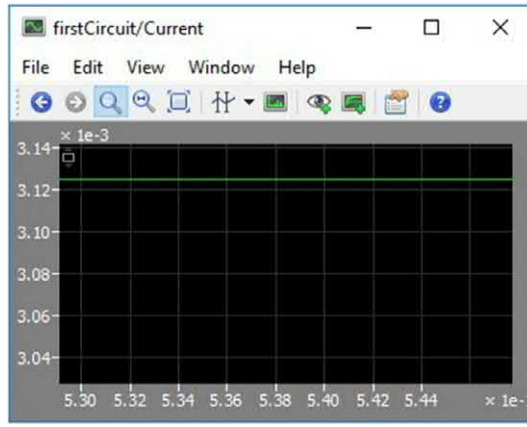


**FIG. 2.74** Zooming the Current scope waveform. Circuit current is about 3.12 mA.

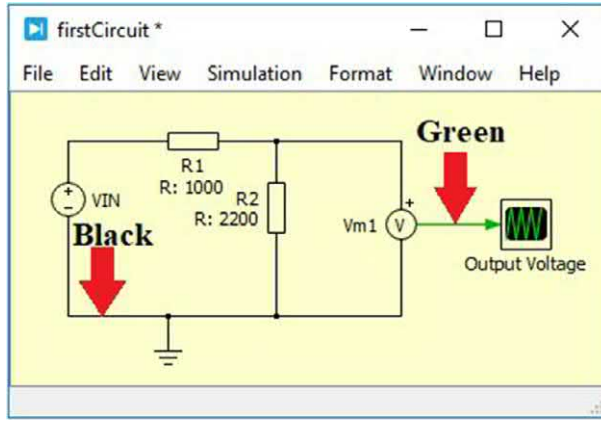


**FIG. 2.75** PLECS use different colors to show wires.

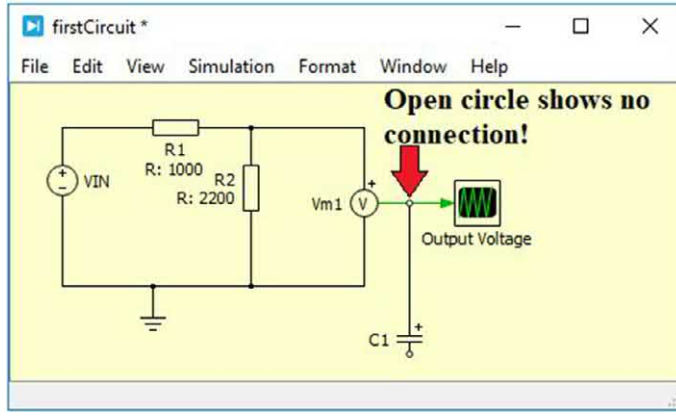


**FIG. 2.76** You cannot connect power circuit components to control signals.

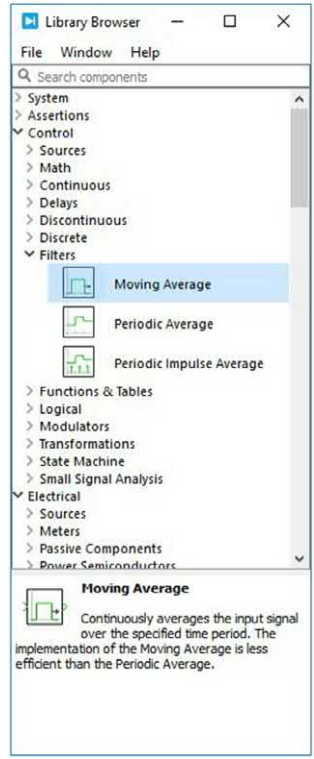


**FIG. 2.77** Moving Average block.

Green signals (control or measurement signals) can connect to blocks, which can process them. For example, you can connect output of a voltmeter to a "Moving Average" block since it can process the measured voltage but you cannot connect the output of a voltmeter to a capacitor (Figs. 2.77 and 2.78).

## 2.2 Example 2.2: RC circuit analysis

We want to simulate a simple RC circuit as our second example.

### 2.2.1 Preparing the simulation

Assume the schematic shown in Fig. 2.79. Capacitor can be found in Electrical > Passive Components as shown in Fig. 2.80. Used components settings are shown in Figs. 2.81–2.83.

We want to simulate the circuit for an interval of length 10 ms (Fig. 2.84). To do this, we click the "Simulation parameters…" and in the appeared window,

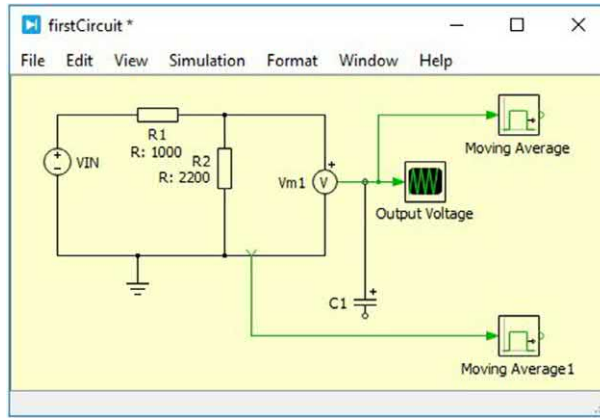


**FIG. 2.78** Moving average input expect control signal, so you can connect it to the output of voltmeter block. If the input port of a block is drawn in green, you can connect it only to green (control signal) wires.

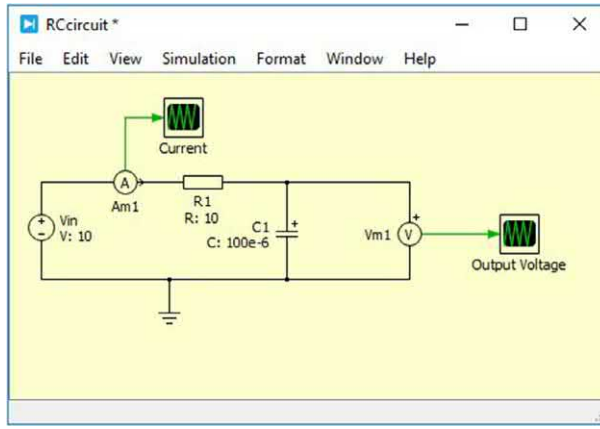


**FIG. 2.79** Schematic of the RC circuit.

set the "Stop time:" text box to 10e-3 as shown in Fig. 2.85. Do the other setting like that shown in Fig. 2.85.

After running the simulation, the waveform shown in Figs. 2.86 and 2.87 will be obtained. As you see, the waveforms are not very smooth, they seem to be piecewise linear.

Close the scopes and click the "Simulation parameters…" again (see Fig. 2.84). Reduce the "Max step size:" box to 1e-6, which means $10^{-6}$ (Fig. 2.88).

If we run the simulation, we obtain the waveforms shown in Figs. 2.89 and 2.90. This time the waveforms are more smooth (But simulation takes more time to complete).

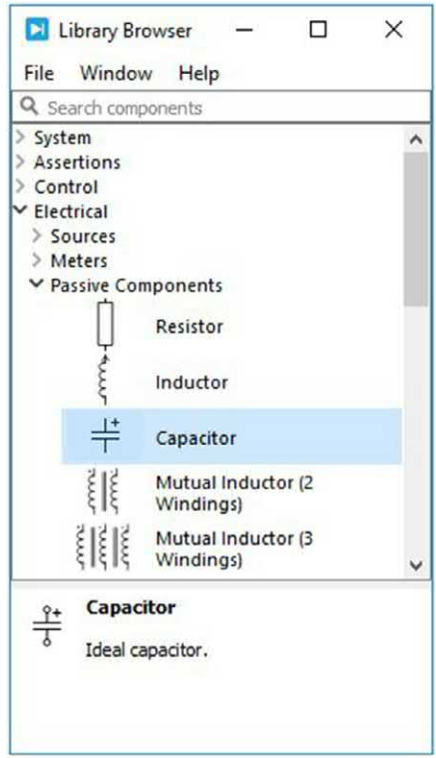


**FIG. 2.80** Capacitor block.

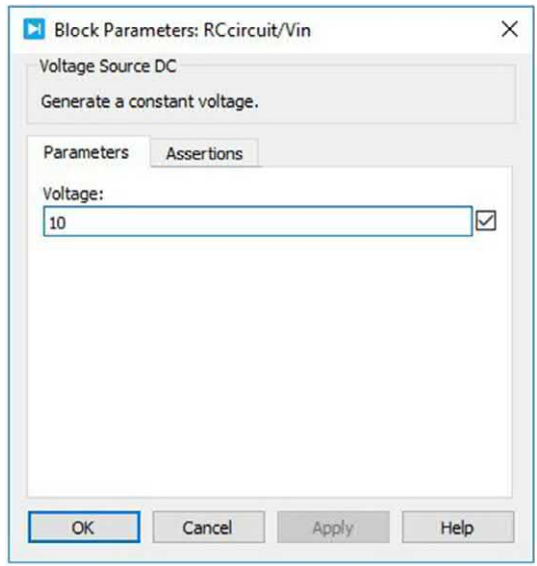


**FIG. 2.81** DC voltage source settings.

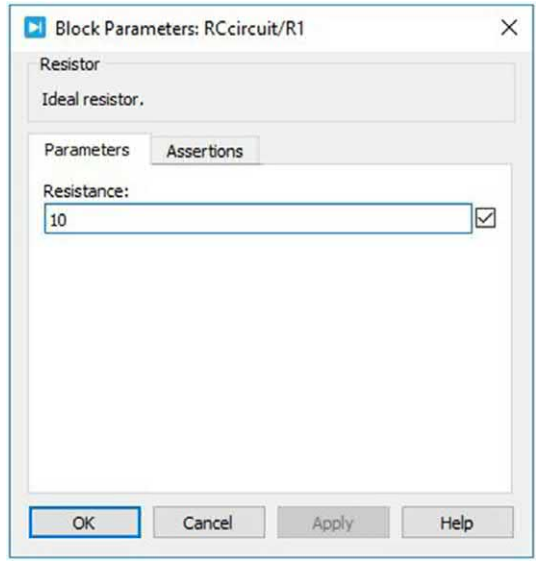


**FIG. 2.82** Resistor settings.

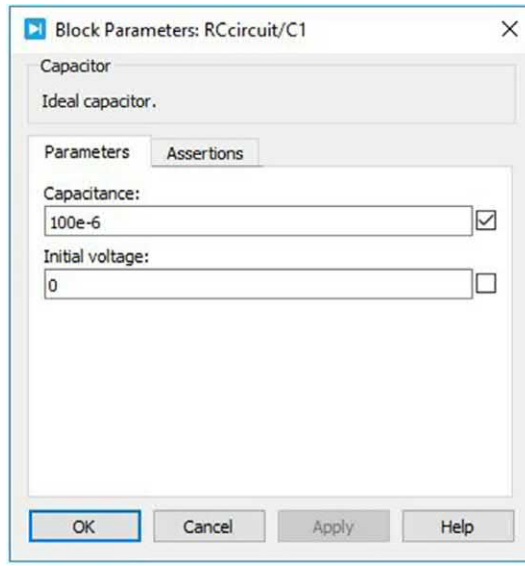


**FIG. 2.83** Capacitor settings.

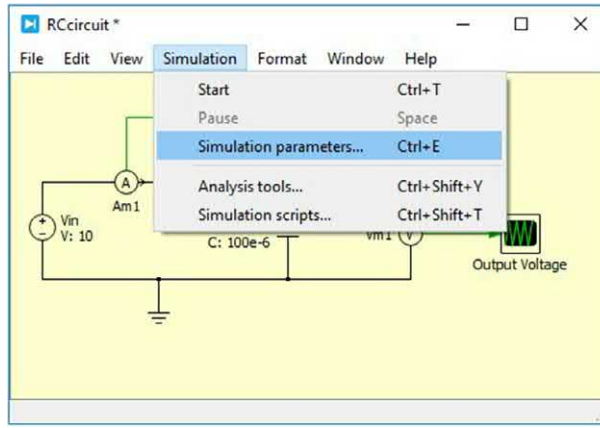


**FIG. 2.84** Simulation parameters.

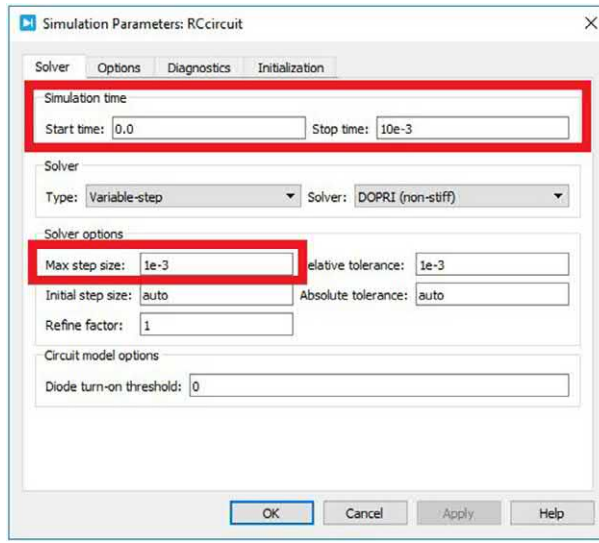


**FIG. 2.85** Simulation settings.

Circuit differential equation (which is a continuous-time equation) must be discretized to be solvable by a digital computer. When you discretize the equation with smaller values (smaller value in "Max step size:" box in Fig. 2.88), you increase the accuracy of response but you increase the required computations as well. You can decrease slightly the "Max step size:" value when you obtain piecewise-like waveforms.

There is no need to change the "Solver" section (see Fig. 2.88) for normal applications. See [1] for more information about the solver.

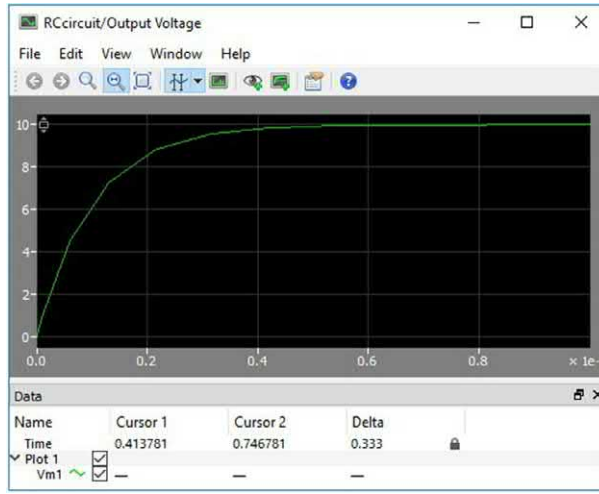


**FIG. 2.86** Capacitor voltage waveform.

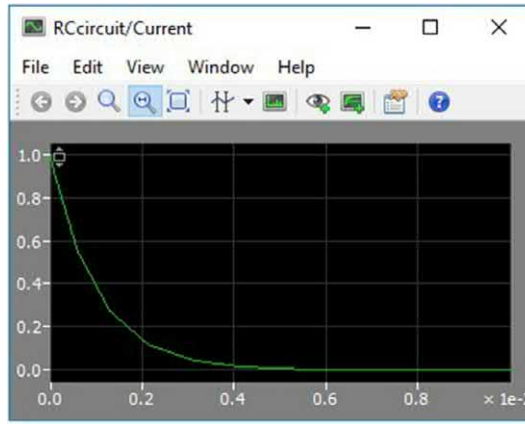


**FIG. 2.87** Circuit current waveform.

### 2.2.2 Specifying the initial condition

You can simulate the circuit with the desired initial conditions. Just double click the capacitor and set the "Initial voltage" box (Figs. 2.91 and 2.92). Here we assume the capacitor initial voltage is 2 V. The capacitor has a terminal shown with a + sign. When you enter "2" in the "Initial voltage:" box, it means $V_{the\ terminal\ with+sign} - V_{the\ terminal\ without+sign} = 2\ V$.

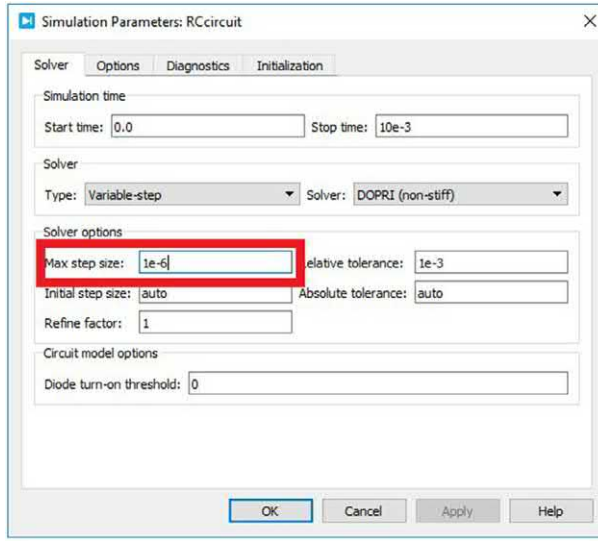


**FIG. 2.88** Max step size text box.

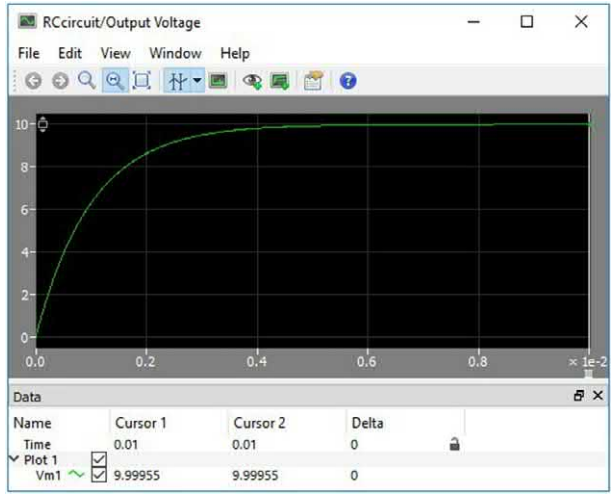


**FIG. 2.89** Capacitor voltage.

If we run the simulation, we obtain the result shown in Fig. 2.93 for capacitor voltage. Note that the voltage starts to increase from 2 V.

You can set the initial current of inductors as well, if your circuit contains any inductors. Just double click on the inductor you want and set its "Initial current:" box. Inductors contain a small arrow, which shows the positive direction.

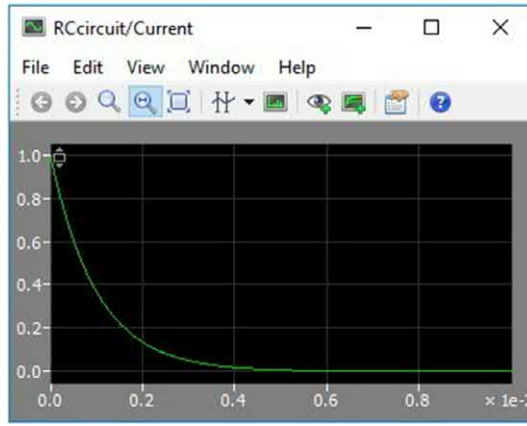


**FIG. 2.90** Circuit current.

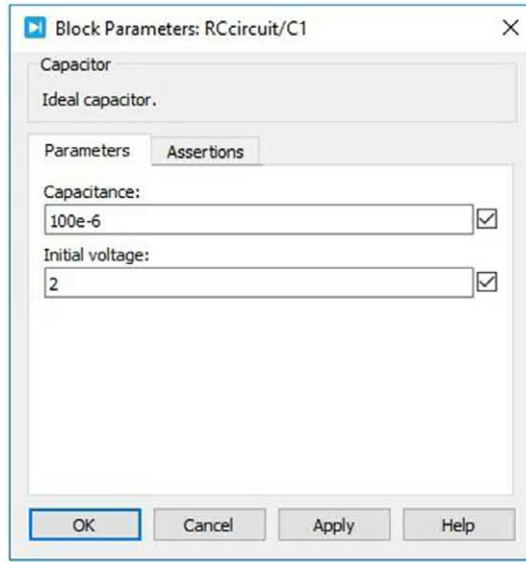


**FIG. 2.91** Setting the capacitor initial voltage to 2 V.

Initial current considers positive when it is in the direction of small arrow (Fig. 2.94).

### 2.2.3 Showing two or more waveforms simultaneously on the same axis

In PLECS, you can see two or more waveforms on the same axis. This makes comparison possible. The process of showing different waveforms on the same

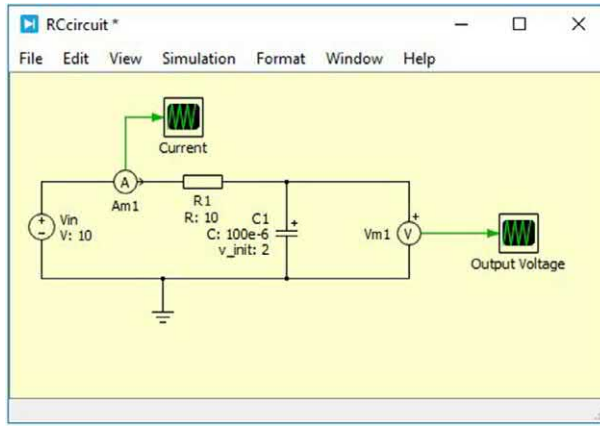


**FIG. 2.92** Schematic after setting the capacitor initial voltage.

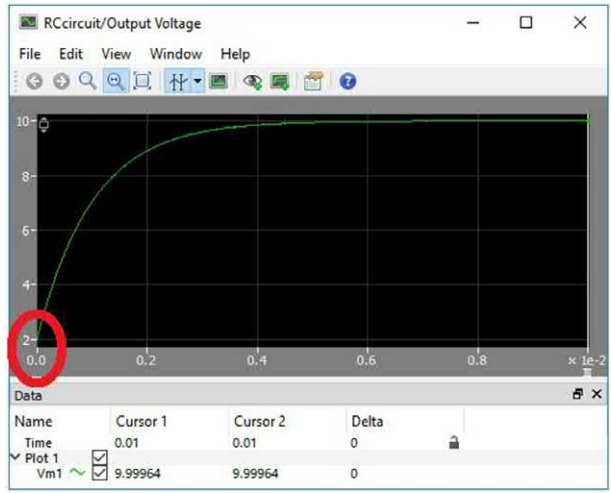


**FIG. 2.93** Capacitor voltage waveform.

axis is shown with the aid of an example. Consider a schematic like that shown in Fig. 2.95. The RC circuit is stimulated with a sinusoidal voltage source. We want to see both the input voltage source and capacitor voltage on the same axis. Input sinusoidal voltage source place and settings are shown in Figs. 2.96 and 2.97, respectively.

Add two voltmeters to the circuit as shown in Fig. 2.98.

Instead of using two scopes to show the outputs of two voltmeter block, we use a single scope, which has a multiplexer in its input. Multiplexer block can be found in the "System" section of "Library Browser." (Figs. 2.99 and 2.100)

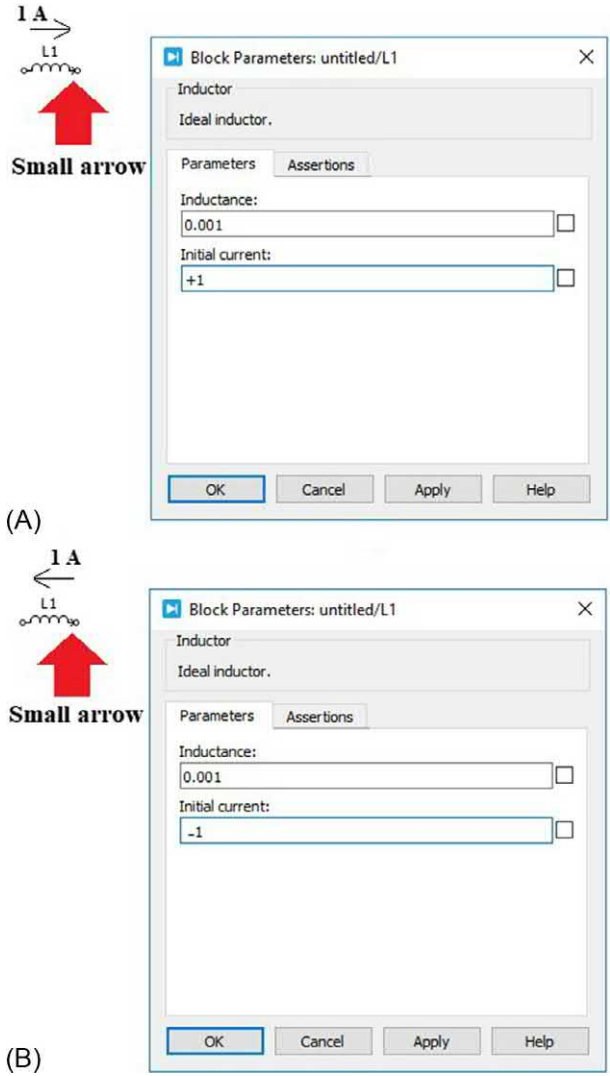


**FIG. 2.94** Setting the inductor initial current. (A) Initial current and the small arrow on the inductor symbol have the same direction (B) Initial current and the small arrow on the inductor symbol have opposite direction.

Double click on the multiplexer block placed in the schematic and decrease its inputs to 2 (Fig. 2.101).

Connect the voltmeter blocks outputs to the input of multiplexer block (Fig. 2.102).

Connect the output of the multiplexer block to a scope (Fig. 2.103).

If we run the simulation, we obtain the result shown in Fig. 2.104. As shown the two waveforms are shown on the same axis.

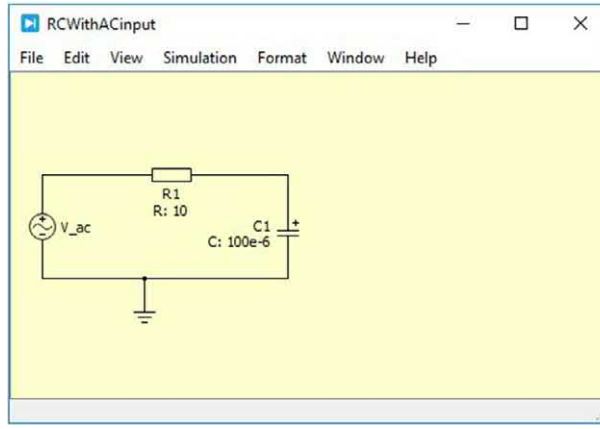


**FIG. 2.95** RC circuit with AC source.

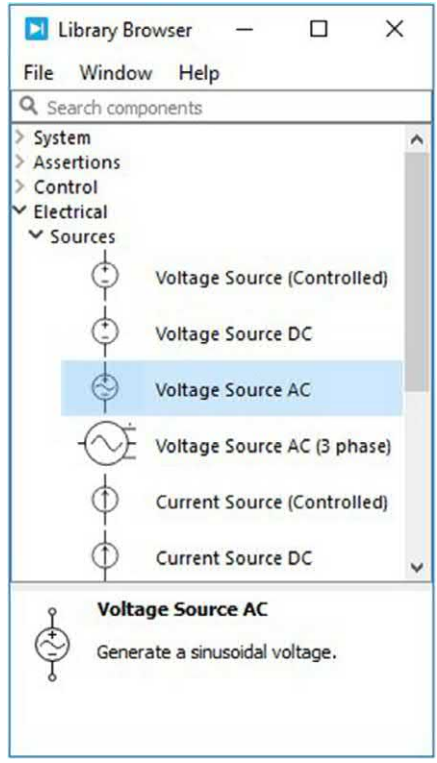


**FIG. 2.96** AC voltage source block.

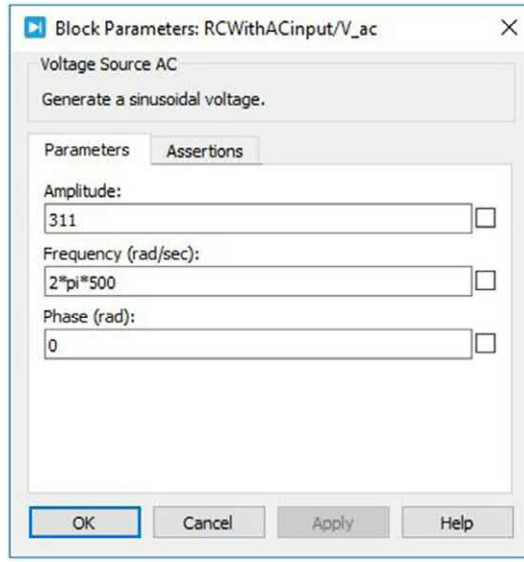


**FIG. 2.97** Settings of the AC source block in Fig. 2.95.

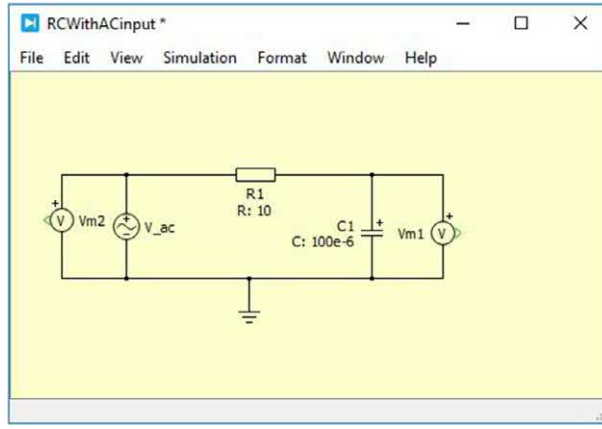


**FIG. 2.98** Adding 2 voltmeter blocks to the schematic.

### 2.2.4 Multiple input scope

You can display different waveform using a scope with multiple axis. Assume the circuit shown in Fig. 2.105. We want to show output of ammeter and voltmeter on different axis.

Double click on scope block. The window shown in Fig. 2.106 will appear.

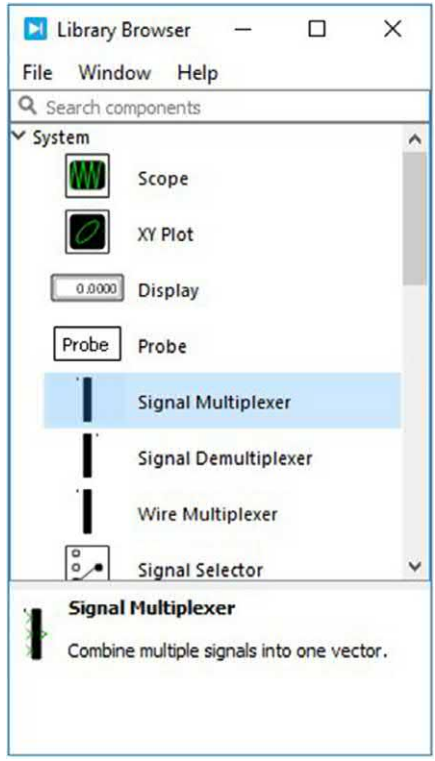


**FIG. 2.99** Multiplexer block.

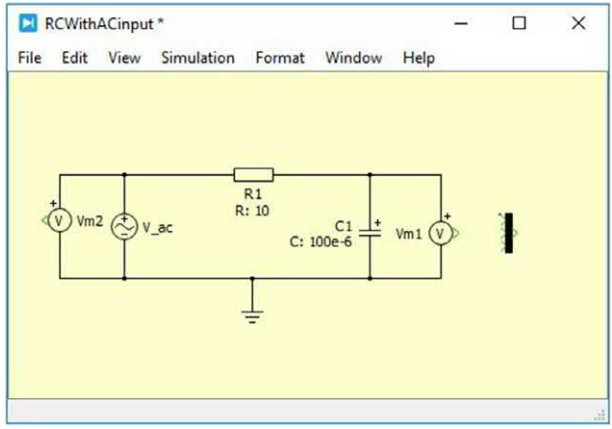


**FIG. 2.100** Adding the multiplexer block to the schematic.

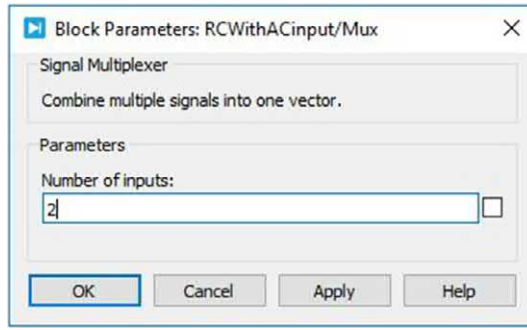


**FIG. 2.101** Specifying the required number of inputs.

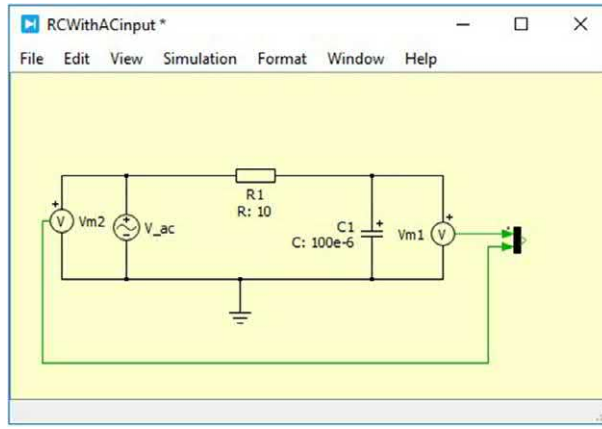


**FIG. 2.102** Connecting the voltmeter outputs to the multiplexer block.

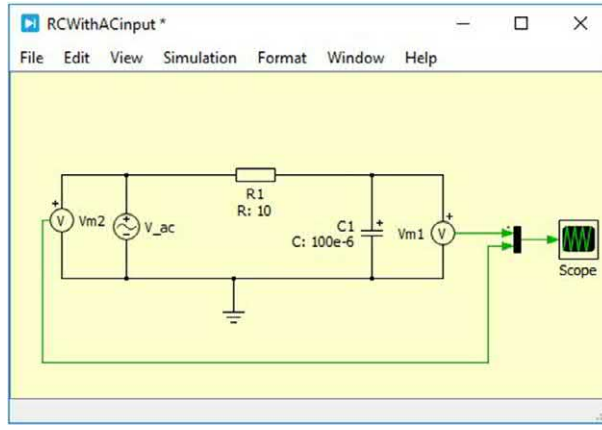


**FIG. 2.103** Connecting the multiplexer block to the scope block.

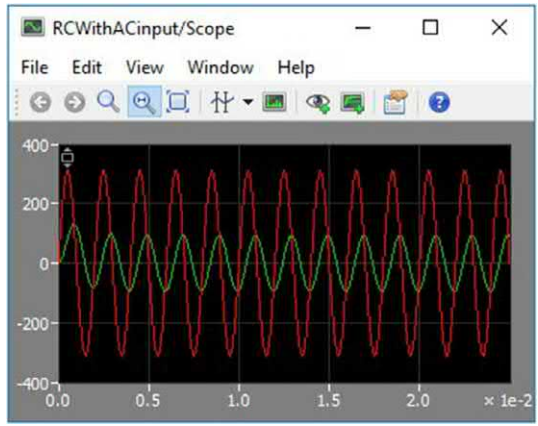


**FIG. 2.104** Simulation result (input source voltage and capacitor voltage).

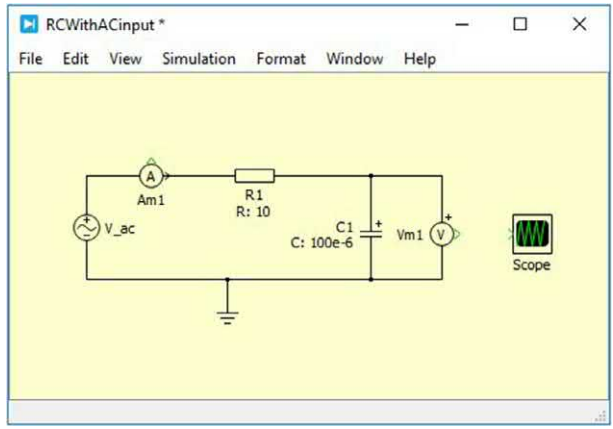


**FIG. 2.105** Scope block can be turned into a multiple input block.

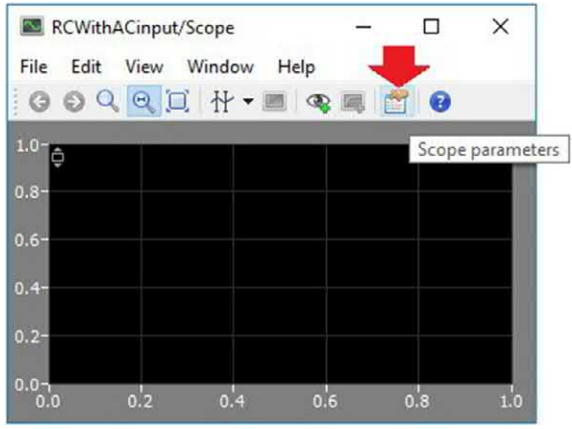


**FIG. 2.106** Scope parameters icon.

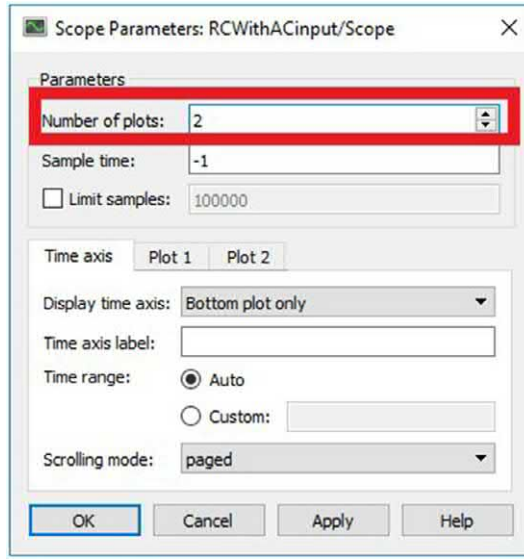


**FIG. 2.107** Scope parameters window.

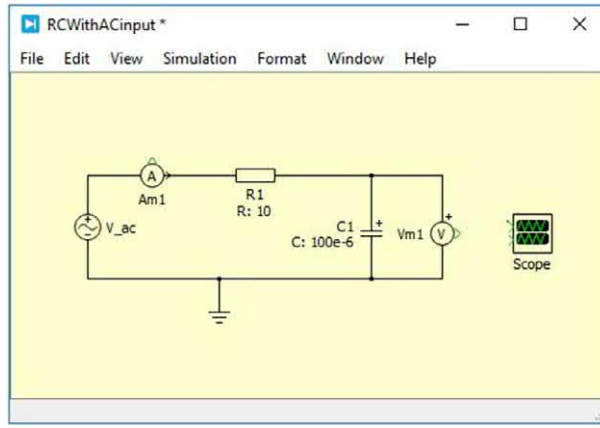


**FIG. 2.108** Scope turned into a multiple input block.

Click on "Scope parameters" icon (see Fig. 2.106). After clicking the icon, window shown in Fig. 2.107 will appear. Increase the "Number of plots:" to 2 and click "OK" button.

The scope has 2 inputs now (Fig. 2.108).

Connect the ammeter and voltmeter to the scope (Fig. 2.109).

If we run the simulation with settings shown in Fig. 2.110, we obtain the waveforms shown in Fig. 2.111.

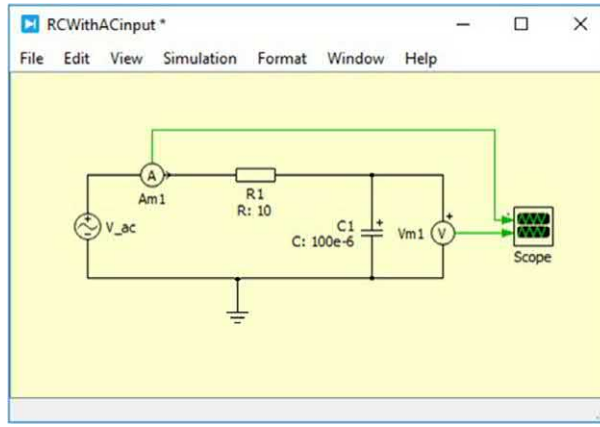


**FIG. 2.109** Connecting the measurement outputs to the scope.

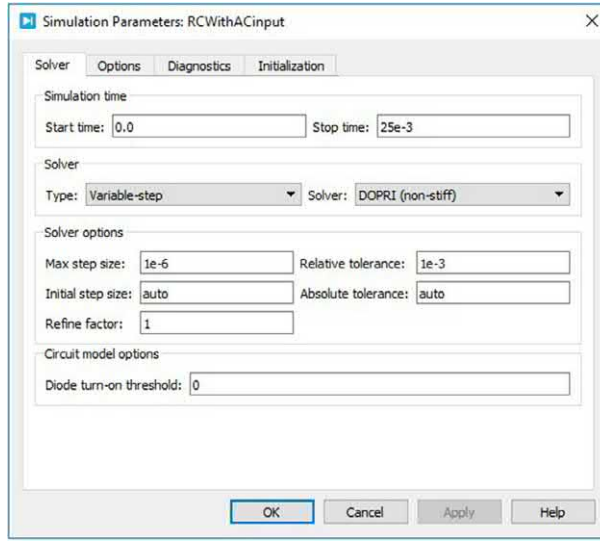


**FIG. 2.110** Simulation parameters window.

## 2.2.5 XY scope block

The scope block shows a waveform in terms of time, i.e., $f(t)$. You can show a waveform in terms of another waveform. Using this capability, you can see the Lissajous curves. Consider the schematic shown in Fig. 2.112. We want to draw the capacitor voltage in terms of input source voltage.

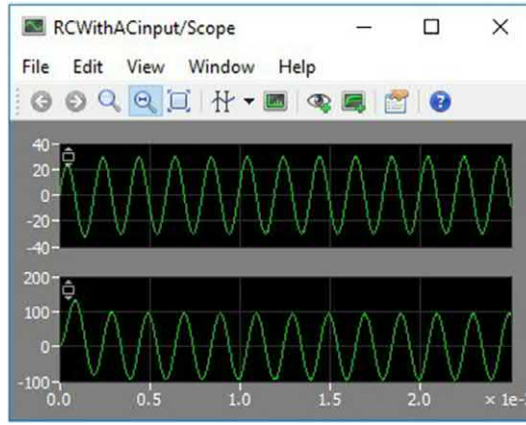


**FIG. 2.111** Simulation result.

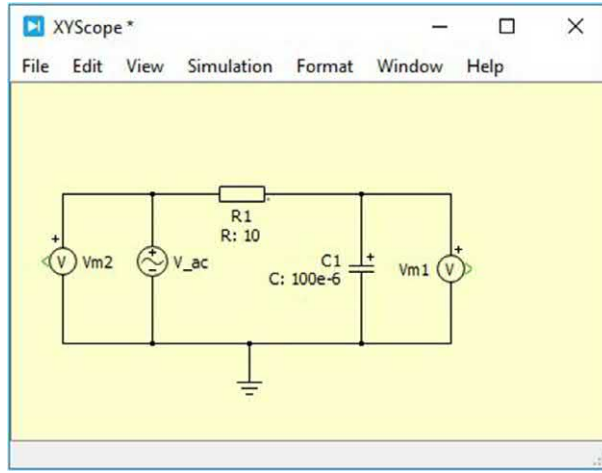


**FIG. 2.112** You can show a waveform in terms of another waveform using XY Plot block.

Add an "XY Plot" block to the schematic. You can find the "XY Plot" block in "System" section of Library Browser (Figs. 2.113 and 2.114).

"XY Plot" block has two inputs. Lower input (Y axis) is drawn in terms of upper input (X axis) (Fig. 2.115).

Connect the voltmeters to the "XY Plot" block (Fig. 2.116).

If we run the simulation with settings shown in Fig. 2.117, we obtain the waveforms shown in Fig. 2.118.

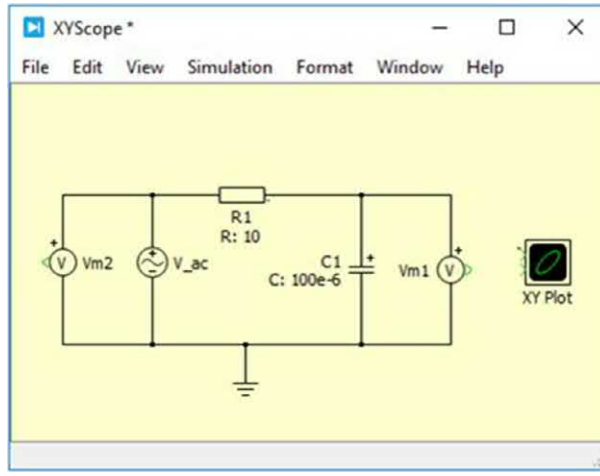


**FIG. 2.113** Adding the XY Plot block to the schematic.

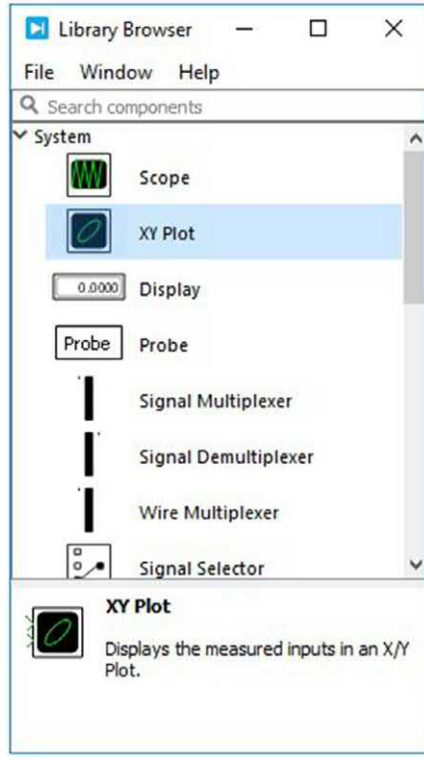


**FIG. 2.114** XY Plot block.

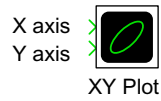


**FIG. 2.115** XY Plot block inputs. Upper one controls the X axis and the lower one controls the Y axis.

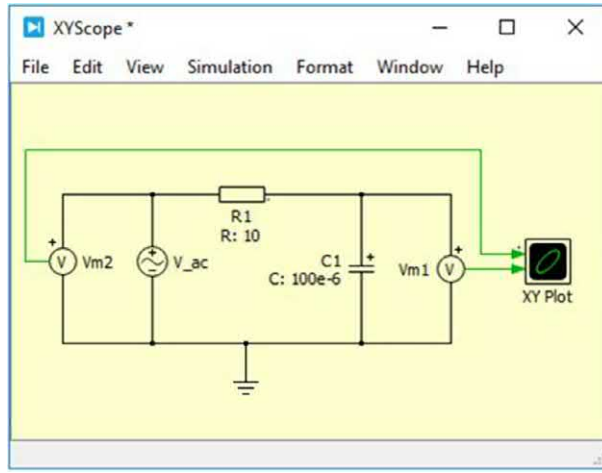


**FIG. 2.116** Connecting the output of measurement devices to the XY Plot block.

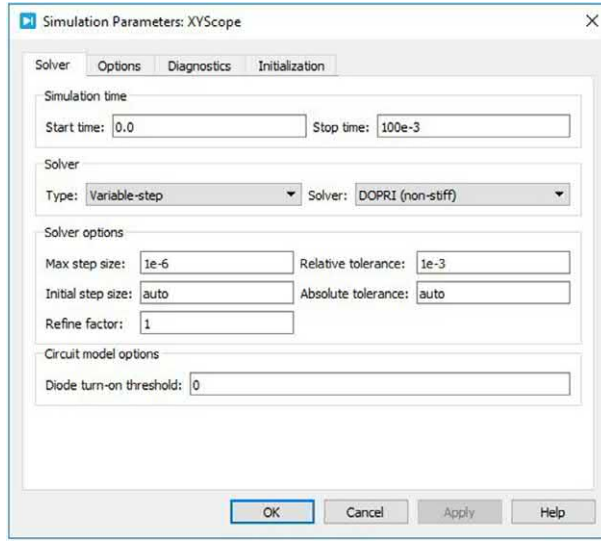


**FIG. 2.117** Simulation settings.

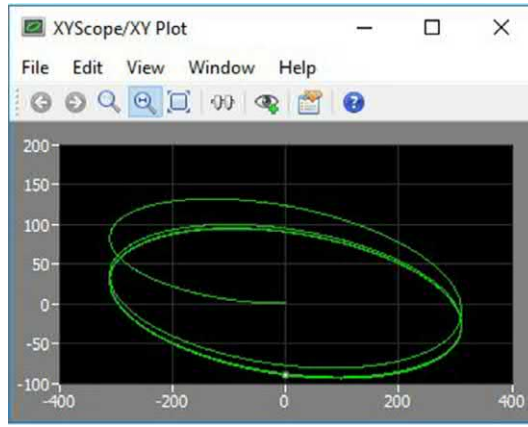


**FIG. 2.118** Simulation result.

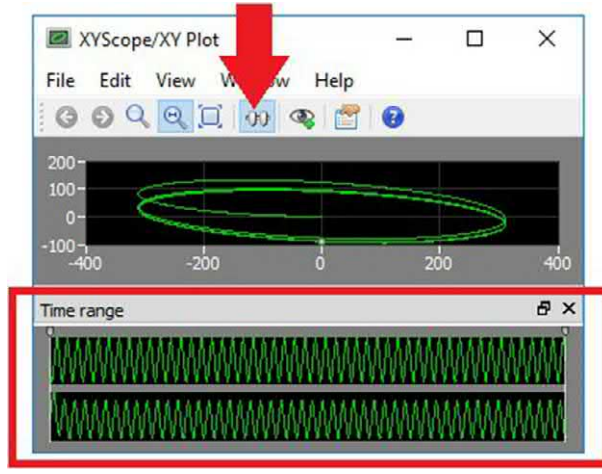


**FIG. 2.119** "Time range" icon.

If you want to see the steady-state curve, only click on the "Time range" icon. The "Time range" section will appear (Fig. 2.119).

Bring the appeared left sliders to the steady-state parts of the graph, i.e., toward right (Figs. 2.120 and 2.121).

The steady-state Lissajous curve will appear as shown in Fig. 2.122.

You can copy the curve into the Windows clipboard by clicking the "Copy…" (Fig. 2.123).

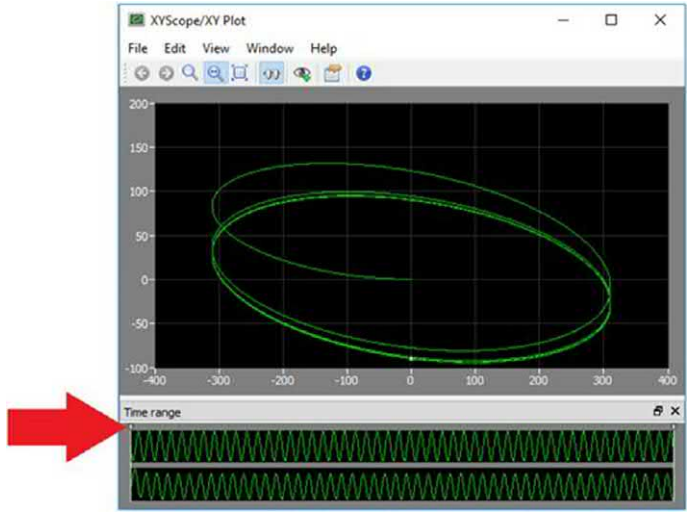


**FIG. 2.120** Use the slider to see only the steady-state part of graph.

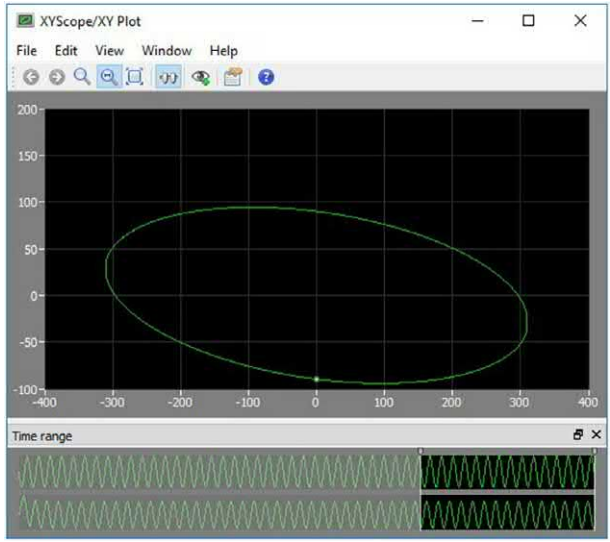


**FIG. 2.121** Move the left slider toward right to obtain the steady-state Lissajous curve.

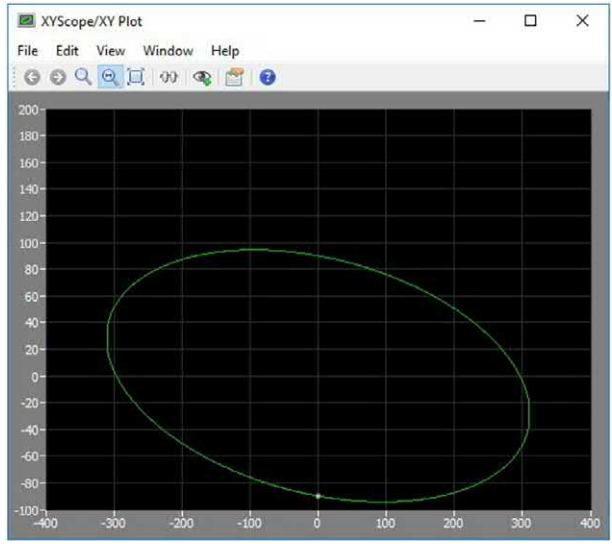


**FIG. 2.122** Steady-state Lissajous curve.

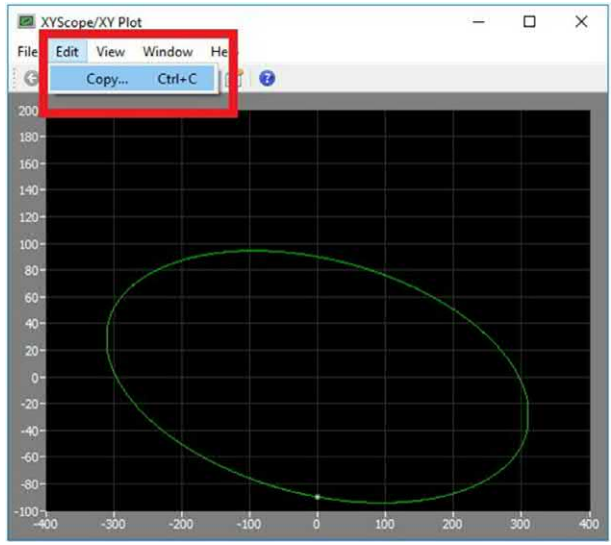


**FIG. 2.123** Copying the obtained graph into the Windows clipboard.

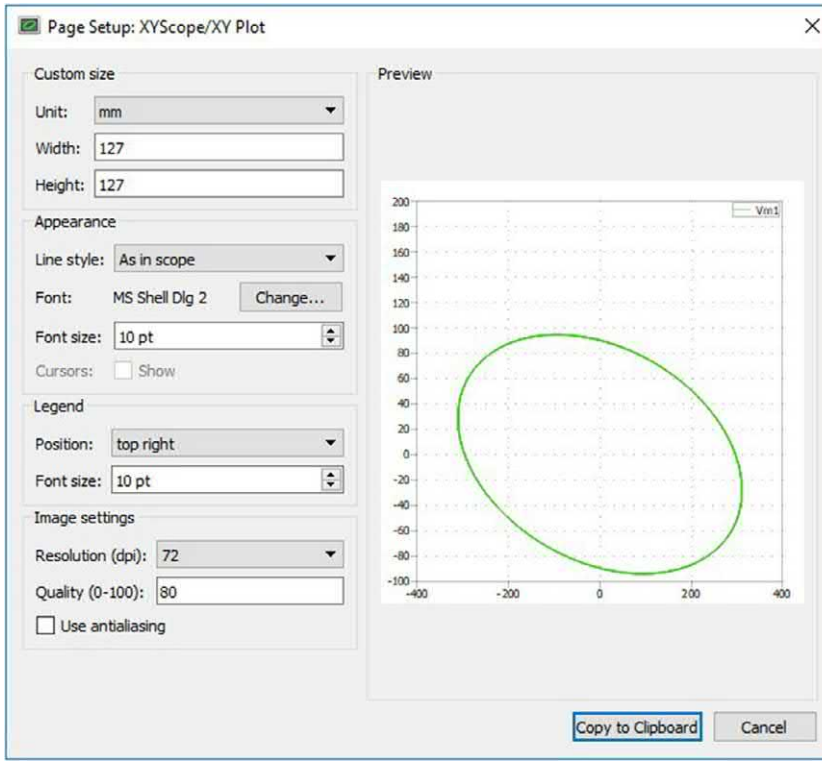


**FIG. 2.124** Page setup window.

After clicking the "Edit…" the window shown in Fig. 2.124 appears, which can be used to obtain the desired image settings.

### 2.2.6 Simulation of control systems

PLECS can simulate both continuous time and discrete time control systems. Related blocks are shown in Figs. 2.125 and 2.126.

Assume that we want to simulate the block diagram shown in Fig. 2.127. Place of blocks required for this system is shown in Figs. 2.128–2.130.

Draw the schematic shown in Fig. 2.131.

Double click on the "Step" block and do the setting as shown in Fig. 2.132.

In order to obtain the $H(s) = \frac{1}{s^3 + 6s^2 + 5s}$, the "Plant" block settings must be done as shown in Fig. 2.133.

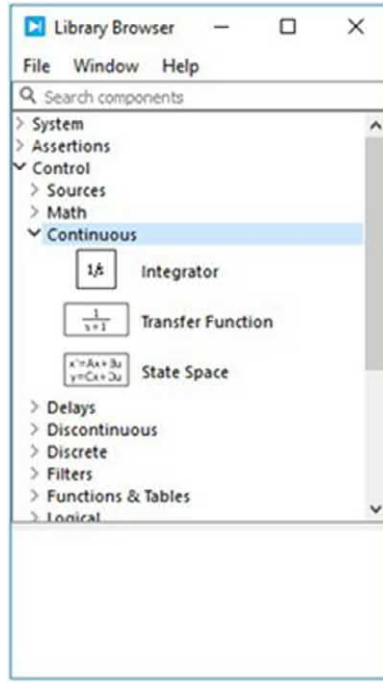


**FIG. 2.125** Continuous time blocks.

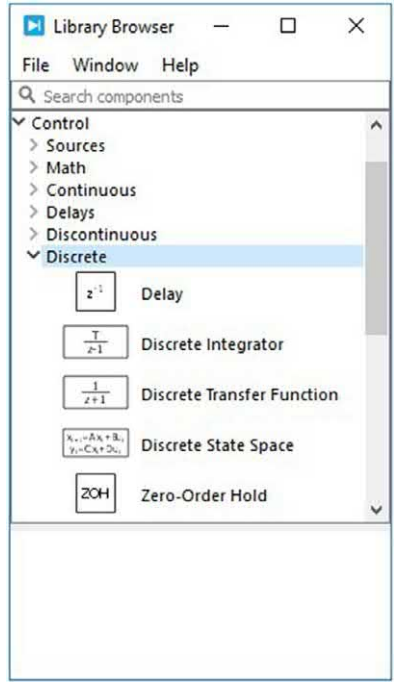


**FIG. 2.126** Discrete time blocks.

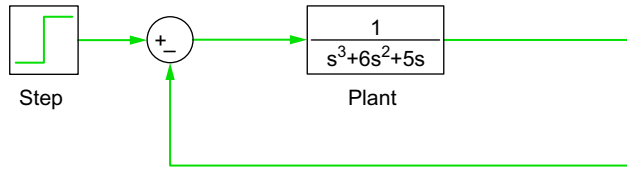


**FIG. 2.127** A simple closed-loop system.

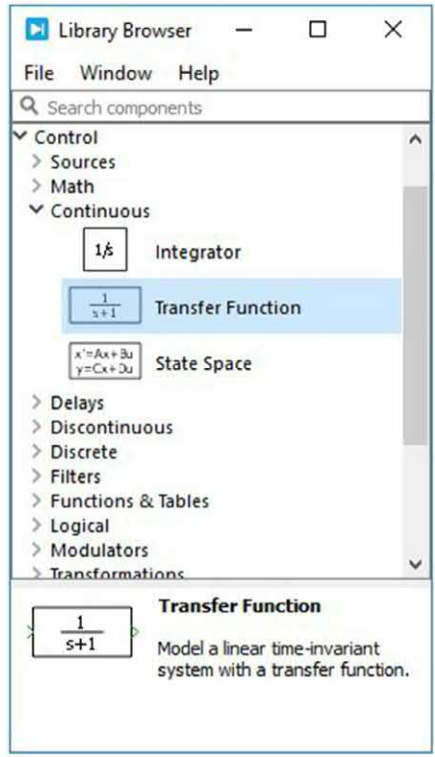


**FIG. 2.128** Transfer function block.

After setting the "Plant" coefficients, the schematic changes to that shown in Fig. 2.134.

If we run the simulation with settings shown in Fig. 2.135, we obtain the waveform shown in Fig. 2.136.

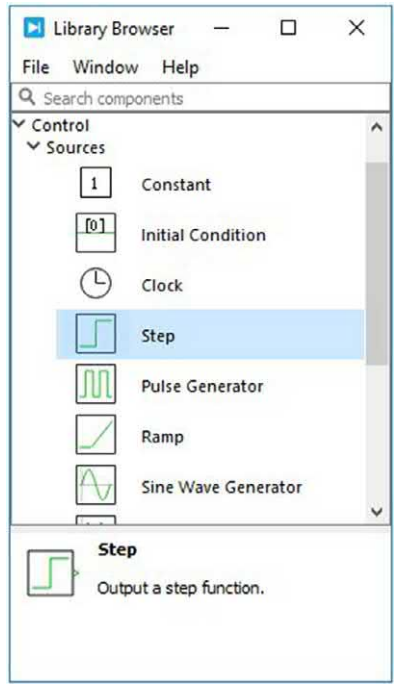


**FIG. 2.129** Step block.

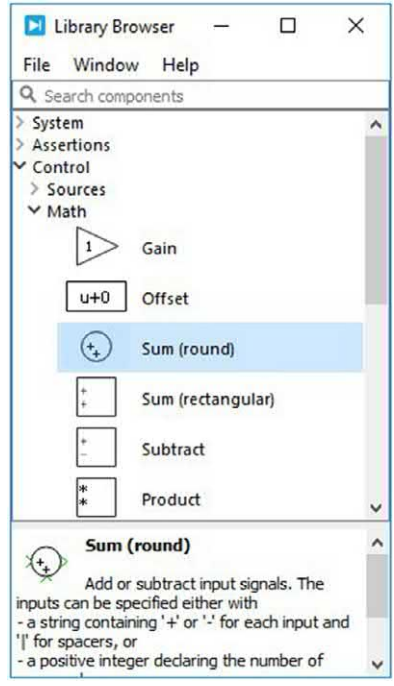


**FIG. 2.130** Summation block.

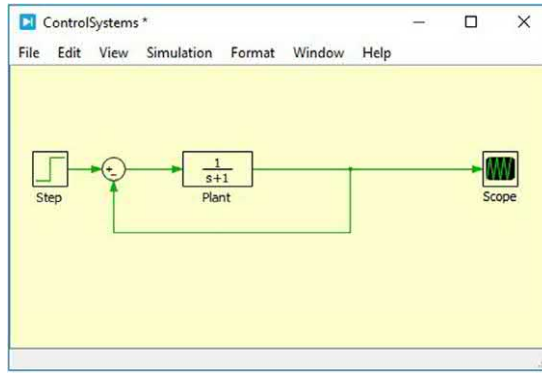


**FIG. 2.131** Drawing the close loop system.

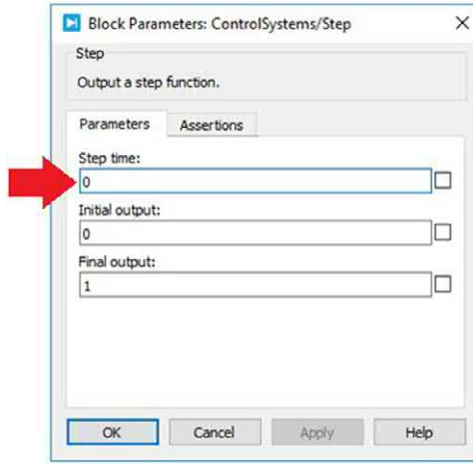


**FIG. 2.132** Step block settings.

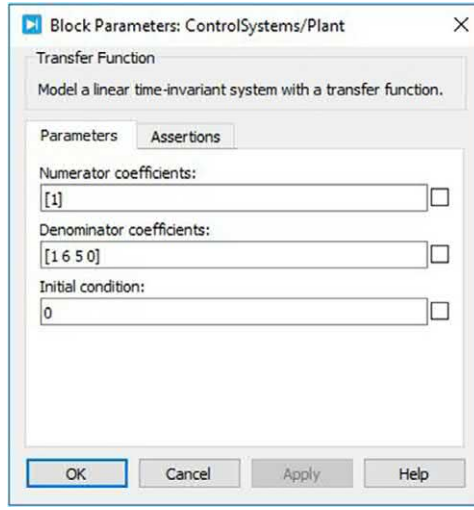


**FIG. 2.133** Plant block settings.

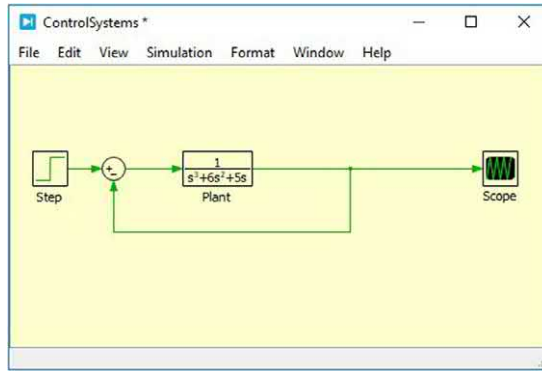


**FIG. 2.134** Ready-to-use simulation schematic.

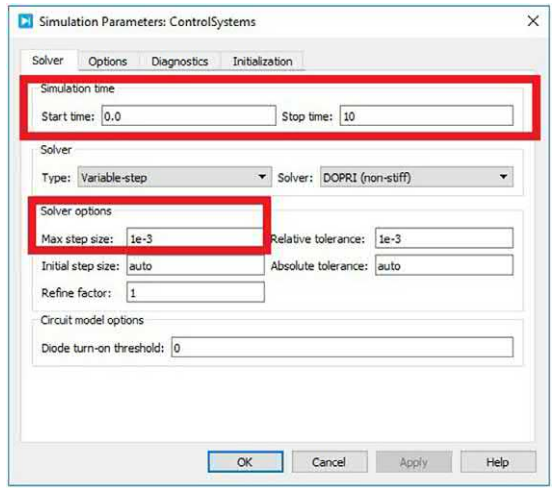


**FIG. 2.135** Simulation settings.

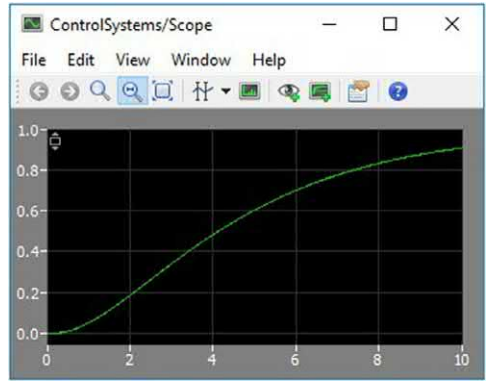


**FIG. 2.136** Simulation result.

### 2.2.7 Getting help in PLECS

PLECS has a powerful help system. For example, assume that you need some information about a block you placed in the schematic (Fig. 2.137). Simply right click on the block and select the "Help."

The block information window will appear (Fig. 2.138).

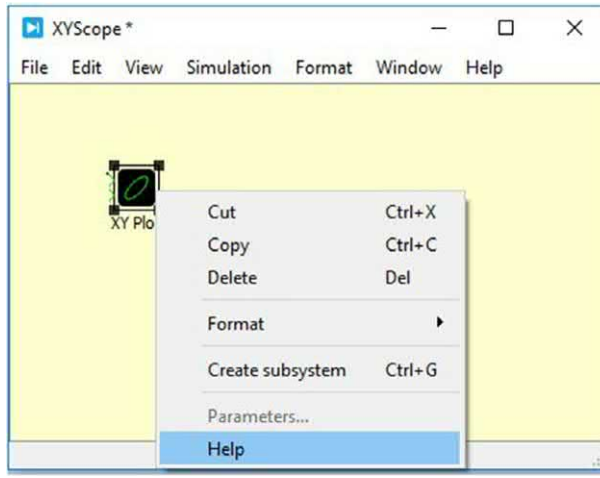


**FIG. 2.137** You can see a block documentation by right clicking on it and selecting the Help.

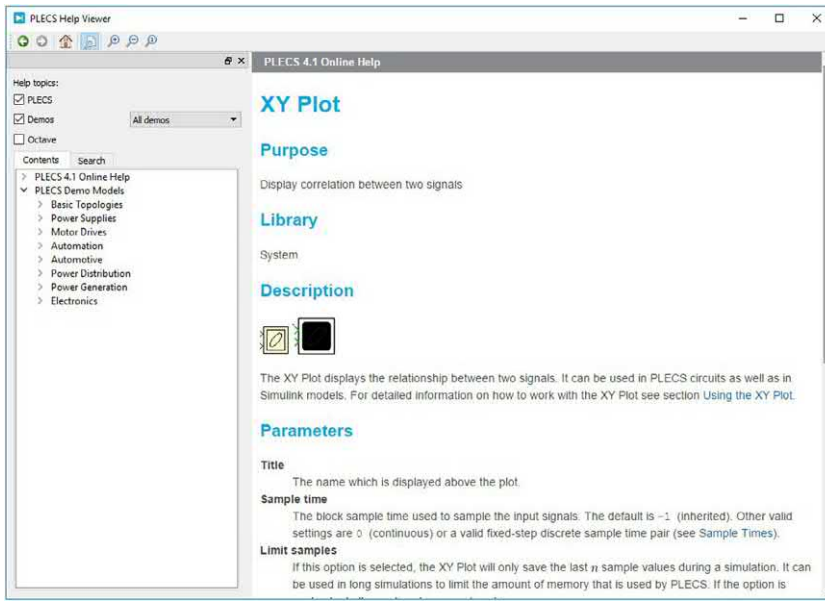


**FIG. 2.138** Online Help for XY Plot block.

You can access the help system by clicking the "PLECS Documentation" as well (Fig. 2.139).

You can access to plenty of sample simulations by clicking the menus in the left of the appeared window (Fig. 2.140).

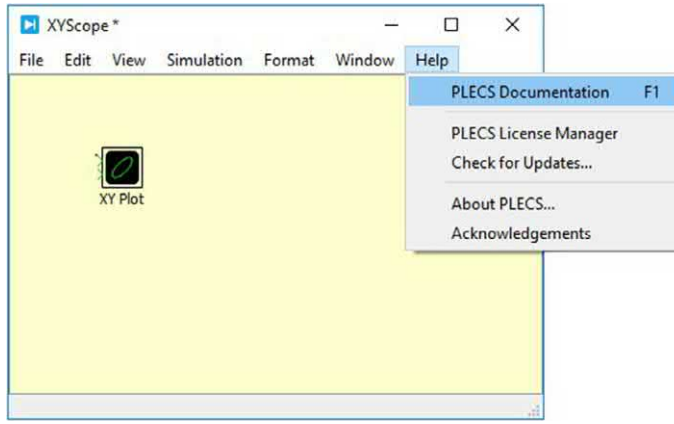


**FIG. 2.139** PLECS documentation.

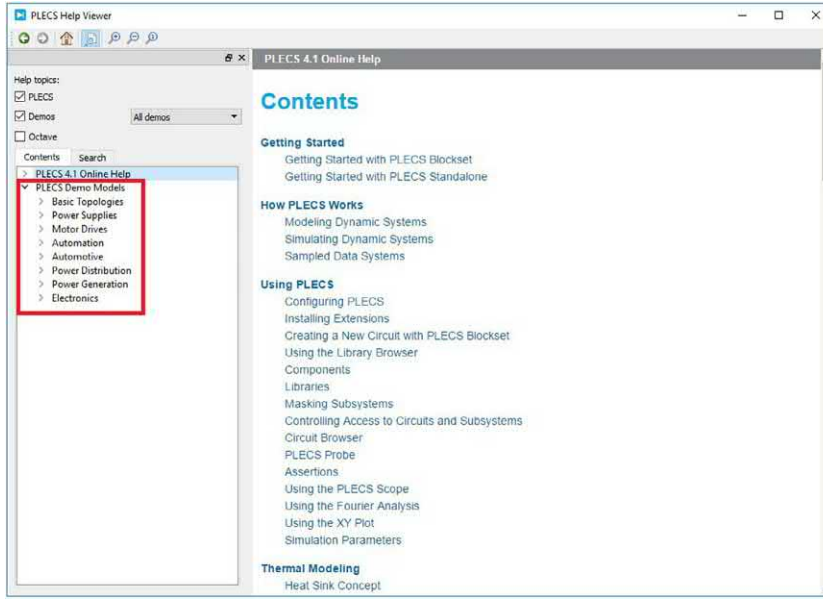


**FIG. 2.140** Demo models provided by Plexim can be a good reference to learn the art of simulation.

## References

[1] PLECS user manual available online at, https://www.plexim.com/download/documentation.

## Further reading

[2] D. Maksimovic, A.M. Stankovic, V.J. Thottuvelil, G.C. Verghese, Modeling and simulation of power electronic converters, Proc. IEEE 89 (6) (Jun 2001) 898–912, https://doi.org/10.1109/5.931486.
[3] M.H. Rashid, SPICE for Power Electronics and Electric Power, CRC Press, 2017.
[4] F. Asadi, N. Abut, Simulation of power electronics converters with PSIM®, (in Turkish), Umuttepe yayınları, 2018.
[5] F. Asadi, N. Abut, Simulation of power electronics converters with MATLAB/Simulink®, (in Turkish), Umuttepe yayınları, 2018.

Chapter 3

# Basics of power electronic circuits simulation with PLECS

## Chapter outline



**Simulation of Power Electronics Converters Using PLECS®. https://doi.org/10.1016/B978-0-12-817364-0.00003-5**

## Introduction

This chapter shows you how simulation of power converter can be done with the aid of PLECS standalone. We give 12 different examples in this chapter. It is a good idea to do some hand analysis and compare the hand analysis results with the ones provided by PLECS. Try to find any source of error between your result and PLECS output. This helps you to understand the power electronics concepts very well.

## 3.1 Example 3.1: MOSFET with resistive load

In this example, we will simulate a MOSFET driving a resistive load.

### 3.1.1 Preparing the simulation

Assume a simulation such as that shown in Fig. 3.1. The MOSFET block can be found under the "Power Semiconductors" section of Library Browser (Fig. 3.2).

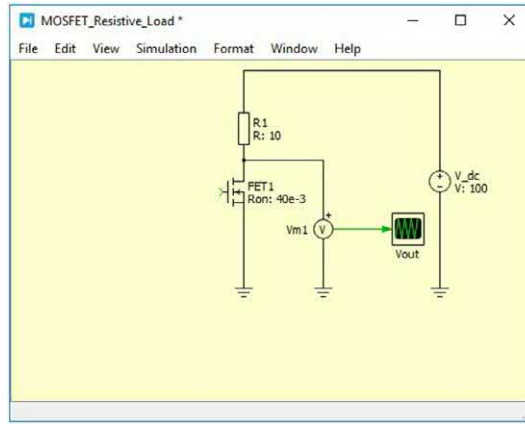


**FIG. 3.1** MOSFET with resistive load.

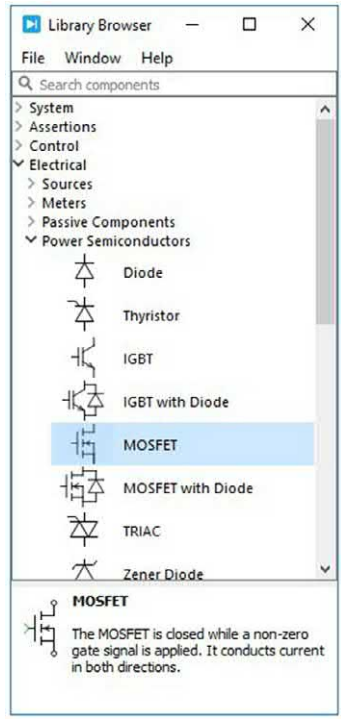


**FIG. 3.2** MOSFET block.

Assume that the drain-source resistance is 40 mΩ. With this assumption, double click the MOSFET block and do the settings as shown in Fig. 3.3.

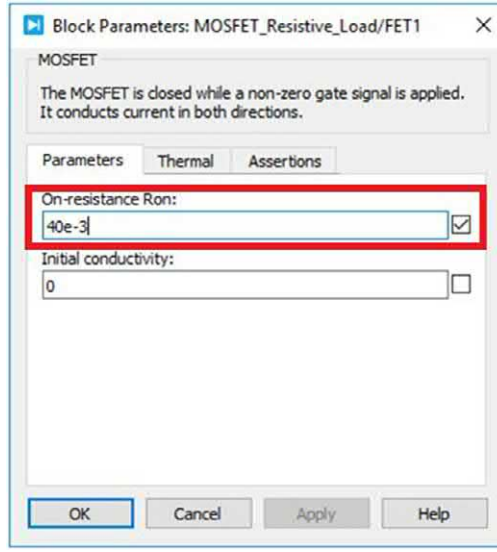


**FIG. 3.3** Specifying the On-resistance of the MOSFET.

Assume that the MOSFET is triggered with the pulse shown in Fig. 3.4.

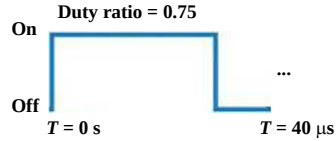


**FIG. 3.4** The MOSFET gate signals.

To obtain the gate signal shown in Fig. 3.4, we change the schematic to that shown in Fig. 3.5. Added blocks places are shown in Figs. 3.6–3.8. "Triangular Wave" settings are shown in Fig. 3.9.

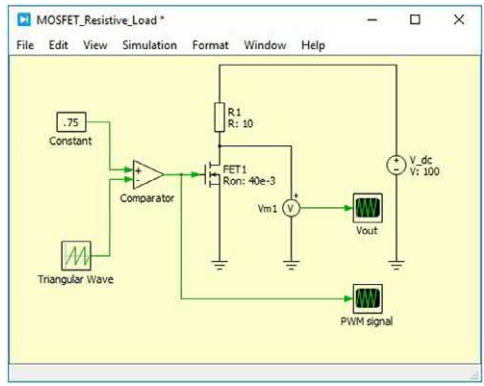


**FIG. 3.5** Adding the PWM generation blocks to the schematic.

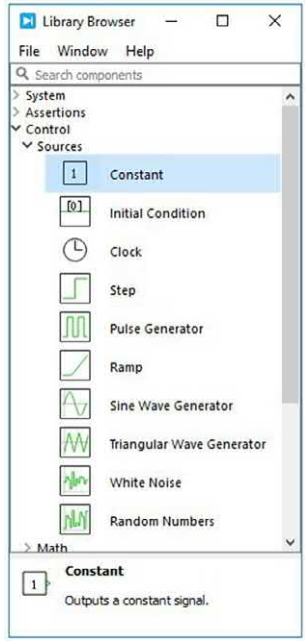


**FIG. 3.6** Constant block.

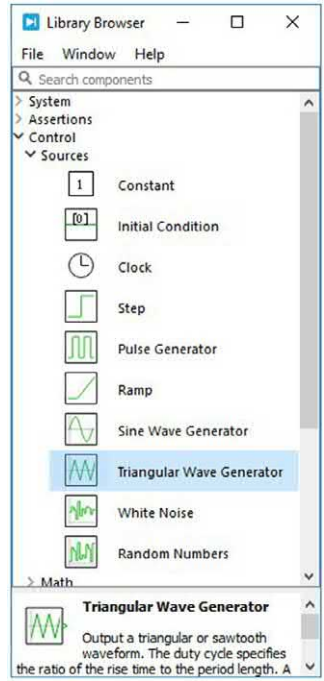


**FIG. 3.7** Triangular Wave Generator block.

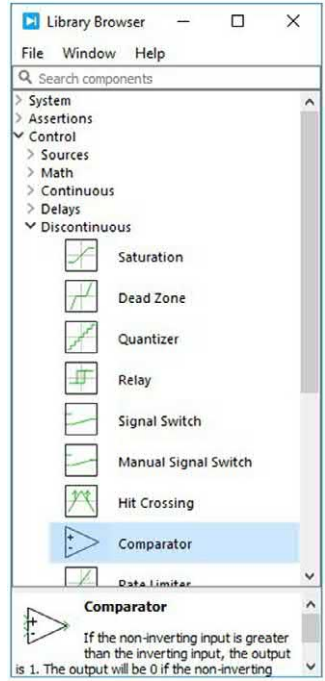


**FIG. 3.8** Comparator block.

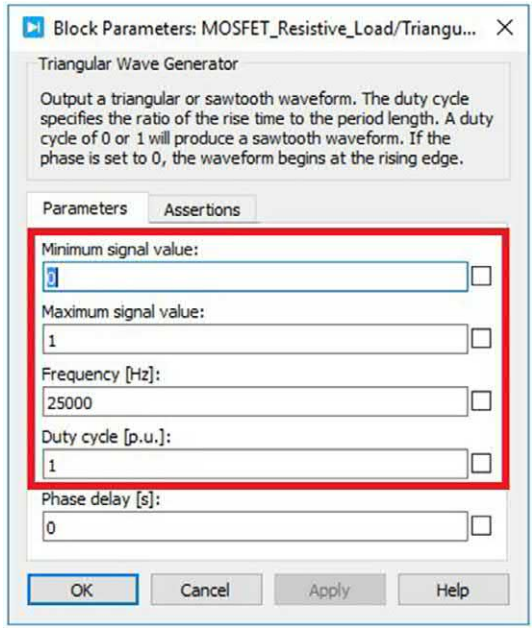


**FIG. 3.9** "Triangular Wave Generator" block settings.

Using the "Triangular Wave Generator" block, one can obtain saw tooth or triangular waveforms. See Figs. 3.10–3.12 for more information on this block setting.

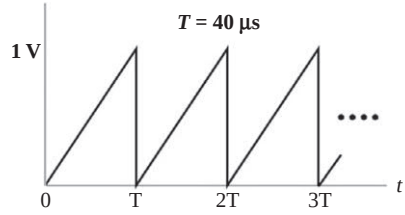


**FIG. 3.10** Output of a "Triangular Wave Generator" block with Minimum signal value: 0, Maximum signal value: 1, Frequency: 25000, Duty cycle [p.u.]: 1.

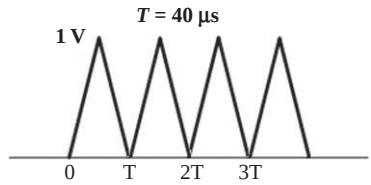


**FIG. 3.11** Output of a "Triangular Wave Generator" block with Minimum signal value: 0, Maximum signal value: 1, Frequency: 25000, Duty cycle [p.u.]: 0.5.

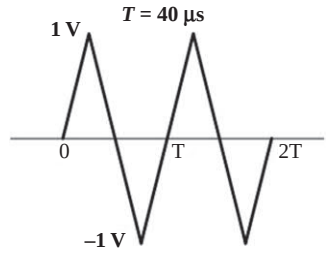


**FIG. 3.12** Output of a "Triangular Wave Generator" block with Minimum signal value: −1, Maximum signal value: 1, Frequency: 25000, Duty cycle [p.u.]: 0.5.

If we run the simulation with the settings shown in Fig. 3.13, we obtain the waveform shown in Fig. 3.14.

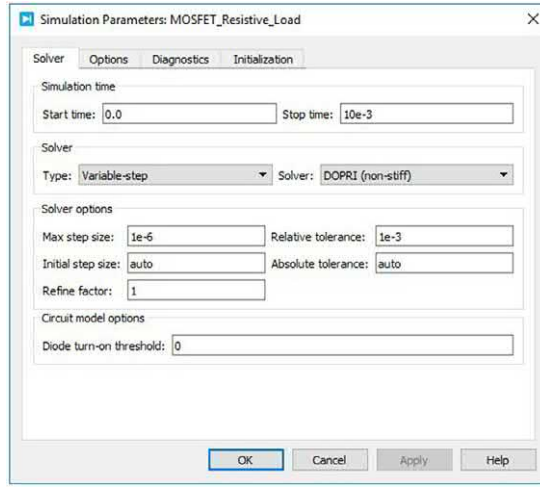


**FIG. 3.13** Simulation parameters.

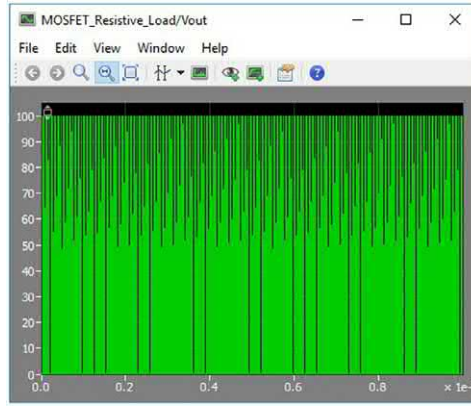


**FIG. 3.14** Simulation result ("Vout" scope).

Use the magnifier icon in the toolbox to see the waveform better (Fig. 3.15).

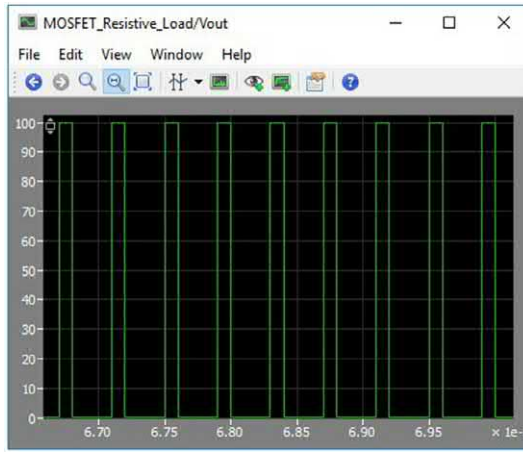


**FIG. 3.15** Load resistor voltage.

MOSFET gate signal is shown in Fig. 3.16. You can use the cursors to ensure that its duty ratio and frequency.

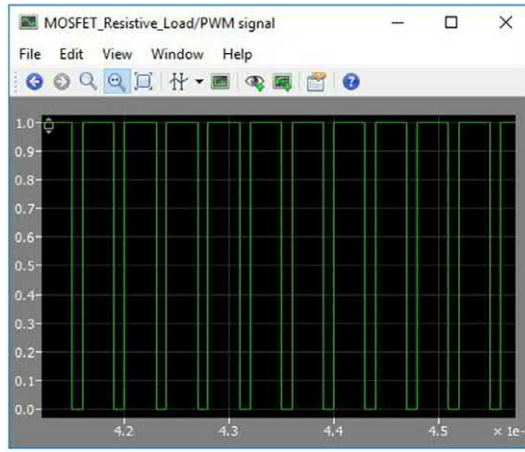


**FIG. 3.16** MOSFET gate signal.

### 3.1.2 Measuring the average and RMS of waveforms

You can use the cursors to measure the average and Root Mean Square (RMS) value of output voltage. To do these measurements, click on Cursors icon (the

icon shown with circle in Fig. 3.17). After clicking the Cursors icon, the "Data" section will appear (Fig. 3.17).

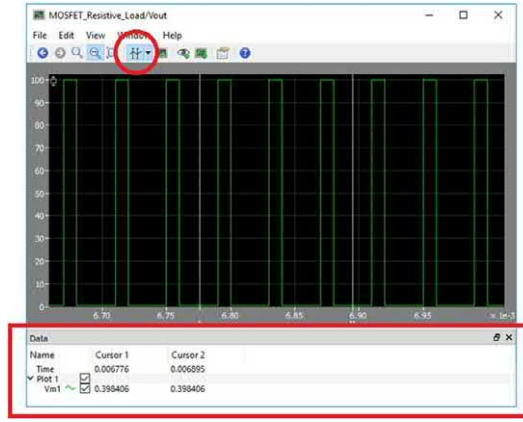


**FIG. 3.17** Adding cursors to the scope.

Click on the small triangle behind the  icon. Click the "Delta" in appeared menu (Fig. 3.18).

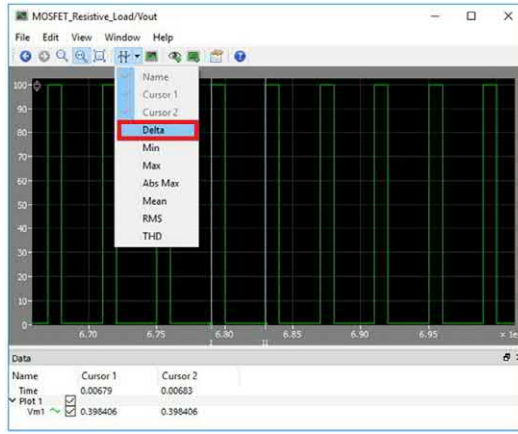


**FIG. 3.18** Measuring the difference between the two cursors.

A section named "Delta" will be added to the "Data" section. Move the cursors until the time difference between them reaches to 40 µs. When the time difference reaches the 40 µs, you capture exactly one period of output voltage between the two cursors (Fig. 3.19).

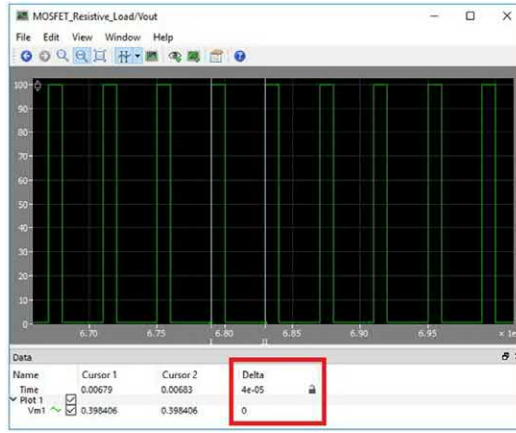


**FIG. 3.19** Time difference between the two cursors is $4e-5=4\times10^{-5}=40$ μs and the voltage difference is 0 V.

Click on the small triangle behind the  icon and click the "Mean" in the appeared menu (Fig. 3.20).

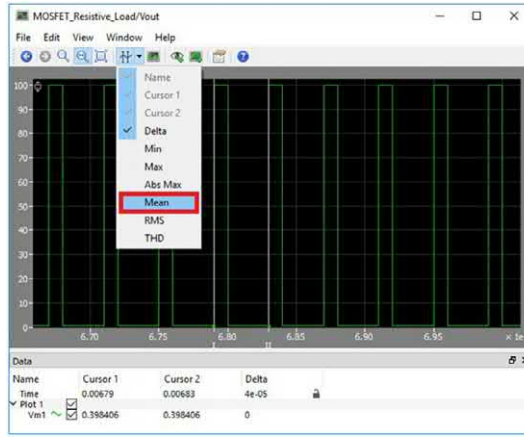


**FIG. 3.20** Measuring the mean value.

PLECS calculates and shows the average value of waveform captured between the two cursors (Fig. 3.21).

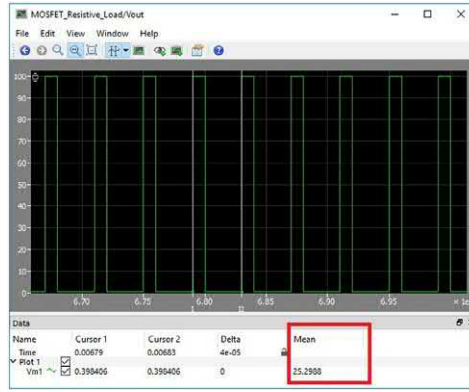


**FIG. 3.21** Load resistor average value is about 25.3 V.

In order to calculate the RMS value of output voltage, click on the small triangle behind the  icon and select the "RMS" in the appeared menu (Fig. 3.22).

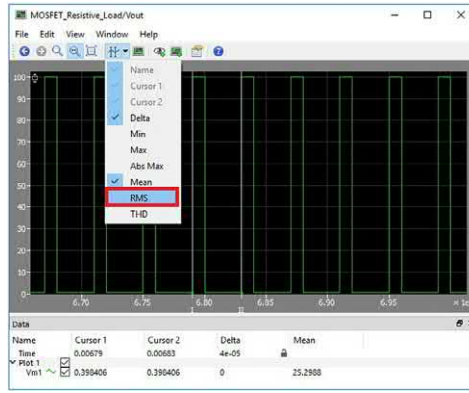


**FIG. 3.22** Measuring the RMS.

PLECS calculates and shows the RMS value of output voltage (Fig. 3.23).

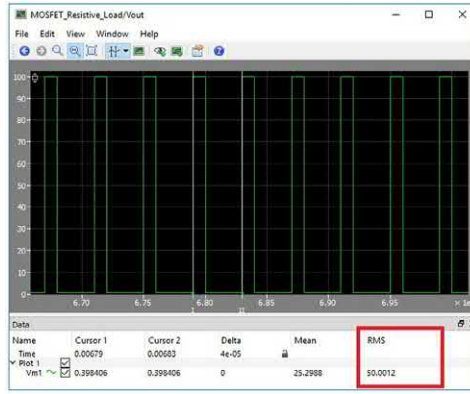


**FIG. 3.23** Load resistor voltage has an RMS about 50 V.

### 3.1.3 Measuring the power dissipated in the load resistor

You can measure the dissipated power in the load resistor easily using the "Probe" block (Fig. 3.24).

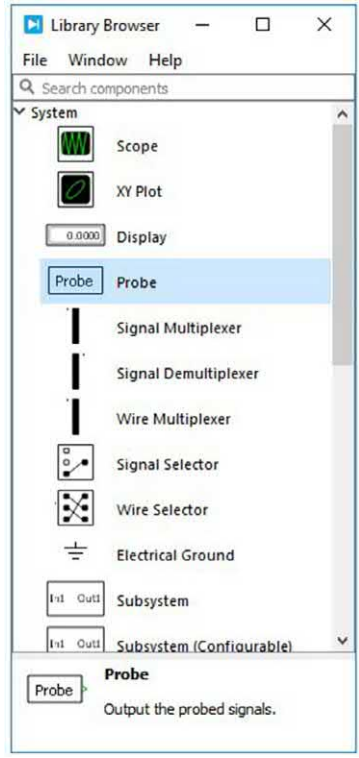


**FIG. 3.24** Probe block.

Add a "Probe" block to the schematic (Fig. 3.25).

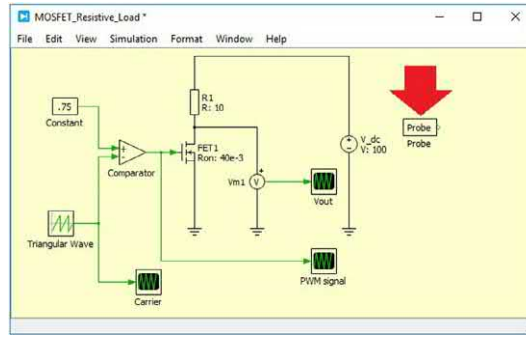


**FIG. 3.25** Adding a probe block to the schematic.

Double click the "Probe" block. The "Probe" block will be opened (Fig. 3.26).

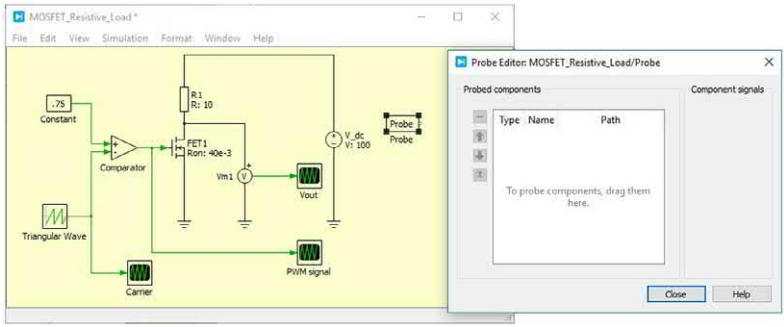


**FIG. 3.26** Double clicking on the probe block will open the block.

Drag and drop the resistor R1 into the "Probed components" window (Fig. 3.27).

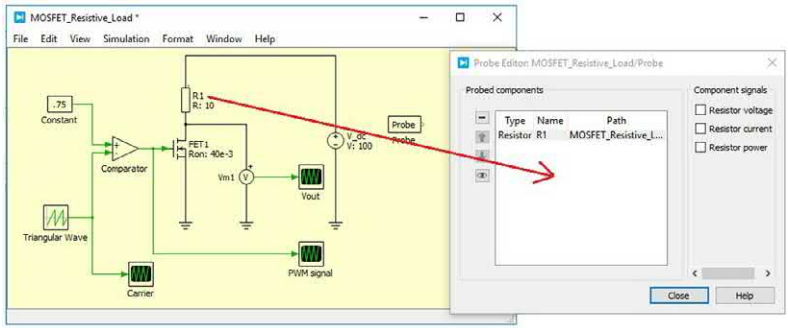


**FIG. 3.27** Drag and drop the resistor into the white region.

The "Probe" block will be changed to that shown in Fig. 3.28. Check the "Resistor power" box since we need to measure the dissipated power in the resistor.

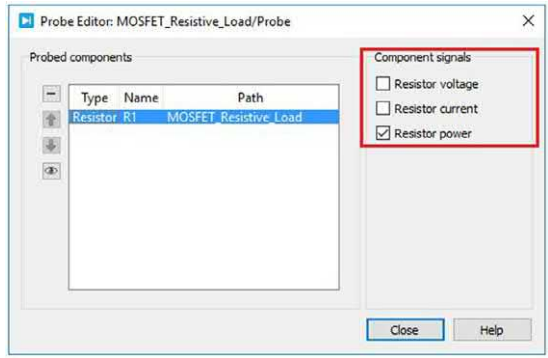


**FIG. 3.28** PLECS shows the measurable quantities for the dropped component.

You can drag and drop other components (passive components, semiconductor switches, electrical machines, etc.) into the "Probe" block and "Probe" block shows you the measurable quantities based on the dropped components. So you can use the "Probe" block with other types of components. It is not limited only to resistors.

Connect the output of the "Probe" block to a scope. We named the scope as "Resistor power" to understand the type of waveform inside it easily (Fig. 3.29).

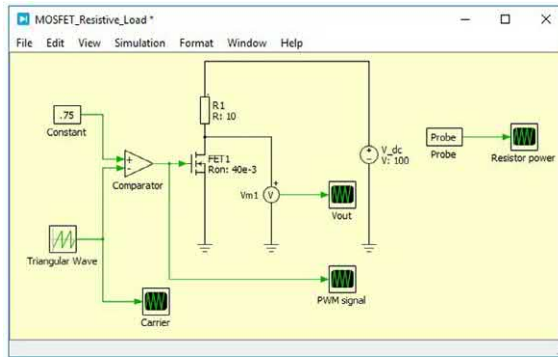


**FIG. 3.29** Connecting the probe block to a scope.

If we run the simulation, we will see the resistor power waveform (Fig. 3.30).

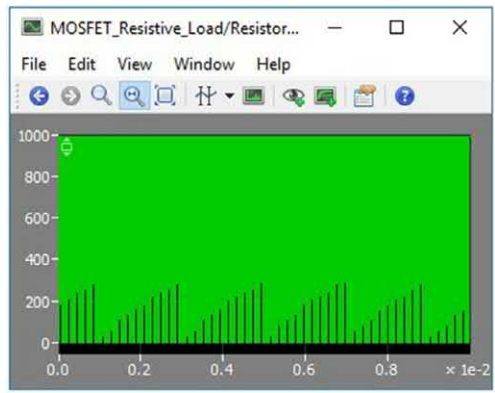


**FIG. 3.30** Resistor power waveform ("Resistor power" scope).

Zoom in the waveform to get a better view using the magnifier icon (Fig. 3.31).

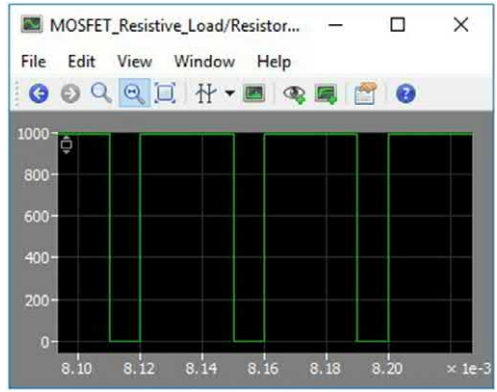


**FIG. 3.31** Zooming the resistor power waveform.

You can measure the average value of dissipated power using the aforementioned techniques (Fig. 3.32).

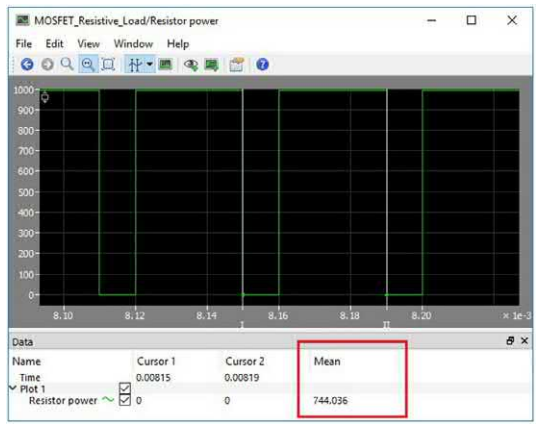


**FIG. 3.32** Average (mean value) of the power waveform.

### 3.1.4 Subsystem block

Consider the schematic shown in Fig. 3.33. The schematic looks crowded and complicated although it is a simple circuit. We can hide some details and keep the schematics simple with the aid of "Subsystem" block (Fig. 3.34).

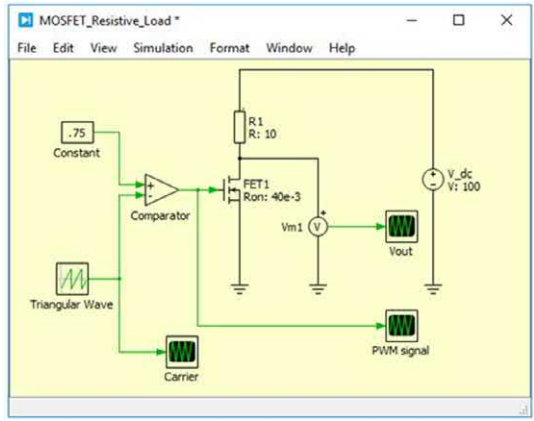


**FIG. 3.33** Schematic seems crowded to some extent.

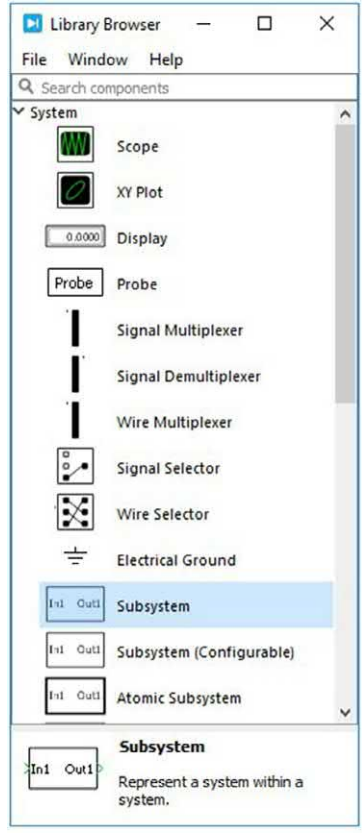


**FIG. 3.34** Subsystem block.

In this example, we show how you can make a subsystem for the PWM generation section of the simulation. To do this, left click on empty point in the schematic and draw a rectangle around the PWM generation blocks (Fig. 3.35).

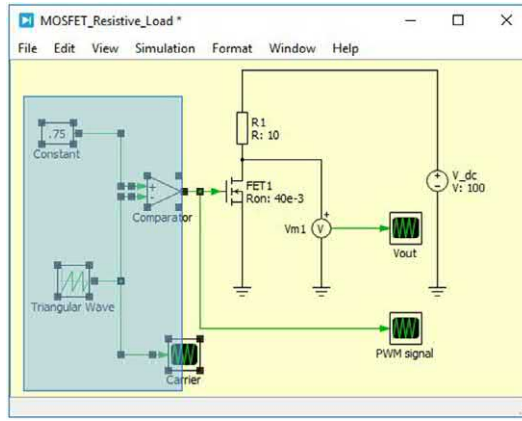


**FIG. 3.35** Selecting the PWM generation blocks.

After releasing the mouse button, the blue rectangle will disappear and the blocks inside it will be selected (Fig. 3.36).

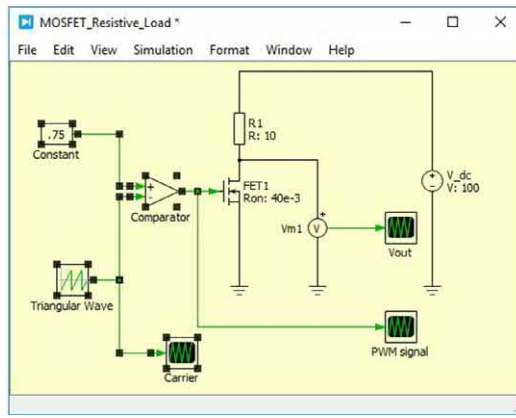


**FIG. 3.36** Selected blocks.

Cut the selected blocks with the aid of "Cut" (Fig. 3.37).

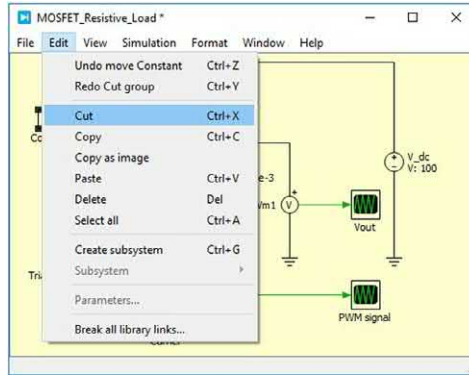


**FIG. 3.37** Cutting the selected blocks.

After Clicking the "Cut," selected blocks will be disappeared from the schematic and they are transferred to the Windows clipboard (Fig. 3.38).

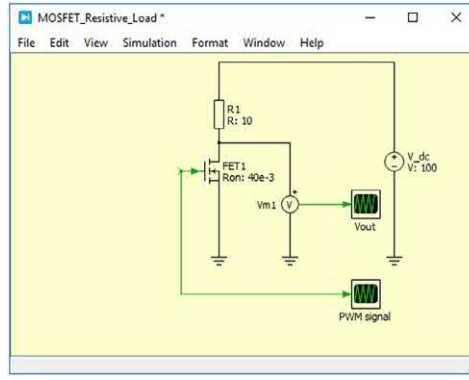


**FIG. 3.38** Schematic after cutting the selected blocks.

Place a subsystem block (see Fig. 3.39) inside the schematic.

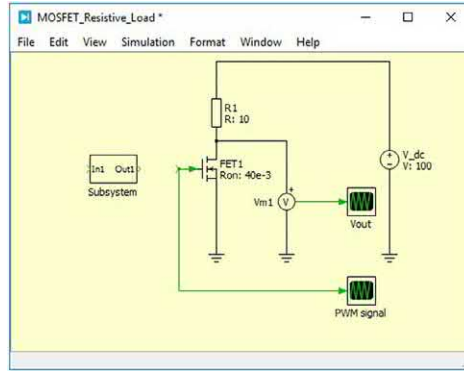


**FIG. 3.39** Adding a subsystem block to the schematic.

Double click on the placed subsystem label and rename it to "PWM Generator" (Fig. 3.40).

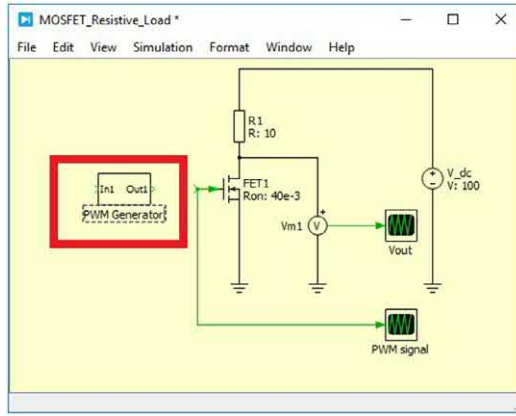


**FIG. 3.40** Renaming the subsystem block.

Double click on the subsystem block to see inside of it. As shown in Fig. 3.41, PLECS by default connects the input and outputs together.

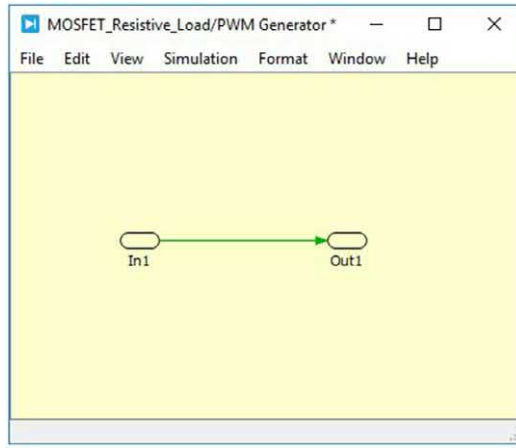


**FIG. 3.41** Opening the subsystem block.

Click on an empty point inside the subsystem block and draw a rectangle around the default blocks and press the keyboard Delete key to remove them (Figs. 3.42 and 3.43).

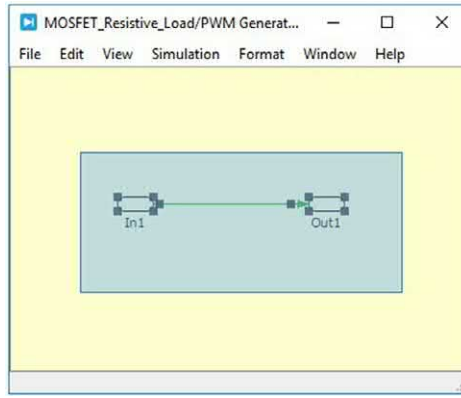


**FIG. 3.42** Selecting the content of the subsystem block.


**FIG. 3.43** Removing the content of the subsystem block.

Paste the content of Windows clipboard (the cut PWM generation circuit) into the subsystem (Figs. 3.44 and 3.45).

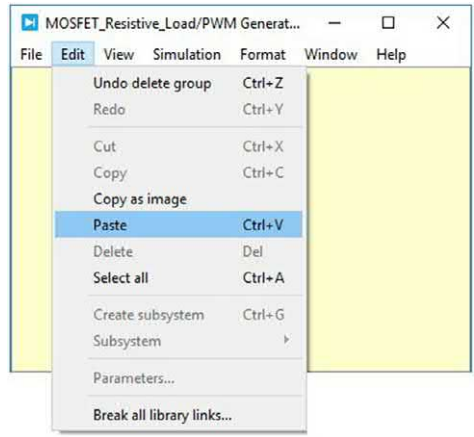


**FIG. 3.44** Paste the PWM generation blocks to the subsystem block.

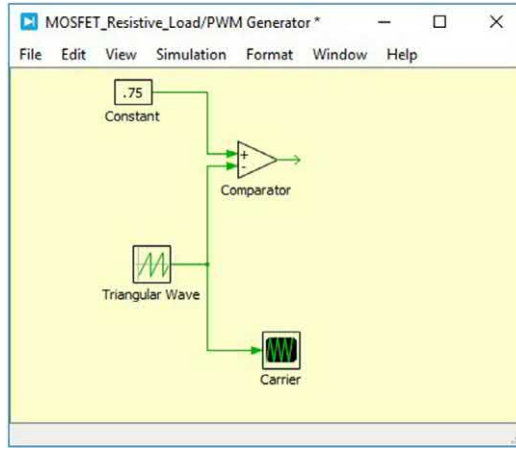


**FIG. 3.45** Subsystem block after pasting the PWM generation blocks.

Change the schematic inside the subsystem to that shown in Fig. 3.46. Input/output port can be found under the System section of Library Browser (Fig. 3.47).

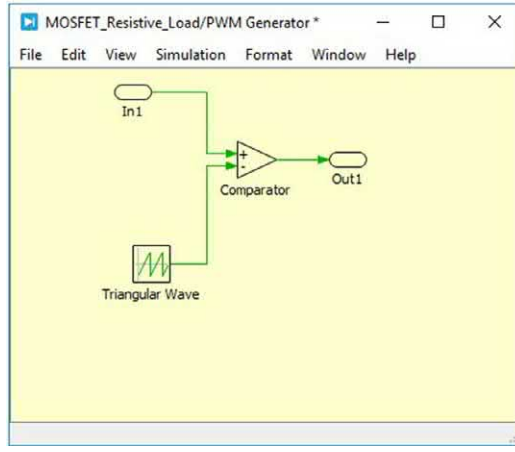


**FIG. 3.46** Adding input and output port to the subsystem.

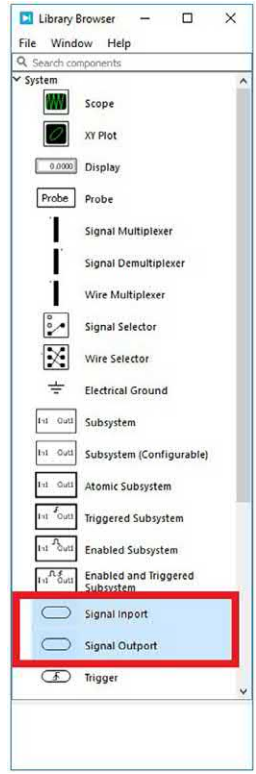


**FIG. 3.47** "Signal Inport" and "Signal Outport" blocks.

Add meaningful labels to the input/output ports(see Fig. 3.48). Close the subsystem window and return to the main schematic. Schematic will appear as shown in Fig. 3.49 now.

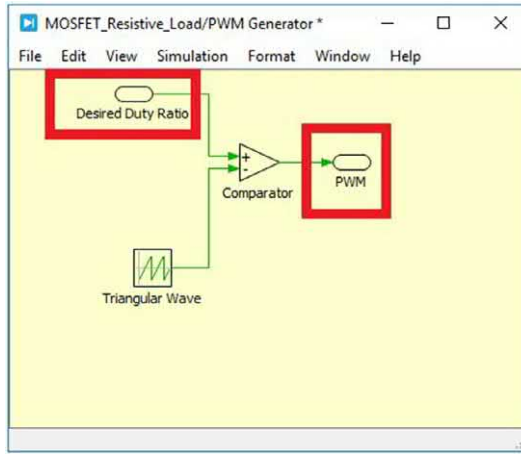


**FIG. 3.48** Renaming the input and output ports.

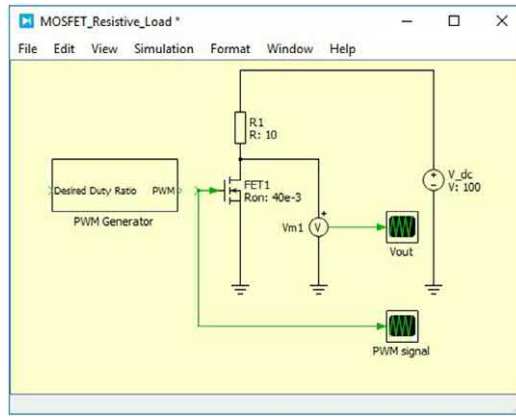


**FIG. 3.49** Schematic with "PWM Generator" subsystem block.

Change the schematic to that shown in Fig. 3.50.

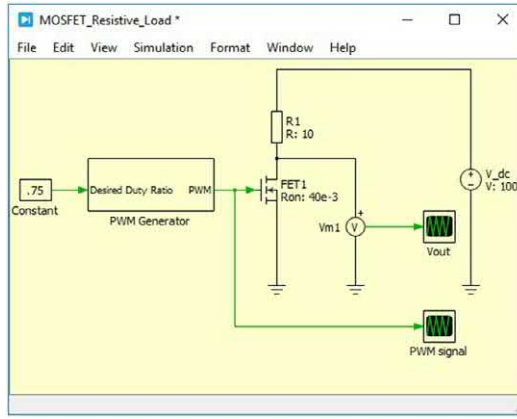


**FIG. 3.50** Connecting the "PWM Generator" subsystem to the rest of the circuit.

The schematic shown in Fig. 3.50 is more easily understandable in comparison to Fig. 3.33. Using the subsystem block inside of your simulations is suggested when it is possible. There is no limitation on the number of subsystems blocks inside your simulation.

### 3.1.5 Measuring the input power

You can measure the input source power in the same way you measured the dissipated power inside the load resistor. To measure the input source power, add a probe block to the schematic (Fig. 3.51).

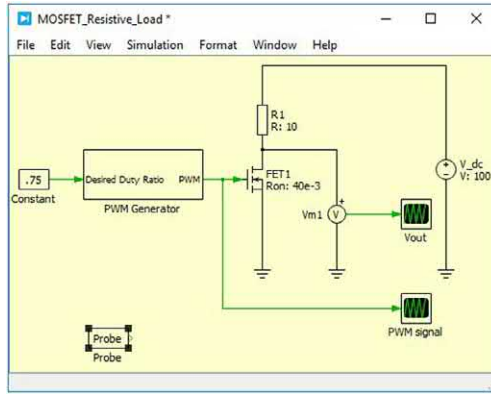


**FIG. 3.51** Adding a probe block to the schematic.

Double click on the probe block to open it (Fig. 3.52).

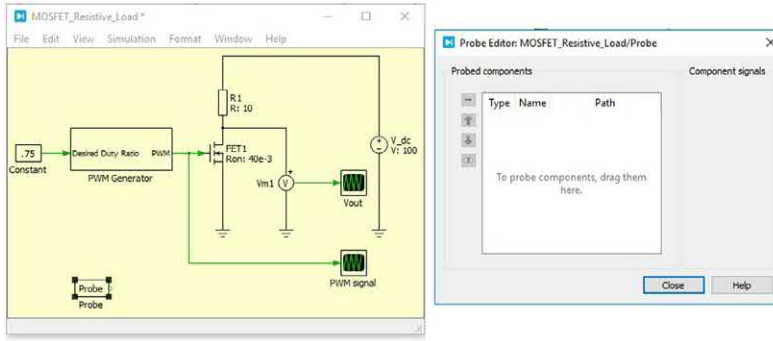


**FIG. 3.52** Opening the probe block.

Drag and drop the input DC source into the probe block. Check the "Source power" to measure the provided power (Fig. 3.53).

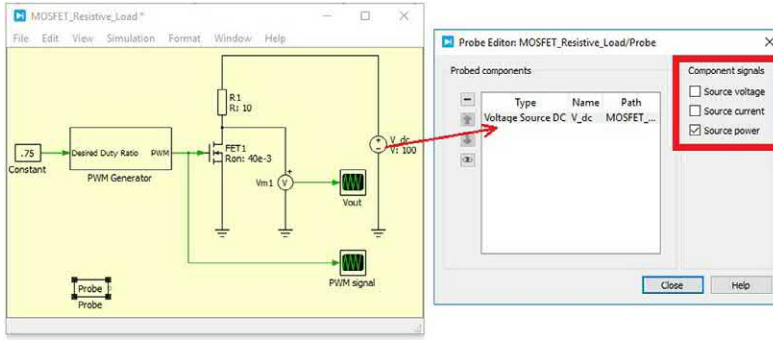


**FIG. 3.53** Drag and drop the input DC source into the white region.

Connect the probe block to a scope block. Name the scope as "Input Power" to remember its content (Fig. 3.54).

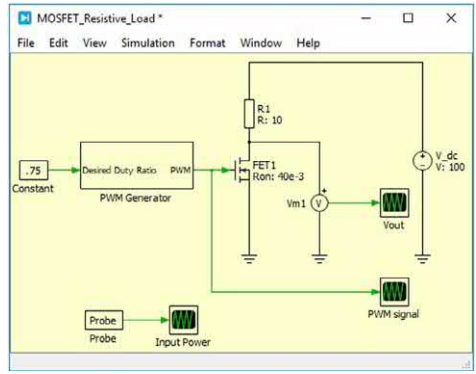


**FIG. 3.54** Connecting the output of probe block to a scope.

If we run the simulation, we obtain the power waveform shown in Fig. 3.55. Zoom in the waveform to obtain a better view (Fig. 3.56).

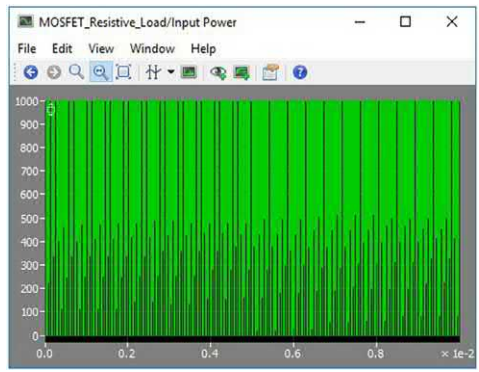


**FIG. 3.55** Input power waveform.

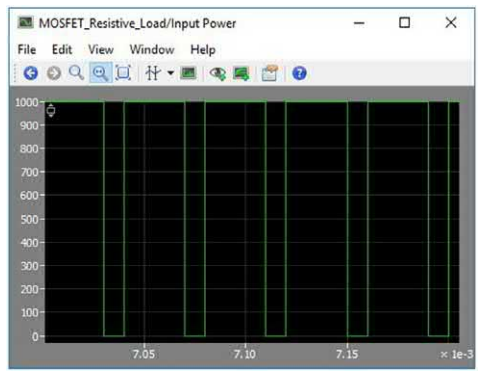


**FIG. 3.56** Zooming the input power waveform.

In order to measure the average input power, you must capture a period of input power waveform between the two cursors. Click the cursor icon and capture a period of the input power waveform between the two cursors (Fig. 3.57).

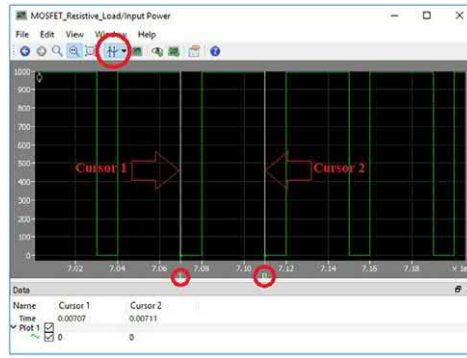


**FIG. 3.57** Adding cursors to the waveform.

Click the small triangle icon behind the cursor icon and select the "Mean" (Fig. 3.58).

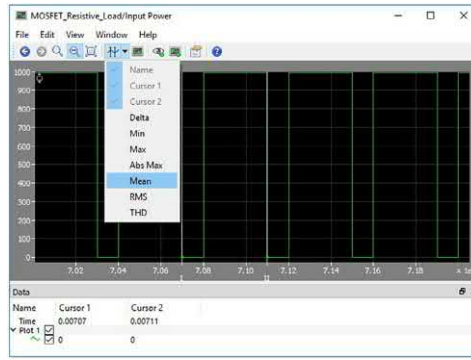


**FIG. 3.58** Measuring the average input power.

PLECS calculates the average input power and displays it (Fig. 3.59).

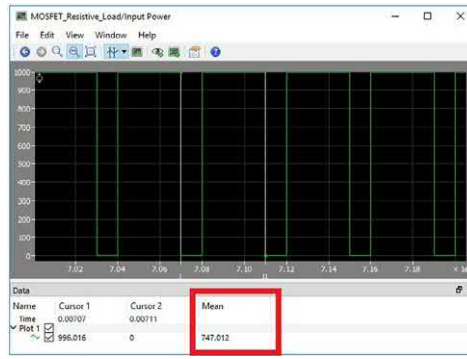


**FIG. 3.59** Average input power is about 747 W.

The calculated power is a little bit greater than the load resistor power since the MOSFET dissipated some power.

### 3.1.6 Generating the PWM signal using ready-to-use blocks

Up to now, we simulate the circuit with our own PWM generation circuit. PLECS contains plenty of ready-to-use PWM generator. They can be found in the "Modulator" section of Library Browser (Fig. 3.60).

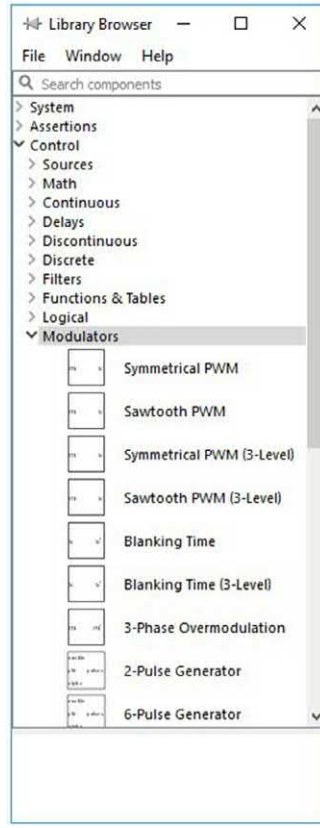


**FIG. 3.60** Different modulator blocks are available in PLECS.

You can see the information about each modulator simply by right clicking on the block name and selecting the "Help" from appeared menu (Figs. 3.61 and 3.62).

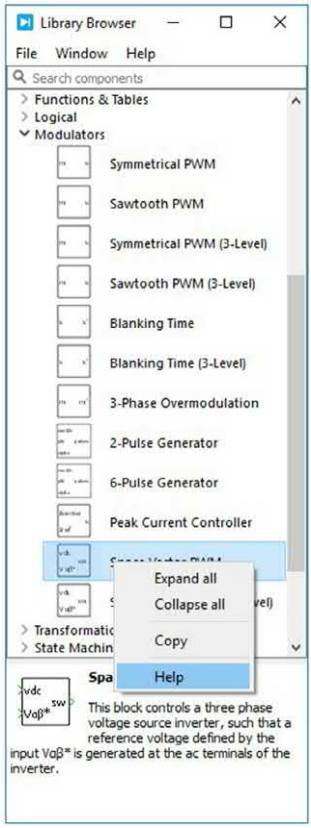


**FIG. 3.61** You can see the blocks documentation by right click on them and select the Help.

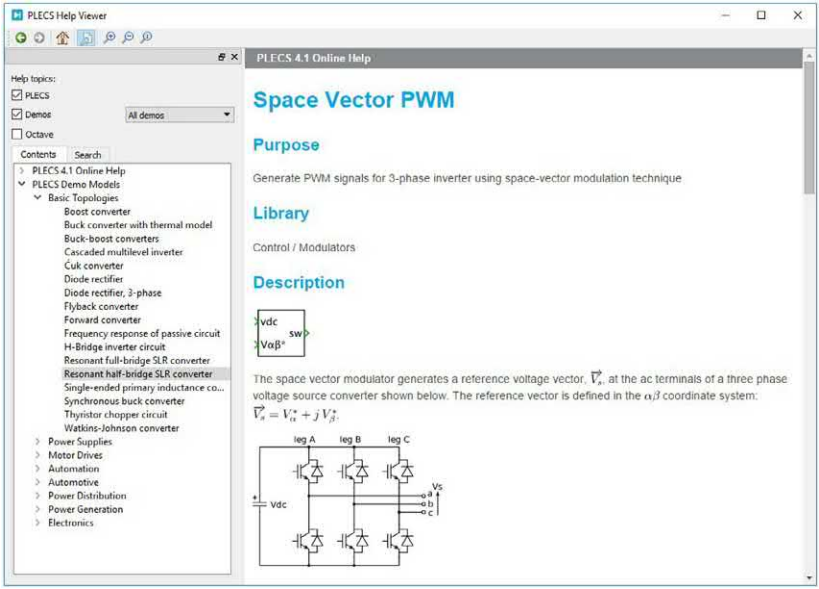


**FIG. 3.62** Space Vector PWM modulator block documentation.

Instead of simulating the circuit in the way shown in Fig. 3.50, one can use the "Sawtooth PWM" block as shown in Fig. 3.63 (Fig. 3.64). "Sawtooth PWM" block settings is shown in Fig. 3.65.

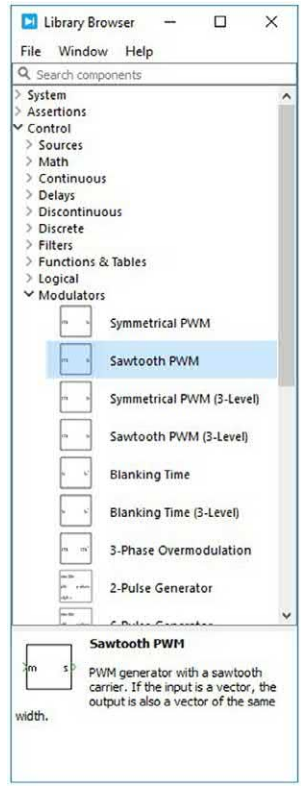


**FIG. 3.63** Sawtooth PWM block.

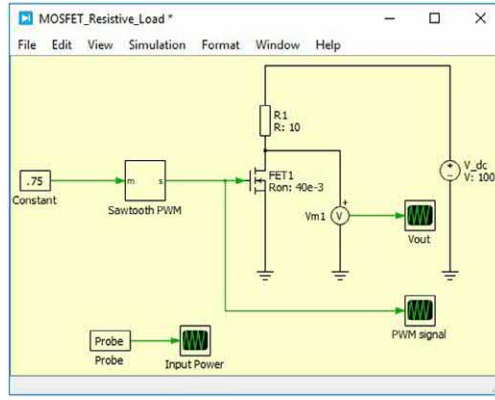


**FIG. 3.64** Adding the Sawtooth PWM block to the circuit.

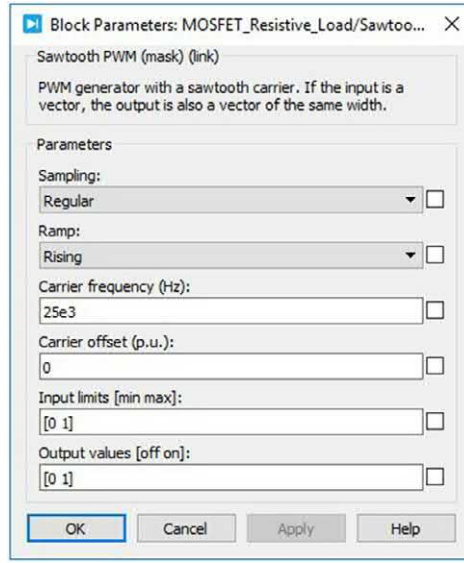


**FIG. 3.65** Sawtooth PWM block settings. Using this setting, gate signal has frequency of 25 KHz and duty ratio equal to the "m" input of block. Since "m" is connected to a constant block of 0.75, duty ratio will be 0.75.

## 3.2 Example 3.2: Uncontrolled single-phase half-wave rectifier

In this example, we will simulate a single-phase half-wave bridge rectifier. Output voltage magnitude is not controllable since the used switch is diode.

### 3.2.1 Preparing the simulation

Assume a rectifier with RL load as shown in Fig. 3.66. The diode block can be found in the "Power Semiconductors" section of Library Browser (Fig. 3.67). Components settings are shown in Figs. 3.68 and 3.69. Model of a forward biased diode is shown in Fig. 3.70. PLECS assumes open circuit to model reverse biased diodes.

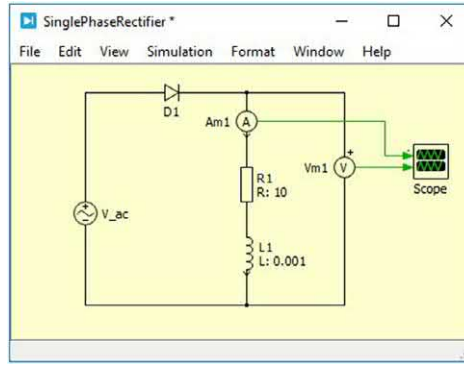


**FIG. 3.66** Simple single-phase half-bridge rectifier.

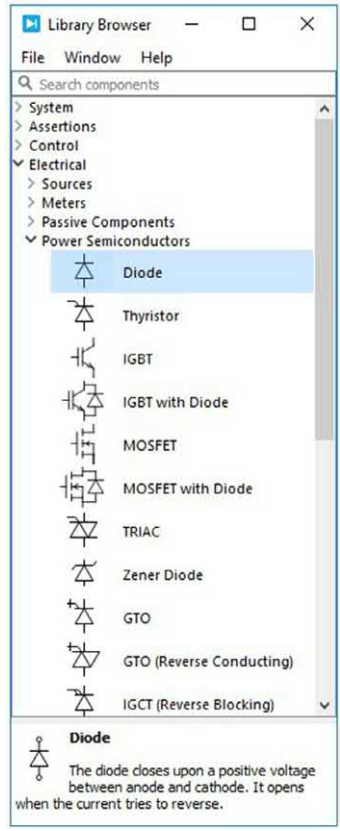


**FIG. 3.67** Diode block.

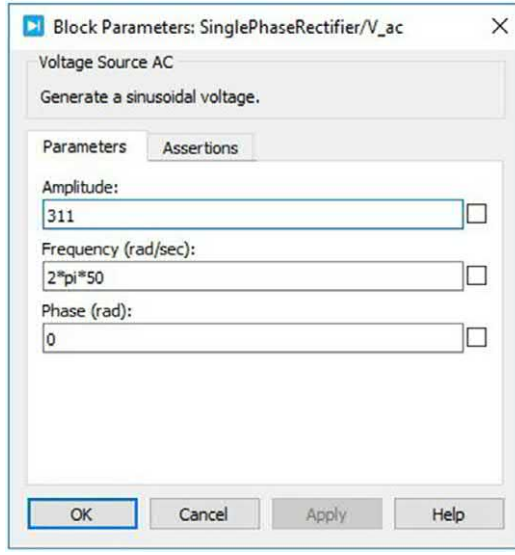


**FIG. 3.68** Input AC source settings.

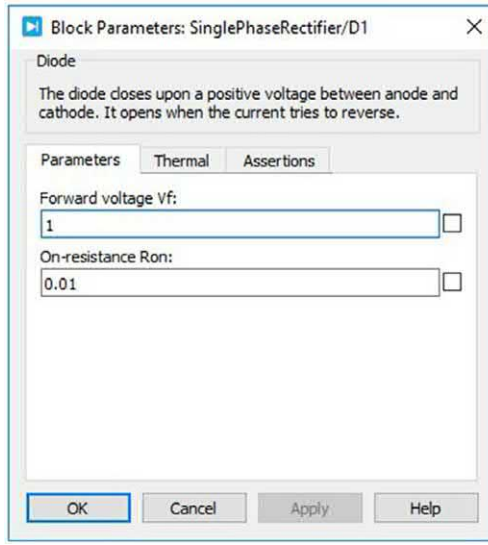


**FIG. 3.69** Diode settings.

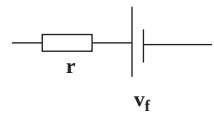


**FIG. 3.70** Forward biased diode.

If we do the simulation with the settings shown in Fig. 3.71, we will obtain the results shown in Fig. 3.72.

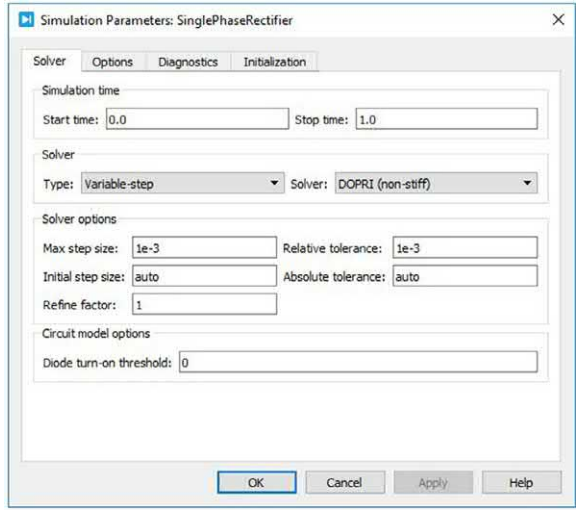


**FIG. 3.71** Simulation parameters.

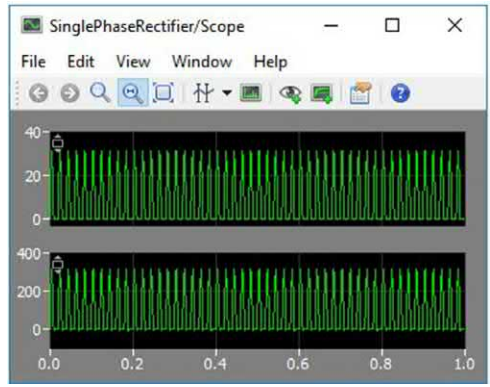


**FIG. 3.72** Simulation results. Upper axis shows current, while the lower one shows voltage.

Zoom the window to obtain a better view (Fig. 3.73).

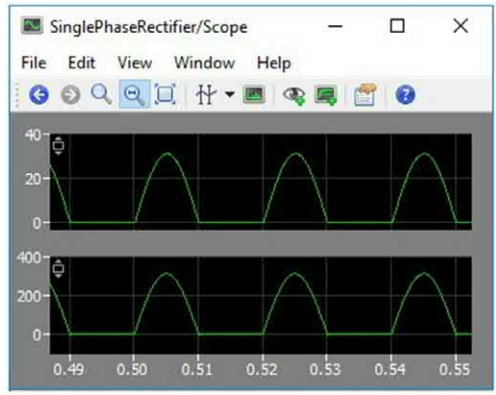


**FIG. 3.73** Zooming in the results.

### 3.2.2 Harmonic content of output

Using PLECS, one can obtain the harmonic content of waveforms easily. For example, in this example, we show how one can obtain the harmonic content of output voltage. Turn on the cursors and capture one period of waveforms. Select the captured waveform from the steady-state part of graph, i.e., where transients finish.

Waveforms inside Fig. 3.74 have no label. So, it is a good idea to show what is what in the first steps. To add labels, double click on the "Plot 1" and "Plot 2" and write suitable names (see Fig 3.75). Upper waveform shows the load current and lower one shows the load voltage (see Fig. 3.76). After writing the suitable names, PLECS shows them on the upper sections of the graph, so one can understand easily what they are.

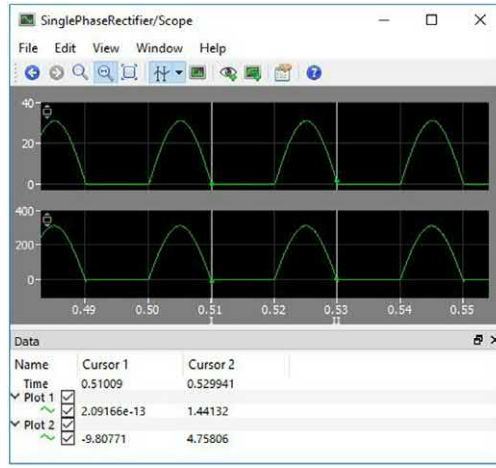


**FIG. 3.74** Capturing one period of waveforms with two cursors.

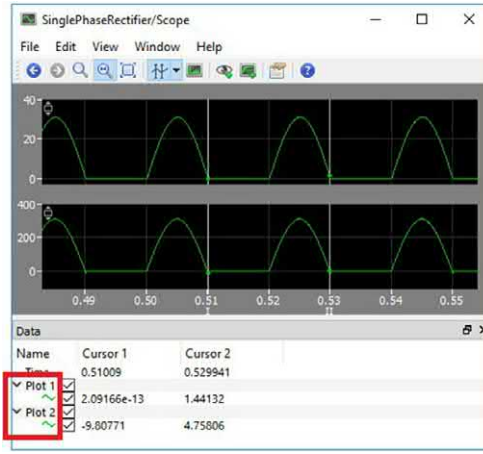


**FIG. 3.75** Waveforms seems meaningless since there is no descriptive labels.

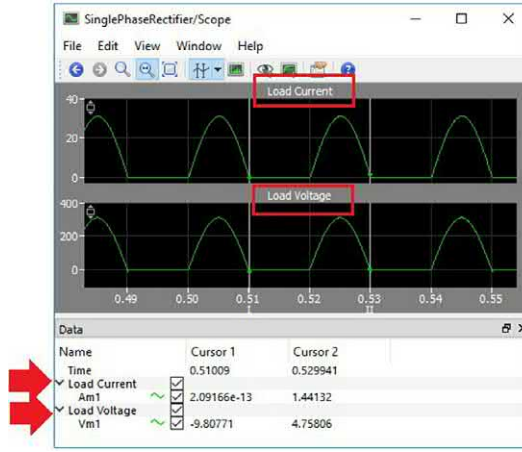


**FIG. 3.76** Adding descriptive labels to the scope.

We are ready to do the harmonic analysis now. To do this, click the "Fourier spectrum" icon (Fig. 3.77).

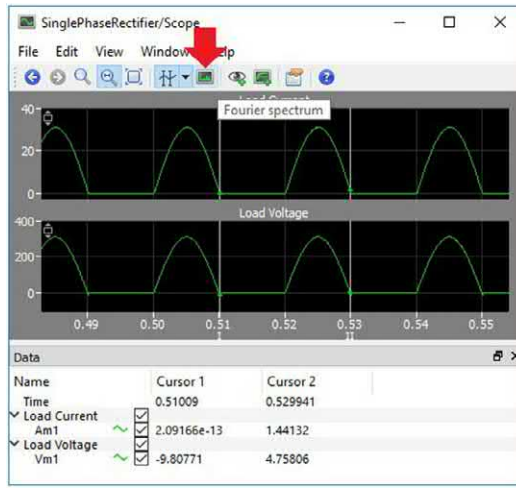


**FIG. 3.77** Fourier spectrum icon.

PLECS analyses the waveform captured between the cursors and opens a window to show the results. The opened window has three important sections (Fig. 3.78).

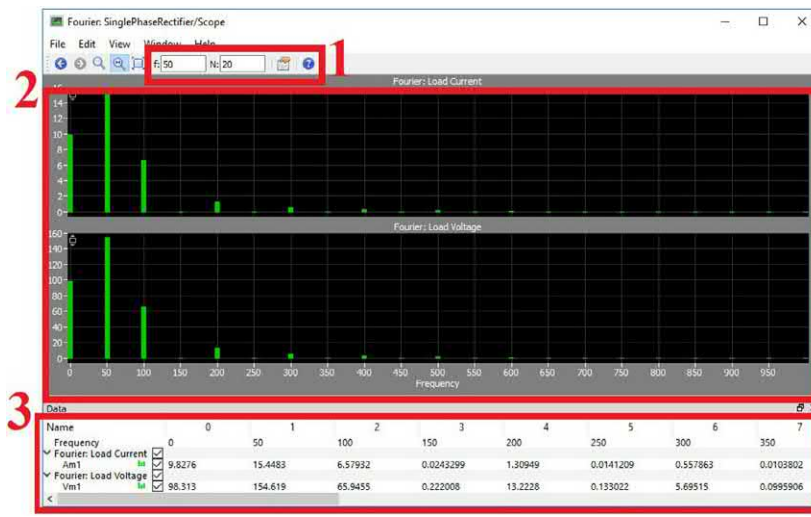


**FIG. 3.78** Fourier analysis result.

First section is composed of two text boxes: "f:" and "N:" text boxes. "f:" text box shows the fundamental frequency of waveform captured between the two cursors. "N:" box shows the number of harmonics involved in computation. By default, it is set to 20. Means PLECS calculate the harmonics up to 20th harmonic.

Second section shows the magnitude of harmonic graphically. It does not show the magnitude in dB. For instance, if waveform contains 110 sin $(2 \times \pi \times 1000)$, you will 110 at 1000 Hz not $20 \times \log(110) = 40.83$ dB.

Third section shows the harmonics magnitudes using numbers, so you can read them easily.

Some time you cannot capture exactly one period of output waveform between the two cursors. Assume a situation like that shown in Fig. 3.79. In this case, the fundamental frequency is calculated as 49.3469 Hz. instead of 50 Hz.

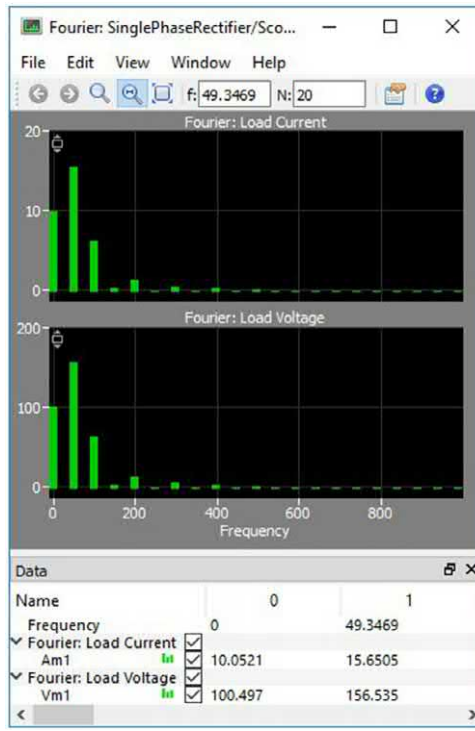


**FIG. 3.79** "f:" box does not equal 50 Hz.

In such cases, you can click on the "f:" box to correct the fundamental frequency. The window shown in Fig. 3.80 will appear.

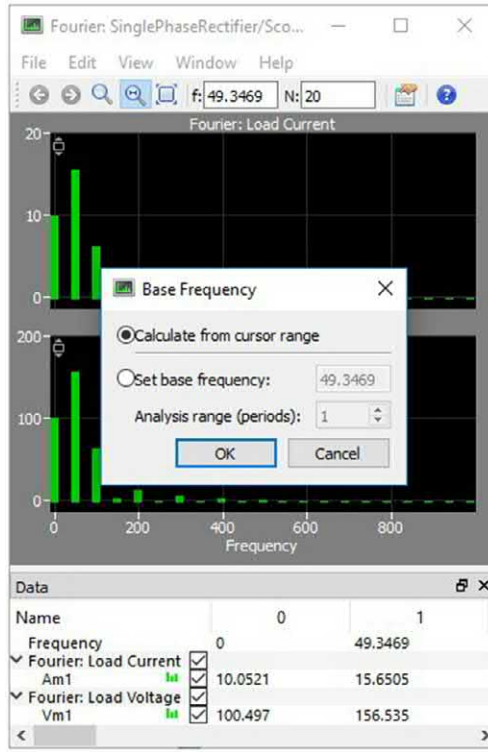


**FIG. 3.80** Base Frequency window.

Select "Set base frequency:" and right click the correct frequency. Click "OK" to apply the changes (Fig. 3.81).

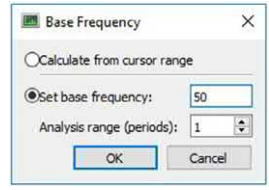


**FIG. 3.81** Setting the fundamental frequency.

As shown in Fig. 3.82, the fundamental frequency will changes to the new value. You can set the desired number of harmonics to be analyzed by clicking on the "N:" box and write the desired number of harmonics.

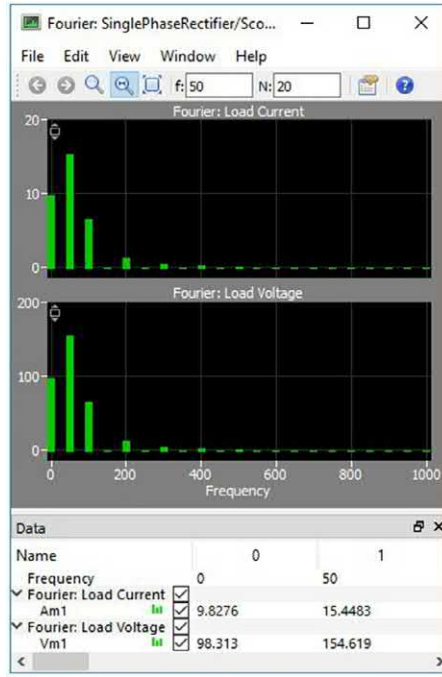


**FIG. 3.82** Analysis results.

### 3.2.3 Measuring the RMS values of voltages/currents

You can measure the RMS value of waveforms easily. Add cursors to the graph and capture one period of waveform (Fig. 3.83).

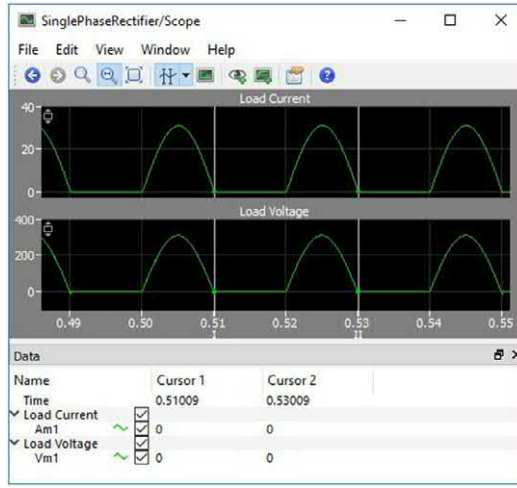


**FIG. 3.83** Capturing one period of output waveforms.

Click the small triangle behind the cursors icon and select the "RMS" (Fig. 3.84).

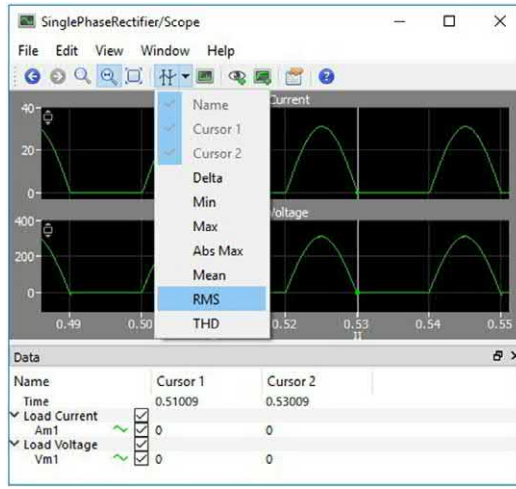


**FIG. 3.84** Calculating the RMS value.

PLECS calculates and shows the RMS value of waveforms. Load current and voltage have RMS of 15.45 A and 154.62 V, respectively (Fig. 3.85).

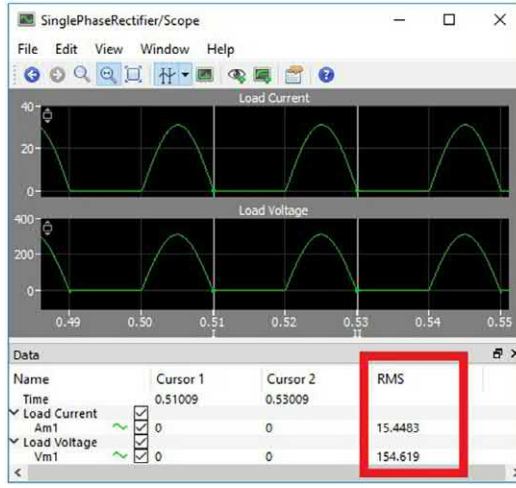


**FIG. 3.85** Load current and load voltage RMS values are calculated as 15.4483 A and 154.619 V, respectively.

### 3.2.4 Capturing a period of output voltage/current

Sometime it is difficult to capture one period of waveforms exactly. In this case, you can ask the PLECS to do that by itself. For example, in the circuit of Fig. 3.66, the load voltage/current waveform period is $\frac{1}{50\,\text{Hz}} = 20\,\text{ms} = 0.02\,\text{s}$, since the source frequency is 50 Hz.

We click on the small triangle behind the cursor icon and select the "Delta" (Fig. 3.86).

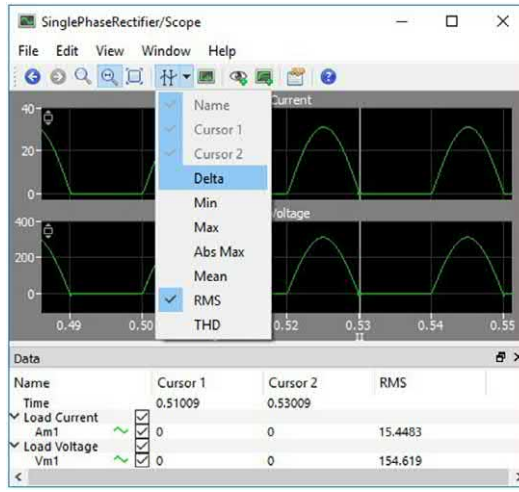


**FIG. 3.86** Measuring the difference between the two cursors.

The Delta section is added to the "Data." In this case, the user succeeds to capture exactly 0.02 S of the waveform. Note that the lock icon in the "Delta" section is open. Means you can slide each cursor independently (Fig. 3.87).

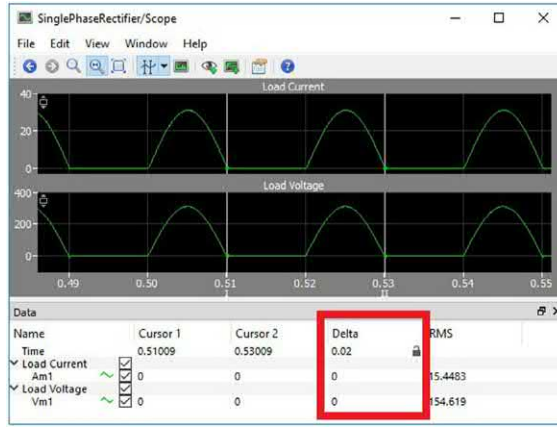


**FIG. 3.87** Difference between the two cursors.

If the captured interval is greater or less than the required time length, you can click on the shown value and right the correct value. For example, assume that instead of .02 s you captured .0187 s. in this case you click on the current value and enter the correct value. After writing the correct value, press Enter key on your keyboard (Figs. 3.88 and 3.89).

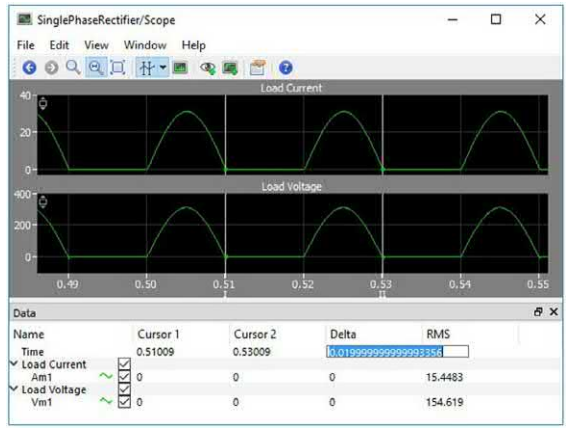


**FIG. 3.88** Double click the Delta box to enter the desired difference.

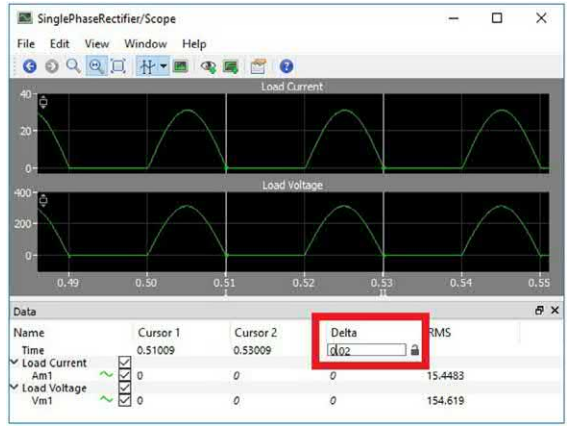


**FIG. 3.89** Entering the desired difference.

If you double click the lock icon, it will turn into a close lock. It means that the time difference between the two cursors keeps constant. So, if you slide one of the cursors, the other one slides automatically to keep the difference constant at the level written in the text box behind the lock icon (Fig. 3.90).

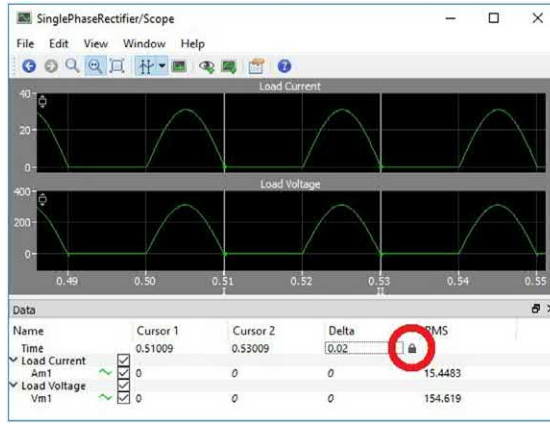


**FIG. 3.90** Closed lock shows that the difference between the two cursors keeps constant even if one of the cursor moves.

Double click on the closed lock icon to open the lock (Fig. 3.91).

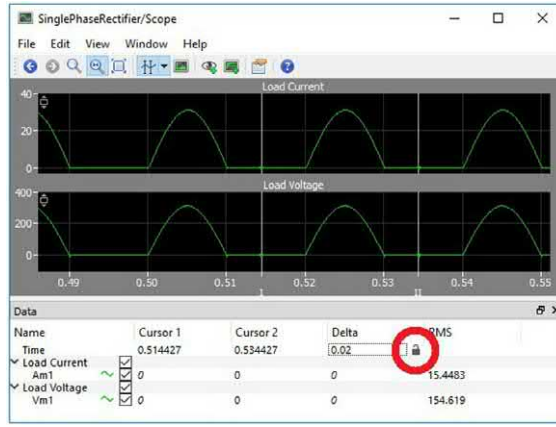


**FIG. 3.91** Open lock shows that you can move each of two cursors independent of the other one.

### 3.2.5 "Discrete RMS value" block

You can measure the RMS and average values of waveforms using the "Discrete RMS value" and "Discrete Mean Value" blocks as well (Figs. 3.92 and 3.93).

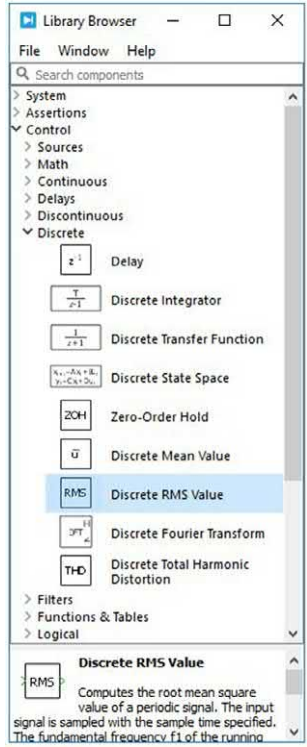


**FIG. 3.92** "Discrete RMS Value" block.

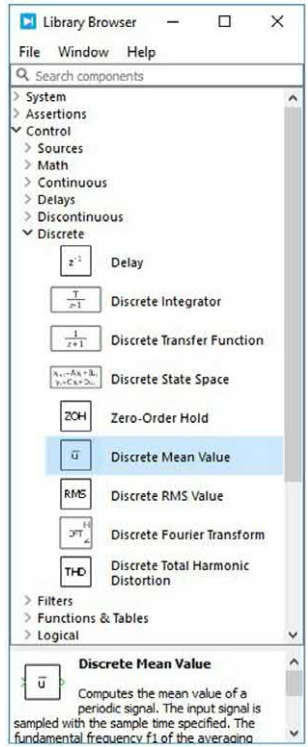


**FIG. 3.93** "Discrete Mean Value" block.

Assume that we want to find the RMS value of load voltage using the "Discrete RMS Value" block. To do this, add a "Discrete RMS Value" block to the schematic (Fig. 3.94).

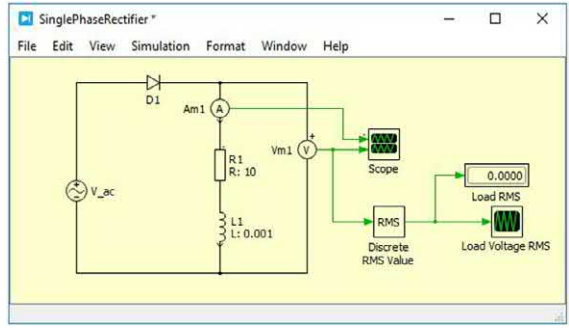


**FIG. 3.94** Adding the "Discrete RMS Value" block to the schematic.

Double click on the "Discrete RMS Value" block and do the settings as shown in Fig. 3.95.

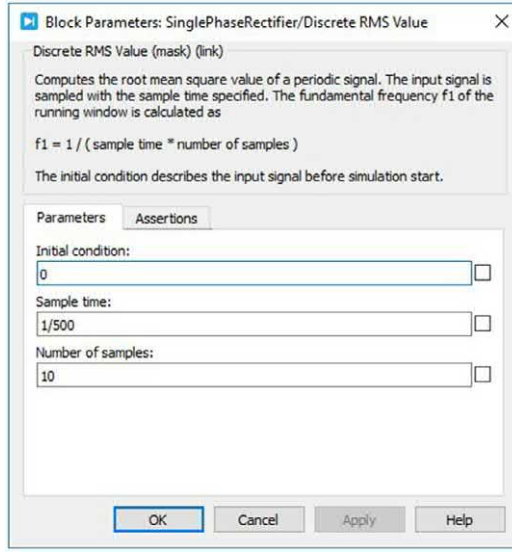


**FIG. 3.95** "Discrete RMS Value" block settings.

Since the output voltage frequency is 50 Hz, RMS calculation must be done in a $\frac{1}{50\text{Hz}} = 20\,\text{ms}$ interval. As shown in Fig. 3.95, the fundamental frequency of "Discrete RMS Value" is calculated with the aid of:

$$f = \frac{1}{\text{Sample time} \times \text{Number of samples}}$$

Since we enter the "Sample time:" box as $\frac{1}{500}$ and "Number of samples:" as 10, the fundamental frequency is calculated as:

$$f = \frac{1}{\frac{1}{500} \times 10} = 50\,\text{Hz}$$

So with this setting, PLECS calculates the RMS over the 0.02 s intervals. "Number of samples" can be selected as 10 for most of simulations but you can increase it if you need more accuracy. For example if "Number of samples" is increased to 20, "Sample time:" must be set to 0.001 to keep the fundamental frequency constant at 50 Hz.

If we run the simulation, we obtain the result shown in Fig. 3.96. RMS value is calculated as 154.73 V.

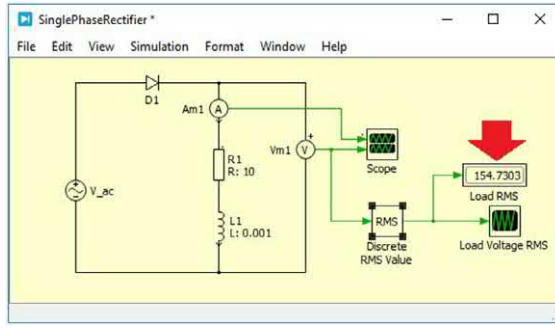


**FIG. 3.96** Calculated RMS value for load voltage.

If we open the "Load Voltage RMS" scope, we can read the RMS value as well (Figs. 3.97 and 3.98).

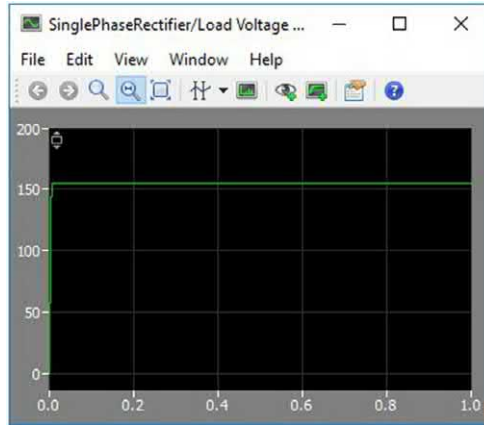


**FIG. 3.97** "Load Voltage RMS" scope waveform.

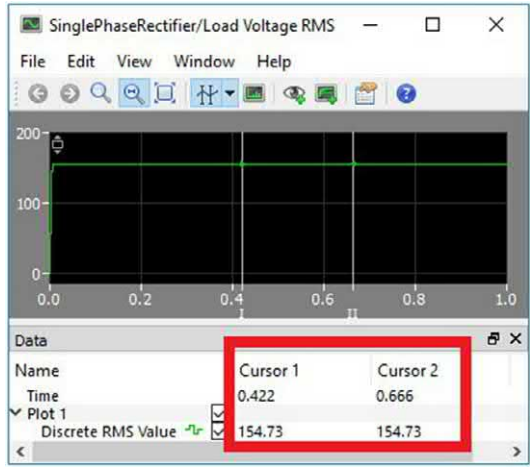


**FIG. 3.98** Adding cursors to the "Load Voltage RMS" scope to read the RMS value. Transient part of the graph is not important. Put the cursors into the steady-state region of the graph.

### 3.2.6 "Discrete mean value" block

You can measure the average output by using the "Discerte Mean Value" block as well. To measure the average of output voltage, change the schematic to that shown in Fig. 3.99.

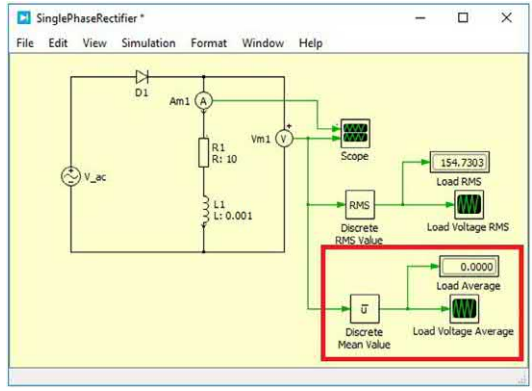


**FIG. 3.99** Adding the "Discrete Mean Value" block to the schematic.

Do the "Discrete Mean Value" block settings as shown in Fig. 3.100.

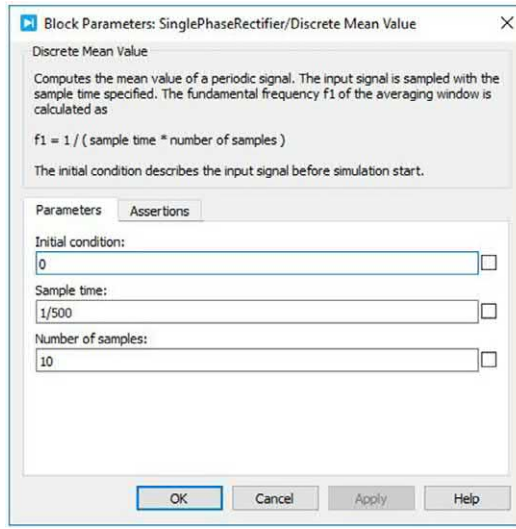


**FIG. 3.100** "Discrete Mean Value" block settings.

Since the output voltage frequency is 50 Hz, average (mean value) calculation must be done in a $\frac{1}{50\text{Hz}} = 20\,\text{ms}$ interval. As shown in Fig. 3.100, the fundamental frequency of "Discrete Mean Value" is calculated with the aid of:

$$f = \frac{1}{\text{Sample time} \times \text{Number of samples}}$$

Since we enter the "Sample time:" box as $\frac{1}{500}$ and "Number of samples:" as 10, the fundamental frequency is calculated as:

$$f = \frac{1}{\frac{1}{500} \times 10} = 50\,\text{Hz}$$

So with this setting, PLECS calculates the average over the 0.02 s intervals. "Number of samples" can be selected as 10 for most of simulations but you can increase it if you need more accuracy. For example if "Number of samples" is increased to 20, "Sample time:" must be set to 0.001 to keep the fundamental frequency constant at 50 Hz.

If we run the simulation, we obtain the result shown in Fig. 3.101. Mean value is calculated as 95.12 V.

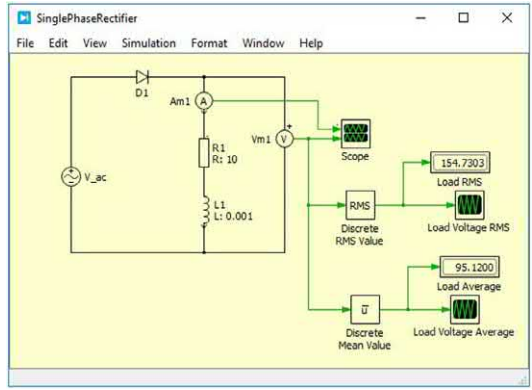


**FIG. 3.101** Load average voltage is about 95 V.

"Load Voltage Average" scope's waveform is shown in Fig. 3.102.

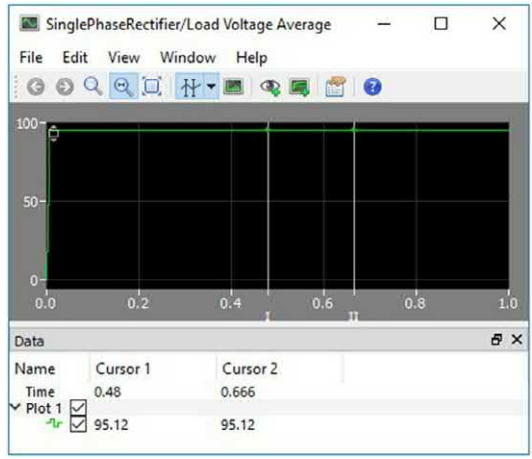


**FIG. 3.102** Adding cursors to the "Load Voltage Average" scope to read the RMS value. Transient part of the graph is not important. Put the cursors into the steady-state region of the graph.

### 3.2.7 Measuring the maximum/minimum of waveforms shown in the scope block

You can find the maximum/minimum of a waveform easily in PLECS. Capture maximum/minimum between the two cursors and click the Max/Min. PLECS find the maximum/minimum of the interval captured between the two cursors and shows the result (Figs. 3.103–3.106).

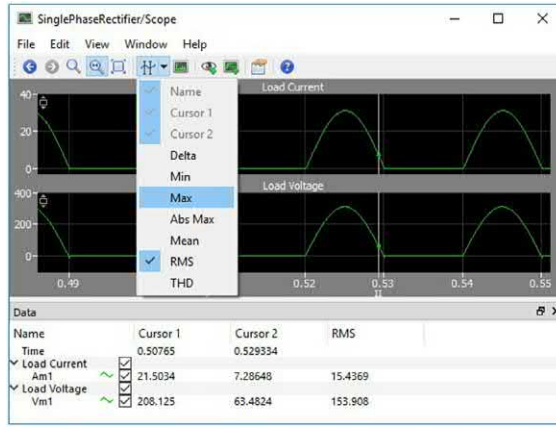


**FIG. 3.103** Calculating the maximum of the waveform captured between the two cursors.

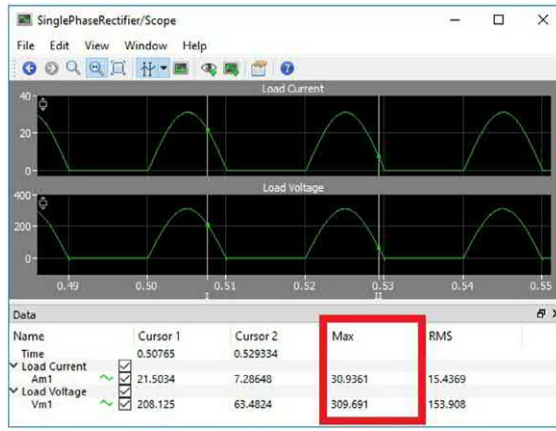


**FIG. 3.104** "Max" column shows the maximum of the waveform captured between the two cursors.

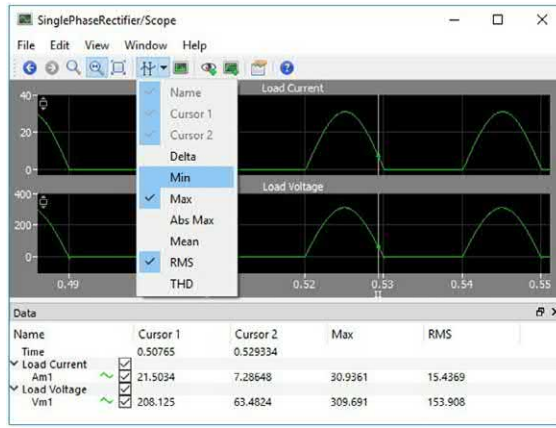


**FIG. 3.105** Calculating the minimum of the waveform captured between the two cursors.

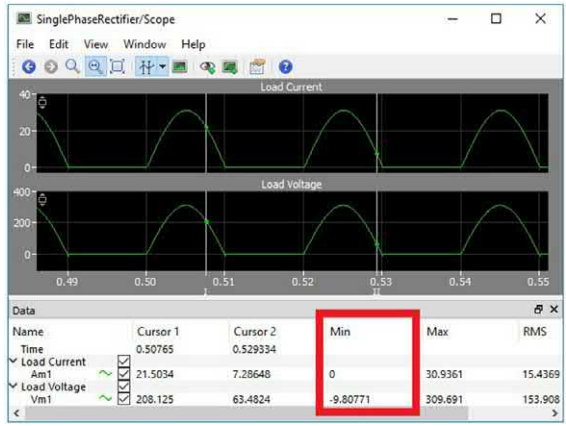


**FIG. 3.106** "Min" column shows the minimum of the waveform captured between the two cursors.

### 3.2.8 Obtaining the load instantaneous power

You can find instantaneous load power waveform by multiplying the load current to load voltage. Product block can be found in the Math section of Library Browser (Figs. 3.107 and 3.108).

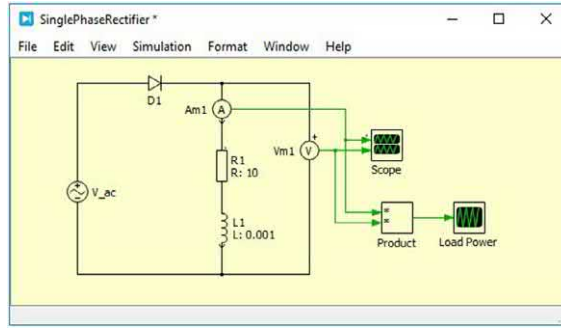


**FIG. 3.107** Calculating the load power.

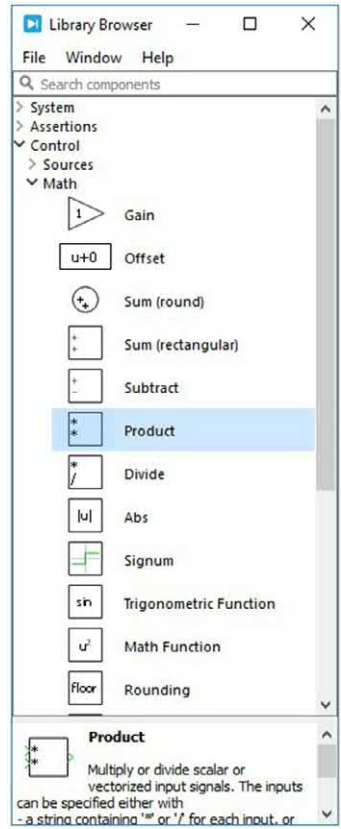


**FIG. 3.108** Product block.

After running the simulation, result shown in Fig. 3.109 will obtained.

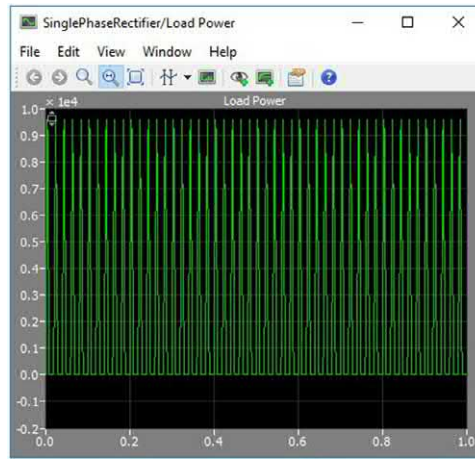


**FIG. 3.109** Load power waveform.

Zoom in the graph to obtain a better view (Fig. 3.110).

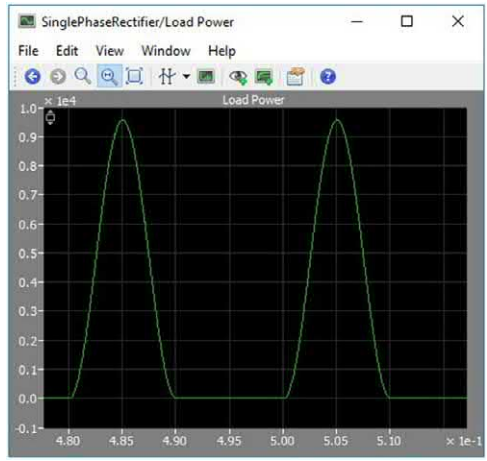


**FIG. 3.110** A closer look to load power waveform.

You can calculate the average power by capturing one period of power waveform and clicking the "Mean." PLECS calculates and shows the average load power (Figs. 3.111–3.113).

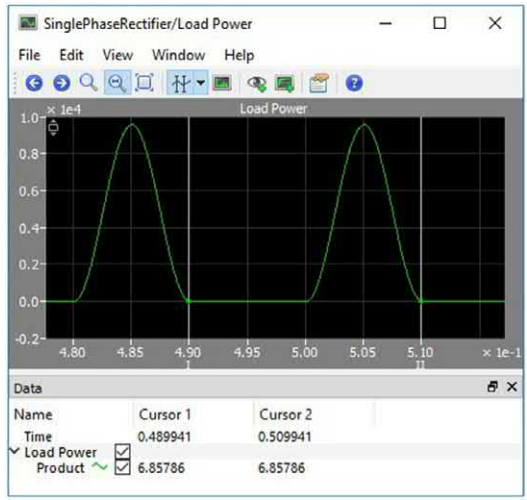


**FIG. 3.111** Capturing a period of the load power.

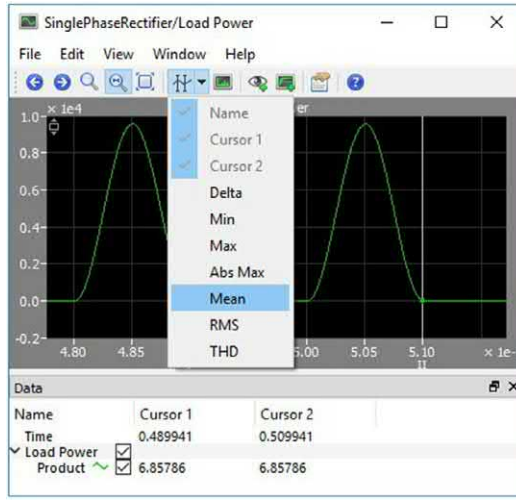


**FIG. 3.112** Calculating the mean value of load power.

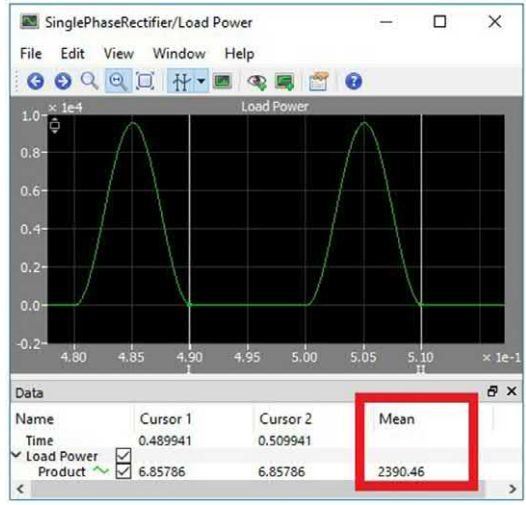


**FIG. 3.113** Average power is about 2.39 KW.

## 3.3 Example 3.3: Single-phase half-wave controlled rectifier

In this example we will simulate a single-phase half-wave rectifier. The output voltages magnitude can be controlled using the thyristor firing angle.

### 3.3.1 Preparing the simulation

Assume a schematic like Fig. 3.114. The thyristor block can be found in the "Power Semiconductors" section of Library Browser (Fig. 3.115). Input voltage source and pulse generator settings are shown in Figs. 3.116 and 3.117, respectively.

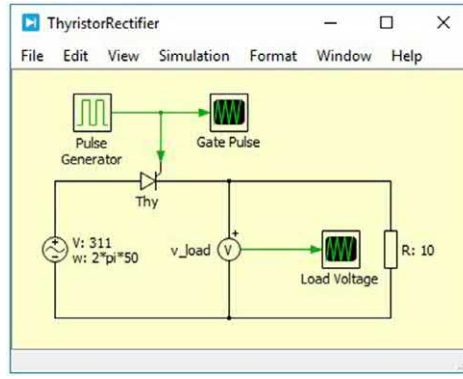


**FIG. 3.114** Controlled single-phase half-wave rectifier.

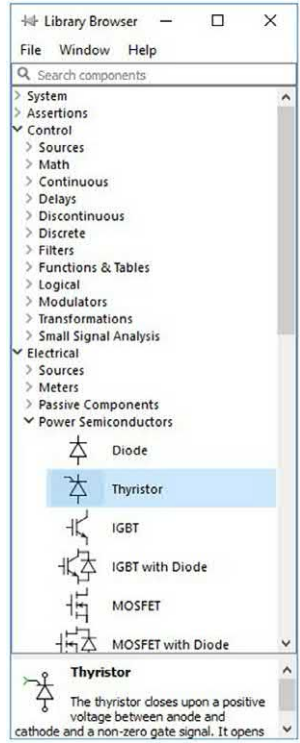


**FIG. 3.115** Thyristor block.

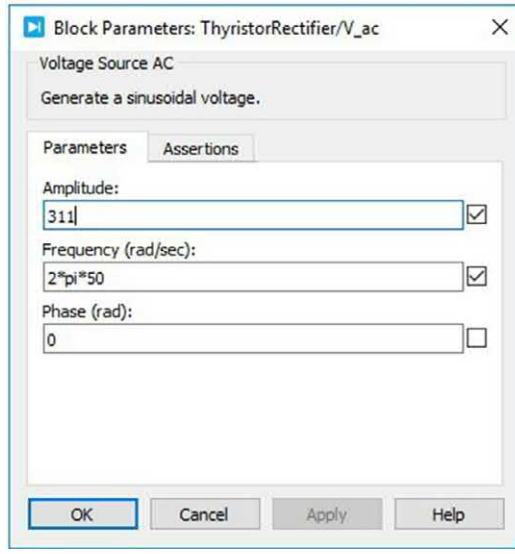


**FIG. 3.116** Input AC source settings.

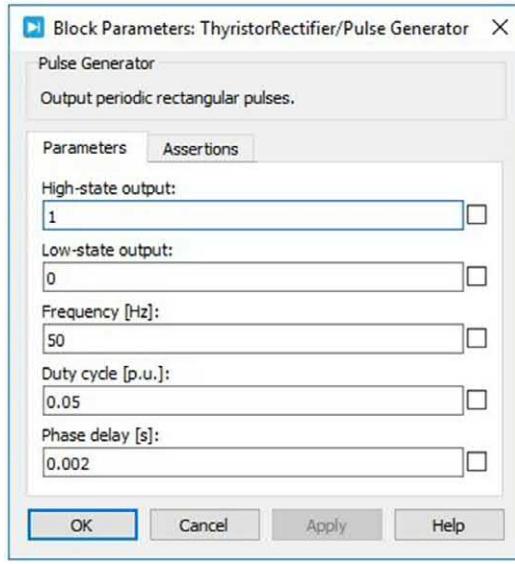


**FIG. 3.117** Pulse generator settings.

Using the settings shown in Fig. 3.118, the following signal is applied to the thyristor gate.

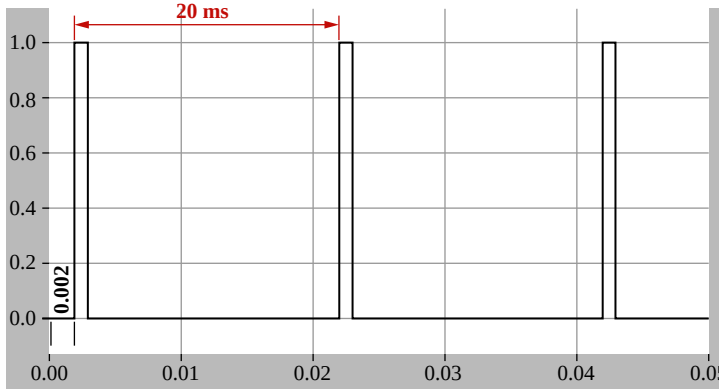


**FIG. 3.118** Thyristor gate pulses. Pulse width is $\text{Duty Cycle}\,[\text{p.u.}] \times \frac{1}{\text{Frequency}\,[\text{Hz}]} = 0.05 \times \frac{1}{50} = 1\,\text{ms}$.

If we run the simulation with the settings shown in Fig. 3.119, we obtain the results shown in Figs. 3.120 and 3.121.

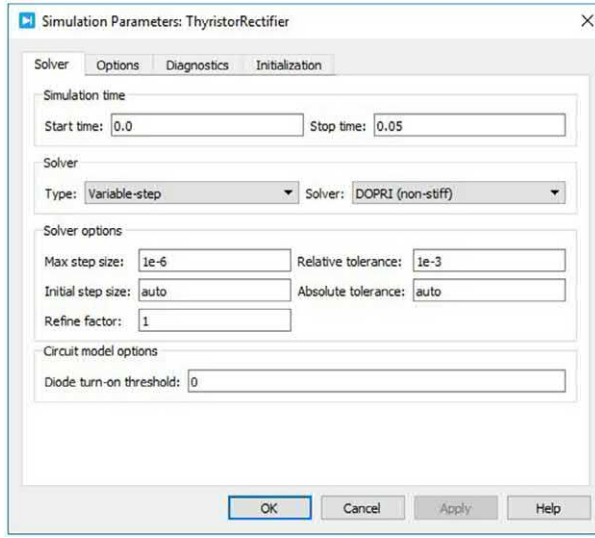


**FIG. 3.119** Simulation parameters.

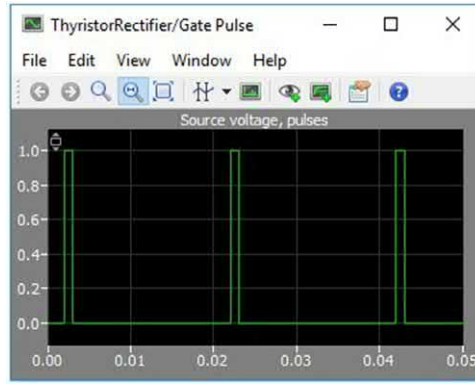


**FIG. 3.120** Thyristor gate signal.

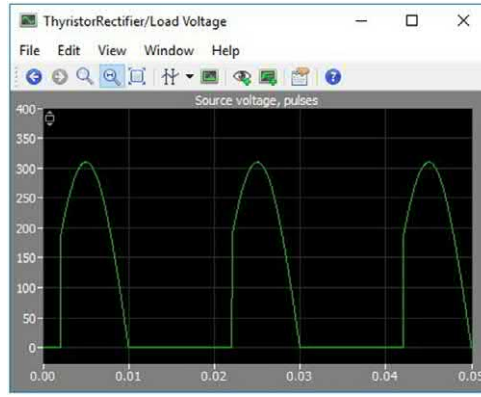


**FIG. 3.121** Load voltage.

### 3.3.2 Calculating the RMS, mean, max/min, etc.

You can measure the drawn waveform RMS, mean value, max/min, etc. using the techniques studied before.

## 3.4 Example 3.4: Single-phase full-wave controlled rectifier

In this example, we will simulate a single-phase full-wave rectifier. The output voltages magnitude can be controlled using the thyristor firing angle.

### 3.4.1 Preparing the simulation

Assume a full-wave controller rectifier shown in Fig. 3.122. The input source settings are shown in Fig. 3.123. The inductor L represents the internal impedance of the source.

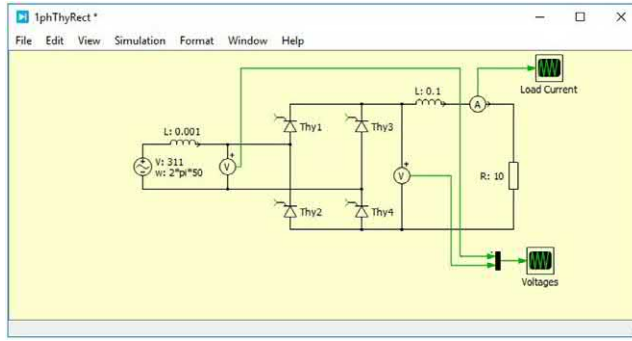


**FIG. 3.122** Controlled single-phase full-wave rectifier.

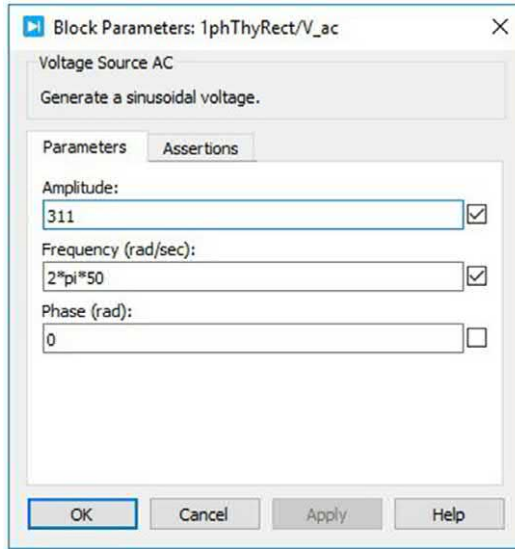


**FIG. 3.123** Input AC source settings.

You can trigger the thyristors using the "2-Pulse Generator" block (Fig. 3.124).

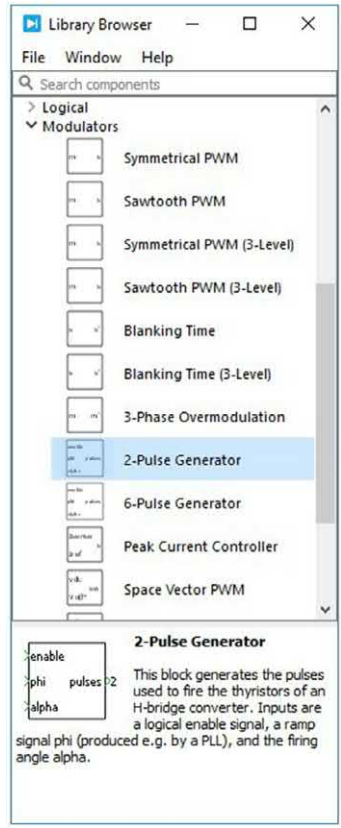


**FIG. 3.124** 2-Pulse Generator block.

Change the schematic to that shown in Fig. 3.125. "Clock" block can be found in the "Sources" section of the Library Browser as shown in Fig. 3.126. New blocks settings are shown in Figs. 3.127–3.129. The desired firing angle is entered into the constant block named "alpha." Here we assumed thyristors are fired at $\frac{\pi}{3}Rad = 60°$.

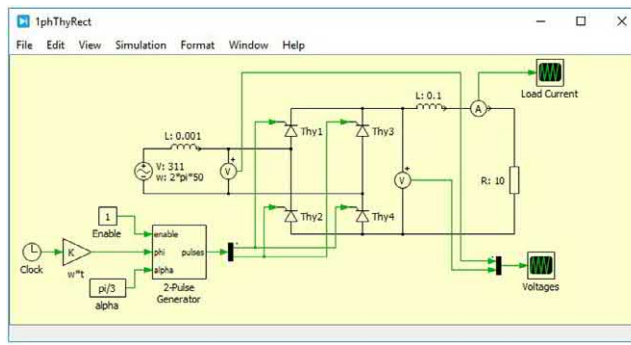


**FIG. 3.125** Adding the 2-Pulse Generator block to the schematic.

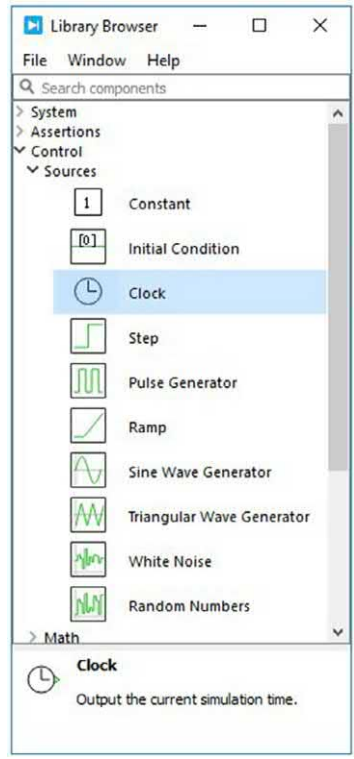


**FIG. 3.126** Clock block.

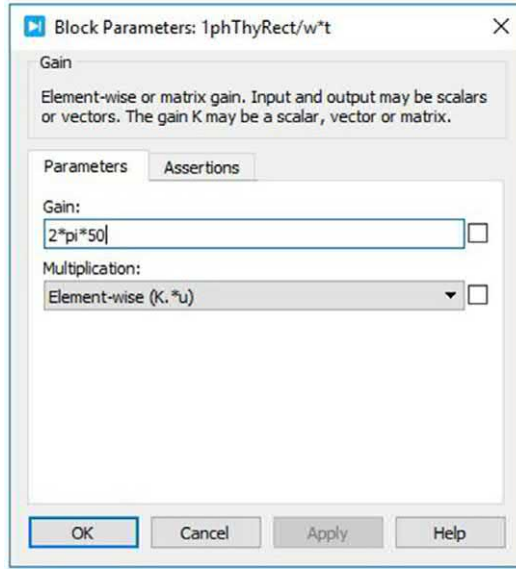


**FIG. 3.127** "w*t" block settings (see Fig. 3.125).

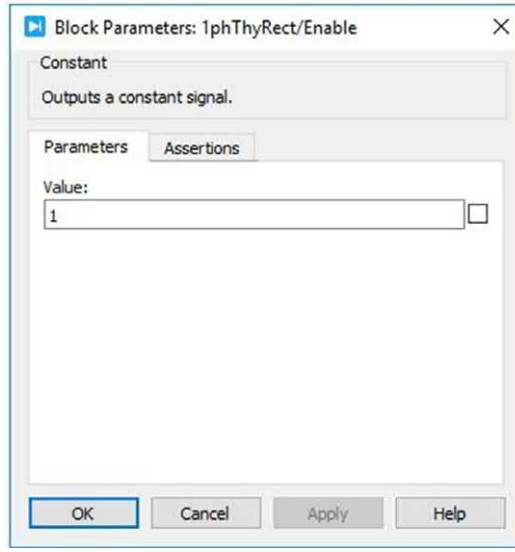


**FIG. 3.128** "Enable" block settings (see Fig. 3.125).

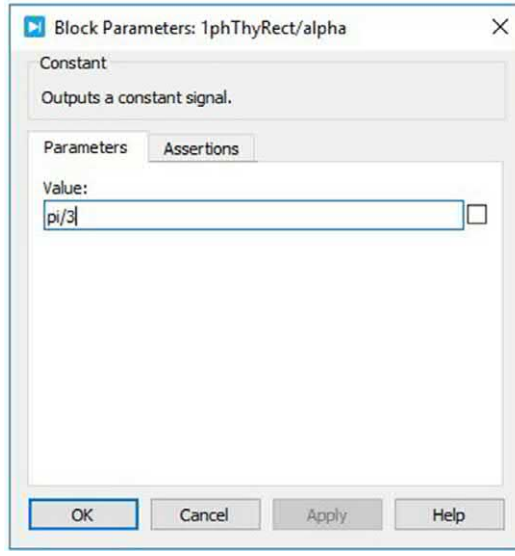


**FIG. 3.129** "Alpha" block settings (see Fig. 3.125).

If we run the simulation, we obtain the results shown in Figs. 3.130 and 3.131.

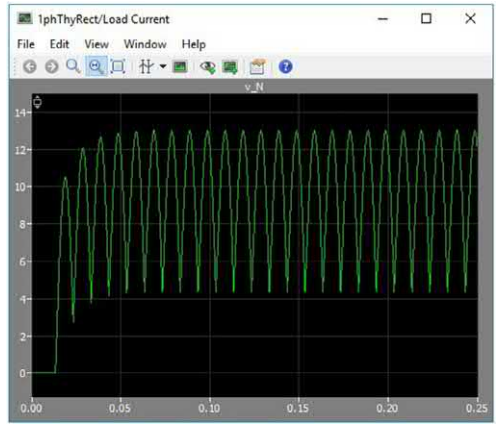


**FIG. 3.130** Load current.

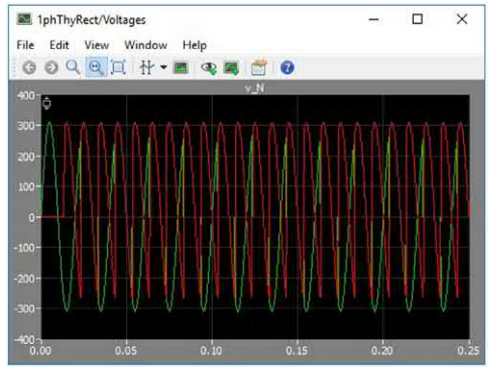


**FIG. 3.131** Input and load voltages.

Zooming in the graph shown in "Voltages" scope to give a better view (Fig. 3.132).

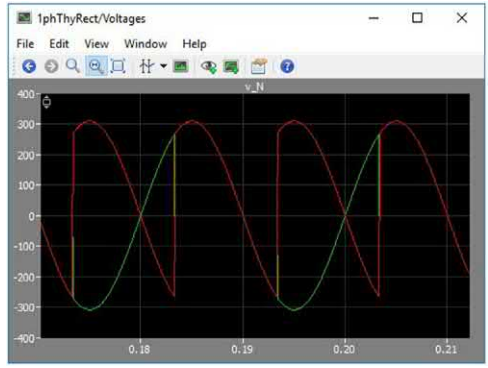


**FIG. 3.132** Zooming in the waveform.

You can measure the drawn waveform RMS, mean value, max/min, etc. using the techniques studied before.

In the schematic shown in Fig. 3.125, we assumed that input source "Phase (rad):" is 0. If the input source "Phase (rad):" is not zero, the simulation diagram must change to that shown in Fig. 3.133.

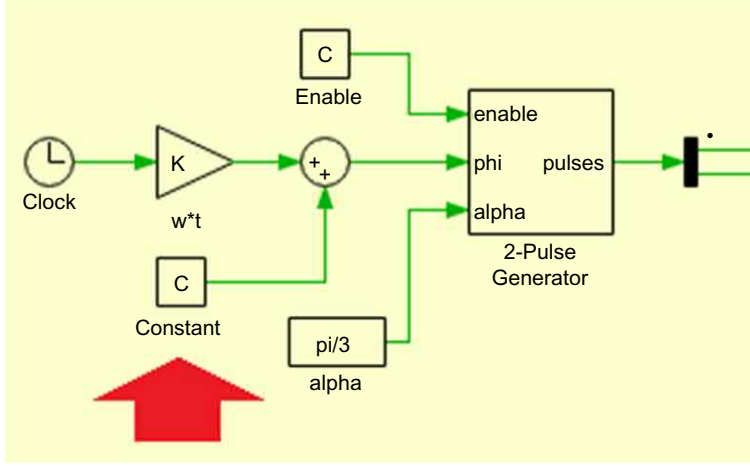


**FIG. 3.133** Change in the simulation for Phase (rad) $\neq 0$ case.

For example if we assume that input source "Phase (rad):" is $\frac{\pi}{4}$, then "Constant" block (Fig. 3.134) (see Fig. 3.133) must be filled as shown in Fig. 3.135.

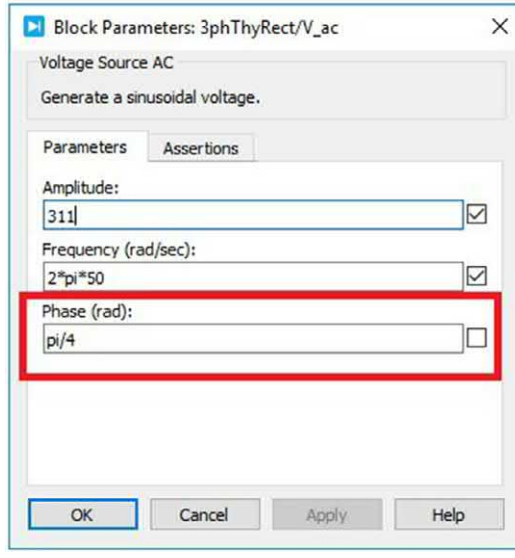


**FIG. 3.134** Phase (rad) assumed to be $\frac{\pi}{4}$ in this example.

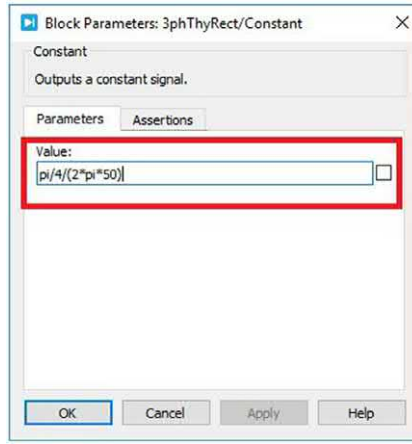


**FIG. 3.135** "Constant" block settings (see Fig. 3.133).

### 3.4.2 Calculating the average output voltage using the "Discrete Fourier transform" block

We studied different methods of calculating the mean value of a waveform before. Yet there is another method: using the "Discrete Fourier Transform" block. "Discrete Fourier Transform" block measures the magnitudes/phase of harmonics specified by the user. If you specify that you want the magnitude of 0th harmonic, it calculates the mean value for you (Fig. 3.136).

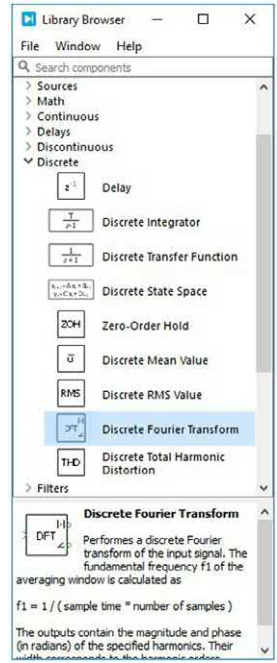


**FIG. 3.136** "Discrete Fourier Transform" block.

For example, assume that we want to calculate the average value (mean value) of output voltage of full-wave single-phase controlled rectifier studied before. We change the schematic to that shown in Fig. 3.137.

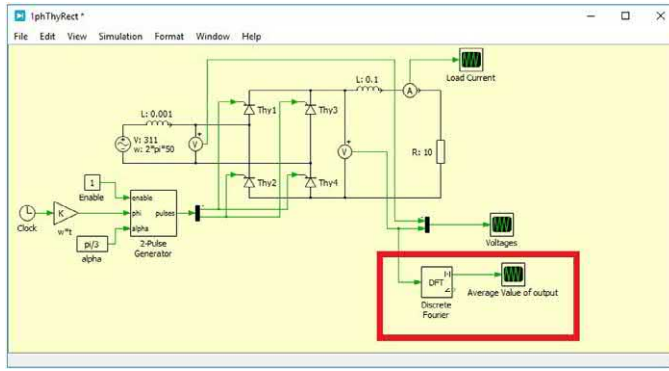


**FIG. 3.137** Adding the "Discrete Fourier Transform" block to the schematic.

Double click the "Discrete Fourier" block to open it and do the settings as shown in Fig. 3.138.

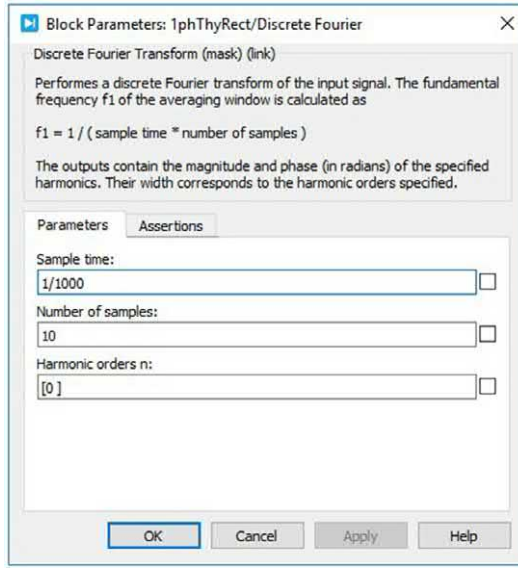


**FIG. 3.138** "Discrete Fourier Transform" block settings.

As shown in Fig. 3.138, the fundamental frequency of "Discrete Fourier Transform" block is calculated with the aid of:

$$f = \frac{1}{\text{Sample time} \times \text{Number of samples}}$$

Since we enter the "Sample time:" box as $\frac{1}{1000}$ and "Number of samples:" as 10, the fundamental frequency is calculated as:

$$f = \frac{1}{\frac{1}{1000} \times 10} = 100\,\text{Hz}$$

"Number of samples" can be selected as 10 for most of simulations, but you can increase it if you need more accuracy. For example if "Number of samples" is increased to 20, "Sample time:" must be set to 0.0005 to keep the fundamental frequency constant at 100 Hz. Remember that full-wave rectifier output voltage has frequency two times greater than input source frequency. You can verify this issue by capturing a period of output voltage between two cursors and measure the time difference (Delta) between the cursors. As shown in Fig. 3.139, the period length is about .01.So, frequency is $\frac{1}{0.01} = 100\,\text{Hz}$.

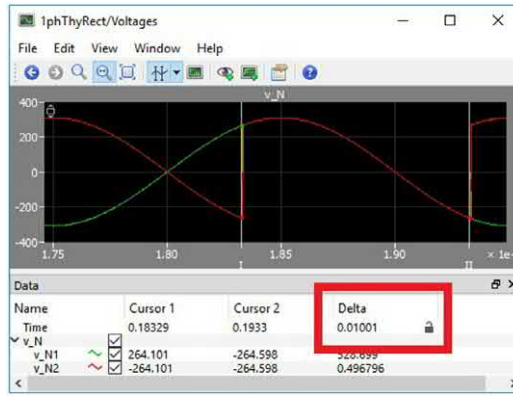


**FIG. 3.139** One period of load voltage takes about 0.01 s. So, its frequency is about 100 Hz.

If we run the simulation, we obtain the waveform shown in Fig. 3.140.

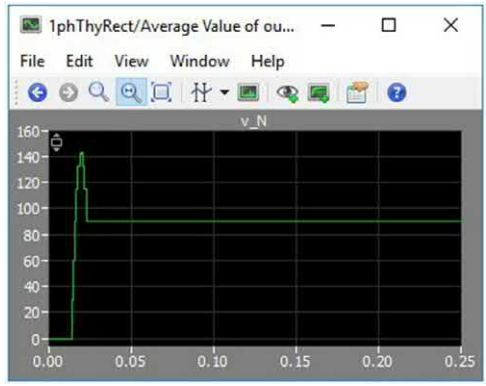


**FIG. 3.140** Average value of load voltage.

Zoom in the waveform to obtain a better view (Fig. 3.141).

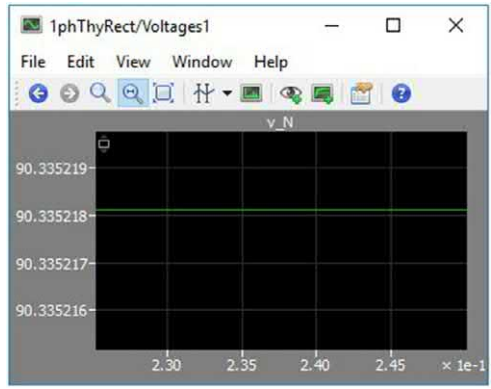


**FIG. 3.141** Average value of load voltage is about 90.3 V.

If you want to measure other harmonics in the load voltage, double click on the "Discrete Fourier" block and enter the wanted harmonic into the "Harmonic orders n:" box. For example if we need harmonics up to 3rd one, we fill the "Harmonic orders n:" box as shown in Fig. 3.142. Simulation result is shown in Fig. 3.143.

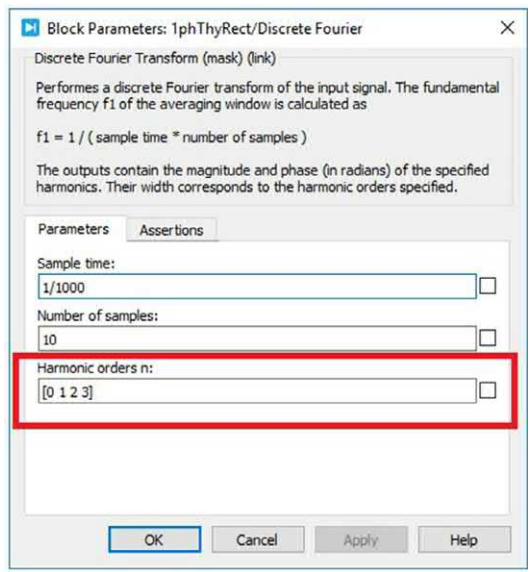


**FIG. 3.142** Discrete Fourier block settings.

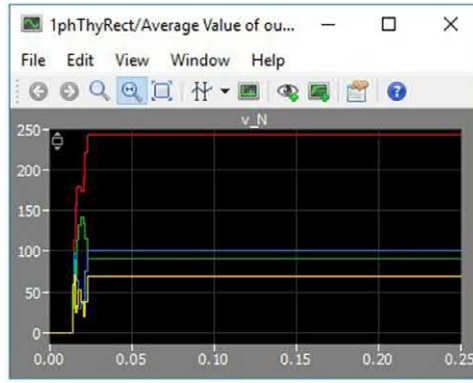


**FIG. 3.143** PLECS shows the harmonics. DC component (green), first harmonic (red), second harmonic (blue), and third harmonic (yellow).

## 3.5 Example 3.5: 3 Phase full-wave controlled rectifier

In this example, we will simulate a 3-phase full-wave rectifier. The output voltages magnitude can be controlled using the thyristor firing angle.

### 3.5.1 Preparing the simulation

Fig. 3.144 shows a 3-phase controlled rectifier. The required gate pulses are provided by the "6-Pulse Generator" block (see Fig. 3.145). Some of the blocks settings used are shown in Figs. 3.146–3.148.

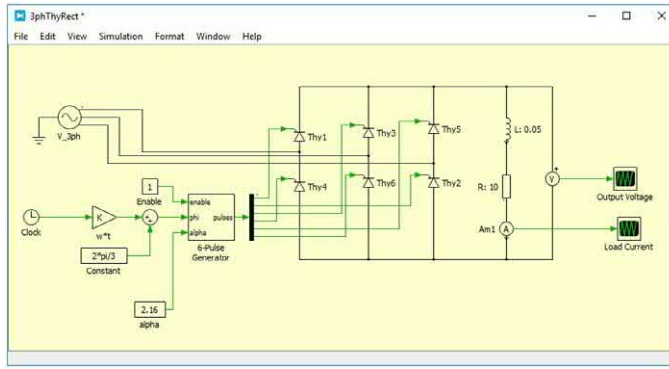


**FIG. 3.144** Controlled 3-phase rectifier.

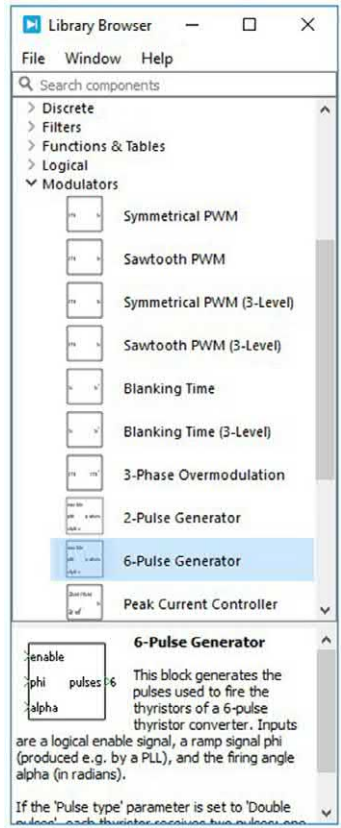


**FIG. 3.145** 6-Pulse Generator block.

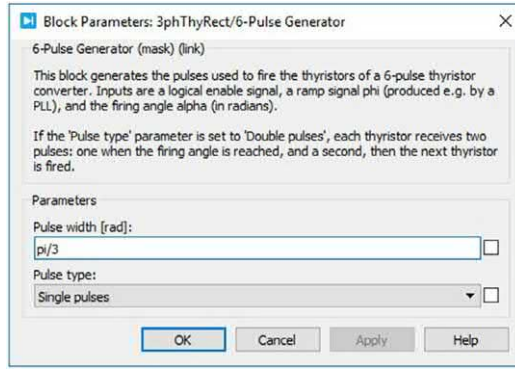


**FIG. 3.146** 6-Pulse generator block settings.

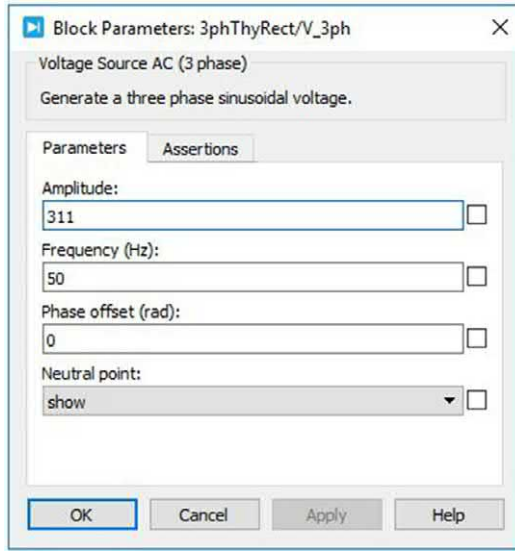


**FIG. 3.147** Input AC source block settings.

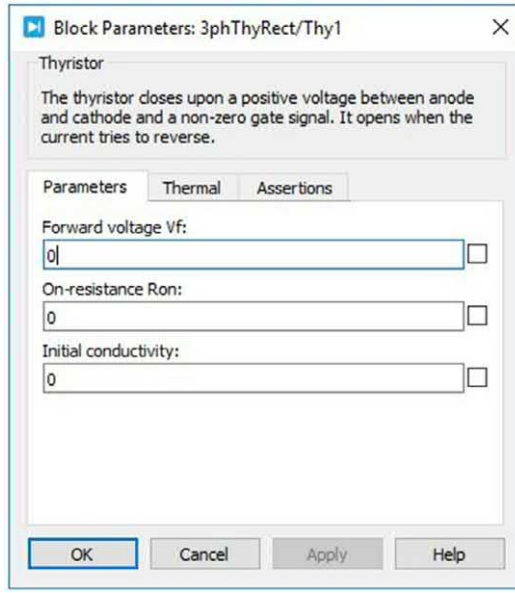


**FIG. 3.148** All the six thyristors are set as shown in the figure.

If we run the simulation, we obtain the results shown in Figs. 3.149 and 3.150.

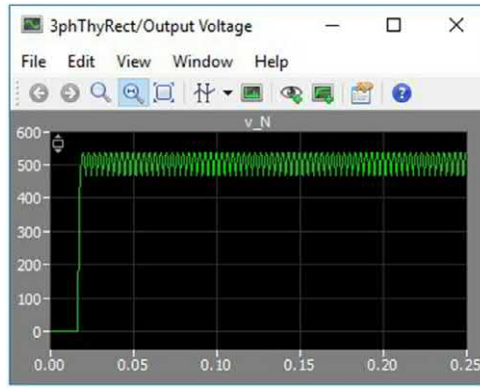


**FIG. 3.149** Load voltage.

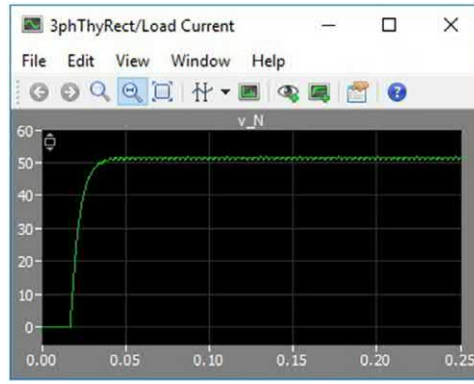


**FIG. 3.150** Load current.

### 3.5.2 Drawing more understandable schematics using "Electrical label," "Signal from," and "Signal goto" blocks

Schematic shown in Fig. 3.144 seems crowded. We can draw it more understandable using the "Electrical Label," "Signal From," and "Signal Goto" blocks (Figs. 3.151 and 3.152).

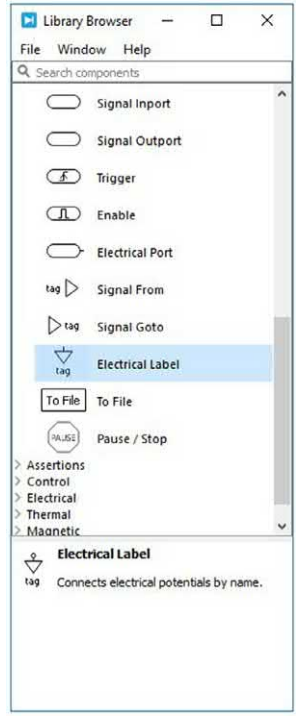


**FIG. 3.151** Electrical Label block.

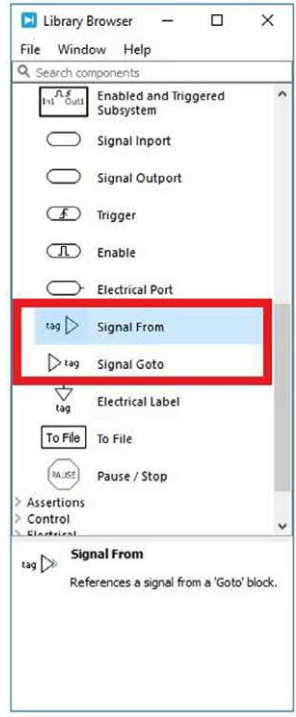


**FIG. 3.152** "Signal From" and "Signal Goto" block.

Place 6 "Electrical Label" blocks in the schematic. Double click on them and change their "Tag name" to A, B, and C. So, you have two "Electrical Label" block with "Tag name" A, two "Electrical Label" block with "Tag name" B, and two "Electrical Label" block with "Tag name" C. Remove the wires between the source and thyristor legs and change the schematic as shown in Fig. 3.153. All the "Electrical Label" blocks with the same "Tag name"s are considered to be connected together. So, Fig. 3.153 is equal to Fig. 3.144 from PLECS viewpoint. But Fig. 3.153 is more understandable from user viewpoint.

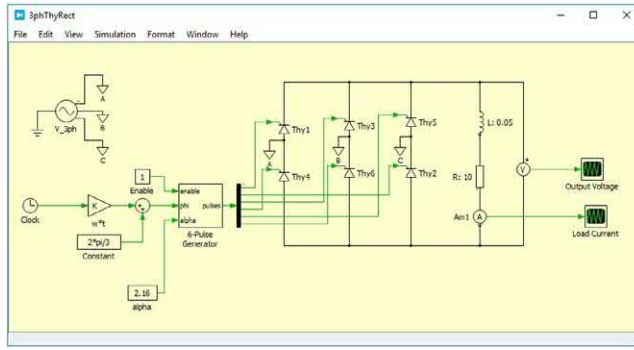


**FIG. 3.153** Schematic is drawn using the "Electrical Label" blocks.

You can even simplify the schematic shown in Fig. 3.153 more as shown in Fig. 3.154.

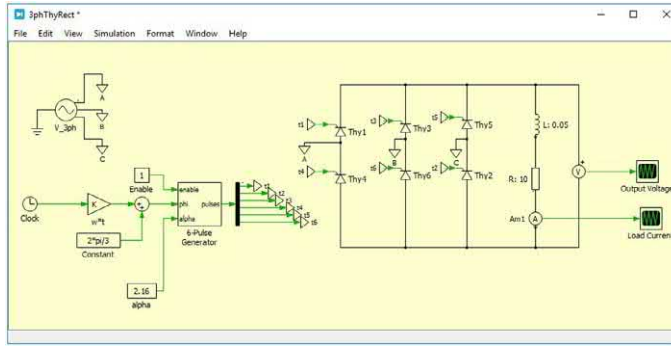


**FIG. 3.154** Schematic looks better when you use the label instead of connecting the parts directly together.

As shown in Fig. 3.153, the wire connecting the multiplexer block to the thyristor gates is green, so they are control signals and you cannot use "Electrical Label" since it is designed to work with power circuit components.

To connect the output of multiplexer to the thyristor gates, you must use "Signal From" and "Signal Goto" blocks.

Add a "Signal Goto" block to the schematic and connect it to first output of multiplexer block (Fig. 3.155).

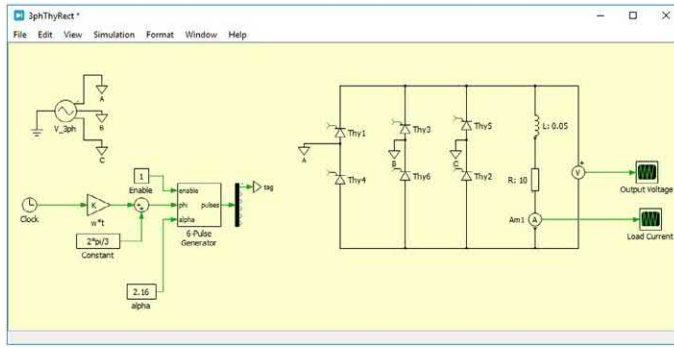


**FIG. 3.155** Connect the "Signal Goto" to the first output of the multiplexer.

Double click on the "Signal Goto" block and set the "Tag name" to "t1" and click the OK button (Fig. 3.156).

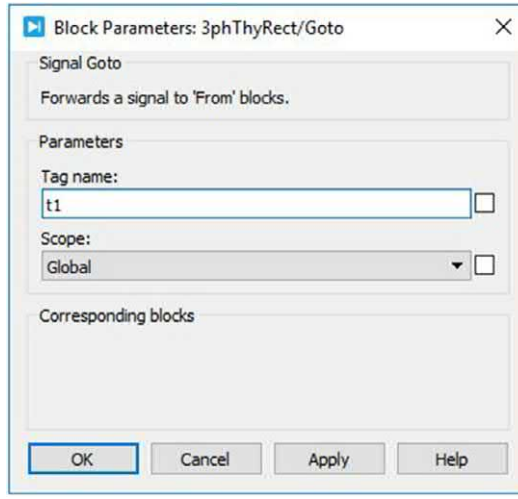


**FIG. 3.156** Renaming the placed "Signal Goto" block to "t1".

After setting the "Tag name" to "t1," the schematic looks like that shown in Fig. 3.157.

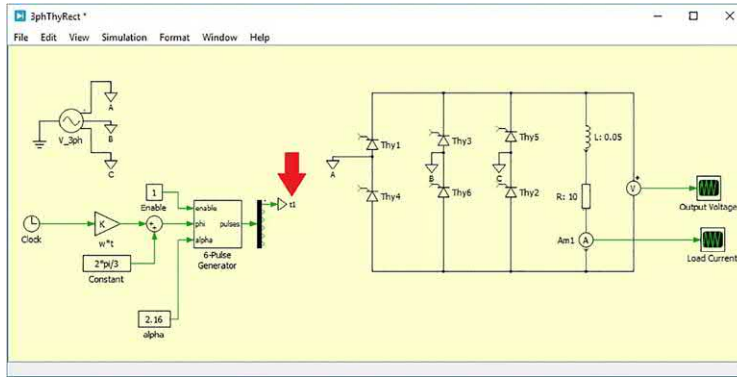


**FIG. 3.157** After renaming the block, new name (t1) will appear on the schematic.

Place a "Signal From" block on the schematic and connect it to the gate of the thyristor named "Thy1" (Fig. 3.158).

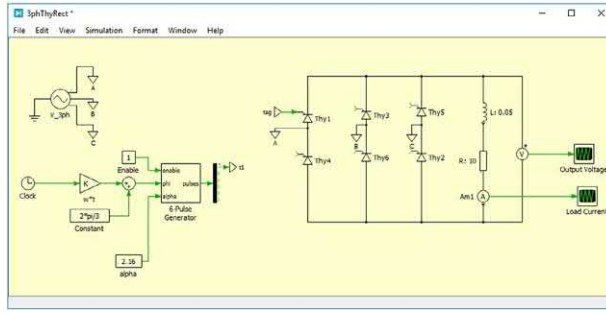


**FIG. 3.158** Connect the "Signal From" to the gate of thyristor "Thy1."]

Double click the "Signal From" block and set the "Tag name:" to "t1" and click the OK button (Fig. 3.159).

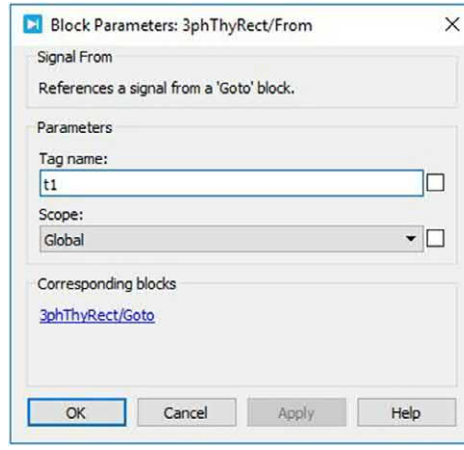


**FIG. 3.159** Renaming the placed "Signal From" block to "t1".

After setting the "Tag name" to "t1," the schematic looks like that shown in Fig. 3.160.

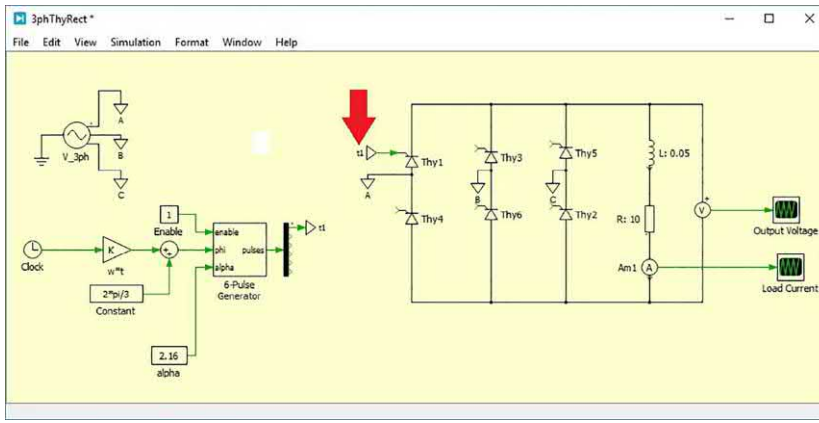


**FIG. 3.160** After renaming the block, new name (t1) will appear on the schematic.

Do the same procedure to place 5 more "Signal Goto" and "Signal From" blocks on the schematic. Name them t2, t3, t4, t5, and t6. Do the required connection in order to change your schematic into the one shown in Fig. 3.154. All the "Signal Goto" and "Signal From" blocks with the same "Tag name" are considered to be connected.

### 3.5.3 Delay block

Assume a rectifier shown in Fig. 3.161.

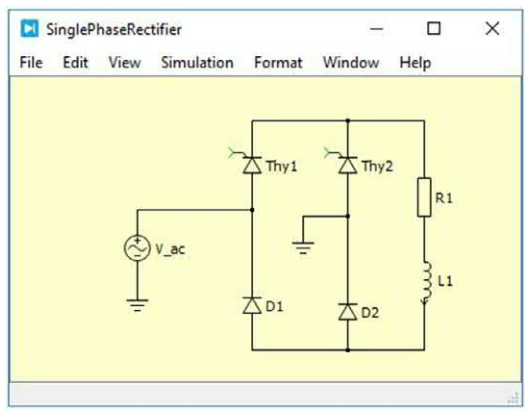


**FIG. 3.161** Another topology of controlled single-phase rectifiers.

In this type of rectifier, control signal for "Thy2" is a delayed version of gate pulse applied to gate of "Thy1." So, there is no need to generate a separate gate signal for "Thy2." You can use the delayed version of the pulse send to the gate of "Thy1." PLECS has a block named "Transport Delay," which can be used for such situations (Fig. 3.162).

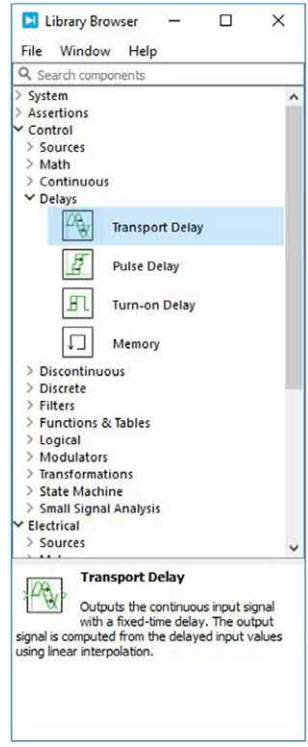


**FIG. 3.162** Transport Delay block.

You can set the amount of required delay by the "Time delay:" box (Fig. 3.163).

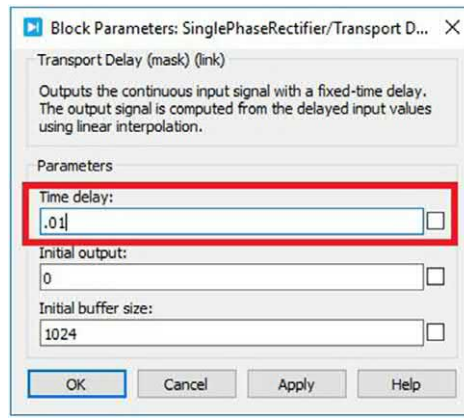


**FIG. 3.163** Setting the required time delay.

## 3.6 Example 3.6: Boost converter

In this example, we will simulate a PWM step up converter.

### 3.6.1 Preparing the simulation

Fig. 3.164 shows the schematic of a Boost converter.

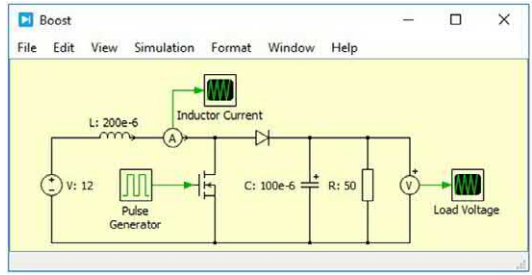


**FIG. 3.164** Boost converter.

As shown in Fig. 3.164, the gate pulse is provided by a "Pulse Generator" block. "Pulse Generator" block provides a pulse with duty ratio of 0.6 and frequency of 25 KHz (Fig. 3.165).

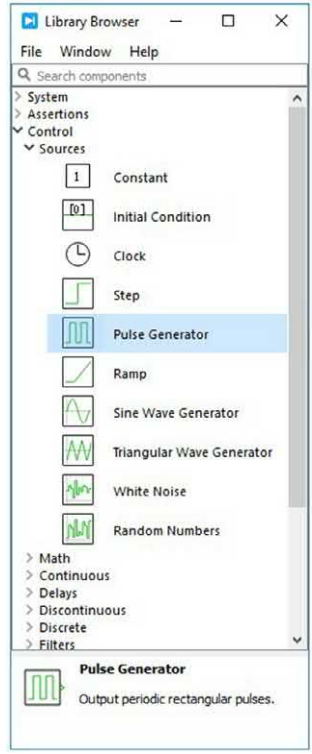


**FIG. 3.165** Pulse Generator block.

Figs. 3.166–3.168 shows the blocks settings used. The MOSFET on resistance is assumed to be 40 mΩ. Diode voltage drop and series resistance are assumed to be 1 V and 0.01 Ω, respectively.

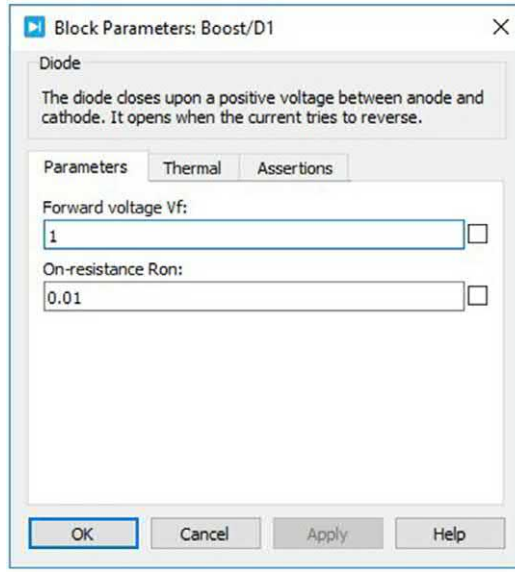


**FIG. 3.166** Diode settings.

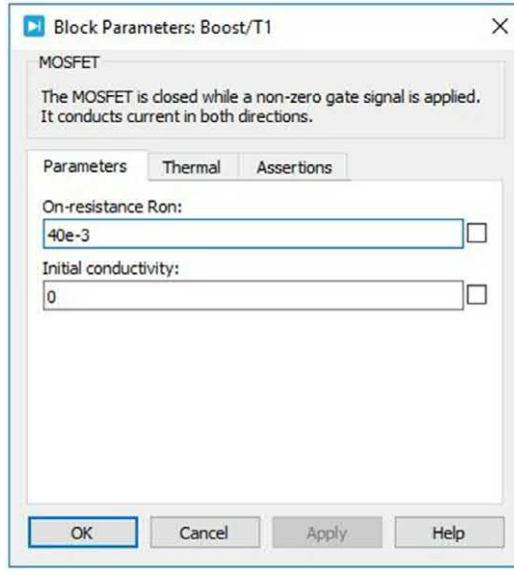


**FIG. 3.167** MOSFET settings.

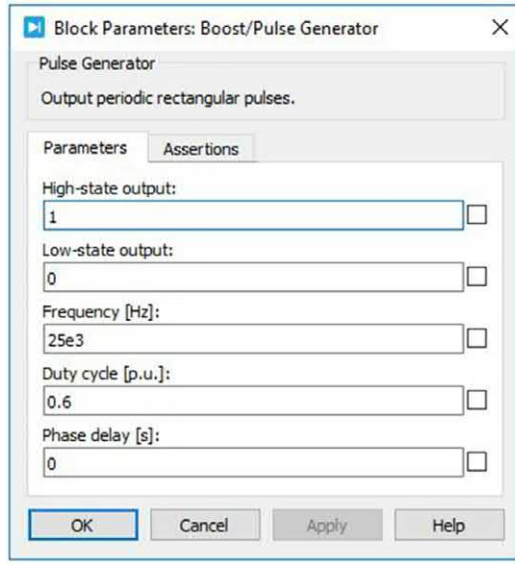


**FIG. 3.168** Pulse Generator settings.

If we run the simulation with the settings shown in Fig. 3.169, we obtain the results shown in Figs. 3.170–3.173.

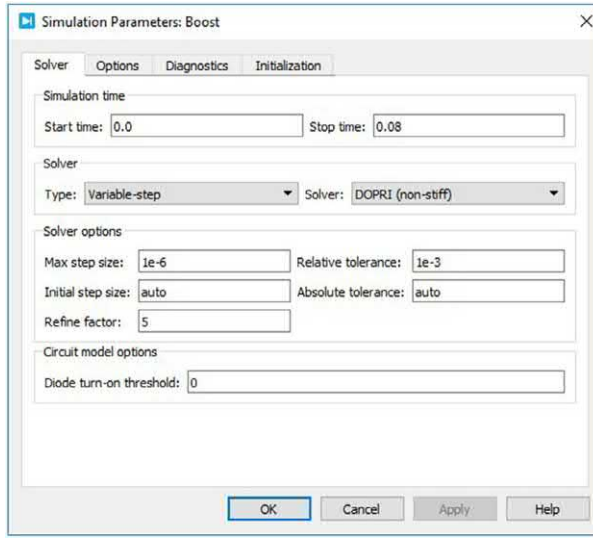


**FIG. 3.169** Simulation parameter.

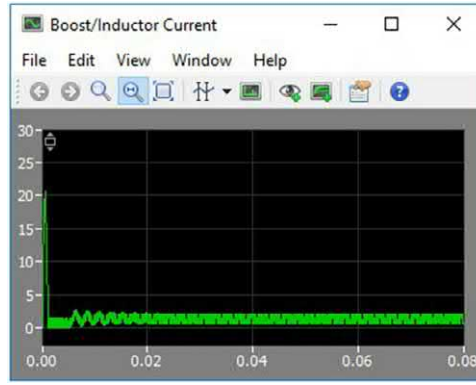


**FIG. 3.170** Inductor current waveform.

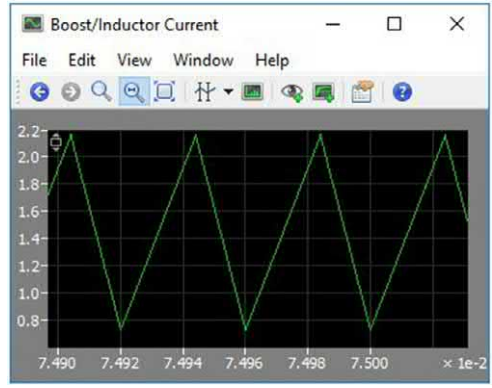


**FIG. 3.171** Zooming in the inductor current waveform.

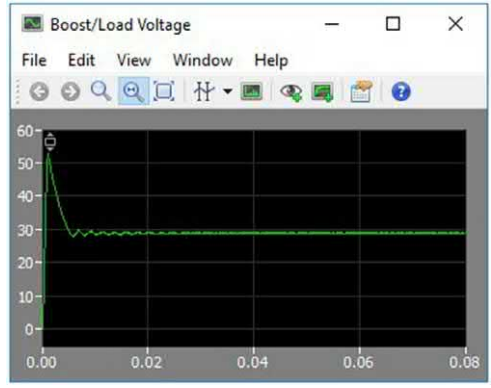


**FIG. 3.172** Load voltage waveform.

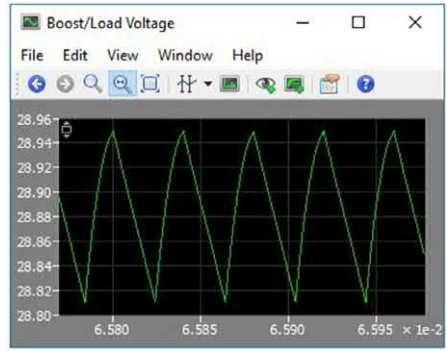


**FIG. 3.173** Zooming in the load voltage.

You can measure the output voltage ripple by placing a cursor on top of the curve and the other one on the bottom of the curve (Fig. 3.174).

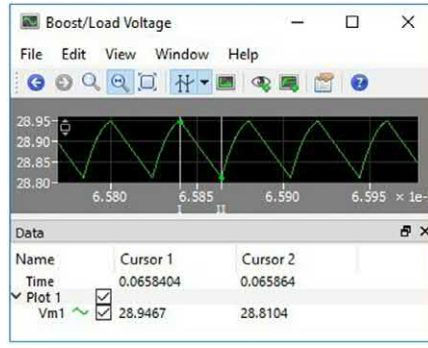


**FIG. 3.174** Putting the cursors on the maximum and minimum points to obtain the output voltage ripple.

Click the small triangle behind the cursor icon and select "Delta" (Fig. 3.175)

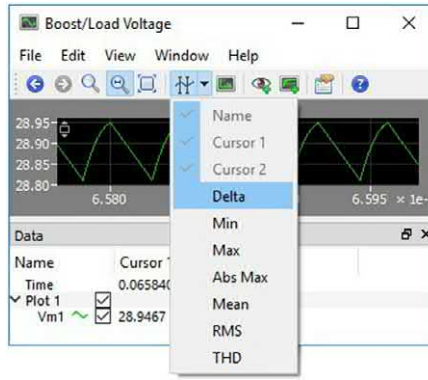


**FIG. 3.175** Measuring the difference between the cursors.

PLECS calculates the time difference and amplitude difference between the two cursors and shows it. So, the output voltage ripple is about 0.136 V = 136 mV (Fig. 3.176).

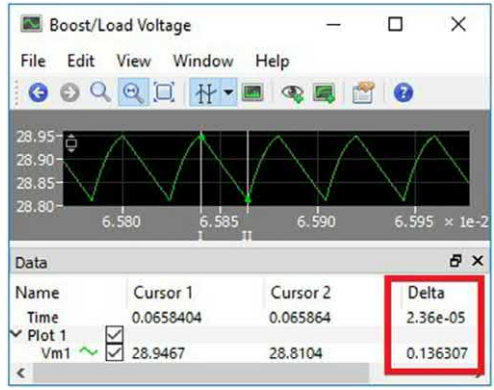


**FIG. 3.176** The time and voltage difference between the two cursors is $2.36 \times 10^{-5}$ s and 0.136 V, respectively.

### 3.6.2 Simulating the circuit using the ready-to-use modulator

Schematic shown in Fig. 3.164 uses the "Pulse Generator" block to turn the MOSFET on and off. Schematic shown in Fig. 3.177 uses the "Sawtooth PWM" block (see Fig. 3.178) to control the MOSFET. "Sawtooth PWM" block settings are shown in Fig. 3.179.

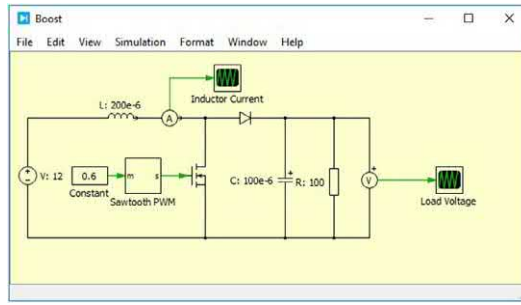


**FIG. 3.177** Using the Sawtooth PWM block to turn on and off the MOSFET.

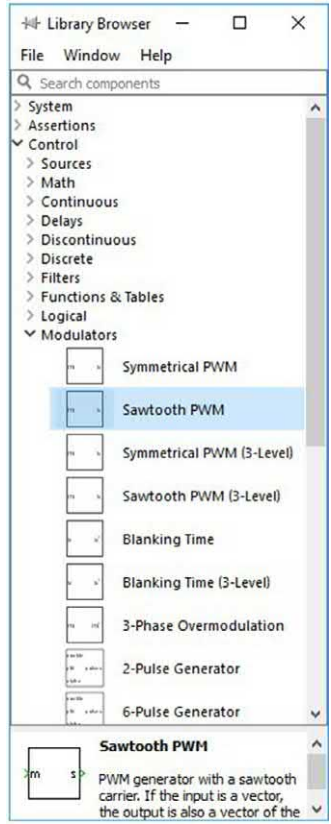


**FIG. 3.178** Sawtooth PWM block.

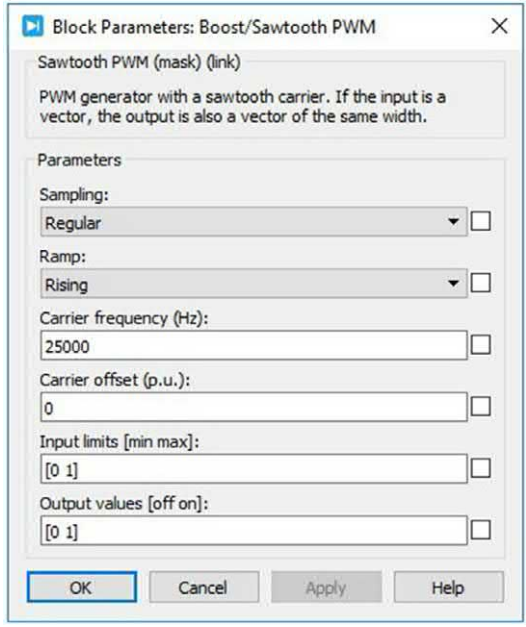


**FIG. 3.179** Sawtooth PWM block settings.

### 3.6.3 Efficiency measurement

You can use the schematic shown in Fig. 3.180 to calculate the converter efficiency. This schematic uses a 10-Ω load. The schematic uses saturation, divide/product, and moving average blocks. These block places are shown in Figs. 3.181–3.183. Some of the blocks settings used are shown in Figs. 3.184–3.186. Here we compute the input and output power and divide them to obtain the efficiency.

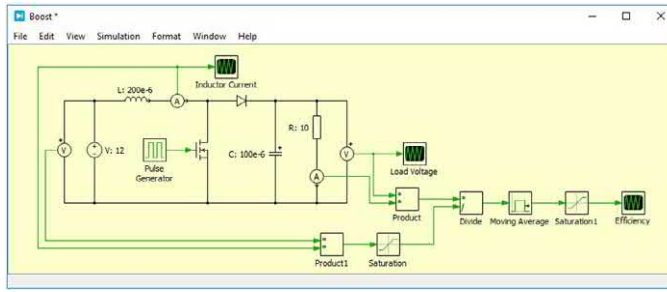


**FIG. 3.180** Measuring the efficiency.

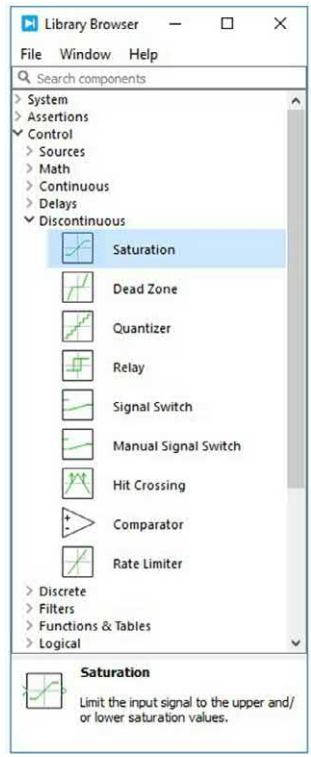


**FIG. 3.181** Saturation block.

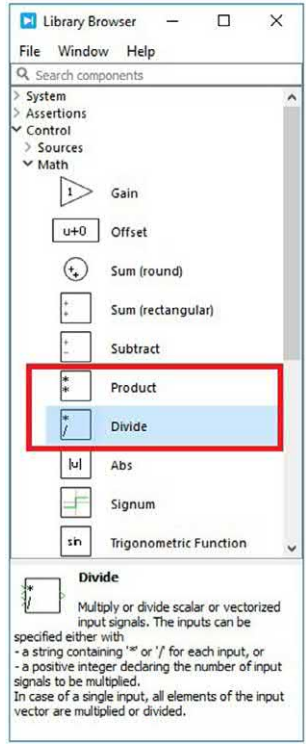


**FIG. 3.182** "Product" and "Divide" blocks.

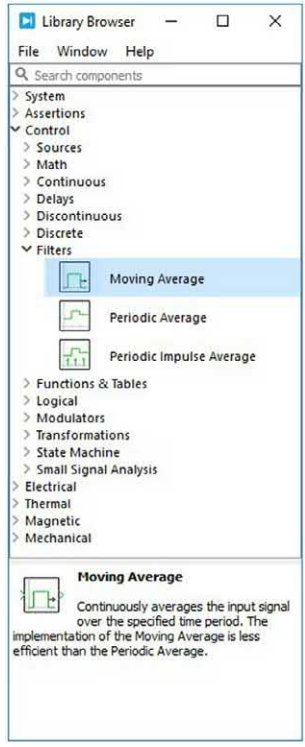


**FIG. 3.183** "Moving Average" block.

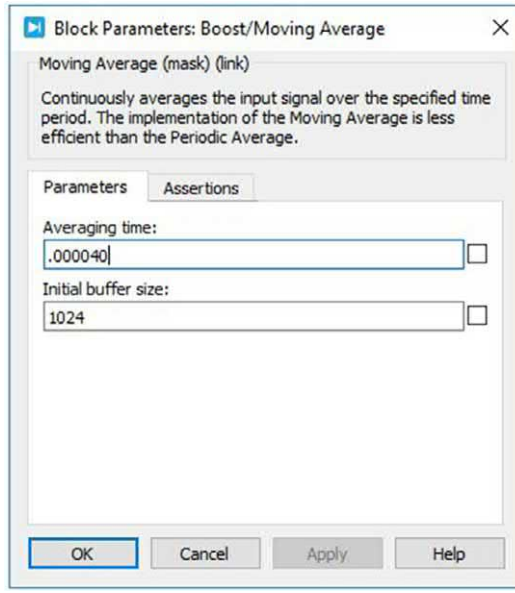


**FIG. 3.184** "Moving Average" block settings (see Fig. 3.180). "Averaging time" must be set equal to the block input waveform period. Since the input has frequency of 25 KHz, "Averaging time" set to 40 μs.

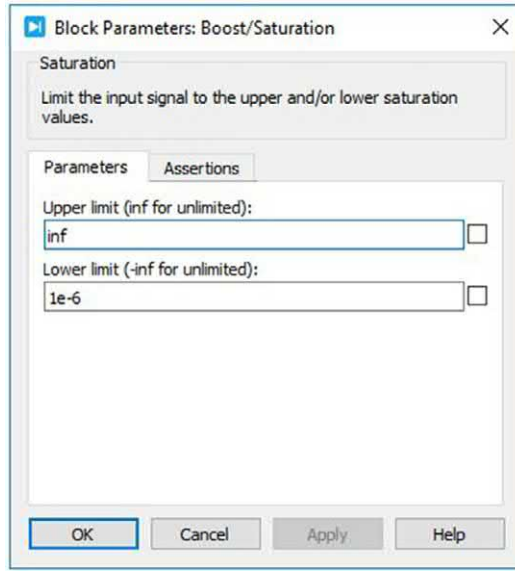


**FIG. 3.185** "Saturation" block settings (see Fig. 3.180).

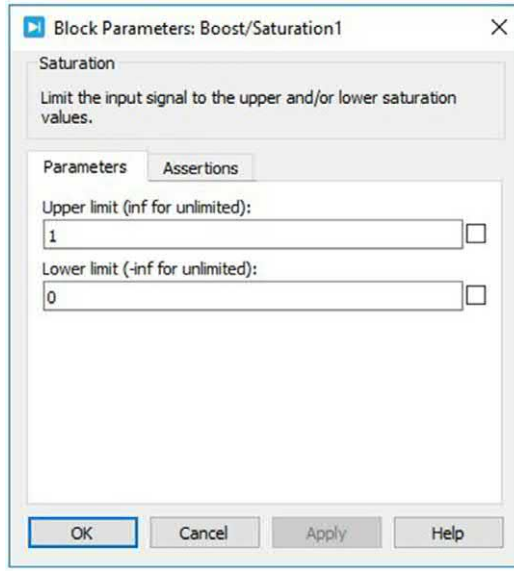


**FIG. 3.186** "Saturation1" block settings (see Fig. 3.180).

If you run the simulation with settings shown in Fig. 3.187, you will obtain the results shown in Fig. 3.188.

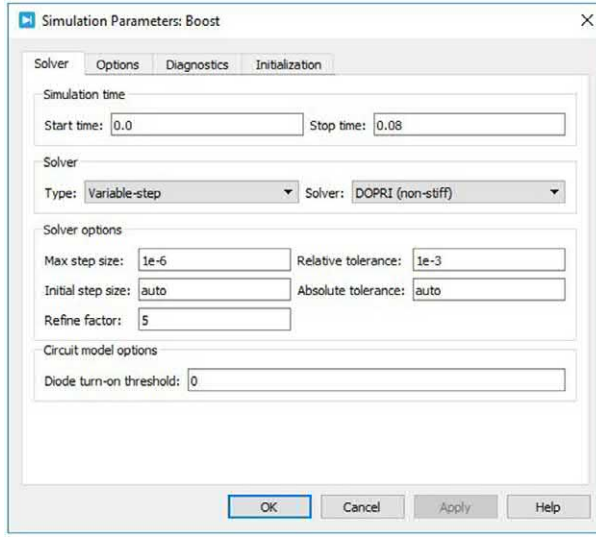


**FIG. 3.187** Simulation parameters.

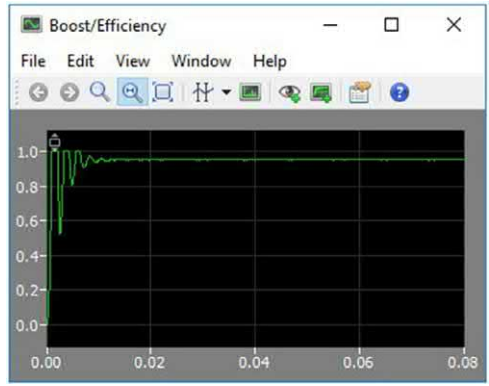


**FIG. 3.188** Calculated efficiency.

You can zoom in to obtain a better view. As shown in Fig. 3.189, the efficiency is about 95%.

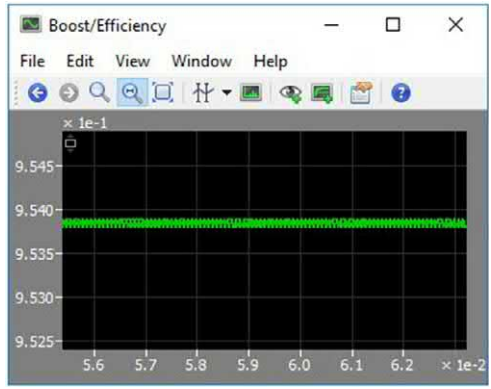


**FIG. 3.189** Zooming the graph. When using the scope to monitor the efficiency, zoom into the steady state of graph. Transients part of graph is not important.

If you try to run the simulation without block named "Saturation"(see Fig. 3.190), you will face an error as shown in Fig. 3.191. The reason is: in $t=0$ the input and output power are zero, so PLECS faces $\frac{0}{0}$. In the schematic shown in Fig. 3.180, we set the lower bound for input power to be $1e-6=10^{-6}$ (see Fig. 3.185) instead of 0, so at $t=0$ PLECS faces $\frac{0}{10^{-6}}$, which causes no problem since it is equal to 0.

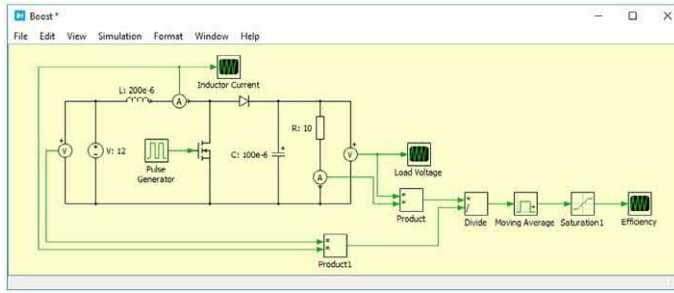


**FIG. 3.190** Schematic diagram without "Saturation" block. Compare with Fig. 3.180.

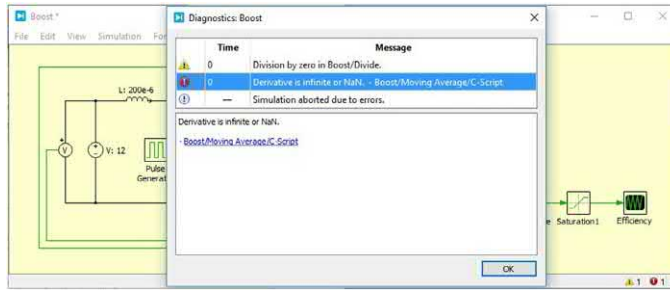


**FIG. 3.191** Generated error message.

## 3.7 Example 3.7: Obtaining the small signal transfer functions for a buck converter

In this example, we will show how you can obtain the small signal transfer functions for a DC-DC step down converter. The obtained Bode plots are used to design the controller. See Chapter 7 of [1] to see an example.

### 3.7.1 Preparing the simulation

Assume a Buck converter schematic shown in Fig. 3.192. Some of the used blocks settings are shown in Figs. 3.193–3.195.

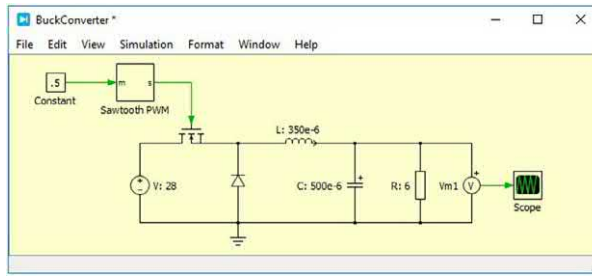


**FIG. 3.192** Buck converter.

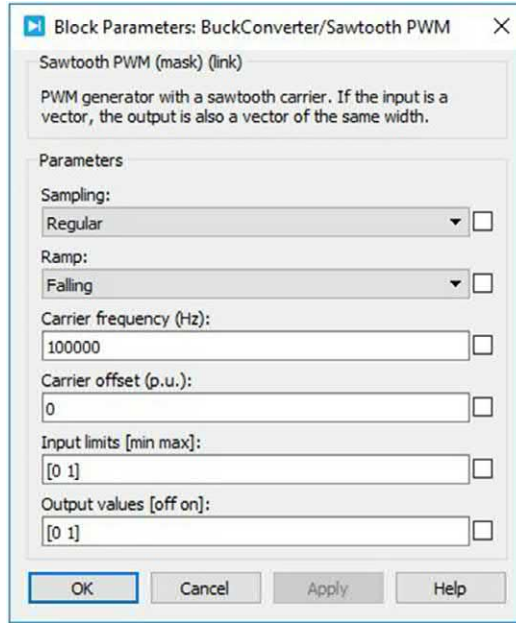


**FIG. 3.193** Sawtooth PWM block settings.

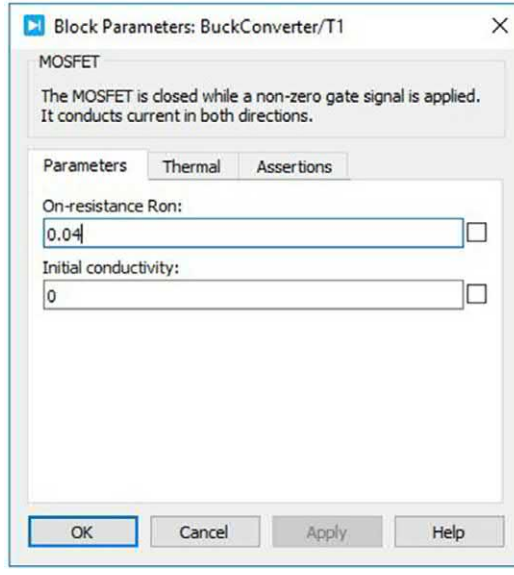


**FIG. 3.194** MOSFET settings.

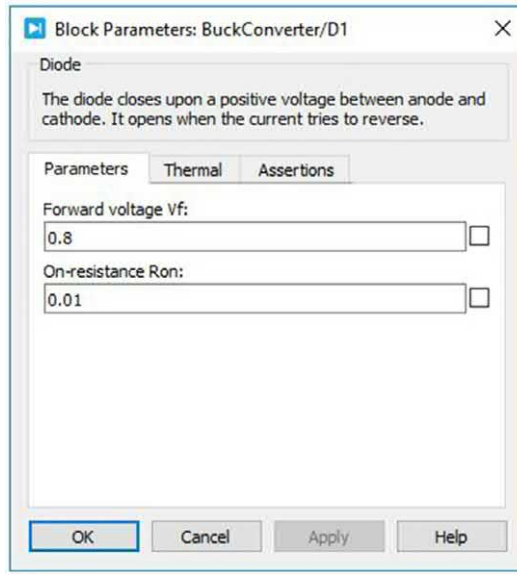


**FIG. 3.195** Diode settings.

If we run the simulation with settings shown in Fig. 3.196, we obtain the waveform shown in Fig. 3.197. Output voltage is about 14 V.

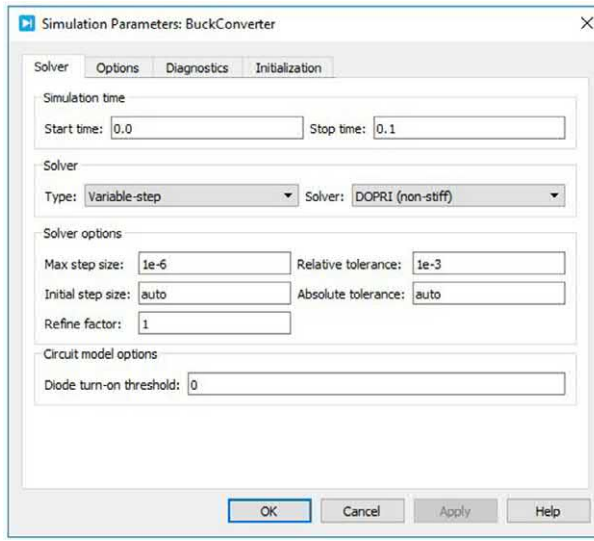


**FIG. 3.196** Simulation Parameters.

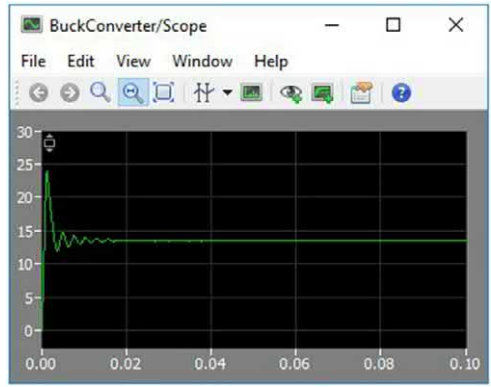


**FIG. 3.197** Output voltage waveform.

Assume that we want to obtain the small signal transfer function from control input (duty ratio) to output voltage. To do this, we change the schematic as shown in Fig. 3.198. This schematic uses "Perturbation" and "Response" blocks. These blocks can be found in the "Small Signal Analysis" section of Library Browser (see Fig. 3.199). "Perturbation" and "Response" blocks settings are shown in Figs. 3.200 and 3.201.

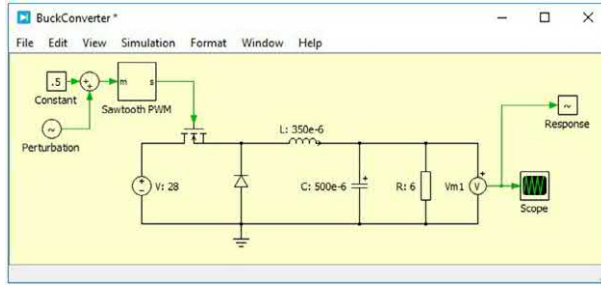


**FIG. 3.198** Adding the "Perturbation" and "Response" blocks to the schematic.

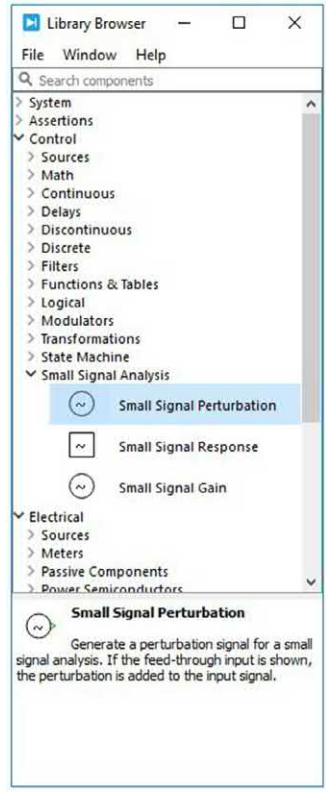


**FIG. 3.199** Small Signal Analysis section of Library Browser.

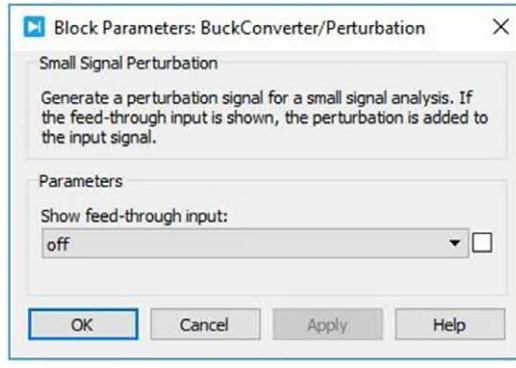


**FIG. 3.200** "Perturbation" block settings.

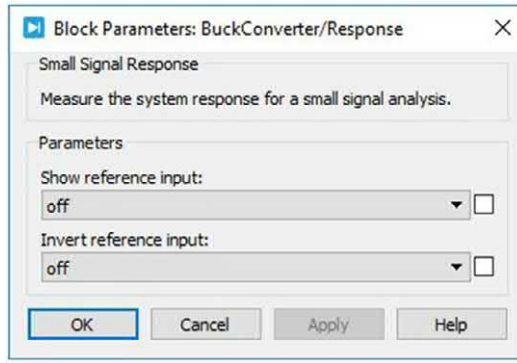


**FIG. 3.201** "Response" block settings.

To obtain the small signal transfer function between the duty ratio and output voltage, click on "Analysis tools…" (Fig. 3.202).

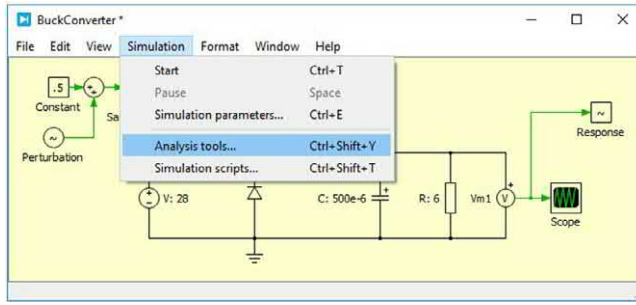


**FIG. 3.202** Use "Analysis tools…" to open the Analysis Tools window.

In the opened window, click on the + sign (Fig. 3.203).

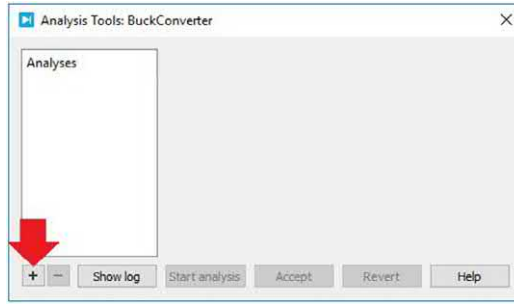


**FIG. 3.203** Analysis Tools window.

A window such as Fig. 3.204 will appear.

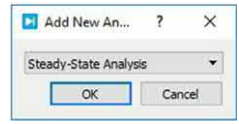


**FIG. 3.204** Add New Analysis window.

Select the "Impulse Response Analysis" (Fig. 3.205)

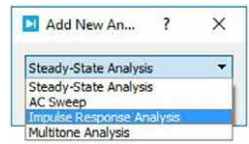


**FIG. 3.205** Select "Impulse Response Analysis" to do small signal analysis.

A window such as that shown in Fig. 3.206 will appear.

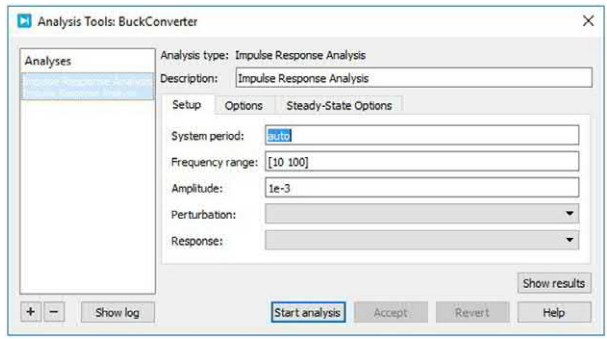


**FIG. 3.206** Analysis Tools window.

Fill the window like Fig. 3.207. Here we want to calculate the transfer function for 10 Hz-50 KHz range. "Amplitude:" box must contain a small value. The converter steady-state duty ratio is 0.5 (see Fig. 3.198). As a rule of thumb, perturbation amplitude must be less than 0.1 of the average value (in this case, $\frac{0.5}{10} = 0.05$).

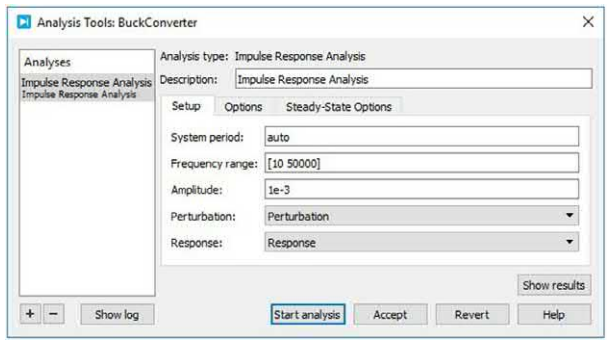


**FIG. 3.207** Analysis Tools window after doing the settings.

Click the "Start analysis" button to obtain the small signal Bode plot (Fig. 3.208).

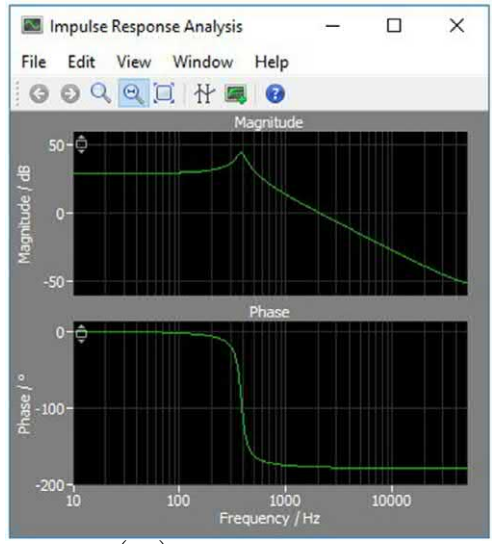


**FIG. 3.208** Simulation results $\left(\frac{\tilde{v}_o(s)}{\tilde{d}(s)}\right)$.

You can read the obtained plot with the aid of cursors like other graphs (Fig. 3.209).

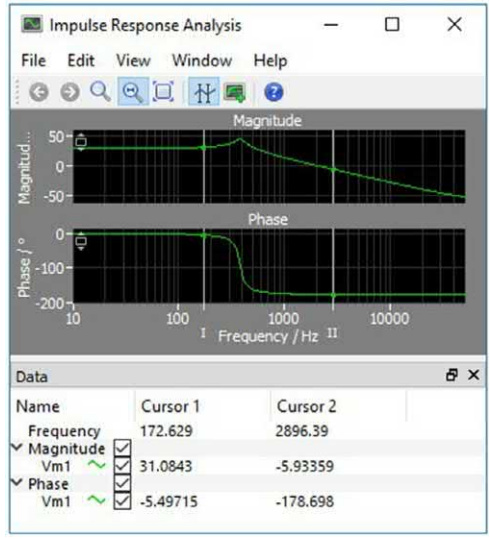


**FIG. 3.209** Adding cursors to the simulation results.

### 3.7.2 Comparison of different simulation results

Assume that you want to see what happens to the Bode plot if load increases to 12 Ω. Click the "Save trace data…" to save the result of analysis for 6 Ω load. Save the graphics at the desired path (Fig. 3.210).

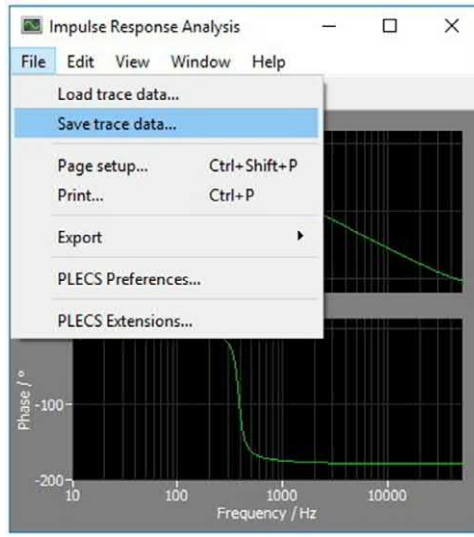


**FIG. 3.210** Use the "Save trace data..." to save the current graph.

After saving the result of analysis for 6-Ω load, return to the schematic and change the load to 12 Ω (Figs. 3.211 and 3.212).

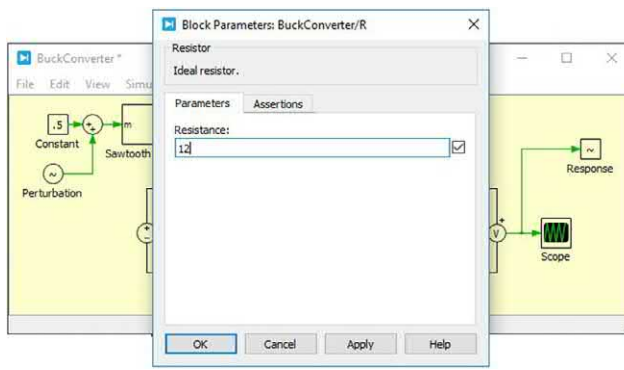


**FIG. 3.211** Increasing the load resistance to 12 Ω.

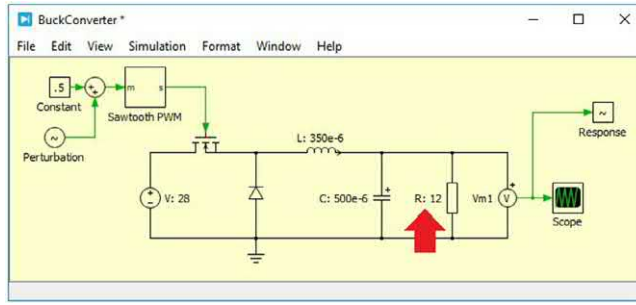


**FIG. 3.212** Schematic after increasing the load resistance.

Go to the "Analysis tools…" (Fig. 3.213).

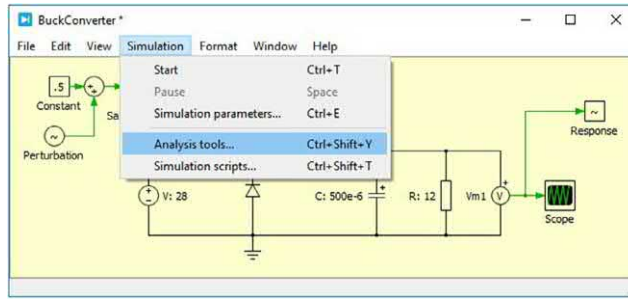


**FIG. 3.213** Use "Analysis tools…" to open the Analysis Tools window.

Click the "Start analysis" button to obtain the result for 12-Ω load (Fig. 3.214).

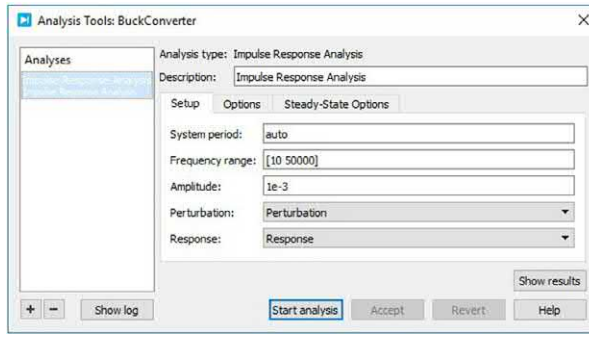


**FIG. 3.214** Analysis Tools window.

Fig. 3.215 shows the analysis result.

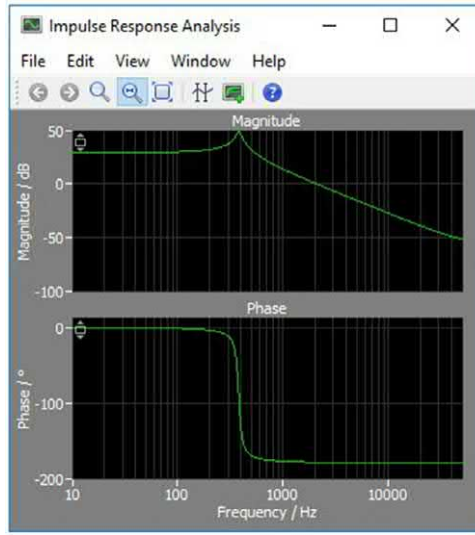


**FIG. 3.215** Simulation results $\left(\frac{\tilde{v}_o(s)}{\tilde{d}(s)}\right)$ for R = 12 Ω.

Click the "Load trace data…" and read the file of 6-Ω analysis (Fig. 3.216).

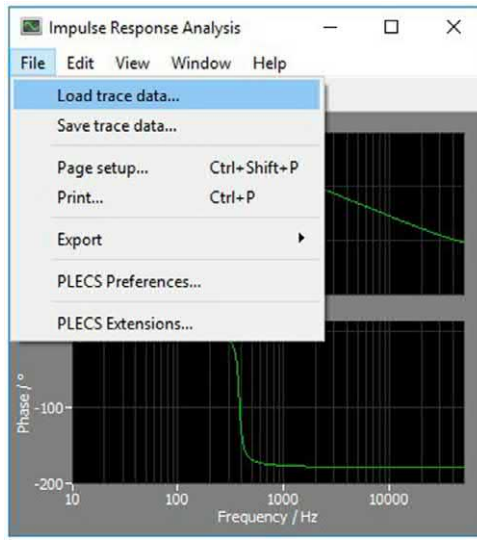


**FIG. 3.216** Use "Load trace data…" to load the saved analysis result (for R = 6 Ω).

PLECS shows both of the results on the same graph. This makes comparison possible (Fig. 3.217).

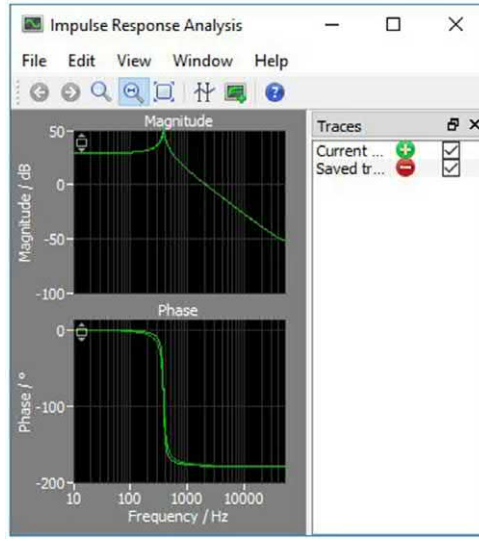


**FIG. 3.217** Traces section is added to the window.

Use magnifier to get a better view. You can close the "Traces" window by clicking on the × icon (Fig. 3.218).

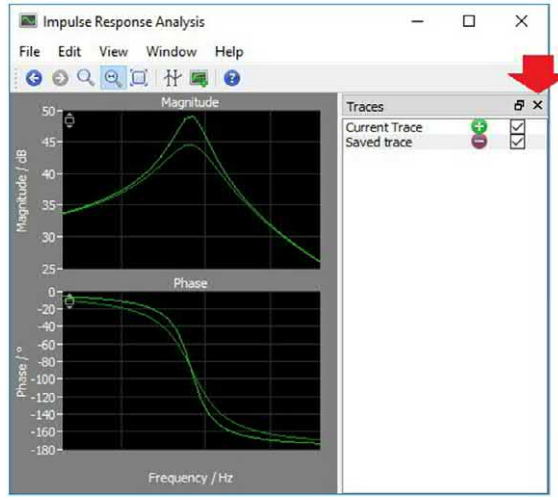


**FIG. 3.218** Zooming in the results.

You can change the graphs color by right clicking on the graph and select the "Edit curve properties" (Fig. 3.219)

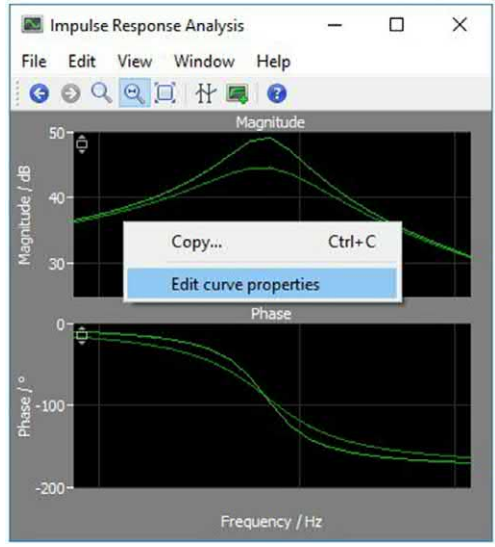


**FIG. 3.219** Right click on the graph and select the "Edit curve properties" to change the curves colors, style, and line width.

Click on "Color" section to select the desired colors (Fig. 3.220).

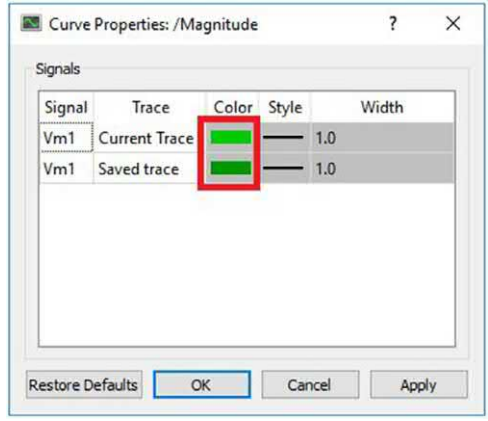


**FIG. 3.220** Curve Properties window.

Select your favorite color from the opened window (Fig. 3.221).

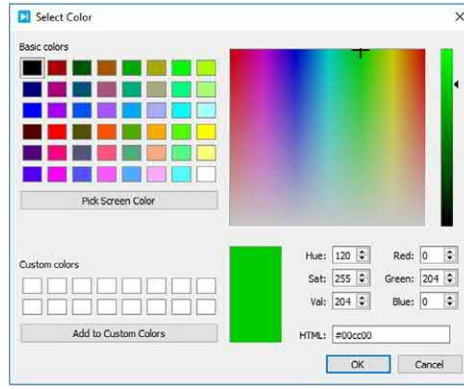


**FIG. 3.221** Select Color window.

You can obtain other small signal transfer functions in the same way you obtain the control to output voltage transfer function. For instance, if you want to obtain the control to inductor current transfer function, change the schematic into the one shown in Fig. 3.222.

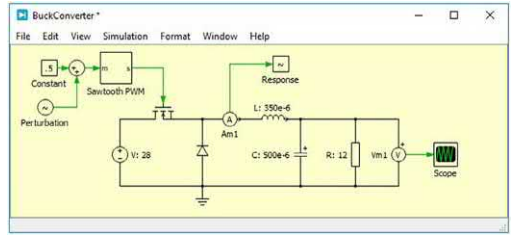


**FIG. 3.222** Schematic to obtain the control to inductor current transfer function $\left(\frac{\tilde{i}_L(s)}{\tilde{d}(s)}\right)$.

Analysis result for Fig. 3.222 is shown in Fig. 3.223.

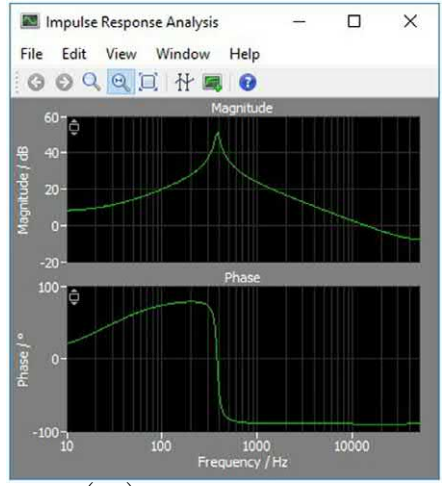


**FIG. 3.223** Simulation result $\left(\frac{\tilde{i}_L(s)}{\tilde{d}(s)}\right)$.

### 3.7.3 Importing the simulation results into the MATLAB

You can transfer the obtained Bode plot into the MATLAB for further process. To do this, you must export the obtained result as a CSV file. To do this click on "All…" (Fig. 3.224).

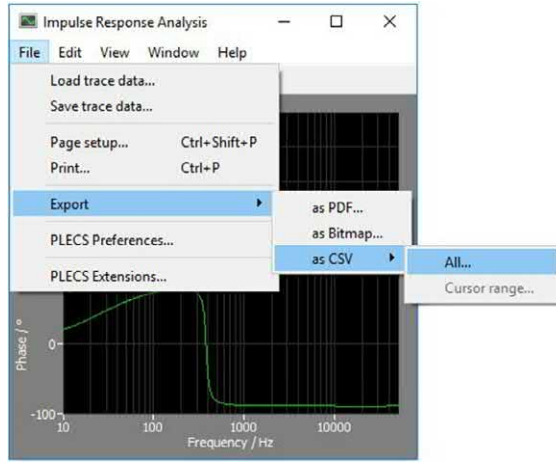


**FIG. 3.224** Exporting the graph as .csv file.

Save the CSV file to desired path. Here we saved it in the "C:\" path and named it data.csv. After saving, open the file in the Notepad and remove the first line. After removing the first line, save the file (Figs. 3.225 and 3.226).

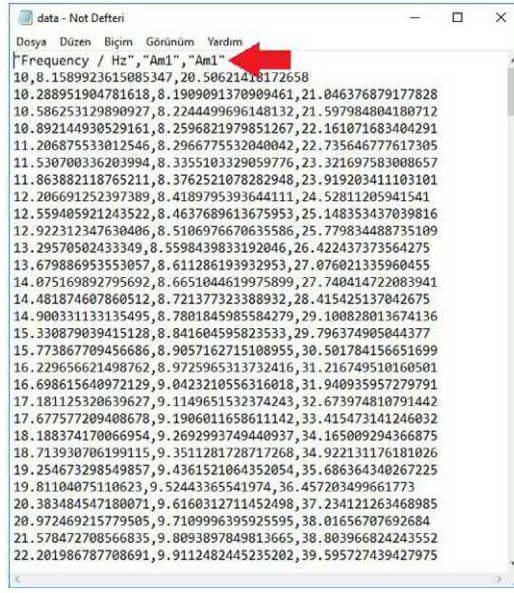


**FIG. 3.225** Opening the data.csv file in Notepad and removing the first line.

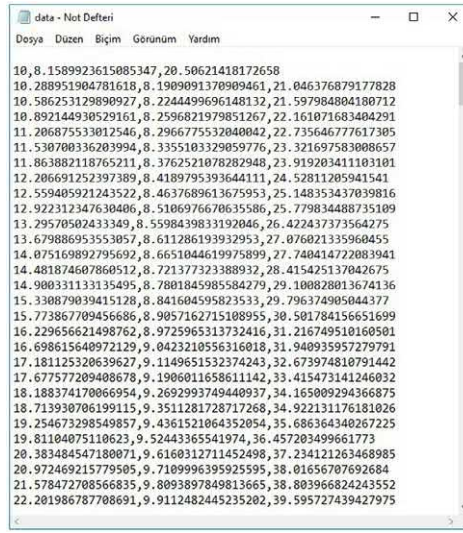


**FIG. 3.226** Removing the first line.

Run the MATLAB. Write the codes shown in Fig. 3.227. This imports the data into the MATLAB (Fig. 3.228).

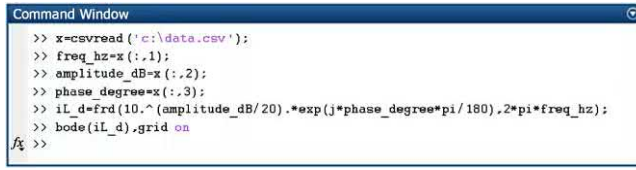


**FIG. 3.227** Reading the data.csv in MATLAB.

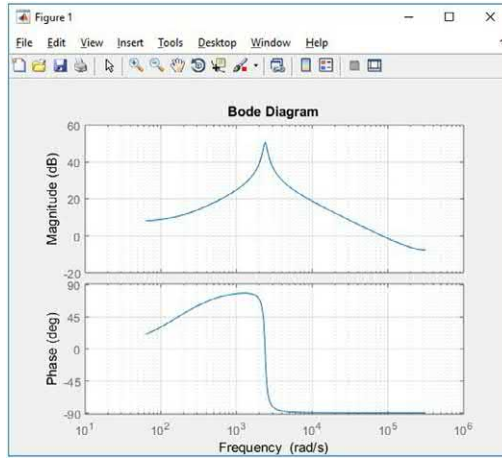


**FIG. 3.228** PLECS graph is regenerated in MATLAB (see Fig. 3.223).

## 3.8 Example 3.8: Mutual inductance

In this example, we will show how you can simulate circuits containing mutual inductors.

### 3.8.1 Preparing the simulation

Assume you want to analyze the circuit shown in Fig. 3.229.

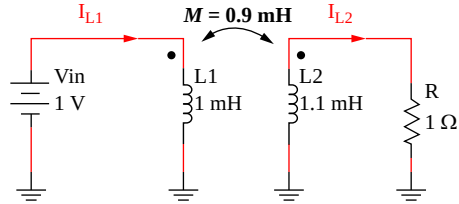


**FIG. 3.229** A simple circuit containing the mutual inductors.

According to basic circuit theory (initial condition assumed to be zero),

$$\begin{cases} L1\dfrac{di_{L1}}{dt} - M\dfrac{di_{L2}}{dt} = V_{in}(\mathrm{t}) \\ Ri_{L2} + L_2\dfrac{di_{L2}}{dt} - M\dfrac{di_{L1}}{dt} = 0 \end{cases}$$

$$\begin{cases} L1\dfrac{di_{L1}}{dt} - M\dfrac{di_{L2}}{dt} = V_{in}(\mathrm{t}) \\ Ri_{L2} + L_2\dfrac{di_{L2}}{dt} - M\dfrac{di_{L1}}{dt} = 0 \end{cases}$$

If we take the Laplace transform of both sides,

$$\begin{bmatrix} L_1 s & -Ms \\ -Ms & R + L_2 s \end{bmatrix} \times \begin{bmatrix} I_{L1}(s) \\ I_{L2}(s) \end{bmatrix} = \begin{bmatrix} V_{in}(s) \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} I_{L1}(s) \\ I_{L2}(s) \end{bmatrix} = \begin{bmatrix} L_1 s & -Ms \\ -Ms & R + L_2 s \end{bmatrix}^{-1} \times \begin{bmatrix} V_{in}(s) \\ 0 \end{bmatrix}$$

is obtained. Since Vin($t$)=1 V, its Laplace transform is Vin($s$) $= \frac{1}{s}$. So, Laplace transform of currents is obtained as:

$$\begin{bmatrix} I_{L1}(s) \\ I_{L2}(s) \end{bmatrix} = \begin{bmatrix} \dfrac{(11s + 10000) \times 10000}{s^2 \times (29s + 100000)} \\ \dfrac{90000}{s(29s + 100000)} \end{bmatrix}$$

We can draw the time domain graph of these equations using commands shown in Fig. 3.230. Results are shown in Figs. 3.231 and 3.232.

```
Command Window
>> I1=tf([11e4 1e8],[29 1e5 0 0]);
>> I2=tf(9e4,[29 1e5 0]);
>> figure(1);impulse(I1), grid minor
>> figure(2);impulse(I2), grid minor
fx >>
```

**FIG. 3.230** MATLAB codes to obtain the time domain graph of $I_{L1}(s)$ and $I_{L2}(s)$.

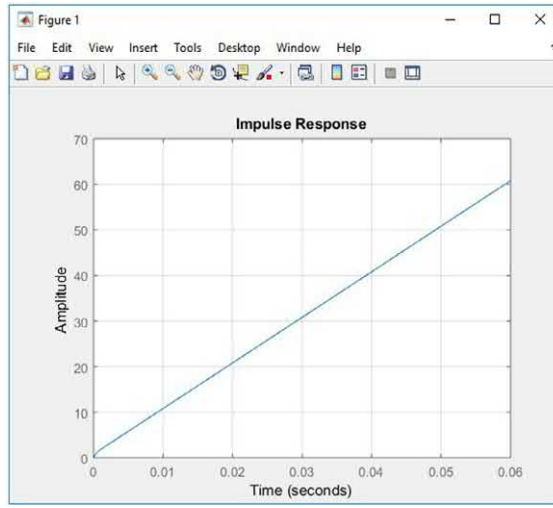


**FIG. 3.231** Time domain graph of $I_{L1}(s)$.

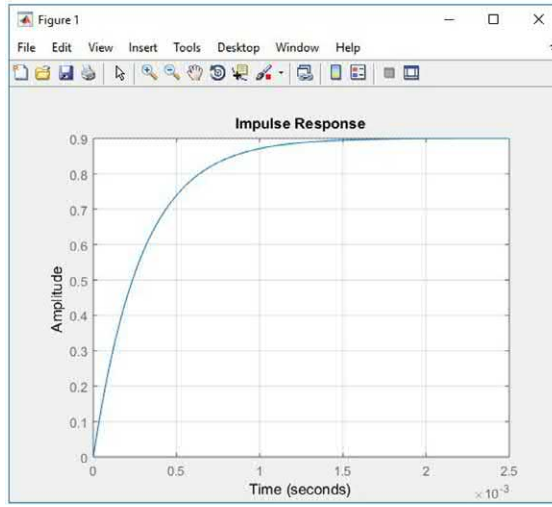


**FIG. 3.232** Time domain graph of $I_{L2}(s)$.

In order to analyze the circuit using PLECS, we draw the schematic shown in Fig. 3.233 This schematic uses the mutual inductor block, which can be found under "Passive Components" section of Library Browser (see Fig. 3.234). As shown in Fig. 3.235, the first winding is shown with a small circle. Other windings are shown with dot.

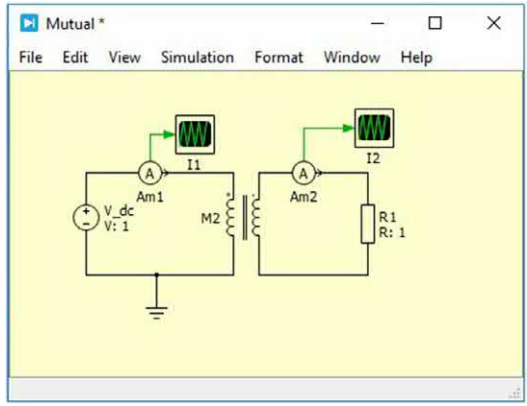


**FIG. 3.233** Schematic to simulate the circuit shown in Fig. 3.229.

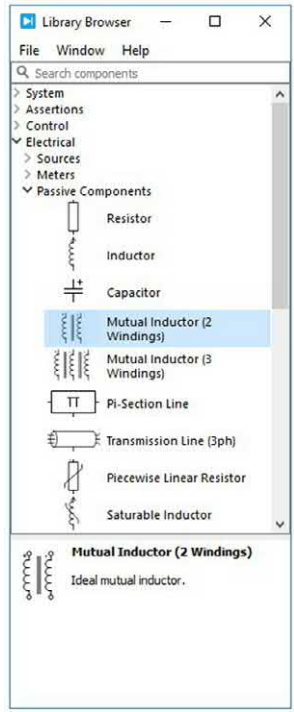


**FIG. 3.234** Mutual Inductor block.

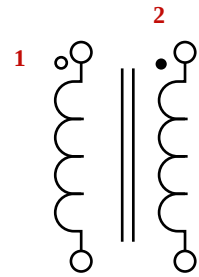


**FIG. 3.235** First winding is shown with a small circuit. Other windings are shown with a small dot.

Double click on the mutual inductor block and do the setting as shown in Fig. 3.236. With these settings the mutual inductor simulate the mutual inductor block shown in Fig. 3.229. The "Inductance:" box takes a matrix. The main diagonal shows the self-inductance of windings. Other elements of the matrix show the mutual inductance between windings (Fig. 3.236). If you right click on the mutual inductance block and select the Help you can see more information about the block (Fig. 3.237).

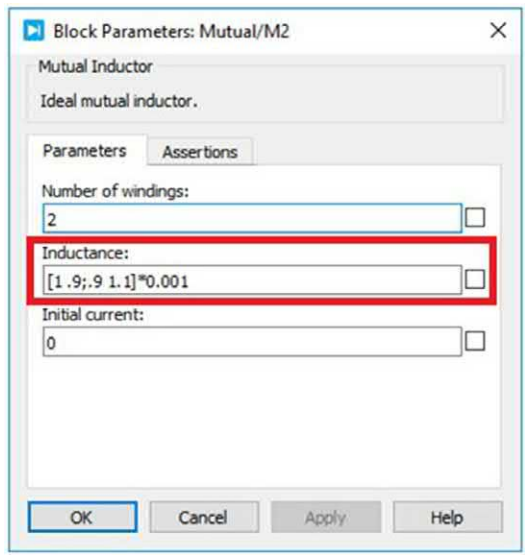


**FIG. 3.236** Setting the parameters of the mutual inductor.

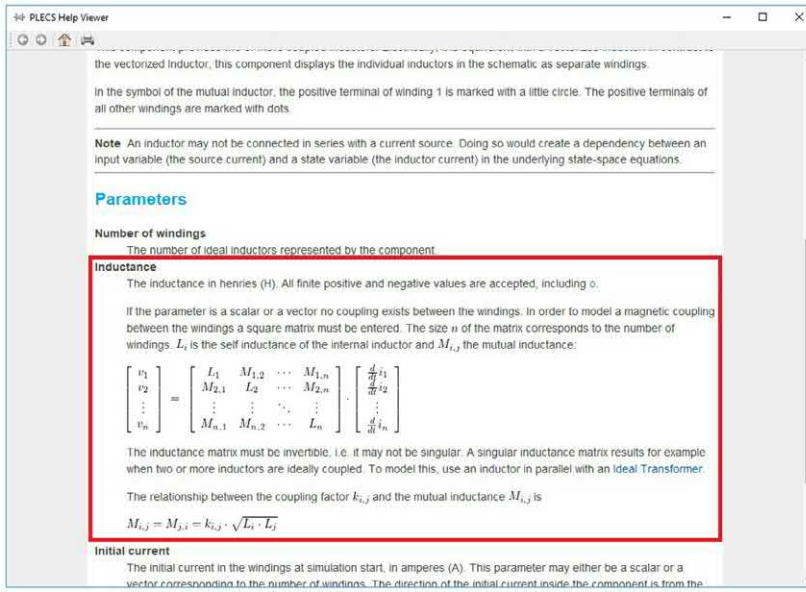


**FIG. 3.237** Documentation for mutual inductor block.

If we run the simulation with the setting shown in Fig. 3.238, the results shown in Figs. 3.239 and 3.240 will be obtained. Compare them with Fig. 3.231 and 3.232. The results are the same.

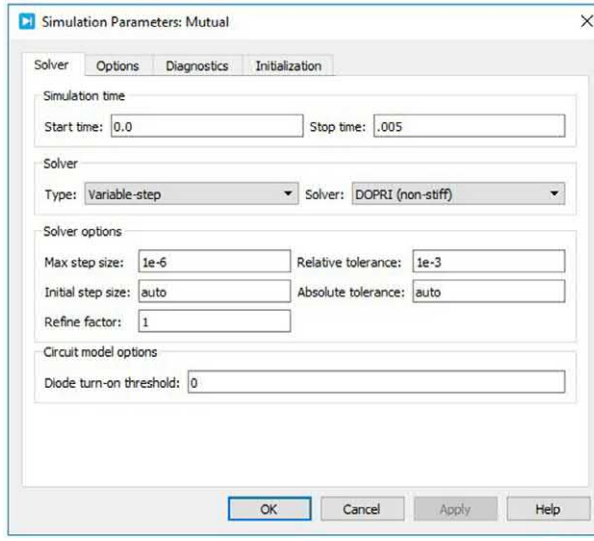


**FIG. 3.238** Simulation parameters.

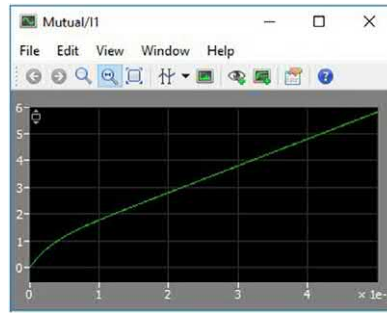


**FIG. 3.239** Primary winding current.

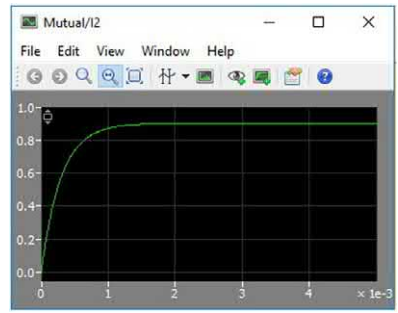


**FIG. 3.240** Secondary winding current.

If your schematic needs transformers, you can find it in the Transformer section of Library Browser (Fig. 3.241).

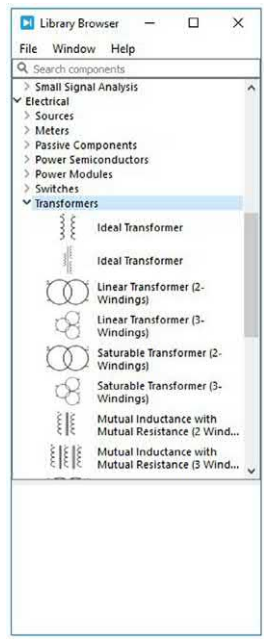


**FIG. 3.241** Transformers section of Library Browser.

### 3.8.2 Using parametric variables to specify the component values

Up to now, we used the numeric values to fill the components settings. PLECS allows you to use variables as well. The process of defining variables is shown with the aid of an example.

Double click on the resistor block and change the "Resistance:" box to "R" (Figs. 3.242 and 3.243).

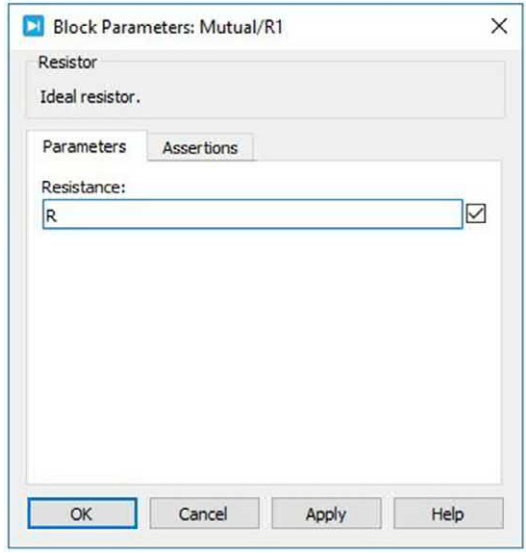


**FIG. 3.242** The Resistance box is not filled with a numeric value.

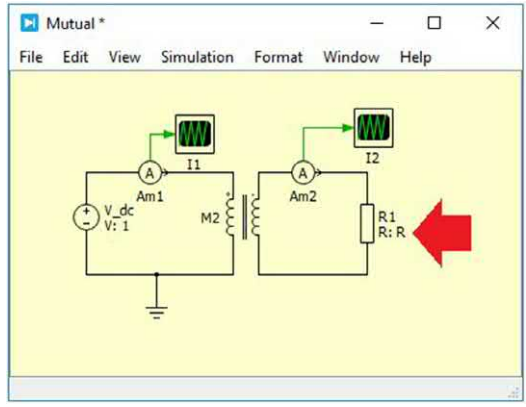


**FIG. 3.243** The schematic after changing the R1 resistor value to R.

Click the "Simulation parameters…" (Fig. 3.244).

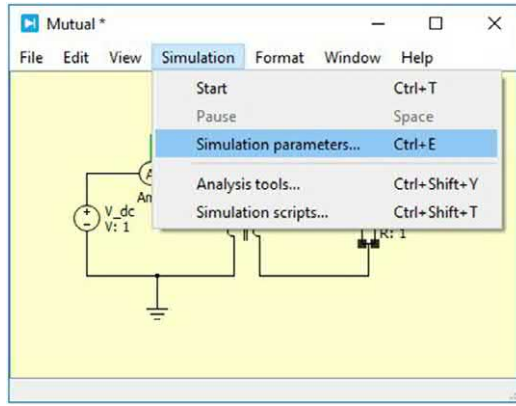


**FIG. 3.244** Opening the Simulation Parameters window by clicking the "Simulation parameters…".

PLECS opens the "Simulation Parameters" window. Go to the "Initialization" pane. Write R = 1 in the "Model initialization commands" section (Fig. 3.245).

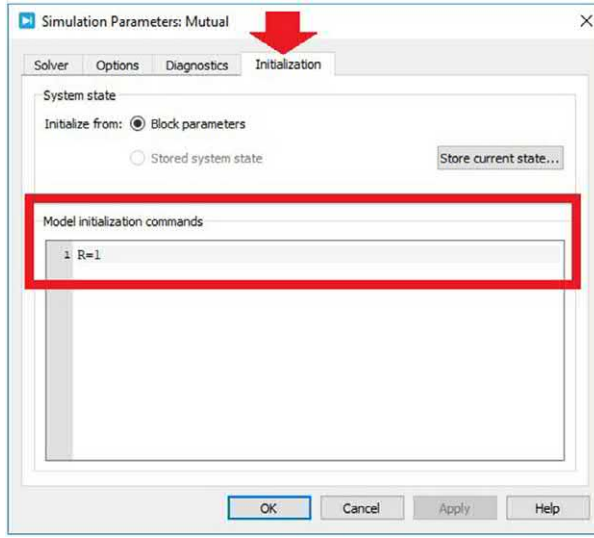


**FIG. 3.245** Initialization tab of Simulation Parameters window.

Using the aforementioned method, you can initialize the schematic more rapidly and more easily. Assume you have a symmetric 3-phase RL load. If you do not use the initialization, you must set 6 parameters if you decide to see the analysis results as load changes. Using initialization, you change just two parameters for each simulation.

## 3.9 Example 3.9: 3-Phase inverter

In this example, we will simulate a 3-phase inverter using the Sine Pulse Width Modulation (SVPWM) technique.

### 3.9.1 Preparing the simulation

The schematic of a 3-phase inverter is shown in Fig. 3.246. The Schematic is composed of three parts:

- PWM Generator
- Power Stage
- Load

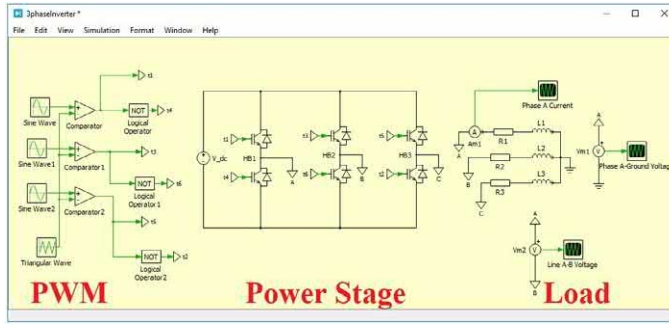


**FIG. 3.246** Simulation diagram of 3-phase inverter.

#### *3.9.1.1 PWM Generator*

The PWM generator section of the inverter is shown in Fig. 3.247. It uses Sine PWM (SPWM) to generate control signals. The PWM generator is composed of "Comparator," "Logical Operator," and "Sine Wave Generator" blocks. See Figs. 3.248–3.250 to learn their places.

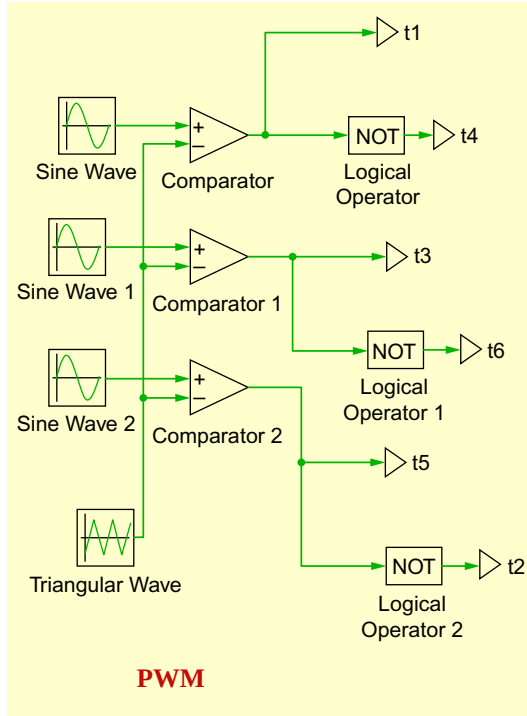


**FIG. 3.247** PWM generation section.

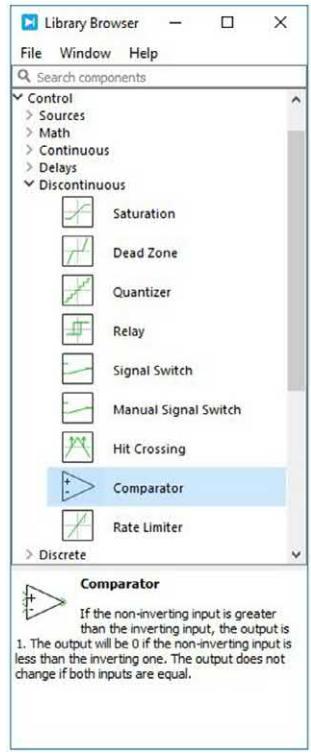


**FIG. 3.248** Comparator block.

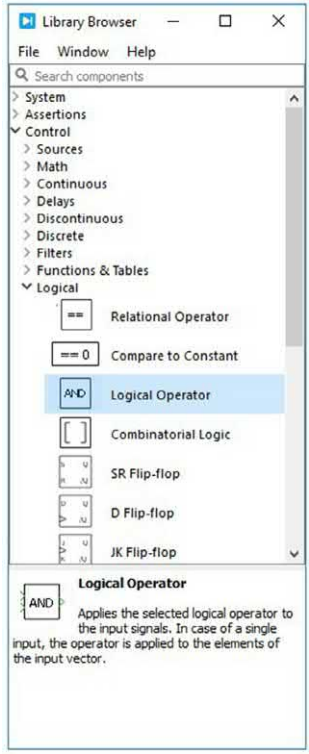


**FIG. 3.249** Logical Operator block.

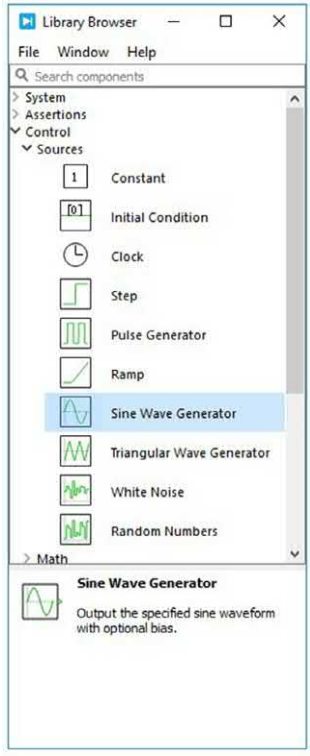


**FIG. 3.250** Sine Wave Generator block.

When you place the "Logical Operator" block on the schematic, it will be shown as Fig. 3.251. It must be converted into a NOT gate.

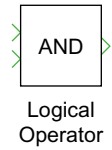


**FIG. 3.251** Logical Operator block.

Double click on the Logical Operator block (Fig. 3.252).

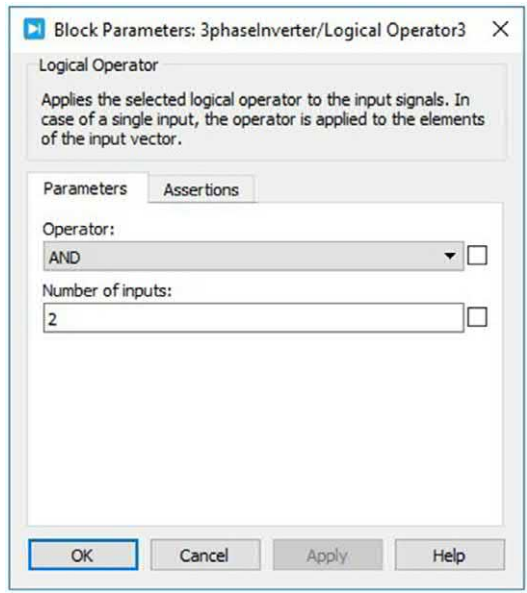


**FIG. 3.252** Logical Operator block settings.

Select the "NOT" from the "Operator" drop down list (Fig. 3.253).

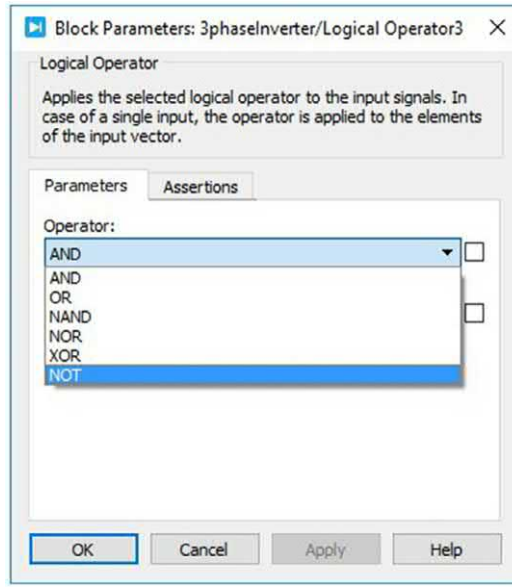


**FIG. 3.253** Turning the logical operator block into a NOT gate.

Set the "Number of inputs:" to 1 (Fig. 3.254).

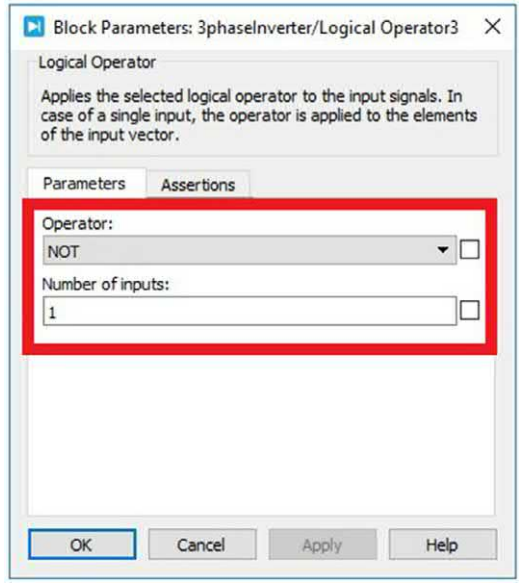


**FIG. 3.254** Turning the Number of inputs into 1.

"Sine Wave Generator" blocks settings are shown in Figs. 3.255–3.257.

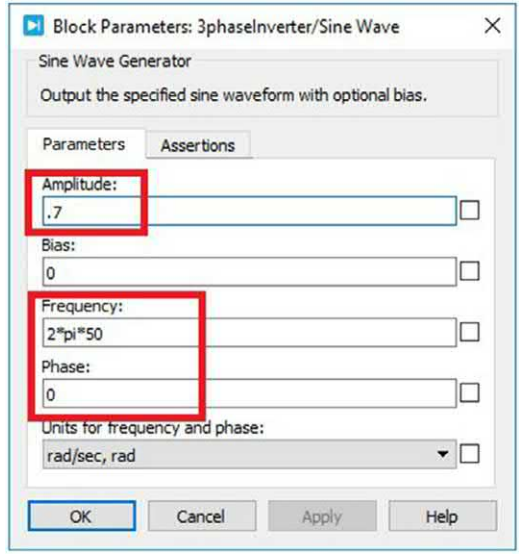


**FIG. 3.255** "Sine Wave" block settings (see Fig. 3.247).

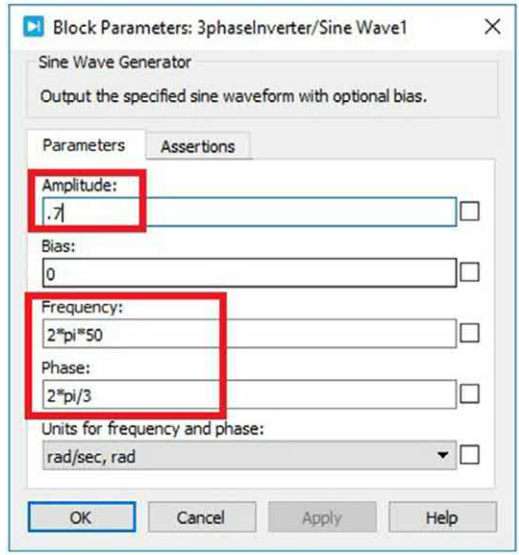


**FIG. 3.256** "Sine Wave1" block settings (see Fig. 3.247).

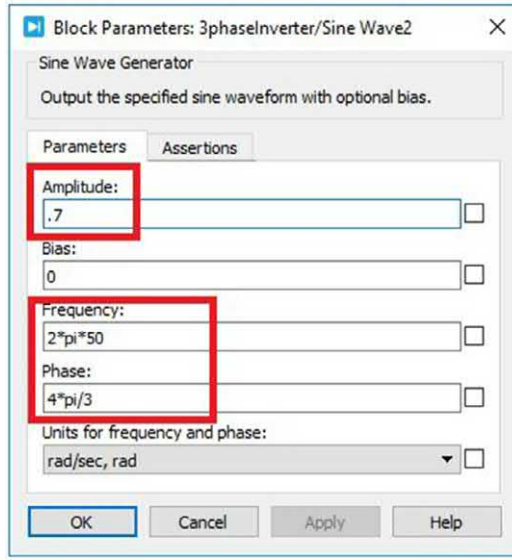


**FIG. 3.257** "Sine Wave2" block settings (see Fig. 3.247).

### 3.9.1.2 *Power Stage*

Power stage is shown in Fig. 3.258. It composed of 6 IGBTs. Instead of using 6 separate IGBT blocks, you can use three ready-to-use IGBT legs (see Fig. 3.259).

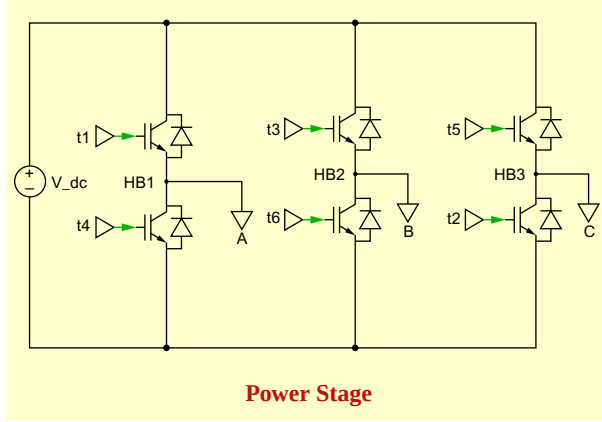


**FIG. 3.258** Power Stage section of 3-phase inverter.

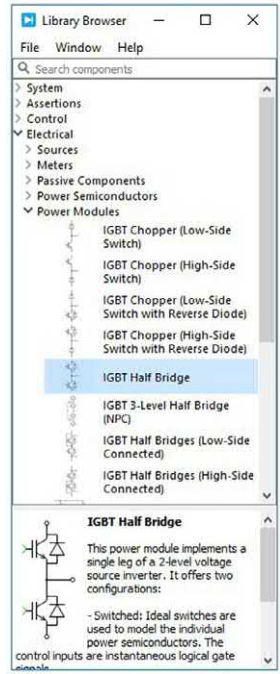


**FIG. 3.259** IGBT Half-Bridge block.

### 3.9.1.3 *Load*

Load is shown in Fig. 3.260. It is Y-connected balanced load ($R = 4\,\Omega$ and $L = 5\,\text{mH}$).

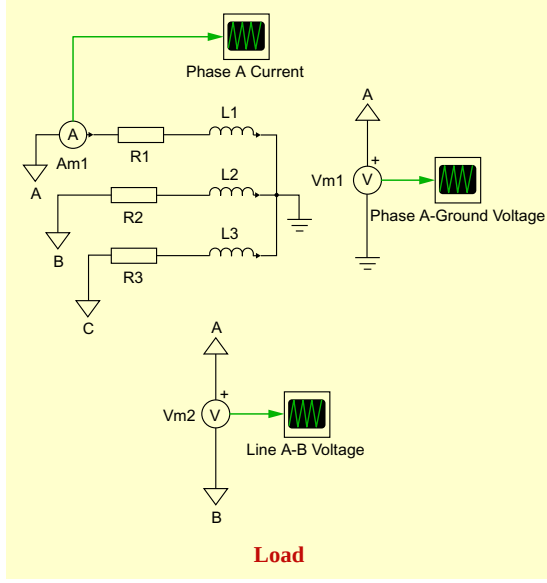


**FIG. 3.260** Load section of 3 phase rectifier ($R = 4\,\Omega$ and $L = 5\,\text{mH}$).

Simulation results are shown in Figs. 3.261–3.263.

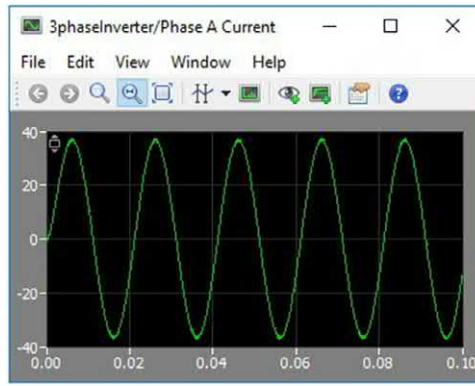


**FIG. 3.261** Phase A current.

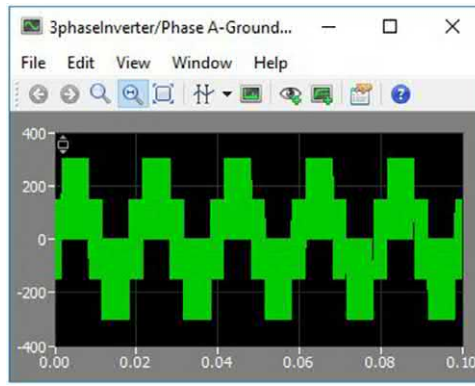


**FIG. 3.262** Phase A-ground voltage.

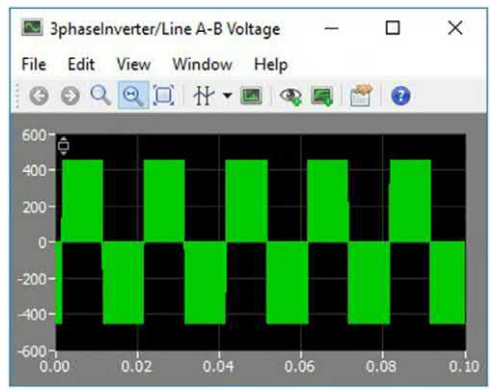


**FIG. 3.263** Line-to-line voltage.

### 3.9.2 Calculating the total harmonic distortion (THD)

PLECS can calculate the THD of a waveform. You can use the "Discrete Total Harmonic Distortion" block to calculate the THD (Fig. 3.264).

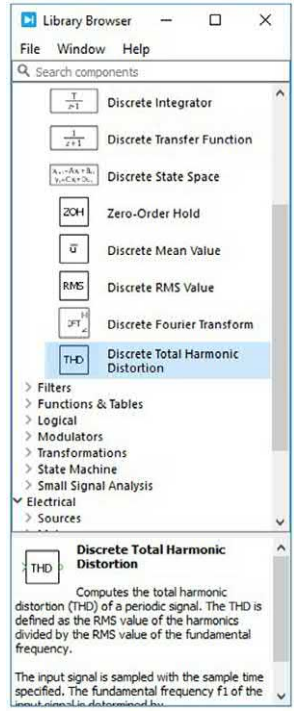


**FIG. 3.264** "Discrete Total Harmonic Distortion" block.

Before calculating the THD of the 3-phase inverter, we will study a simple example to learn how "Discrete Total Harmonic Distortion" block works. Assume a simulation like that shown in Fig. 3.265.

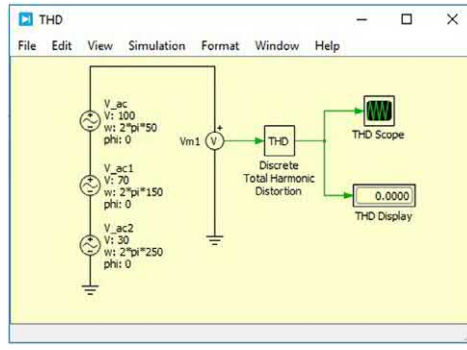


**FIG. 3.265** A simple simulation diagram to understand the working principle of "Discrete Total Harmonic Distortion" block.

According to Fig. 3.265, the input voltage is

$$100\sin(2\times\pi\times50\times t)+70\sin(2\times\pi\times150\times t)+30\sin(2\times\pi\times250\times t)$$

This voltage has fundamental frequency of 50 Hz and contains 3rd and 5th harmonics. This voltage can be drawn easily using MATLAB as shown in Fig. 3.266. Result is shown in Fig. 3.267. As you can see, the waveform does not seems like a pure sinusoidal wave since it contains harmonics. So, we expect a high THD for it.

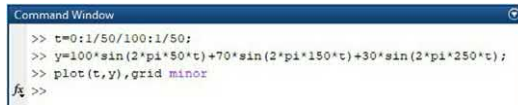


**FIG. 3.266** MATLAB code to draw one period of the $100\sin(2\times\pi\times50\times t)+70\sin(2\times\pi\times150\times t)+30\sin(2\times\pi\times250\times t)$.

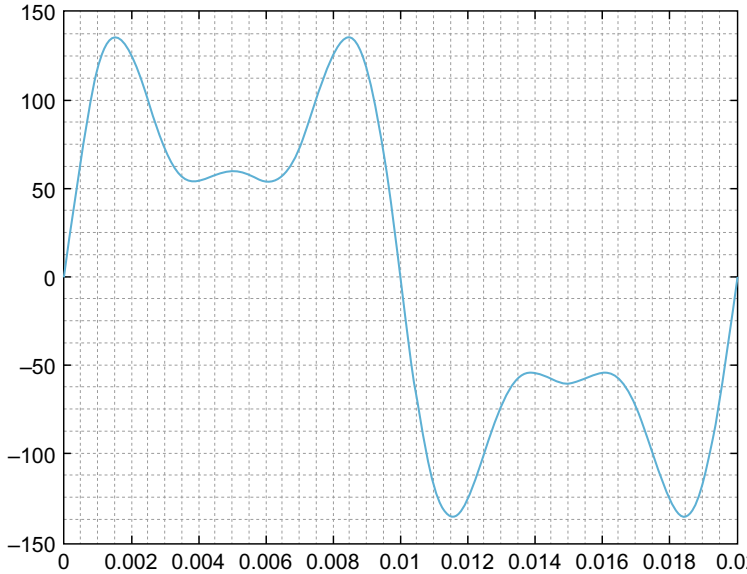


**FIG. 3.267** Diagram of $100\sin(2\times\pi\times50\times t)+70\sin(2\times\pi\times150\times t)+30\sin(2\times\pi\times250\times t)$.

THD of input voltage can be calculated easily using the following formula

$$\mathrm{THD}=\frac{\sqrt{\sum_{n=2}^{\infty}V_n{}^2}}{V_1}=\frac{\sqrt{\left(\frac{70}{\sqrt{2}}\right)^2+\left(\frac{30}{\sqrt{2}}\right)^2}}{\frac{100}{\sqrt{2}}}=\frac{53.85}{70.71}=0.76$$

$V_n$ shows RMS value of the $n$th harmonic.

We want to compare the simulation result with the pencil-and-paper analysis. Double click on the "Discrete Total Harmonic Distortion" block and do the setting as shown in Fig. 3.268.

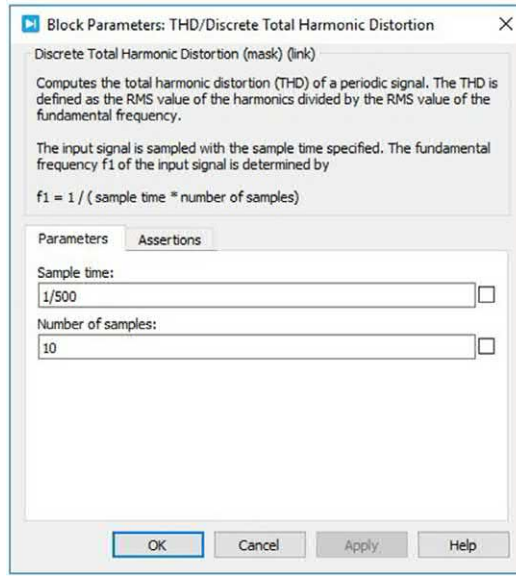


**FIG. 3.268** "Discrete Total Harmonic Distortion" block settings.

As shown in Fig. 3.268, the fundamental frequency of "Discrete Total Harmonic Distortion" block is calculated with the aid of:

$$f = \frac{1}{\text{Sample time} \times \text{Number of samples}}$$

Since we enter the "Sample time:" box as $\frac{1}{500}$ and "Number of samples:" as 10, the fundamental frequency is calculated as:

$$f = \frac{1}{\frac{1}{500} \times 10} = 50\,\text{Hz}$$

So with these settings, we specify the fundamental frequency correctly. If we run the simulation with the settings shown in Fig. 3.269, we obtain the result shown in Fig. 3.270. As you can see, PLECS calculates the THD as 0.7000, which is close to pencil-and-paper analysis.

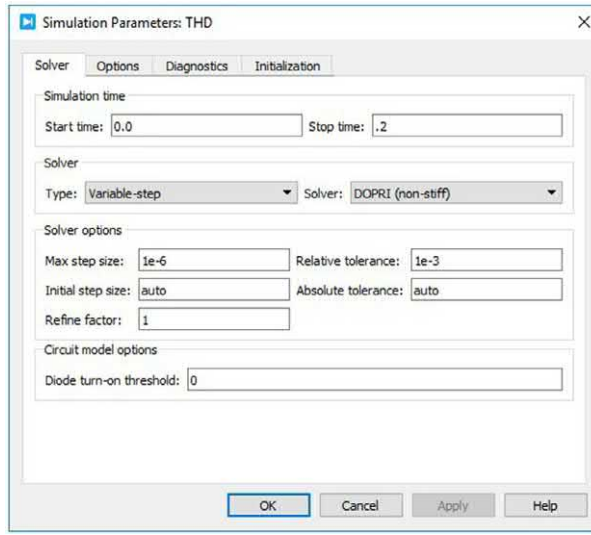


**FIG. 3.269** Simulation Parameters.

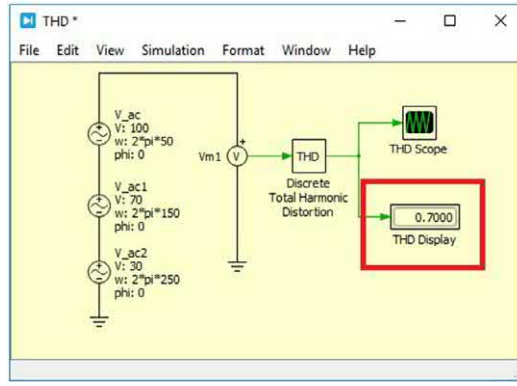


**FIG. 3.270** With settings shown in Fig. 3.268, THD is calculated as 0.7000.

You can open the "THD Scope" block and see the calculated THD as well. When you use scopes to monitor the output of "Discrete Total Harmonic Distortion" block only, notice the steady-state part of graph (Figs. 3.271 and 3.272). Transients part of graph has no importance.


**FIG. 3.271** Output of "Discrete Total Harmonic Distortion" block.

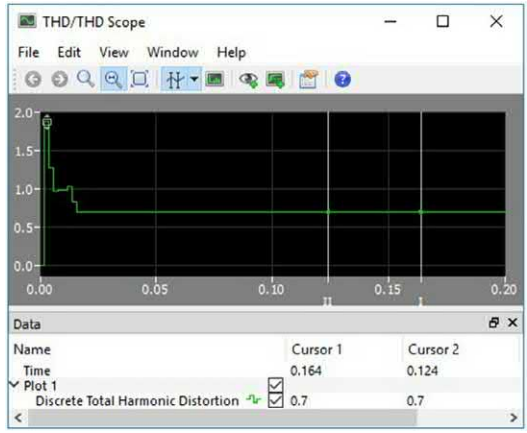


**FIG. 3.272** Using cursors to read the THD. Place cursor in the steady-state portion of the graph, transients part is not important. THD is calculated as 0.7.

"Number of samples" can be selected as 10 for most of simulations but you can increase it if you need more accuracy. We increase the "Number of samples" to 100 and decrease the "Sample time" to $\frac{1}{5000}$. So, the fundamental frequency is 50 Hz. If we run the simulation with settings shown in Fig. 3.273, the result shown in Fig. 3.274 will be obtained, which is close to the pencil-and-paper analysis.

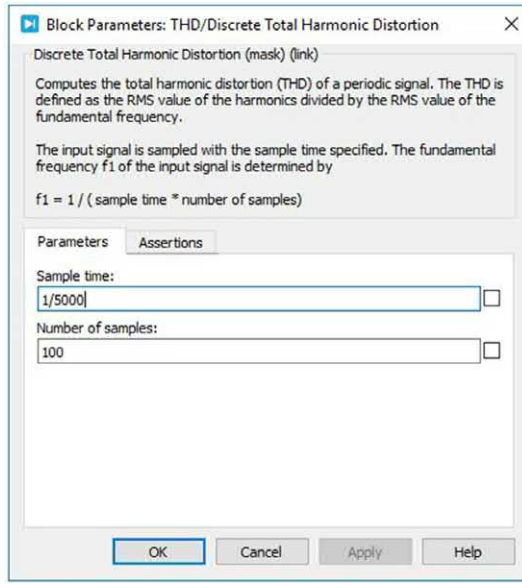


**FIG. 3.273** Increasing the "Number of samples" box to 100.

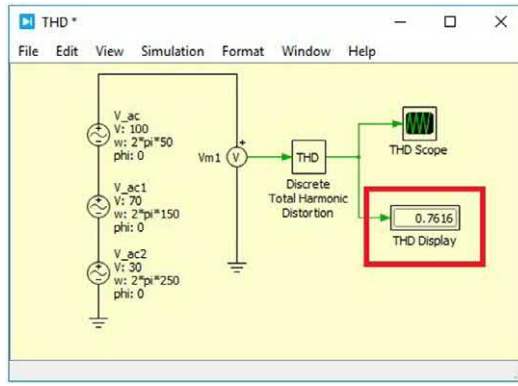


**FIG. 3.274** With settings shown in Fig. 3.273 THD is calculated as 0.7616.

We are ready to do the THD analysis of 3-phase inverter at this point. We change the schematic to that shown in Fig. 3.275. The "Discrete Total Harmonic Distortion" block settings are the same as Fig. 3.273.

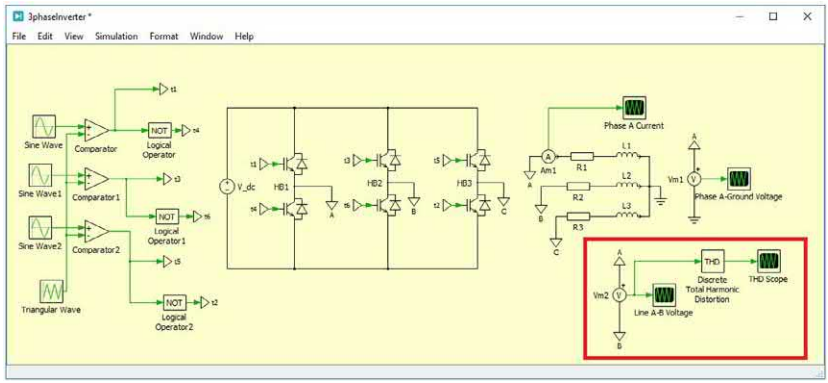


**FIG. 3.275** Connecting a "Discrete Total Harmonic Distortion" block to line-line voltage to measure its distortion.

If we run the simulation, we obtain the results shown in Fig. 3.276.

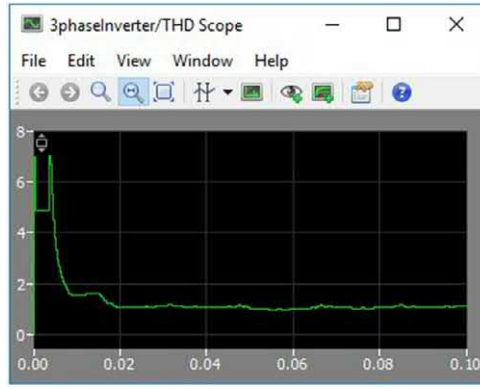


**FIG. 3.276** Output of "Discrete Total Harmonic Distortion" block.

You can zoom in the graph to see more details. The THD is about 1.10 (Fig. 3.277).

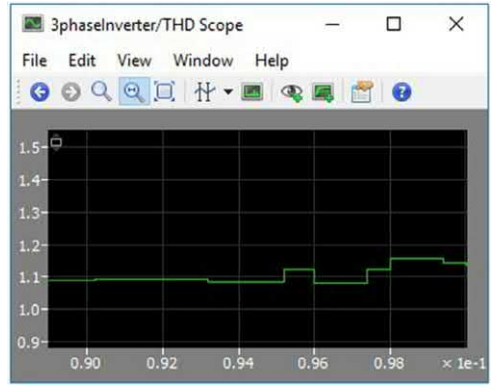


**FIG. 3.277** THD is about 1.1.

### 3.9.3 "Fourier series" block

Simulation diagram shown in Fig. 3.265 and redrawn in Fig. 3.278 for ease of reference can be drawn as shown in Fig. 3.279 using the "Fourier Series" block. Fourier series block can be found in the Functions and Tables section of Library Browser (Fig. 3.280).

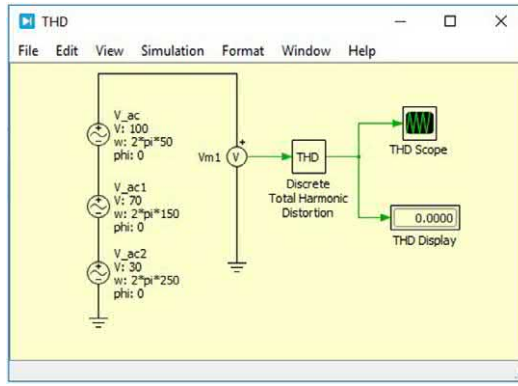


**FIG. 3.278** Producing the $100\sin(2\times\pi\times50\times t)+70\sin(2\times\pi\times150\times t)+30\sin(2\times\pi\times250\times t)$ using the AC voltage sources.

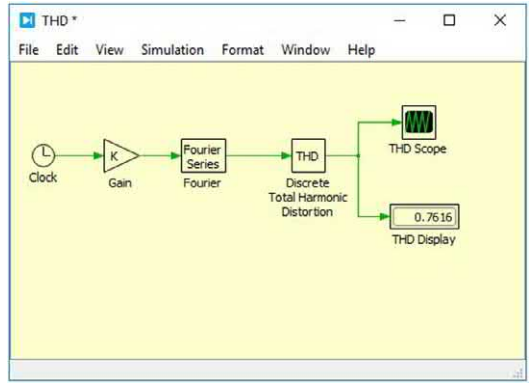


**FIG. 3.279** Using the Fourier Series block to produce the $100\sin(2\times\pi\times50\times t)+70\sin(2\times\pi\times150\times t)+30\sin(2\times\pi\times250\times t)$]

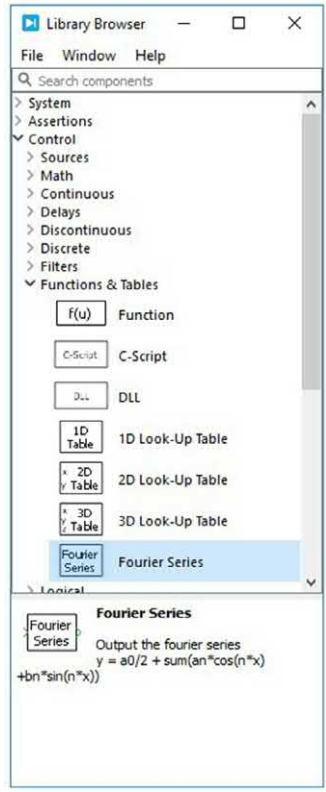


**FIG. 3.280** Fourier Series block.

Fourier series block takes the coefficients $a_n$ and $b_n$ and produces the output ($y$) given by:

$$y = \frac{a_0}{2} + \sum_{n=1,2,3,\ldots} a_n \cos(n.x) + \sum_{n=1,2,3,\ldots} b_n \sin(n.x),$$

where $x$ shows the input signal to the block. You can right click on the Fourier block and click the Help to see its description (Fig. 3.281).

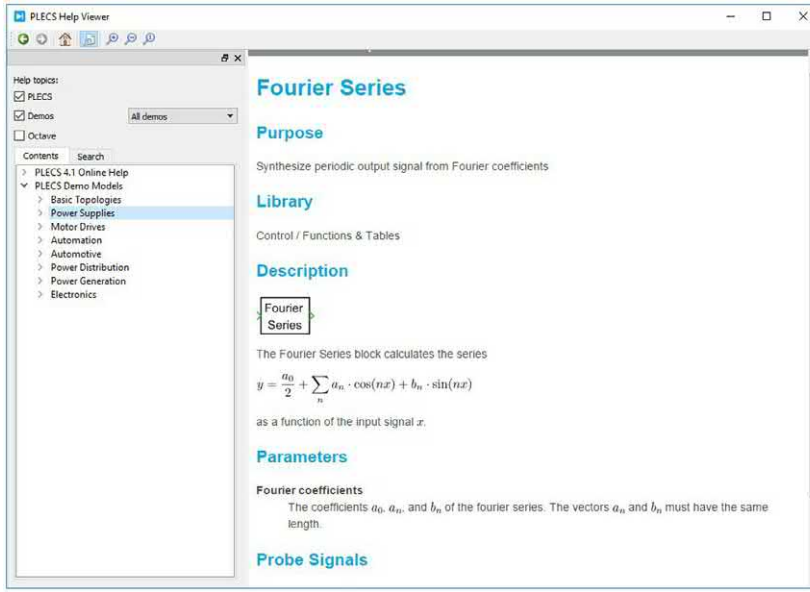


**FIG. 3.281** Fourier Series block documentation.

Double click on the Fourier block and set the parameters as shown in Fig. 3.282.

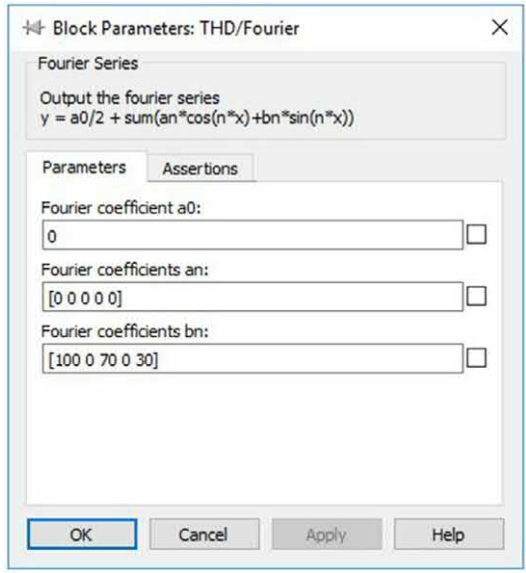


**FIG. 3.282** Fourier Series block settings.

Using the values shown in Fig. 3.282, we obtain the following output:

$$y = 100\sin(x) + 70\sin(3x) + 30\sin(5x)$$

If the input to the Fourier series block ($x$) equal to $2\pi \times 50 \times t$, we can produce the signal $y = 100\sin(2 \times \pi \times 50) + 70\sin(2 \times \pi \times 150) + 30\sin(2 \times \pi \times 250)$, which is exactly the required waveform. One can obtain $x = 2\pi \times 50 \times t$ by passing the clock signal from a constant gain block as shown in Fig. 3.283 (Fig. 3.284).

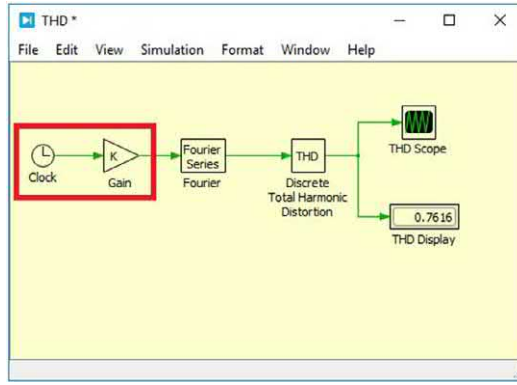


**FIG. 3.283** Producing the $2 \times \pi \times 50 \times t$ as the input of Fourier Series block. $t$ shows the time. Gain block equals to $2 \times \pi \times 50$.

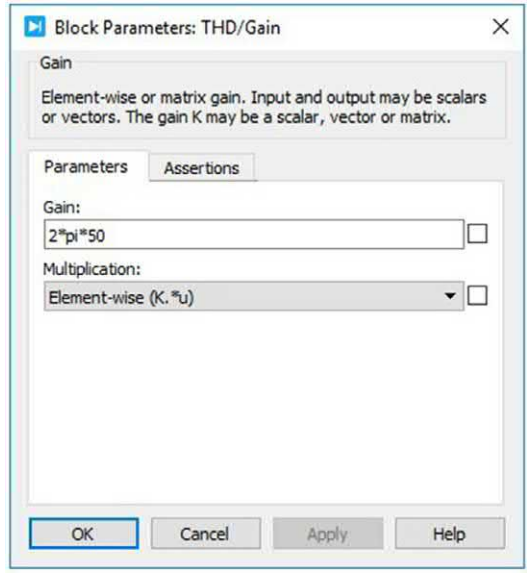


**FIG. 3.284** Gain block settings.

Clock block can be found in the "Sources" section of Library Browser (Fig. 3.285).

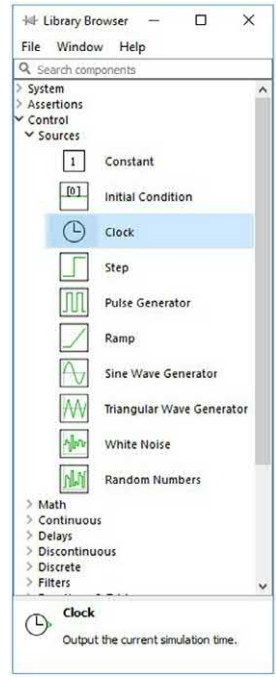


**FIG. 3.285** Clock block.

You can convert the output of Fourier series block into a voltage (which can drive circuits) using a controlled voltage source block. Controlled voltage source block can be found in the Sources section of Library Browser (Figs. 3.286 and 3.287).

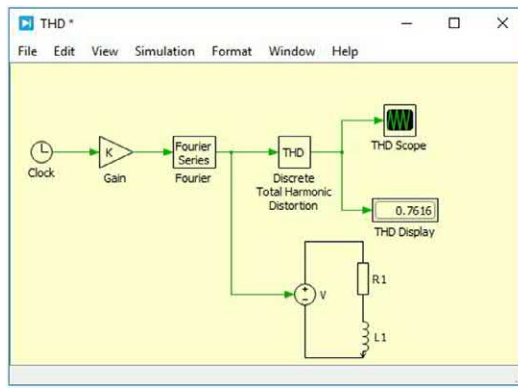


**FIG. 3.286** Conversion of Fourier Series block output into voltage using a controllable voltage source.

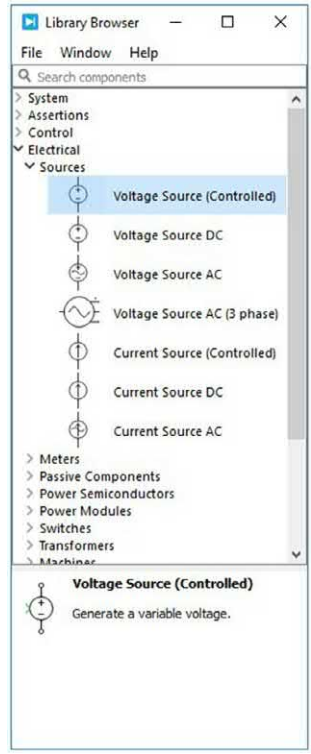


**FIG. 3.287** Voltage Source (Controlled) block.

## 3.10 Example 3.10: Simulation of electrical machines

PLECS has a powerful library of electrical machines. In this example, we will simulate a DC motor with a variable load.

### 3.10.1 Preparing the simulation

Simulation of electrical machines is possible in PLECS. PLECS has a power Machines library, which contains models of most electrical machines (Fig. 3.288).

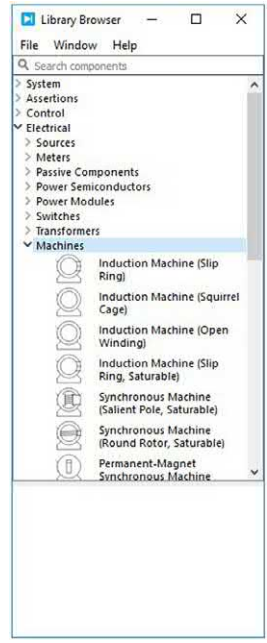


**FIG. 3.288** Machines section of the Library Browser.

PLECS has mechanical components such as loads, gear boxes, etc. These parts are placed in the "Mechanical" section of Library Browser (Fig. 3.289).

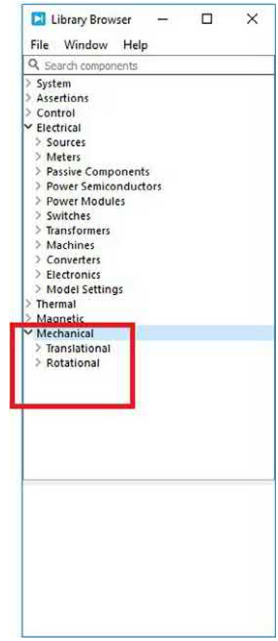


**FIG. 3.289** Mechanical section of Library Browser. It contains blocks to simulate both translational and rotational systems.

In this section, we study a simple example. Assume a simulation diagram such as one shown in Fig. 3.290. The blocks places used are shown in Figs. 3.291–3.294. The motor torque is 15 N m for $0 < t < 2$ s and increase to 30 N m or $t > 2$ s. We monitor the shaft speed.

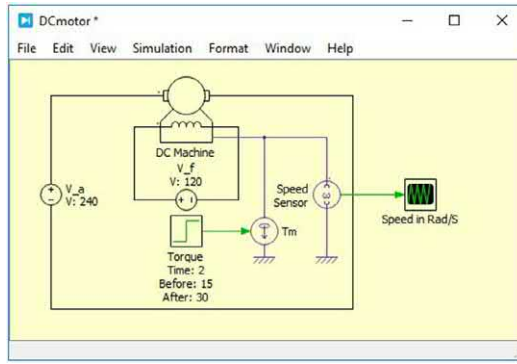


**FIG. 3.290** Simulation of DC machine connected to a variable load.

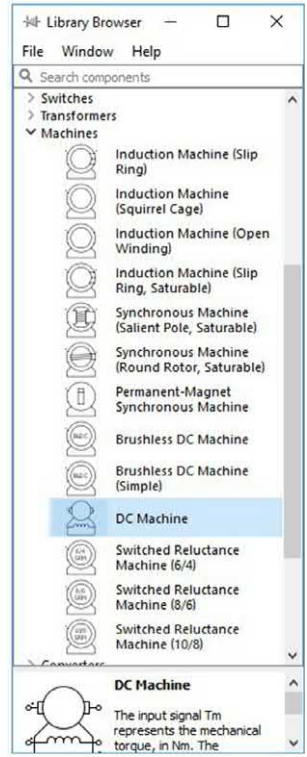


**FIG. 3.291** DC machine block.

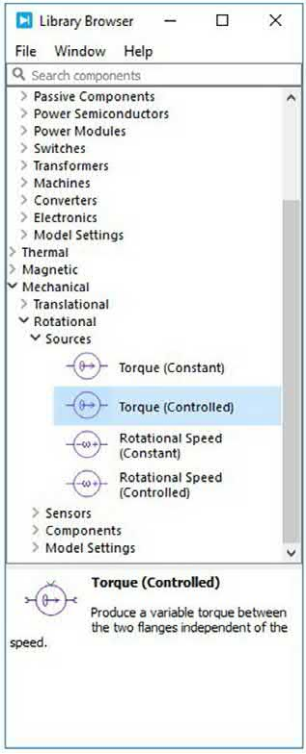


**FIG. 3.292** Torque (Controlled) block.

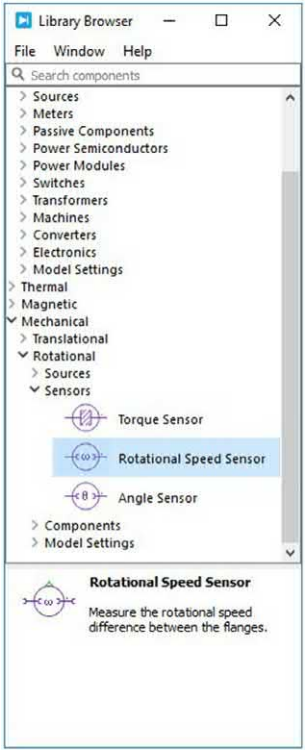


**FIG. 3.293** Rotational Speed Sensor block.

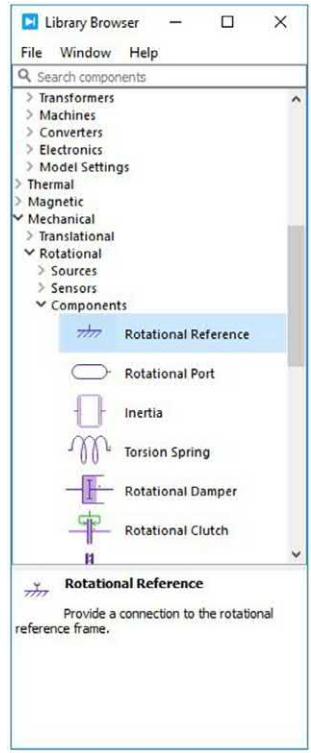


**FIG. 3.294** Rotational Reference block.

Blocks settings used are shown in Figs. 3.295 and 3.296.

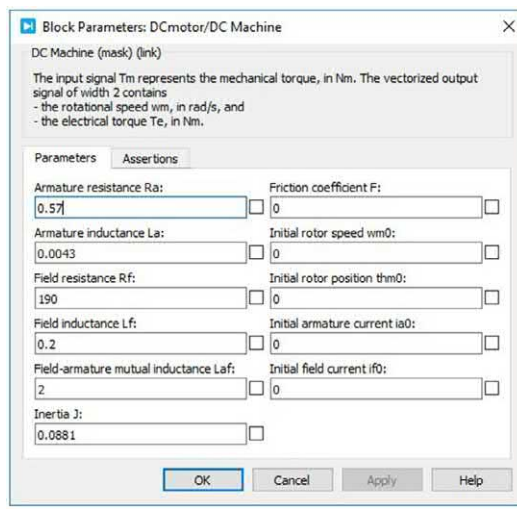


**FIG. 3.295** DC Machine settings.

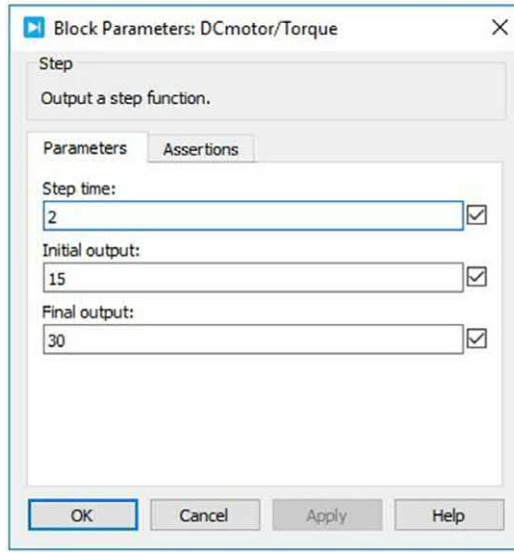


**FIG. 3.296** Torque block settings.

If we run the simulation with settings shown in Fig. 3.297, we obtain the results shown in Fig. 3.298.

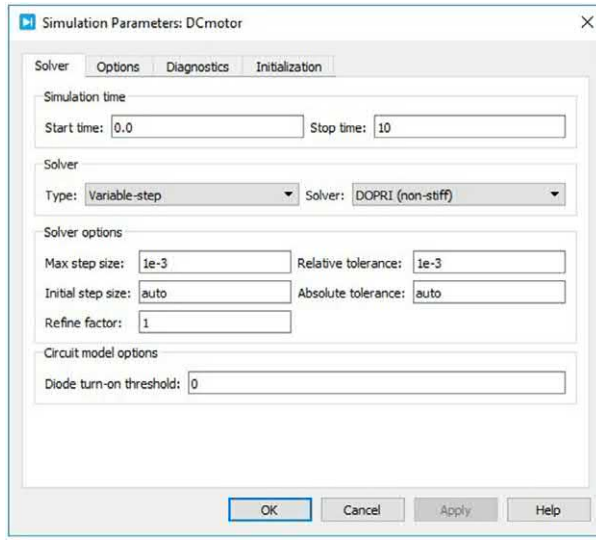


**FIG. 3.297** Simulation Parameter.

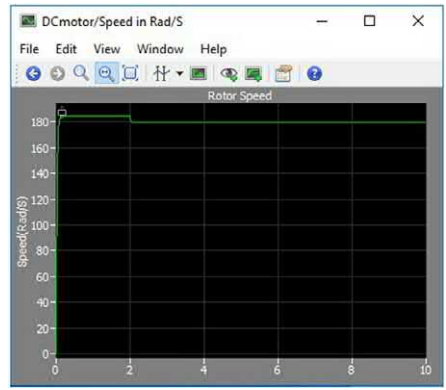


**FIG. 3.298** Rotor speed graph.

### 3.10.2 Monitoring using the probe block

You can use probe block to monitor the desired output as well. For example, assume that we want to see the armature current and shaft speed using the probe block. To do this, place a probe block on the schematic, double click on it to open it, and drag and drop the electric machine inside it (Fig. 3.299).

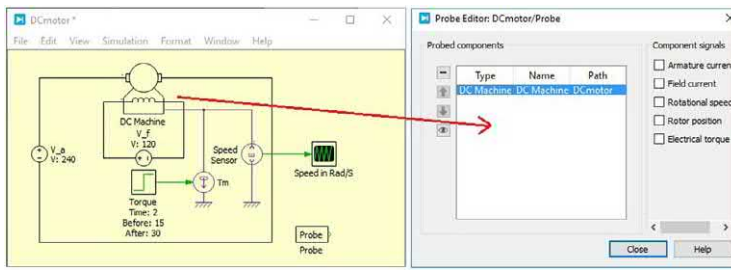


**FIG. 3.299** Dragging and dropping the DC Machine into the probe block.

Check the "Armature current" and "Rotational speed" boxes (Fig. 3.300).

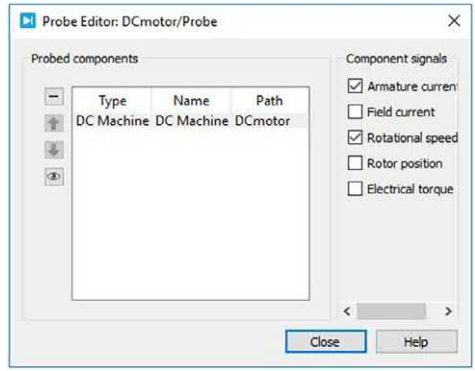


**FIG. 3.300** Probe block settings.

Connect the output of probe block to a demultiplexer and two scope blocks as shown in Fig. 3.301. Demultiplexer block can be found in the "System" section of Library Browser (Fig. 3.302).

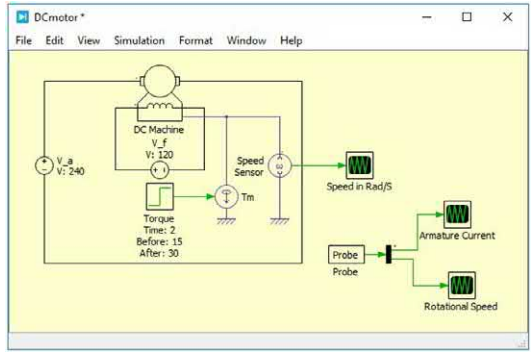


**FIG. 3.301** Connecting the probe block to a demultiplexer and scope blocks.

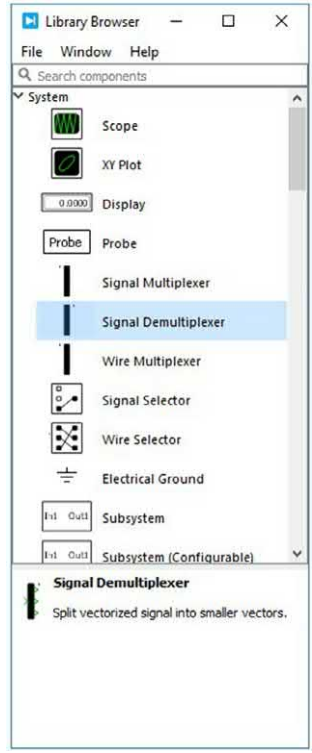


**FIG. 3.302** Signal Demultiplexer block.

If we run the simulation, we obtain the results shown in Figs. 3.303 and 3.304. As expected, machine speed decreases and the drawn current increases.

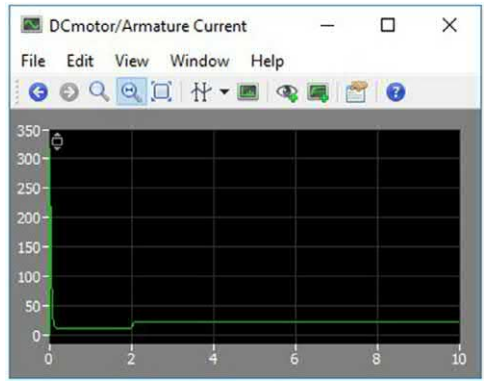


**FIG. 3.303** Armature current graph.

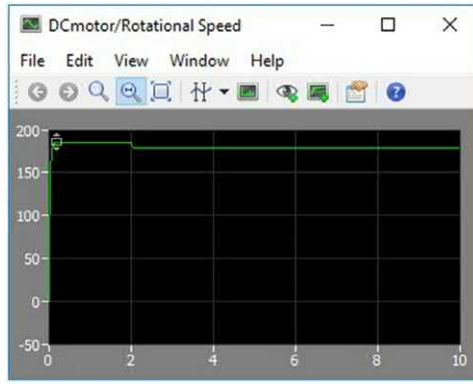


**FIG. 3.304** Shaft speed graph.

## References

[1] D. Hart, Power Electronics, Mc Graw Hill, 2011.

## Further reading

[2] P. Krein, Elements of Power Electronics, Oxford University Press, 2014.
[3] N. Mohan, T. Undeland, Power Electronics Converters, Applications and Design, Wiley, 2002.
[4] M. Rashid, Power Electronics Devices, Circuits and Applications, Pearson, 2013.
[5] R. Erikson, D. Maksimovic, Fundamentals of Power Electronics, Springer, 2001.
[6] S. Ang, A. Oliva, Power Switching Converters, Taylor & Francis, 2005.
[7] M.K. Kazimierczuck, Pulse Width Modulated DC-DC Power Converters, John Wiley, 2012.
[8] K. Ogata, Matlab for Control Engineers, Pearson, 2007.

Chapter 4

# Simulink® version of PLECS®

## Chapter outline



## 4.1 Introduction

We studied the standalone version of PLECS in the previous chapters. Simulink version of PLECS is the focus of this chapter. The Simulink version uses the Simulink solver to simulate the circuits. Working with Simulink version of PLECS is quite easy and similar to the standalone version.

Using the Simulink version of PLECS, you have access to all the Simulink blocks. So, the Simulink power is added to the PLECS power. For instance, assume that you want to simulate a converter, which has a fuzzy logic controller. You can simply use the Fuzzy Logic Toolbox® blocks and see the results readily. Such a simulation is not an easy task in standalone version. So, ensure to choose right tool for your problem.

## 4.2 Simulation of diode-clamped inverter

The user must enter the Simulink environment of MATLAB in order to access the PLECS block set. Type `simulink` in the command window to enter the Simulink environment (Fig. 4.1).


Simulation of Power Electronics Converters Using PLECS®. https://doi.org/10.1016/B978-0-12-817364-0.00004-7

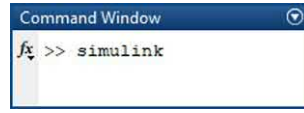


**FIG. 4.1** Entering the Simulink environment.

The PLECS block sets are added to the Simulink Library Browser window (Fig. 4.2).

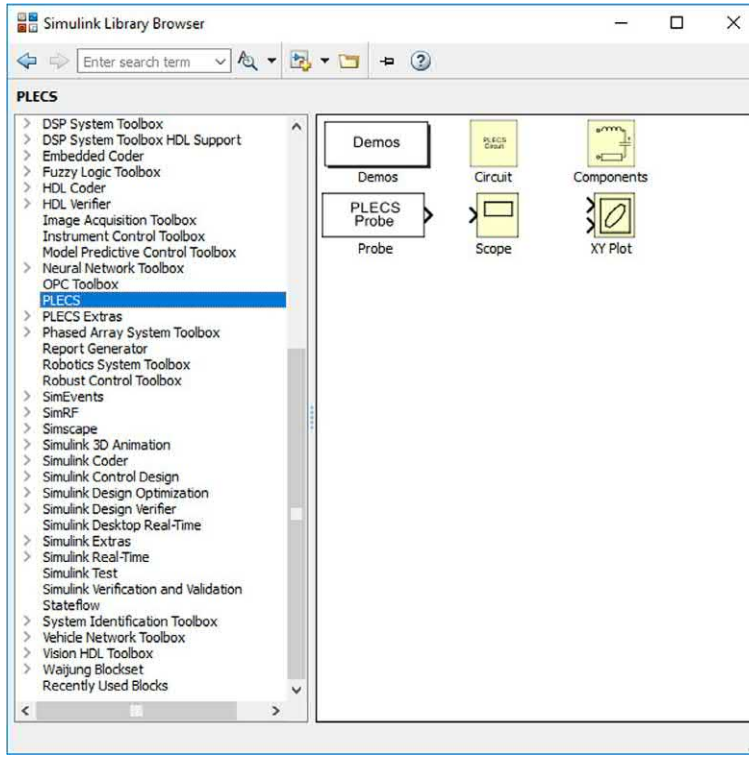


**FIG. 4.2** The PLECS blockset.

In order to simulate a power electronics converter, you must add a Circuit block to your simulation (Fig. 4.3).

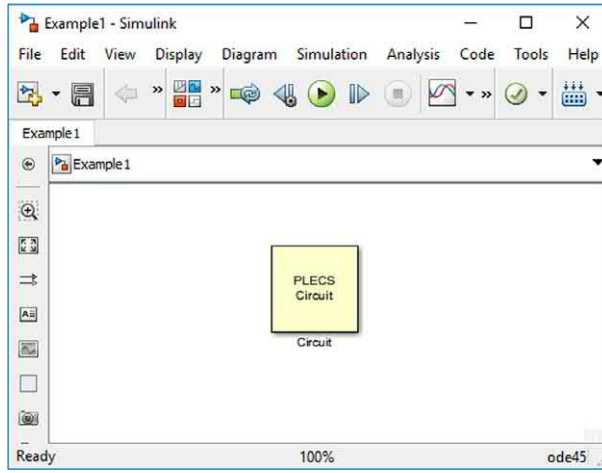


**FIG. 4.3** The PLECS circuit block.

Double click the PLECS Circuit block placed in the Simulink environment. The window shown in Fig. 4.4 will appear. As you see, the simulation environment is quite similar to the standalone version.

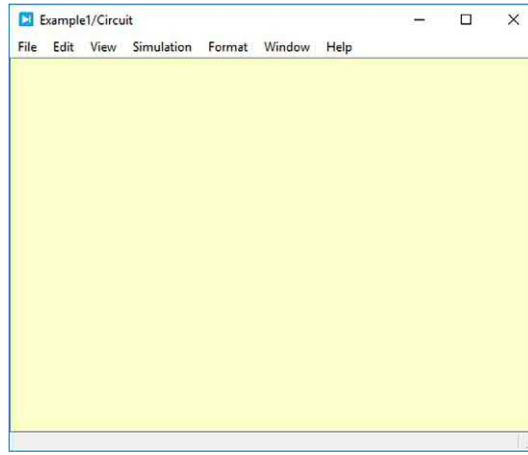


**FIG. 4.4** Inside the PLECS circuit block. You cannot use blocks from other Simulink libraries inside this area. Only blocks provided by PLECS block set can be used inside the PLECS circuit block.

You can import a file produced by standalone version of PLECS using the File menu (Fig. 4.5).

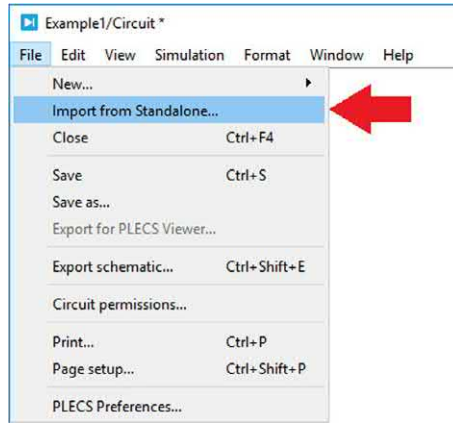


**FIG. 4.5** Importing a file produced by the PLECS Standalone.

Like the standalone version, the components used in the simulation are selected from the Library Browser window (Fig. 4.6).

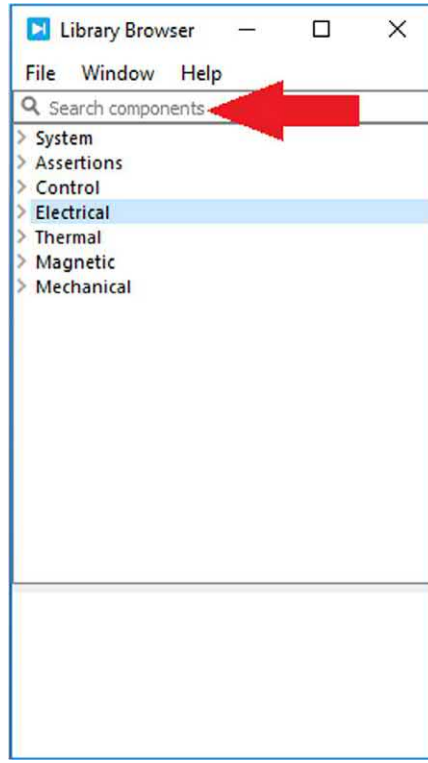


**FIG. 4.6** Library Browser window. You can search for a block by typing its name inside the Search components box.

Use the Window menu to appear the Library Browser window (Fig. 4.7).

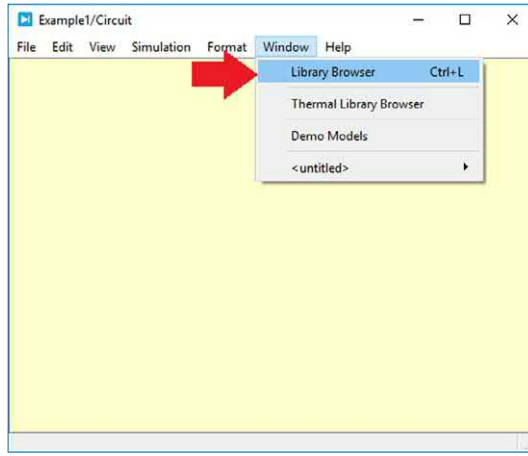


**FIG. 4.7** Click the Library Browser window to make the Library Browser window appear.

You can click the Components icon (Fig. 4.8) to appear the Library Browser window, as well.

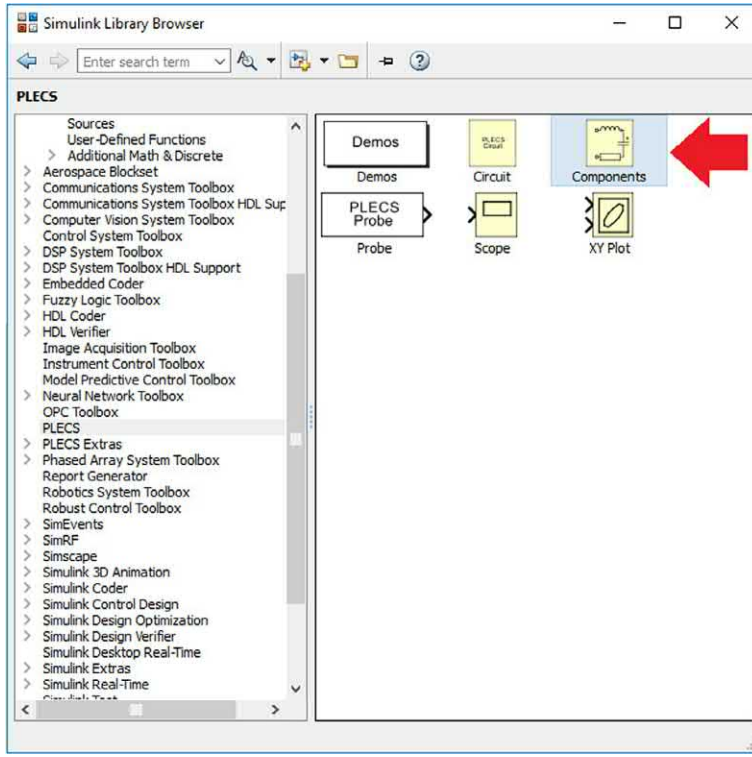


**FIG. 4.8** The Components section of PLECS block set.

## 4.3 Simulation of a diode-clamped multilevel inverter

Simulation of a diode-clamped multilevel inverter is studied as the first example. The simulation file is shown in Fig. 4.9.

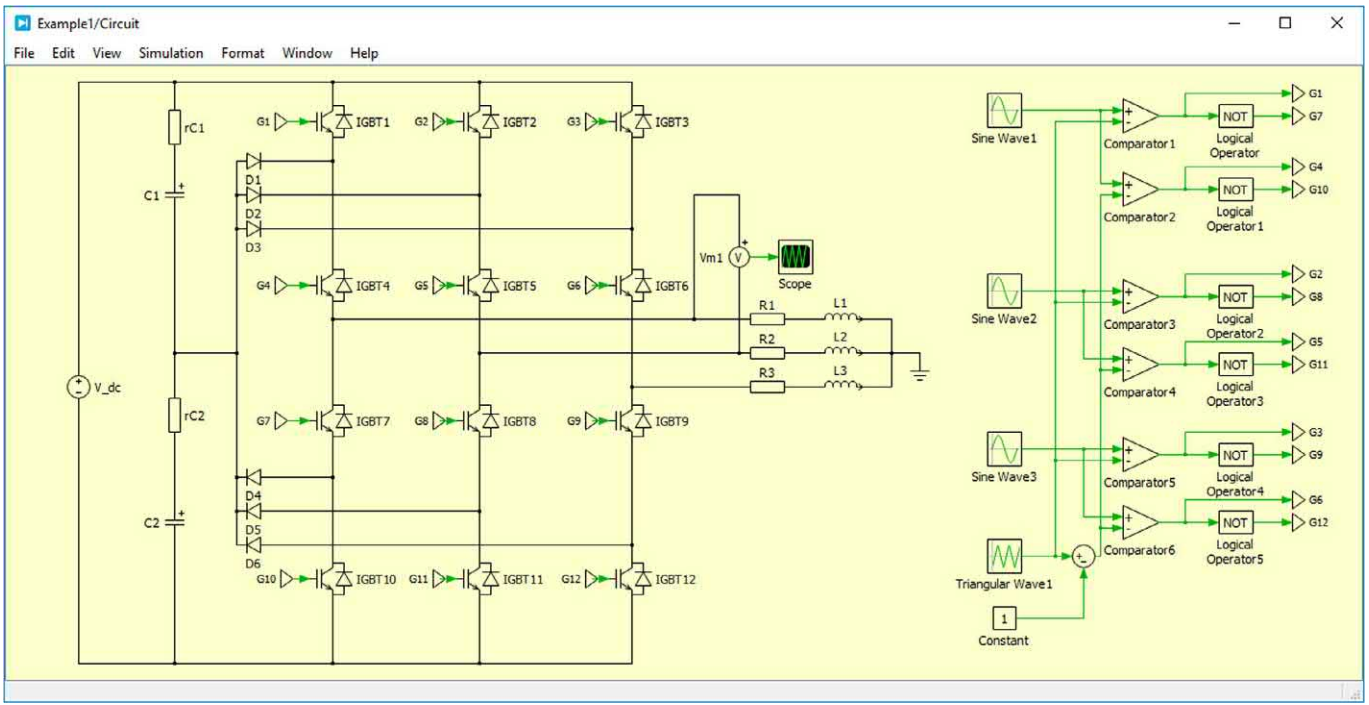


**FIG. 4.9** Schematic of diode-clamped multilevel inverter.

The prepared simulation file is composed of a power stage (Fig. 4.10) and a PWM generation section (Fig. 4.11).

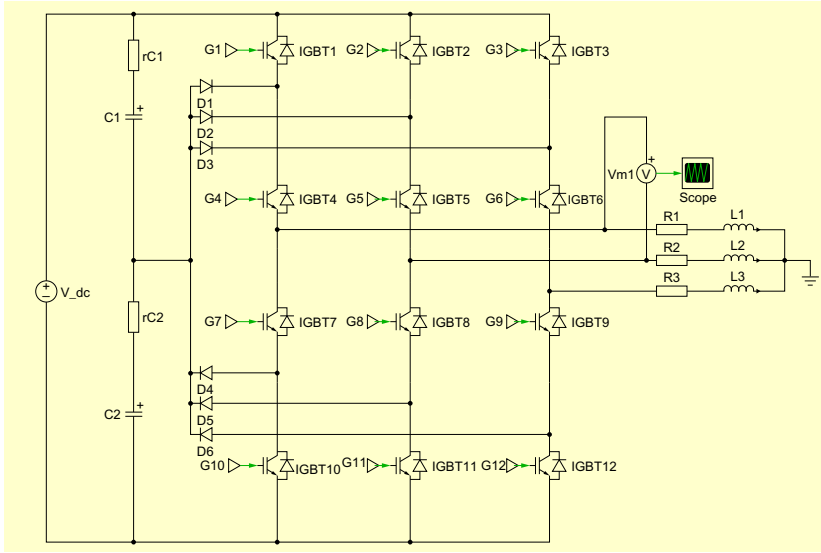


**FIG. 4.10** Power stage of diode-clamped multilevel inverter.

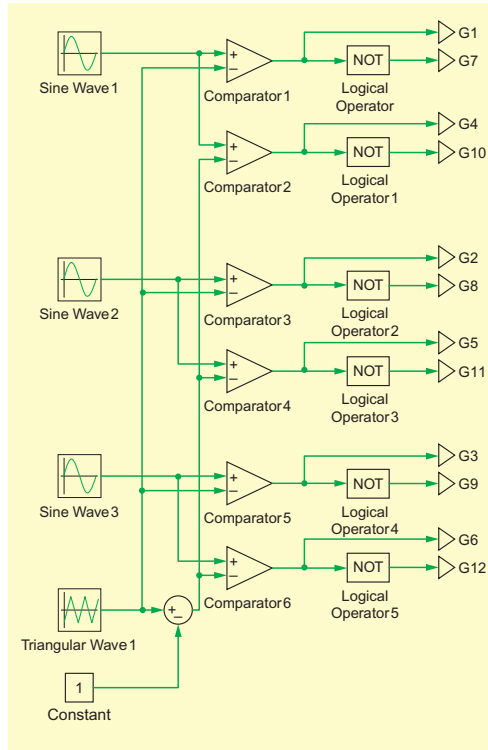


**FIG. 4.11** PWM generation section of diode-clamped multilevel inverter.

Production of PWM signal for multilevel inverters requires more than one carrier (Fig. 4.12).

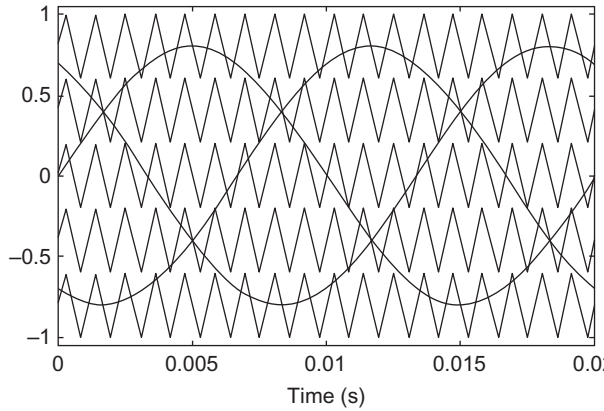


**FIG. 4.12** Production of PWM signal for a three-phase diode-clamped multilevel inverter with 11 levels of output. There are five carriers.

The required carriers for the studied diode-clamped inverter (Fig. 4.9) are shown in Fig. 4.13.

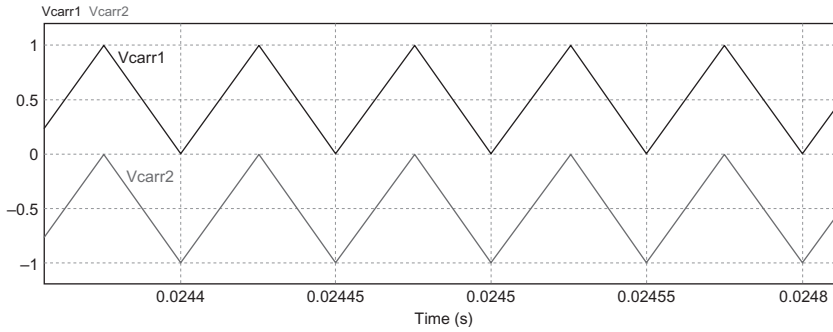


**FIG. 4.13** Carriers for production of PWM signal for a diode-clamped multilevel inverter with 5 levels of output. There are two carriers. The reference signal is not shown in this figure.

### 4.3.1 The power stage

Values of power stage components are shown in Figs. 4.14–4.20.

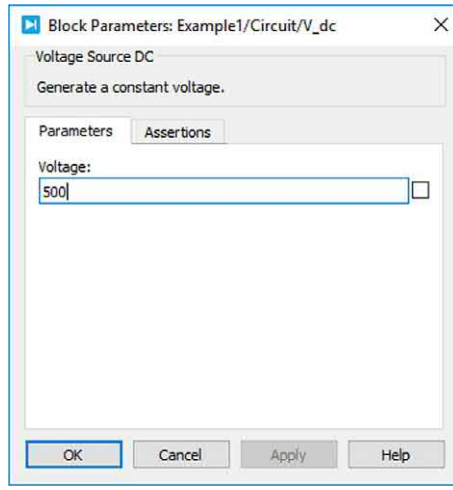


**FIG. 4.14** Input DC source settings.

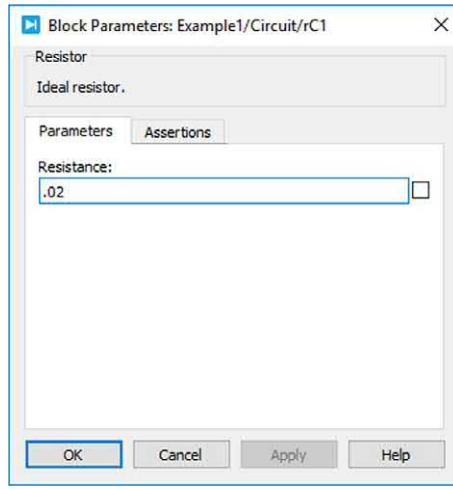


**FIG. 4.15** Resistor rC1 settings. The resistor rC2 has the same settings.

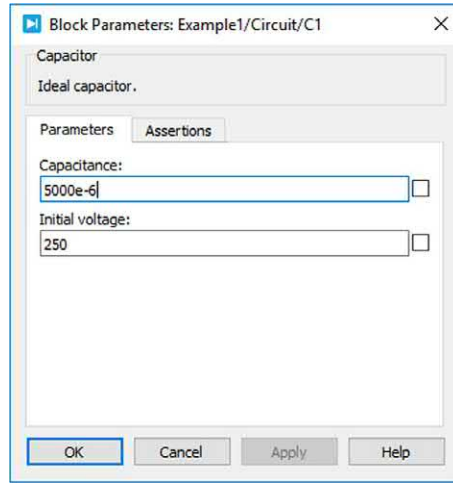


**FIG. 4.16** Capacitor C1 settings. The capacitor C2 has the same settings.

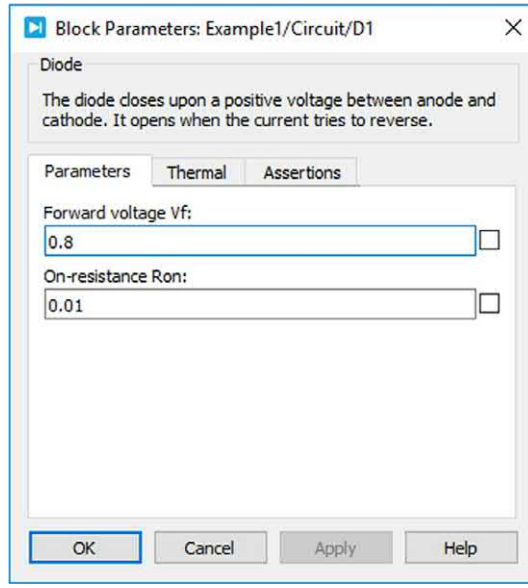


**FIG. 4.17** Diode D1 settings. Other diodes have the same settings.

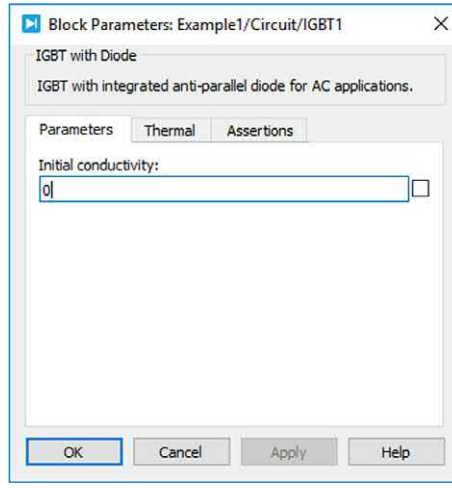


**FIG. 4.18** IGBT1 settings. Other IGBTs have the same settings.

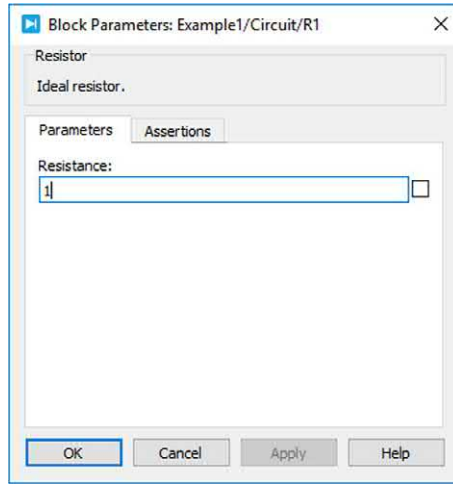


**FIG. 4.19** Resistor R1 settings. Resistors R2 and R3 have the same settings.

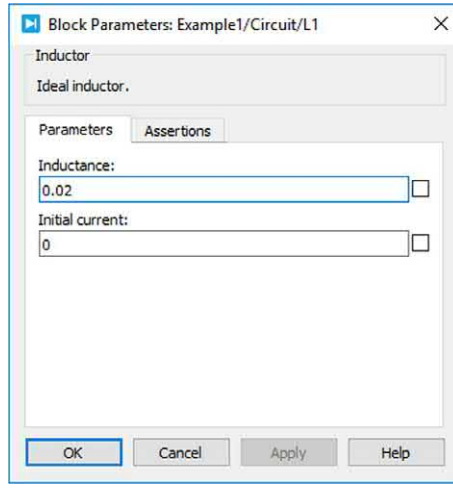


**FIG. 4.20** Inductor L1 settings. Inductors L2 and L3 have the same settings.

The line-line voltage is measured with the aid of a voltmeter. The voltmeter can be found in the Meters section of Library Browser window (Fig. 4.21).

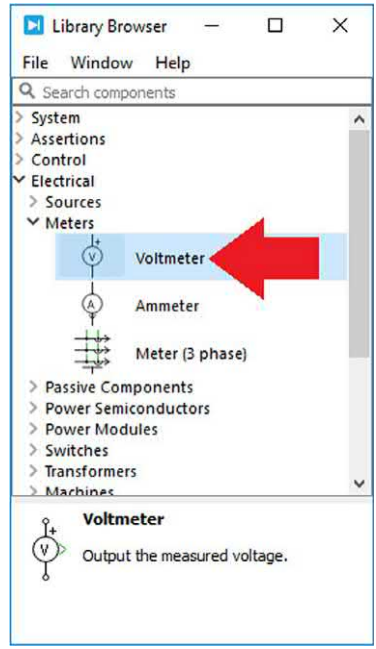


**FIG. 4.21** Voltmeter block.

The power stage has 12 Signal From blocks. The Signal From block can be found in the System section of library browser window (Figs. 4.22 and 4.23).

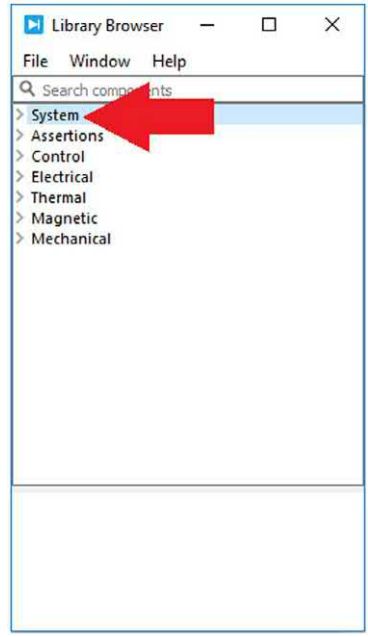


**FIG. 4.22** System section of Library Browser window.

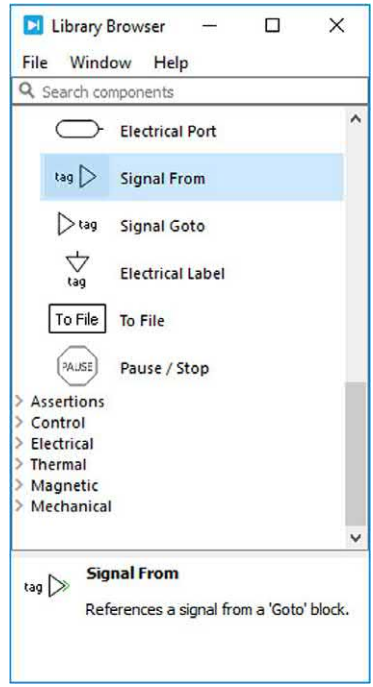


**FIG. 4.23** Signal From block.

The Tag name box of Signal From blocks is filled with G1, G2, G3, …, G12 (see Fig. 4.24). The Gi is the Signal From block connected to the gate of i-th IGBT.

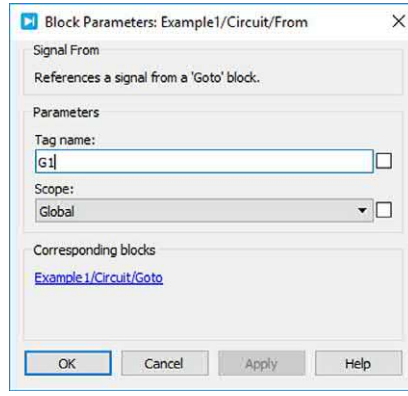


**FIG. 4.24** The Signal From block G1 settings. The Signals From blocks G2, G3, G4, …, G12 have G2, G3, G4, …, G12 in their Tag name box, respectively.

In fact, the simulation can be done without using the Signal Goto and Signal From blocks. However, the schematic becomes quite messy and un-understandable. Fig. 4.9 is redrawn in Fig. 4.25 for ease of reference. Compare Fig. 4.25 with Fig. 4.26. Fig. 4.26 is more structured and understandable than Fig. 4.25.

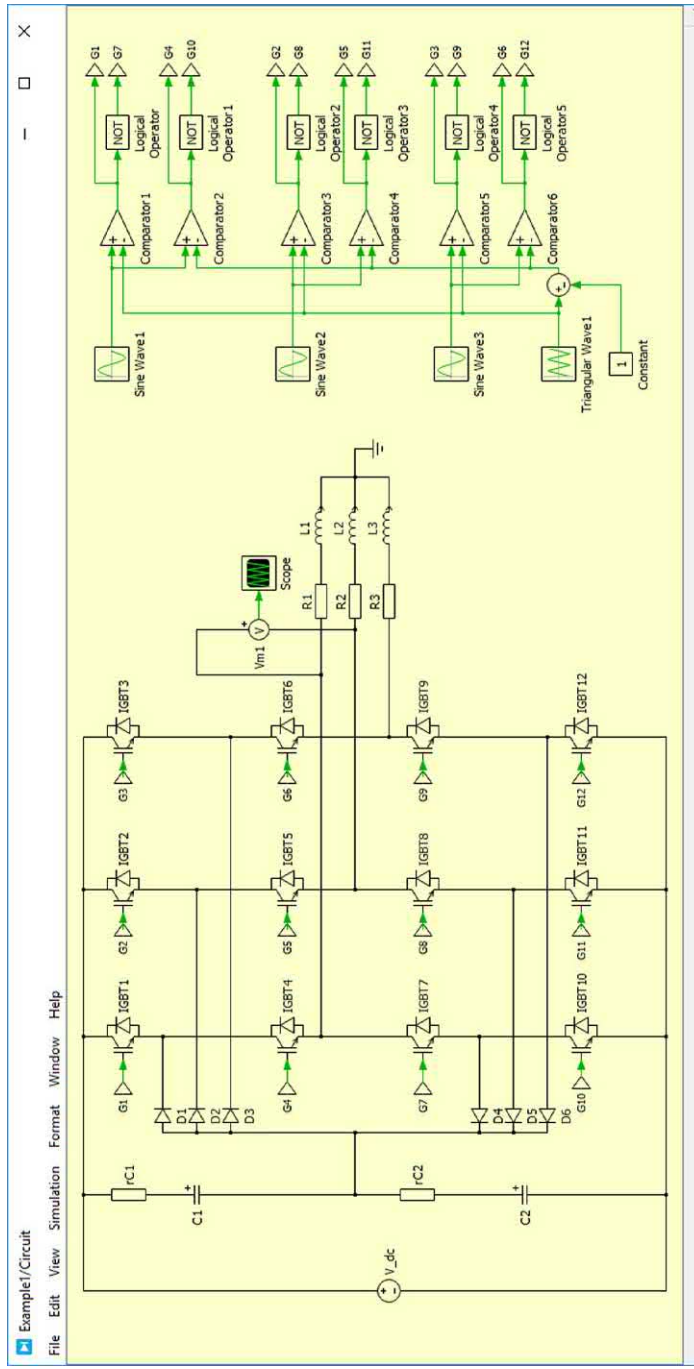


**FIG. 4.25** A good schematic example.

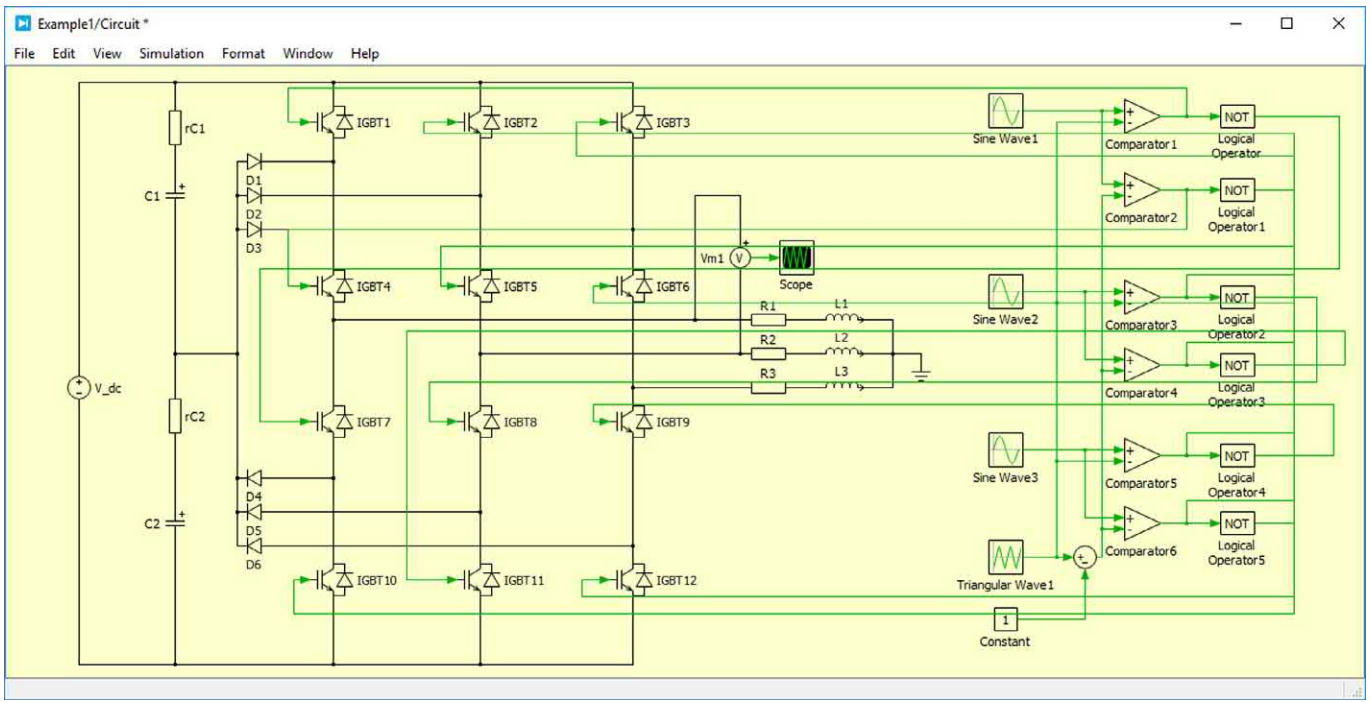


**FIG. 4.26** A messy and difficult-to-understand schematic. Avoid such schematics.

### 4.3.2 The PWM generation part

The PWM generation section of the simulation file is reshown in Fig. 4.27.

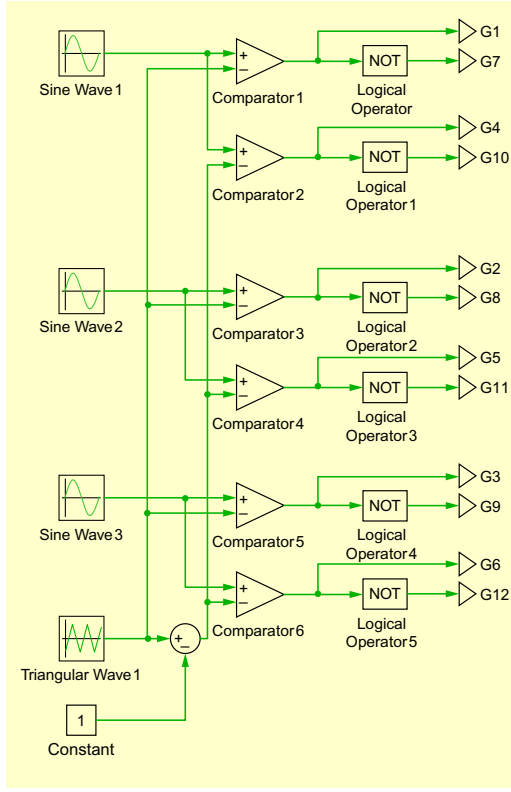


**FIG. 4.27** The PWM generation section.

Settings of the used blocks are shown in Figs. 4.28–4.32.

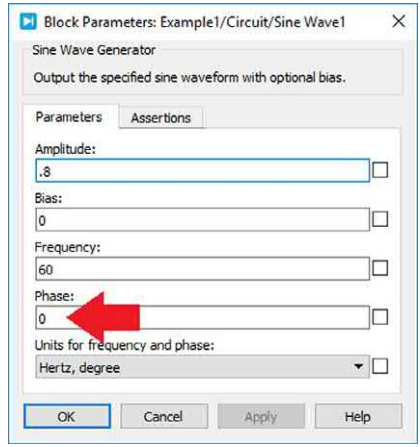


**FIG. 4.28** The Sine Wave1 block settings.

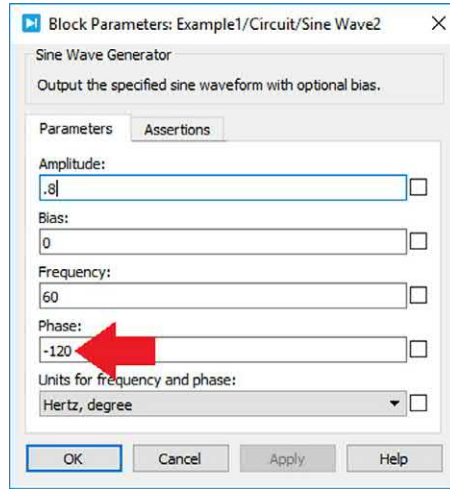


**FIG. 4.29** The Sine Wave2 block settings.

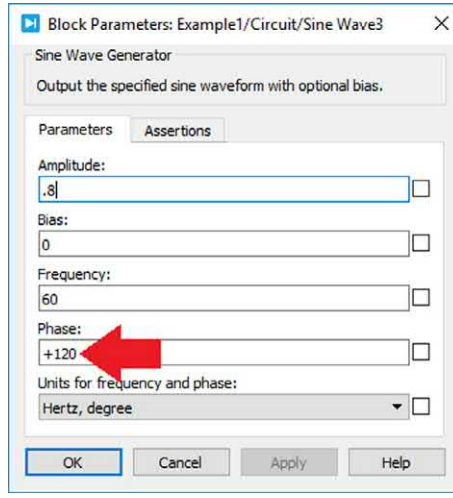


**FIG. 4.30** The Sine Wave3 block settings.

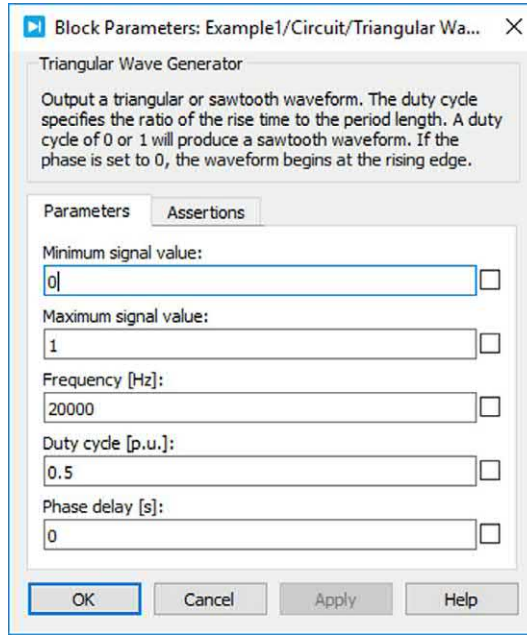


**FIG. 4.31** The Triangular Wave block settings.

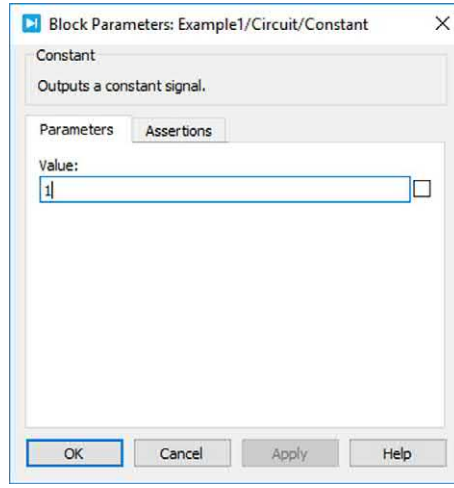


**FIG. 4.32** The Constant block settings.

The PWM generation section uses 6 comparators and not blocks. The comparator block can be found in the Discontinuous section of Library Browser window (Fig. 4.33).

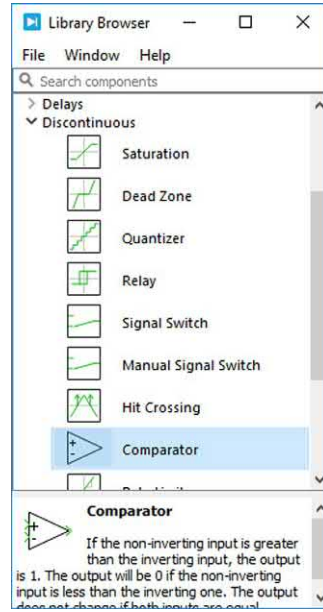


**FIG. 4.33** The Comparator block.

The required not gates are produced with the aid of Logical Operator block (Fig. 4.34). Set the Operator to NOT in order to obtain a not gate (Fig. 4.35).

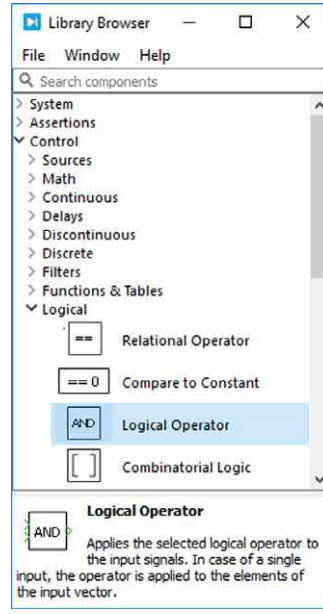


**FIG. 4.34** The Logical Operator block.

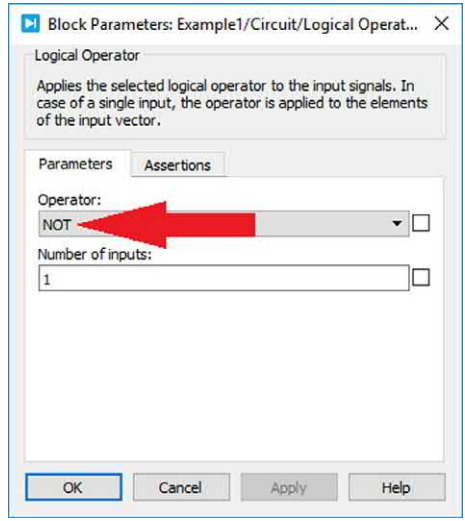


**FIG. 4.35** The Logical Operator block can be turned into a not block by selecting the NOT.

The calculated signals are transferred to the gate of IGBTs with the aid of 12 Signal Goto blocks. The Signal Goto block can be found in the System section of Library Browser (Figs. 4.36 and 4.37).

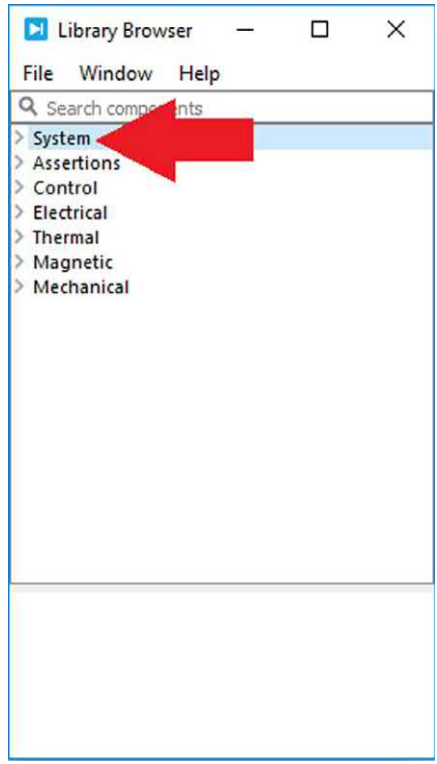


**FIG. 4.36** The System section of Library Browser window.

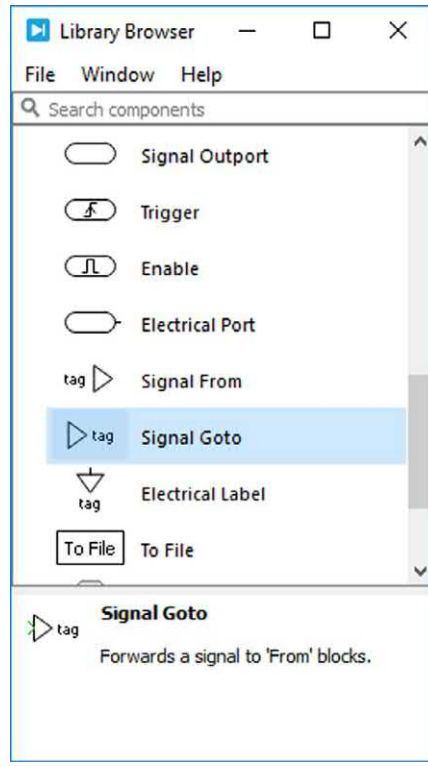


**FIG. 4.37** The Signal Goto block.

The Tag name box of Signal Goto blocks is filled with G1,G2,G3,…,G12. Gi is the signal, which goes to the gate of i-th IGBT (Fig. 4.38).

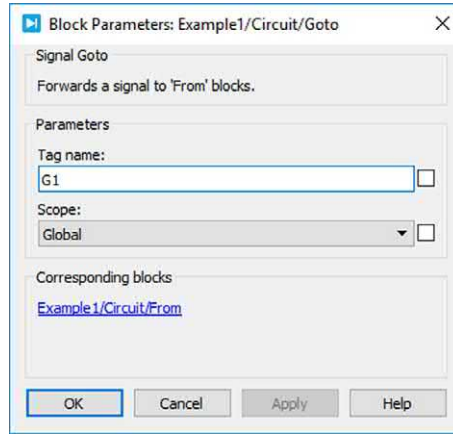


**FIG. 4.38** The Signal Goto block G1 settings. The Signal Goto blocks G2, G3, G4, …, G12 have G2, G3, G4, …, G12 in their Tag name box, respectively.

### 4.3.3 Simulation of circuit

Click the Simulink parameters… to set the desired simulation interval and solver (Fig. 4.39).

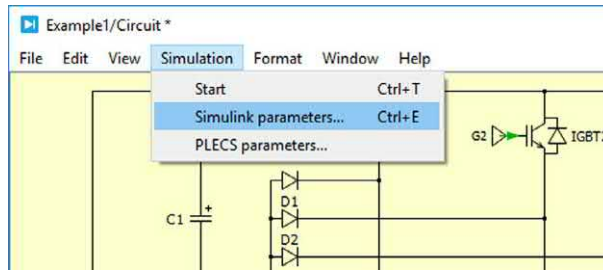


**FIG. 4.39** Use the Simulink parameters to set the simulation settings.

After you clicked the Simulink parameters… the window shown in Fig. 4.40 will appear. Use the Stop time box to set the desired simulation interval. Also, use the Solver to select the desired type of solver. Selection of ode23t(mod, stiff/Trapezoidal) is suggested.

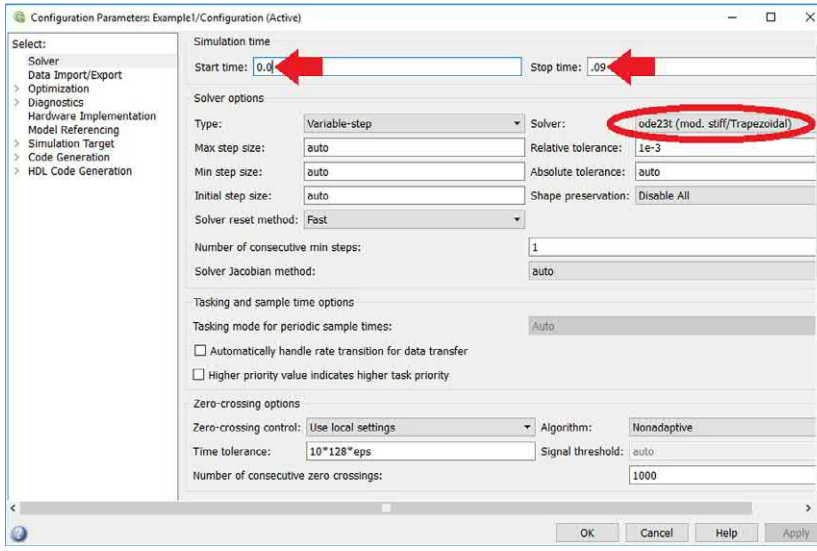


**FIG. 4.40** Configuration Parameters window.

After the desired simulation interval and Solver is entered, you can run the simulation. Click the Start in order to run the simulation (Fig. 4.41).

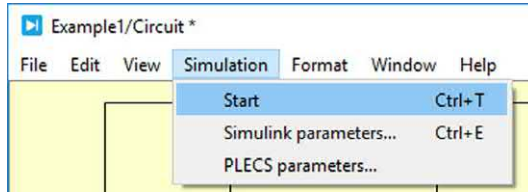


**FIG. 4.41** Click the Start to run the simulation.

You can run the simulation by clicking the run button in the Simulink environment as well (Fig. 4.42).

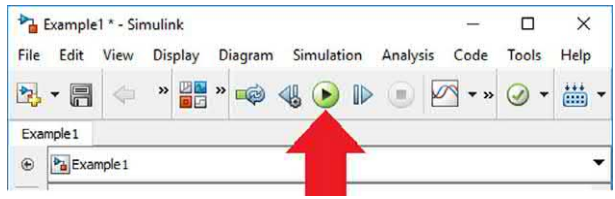


**FIG. 4.42** The Run button.

After the simulation is run, you can double click the scope block and see the line-line voltage waveform (Fig. 4.43).

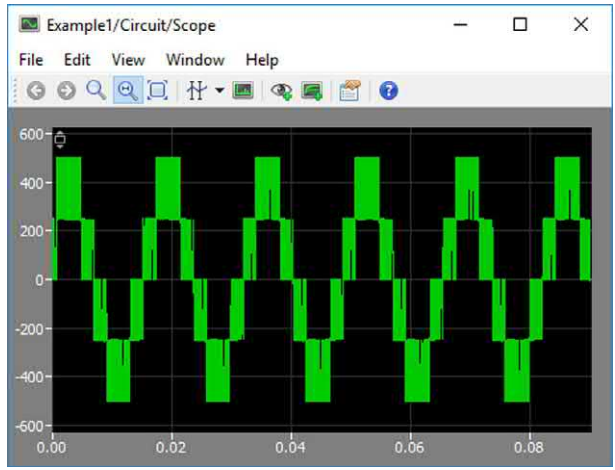


**FIG. 4.43** Line-line voltage of multilevel inverter.

## 4.4 Sending/receiving signals to/from Simulink environment

You can send/receive the signals to/from Simulink environment easily with the aid of Signal Outport and Signal Inport blocks, respectively. The process of sending and receiving a signal is shown with two examples.

Assume that we want to send the line-line voltage to Simulink environment. In order to do this, add a Signal Outport block (Fig. 4.44) to the schematic as shown in Fig. 4.45. The Signal Outport block can be found in the System section of Library Browser (Fig. 4.46).

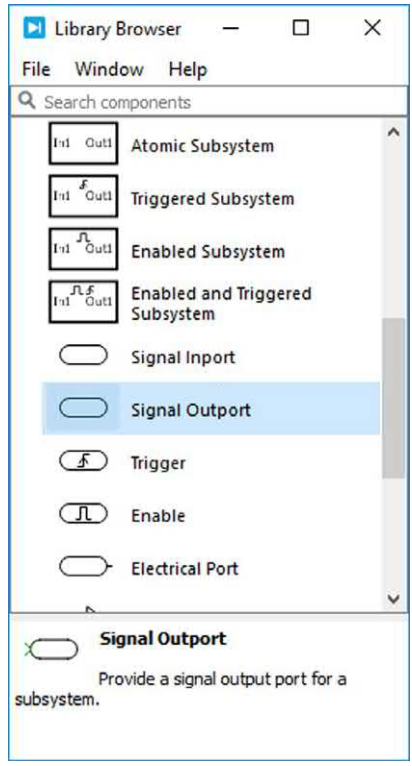


**FIG. 4.44** Signal Outport block.

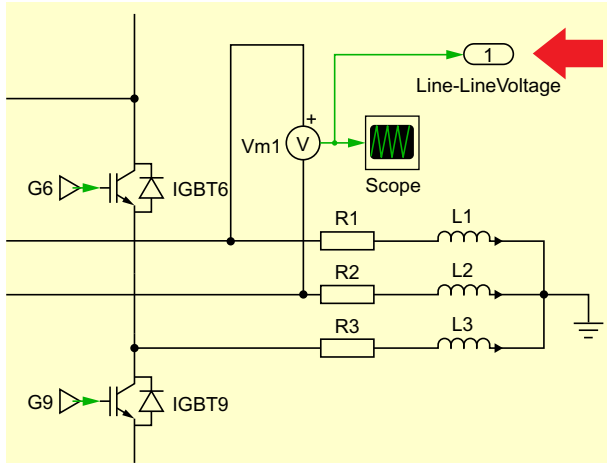


**FIG. 4.45** Addition of a Signal Outport block to the schematic. The default name of Signal Outport block is Out1. Double click the default name in order to change it to Line-LineVoltage.

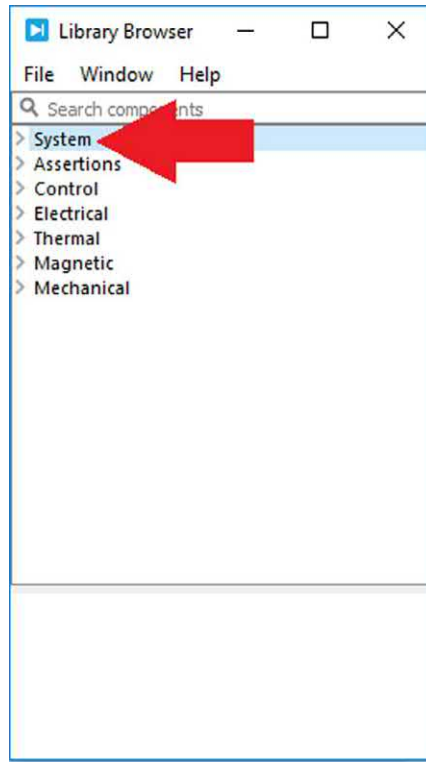


**FIG. 4.46** The system section of Library Browser.

After the Signal Outport block is added to the schematic, an output port is added to the Circuit block in the Simulink environment (Fig. 4.47). You can connect the output port to oscilloscope or To Workspace blocks (Fig. 4.48).

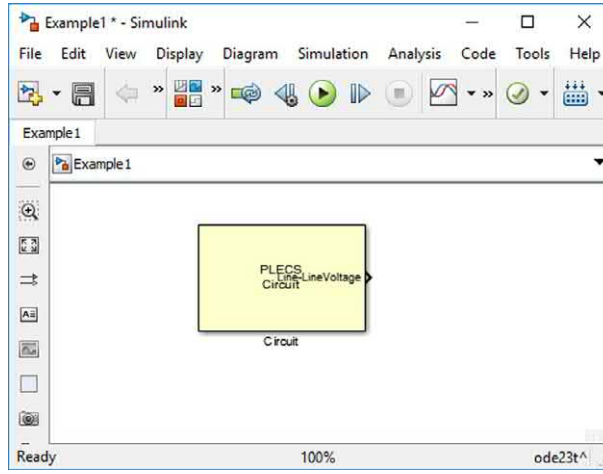


**FIG. 4.47** An output is added to the PLECS Circuit block.

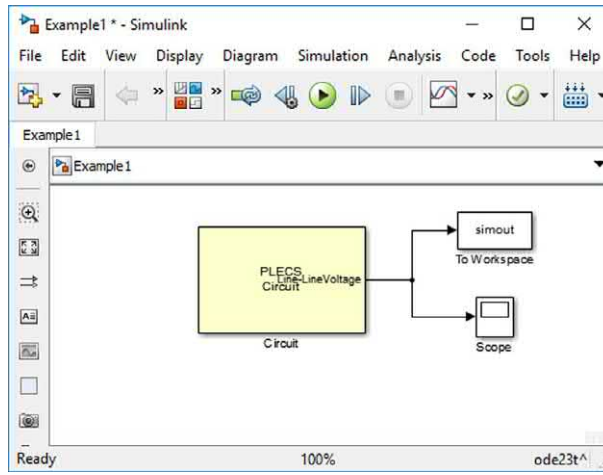


**FIG. 4.48** Connecting the output port to other blocks.

The schematic inside the Circuit block can receive signals from the Simulink environment as well. For instance, assume we want to set the value of input DC source form Simulink environment. The independent DC source in the input of inverter is replaced with a controlled voltage source (Fig. 4.49). The controlled voltage source can be found in the Sources section of Library Browser window (Fig. 4.50).

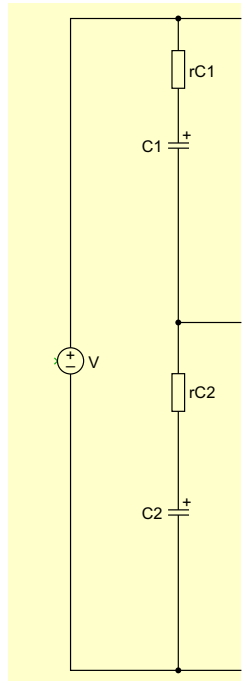


**FIG. 4.49** Addition of a controlled voltage source block to the schematic.

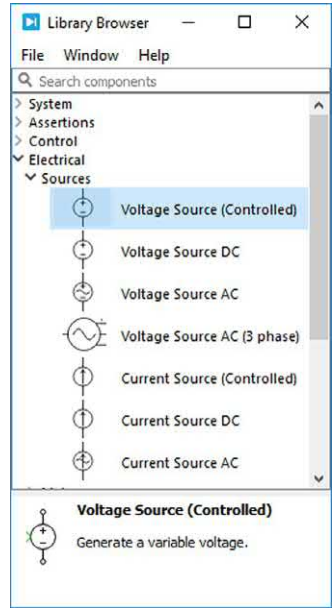


**FIG. 4.50** Voltage Source (Controlled) block can be found in the Sources section of Library Browser.

The input port of the placed controlled voltage source is connected to a Signal Inport block (Fig. 4.51). The Signal Inport block (Fig. 4.52) can be found in the System section of Library Browser window (Fig. 4.53).

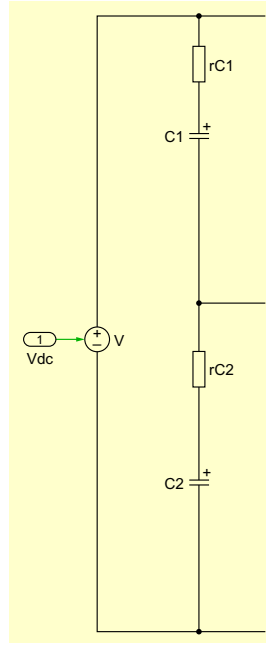


**FIG. 4.51** Addition of a Signal Inport block to the schematic.

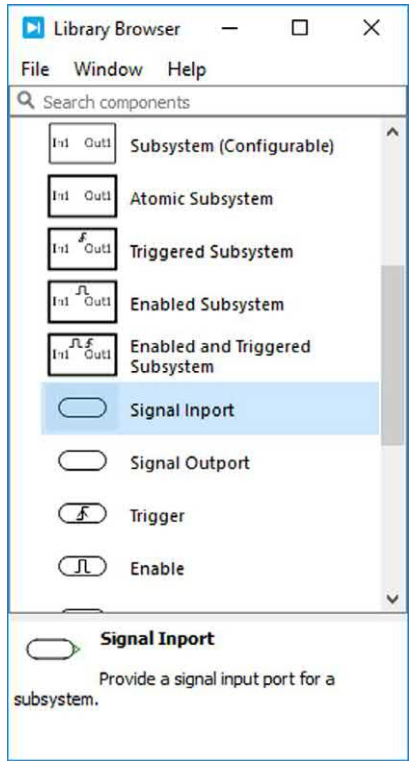


**FIG. 4.52** The Signal Inport block.

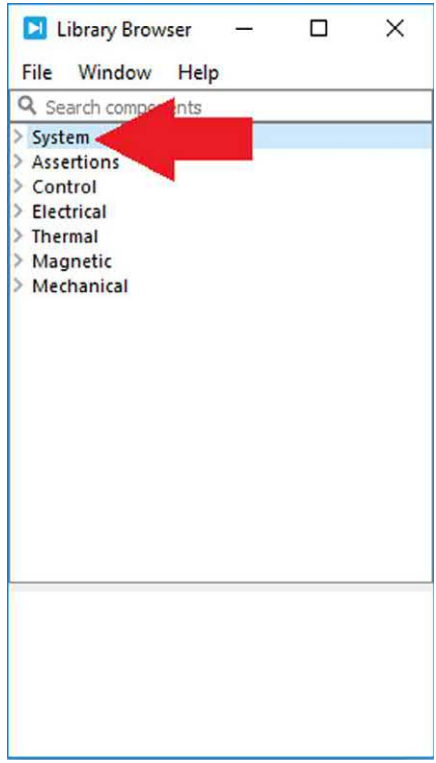


**FIG. 4.53** The System section of Library Browser.

After you add the Signal Inport block to the schematic, an input port is added to the Circuit block inside the Simulink environment (Fig. 4.54).

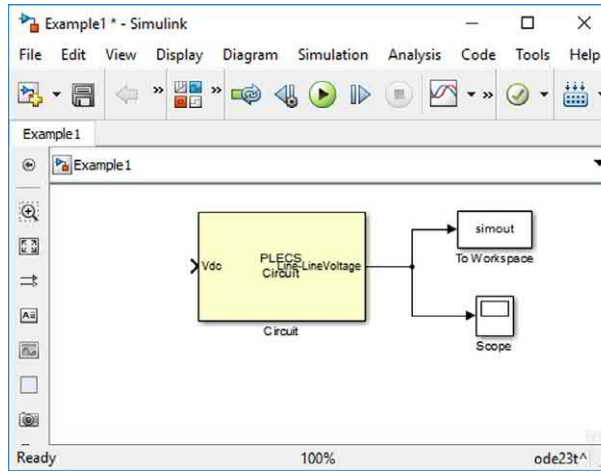


**FIG. 4.54** An input port is added to the PLECS Circuit block.

The input port can be connected to a Constant block to set the value of input DC voltage (Fig. 4.55).

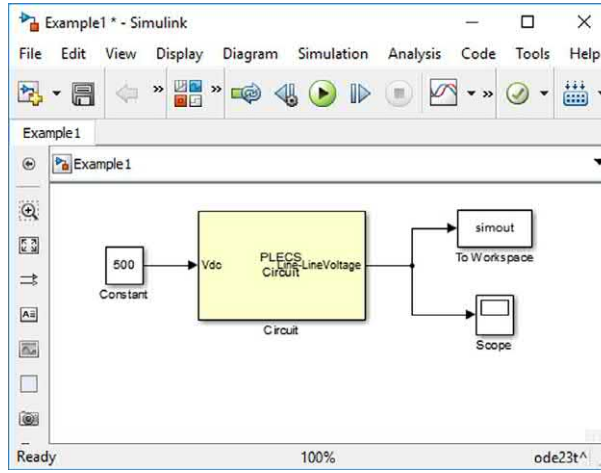


**FIG. 4.55** The input port is connected to a constant block.

## 4.5 Simulation of a cascaded inverter

A single-phase inverter is shown in Fig. 4.56.

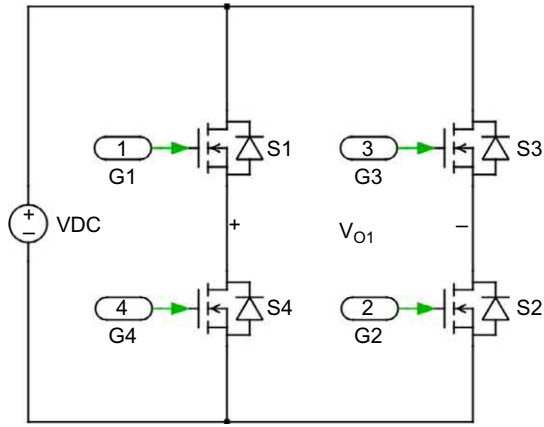


**FIG. 4.56** Single-phase inverter circuit.

This topology can produce three different output voltages ($V_{O1}$). The output voltage can be -VDC, 0, +VDC. When switches S3 and S4 are closed, the output voltage is –VDC. When switches S1 and S2 are closed, the output voltage is +VDC. When S1 and S3 are closed or S2 and S4 are closed, the output voltage will be 0 volt. In order to obtain the output waveform shown in part (a) of Fig. 4.57, the switching pattern shown in part (b) of Fig. 4.57 must be applied to the inverter.

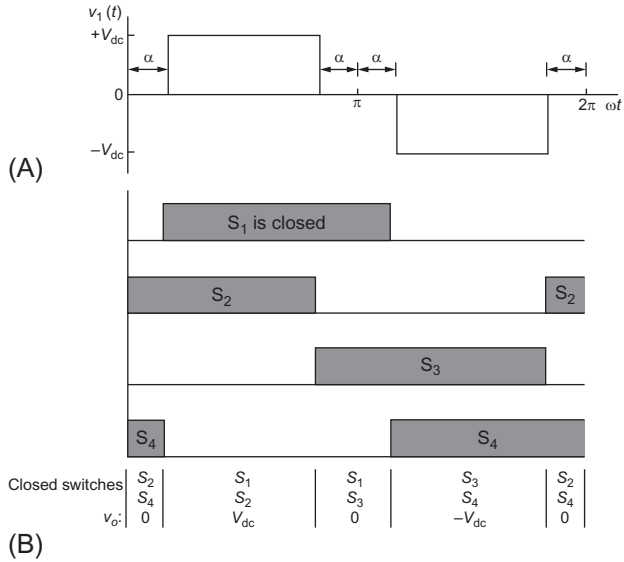


**FIG. 4.57** (A) Output voltage, (B) Required switching pattern to produce waveform shown in part (A).

The building block shown in Fig. 4.56 can be used to make a larger inverter. Circuit shown in Fig. 4.58 uses cascaded connection of two single-phase inverters. This circuit can produces -2VDC, -VDC, 0, +VDC, and +2VDC in its outputs. Increasing the levels of output voltage decreases the Total Harmonic Distortion (THD) of output voltage.

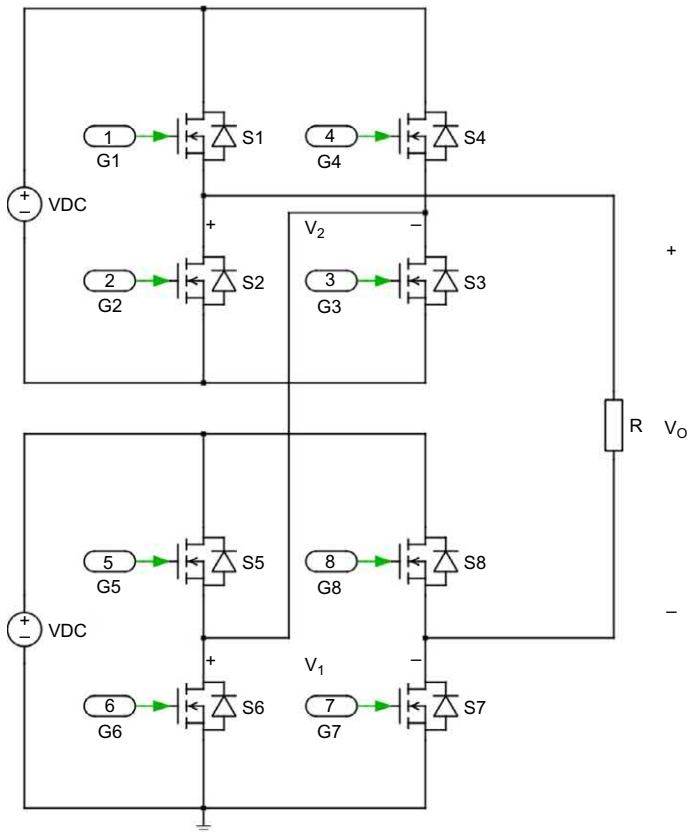


**FIG. 4.58** Cascade connection of two single-phase inverter. Note that $v_O = v_1 + v_2$.

Fig. 4.59 shows the output voltage of circuit shown in Fig. 4.58 and the required switching pattern.

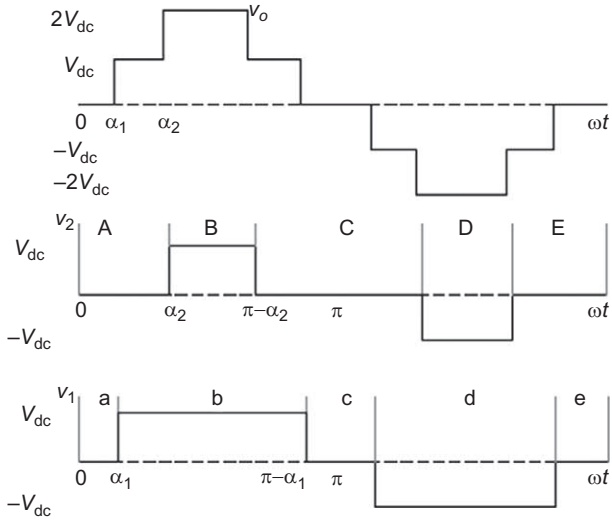


**FIG. 4.59** Voltage waveforms of cascaded inverter (Fig. 4.58). Note that $v_O = v_1 + v_2$.

Tables 4.1 and 4.2 show the status of switches in order to produce the output voltage shown in Fig. 4.59. 1 shows a closed switch, i.e., short circuit, and 0 shows the opened switch, i.e., open circuit.

**TABLE 4.1** Control signals for upper inverter switches (see Figs. 4.58 and 4.59).

| Interval name | Description of interval | S1 status | S2 status | S3 status | S4 status |
|---|---|---|---|---|---|
| **A** | $0 < \omega t < \alpha_2$ | 1 | 0 | 0 | 1 |
| **B** | $\alpha_2 < \omega t < \pi - \alpha_2$ | 1 | 0 | 1 | 0 |
| **C** | $\pi - \alpha_2 < \omega t < \pi + \alpha_2$ | 1 | 0 | 0 | 1 |
| **D** | $\pi + \alpha_2 < \omega t < 2\pi - \alpha_2$ | 0 | 1 | 0 | 1 |
| **E** | $2\pi - \alpha_2 < \omega t < 2\pi$ | 1 | 0 | 0 | 1 |

**TABLE 4.2** Control signals for lower inverter switches (see Figs. 4.58 and 4.59).

| Interval name | Description of Interval | S5 status | S6 status | S7 status | S8 status |
|---|---|---|---|---|---|
| **a** | $0<\omega t<\alpha_1$ | 1 | 0 | 0 | 1 |
| **b** | $\alpha_1<\omega t<\pi-\alpha_1$ | 1 | 0 | 1 | 0 |
| **c** | $\pi-\alpha_1<\omega t<\pi+\alpha_1$ | 1 | 0 | 0 | 1 |
| **d** | $\pi+\alpha_1<\omega t<2\pi-\alpha_1$ | 0 | 1 | 0 | 1 |
| **e** | $2\pi-\alpha_1<\omega t<2\pi$ | 1 | 0 | 0 | 1 |

We want to simulate the circuit shown in Fig. 4.58 for $\alpha_1=20°$ and $\alpha_2=40°$. We use the Simulink model shown in Fig. 4.60.

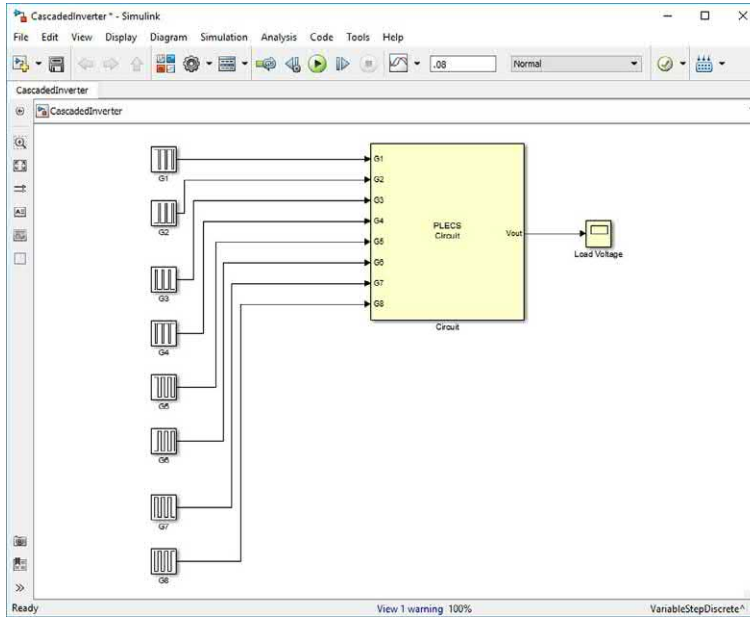


**FIG. 4.60** Simulink model of cascaded inverter.

The schematic of circuit inside the PLECS Circuit block is shown in Fig. 4.61.

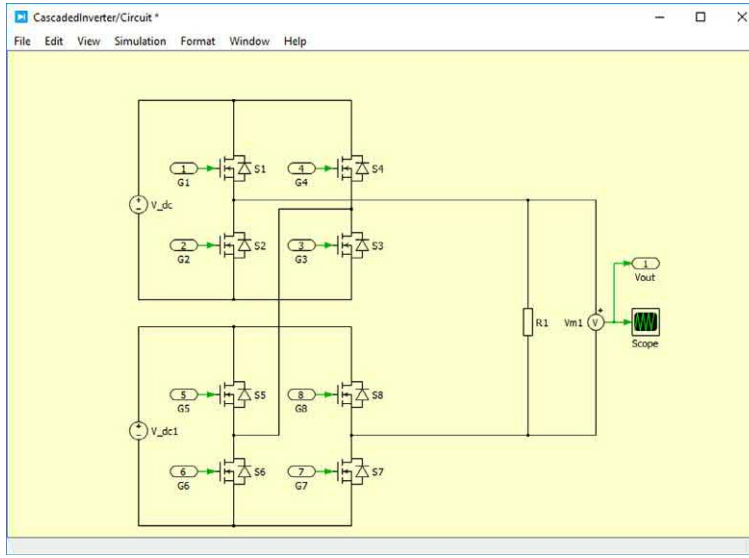


**FIG. 4.61** Schematic of cascaded inverter.

The settings of used components are shown in Figs. 4.62–4.64.

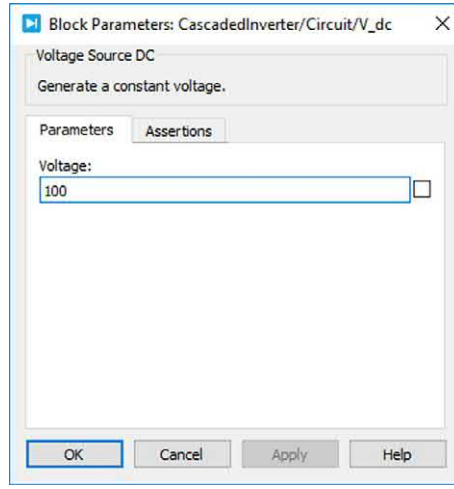


**FIG. 4.62** Setting of V_dc block. The V_dc1 block has the same settings.

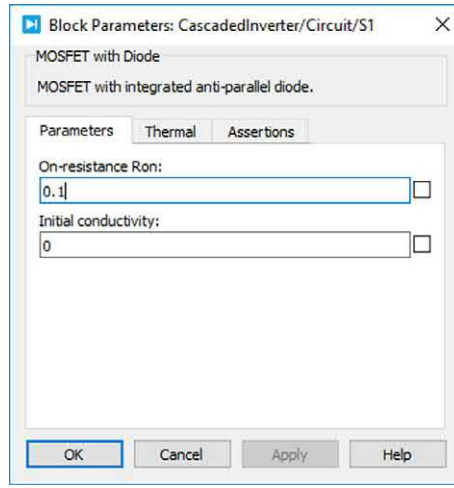


**FIG. 4.63** The MOSFET S1 settings. S2, S3, S4, …, S8 have the same settings.

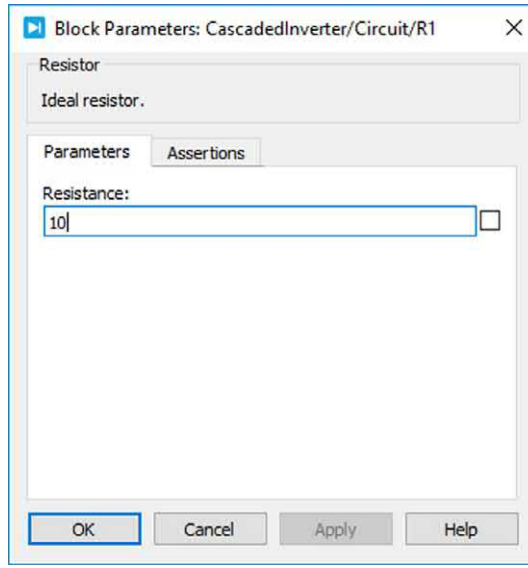


**FIG. 4.64** Resistor R1 settings.

We use the Repeating Sequence block (Fig. 4.65) to produce the required gate signals. The MOSFET will be closed once we send 1 to its gate and will be opened once we send 0 to its gate.

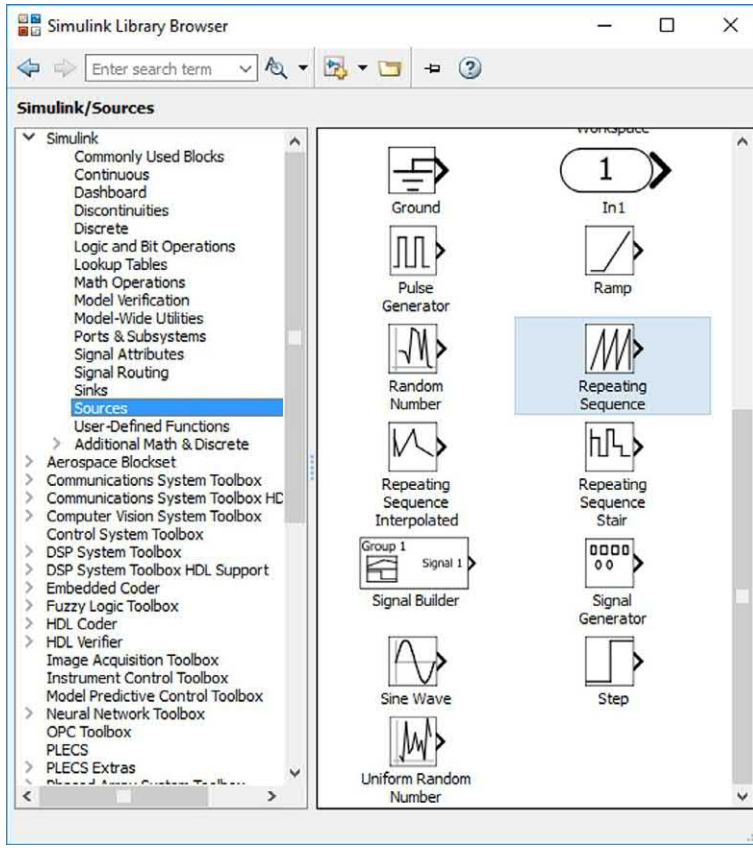


**FIG. 4.65** Repeating Sequence block.

Assume that you want to produce the waveform shown in Fig. 4.66 with the aid of Repeating Sequence block. The given graph is given in terms of angles. We need to know the switching times when working with the Repeating Sequence block.

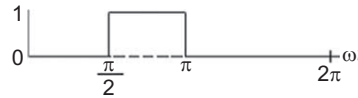


**FIG. 4.66** Sample waveform. The vertical axis is angle in radyan.

We must translate the $\omega t$ axes from angles into time. We must know the period of given waveform to do the translation. Assume that the waveform shown in Fig. 4.66 has the frequency of 1 kHz (period equals to $\frac{1}{1000} = 1\,\text{ms}$).

The switching time will be $\frac{\frac{\pi}{2}}{2\pi} \times 1\,\text{ms} = 0.25\,\text{ms}$ and $\frac{\pi}{2\pi} \times 1\,\text{ms} = 0.5\,\text{ms}$. Fig. 4.67 shows the time domain equivalent of Fig. 4.66.

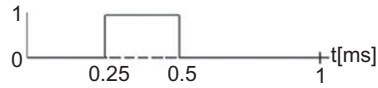


**FIG. 4.67** Time domain equivalent of waveform shown in Fig. 4.66. The vertical axis is angle in seconds.

According to Fig. 4.67, the signal is 0 for $0 < t < 0.25\,\text{ms}$, 1 for $0.25\,\text{ms} < t < 0.5\,\text{ms}$, and 0 for $0.5\,\text{ms} < t < 1\,\text{ms}$. Assume the transition from 0 to 1 or 1 to 0 takes 0.01 ms. Then, the signal is 0 for [0,0.25 ms − 0.01 ms], the transition interval is [0.25 ms − 0.01 ms, 0.25 ms − 0.01 ms + 0.01 ms]. After the transition, the signal will be at 1 and remain there up to next transition, i.e., the signal is 1 for [0.25 ms, 0.5 ms − 0.01 ms]. There is another transition from 1 to 0 at [0.5 ms − 0.01 ms, 0.5 ms]. After that transition the signal will stay at 0, i.e., the signal is 0 for [0.5 ms, 1 ms].

Fig. 4.68 shows the required setting for Repeating Sequence block in order to produce the aforementioned signal.

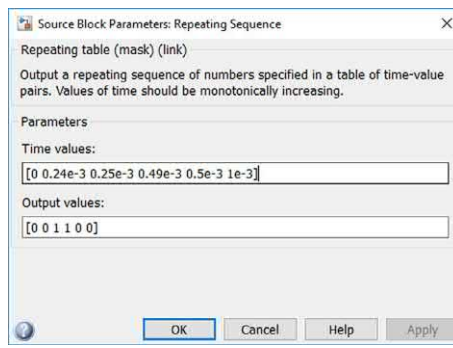


**FIG. 4.68** Required setting to produce the waveform shown in Fig. 4.67. It is assumed that transitions take 0.01s.

The output signal of Repeating Sequence block shown in Fig. 4.68 is shown in Fig. 4.69.

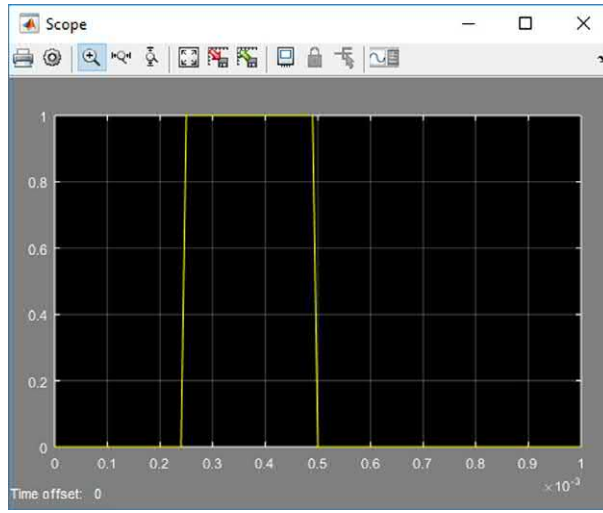


**FIG. 4.69** Output of Repeating Sequence block with the setting shown in Fig. 4.68. Repeating Sequence block produces a periodic output. Only one period is shown in this figure.

The required setting for blocks G1, G2, G3, …, G8 is shown in Figs. 4.70–4.77. The setting for this block is done with respect to Table 4.1 and 4.2.

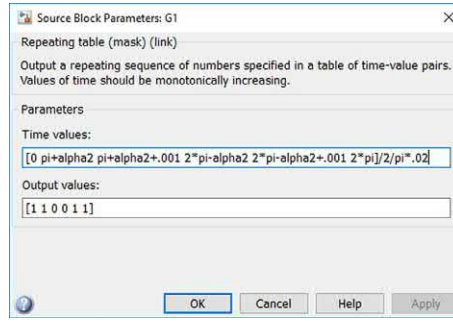


**FIG. 4.70** Settings of block G1. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

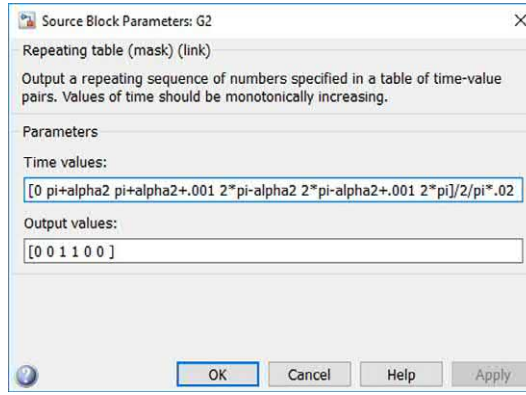


**FIG. 4.71** Settings of block G2. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

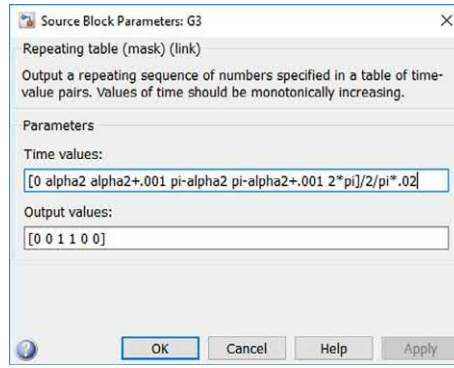


**FIG. 4.72** Settings of block G3. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

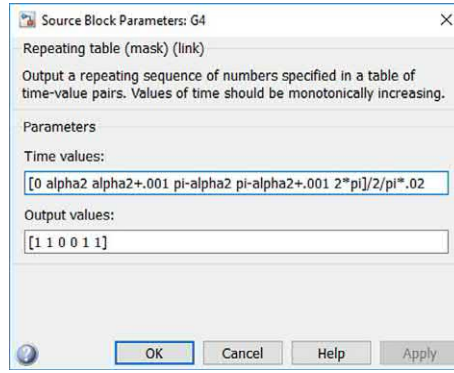


**FIG. 4.73** Settings of block G4. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

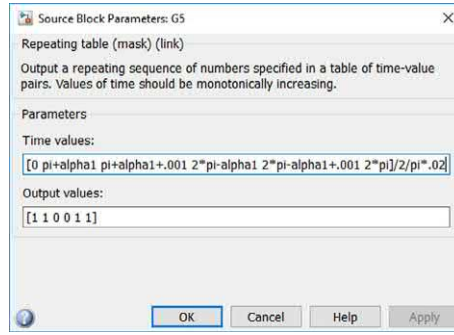


**FIG. 4.74** Settings of block G5. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

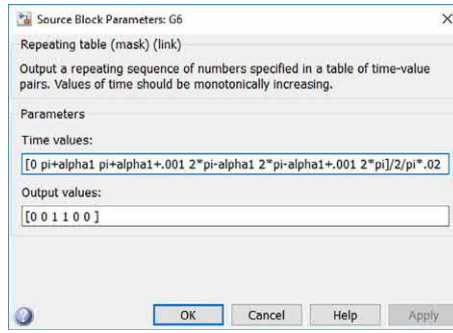


**FIG. 4.75** Settings of block G6. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

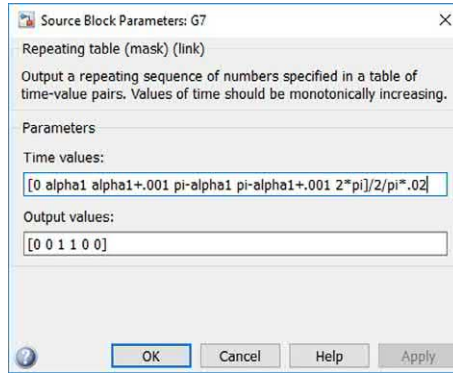


**FIG. 4.76** Settings of block G7. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

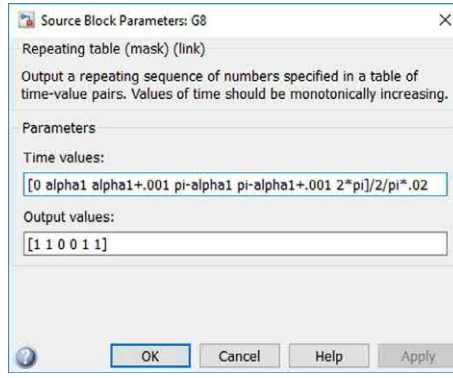


**FIG. 4.77** Settings of block G8. It is assumed that transitions takes at $\frac{0.001}{2\pi} \times 0.02 = 3.2\,\mu s$.

Click the gear icon in the Simulink environment and set the solver and stop time as shown in Fig. 4.78.

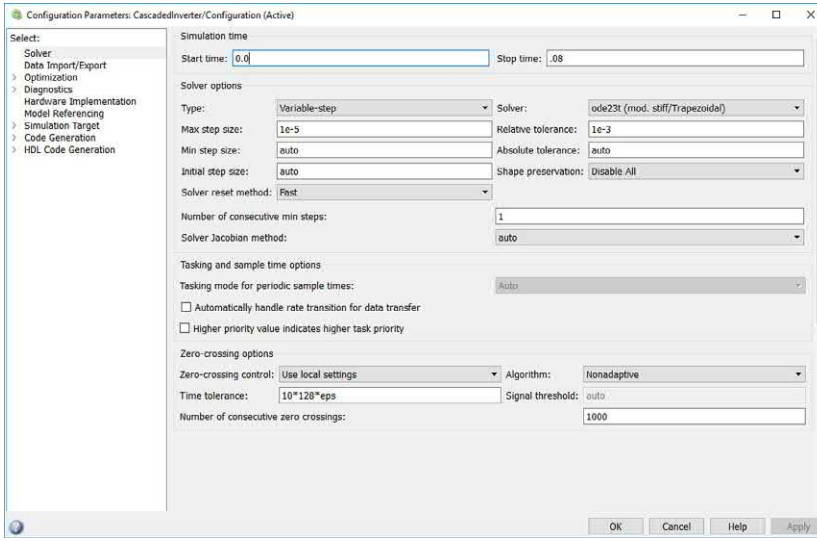


**FIG. 4.78** Configuration parameters window.

Don't forget to initialize the values of $\alpha_1$ and $\alpha_2$ before running the simulation (Fig. 4.79).

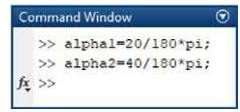


**FIG. 4.79** Initialization of variables `alpha1` and `alpha2` in radyan.

Run the simulation. The simulation result is shown in Fig. 4.80.

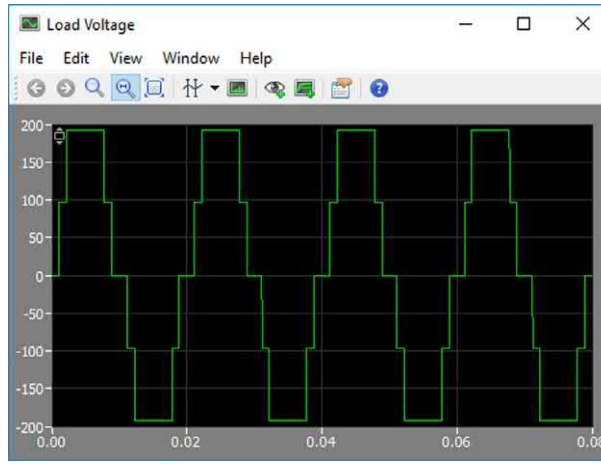


**FIG. 4.80** Simulation result (load voltage).

There is no limitation on the number of cascaded stages. For instance, the inverter shown in Fig. 4.81 is composed of five stages. The produced output voltage is shown in Fig. 4.82. Note that cascaded inverters require separate DC sources, which is one of their disadvantages.

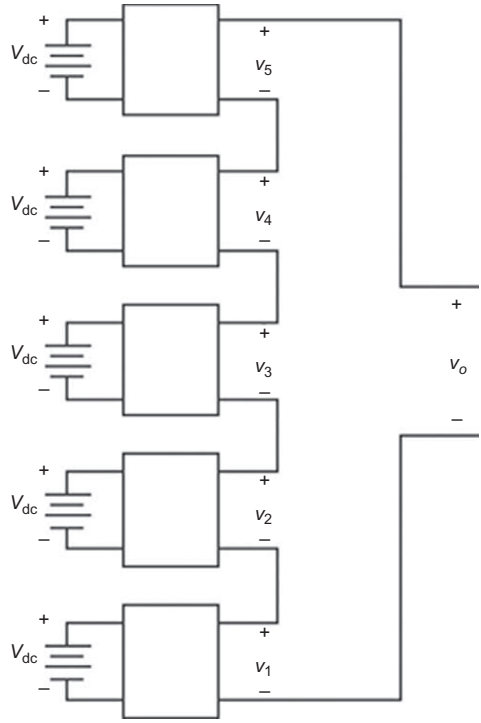


**FIG. 4.81** A cascaded inverter composed of five stages.

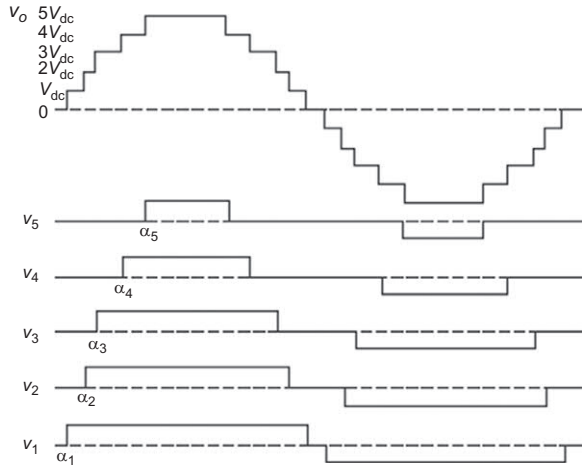


**FIG. 4.82** Output voltage of inverter shown in Fig. 4.81.

## 4.6 Measurement with the probe block

You can use the Probe block to measure the desired quantities. Consider the simple RLC circuit shown in Fig. 4.83.

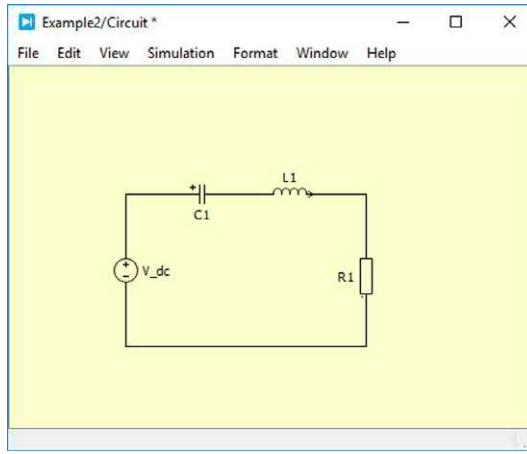


**FIG. 4.83** A simple RLC circuit. V_dc = 100 V, C1 = 100 μf, L1 = 1 mH, and R = 1 Ω.

Add a PLECS Probe block to Simulink simulation (Fig. 4.84). The PLECS Probe block can be found in the PLECS section of Simulink Library Browser (Fig. 4.85)

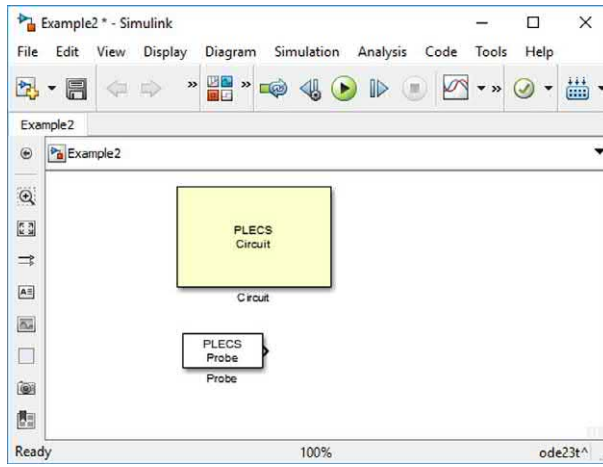


**FIG. 4.84** Addition of a PLECS Probe block to the schematic.

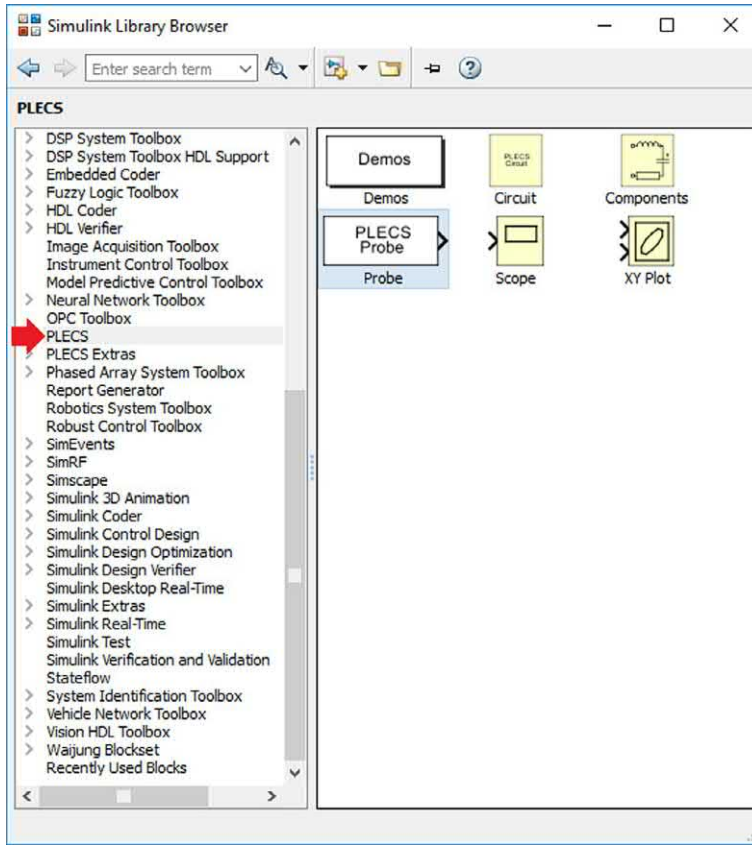


**FIG. 4.85** PLECS Probe block can be found in the PLECS section of Simulink Library Browser.

Open the PLECS Probe block by double clicking on it. Open the Circuit block as well (Fig. 4.86).

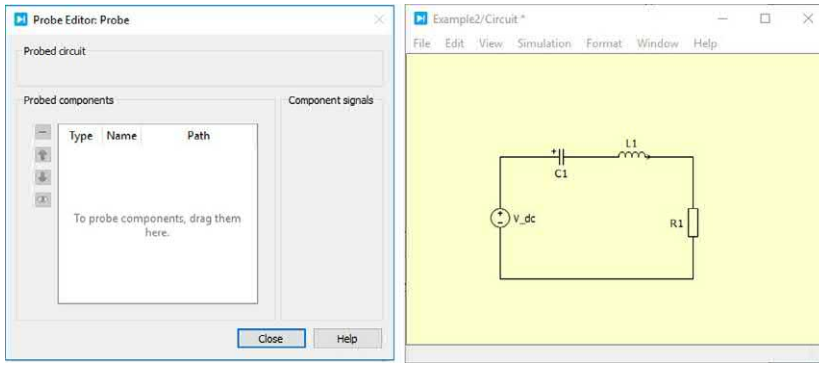


**FIG. 4.86** The opened Probe block and drawn schematic.

We want to see the instantaneous dissipated power of resistor. The power can be calculated by product of current through the resistor and voltage across the resistor. Drag the resistor from the schematic and drop it in the white area of Probed components (Fig. 4.87).

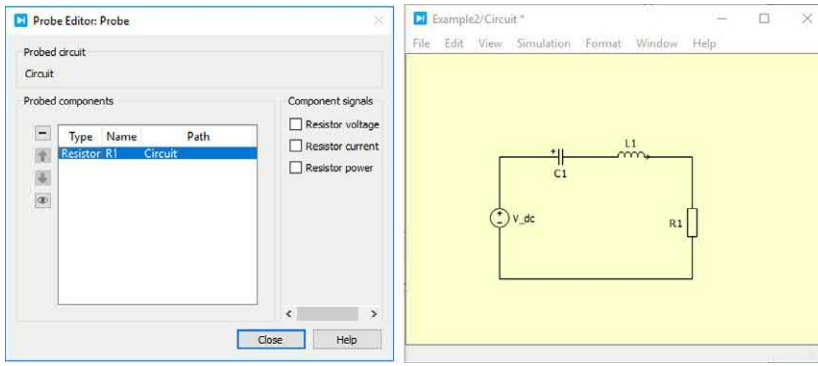


**FIG. 4.87** Drag and drop the resistor R1 onto the Probed components box of opened Probe block.

Select the desired quantities to be measured from the Component signals section of the window. In this case we need the voltage and current of resistor, so Resistor voltage and Resistor current of boxes are checked (Fig. 4.88).

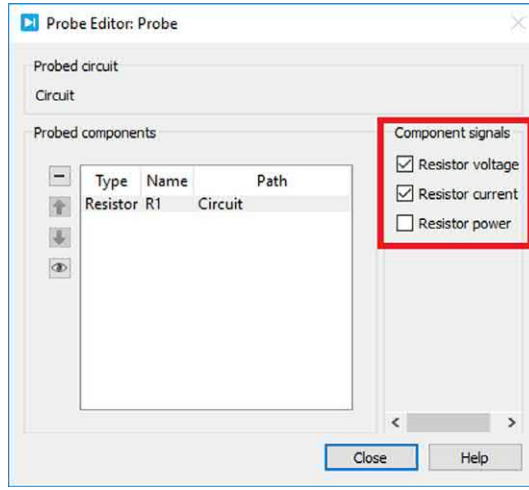


**FIG. 4.88** The measurable signals.

There is a simple dot behind the resistor symbol in the schematic (Fig. 4.89). The PLECS Probe assumes the current, which enters the dot as positive. The PLECS Probe measures the resistor voltage with respect to undotted pin, i.e., the PLECS Probe measures $v_{dotted\ pin} - v_{undotted\ pin}$.

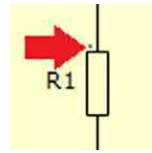


**FIG. 4.89** The dot behind the resistor icon.

Add a demultiplexer block to output of PLECS Probe block. The multiplexer block separates the voltage and current. Use a multiply block to calculate the power (Fig. 4.90).

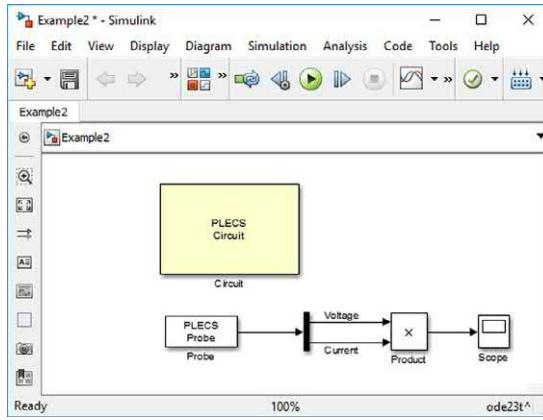


**FIG. 4.90** Completed Simulink model.

Simulation result is shown in Fig. 4.91.

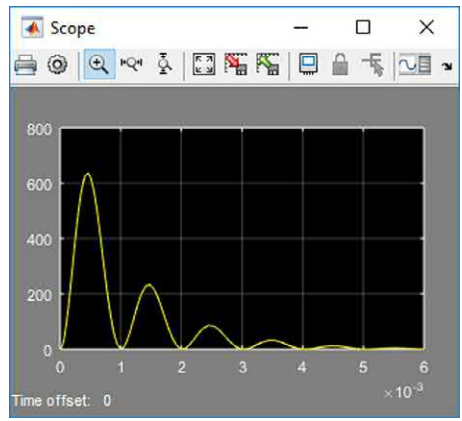


**FIG. 4.91** Simulation result.

## 4.7 Extraction of frequency response of DC-DC converters

You can obtain the small signal-frequency response of DC-DC converters with the aid of Impulse Response Analysis block. We show how to extract the frequency response of control-to-output transfer function in this section.

Assume a buck converter like the one shown in Fig. 4.92. Values of components can be read from the schematic.

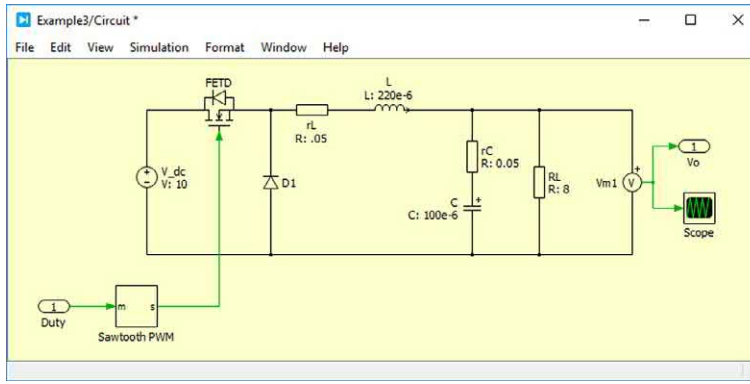


**FIG. 4.92** Schematic of the buck converter. The 5-V output voltage is needed.

The settings for diode, MOSFET, and Sawtooth PWM generation block are shown in Figs. 4.93–4.95.

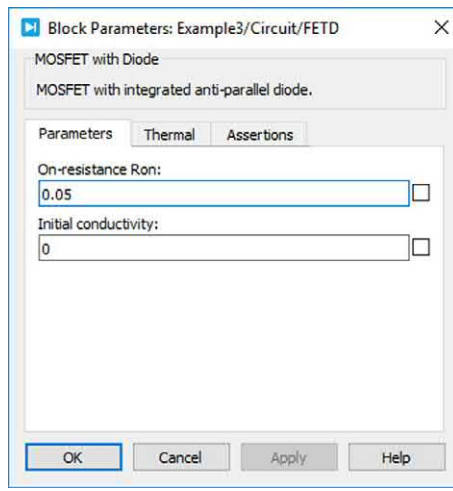


**FIG. 4.93** Settings of MOSFET block.

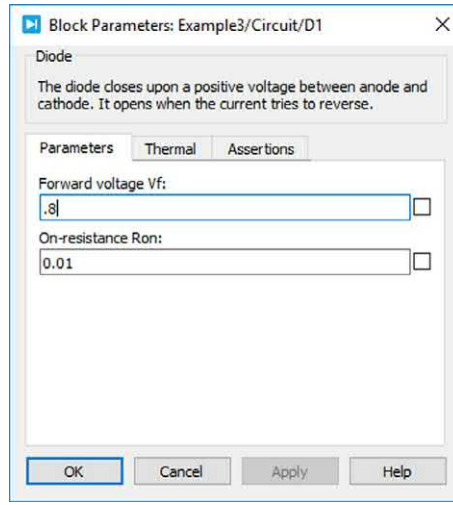


**FIG. 4.94** Settings of diode block.

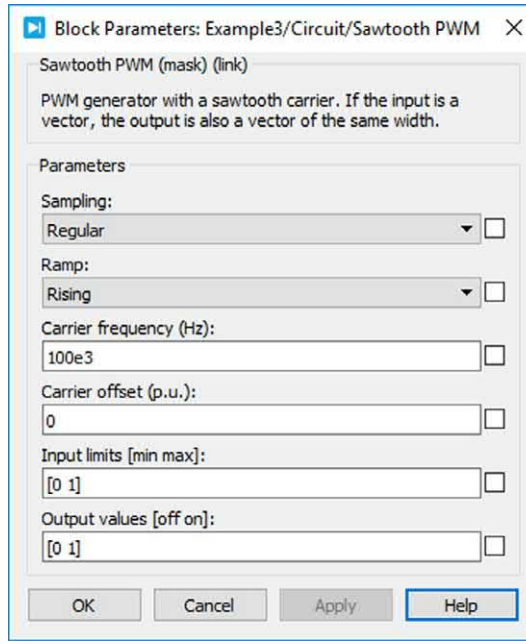


**FIG. 4.95** Sawtooth PWM block settings.

When you need to see the details behind a block, you can double click on the block and click the Help button. For instance, if you click the Help button in Fig. 4.96, the window shown in Fig. 4.97 will appear. This window shows the detail of Sawtooth PWM generation block.

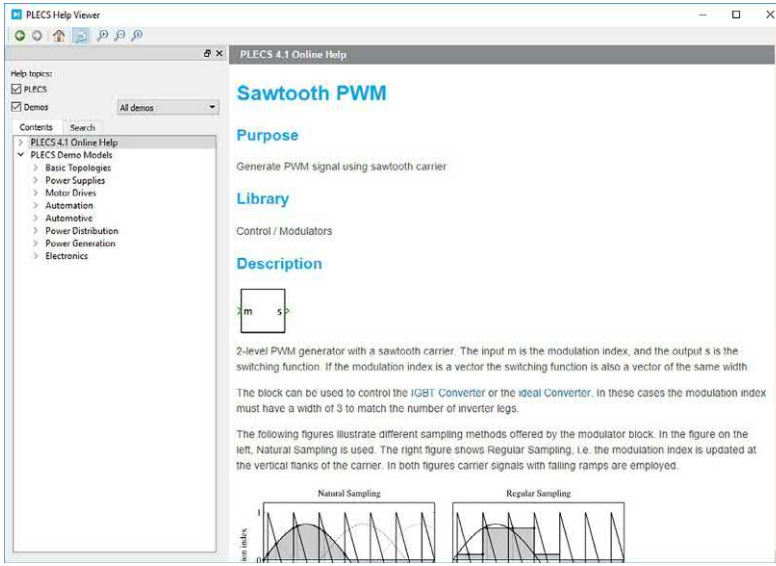


**FIG. 4.96** Help of Sawtooth PWM block.

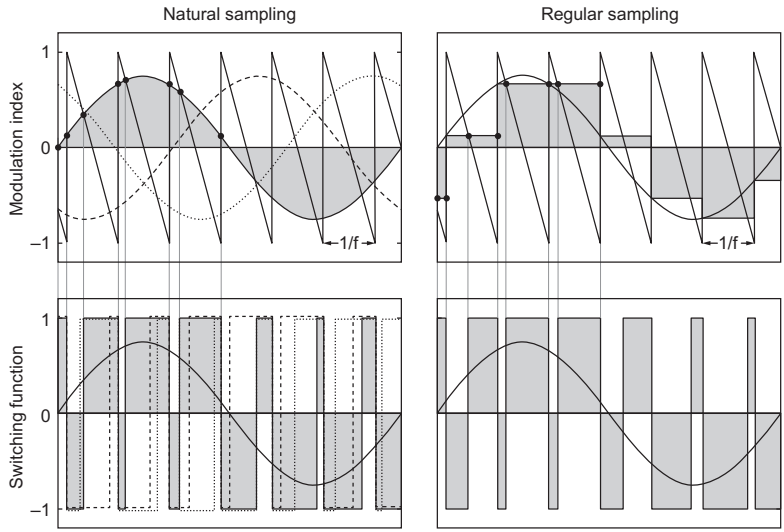


**FIG. 4.97** Comparison between Natural Sampling and Regular Sampling. The modulating signal is shown with a sine wave. The carrier is the saw tooth signal.

Sampling (see Fig. 4.95) can be Natural or Regular. As shown in Fig. 4.97, in regular sampling, the modulating signal is sampled at the beginning of switching interval and doesn't change within one period. In natural sampling, the modulating signal is not sampled. The natural sampling is a good option if you plan to use an analog modulator. If you want to use a digital modulator, use the Regular Sampling.

Add the Impulse Response Analysis block to the Simulink file as shown in Fig. 4.98. The Impulse Response Analysis block can be found in the Analysis Tools section of the Simulink Library Browser (Fig. 4.99).

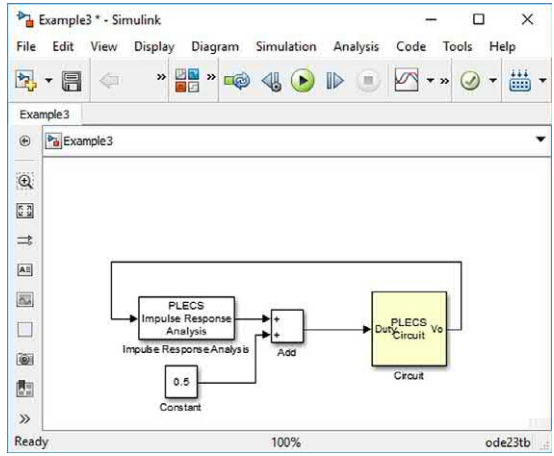


**FIG. 4.98** Completed simulation to extract the small signal control-to-output transfer function. The output of 5 V is obtainable with duty ratio of 0.5.

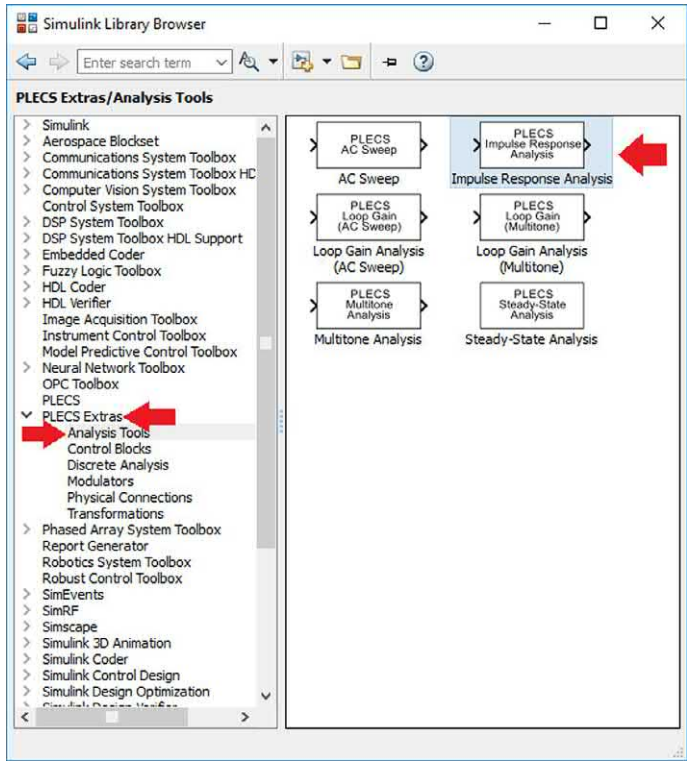


**FIG. 4.99** The Impulse Response Analysis block.

Double click the Impulse Response Analysis block placed in the Simulink environment. The window shown in Fig. 4.100 will appear.

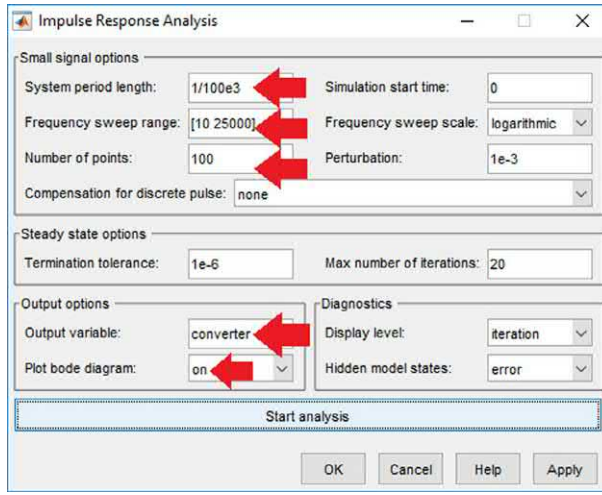


**FIG. 4.100** Impulse Response Analysis block settings.

Fill the System period length box with 1/f, where f is the switching frequency of converter. Enter the desired frequency range, i.e., frequency range of output graph, in the Frequency sweep range box. The Impulse Response Analysis produces a logarithmically spaced frequency vector according to the values entered to Frequency sweep range and Number of points boxes. The Number of points box is the length of produced frequency vector. For instance according to the values shown in Fig. 4.100, the produced frequency vector will have 100 members, the minimum member is 10, and the maximum member is 25000. The frequency vector values can be obtained with this MATLAB command: `logspace(log(10),log10(25e3),100)`. Increasing the value entered into the Number of points box will produce a smoother graph; however, the analysis takes more time to be done.

After the user presses the Start analysis button, the result shown in Fig. 4.101 will appear. Note that the unit of frequency is Hertz in this plot.

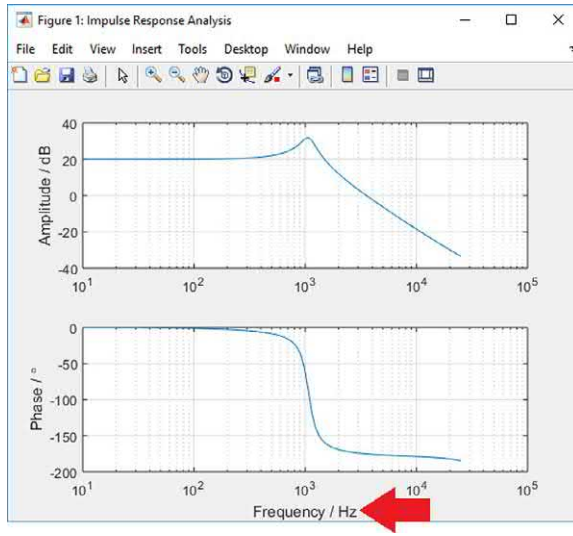


**FIG. 4.101** Result of analysis. The horizontal axis has the unit of Hertz.

Use the Data Cursor icon (Fig. 4.102) to read the values of different points of the graph. After you clicked the Data Cursor icon, click the point, which you want to read its value (Fig. 4.103). The value is shown in a box.

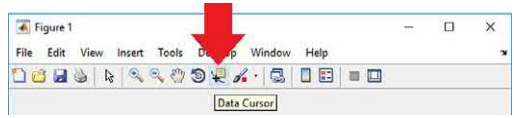


**FIG. 4.102** The Data Cursor icon.

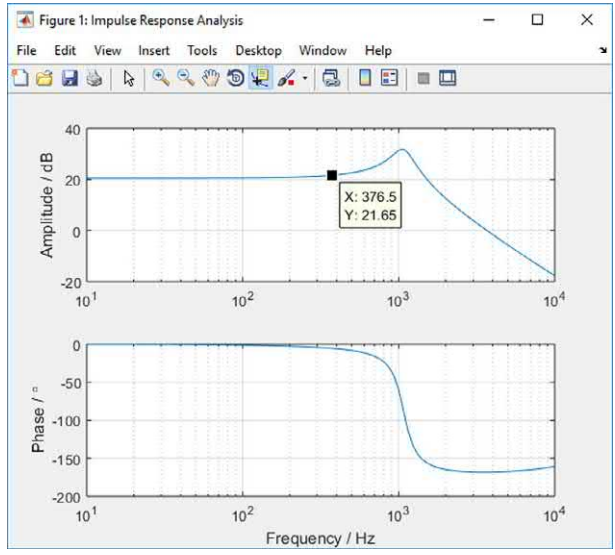


**FIG. 4.103** Addition of a datatip to the graph helps the user to read the values more easily.

You can move the datatip added to the graph. In order to make the movement smooth, right click on the data tip and select the Mouse Position (Fig. 4.104). If you want to remove the added datatip, right click on it and select the Delete Current Datatip.

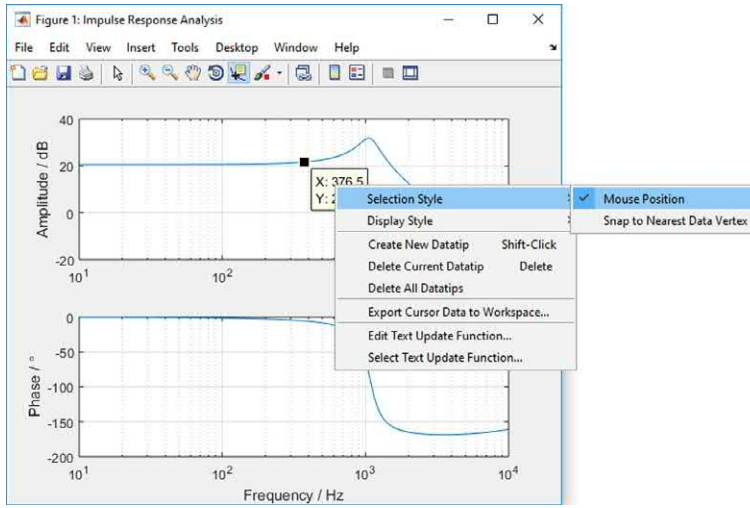


**FIG. 4.104** Select Mouse Position to move the added data tip more smoothly.

You can save the obtained graph as graphic file. In order to do this, click the Save As … (Fig. 4.105)

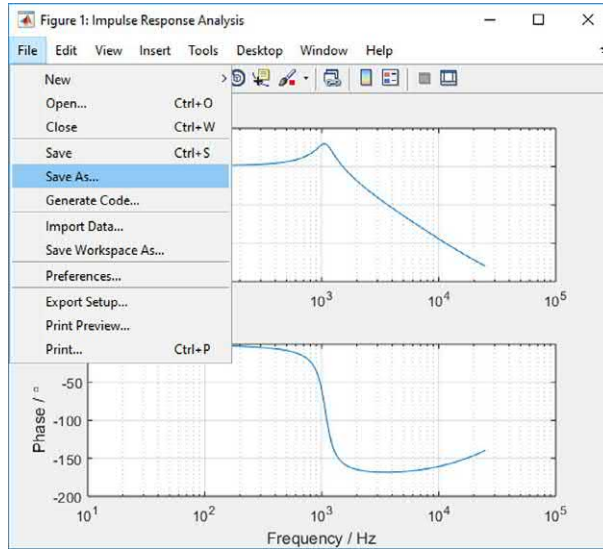


**FIG. 4.105** Use Save As… to export the obtained graph as a graphical file.

Set the desired path, name, and output file format in the appeared window (Fig. 4.106).

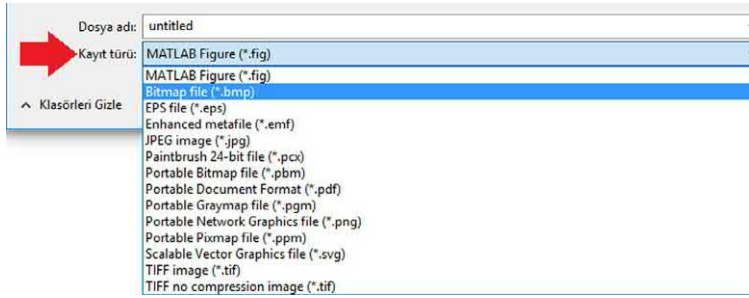


**FIG. 4.106** Selection of output file format.

If you notice to the Workspace, you will see that a new variable is added to it (Fig. 4.107). The variable name is the same as the one written in Output variable box (see Fig. 4.100).


**FIG. 4.107** After analysis is done, a new variable is added to the Workspace.

The variable `converter` has two fields: F and G. The field F keeps the frequency and G is the response of converter. F is real vector and G is a complex vector (Fig. 4.108).

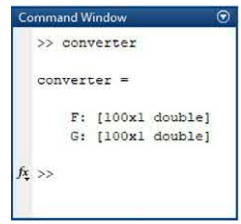


**FIG. 4.108** Fields of the variable `converter`.

For instance, according to Fig. 4.109, the value of 10th element of F and G is 18.7382 and $10.6736 - 0.0442i$, respectively.

```
Command Window
>> converter.F(10)

ans =

   18.7382

>> converter.G(10)

ans =

  10.6736 - 0.0442i

fx >>
```

**FIG. 4.109** Values of 10th elements of F and G. Note that $10.6736 - 0.0442i = 10.6737e^{-j\times 0.2372^\circ}$.

This means at 18.7382 Hz ($=18.7382\times 2\pi = 117.7356\,\frac{\text{Rad}}{\text{s}}$), value of magnitude plot is $20\times\log(10.6737) = 20.5663$ db and value of phase plot is $-0.2372^\circ$. You can add cursor to the obtained graph and check this calculation (Fig. 4.110).

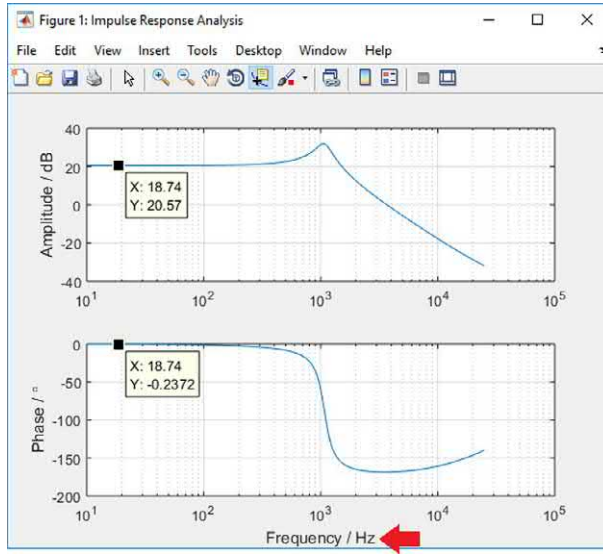


**FIG. 4.110** Magnitude and phase values at 18.74 Hz.

## 4.8 Fitting a transfer function to obtained graph

The result of previous analysis was graphical, i.e., the software didn't give us the equation of transfer function. You can use the System Identification Toolbox® to fit a transfer function to the obtained data.

In order to estimate a transfer function for the obtained data, the frequency response data model (frd object) of obtained data are formed (Fig. 4.111). Since the `converter.F` is in Hertz, it must be multiplied with $2\pi$ in order to obtain it in $\frac{\text{Rad}}{\text{s}}$.

```
Command Window
>> H=frd(converter.G,2*pi*converter.F);
fx >>
```

**FIG. 4.111** Formation of frd object.

You can draw the Bode diagram of frd model with the aid of `bode` command (Fig. 4.112). The result is shown in Fig. 4.113.

```
Command Window
>> H=frd(converter.G,2*pi*converter.F);
>> bode(H),grid on
>>
```

**FIG. 4.112** Drawing the frequency response of frd object H.

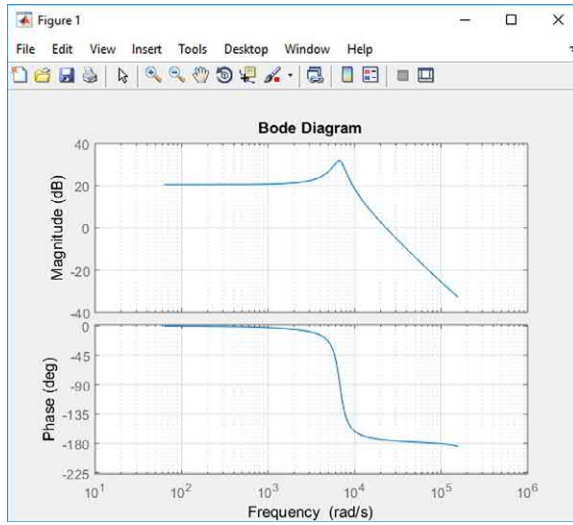


**FIG. 4.113** Frequency response of H. The vertical axis of graph has the unit of $\frac{\text{Rad}}{\text{s}}$.

As shown in Fig. 4.114, the graph starts from $62.8\,\frac{\text{Rad}}{\text{s}}$ to $1.57 \times 10^5\,\frac{\text{Rad}}{\text{s}}$ (10 Hz to 25 kHz).

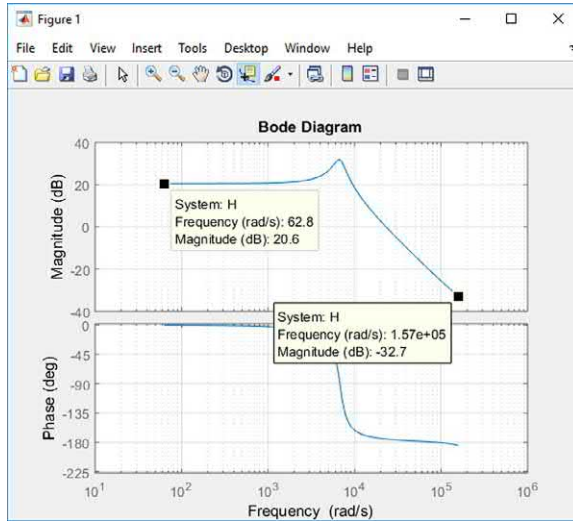


**FIG. 4.114** The frequency response graph of H starts from $62.8\,\frac{\text{Rad}}{\text{s}} = 10\,\text{Hz}$ and ends at $1.57 \times 10^5\,\frac{\text{Rad}}{\text{s}} = 25\,\text{kHz}$.

You can estimate a transfer function for the frd object H with the aid of `tfest` command. We want to find a second-order estimation since the buck converter contains two independent energy storage elements (a capacitor and an inductor). Result is shown in Fig. 4.115.


**FIG. 4.115** Estimation of a second-order controller to frd object H.

The Fit to estimation data (Fig. 4.116) shows the goodness of fit. Since it is near to 100%, the estimation overlaps the original frequency response very good.

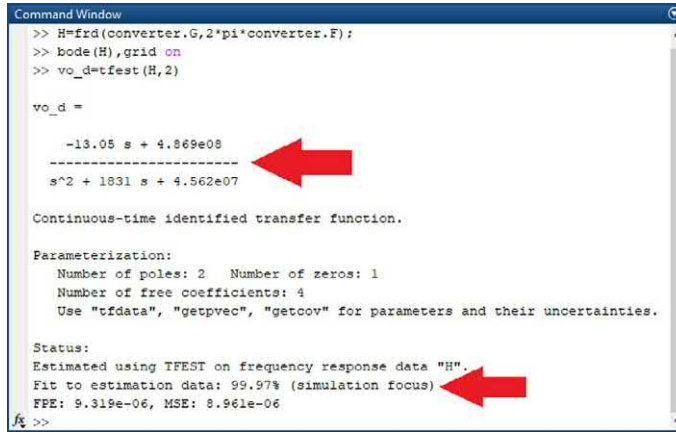


**FIG. 4.116** Estimated transfer function.

The code shown in Fig. 4.117 compares the frequency response of original system (i.e., the frequency response produced by PLECS) with the estimated one. Result is shown in Fig. 4.118.

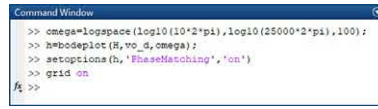


**FIG. 4.117** Comparison of the frequency response of estimated transfer function and the original system.

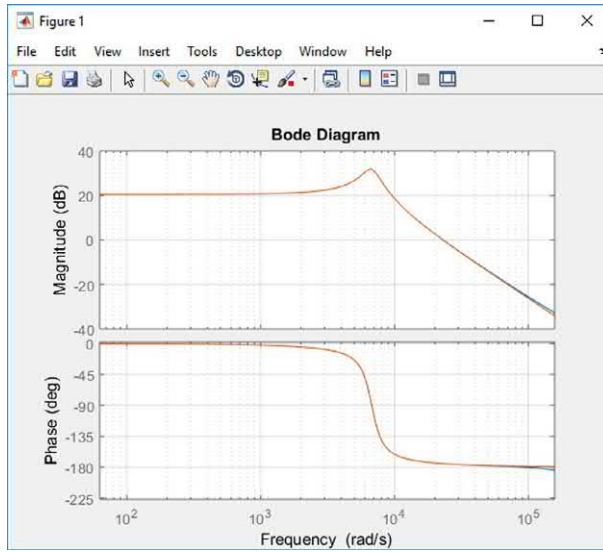


**FIG. 4.118** Comparison results. The two curves overlap almost everywhere.

## 4.9 Designing a controller

We design a PI controller for the estimated transfer function. MATLAB® has a powerful command (`pidTuner`) to design PID controllers. Enter the command shown in Fig. 4.119 to start the design process.

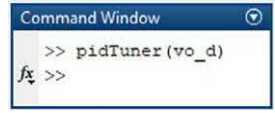


**FIG. 4.119** Running the pidTuner application of MATLAB.

After you entered the `pidTuner(vo_d)`command, the window shown in Fig. 4.120 will appear. Use the Type to select the desired controller type (i.e., P, I, PI, I, PID). Move the sliders until you obtain the desired response. The controller parameters are shown in the right button section of window.

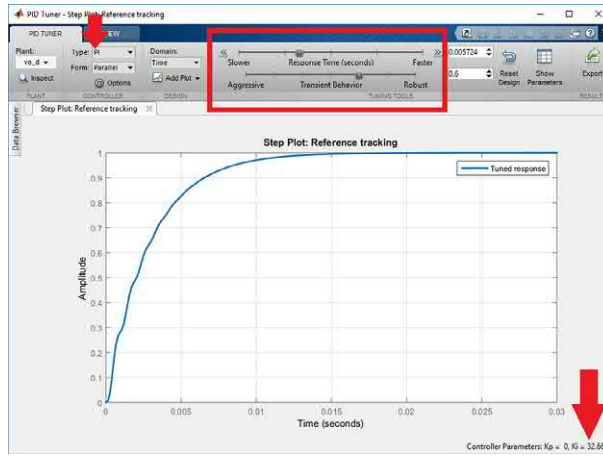


**FIG. 4.120** The PID Tuner window. Change the sliders until you obtain the desired result.

You can tune the controller with the frequency domain criteria (i.e., phase margin and gain margin) as well. In order to do this, select the Frequency (Fig. 4.121).

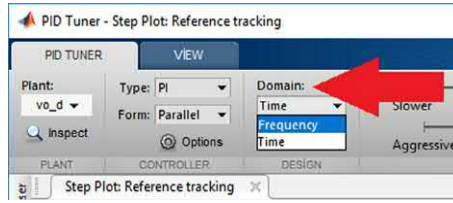


**FIG. 4.121** The tuning can be done in the frequency domain.

The response shown in Fig. 4.120 seems good. It is not oscillatory and the settling time is 15 ms. We want to simulate the buck converter with this controller. In order to simulate the closed-loop buck converter, the simulation diagram shown is changed like Fig. 4.122.

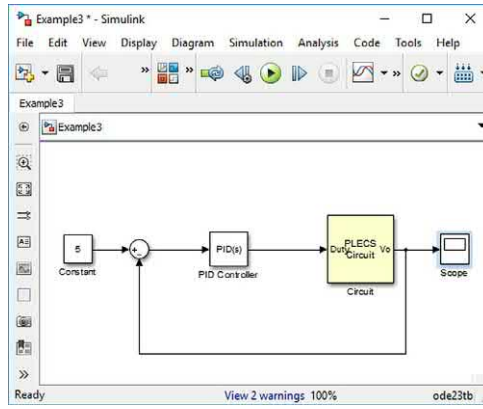


**FIG. 4.122** The completed Simulink model. Kp = 0, Ki = 32.66, Kd = 0 for PID Controller block.

Setting of PID controller block is shown in Fig. 4.123. The simulation result is shown in Fig. 4.124. As shown, the system tracks the command with zero steady-state error.

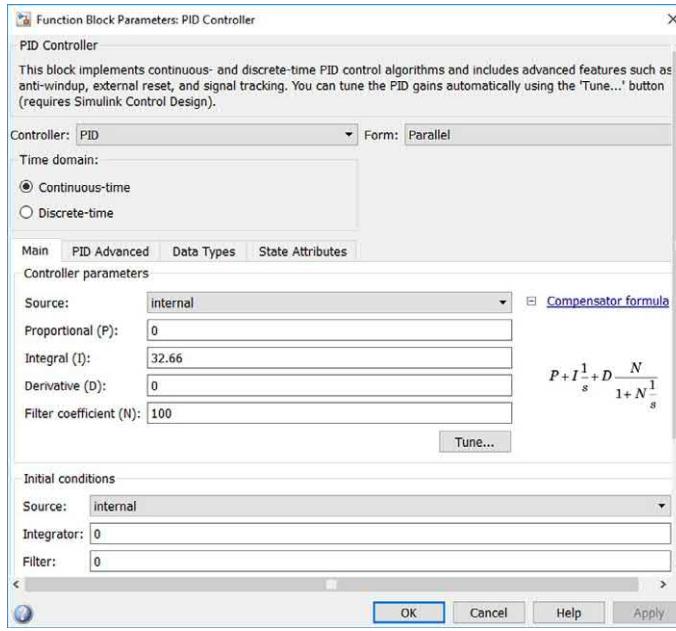


**FIG. 4.123** PID controller block settings.

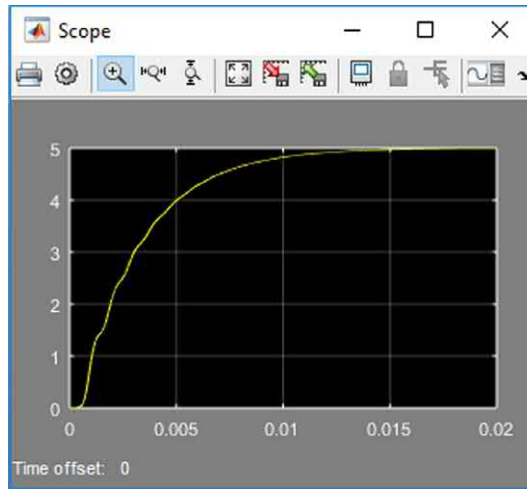


**FIG. 4.124** Simulation result.

You can study the effect of change in reference command with the simulation diagram shown in Fig. 4.125. The value of reference command in this simulation changes from 5 V to 8 V at 20 ms. The step block settings is shown in Fig. 4.126. The simulation result is shown in Fig. 4.127.

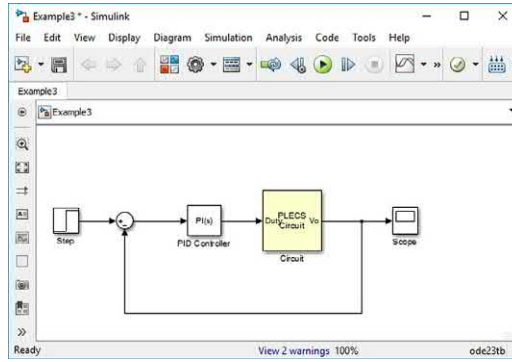


**FIG. 4.125** The reference of feedback loop changes from 5 V to 8 V at $t = 20$ ms.

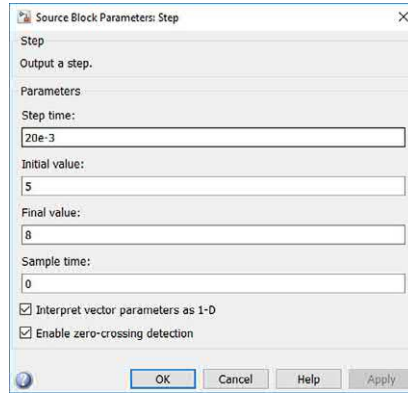


**FIG. 4.126** Setting of Step block.

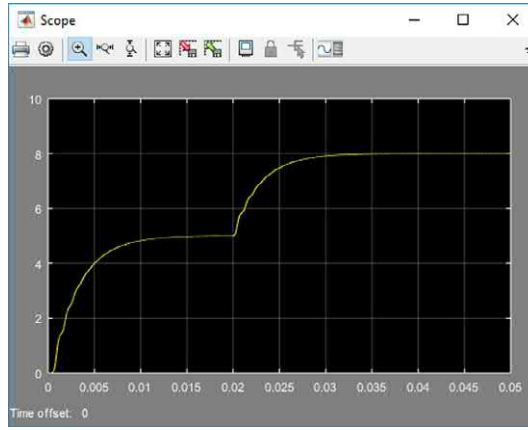


**FIG. 4.127** Simulation result.

You can study the effect of change in output load as well. In order to do this, the schematic is changed as shown in Fig. 4.128. Before closing the FETD1, the output load is 8 Ω. When the step block forces the FETD1 to conduct, the output load changes to $\frac{8\times8}{8+8}=4\,\Omega$. The step block settings are shown in Fig. 4.129. Simulation result is shown in Fig. 4.130. As shown, the controller keeps the voltage constant despite of disturbance (i.e., change in output load).

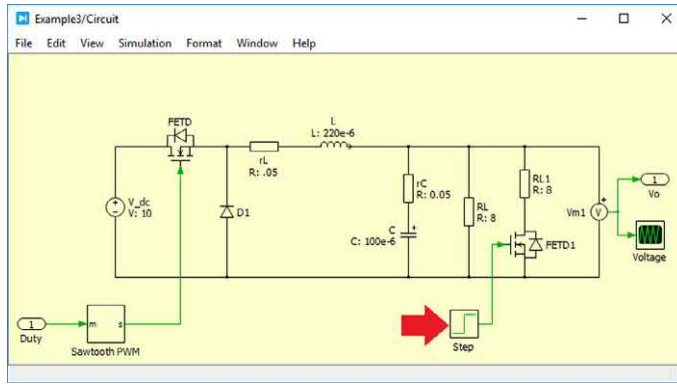


**FIG. 4.128** Schematic to study the effect of change in output load.

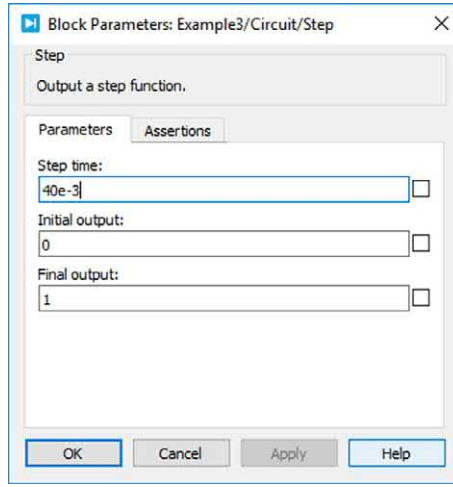


**FIG. 4.129** The Step block settings.

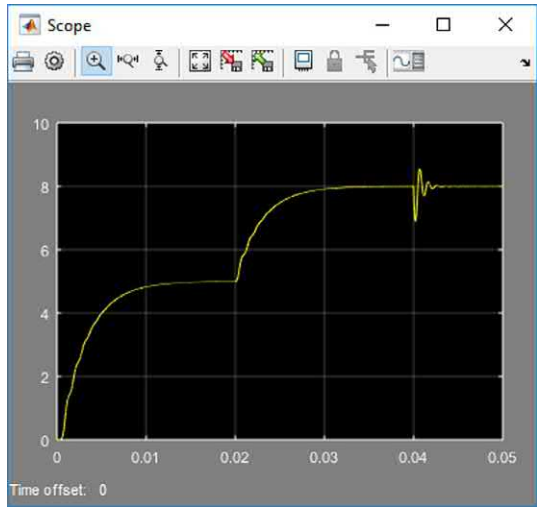


**FIG. 4.130** The simulation result.

It is recommended to use the scope block provided by PLECS block set to see the voltage/currents (Fig. 4.131). The PLECS scope provides much more capability to see voltage/currents in comparison to the general-purpose scope block of Simulink®. The PLECS scope can be found in the PLECS section of Simulink library browser window (Fig. 4.132).

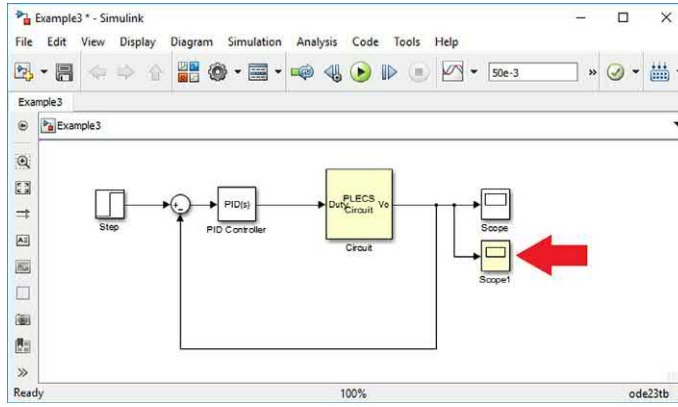


**FIG. 4.131** PLECS Scope block is a better option to analyze the voltage/currents.

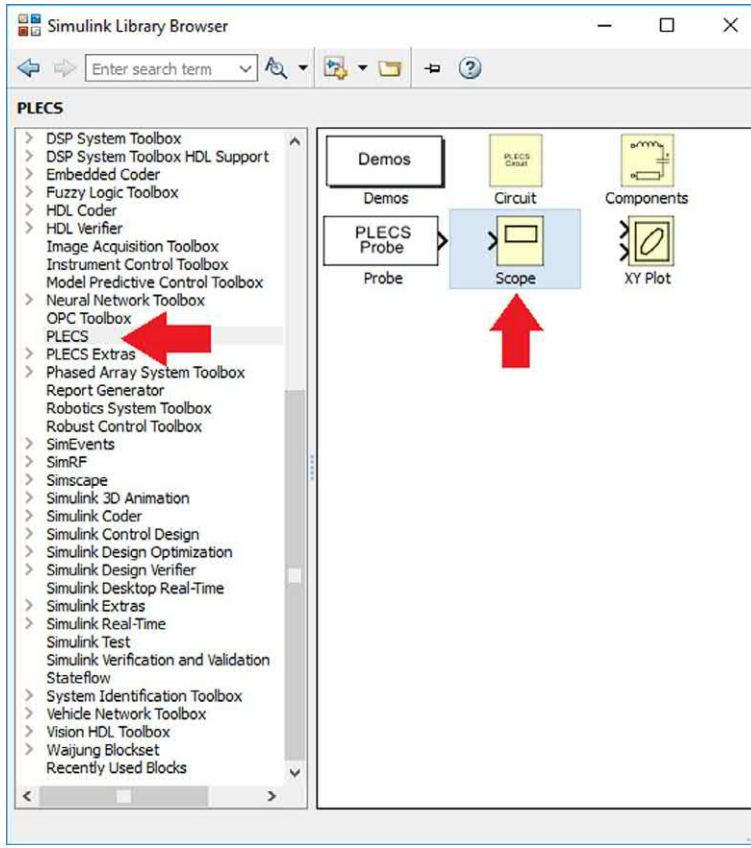


**FIG. 4.132** The Scope block of PLECS blockset.

You can test the designed controller with another type of disturbance as well. The schematic shown in Fig. 4.133 changes the input voltage from 10 V to 12 V at 45 ms. The step block settings are shown in Fig. 4.134.

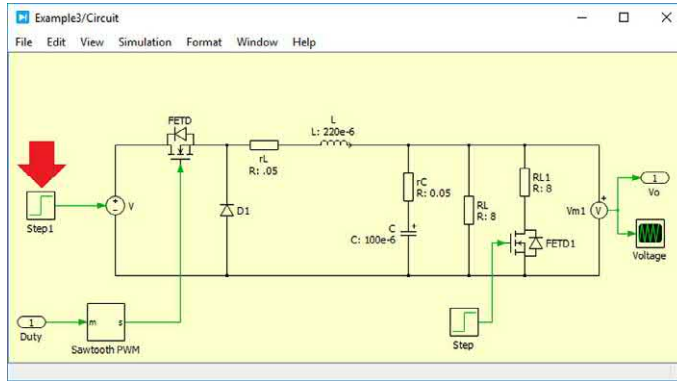


**FIG. 4.133** Schematic to study the effect of change in input voltage.

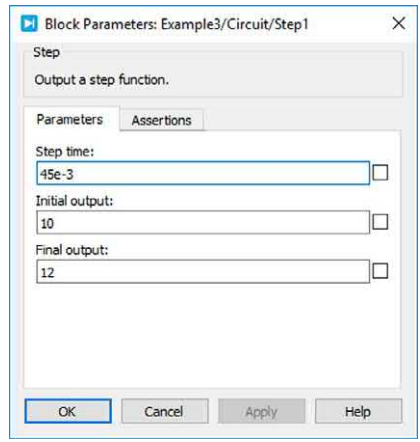


**FIG. 4.134** Setting of the Step1 block.

Increase the simulation interval from 50 ms to 60 ms and run the simulation. The simulation result is shown in Fig. 4.135. As shown, the controller keeps the output voltage constant despite the change in the input voltage (Fig. 4.136).

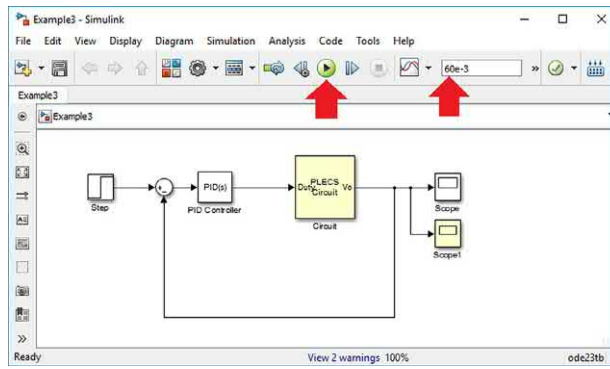


**FIG. 4.135** Increasing the simulation time to 60 ms. Click the Run button to run the simulation.

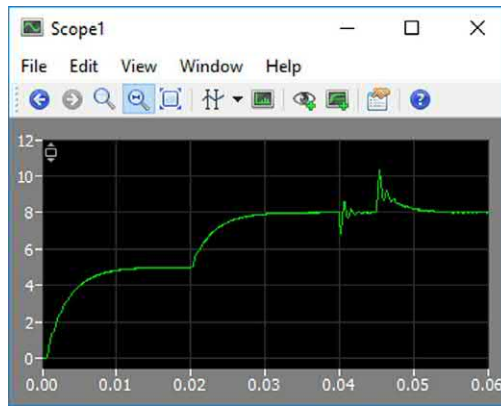


**FIG. 4.136** Simulation result.

## 4.10 Obtaining the control-to-inductor current transfer function

You can obtain the transfer function between the control input (duty ratio) and inductor current with the schematic diagram shown in Fig. 4.137. The Simulink® model must be like Fig. 4.138.

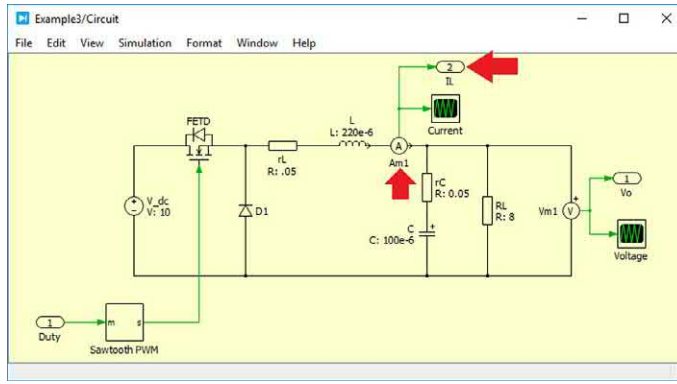


**FIG. 4.137** Addition of an ampere meter and Signal Outport blocks to the schematic.

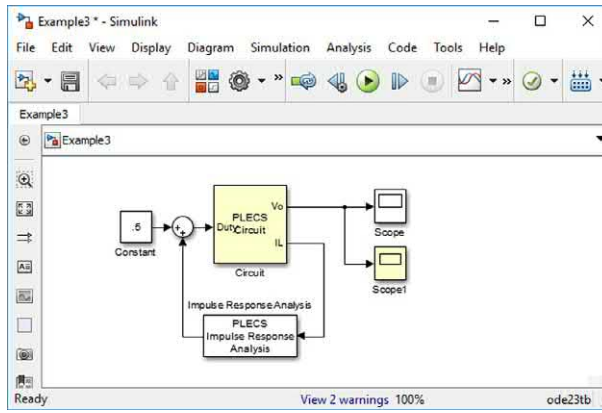


**FIG. 4.138** The Simulink model to extract the $\frac{\tilde{i}_L(s)}{\tilde{d}(s)}$.

Setting of PLECS Impulse Response Analysis block is shown in Fig. 4.139. We want to obtain the frequency response in the 10 Hz–25 kHz interval. Click the Start analysis button to start the analysis. The simulation result is shown in Fig. 4.140.

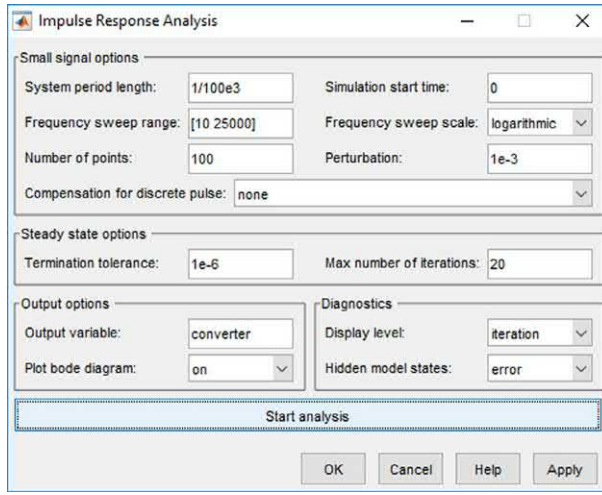


**FIG. 4.139** The Impulse Response Analysis block settings.

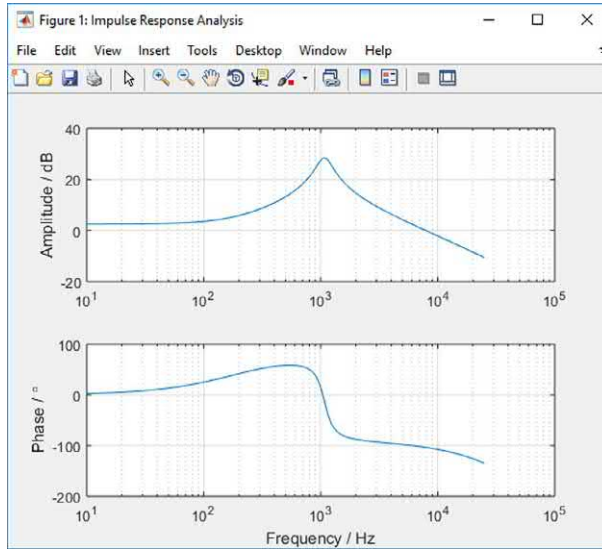


**FIG. 4.140** Control-to-inductor current transfer function.

## 4.11 Extraction of output impedance

You can obtain the output impedance of converter with the aid of schematic shown in Fig. 4.141 and Simulink model shown in Fig 4.142.

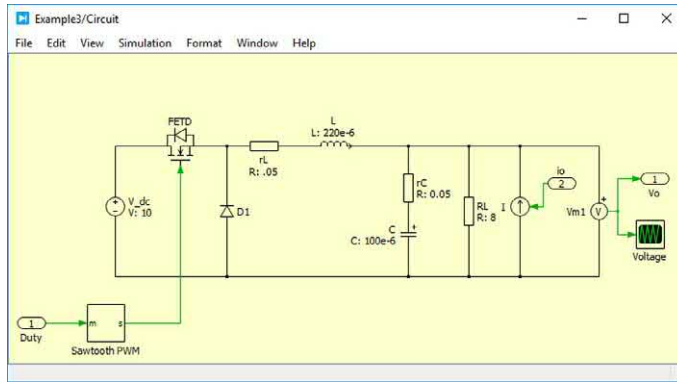


**FIG. 4.141** The schematic to extract the output impedance.

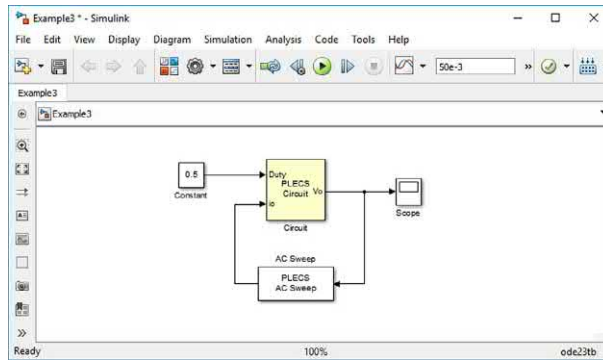


**FIG. 4.142** The Simulink model to extract the output impedance.

The AC sweep block can be found in the PLECS Extras section of Simulink Library Browser (Fig. 4.143).

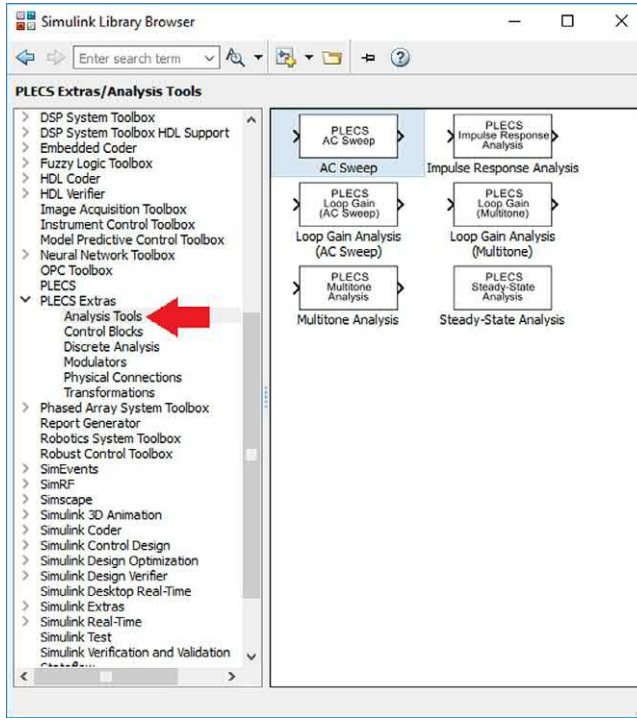


**FIG. 4.143** AC sweep can be found in the Analysis Tools section of Simulink Library Browser.

Double click the AC sweep block and change the block settings like Fig. 4.144.

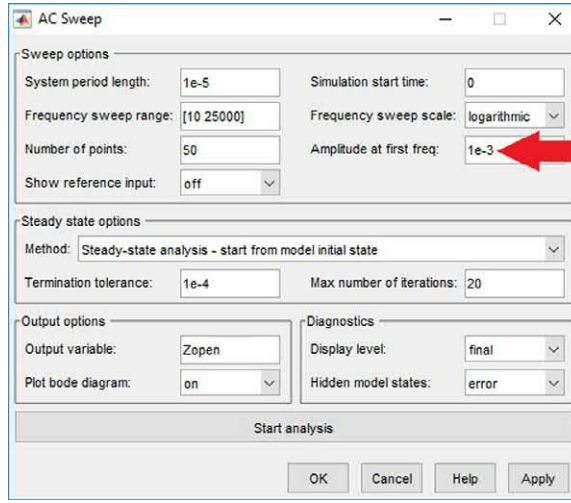


**FIG. 4.144** Setting of AC sweep block. It is recommended to click the Help button of AC sweep block and read the provided document.

Run the analysis by clicking the Start analysis. The result shown in Fig. 4.145 will appear.

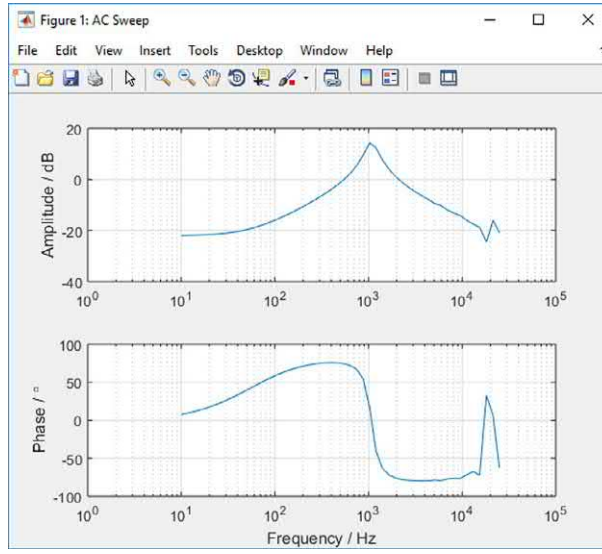


**FIG. 4.145** Simulation result for Amplitude at first freq.= 1 m.

The high-frequency portion of graph is not smooth, i.e., there are some fluctuations in the high-frequency portion of the graph. Increase the Amplitude at first freq. (Fig. 4.144) to 5e-3 and rerun the analysis. Fig. 4.146 shows the analysis result.

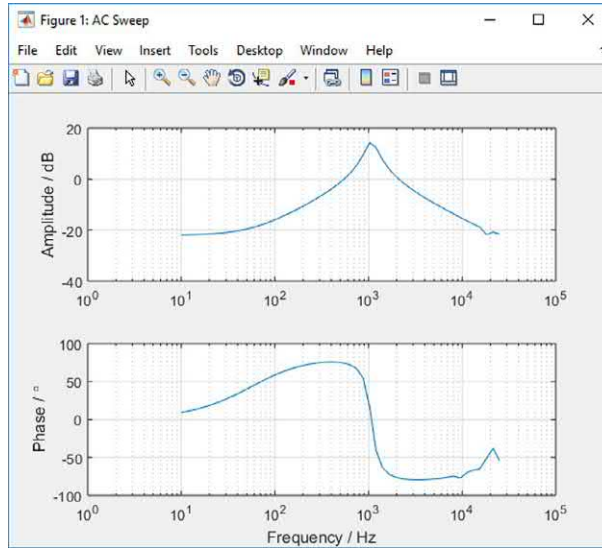


**FIG. 4.146** Simulation result for Amplitude at first freq.= 5 m.

As shown in Fig. 4.146, the curves are smoother in comparison to Fig. 4.145. If the Amplitude at first freq. (Fig. 4.144) increases to 10e-3, the result shown in Fig. 4.147 will appear. When there are fluctuations in the high-frequency portion of obtained transfer function, simply increase the Amplitude at first freq. in order to obtain a smoother graph.

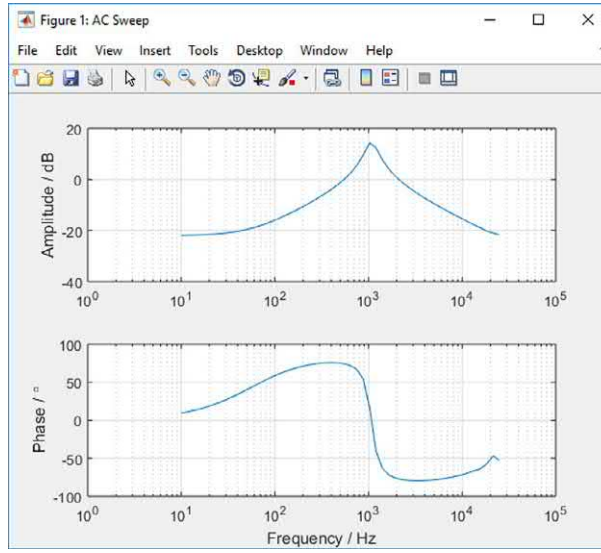


**FIG. 4.147** Simulation result for Amplitude at first freq.= 10 m.

## 4.12 Steady-state analysis

Consider a schematic diagram and Simulink model like the one shown in Figs. 4.148 and 4.149, respectively. We want to obtain the steady-state values of inductor current and output voltage.

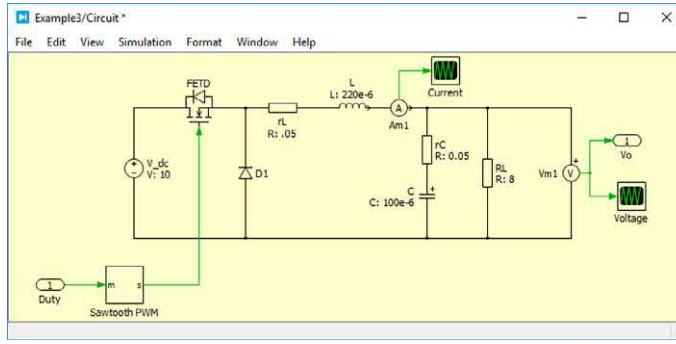


**FIG. 4.148** Schematic of buck converter. The output voltage of 5 V is needed.

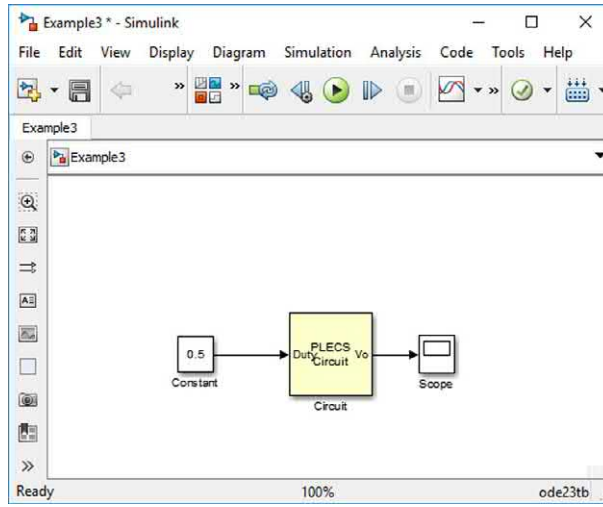


**FIG. 4.149** The Simulink model.

The Simulink model configurations are shown in Fig. 4.150.

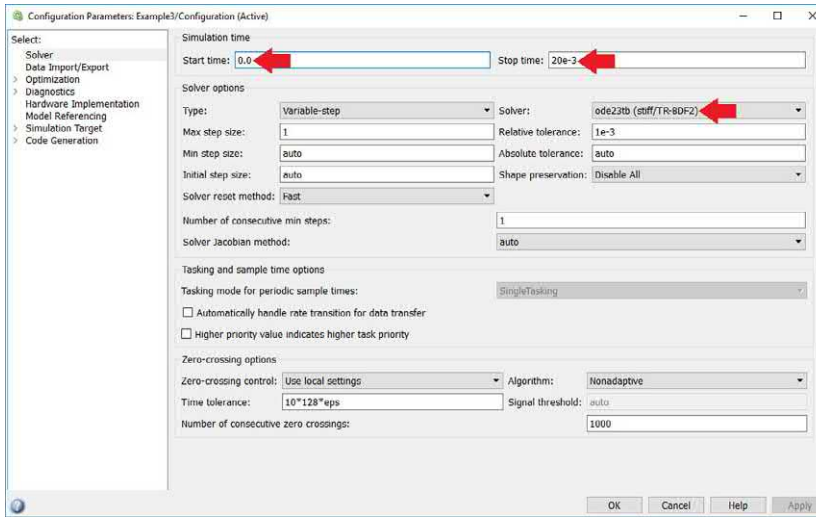


**FIG. 4.150** Configuration Parameters window.

Fig. 4.151 shows the output voltage.

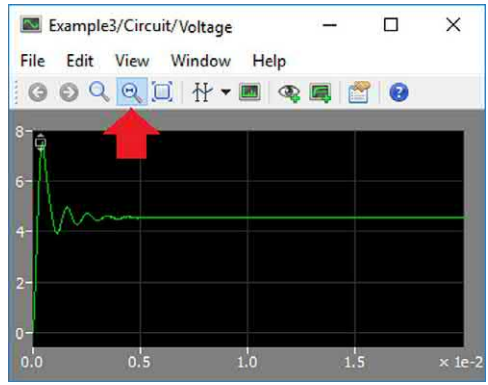


**FIG. 4.151** Output voltage (voltage of resistor).

You can use the magnifier icon (Fig. 4.151) to zoom into the steady-state portion of the graph and see the steady-state values. The steady-state portion of the graph is shown in Fig. 4.152.

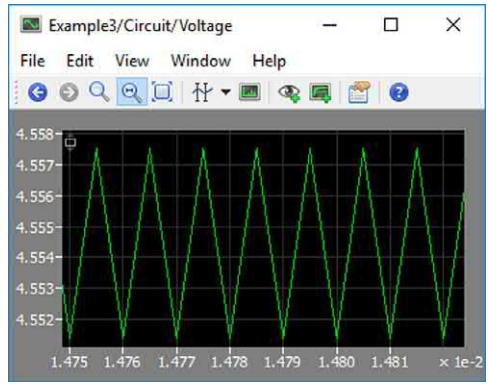


**FIG. 4.152** Steady-state portion of output voltage.

Fig. 4.153 shows the steady inductor current.

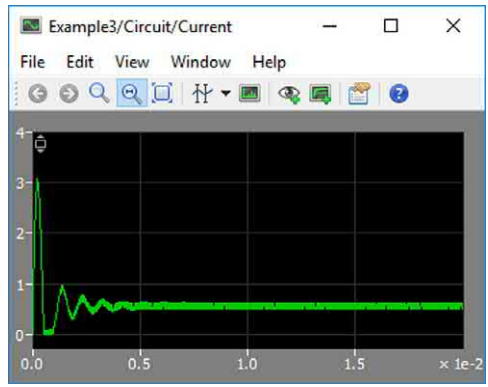


**FIG. 4.153** Inductor current.

The magnifier icon is used to see the steady-state portion of the graph.

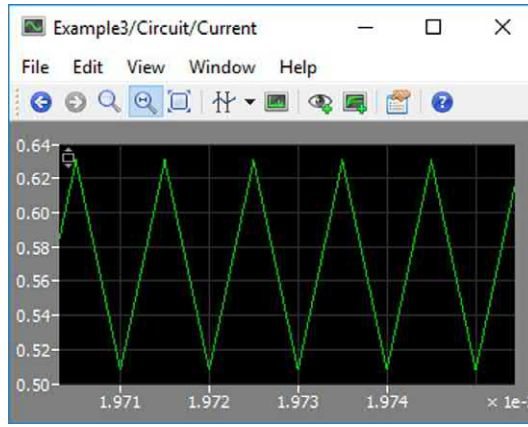


**FIG. 4.154** Steady-state portion of inductor current.

PLECS can calculate the steady-state operating point of converter by itself. So, there is no need to run the simulation and zoom into the steady-state portion of the graph. In order to calculate the Steady-state operating point, add a Steady-State Analysis block to the Simulink model as shown in Fig. 4.155. The Steady-State Analysis block can be found in the PLECS Extras section of Simulink Library Browser (Figs. 4.156 and 4.157).

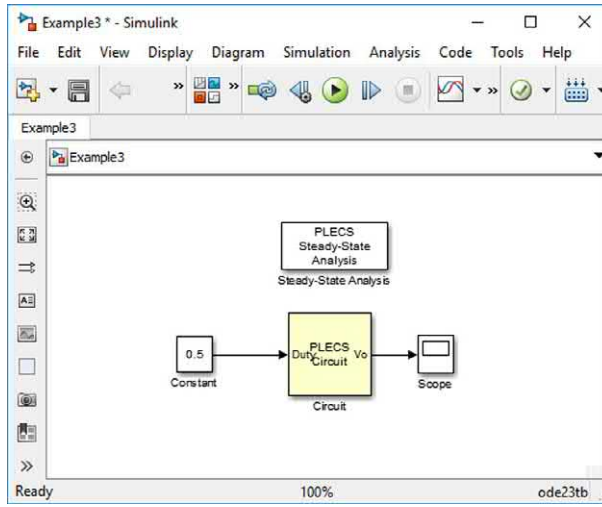


**FIG. 4.155** Simulink model to extract the steady-state values.

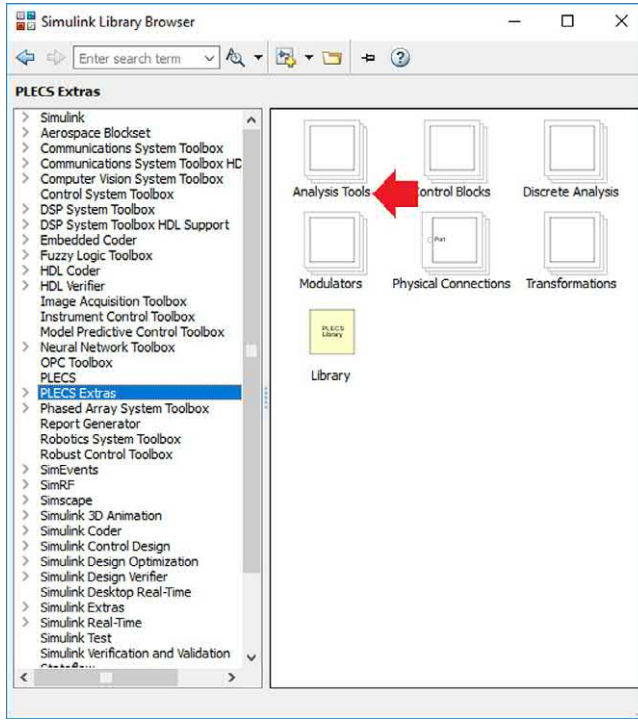


**FIG. 4.156** Steady-State Analysis block can be found in the Analysis Tools section of Simulink Library Browser.

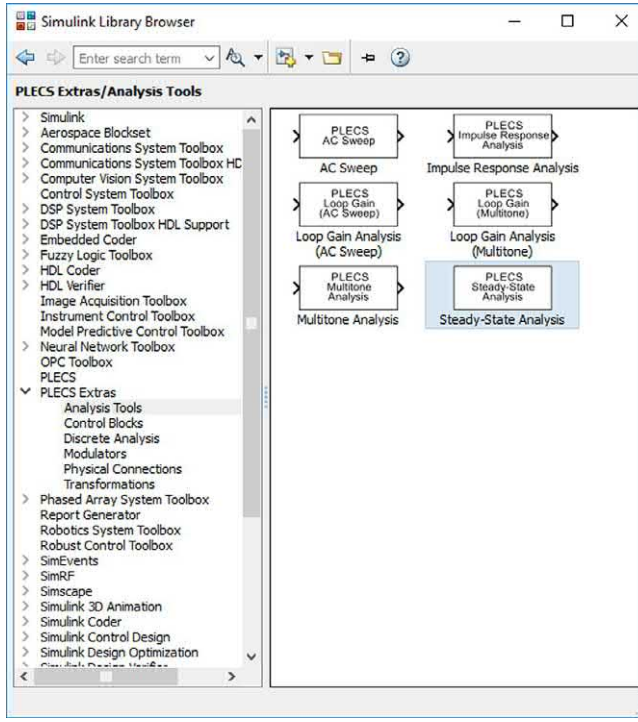


**FIG. 4.157** Steady-State Analysis block.

Double click the PLECS Steady-State Analysis block. The window shown in Fig. 4.158 will appear.

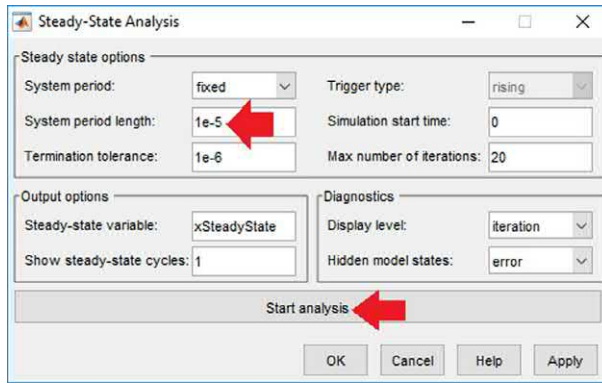


**FIG. 4.158** The Steady-State Analysis block settings.

The System period length is filled with 1/f, where f is the switching frequency. Since the switching frequency is 100 kHz, it is filled with 1e − 5, which is equal to $10^{-5}$. Click the Start analysis button (Fig. 4.158) to run the simulation. After simulation is finished, double click the PLECS circuit block in the Simulink model to open it. Double click the scopes to see the steady-state waveforms (Figs. 4.159 and 4.160). Compare these results with the result of previous analysis (Figs. 4.152 and 4.154). The results are the same.

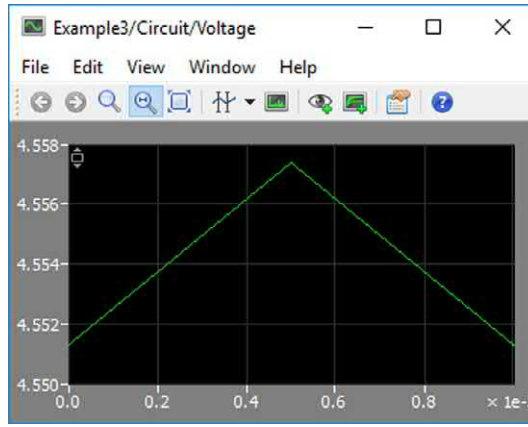


**FIG. 4.159** Steady-state output voltage waveform.

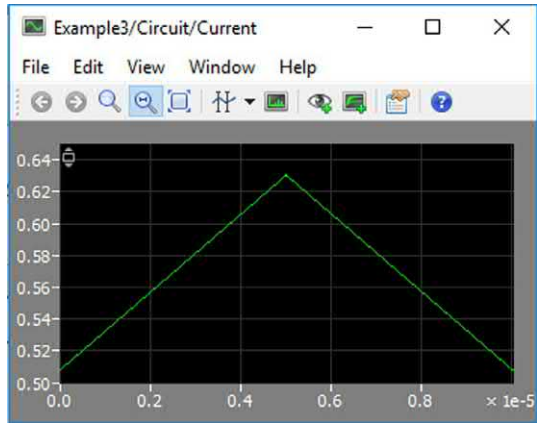


**FIG. 4.160** Steady-state inductor current waveform.

## 4.13 More simulation examples

Simulink version of PLECS comes with many different simulation examples. To access this example, double click the Demos icon in the Simulink Library Browser (Fig. 4.161).

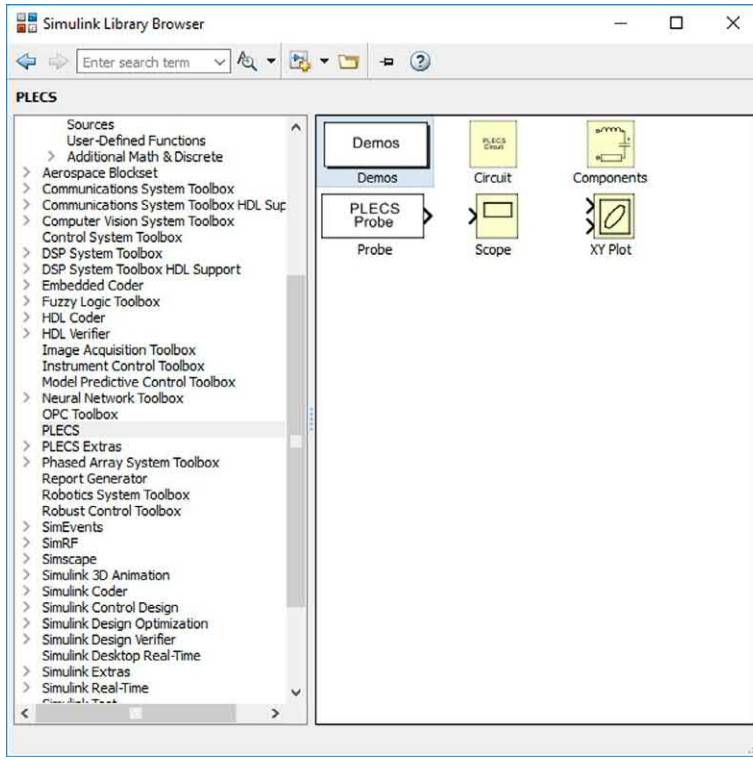


**FIG. 4.161** Demos section of PLECS block set.

After you double click the Demos, PLECS Help Viewer will be opened. Use the Contents tab in the left of window to select the category you want (Fig. 4.162).

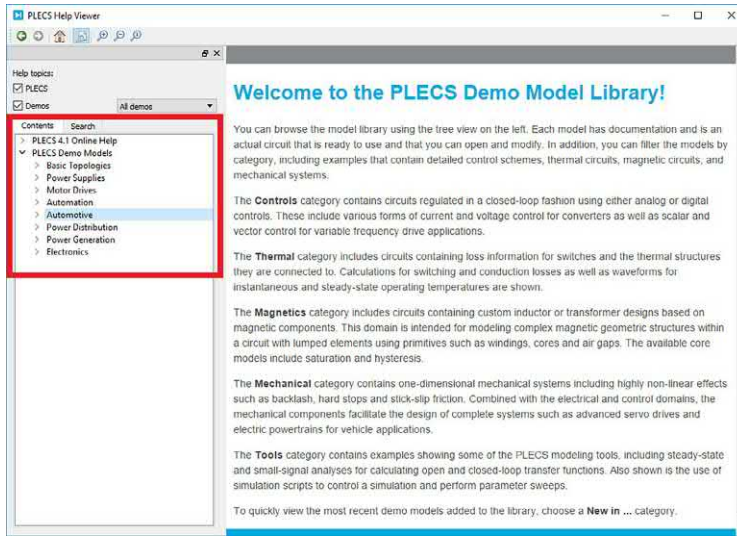


**FIG. 4.162** PLECS Help Viewer.

For instance, assume we want to see prepared examples related to Automotive applications. We click the Automotive section of Contents. A description about the simulation appears in the right window. You can open the model by clicking the Open this model (Fig. 4.163).

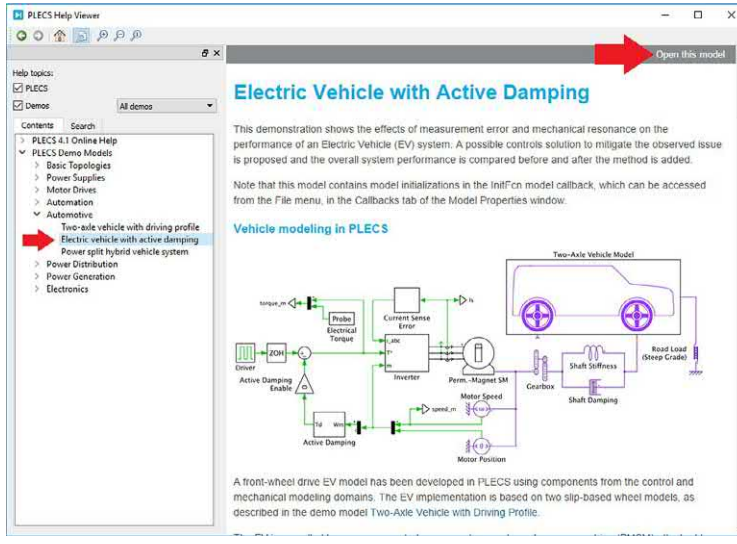


**FIG. 4.163** A sample example related to automotive. Click the Open this model to open the prepared simulation in Simulink.

After you clicked the Open this model, the prepared simulation will appear in the Simulink environment (Fig. 4.164).

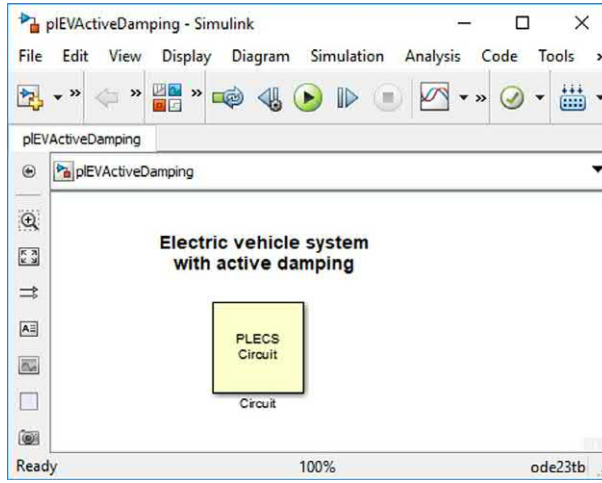


**FIG. 4.164** After Open this model is clicked, the prepared sample simulation is opened in the Simulink environment.

## Further reading

[1] F. Asadi, N. Abut, Simulation of power electronics converters with MATLAB/Simulink® (in Turkish), Umuttepe yayınları, 2018.
[2] F. Asadi, K. Eguchi, Dynamics and control of DC-DC converters, Morgan & Claypool, 2018. ISBN: 978-168-1732-98-5.
[3] F. Asadi, Computer techniques for dynamic modelling of DC-DC power converters, Morgan & Claypool, 2018. ISBN: 978-168-1734-19-4.
[4] F. Asadi, N. Abut, et al., Development of a power electronics converter dynamics toolbox for MATLAB, Int. J. Adv. Appl. Sci. 4 (6) (2017) 56–62.
[5] F. Asadi, N. Abut, et al., Designing a PI controller for Cuk converter using converter dynamics toolbox for MATLAB, Int. J. Adv. Appl. Sci. 4 (6) (2017) 175–180.
[6] F. Asadi, N. Abut, et al., Joy of controller design: controller design based on Kocaeli University's converter dynamics toolbox for MATLAB, Int. J. Adv. Appl. Sci. 4 (7) (2017) 5–10.
[7] F. Asadi, N. Abut, et al., KUCA: Kocaeli University Converter Analysis simulation software in power electronics, Int. J. Adv. Appl. Sci. 3 (12) (2016) 55–61.
[8] F. Asadi, N. Abut, et al., Pole placement based on derivative of states, Int. J. Adv. Appl. Sci. 3 (10) (2016) 100–102.

Chapter 5

# Thermal analysis of power electronics converters with PLECS

## Chapter outline



## 5.1 Introduction

The previous chapters focused on the electrical simulations of power electronics circuits. This chapter focuses on the thermal aspects of power electronics converters. Power stage of a power electronics converter is composed of capacitors, inductors, and semiconductors switches. Semiconductor switches dissipate a

Simulation of Power Electronics Converters Using PLECS®. https://doi.org/10.1016/B978-0-12-817364-0.00005-9

part of energy in form of heat. The energy losses in the semiconductor switches increase the temperature of device. The produced thermal energy must be taken from the semiconductor switch with the aid of a heat sink; otherwise, the semiconductor switch fails, i.e., it burns. So, good thermal design, i.e., designing a suitable heat sink, is an important part of power electronics converters design process.

This chapter focuses on the thermal analysis capabilities of PLECS®. A single-phase inverter is studied as an illustrative example in this chapter. The switches energy losses are modeled with the aid of datasheet. Total energy losses are calculated with PLECS® and a suitable heat sink is designed for the inverter. Effect of modulation strategy on inverter losses is studied as well. Thermal analysis of other types of power electronics converters can be done in the same way shown in this chapter.

## 5.2 Single-phase open-loop inverter

Single-phase inverters are commonly used for residential photovoltaic applications, uninterruptible power supplies, and standalone power supplies. One important design aspect for an inverter is the thermal design. In particular, the heat sink thermal resistance must be calculated in order to keep the peak heat sink and junction temperatures within specified design limits. The thermal design is highly dependent on the semiconductor losses, which can be calculated easily using the thermal modeling features of PLECS.

Consider the single-phase inverter shown in Fig. 5.1.

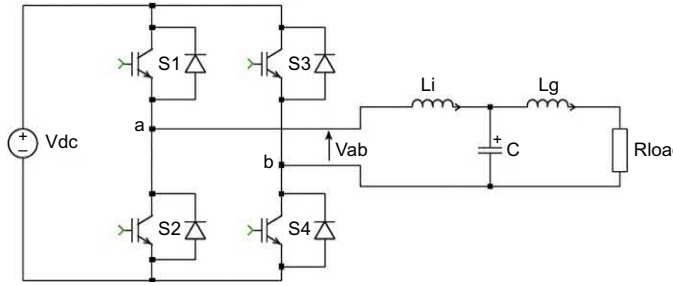


**FIG. 5.1** The schematic of single-phase inverter. Assume that inverter legs (i.e., switch S1-S2 or S3-S4) are realized with Infineon EasyPACK™ IGBT Power Modules F4-50R06W1E3. The datasheet can be found in appendixes. According to datasheet, the device junction can withstand up to 175°C; however, in this chapter, we limit the maximum junction temperature to 125°C in order to increase the device life.

The inverter parameters are shown in Table 5.1.

**TABLE 5.1 Parameters of single-phase inverter shown in Fig. 5.1.**

| | |
|---|---|
| Input DC voltage | 400 V |
| Peak output voltage | 325 V |
| Output frequency | 50 Hz |
| Load resistance | 17.6 Ω |
| Switching frequency | 16 kHz |
| $L_i$ | 0.75 mH |
| $L_g$ | 0.5 mH |
| $C$ | 2.2 μF |

We use the open loop control to the output voltage in this example. Block diagram of open-loop voltage control strategy is given in Fig. 5.2. We want to obtain a sinusoidal output voltage with peak amplitude of 325 V.

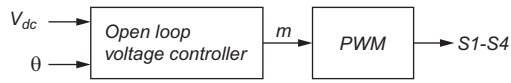


**FIG. 5.2** Open-loop control of single-phase inverter.

The switches are modulated using a bipolar sinusoidal PWM strategy as depicted in Fig. 5.3. With bipolar modulation, the switches S1, S4 are turned on together as a pair to create a positive voltage at the inverter output terminals and the switch pair S2, S3 are turned on to create a negative output voltage.

The modulation index is calculated in order to create a sinusoidal output voltage with a peak amplitude of 325 V.

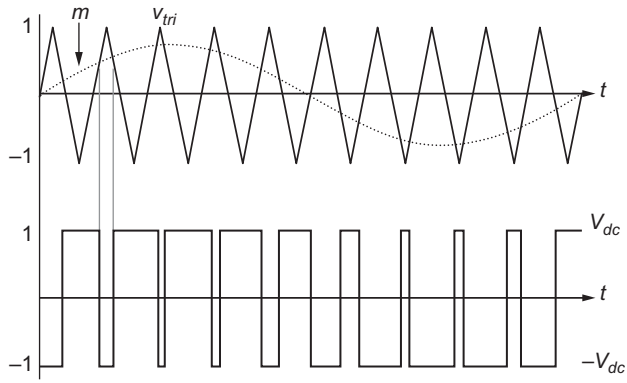


**FIG. 5.3** Bipolar modulation.

$$m = \frac{V_O^*}{V_{dc}} = \frac{325\sin(\theta)}{V_{dc}},$$

where $V_O^*$ is the reference sinusoidal output voltage and $\theta = 2\pi ft$ is the reference output voltage angle given as a function of output frequency, $f$, and time, $t$.

## 5.3 Electrical simulation of single-phase inverter

Fig. 5.4 shows the schematic of single-phase inverter in the PLECS environment. We want to obtain the electrical waveforms of the circuit in this section.

Settings of blocks used are shown in Figs. 5.5–5.7.

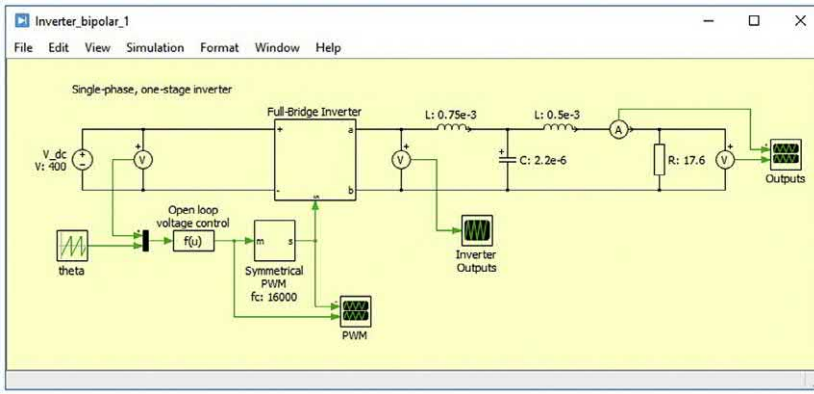


**FIG. 5.4** Schematic of single-phase inverter in the PLECS environment.

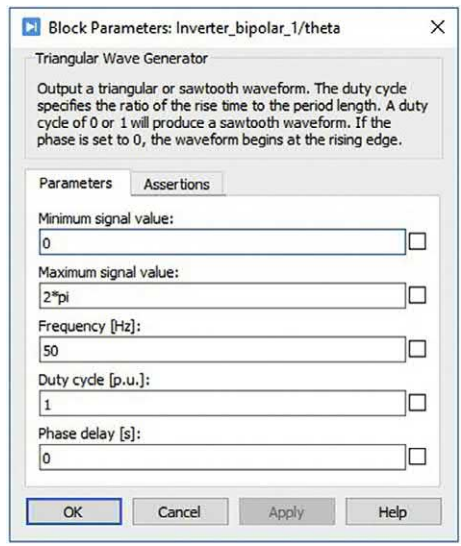


**FIG. 5.5** Settings of theta block.

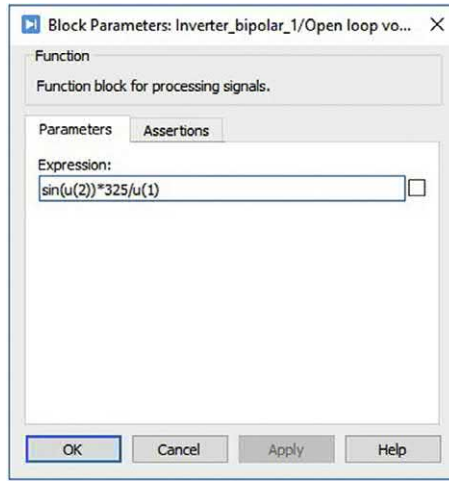


**FIG. 5.6** Setting of Open-loop voltage control Function block.

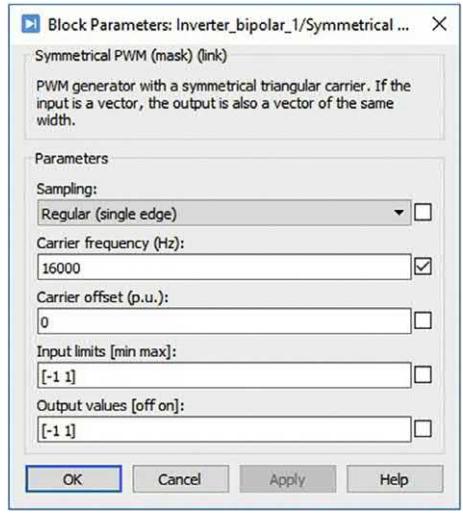


**FIG. 5.7** Settings of Symmetrical PWM block.

Value of input DC voltage ($V_{dc}$) and $\theta$ is entered into the Open-loop voltage control block with the aid of a Signal Multiplexer block (Fig. 5.8).

Inside of Full-bridge Inverter subsystem is shown in Fig. 5.9. The two function blocks (Fig. 5.10) close the required switches according to the signal entering s port of subsystem. IGBT1 and IGBT4 are closed when the signal entered to s port is positive, and IGBT2 and IGBT3 are closed when the signal entered s port is negative.

Figs. 5.11 and 5.12 show the settings of the two function blocks.

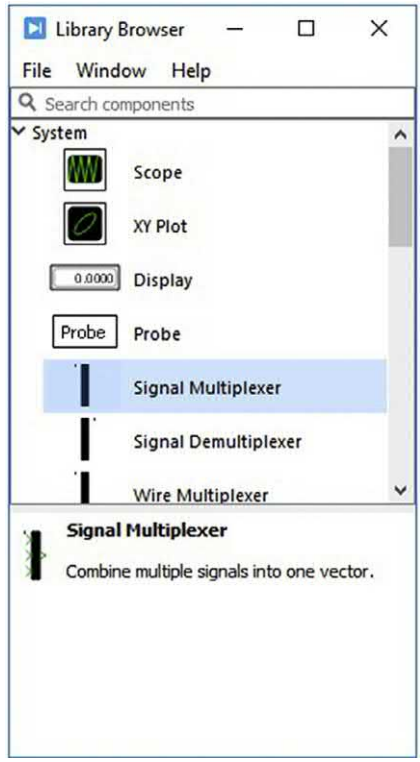


**FIG. 5.8** Signal Multiplexer block can be found in the System section of Library Browser.

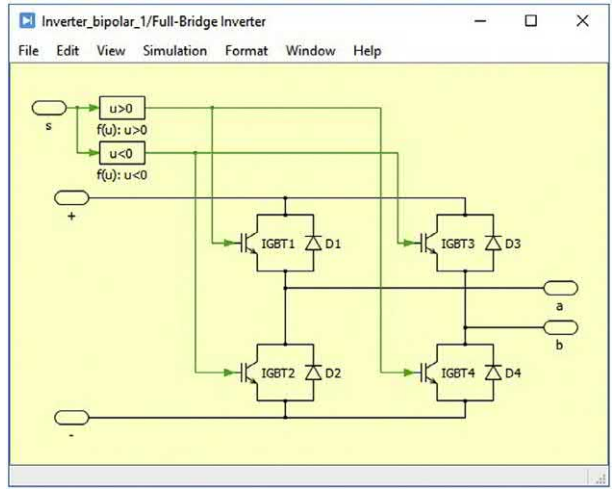


**FIG. 5.9** Inside the Full-Bridge Inverter subsystem.

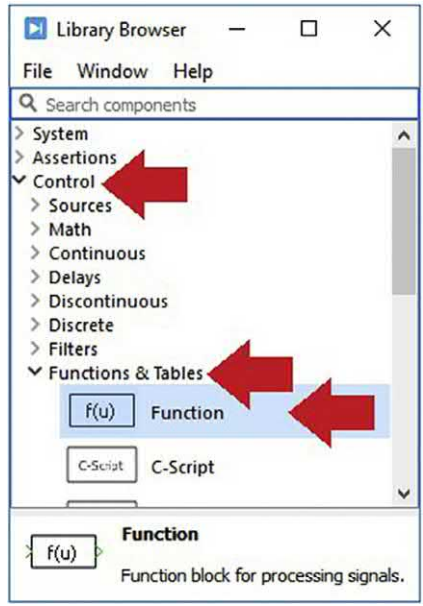


**FIG. 5.10** Function block can be found in the functions and tables section of Library Browser.

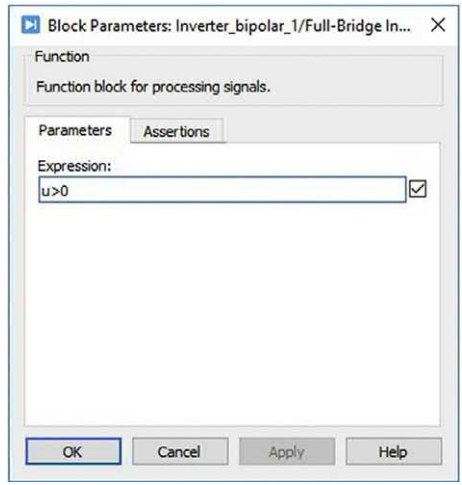


**FIG. 5.11** Settings of upper Function block (see Fig. 5.9).

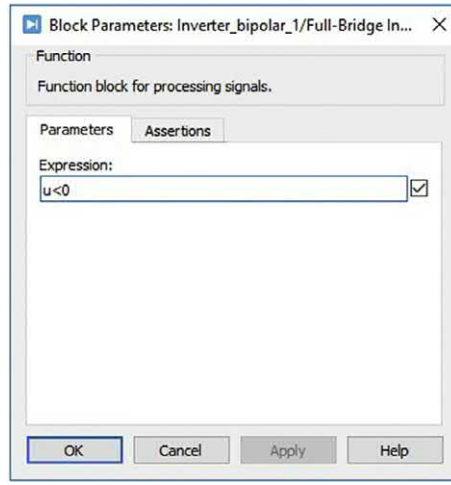


**FIG. 5.12** Setting of lower Function block (see Fig. 5.9).

Don't use the IGBT with diode block (Fig. 5.13) for the power stage of inverter. Instead use the IGBT and diode blocks (Fig. 5.14). This simplifies the thermal modeling of converter.

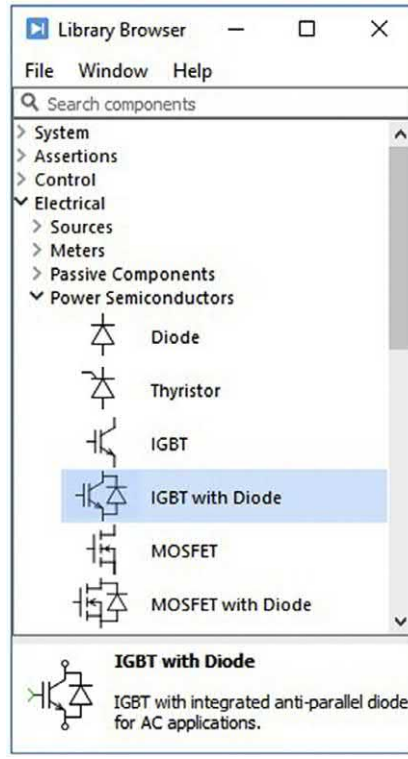


**FIG. 5.13** IGBT with Diode block.

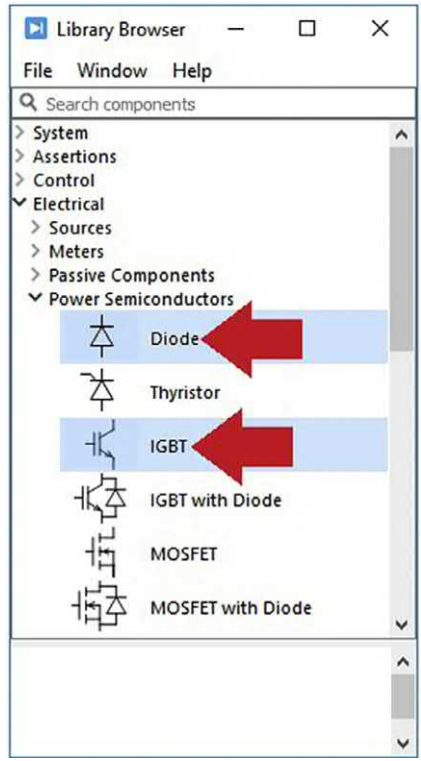


**FIG. 5.14** IGBT and Diode blocks.

Settings of IGBT's and diodes are shown in Figs. 5.15 and 5.16, respectively.

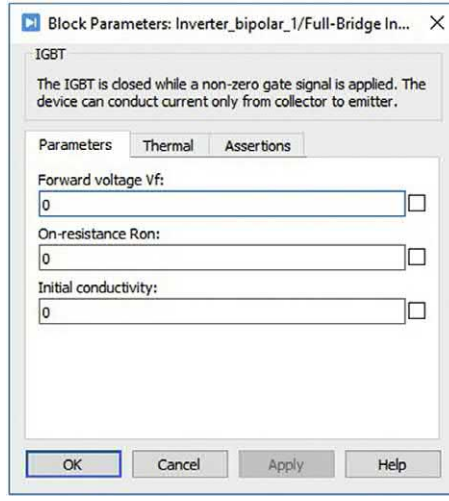


**FIG. 5.15** IGBT block settings. All the IGBTs have these settings.

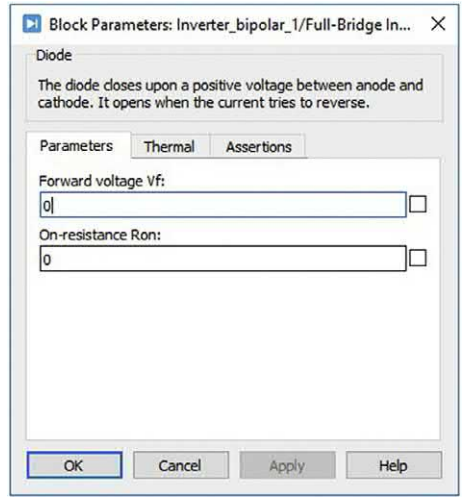


**FIG. 5.16** Diode block settings. All the diodes have these settings.

Click the Simulation parameters (Fig. 5.17) and change the settings as shown in Fig. 5.18.

Press Ctrl+T or click the Start (Fig. 5.19) to run the simulation.

The simulation results are shown in Figs. 5.20–5.24.

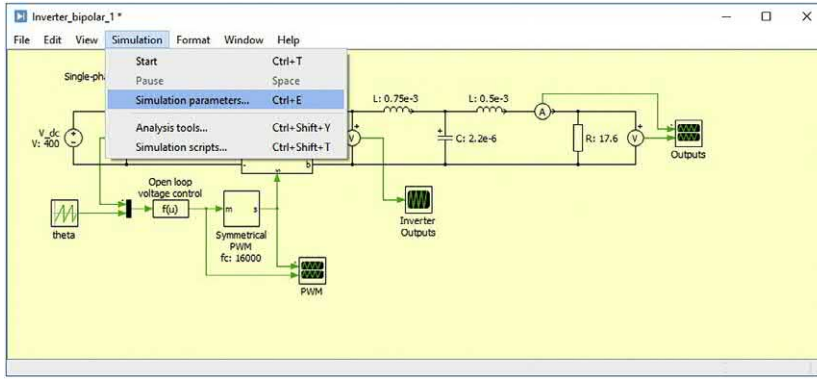


**FIG. 5.17** Simulation Parameters window can be made visible with the aid of Simulation parameters in the Simulation window.

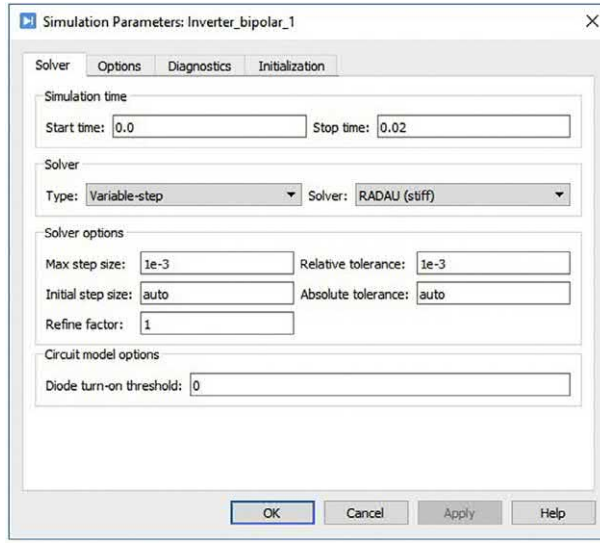


**FIG. 5.18** Simulation Parameters window.

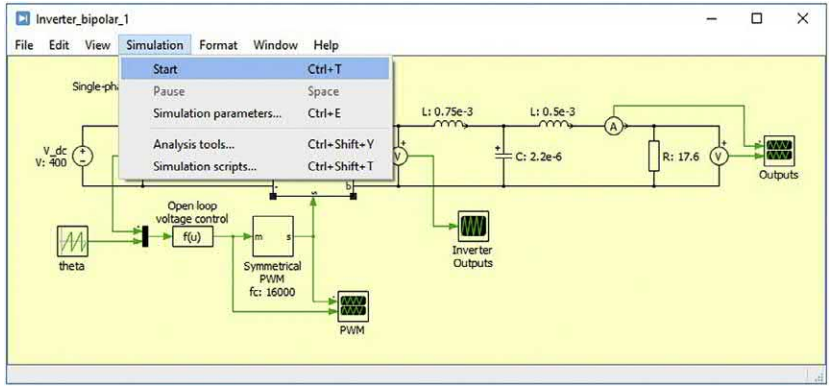


**FIG. 5.19** Running the simulation.

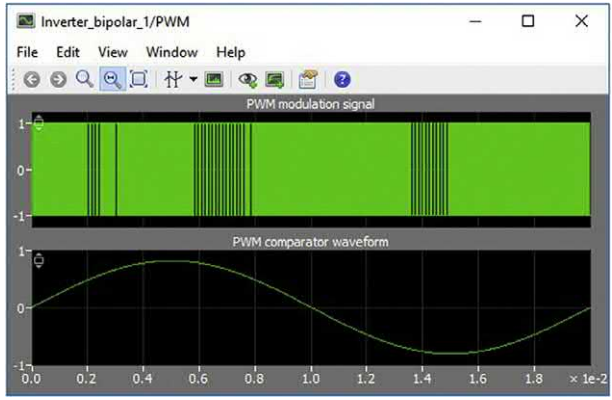


**FIG. 5.20** PWM scope waveforms. Use the magnifier icon to zoom in.

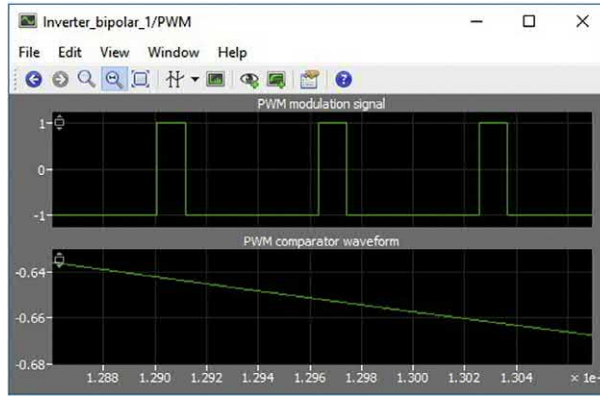


**FIG. 5.21** Close up of PWM scope waveforms.

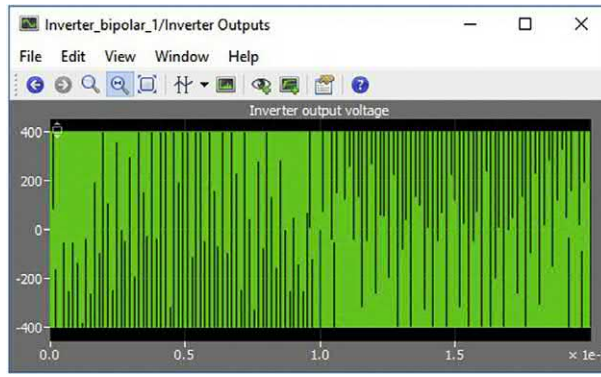


**FIG. 5.22** Inverter Outputs scope waveform.

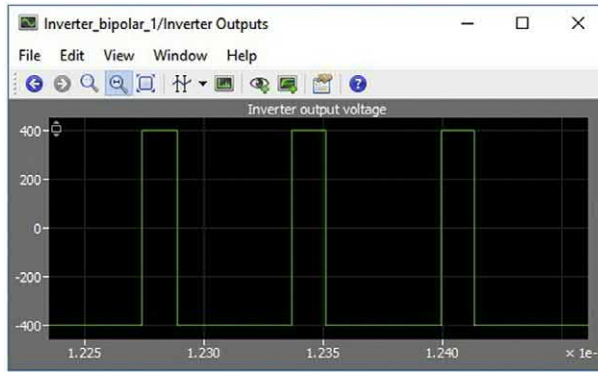


**FIG. 5.23** Close up of Inverter output voltage scope waveform.

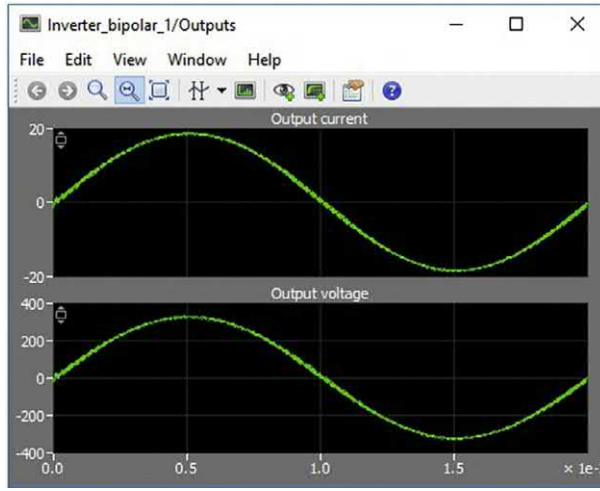


**FIG. 5.24** Outputs scope waveform.

## 5.4 Thermal description of semiconductor switches

To calculate the inverter losses and simulate the thermal performance of the inverter, thermal loss descriptions of the semiconductors are first required. Using the data sheet for the Infineon F4-50R06W1E3 IGBT module, we will create a thermal description for the IGBT and body diode. We will need to enter the following information for each component: conduction losses, switching losses, and thermal impedance between junction and case.

## 5.5 Switching losses

The current and voltage of a semiconductor switch does not change instantaneously. This concept is shown in Fig. 5.25.

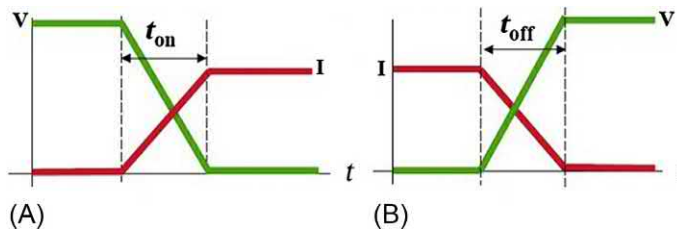


**FIG. 5.25** The semiconductor switch (A) turns on (B) turns off.

As shown in Fig. 5.25A and B, during the $t_{off}$ or $t_{on}$ the current and voltage are not zero, so their product, i.e., the power loss, is not zero. The power lost during the turn on is called turn-on switching loss and the power during the turn

off is called turn-off switching loss. Switching loss happens only in transitions, i.e., when an on device turns off or when an off device turns on.

The switching losses are modeled (with the aid of datasheet) in the next sections.

### 5.5.1 Turn-on switching losses for the IGBT

In order to define the switching losses of IGBT, open the Full-Bridge Inverter subsystem and double click on the IGBTs, i.e., IGBT1. A window like the one shown in Fig. 5.26 will be opened.

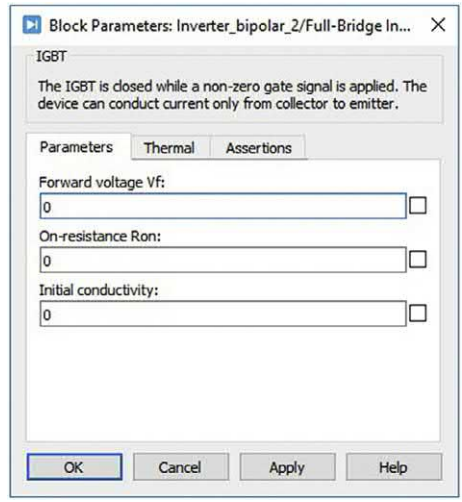


**FIG. 5.26** IGBT parameters window.

Click the Thermal tab (Fig. 5.27).

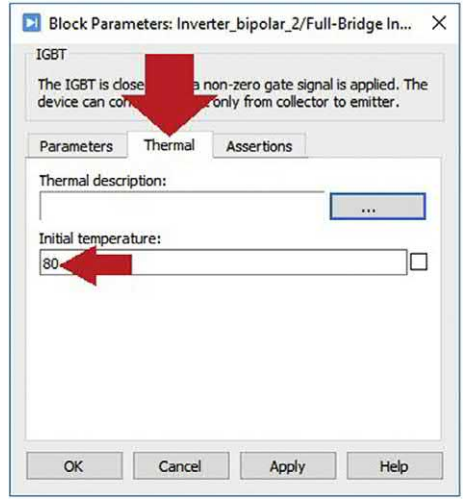


**FIG. 5.27** Thermal tab of IGBT. It is assumed that junction initial temperature is 80°C.

Click the button shown in Fig. 5.28 to open the drop down list. Click the New thermal description to enter the switching and conduction losses of IGBT.

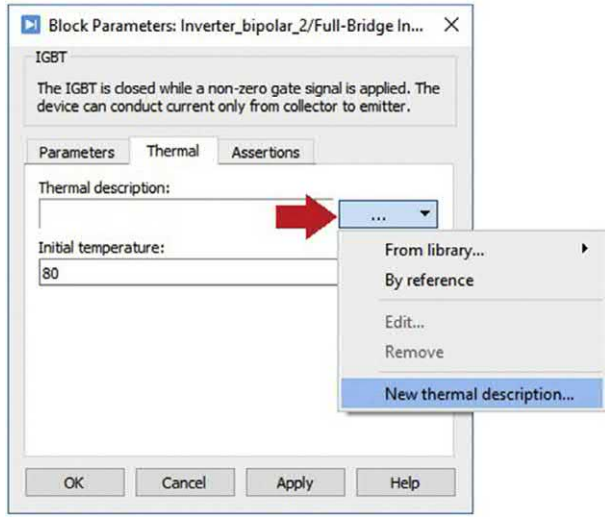


**FIG. 5.28** The thermal behavior of IGBT is defined with the aid of New thermal description.

After you clicked the New thermal description, the window shown in Fig. 5.29 will appear. The switching and conduction losses of IGBT are set with the aid of this window.

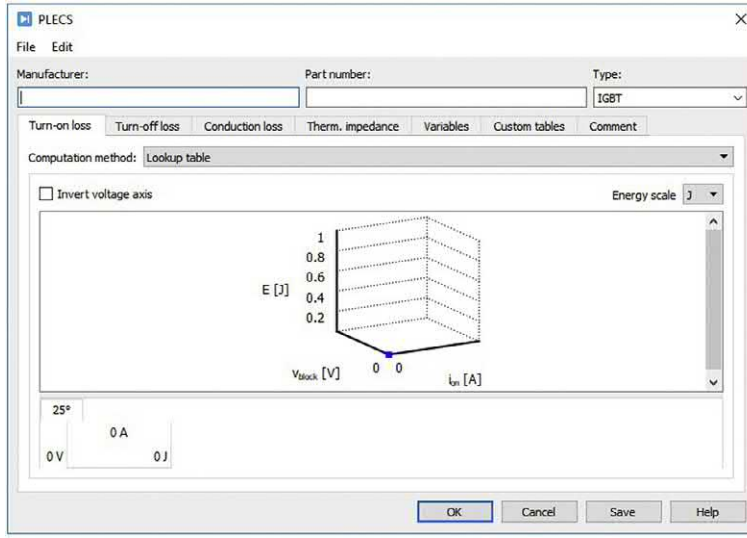


**FIG. 5.29** It is recommended to click the Help button and read the provided help page of window in order to see the details of this window.

First of all enter the manufacturer name and part number to the Manufacturer and Part number boxes, respectively. Set the Type to IGBT since we are modeling an IGBT (Fig. 5.30).

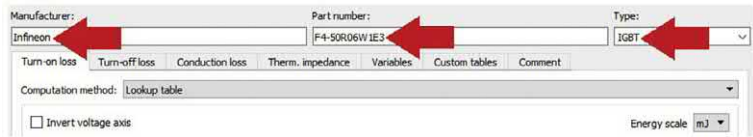


**FIG. 5.30** Entering the IGBT information.

Set the Computation method to Lookup table. Selection of Lookup table lets you enter the blocking voltage, the device current, and the junction temperature according to the graphs given in datasheet. Set the Energy scale to milli Joul (mj), since the datasheets generally give the losses in terms of mJ (Fig. 5.31).

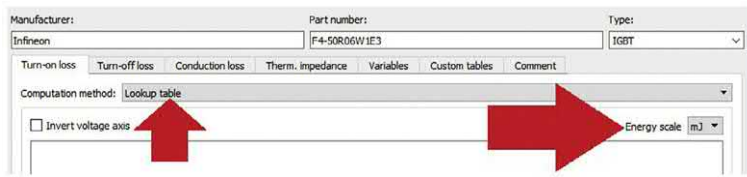


**FIG. 5.31** It is recommended to select Lookup table for Computation method and mj for Energy scale. When you use Lookup table, PLECS uses interpolation (or extrapolation) to calculate values that are not defined in the given table.

The graph of switching losses for IGBT is shown in Fig. 5.32. The datasheet gives the switching losses for two junction temperatures, 125°C and 150°C. We use the $E_{on}$ curves to model the turn on switching losses of the IGBT.

Go to Turn-on loss tab in order to enter the turn-on losses (Fig. 5.33).

Enter the data for 125°C and 150°C to the software (Figs. 5.34 and 5.35). The datasheet only provides the data for 300 V. To add a linear relationship between the switching losses and voltage, extend loss line to 0 V by entering loss values 0 mJ at 0 V for all currents.

You can add a new temperature tab to the table by right clicking on the temperature tab and selecting the New temperature values (Fig. 5.36).

You can add a new current column to the table by right clicking on one of the current columns and selecting the New current values (Fig. 5.37).

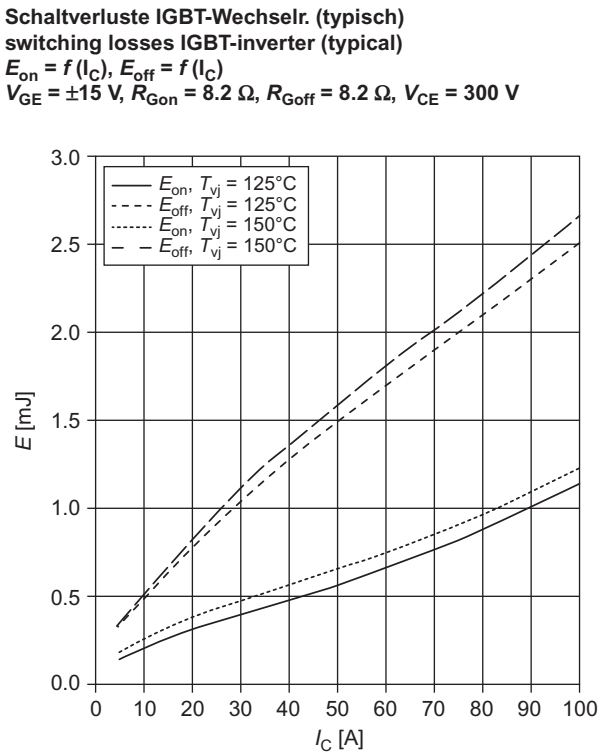


**FIG. 5.32** Switching losses versus collector current. Eon shows the turn-on losses, while the Eoff shows the turn-off losses. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

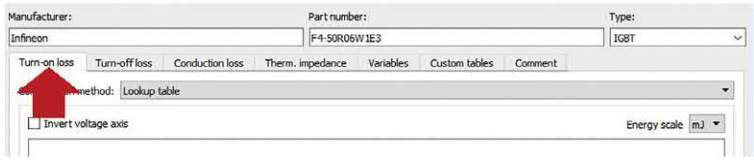


**FIG. 5.33** Turn-on tab is used to enter the turn-on losses data.

You can add a new voltage row to the table by right clicking on one of the voltage rows and selecting the New voltage values (Fig. 5.38).

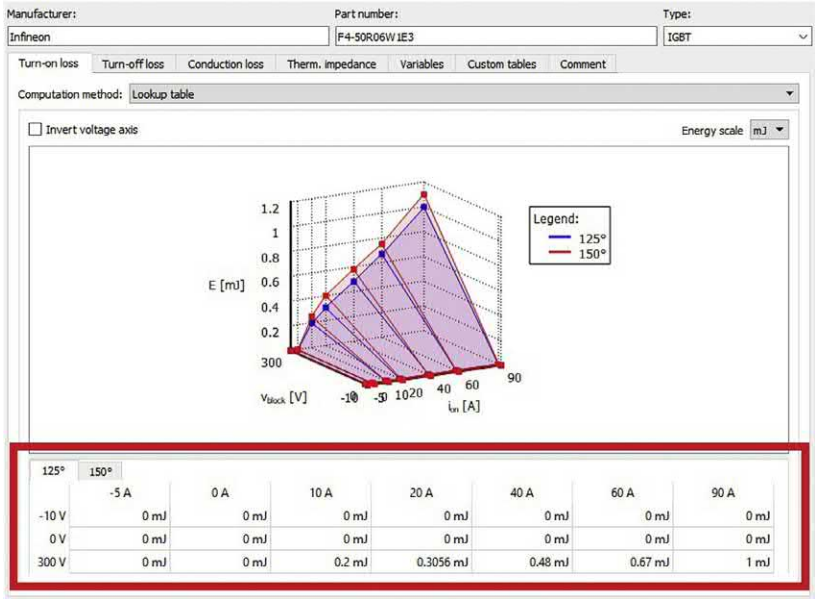


**FIG. 5.34** Turn on switching losses for 125°C and different collector currents.

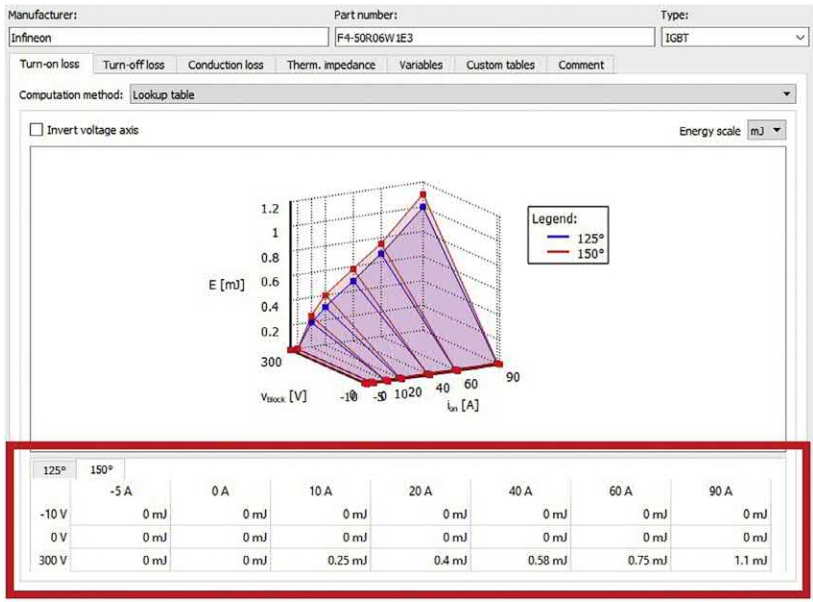


**FIG. 5.35** Turn on switching losses for 150°C and different collector currents.

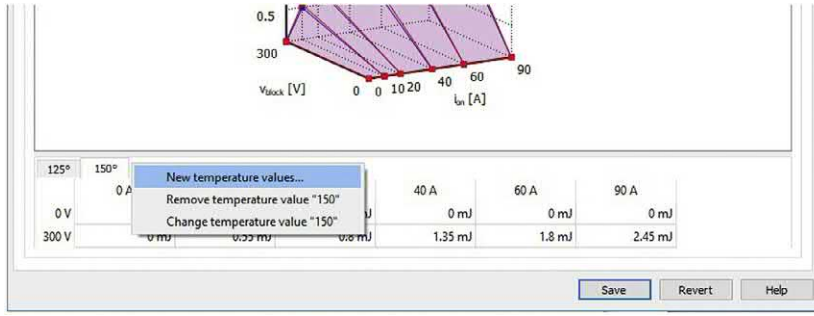


**FIG. 5.36** Addition of new temperature data points.


**FIG. 5.37** Addition of new current data point.

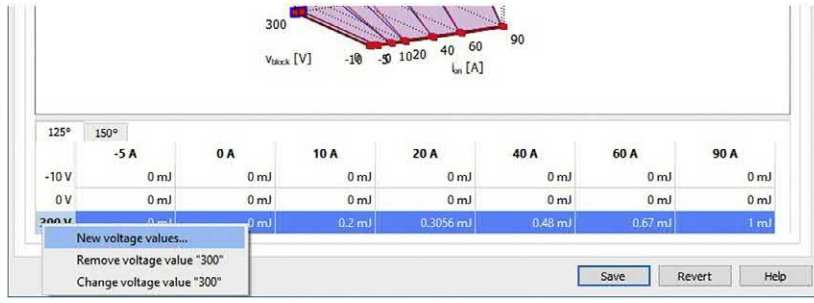


**FIG. 5.38** Addition of new voltage data point.

### 5.5.2 Turn-off switching losses for the IGBT

Graph of switching loss of IGBT is redrawn in Fig. 5.39 for ease of reference. We use the $E_{off}$ curves to model the turn-off switching losses of the IGBT.

In order to model the turn-off switching losses of IGBT, click the Turn-off loss tab (Fig. 5.40).

Enter the dissipated energy according to the graph shown in Fig. 5.39 (use the $E_{off}$ curve). To add a linear relationship between the switching losses and

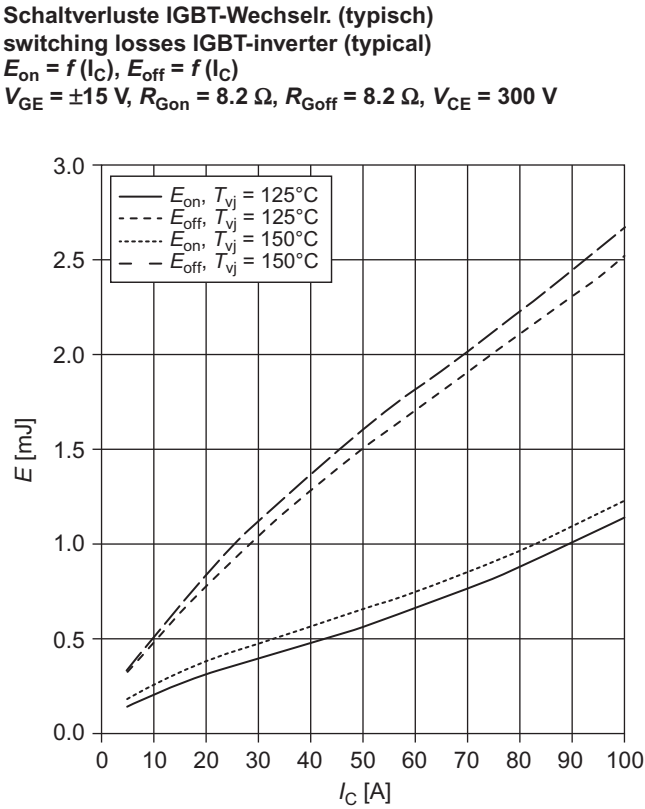


**FIG. 5.39** Switching losses versus collector current. $E_{off}$ shows the turn-off losses. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

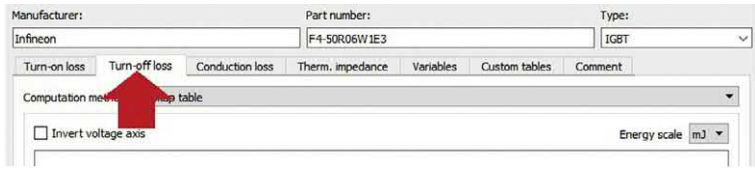


**FIG. 5.40** Turn-off loss tab of thermal editor.

voltage, extend loss line to 0 V by entering loss values 0 mJ at 0 V for all currents (Figs. 5.41 and 5.42).

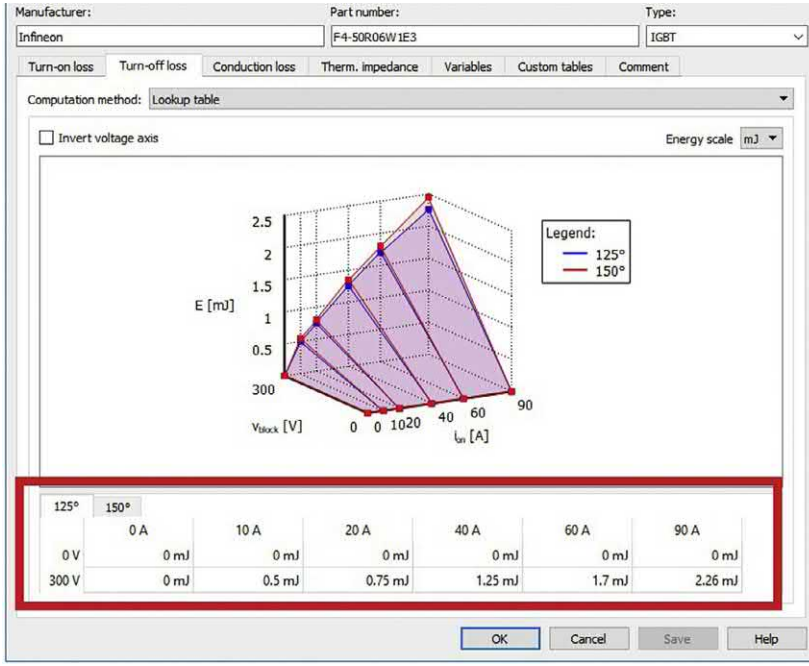


**FIG. 5.41** Turn-off switching losses for 125°C and different collector currents.

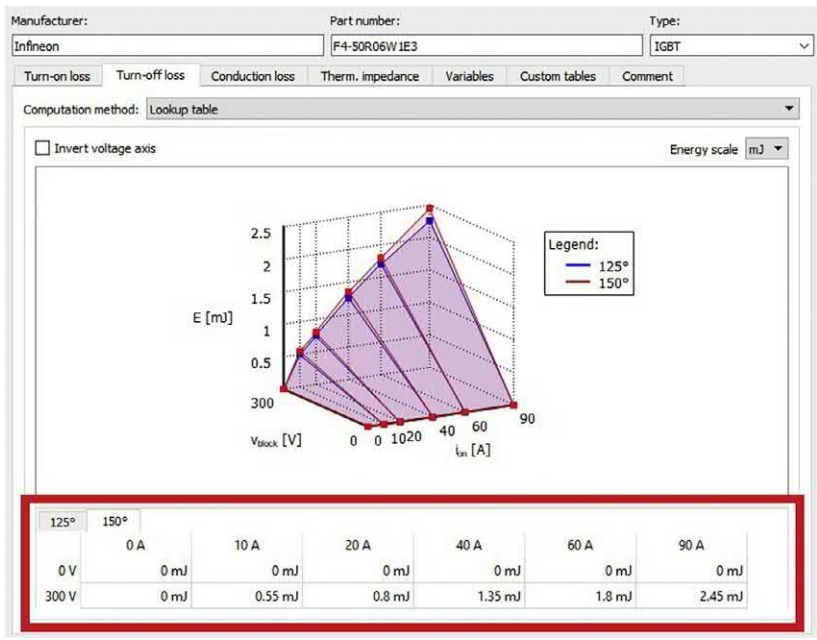


**FIG. 5.42** Turn-on switching losses for 150°C and different collector currents.

## 5.6 Conduction losses for the IGBT

According to Fig. 5.25, during the transients some power is lost. The switching losses are not the only losses of a semiconductor switch. After transient is passed and the device reaches its steady state, some power are lost in form of heat, since the junction of switch has its own resistance and resistances dissipate energy in the form of heat according to $P = RI^2$ equation. Such a power loss is called conduction power loss.

Graph of collector current vs. collector-emitter voltage (for different junction temperatures) is shown in Fig. 5.43. We use this graph to model the conduction losses of the IGBT.

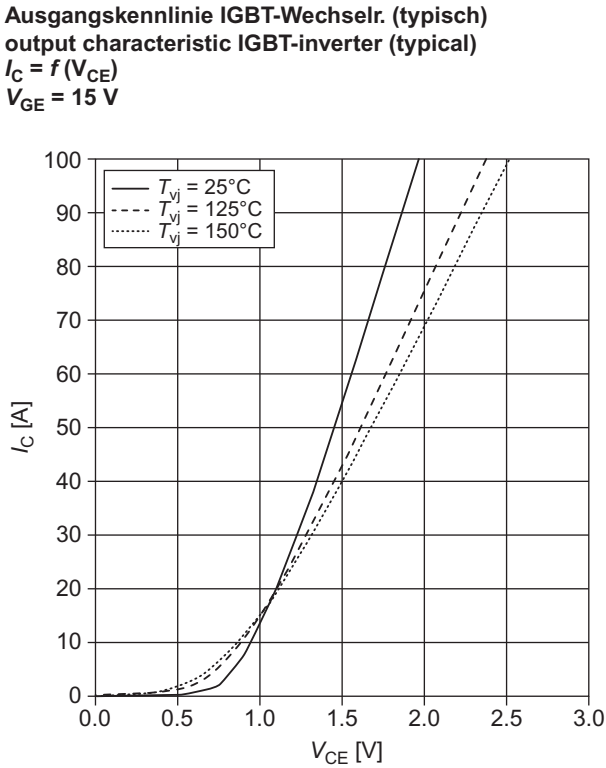


**FIG. 5.43** Graph of collector current versus collector-emitter voltage for different temperatures. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

Click the Conduction loss tab in order to start modeling the conduction losses (Fig. 5.44).

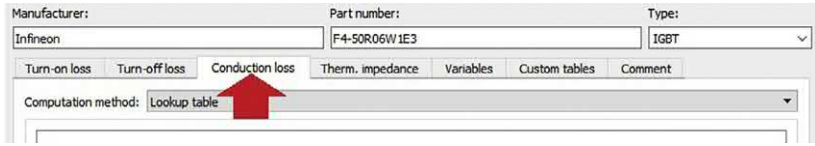


**FIG. 5.44** Conduction loss tab of thermal editor.

The data sheet provides the conduction losses for the IGBT for three different temperatures: 25°C, 125°C, and 150°C. Since the final junction temperature of the devices is not expected to exceed 125°C, it is sufficient to define the conduction losses at 25°C and 125°C (Fig. 5.45). You can enter the data for 150°C if you prefer to do so.

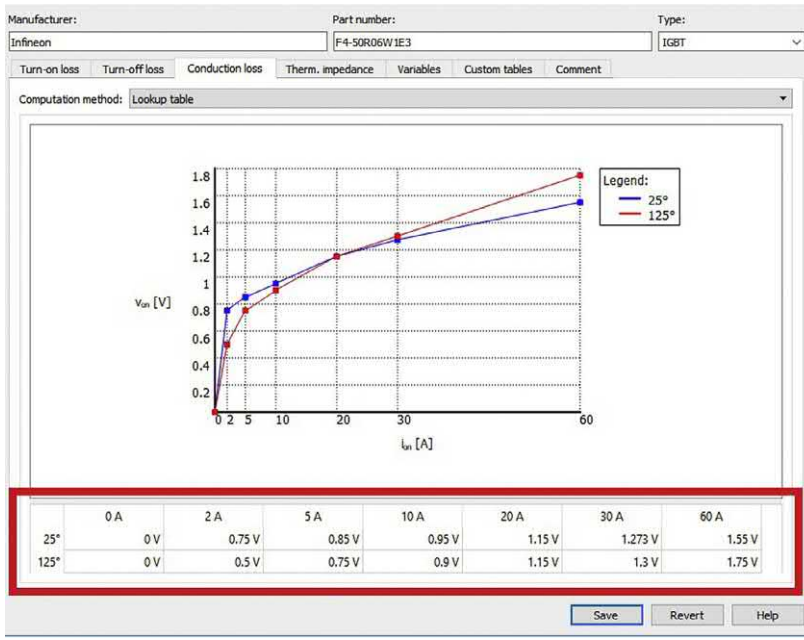


**FIG. 5.45** Collector-emitter voltage drop for different collector currents and junction temperatures.

## 5.7 Thermal impedances

The junction-case transient thermal impedance curves for the IGBT and diode are displayed in the data sheet along with the coefficients for a four-stage Foster network. The junction-case transient thermal impedance curve for the IGBT is shown in Fig. 5.46.

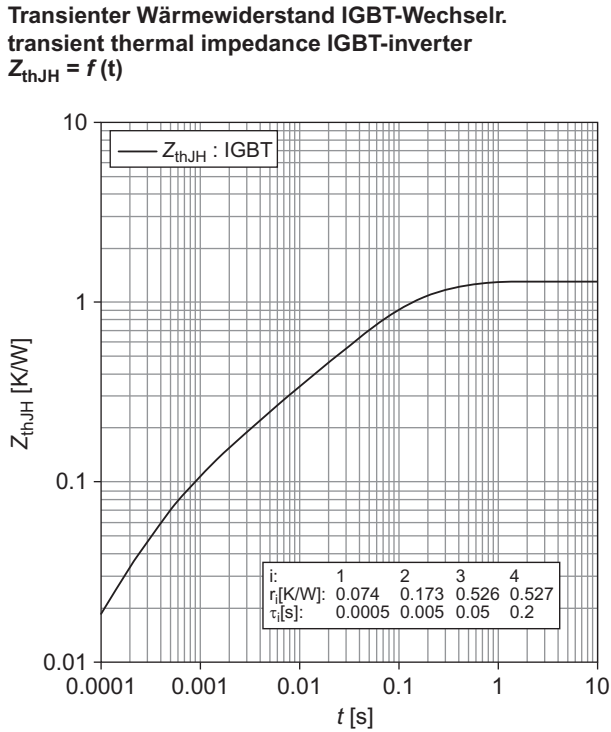


**FIG. 5.46** Thermal impedance graph of IGBT. Parameters of the fourth-order Foster network are given by datasheet. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

The Foster coefficients should not be used unless the case temperature of the device is held constant. Due to the series-connected capacitors in the Foster network, temperature variations at the case end of the chain are immediately propagated back to the junction end of the chain, rendering the transient response invalid.

If the case temperature is not constant, it is better to represent the junction-case thermal impedance using a first-order Cauer network as depicted in Fig. 5.47.

The resistance can be obtained directly from the thermal impedance curve. The transient thermal impedance curve corresponds in system theory to the step response and therefore contains the full thermal description of the system. The equation for the thermal resistance is:

$$Z_{th}(t) = \frac{T_{j1} - T_j(t)}{P_1},$$

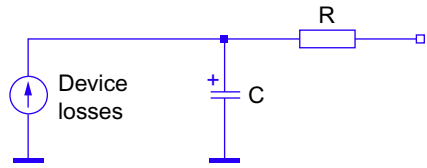


**FIG. 5.47** First-order Cauer thermal impedance network.

where $T_{j1}$ is a stationary temperature that the component is first heated to with a defined power dissipation $P_1$, and $T_{j1}(t)$ is the cooling temperature over time after the power dissipation is reduced to zero.

The transient thermal impedance curve for the diode is shown in Fig. 5.48. This curve is used to model the thermal impedance of the body diode.

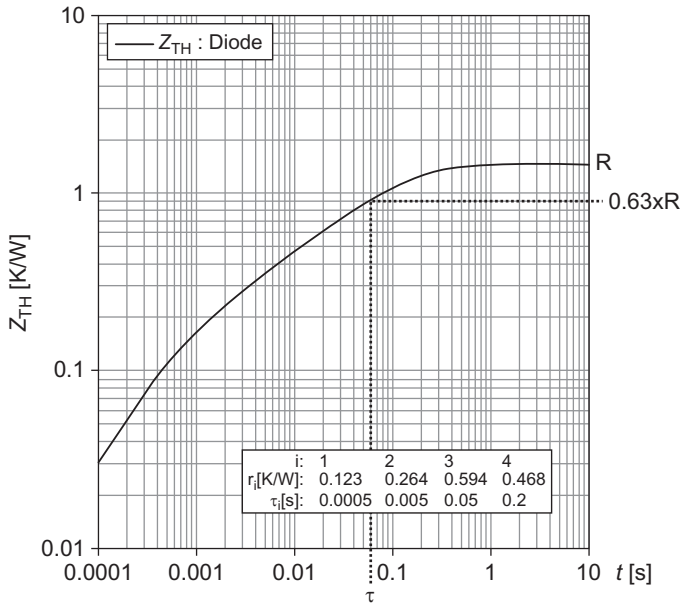


**FIG. 5.48** The transient thermal impedance curve for the body diode. Parameters of the fourth-order Foster network are given by datasheet. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

The capacitance is calculated using:

$$C = \frac{\tau}{R},$$

where $\tau$, the time constant, is measured as the time taken for the resistance to reach 63% of its final value (see Fig. 5.48).

Note: The Foster representation of a thermal impedance is a mathematical representation of a thermal impedance that bears no resemblance to a physical structure. The internal node voltages do not represent the temperature distribution in a real system, and to extend the network to accommodate a heat sink, all Foster coefficients for the entire thermal network would need to be recalculated. Internally, PLECS always uses the Cauer network to calculate the thermal transitions. Foster networks are converted to Cauer networks at simulation start. Strictly speaking, this conversion is only accurate if the temperature at the outer end of the network, i.e., the case, is held constant.

For practical purposes, the conversion should yield accurate results if the external thermal capacitance is much bigger than the capacitances within the network.

In order to enter the thermal impedance of IGBT, click the Therm. Impedance tab (Fig. 5.49). Enter the four Foster parameters provided by the datasheet (Fig. 5.46).

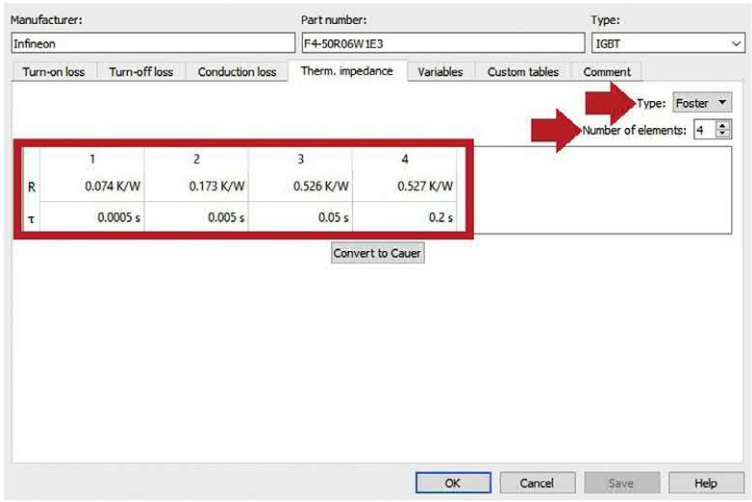


**FIG. 5.49** Entering the thermal impedance of IGBT. The numbers are entered according to Fig. 5.46.

## 5.8 Adding comments

You can add required comments by using the Comment tab. Enter the desired comments in the provided text box (Fig. 5.50).

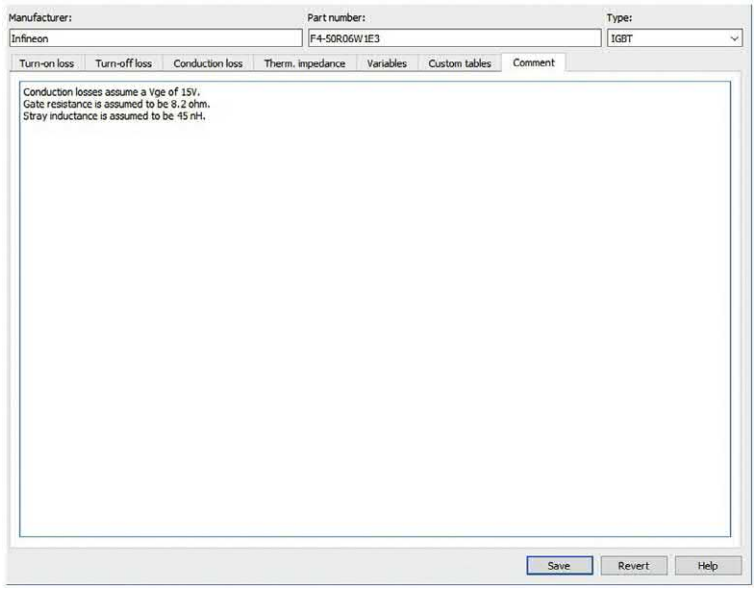


**FIG. 5.50** The comment tab of thermal editor can be used when you need to add comment to the produced model.

## 5.9 Saving the produced thermal model

The produced model can be saved with the aid of File menu (Fig. 5.51).

After Save is clicked, a window will appear, which permits you to save the

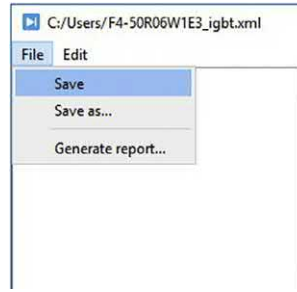


**FIG. 5.51** Use the File menu to save the produced model. You can click the Save button (see Fig. 5.50) in order to save the produced model as well.

produced model in the desired path of your computer. PLECS saves the file with .xml extension (Fig. 5.52).

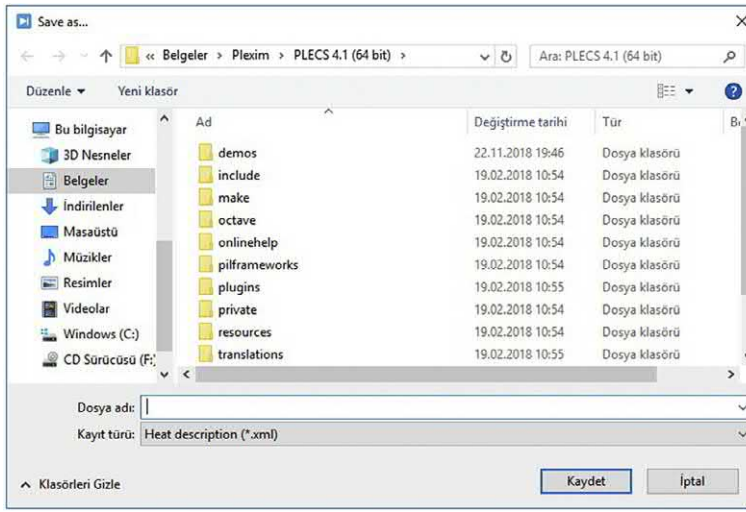


**FIG. 5.52** Save as window.

## 5.10 Adding the produced model to thermal search path of PLECS

After you saved the model, you must add it to thermal search path of PLECS. This lets you to use the produced model in your simulations easily and quickly. Click the PLECS Preferences in order to add the produced model to thermal search path of PLECS (Fig. 5.53).

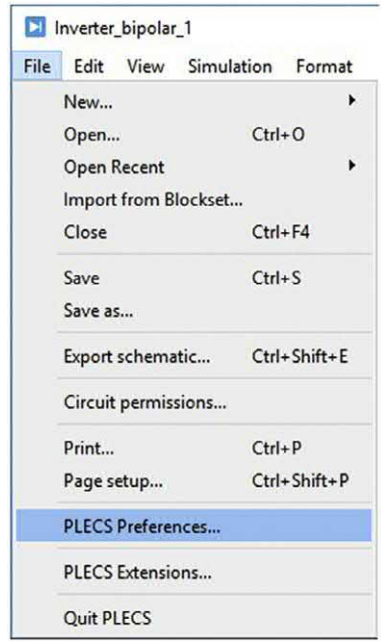


**FIG. 5.53** PLECS Preferences can be found in the File menu.

After you clicked the PLECS Preferences, the window shown in Fig. 5.54 will appear.

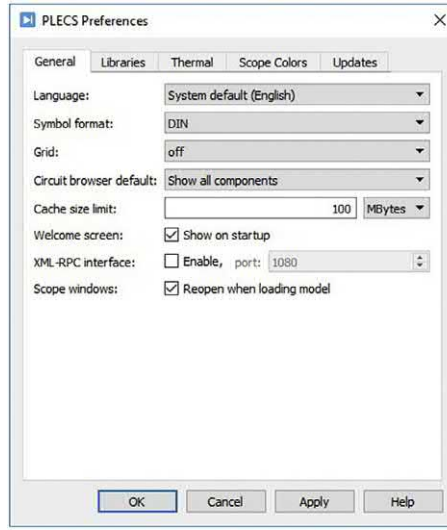


**FIG. 5.54** PLECS Preferences window.

Go to Thermal tab and then click the + button (Fig. 5.55).

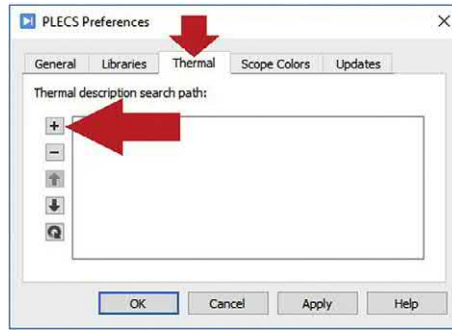


**FIG. 5.55** Thermal tab of PLECS Preferences window.

After you clicked the + button, PLECS opens the Select directory window. Go to the folder, which you saved the model and click the Select folder button in Select directory window. This adds the path of produced model to the thermal description search path of PLECS. There is no limitation on number of thermal descriptions in the thermal description search path. You can add as many as thermal models to the search path you want.

Once the model location is added to the thermal description search path of PLECS, you can add it to your simulations using the From library (Fig. 5.56).

Add the produced thermal model to IGBT1, IGBT2, IGBT3, and IGBT4 inside the subsystem model before proceeding.

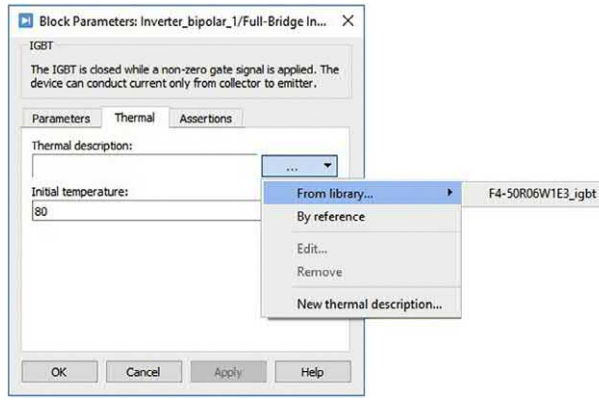


**FIG. 5.56** You can access the model after you add the produced model to Thermal description search path of PLECS.

## 5.11 Modeling losses of body diode

Up to now, we modeled the losses of IGBT. We must model the losses of body diode of IGBT as well. The process of modeling losses of diode is quite similar to the process of modeling losses of IGBT.

In order to model the losses of diodes, double click on one of the diodes inside the Full-bridge inverter subsystem. The window shown in Fig. 5.57 will appear.

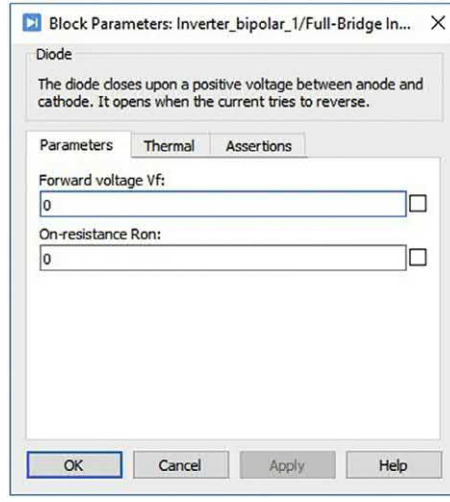


**FIG. 5.57** The diode settings.

Click the Thermal tab (Fig. 5.58).

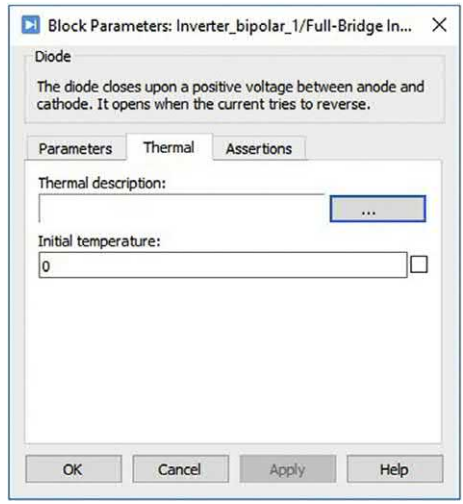


**FIG. 5.58** The Thermal tab of diode settings.

Click the Thermal description button and select the New thermal description (Fig. 5.59).

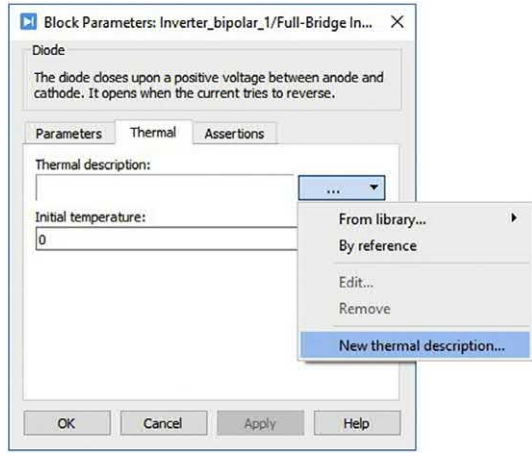


**FIG. 5.59** Use the New thermal description in order to define the diode losses.

The window shown in Fig. 5.60 will appear.

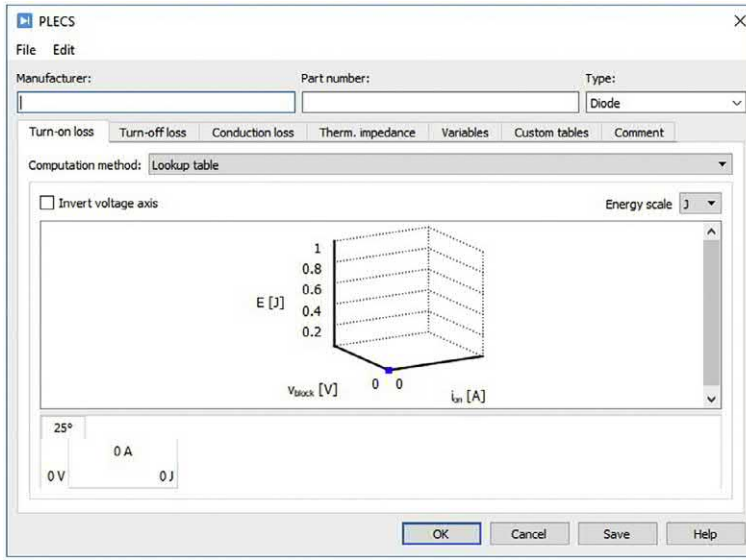


**FIG. 5.60** The thermal editor window.

You can enter the manufacturer name and part number in the Manufacturer and Part number boxes, respectively (Fig. 5.61).

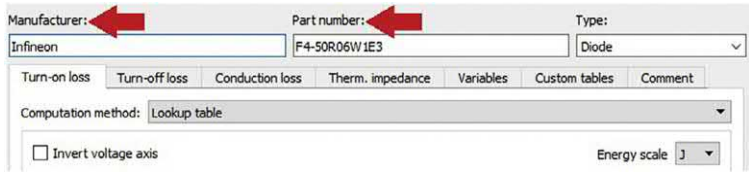


**FIG. 5.61** Entering the diode information.

### 5.11.1 The turn-on losses of body diode

Generally the turn-on losses of diode are negligible and can be ignored. The turn-off losses are important and must be modeled. So, you can ignore the turn-on loss and go to the Turn-off loss tab in order to start modeling the turn-off losses.

### 5.11.2 The turn-off losses of body diode

The turn-off losses curve for $V_{CE} = 300\,V$ is shown in Fig. 5.62. The losses are given for two junction temperatures, namely, 125°C and 150°C.

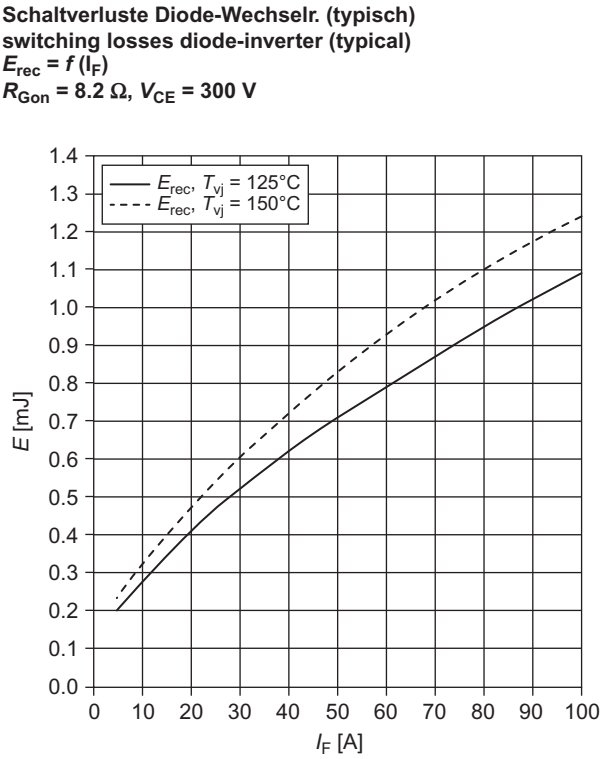


**FIG. 5.62** Turn-off switching losses of body diode for different junction temperatures and currents. $I_F$ shows the forward current of diode, i.e., the current from anode to cathode. The anode and cathode of body diode are connected to emitter and collector of IGBT, respectively. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

The turn-off tables are filled according to the curve shown in Fig. 5.62 (Figs. 5.63 and 5.64).

### 5.11.3 The conduction losses of body diode

The curve for conduction losses of body diode is shown in Fig. 5.65.

The conduction losses tables are filled according to curve shown in Fig. 5.65. Since the final junction temperature of the devices is not expected to exceed 125°C, it is sufficient to define the conduction losses at 25°C and 125°C (Fig. 5.66). You can enter the data for 150°C if you prefer to do so.

## 5.12 Thermal impedance of body diode

The thermal impedance of body diode is shown in Fig. 5.67.

The thermal impedance table of body diode is filled according to Fig. 5.67.

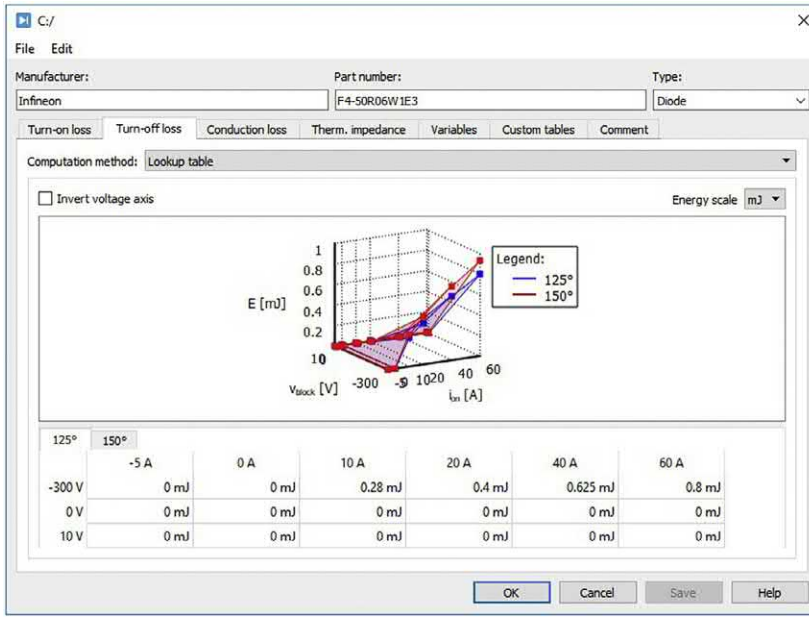


**FIG. 5.63** Turn-off switching losses for junction temperature of 125°C and different voltages ($V_{\text{anode}} - V_{\text{cathode}}$) and currents (current from anode to cathode).

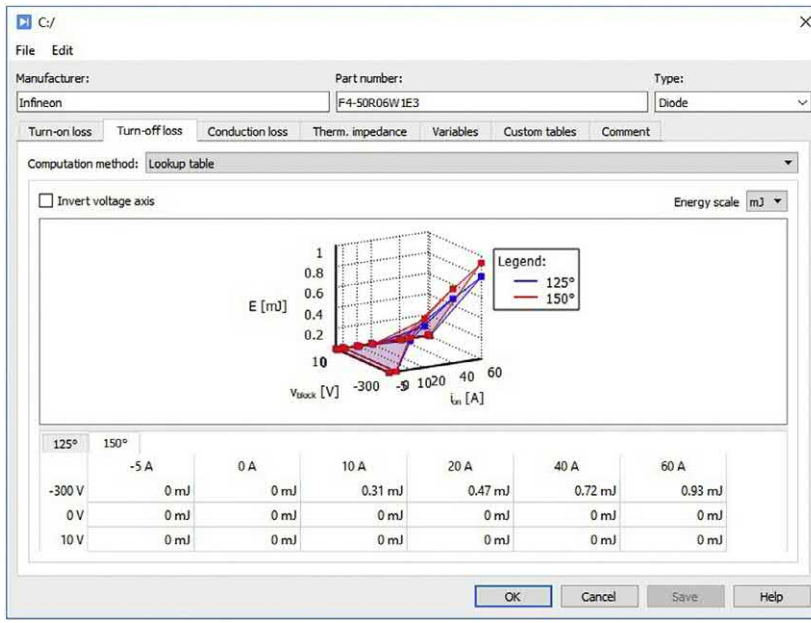


**FIG. 5.64** Turn-off switching losses for junction temperature of 150°C and different voltages ($V_{\text{anode}} - V_{\text{cathode}}$) and currents (current from anode to cathode).

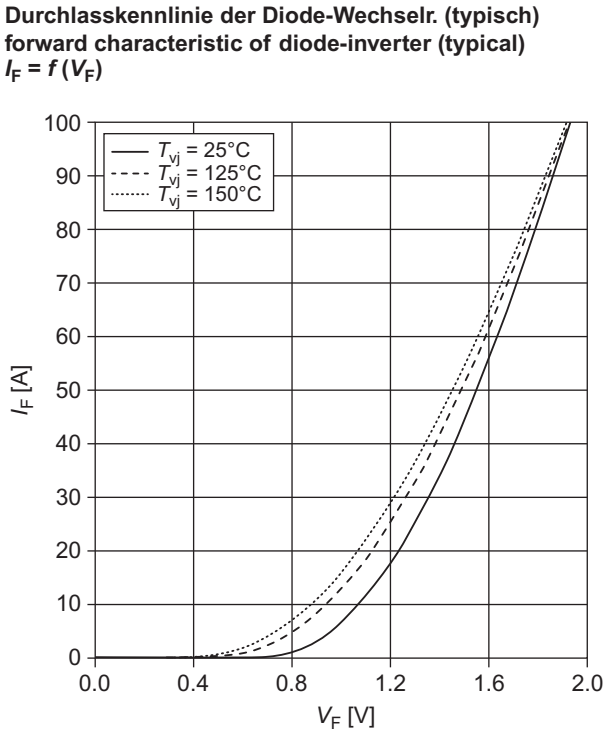


**FIG. 5.65** Graph of diode forward current (current from anode to cathode) versus diode forward ($V_{anode} - V_{cathode}$) voltage drop. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

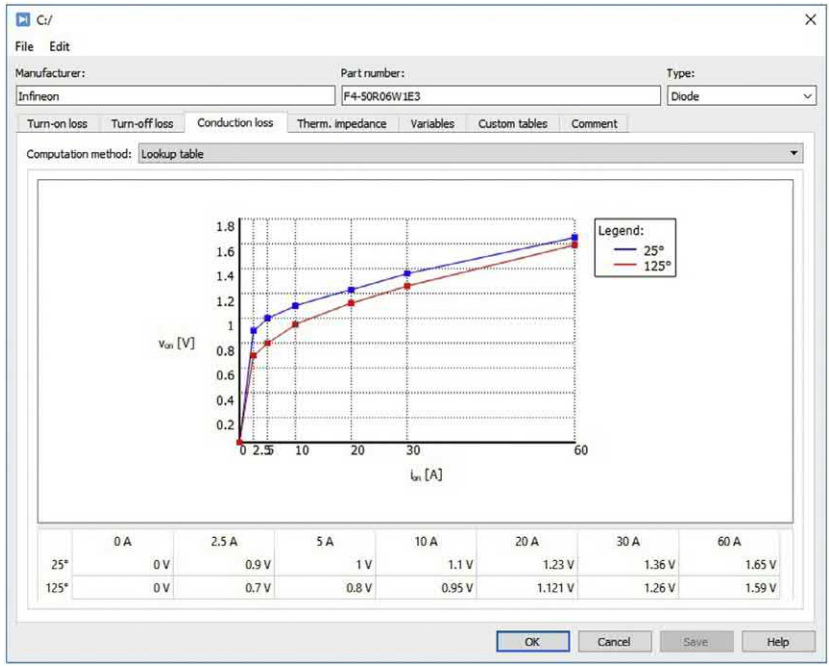


**FIG. 5.66** Entering the conduction loss of diode into the thermal editor.

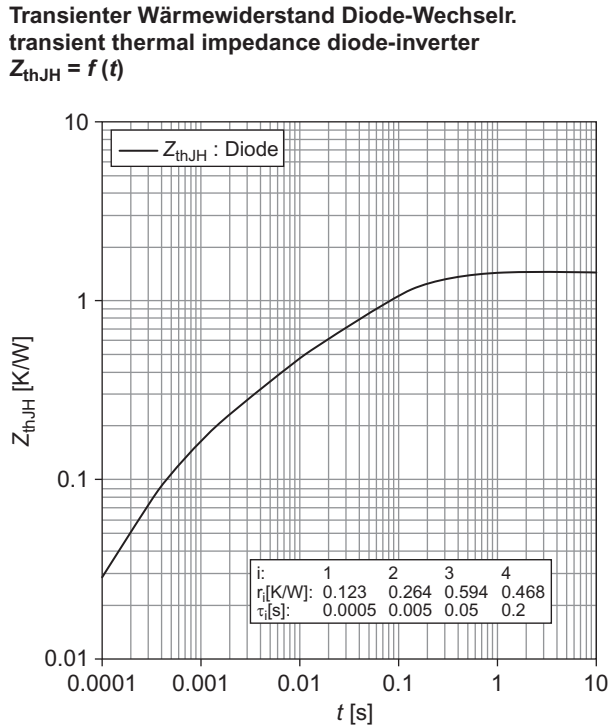


**FIG. 5.67** Thermal impedance of body diode. Parameters of the fourth-order Foster network are given by datasheet. *(Copyright with kind permission by Infineon Technologies AG, Germany.)*

Modeling of body diode losses is finished here (Fig. 5.68). Save the produced model in the desired path as an .xml file, add the path to thermal search path, and add the produced model to all the diodes, i.e., D1, D2, D3, and D4, inside the Full-Bridge Inverter subsystem.

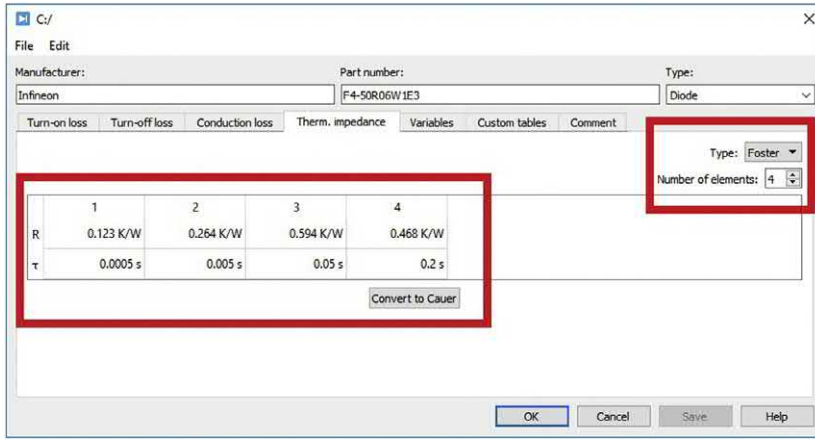


**FIG. 5.68** Entering the thermal impedance of body diode.

## 5.13 Loss measurements

We are ready to measure the inverter losses. As a starting point, assume a worst-case heat sink temperature of 80°C.

To set the heat sink temperature to this value, place a Heat Sink component (Fig. 5.69) over the Full-Bridge Inverter subsystem (Fig. 5.70). Set the heat sink thermal capacitance to 0 J/K (Fig. 5.71) and use a Constant Temperature (Grounded) thermal source component (Fig. 5.72) to set the heat sink temperature (Figs. 5.73 and 5.74). Also set the initial device temperatures to the same temperature as the initial heat sink temperature (by default the initial temperatures are 0°C).

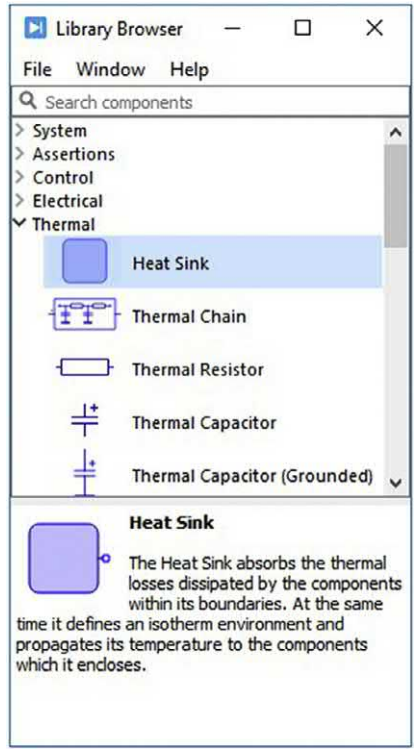


**FIG. 5.69** The Heat Sink block can be found in the Thermal section of Library Browser.

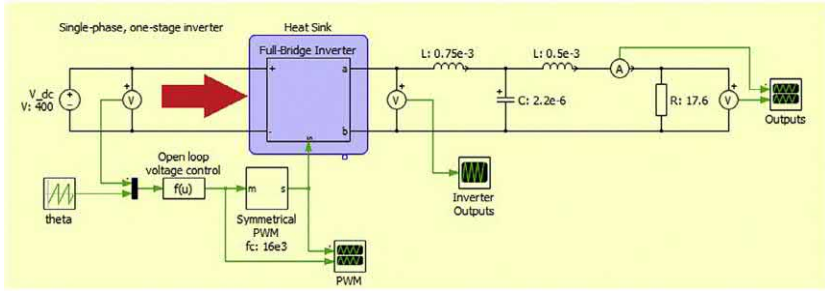


**FIG. 5.70** Addition of Heat Sink block to the schematic.

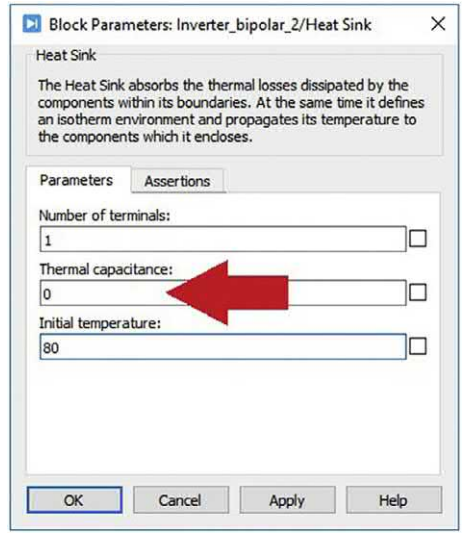


**FIG. 5.71** Double click on the heat sink block in order to set the thermal capacitance to zero. We are interested in the steady-state behavior, i.e., final values of temperatures, so the Thermal capacitance (which affects the transient behavior, not the steady-state behavior) is set to zero.

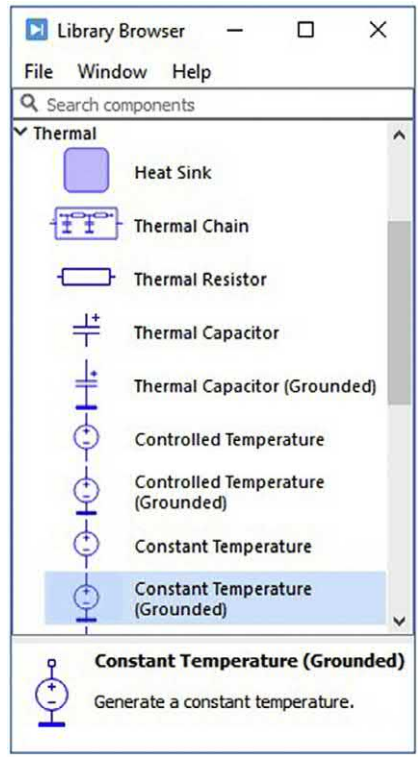


**FIG. 5.72** The Constant Temperature (Grounded) block can be found in the Thermal section of Library Browser.

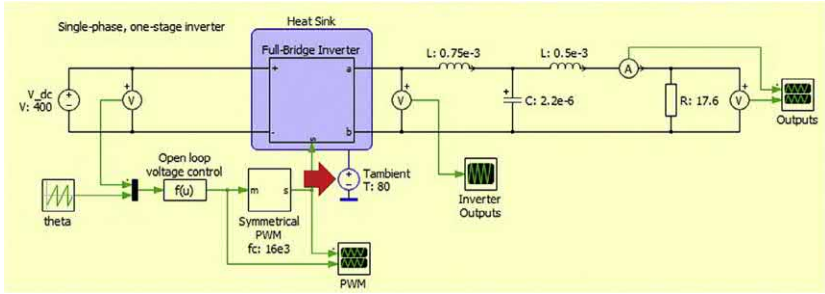


**FIG. 5.73** The Constant Temperature (Grounded) is connected to the Heat Sink block to keep its temperature constant.

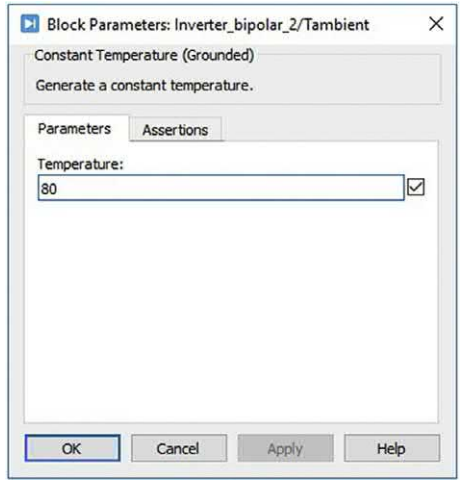


**FIG. 5.74** Settings of Constant Temperature (Grounded) block.

The semiconductor losses are measured with the aid of loss calculation subsystems added to the schematic (Figs. 5.75 and 5.76). The inside of loss calculation subsystems is studied next.

### 5.13.1 Calculation of IGBT's losses

Here, we study the blocks, which calculate the IGBT1 losses. These blocks are shown in Fig. 5.77. The blocks, which calculate the losses for other IGBTs, are composed of same blocks. So, they are not studied.

The input of Loss Calculation IGBT1 is a probe block (Fig. 5.78). The Probe block can be found at System section of Library Browser.

Add a Probe block to the schematic (Fig. 5.79).

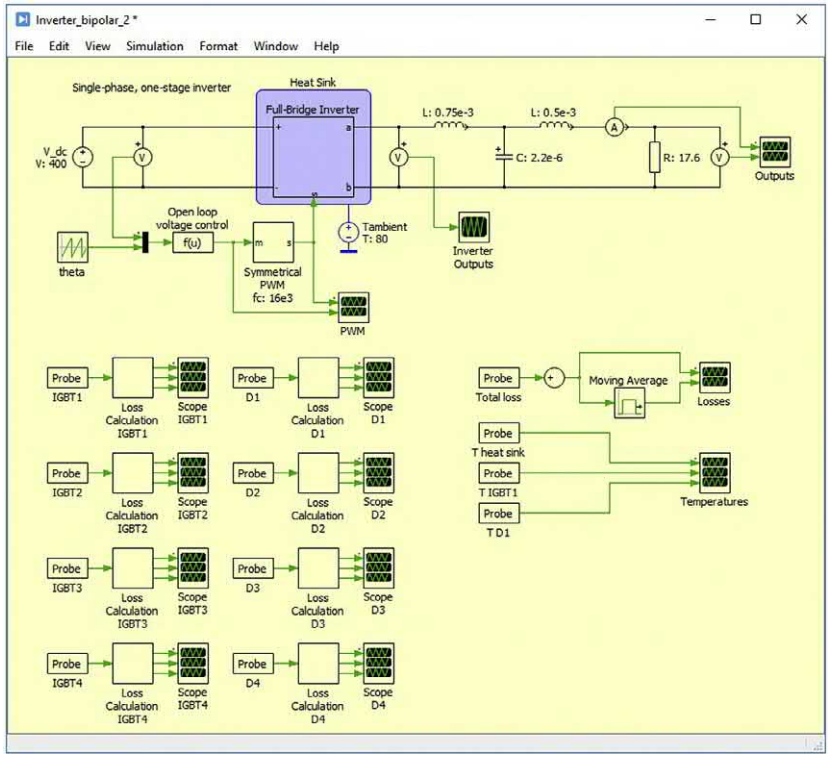


**FIG. 5.75** Loss calculation and monitoring blocks are added to the schematic.

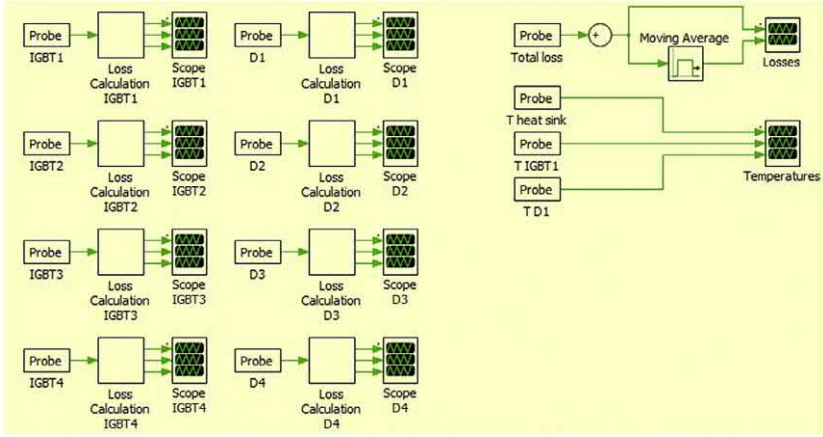


**FIG. 5.76** Close up of loss calculation and monitoring blocks.

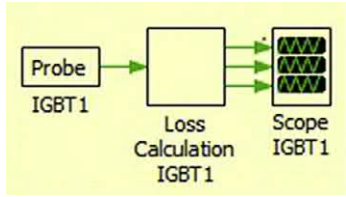


**FIG. 5.77** IGBT1 Probe block and Loss Calculation IGBT1 subsystem, measure the losses of IGBT1.

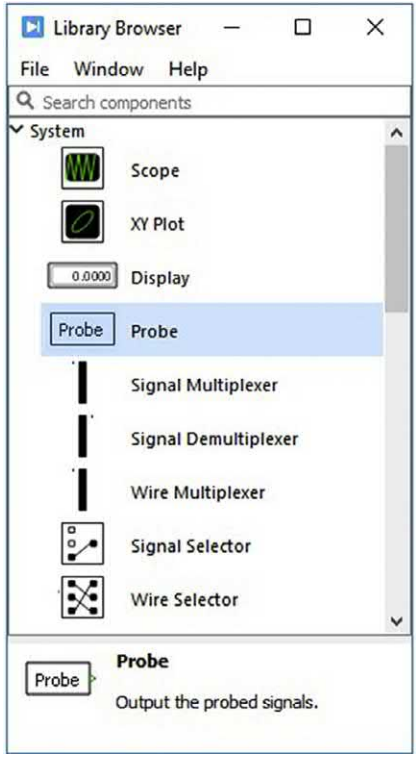


**FIG. 5.78** The Probe block can be found in the System subsection of Library Browser.

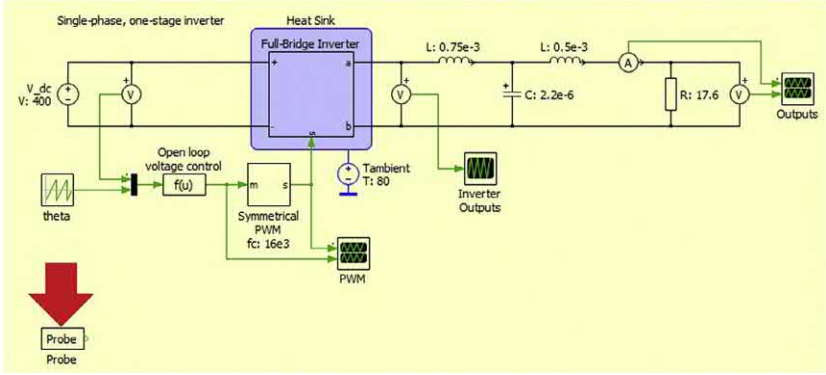


**FIG. 5.79** A Probe block is added to the schematic.

Double click on the text below the Probe block to change it to IGBT1 (Fig. 5.80).


**FIG. 5.80** Changing the Probe block label.

Open the Full-Bridge Inverter block. Drag and drop the IGBT1 inside the Full-Bridge Inverter block onto the probe block (Fig. 5.81).

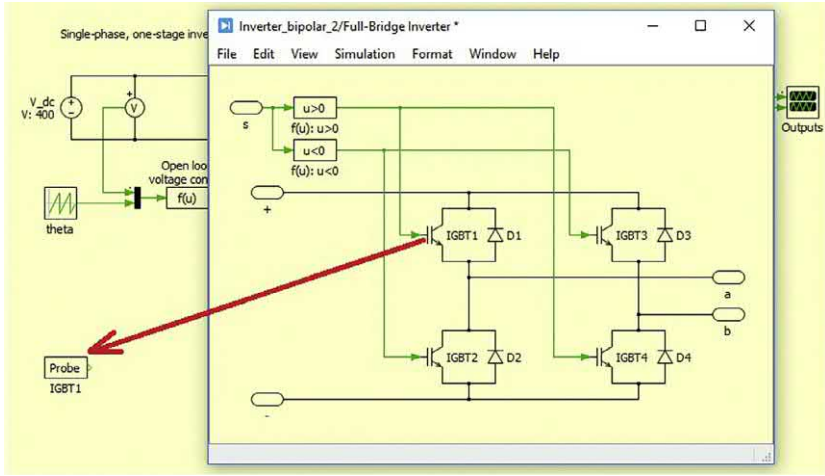


**FIG. 5.81** Drag and drop the IGBT1 from Full-Bridge Inverter subsystem onto the Probe block.

After you dropped the IGBT1 block onto the probe block, the window shown in Fig. 5.82 will appear.

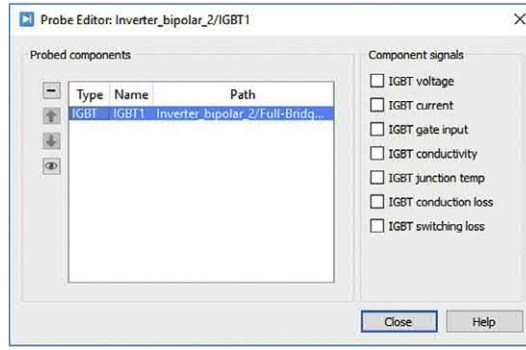


**FIG. 5.82** The IGBT1 Probe block.

Select the IGBT conduction loss and IGBT switching loss (Fig. 5.83). So, the output of Probe block will be IGBT1 conduction loss and IGBT1 switching loss. The summation of these two will give us the total loss for IGBT1.

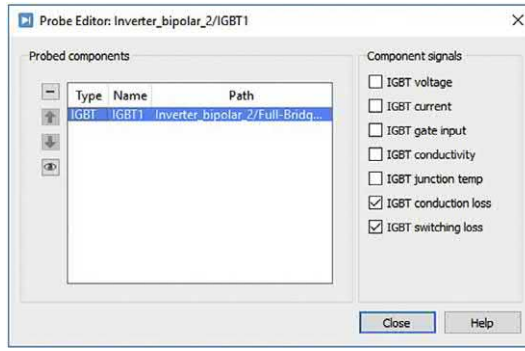


**FIG. 5.83** Select the IGBT conduction loss and IGBT switching loss.

The inside of Loss Calculation IGBT1 subsystem is shown in Fig. 5.84. Two average blocks are used in order to calculate the average values of losses.

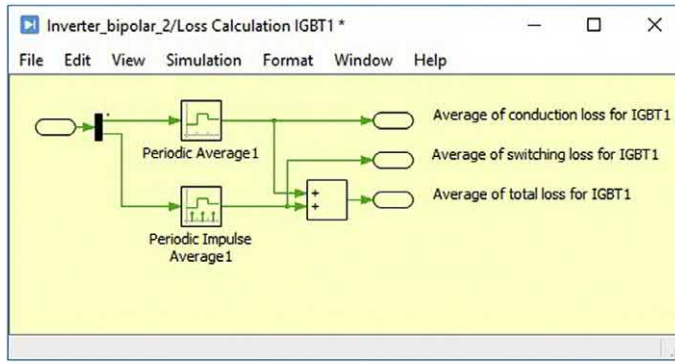


**FIG. 5.84** Calculation of average conduction loss, average switching loss, and total average loss (conduction loss + switching loss) for IGBT1.

The switching loss has an impulsive nature: It happens only when the switch status changes, i.e., when the on switch turns off or when the off switch turns on. So, we need to use the Periodic Impulse Average block in order to calculate the average of such a waveform. The conduction loss happens during the on period and its nature is not impulsive like the switching loss. So, average of conduction loss is calculated with a Periodic Average block.

The Periodic Average and Periodic Impulse Average can be found in the Filters section of Library Browser (Figs. 5.85 and 5.86).

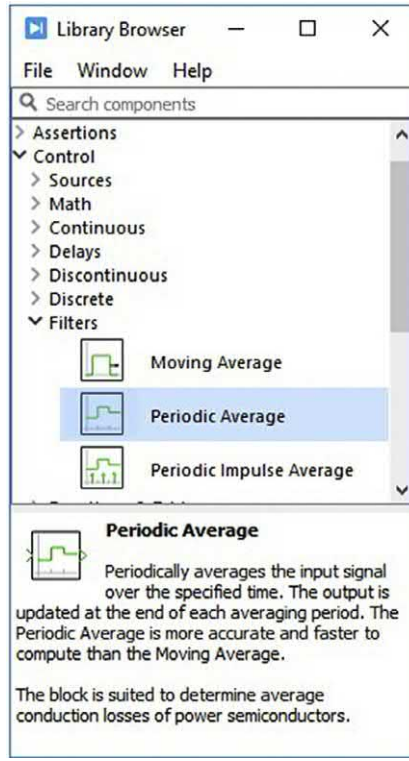


**FIG. 5.85** The Periodic Average block can be found in the Filters section of Library Browser.

The switching frequency is 16 kHz. So, the averaging time of Periodic Average and Periodic Impulse Average blocks must be set to $\frac{1}{16000} = 62.5\,\mu s$. Settings of Periodic Average and Periodic Impulse Average blocks are shown in Figs. 5.87 and 5.88, respectively.

### 5.13.2 Calculation of body diode's losses

The losses for diodes are calculated in the same way. Here, we study the calculation of losses for diode D1only. The calculation of losses for D2, D3, and D4 is the same. Fig. 5.89 shows the blocks, which calculate the losses of D1.

The Probe block settings are shown in Fig. 5.90.

The inside of Loss Calculation D1 subsystem is shown in Fig. 5.91. It is the same as Fig. 5.84.

### 5.13.3 Calculation of total losses

The losses of IGBT1, IGBT2, IGBT3, IGBT4, D1, D2, D3, and D4 are calculated individually. In order to obtain the total losses, the losses of four IGBTs

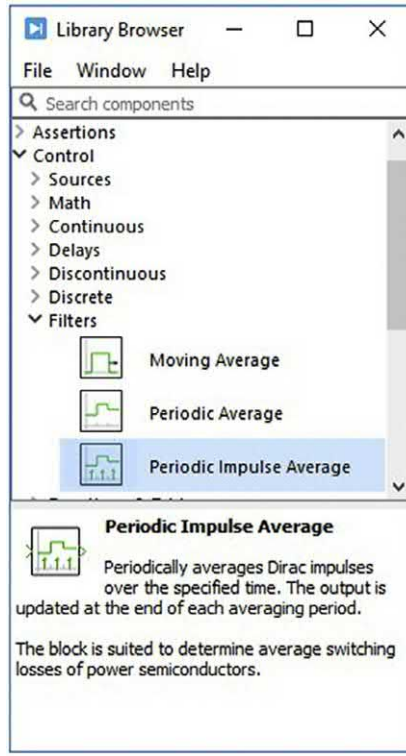


**FIG. 5.86** The Periodic Impulse Average block can be found in the Filters section of Library Browser.

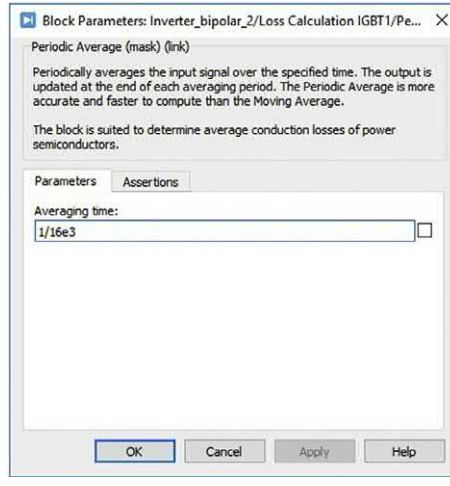


**FIG. 5.87** The Periodic Average block settings.

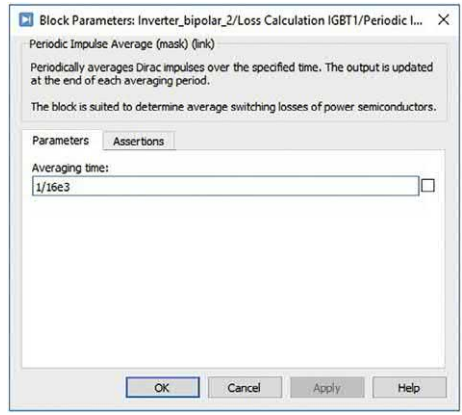


**FIG. 5.88** The Periodic Impulse Average block settings.

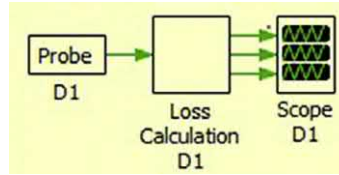


**FIG. 5.89** D1 Probe block and Loss Calculation D1 subsystem measure the losses of diode D1.

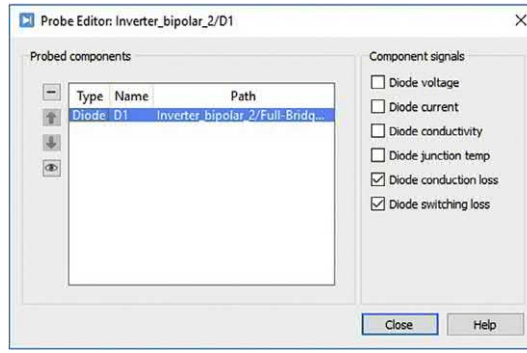


**FIG. 5.90** The D1 Probe block.

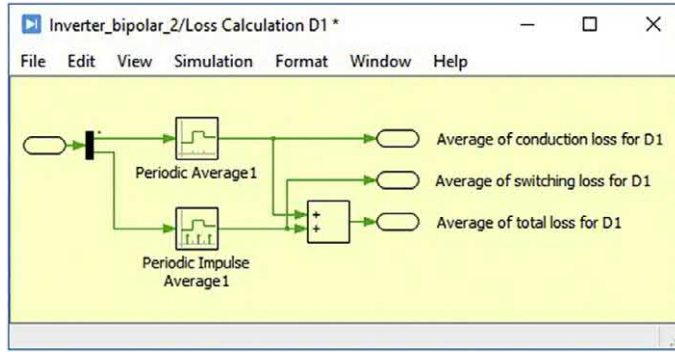


**FIG. 5.91** Calculation of average conduction loss, average switching loss, and total average loss (conduction loss+switching loss) for diode D1.

and for body diodes must be summed together. This is done with the aid of blocks shown in Fig. 5.92.

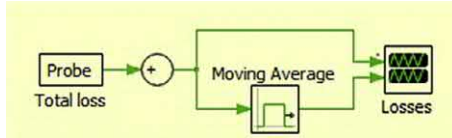


**FIG. 5.92** Calculation of overall total losses. The scope will show both the instantaneous and average losses.

In order to calculate the total losses, add a Probe block to the simulation and rename it to Total loss (Fig. 5.93).

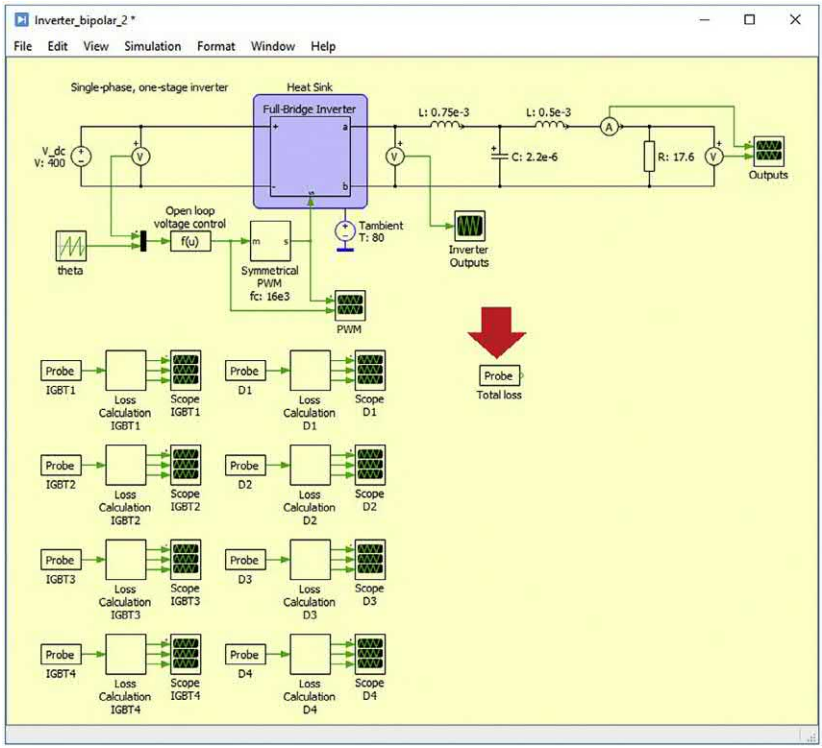


**FIG. 5.93** A probe named Total loss is added to the schematic.

Double click the Total loss Probe block in order to open it (Fig. 5.94).

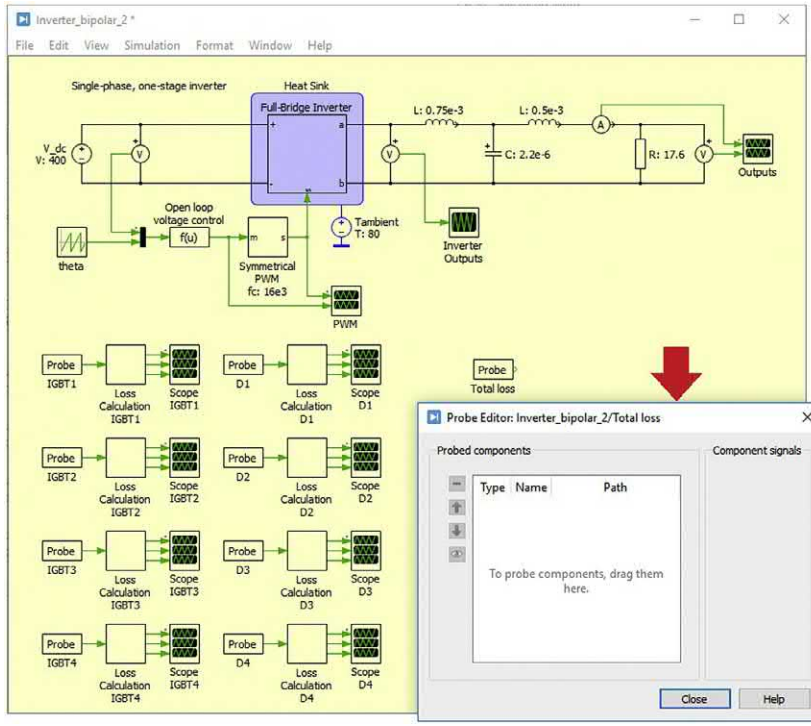


**FIG. 5.94** Total loss Probe block is opened.

Drag the Loss Calculation IGBT1, Loss Calculation IGBT2, Loss Calculation IGBT3, Loss Calculation IGBT4, Loss Calculation D1, Loss Calculation D2, Loss Calculation D3, and Loss Calculation D4 into the Total loss Probe block. Fig. 5.95 shows the Total loss Probe block after the drag and drops are finished.

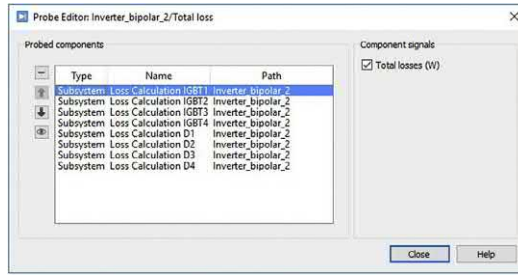


**FIG. 5.95** All the subsystems are drag and dropped onto the Total loss Probe block.

Connect the output of the Total loss Probe block to a summation block (Fig. 5.92). The settings of sum block are shown in Fig. 5.96. With these settings, the sum output will be the summation of all the 8 inputs.

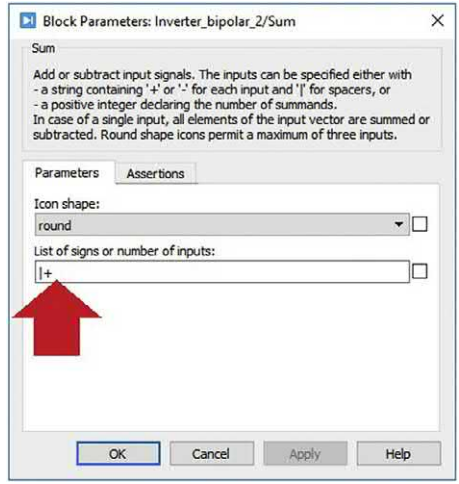


**FIG. 5.96** Sum block settings.

Add a Moving Average block to output of summer in order to calculate the average of power loss (Fig. 5.92). The settings of Moving Average block are shown in Fig. 5.97. In order to obtain the steady-state waveform, the Averaging time box must be filled with a large enough number, i.e., $k \times \frac{1}{f}$, where $f$ is switching frequency and $k > 100$ is a large number.

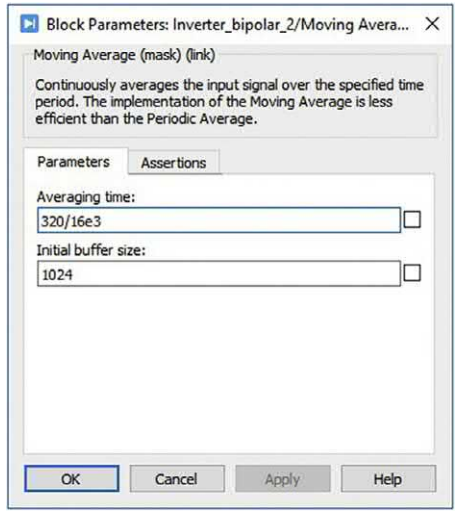


**FIG. 5.97** Moving average block settings.

## 5.14 Junction temperatures measurement

The junction temperatures can be seen with the aid of following blocks (Fig. 5.98).

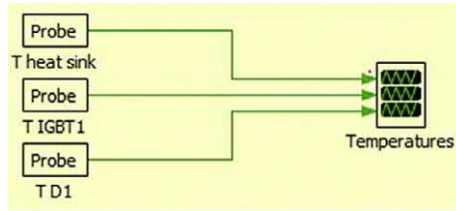


**FIG. 5.98** The blocks, which monitor the junction temperatures.

The Probe block settings are shown in Figs. 5.99–5.101.

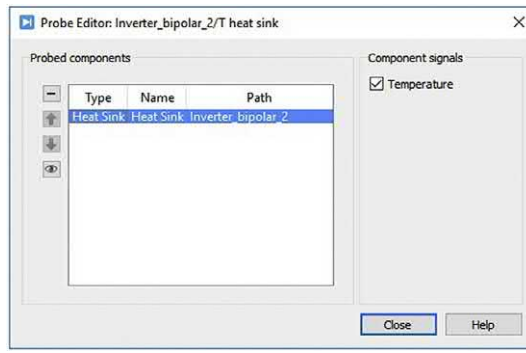


**FIG. 5.99** Drag and drop the heat sink into the T heat sink Probe block. Since the heat sink is connected to a Constant Temperature (grounded) block, its temperature keeps constant.

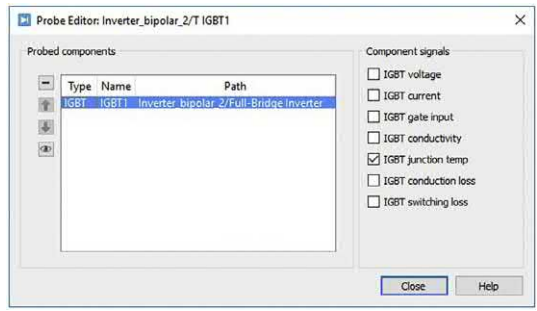


**FIG. 5.100** Drag and drop the IGBT1 into the T IGBT1 Probe block and select the IGBT junction temp to measure the junction temperature.

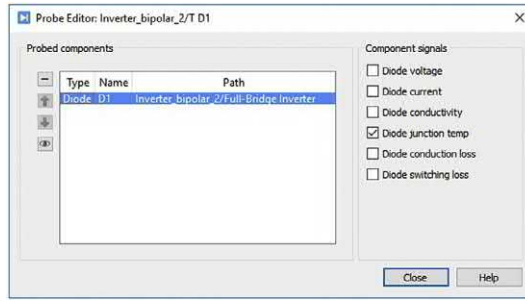


**FIG. 5.101** Drag and drop the D1 into the T D1 Probe block and select the Diode junction temp to measure the junction temperature.

## 5.15 Running the simulation

We are ready to run the simulation. Run the simulation with the settings shown in Fig. 5.102. The simulation results are shown in Figs. 5.103–5.109.

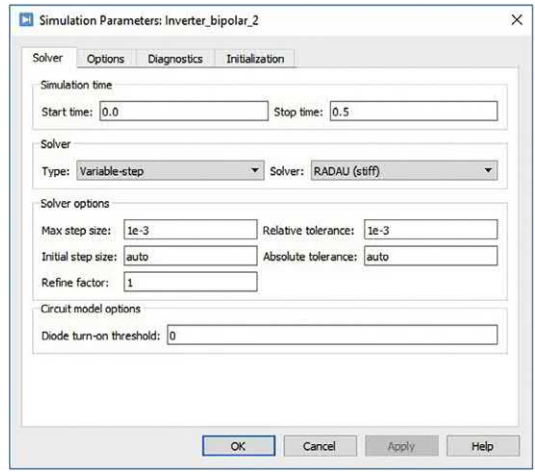


**FIG. 5.102** Simulation Parameters window.

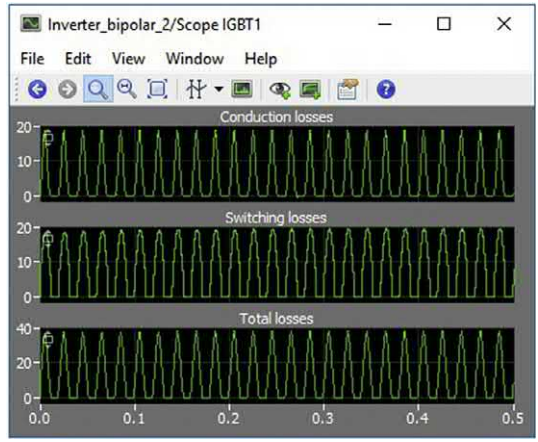


**FIG. 5.103** Conduction losses, switching losses, and total losses for IGBT1.

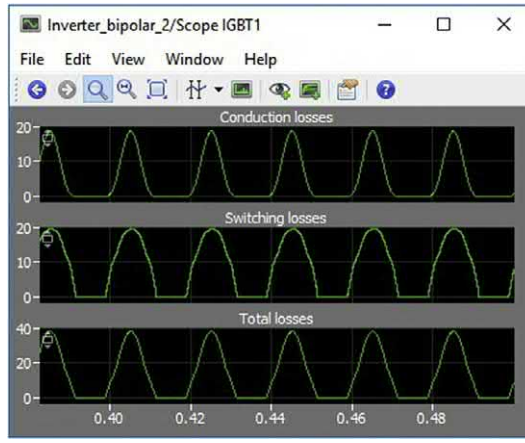


**FIG. 5.104** You can use the magnifier icon in order to get a closer look of waveforms shown in Fig. 5.103.

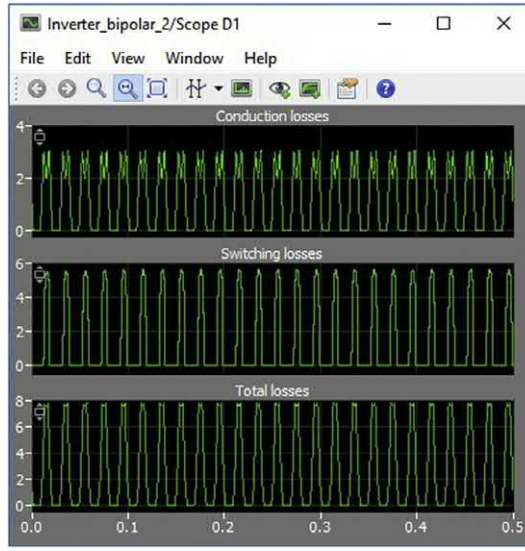


**FIG. 5.105** Conduction losses, switching losses, and total losses for diode D1.

According to Fig. 5.109, when the heat sink temperature is 80°C, the peak junction temperature of IGBTs is less than 125°C. So, the IGBT will not fail under this condition.


**FIG. 5.106** You can use the magnifier icon in order to get a closer look of waveforms shown in Fig. 5.105.

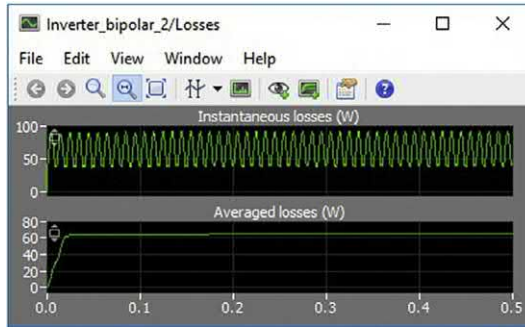


**FIG. 5.107** The instantaneous and average waveform of overall total losses of semiconductor switches (IGBT1, IGBT2, IGBT3, IGBT4, D1, D2, D3, and D4).

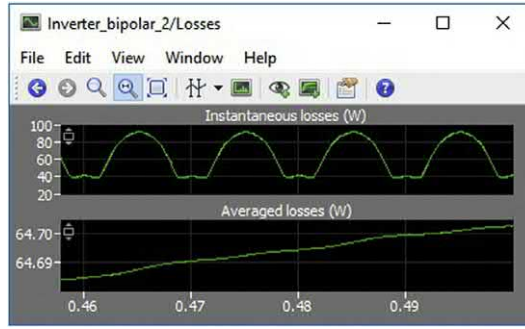


**FIG. 5.108** A closer look to the overall total losses of semiconductor switches.

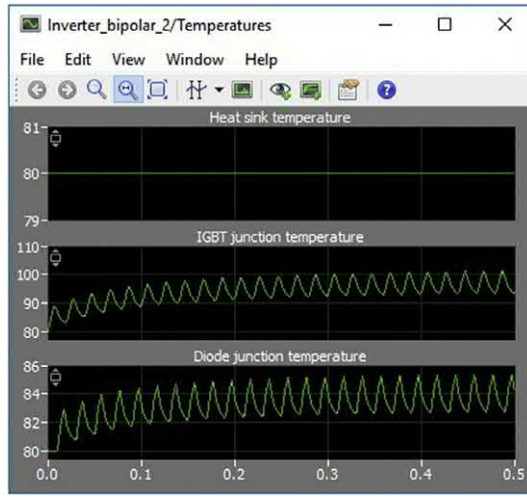


**FIG. 5.109** Junction temperature of IGBTs and diodes.

As an exercise, you can increase the value of the Constant Temperature (Grounded) block and obtain the maximum temperature, which limit the peak junction temperature to 125°C.

## 5.16 Designing the heat sink

Using the measured average power (Fig. 5.107), we can calculate the thermal resistance that is required to keep the heat sink temperature at or below 80°C by using the thermal power flow equation:

$$T_{\text{heat sink}} = T_{\text{ambient}} + P_{\text{loss}}.R_{\text{th}}$$

Assume that the ambient temperature is 40°C. According to Fig. 5.107, the average power loss is about 63 W. So, the thermal resistance needed to limit the maximum heat sink temperature to 80°C is:

$$80 = 40 + 63 \times R_{\text{th}} \Longrightarrow R_{\text{th}} = 0.635 \frac{^{\circ}C}{W}$$

Complete the thermal circuit by placing the calculated thermal resistance between the heat sink and ambient temperature source (Figs. 5.110, 5.111, and 5.112). Set the ambient temperature to 40°C (Fig. 5.113) and place a Heat Flow Meter block (Fig. 5.114) in series with the resistor to monitor the total thermal losses.

Set the heat sink capacitance to 10 J/K and set its initial temperature to 40°C (Fig. 5.115).

Note: The thermal capacitance is generally not calculated, but is dependent on the mass of the heat sink and the type of material. Thermal capacitance is not

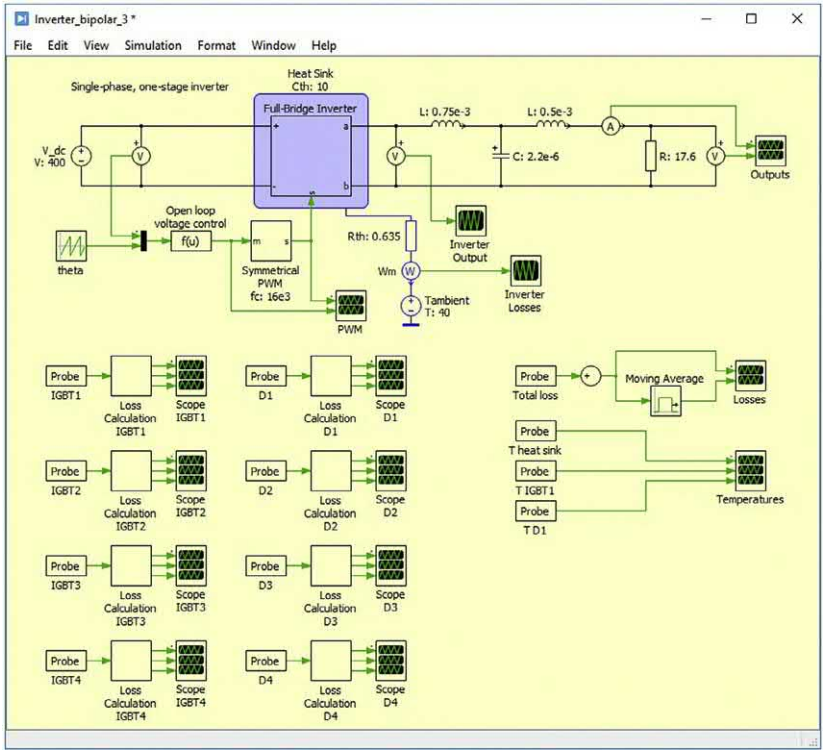


**FIG. 5.110** Thermal resistance of heat sink is considered in this added to the schematic.

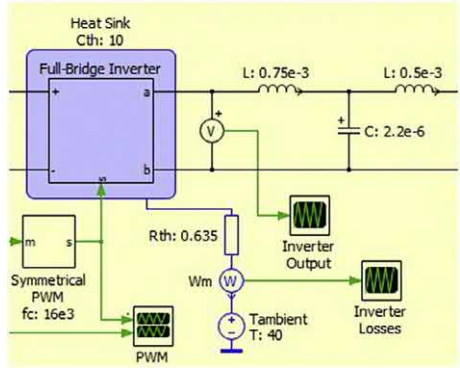


**FIG. 5.111** Closer look to blocks added to the schematic.

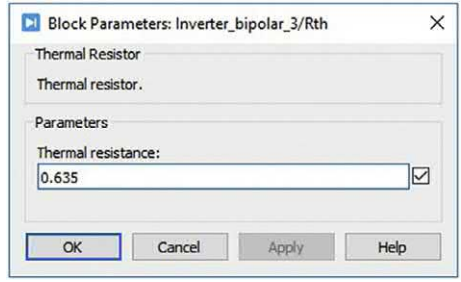


**FIG. 5.112** Thermal resistance of heat sink is set to 0.635°C/W.

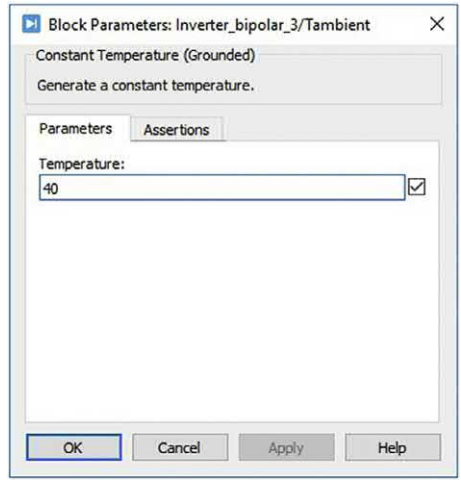


**FIG. 5.113** Ambient temperature is set to 40°C.

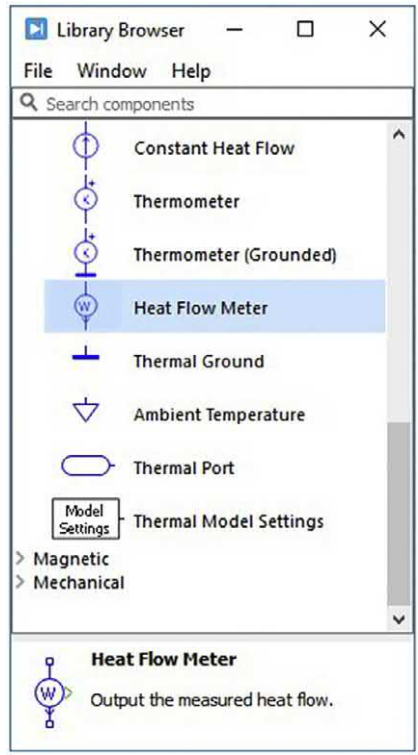


**FIG. 5.114** The Heat Flow Meter block can be found in the Thermal section of Library Browser.

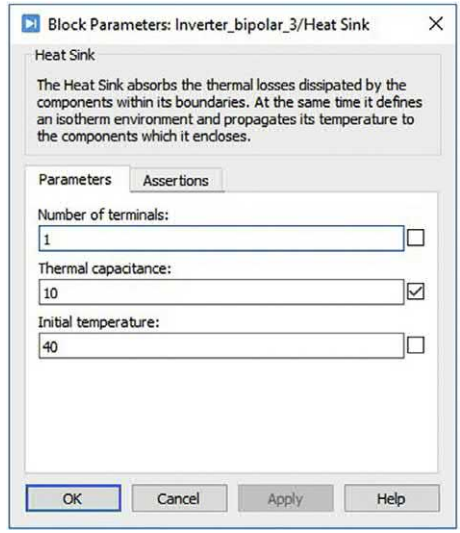


**FIG. 5.115** Double click the heat sink block in order to set its Thermal capacitance and Initial temperature.

as critical as thermal resistance because it is the thermal resistance that determines the steady-state operating temperature. The thermal capacitance, a measure of the heat storage ability of the heat sink, determines the rate of temperature rise during transient overload conditions.

We want to obtain the steady-state temperatures of junctions. You can use the Steady-State Analysis for this purpose. In order to do Steady-State Analysis, click the Analysis tools (Fig. 5.116).

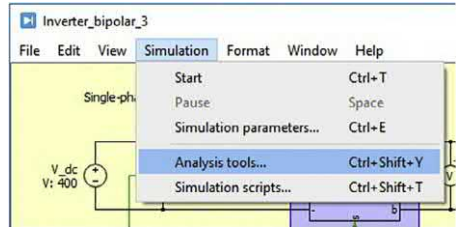


**FIG. 5.116** Click the Analysis tools in order to do Steady-State Analysis.

The window shown in Fig. 5.117 will appear. Click the + button.
After you clicked the + button, the window shown in Fig. 5.118 will appear.


**FIG. 5.117** The Analysis Tools window.

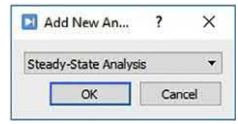


**FIG. 5.118** Add New Analysis window.

Click the OK button. After you clicked the OK button, the Analysis Tools window will appear. Do the setting as shown in Fig. 5.119.

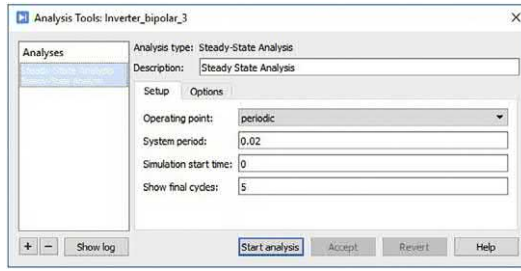


**FIG. 5.119** Analysis Tools window. Since the output frequency of inverter is 50 Hz, the system period is set to $1/50 = 0.02$ s.

Click the Start Analysis button in order to run the simulation. The simulation results are shown in Figs. 5.120–5.124.

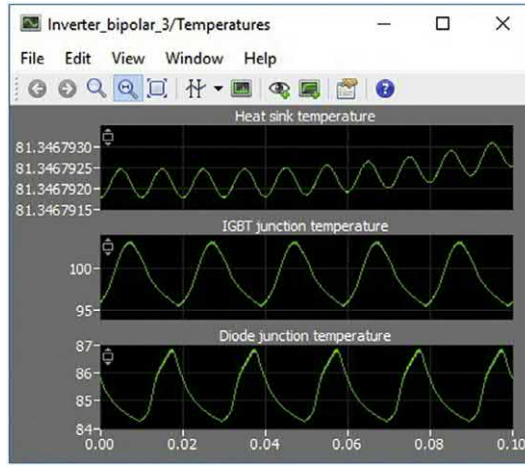


**FIG. 5.120** Temperatures of heat sink and junctions.

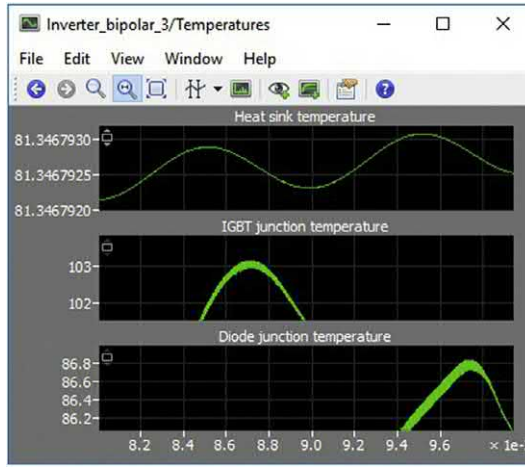


**FIG. 5.121** Closer look at Fig. 5.120. The junction temperatures are well below 125°C and the heat sink temperature is about 80°C.

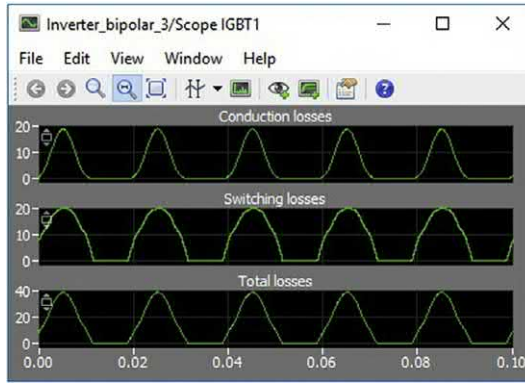


**FIG. 5.122** Losses for IGBT 1.


**FIG. 5.123** Losses for diode D1.

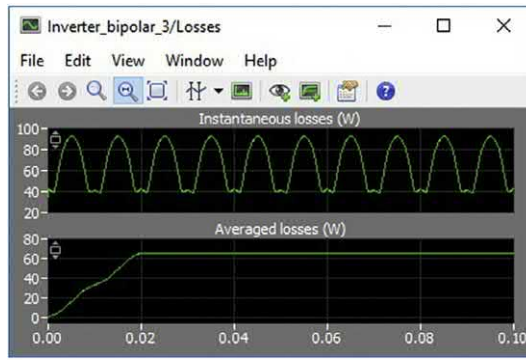


**FIG. 5.124** Graph of instantaneous and average losses.

## 5.17 Effect of modulation technique on losses

We used bipolar sinusoidal PWM technique in the previous sections of this chapter. In this section, we use unipolar sinusoidal PWM technique.

### 5.17.1 Review of unipolar PWM

With unipolar PWM, inverter legs A and B are switched separately. The switching signal for leg A is generated by comparing the modulation signal, $m_a$, with the triangular carrier signal. Similarly, the inverted modulation signal, $m_b$, is

compared with the triangular carrier to generate the switching signal for leg B (Fig. 5.125).

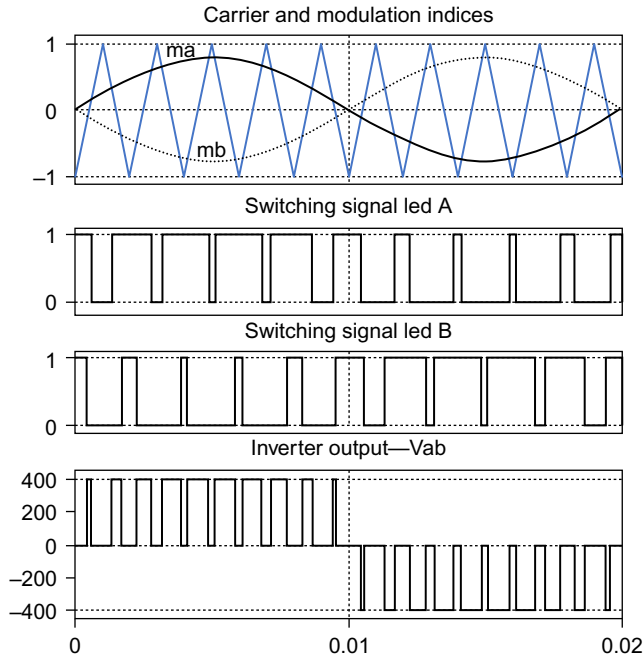


**FIG. 5.125** Unipolar modulation.

Compared with bipolar PWM, unipolar PWM has an additional switching state that creates a zero-output voltage. When both bottom or top switches in legs A and B are active, each inverter leg has the same output voltage and the total inverter output voltage, $V_{ab}$, is therefore 0 V. With this additional switching state, the output voltage has a three-level characteristic, having a value of $\pm V_{dc}$ or 0 $V$.

Unipolar PWM has a number of advantages over bipolar PWM. Due to the three-level output voltage, the change in voltage across the output filter is smaller, resulting in lower current ripple. In addition, the number of IGBTs that change state during a switching event is reduced from four to two, resulting in lower switching losses. For example, when switches S2 and S4 (Fig. 5.1) are on, creating an output of 0 V, the transition to an output of $V_{dc}$ is implemented by turning S1 on and S2 (Fig. 5.1) off. The state of S4 remains unchanged. In other words, the switch in the opposite leg retains its previous state.

Unipolar PWM does however have the drawback of generating a large common-mode voltage that can generate ground currents.

## 5.18 Calculation of losses for a unipolar PWM inverter

The schematic of previous bipolar inverter is changed as shown in Fig. 5.126. Only the modulation block is changed. The inside of Unipolar PWM subsystem block is shown in Fig. 5.127.

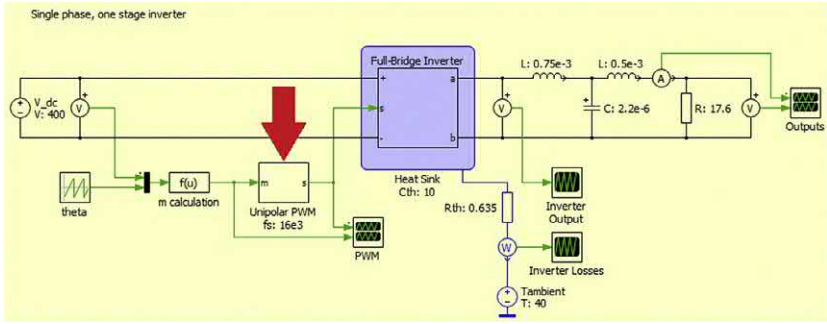


**FIG. 5.126** The bipolar PWM block is removed and a new subsystem is added to the schematic.

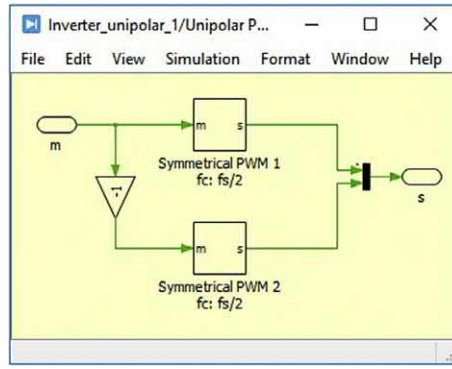


**FIG. 5.127** Inside of Unipolar PWM subsystem.

The settings of Symmetrical PWM 1 and Symmetrical PWM 2 blocks (Fig. 5.127) are shown in Figs. 5.128 and 5.129, respectively.

Run the Steady-State Analysis with the settings shown in Fig. 5.130.

The analysis results are shown in Figs. 5.131 and 5.132. As shown in Fig. 5.131, the losses decreased to about 40 W. The junction temperatures are decreased accordingly.

Here is the summary of this chapter: This chapter showed how to create a thermal description for IGBTs and diodes using data sheet values. The thermal design approach of choosing a worst-case heat sink temperature as the system reference point and measuring the semiconductor losses at this operating point allows the thermal resistance required to maintain this operating point to be calculated in a single step.

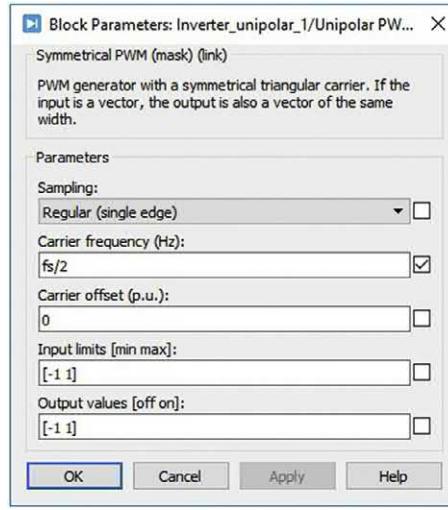


**FIG. 5.128** The Symmetrical PWM 1 (Fig. 5.127) settings, fs = 16 kHz.

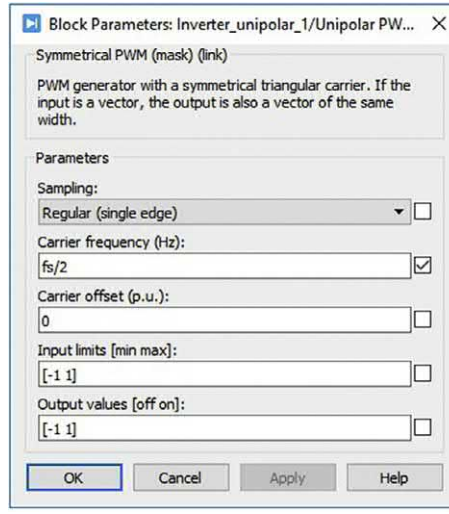


**FIG. 5.129** The Symmetrical PWM 2 (Fig. 5.127) settings, fs = 16 kHz.

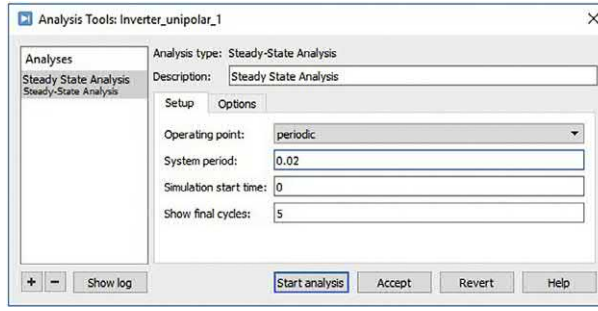


**FIG. 5.130** Analysis Tools window.

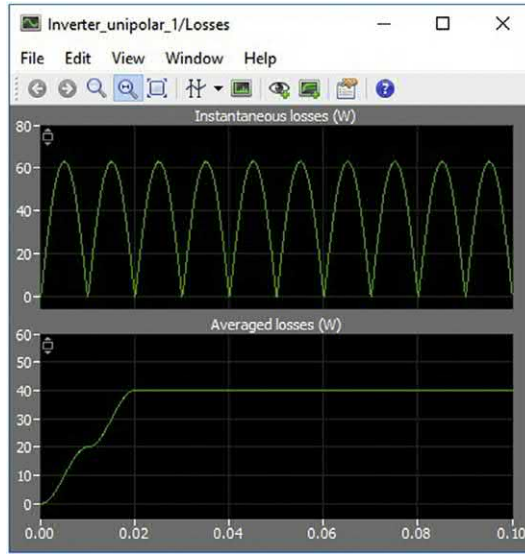


**FIG. 5.131** Graph of instantaneous and average losses.

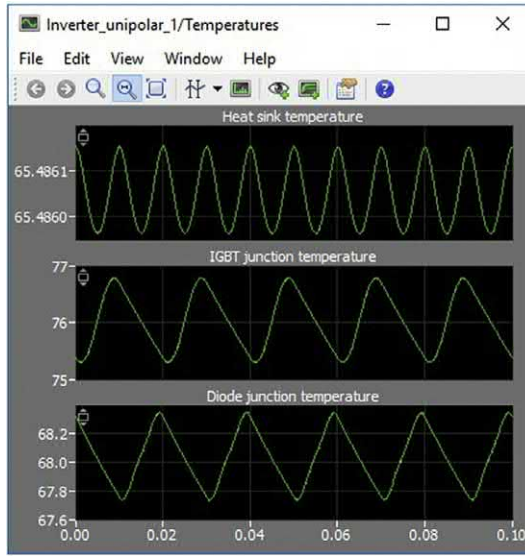


**FIG. 5.132** Temperatures of heat sink and junctions.

To set the peak device junction temperature rather than the heat sink temperature to a reference point, a few design iterations are required. Thermal simulations have other uses in addition to evaluating the thermal performance of a converter or assisting with the design of a thermal circuit. They are also useful

for making relative comparisons between converter losses when the modulation strategy or type of semiconductor switches is changed.

## Further reading

[1] M. Marz and P. Nance, Thermal modeling of power electronic systems, www.iisb.fraunhofer.de.
[2] S. Munk-Nielsen, L.N. Tutelea, U. Jaeger, Simulation with ideal switch models combined with measured loss data provides a good estimate of power loss, in: IEEE Industry Applications Conference, vol. 5, October 8–12, 2000, pp. 2915–2922.
[3] P. Jack, Holman, Heat Transfer, McGraw-Hill Education, 2009.
[4] Y. Cengel, A. Ghajar, Heat and Mass Transfer: Fundamentals and Applications, McGraw-Hill Education, 2014.

Chapter 6

# Extraction of power electronics converters uncertainties with PLECS®

## Chapter outline



## 6.1 Introduction

Modeling is the process of formulating a mathematical description of the system. A model, no matter how detailed, is never a completely accurate representation of a real physical system. A mathematical model is always just an approximation of the true, physical reality of the system dynamics.

Uncertainty refers to the differences or errors between model and real systems and whatever methodology is used to present these errors will be called an uncertainty model. Successful robust control-system design would depend on, to a certain extent, an appropriate description of the perturbation considered.

This chapter shows how PLECS® can be used to extract the uncertain model of power electronics converters. The chapter starts with a brief review of concept of uncertainty. After reviewing the concepts, an illustrative example (a Zeta converter) is studied. In this chapter, we will use the MATLAB® programming and commands of Robust Control Toolbox®. It is assumed that the reader is familiar with MATLAB® programming.


Simulation of Power Electronics Converters Using PLECS®. https://doi.org/10.1016/B978-0-12-817364-0.00006-0

## 6.2 Uncertainty models

Different uncertainty models are studied in this section. Studying Chapters 2 and 9 of [1] is recommended in order to obtain more information about modeling uncertainties of dynamical systems.

### 6.2.1 Parametric uncertainty

Inaccurate description of component characteristics, torn-and-worn effects on plant components, or shifting of operating points cause dynamic perturbations in many industrial control systems. Such perturbations may be represented by variations of certain system parameters over some possible value ranges. They affect the low-frequency range performance and are called "parametric uncertainties." Studying an example is quite helpful. Assume the simple RLC circuit shown in Fig. 6.1.

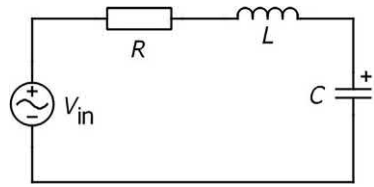


**FIG. 6.1** Typical RLC circuit.

The transfer function between the capacitor voltage and the input voltage can be written as:

$$\frac{v_c(s)}{v_{in}(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}} = \frac{a}{s^2 + bs + a},$$

where $a = \frac{1}{LC}$ and $b = \frac{R}{L}$. $R$, $L$, and $C$ can be written as $R = R_0 + \delta_R$, $L = L_0 + \delta_L$ and $C = C_0 + \delta_C$. $R_0$, $L_0$, and $C_0$ show the nominal values of resistor, inductor, and capacitor, respectively. $\delta_R$, $\delta_L$, and $\delta_C$ show component values variations, i.e., the effect of aging, measurement error, replacement of the components, etc.

$a$ and $b$ can be written in the same way as, $a_0 + \delta_a$ and $b_0 + \delta_b$, respectively. $a_0 = \frac{1}{L_0 C_0}$ and $b_0 = \frac{R_0}{L_0}$ show the nominal values of $a$ and $b$, respectively. According to the values of $R_0$, $L_0$, $C_0$, $\delta_R$, $\delta_L$, and $\delta_C$, $a$ and $b$ can be written as:

$$a_{min} < a < a_{max}$$

$$b_{min} < b < b_{max}$$

So, equation 1, no longer describe a single transfer function. It is a family of transfer functions with uncertain coefficients. It has parametric uncertainty.

### 6.2.2 Unstructured uncertainty

Many dynamic perturbations that may occur in different parts of a system can, however, be lumped into one single perturbation block $\Delta$, for instance, some unmodeled, high-frequency dynamics. This uncertainty representation is referred to as "unstructured" uncertainty. In the case of linear, time-invariant systems, the block $\Delta$ may be represented by an unknown transfer function matrix. The unstructured dynamics uncertainty in a control system can be described in different ways. The most famous ones are additive and input/output multiplicative perturbation configurations. If $G_p(s)$, $G_o(s)$, and $I$ show the perturbed system dynamics, a nominal model description of the physical system and identity matrix, respectively, then:

- Additive perturbation: $G_p(s) = G_o(s) + \Delta(s)$
- Input multiplicative perturbation: $G_p(s) = G_o(s) \times [I + \Delta(s)]$
- Output multiplicative perturbation: $G_p(s) = [I + \Delta(s)] \times G_o(s)$

In Single-Input Single-Output (SISO) systems, there is no difference between Input multiplicative perturbation and output multiplicative perturbation. In Multi-Input Multi-Output (MIMO) systems, the two descriptions are not necessarily the same.

It is a good idea to normalize the unknown transfer function $\Delta$, i.e., $\Delta = W\Delta_n$, such that $\|\Delta_n\|_\infty \leq 1$. $\|.\|_\infty$ shows the infinity norm of the transfer function. With such a normalized $\Delta_n$, the previous representations can be written as:

- Additive perturbation: $G_p(s) = G_o(s) + W_a(s)\Delta_n(s)$
- Input multiplicative perturbation: $G_p(s) = G_o(s) \times [I + W_m(s)\Delta_n(s)]$
- Output multiplicative perturbation: $G_p(s) = [I + W_m(s)\Delta_n(s)] \times G_o(s)$,

where $W_a(s)$ and $W_m(s)$ show the additive uncertainty weight and multiplicative uncertainty weight, respectively.

Assume that $G_{p1}(s)$, $G_{p2}(s)$, $G_{p3}(s)$, …, $G_{pn}(s)$ are $n$ samples of perturbed system dynamics (assume that $G_{p1}(s)$, $G_{p2}(s)$, $G_{p3}(s)$, …, $G_{pn}(s)$ are SISO systems). Then, in order to calculate the additive uncertainty weight $W_a(s)$, it is enough to find such a weight in which its magnitude is greater than $G_{p1}(s) - G_o(s)$, $G_{p2}(s) - G_o(s)$, $G_{p3}(s) - G_o(s)$, …, $G_{pn}(s) - G_o(s)$ for desired frequency range.

The multiplicative uncertainty weight $W_m(s)$ can be calculated in the same way. In this case, magnitude of $W_m(s)$ must be larger than $\frac{G_{p1}(s)-G_o(s)}{G_o(s)}, \frac{G_{p2}(s)-G_o(s)}{G_o(s)}, \frac{G_{p3}(s)-G_o(s)}{G_o(s)}, \ldots, \frac{G_{pn}(s)-G_o(s)}{G_o(s)}$ in the desired frequency range.

### 6.2.3 Structured uncertainty

In some problems, the uncertain parts can be taken out from the dynamics and the whole system can be rearranged in a standard configuration of (upper)

Linear Fractional Transformation $F(M, \Delta)$. The uncertian block $\Delta$ would then have the following general form:

$$\Delta = \text{diag}\{\delta_1 I_{r_1}, \delta_2 I_{r_2}, \delta_3 I_{r_3}, \ldots, \delta_s I_{r_s}, \Delta_1, \ldots, \Delta_f\}, \delta_i \in \mathbb{C}, \Delta_j \in \mathbb{C}^{m_j \times m_j},$$

where $\sum_{i=1}^{s} r_i + \sum_{j=1}^{f} m_j = n$ with n is the dimension of the block $\Delta$. So, $\Delta$ consist of s repeated scalar blocks and f full blocks. The full blocks need not be square. Since the $\Delta$ considered has a certain structure, such description is called structured.

## 6.3 Robust control

Robust control is a design methodology that explicitly deals with uncertainty. Robust control designs a controller such that:

- Some level of performance of the controlled system is guaranteed.
- Irrespective of the changes in the plant dynamics/process dynamics within a predefined class, the stability is guaranteed.

Some of the well-known robust control design techniques are studied briefly now.

### 6.3.1 Kharitonov's theorem

Kharitonov's theorem is used to assess the stability of a dynamical system when the physical parameters of the system are uncertain. It can be considered as a generalization of Routh-Hurwitz stability test. Routh-Hurwitz is concerned with an ordinary polynomial, i.e., a polynomial with fixed coefficients, while Kharitonov's theorem can study the stability of polynomials with uncertain (varying) coefficients.

Kharitonov's theorem is an analysis tool more than a synthesis tool. Kharitonov's theorem can be used to tune simple controllers such as PID. Designing high-order controllers using Kharitonov's theorem is not so common.

Refs. [2] and [3] are good references for control engineering applications of Kharitonov's theorem. Plenty of tools and related theorems are gathered there.

### 6.3.2 $H_\infty$ Control

$H_\infty$ techniques formulate the required design specifications (control goles) as an optimal control problem in the frequency domain. In order to do this, some fictitious weighting functions are added to the system model. Weighting functions are selected with respect to the required design specifications. Selection of weights is not a trivial task and requires some trial and error to obtain the desired specifications. In fact, the most crucial and difficult task in robust controller design is a choice of the weighting functions. Refs. [4–6] give very general

guidelines for selection of the weights. Refs. [7] and [8] used intelligent optimization methods (genetic algorithm) to find the best weighting functions.

The $H_\infty$ design does not always ensure robust stability and robust performance of the closed loop system. This is the main disadvantage of $H_\infty$ design techniques.

$H_\infty$ techniques are studied in many papers and books. Some of the well known are introduced here. Ref. [9] is the pioneering work of Zames, which introduced the $H_\infty$ control. Ref. [10] is a good tutorial paper on $H_\infty$ control with some numeric examples. Refs. [11] and [12] are general texts on robust control and studied the $H_\infty$ control in detail. Refs. [13] and [14] are good references to learn how to design $H_\infty$ controllers using MATLAB®.

### 6.3.3 μ Synthesis

The μ synthesis uses the D-K or μ-K iteration methods to minimize the peak value of the structured singular value of the closed-loop transfer function matrix over the set of all stabilizing controllers K. The structured singular value of a closed-loop system transfer matrix M(s), with uncertainty $\mathbf{\Delta}$ and singular values $\sigma$, is defined as:

$$\|M\|_\mu = \mu_\Delta{}^{-1}(M) := \overset{min}{\Delta\in\Delta}\{\overline{\sigma}(\Delta) : det(I - M\Delta) = 0\}^{\Delta\in\mathbf{\Delta}}$$

Usually the controller designed using the μ synthesis has a high order, which makes the implementation difficult. A model order reduction procedure is usually required.

The $H_\infty$ control design techniques consider the system uncertainty in the unstructured form, so the controller design using the $H_\infty$ techniques is conservative. The μ synthesis considers the uncertainty structures, so its output is less conservative.

## 6.4 Case study: A zeta converter

A power electronics converter is composed of passive components (i.e., capacitors and inductors), switches (i.e., MOSFET, IGBT, SCR, etc.), energy sources (i.e., Battery, AC grid, etc.), loads and some control strategy. Each component of the converter has its own variations and tolerances. Component variations come from different sources. For instance, value of a capacitor changes with temperature and aging. So, a power electronics converter can be considered as an uncertain dynamical system.

In this section, we will show how you can use PLECS® to extract the uncertain dynamical model of a Zeta converter. We will extract the nominal dynamical model first (component changes are neglected). Effect of components changes on dynamical behavior will be studied next.

You can extract the uncertain model of other types of converters in the same way shown in this chapter.

### 6.4.1 Analyzing the system without uncertainty

The schematic shown in Fig. 6.2 is used to extract the $\frac{v_o(s)}{d(s)}$ transfer function (i.e., the control-to-output transfer function). Nominal values of components are shown in Table 6.1.

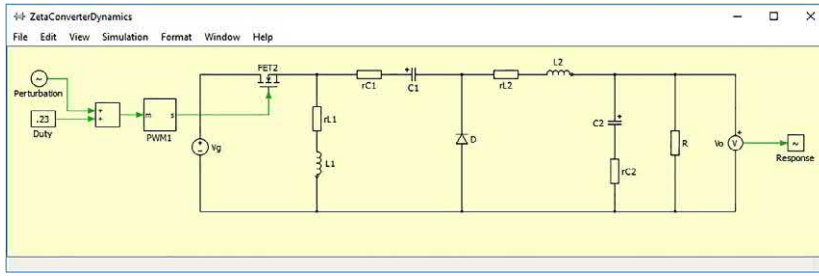


**FIG. 6.2** Extraction of the $\frac{v_o(s)}{d(s)}$ transfer function Bode diagram for the studied Zeta converter.

**TABLE 6.1** Nominal values of Zeta converter parameters (see Fig. 6.2).

| | Nominal value |
|---|---|
| Input DC source voltage, Vg | 20 V |
| MOSFET Drain-Source resistance, rds | 10 mΩ |
| Capacitor, $C_1$ | 100 μF |
| Capacitor $C_1$ Equivalent Series Resistance(ESR), $rC_1$ | 0.19 Ω |
| Capacitor, $C_2$ | 220 μF |
| Capacitor $C_2$ Equivalent Series Resistance(ESR), $rC_2$ | 0.095 Ω |
| Inductor, $L_1$ | 100 μH |
| Inductor ESR, $rL_1$ | 1 mΩ |
| Inductor, $L_2$ | 55 μH |
| Inductor ESR, $rL_2$ | 0.55 mΩ |
| Diode voltage drop, vD | 0.7 V |
| Diode forward resistance, rD | 10 mΩ |
| Load resistor, R | 6 Ω |
| Switching Frequency, Fsw | 100 Hz |
| Duty ratio | 0.23 |

The "Small Signal Perturbation" and "Small Signal Response" blocks (Fig. 6.3) are added to suitable places in order to extract the small signal transfer function from perturbation of duty ratio to the perturbation of the output voltage.

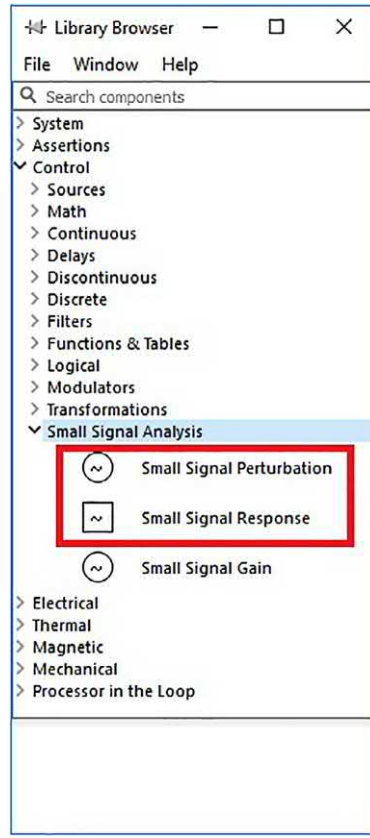


**FIG. 6.3** "Small Signal Perturbation" and "Small Signal Response" blocks.

You can double click each component and enter its value like the previous chapters. However, use of Initialization tab of Simulation Parameters window (Fig. 6.4) is recommended in this chapter. As you will see, this simplifies the tasks considerably.

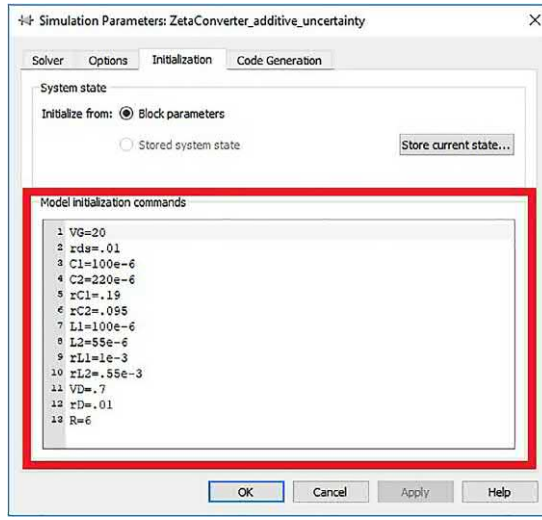


**FIG. 6.4** Simulation Parameters window appear when you click the Simulation Parameters … in the Simulation menu. rds,VD, and rD show the Drain-Source resistance of closed MOSFET, voltage drop of forward-biased diode, and series resistance of forward-biased diode, respectively.

After variables are defined in the Model initialization commands section of Simulation Parameters window (Fig. 6.4), you must double click each component inside the schematic editor and enter the corresponding variable into it. For instance, variable named R is used to define the output load value. You must double click the output load and write R in its resistance box in order to tell PLECS® that R is used for output load (Fig. 6.5).

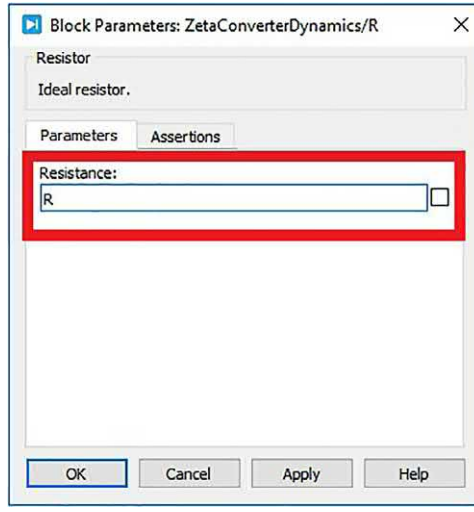


**FIG. 6.5** Double click the output load and write R in the Resistance box in order to tell PLECS® that variable R is used to represent the output load. Variable R value is 6 Ω (see Fig. 6.4).

The PWM signal is produced with the aid of a "Sawtooth PWM" block (Fig. 6.6). Fig. 6.7 shows the settings of the "Sawtooth PWM" block used in Fig. 6.2.

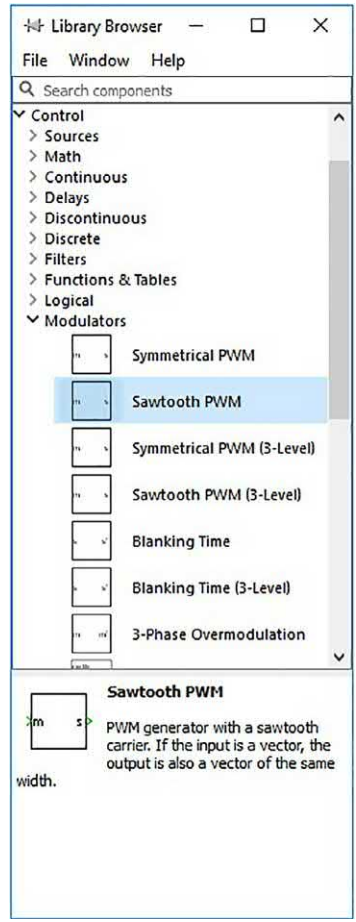


**FIG. 6.6** "Sawtooth PWM" block.

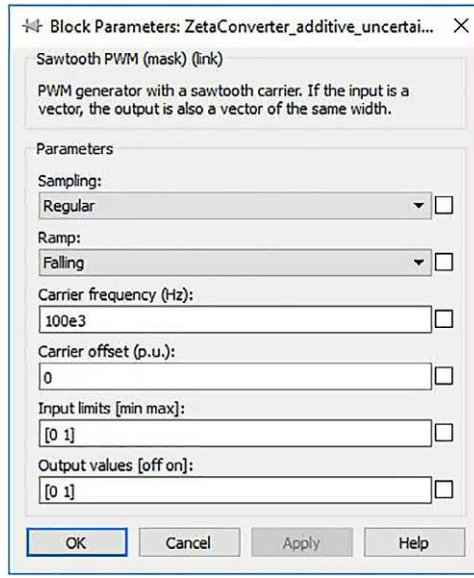


**FIG. 6.7** Settings of the "Sawtooth PWM" block used in Fig. 6.2.

Click the "Analysis tools…" in order to obtain the converter small signal transfer function (Figs. 6.8 and 6.9).

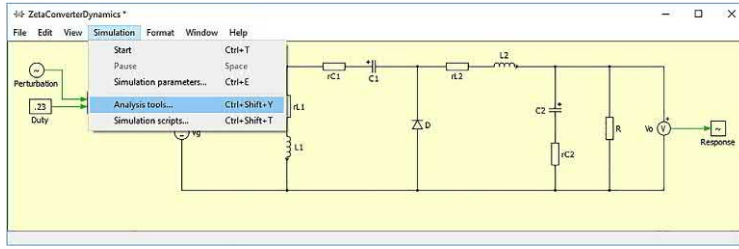


**FIG. 6.8** Click "Analysis tools…" in order to open the "Analysis Tools" window.

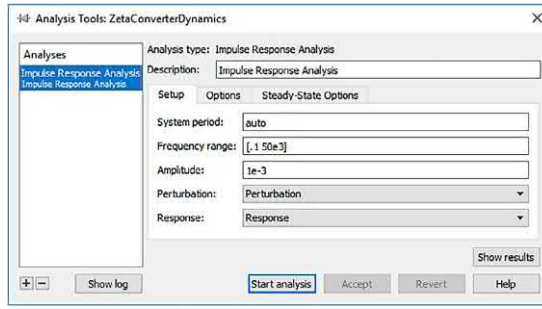


**FIG. 6.9** The desired frequency range is entered into the "Frequency range" box. The "Amplitude" box is filled with a small number. The perturbation produced by the Perturbation block will be added to the duty cycle which has the steady-state value of 0.23 (see Table 6.1), so, the amplitude of Perturbation block must be quite small in comparison to 0.23.

Enter the desired frequency range in the opened window and click the "Start analysis" button.

The simulation result is shown in Fig. 6.10.

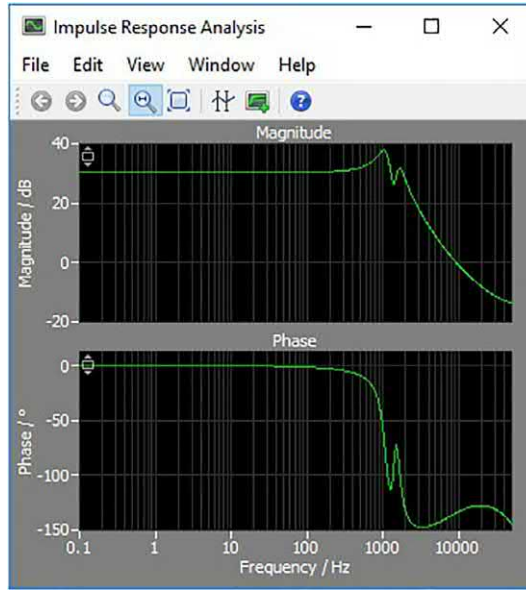


**FIG. 6.10** Bode diagram of $\frac{v_o(s)}{d(s)}$ transfer function.

You can export the obtained result as a .csv (Comma Separated Values) file. The .csv file is the medium to transfer the obtained results into MATLAB®. Use the File menu in order to export the graphics as a .csv file (Fig. 6.11).

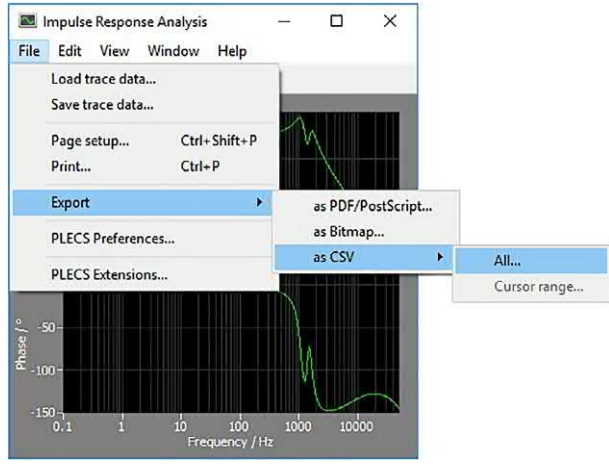


**FIG. 6.11** Use "Export" to produce the .csv files.

Assign the desired name and path in the "Export as" window. Here, the "nominal_values_freq_resp.csv" name is selected (Fig. 6.12).

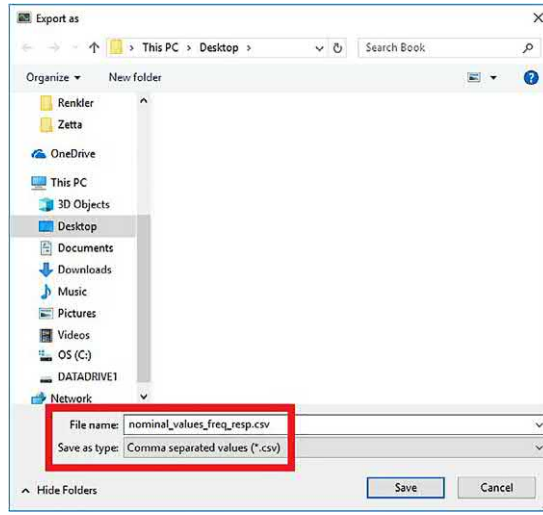


**FIG. 6.12** The "Export as" window.

You can open the saved file (nominal_values_freq_resp.csv) in Notepad. As shown in Fig. 6.13, the saved file has three columns. First column is the frequency in Hertz, second column is the magnitude in dB, and finally the third one is the phase in Radians.

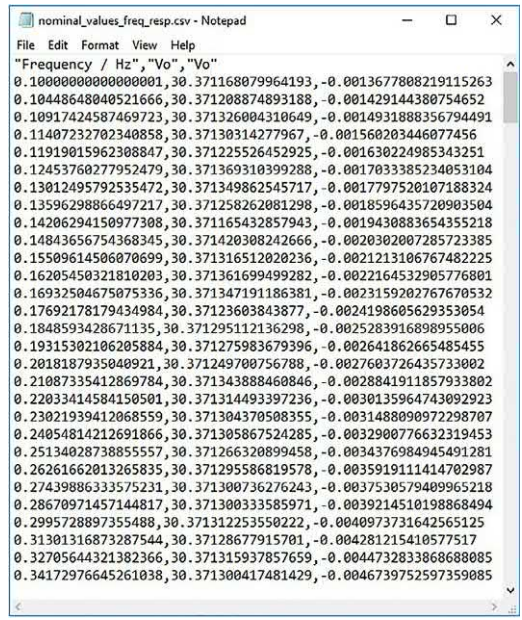


**FIG. 6.13** The .csv is opened in Notepad.

Clear the first line ("Frequency /Hz,""Vo," "Vo") before importing the file into the MATLAB® environment (Fig. 6.14).

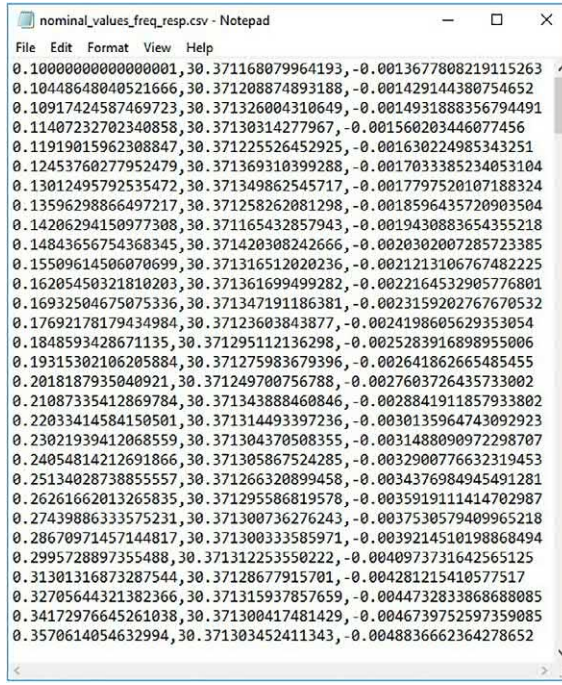


**FIG. 6.14** First line of the .csv file is removed.

The following code (Fig. 6.15) reads the .csv file and redraws the Bode diagram in the MATLAB® environment. The drawn Bode diagram is shown in Fig. 6.16. This figure is the same as Fig. 6.10. So, we import the results into the MATLAB® successfully. Using the "`tfest`" command, one can estimate a transfer function for the diagram provided by PLECS®.

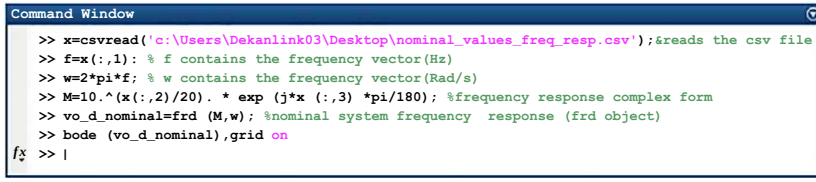


**FIG. 6.15** Required code for importing the produced .csv file into MATLAB®.

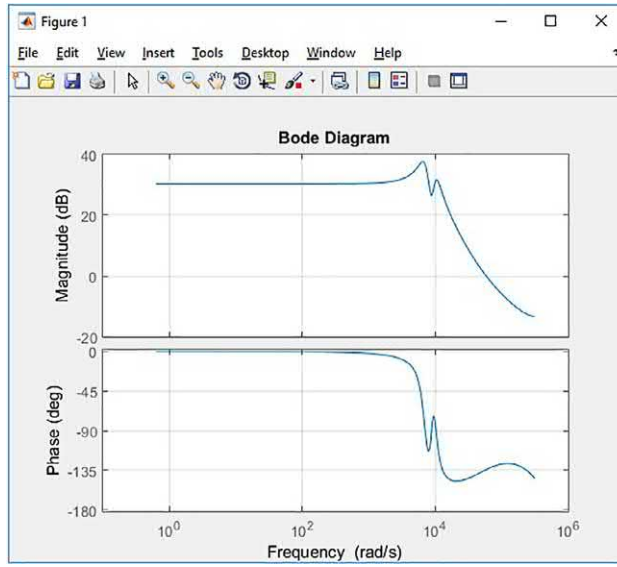


**FIG. 6.16** Fig. 6.10 is regenerated in MATLAB® environment. The horizontal axis in Fig. 6.10 uses Hz unit, while this figure uses $\frac{rad}{s}$.

You can use the inductor currents as output as well. For instance, the schematic shown in Fig. 6.17 extracts the $\frac{i_{L_2}(s)}{d(s)}$ transfer function. The "Am1" is an ammeter block. Simulation results are shown in Fig. 6.18.

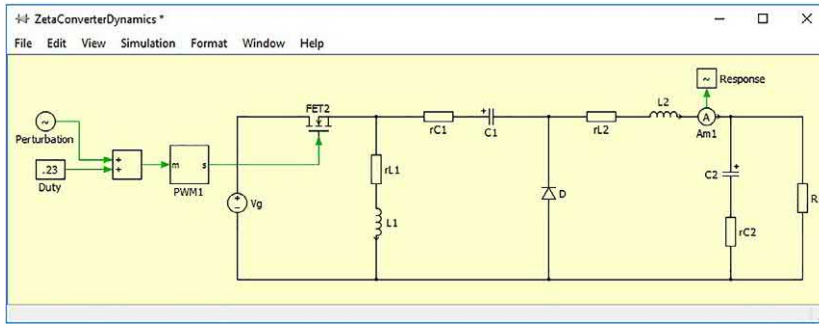


**FIG. 6.17** Extraction of the $\frac{i_{L_2}(s)}{d(s)}$ transfer function Bode diagram.

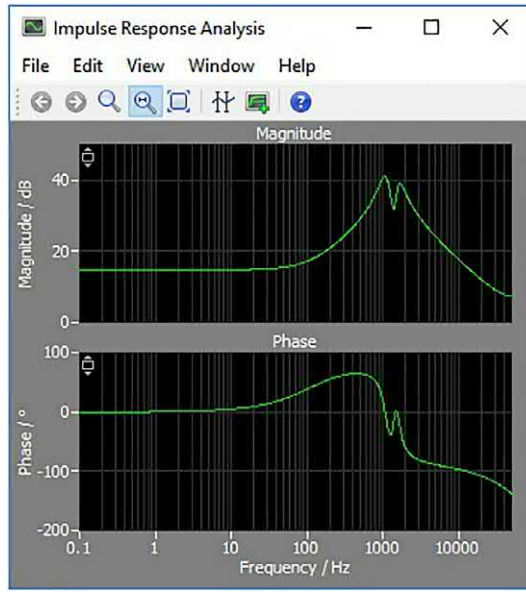


**FIG. 6.18** Bode diagram of $\frac{i_{L_2}(s)}{d(s)}$ transfer function.

You can add cursor to the shown Bode diagram using the icon shown in Fig. 6.19.

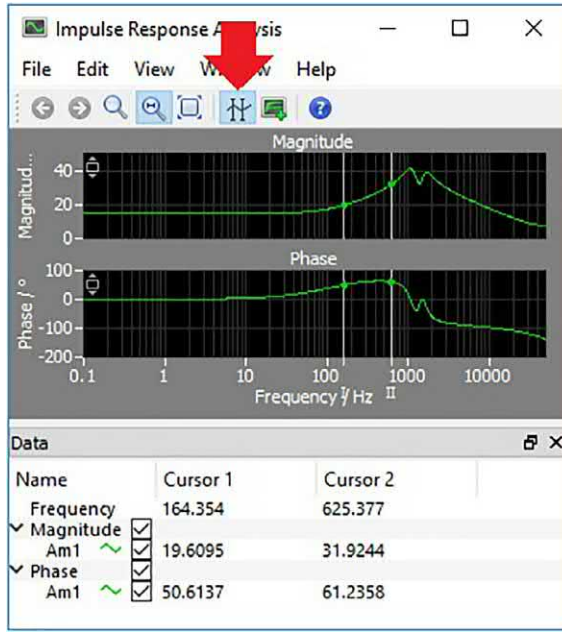


**FIG. 6.19** Cursors can be used to read the diagram easily. Use the Cursors icon (shown with arrow) to add cursors to the diagram.

### 6.4.2 Audio susceptibility

The open-loop line-to-output transfer function (also termed power supply ripple rejection (PSRR) or audio susceptibility) is defined as the transfer function from perturbation of the input voltage to perturbation of the output voltage with duty ratio held constant. The audio susceptibility of the studied Zeta converter can be obtained with the aid of the schematic shown in Fig. 6.20. The Perturbation block adds small perturbations to the input voltage and the Response block measures the effects on output voltage.

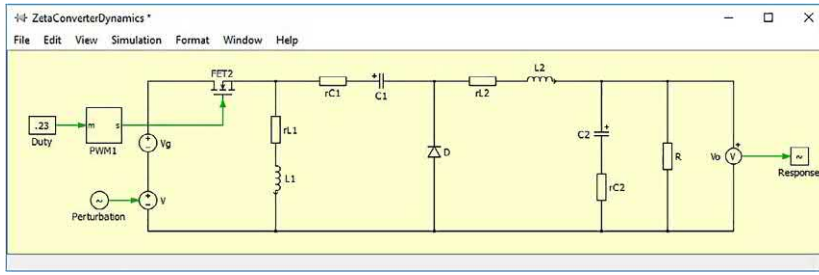


**FIG. 6.20** Extraction of the $\frac{v_o(s)}{v_{in}(s)}$ transfer function.

The block named "V" in the schematic shown in Fig. 6.21 is a controlled voltage source.

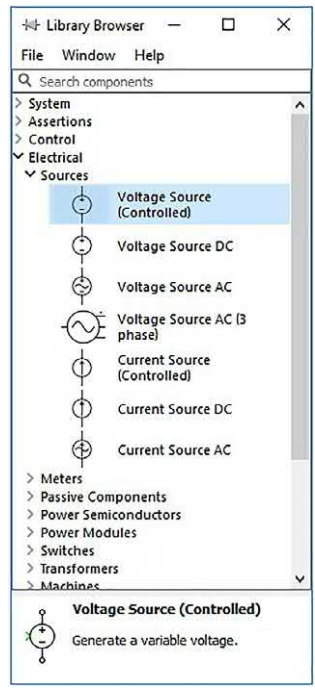


**FIG. 6.21** Controlled voltage source block can be found in the Sources section of Library Browser.

After running the simulation with the settings shown in Fig. 6.22, the result shown in Fig. 6.23 is obtained.

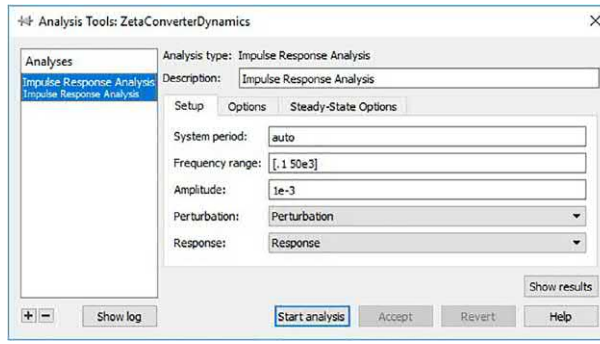


**FIG. 6.22** Simulation settings.

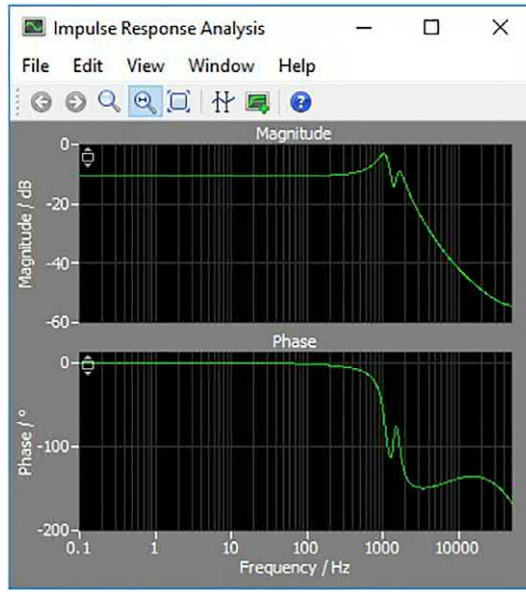


**FIG. 6.23** Bode diagram of $\frac{v_o(s)}{v_{in}(s)}$ transfer function.

### 6.4.3 Output impedance

The converter output impedance can be extracted with the aid of schematic shown in Fig. 6.24. The Perturbation block injects a small current to the output of converter and the Response block measures the effects on output voltage. So, result of analysis has the dimension of Ohm's (since $\frac{changes\ of\ output\ voltage\ (V)}{changes\ of\ injected\ current\ (A)}$ has the dimension of Ohm's).

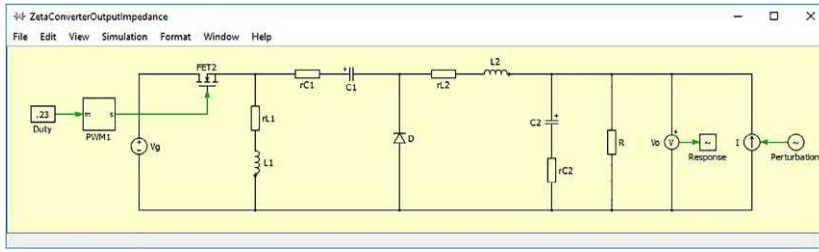


**FIG. 6.24** Extraction of output impedance.

The block named "I" in the schematic shown in Fig. 6.25 is a controlled current source.

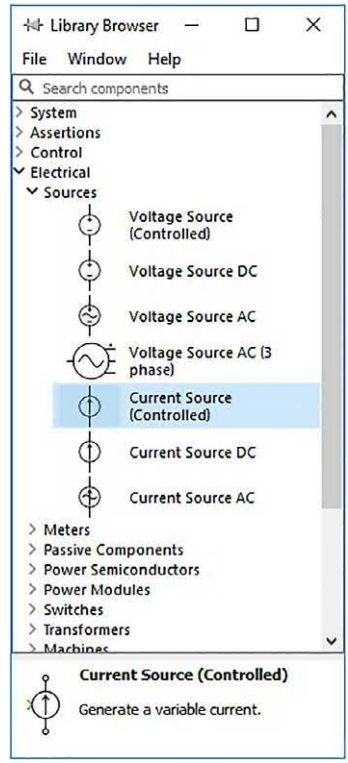


**FIG. 6.25** Controlled current source block can be found in the Sources section of Library Browser.

After running the simulation with the settings shown in Fig. 6.26, the result shown in Fig. 6.27 is obtained.

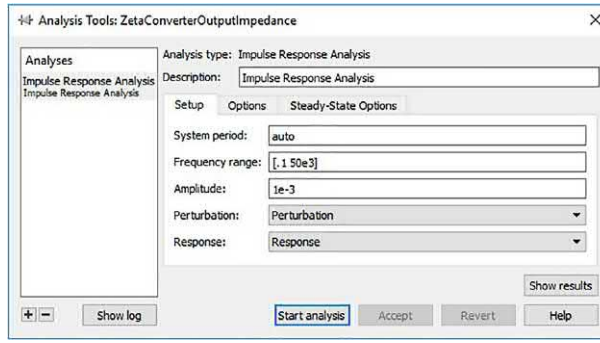


**FIG. 6.26** Simulation settings.

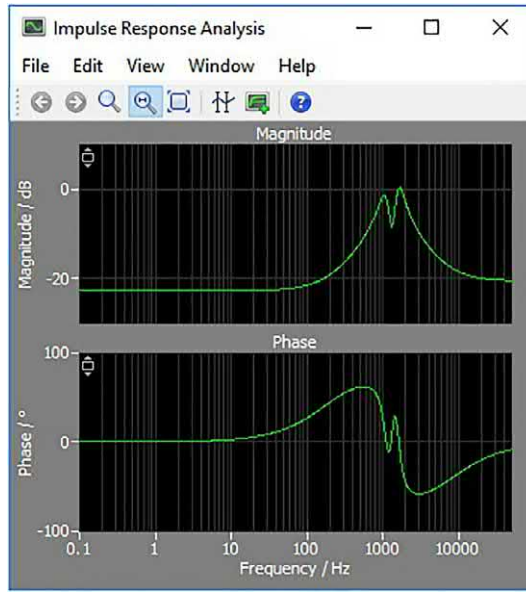


**FIG. 6.27** Bode diagram of output impedance.

### 6.4.4 Using the PLECS® to extract the uncertain model of the DC-DC converters

The previous section studied the small signal transfer functions of the converter for nominal values of components. We neglect the component changes in the previous section of this chapter. In this section, we consider the components changes. The components changes come from different sources as mentioned before. For instance, each component has its own tolerances. Even aging and temperature changes cause the component values to change. In this section,

effects of components changes on the converter dynamics are studied. This section shows how PLECS® can be used to extract the uncertain model of studied Zeta converter.

#### 6.4.4.1 Additive uncertainty model

Assume that the Zeta converter components have variations shown in Table 6.2.

For instance, according to Table 6.2, ESR of $C_1$ changes between 0.19 $\Omega \times 0.9 = 0.171\ \Omega$ and 0.19 $\Omega \times 1.9 = 0.361\ \Omega$.

**TABLE 6.2 The Zeta converter parameters (see Fig. 6.2).**

| | Nominal Value | Variations |
|---|---|---|
| Input DC source voltage, Vg | 20 V | ±20% |
| MOSFET Drain-Source resistance, rds | 10 mΩ | ±20% |
| Capacitor, $C_1$ | 100 μF | ±20% |
| Capacitor $C_1$ Equivalent Series Resistance (ESR), $rC_1$ | 0.19 Ω | [−10%,+90%] |
| Capacitor, $C_2$ | 220 μF | ±20% |
| Capacitor $C_2$ Equivalent Series Resistance (ESR), $rC_1$ | 0.095 Ω | [−10%,+90%] |
| Inductor, $L_1$ | 100 μH | ±10% |
| Inductor ESR, $rL_1$ | 1 mΩ | [−10%,+90%] |
| Inductor, $L_2$ | 55 μH | ±10% |
| Inductor ESR, $rL_2$ | 0.55 mΩ | [−10%,+90%] |
| Diode voltage drop, vD | 0.7 V | ±30% |
| Diode forward resistance, rD | 10 mΩ | [−10%,+50%] |
| Load resistor, R | 6 Ω | ±80% |
| Switching Frequency, Fsw | 100 kHz | – |

The schematic shown in Fig. 6.28 can be used to extract the additive uncertainty model of the studied Zeta converter. This schematic is used to extract the uncertain model of $\frac{v_o(s)}{d(s)}$ transfer function.

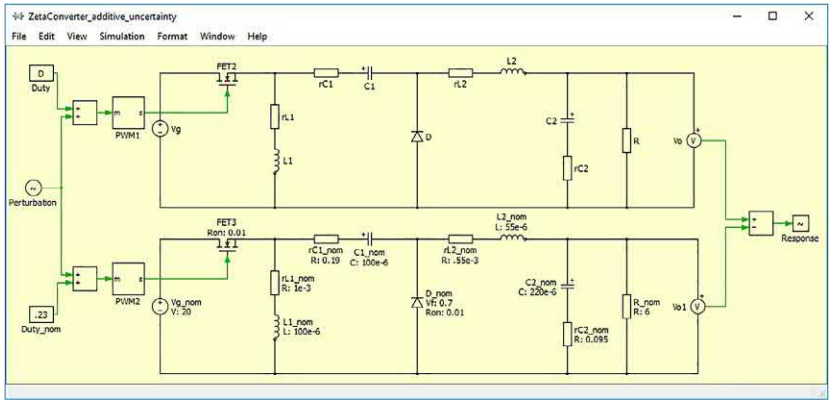


**FIG. 6.28** Schematic to extract the additive uncertainty model of the studied Zeta converter.

The schematic is composed of two Zeta converters. The lower Zeta converter has the nominal components. Each component of lower converter is double clicked and the nominal value of component is entered. For instance, value of the inductor connected to the output capacitor is set to 55 μH (Fig. 6.29).

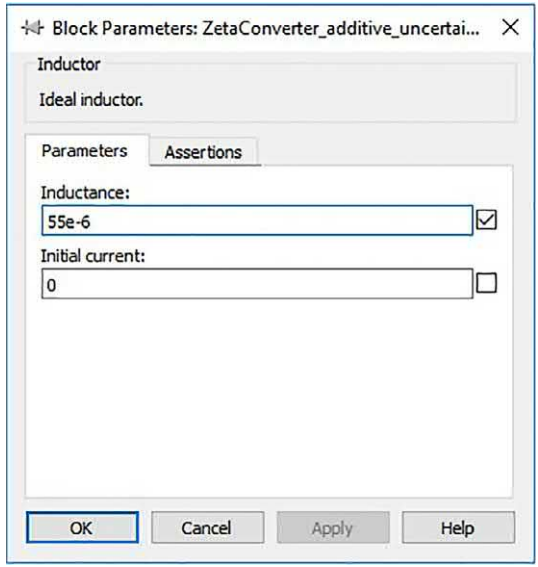


**FIG. 6.29** The "Inductance" box is filed with a numeric value.

The upper Zeta converter will be supplied with the components selected randomly from their allowed interval (A MATLAB® program will produce the random values). In this section of schematic, value of each component is controlled

with a variable, which will be initialized in the beginning of simulation. For instance, value of the inductor connected to the output capacitor is set by a variable named L2 (Fig. 6.30). According to Table 6.2, $L_{2,min} < L_2 < L_{2,max}$, where $L_{2,min} = 0.55\,\mu H \times 0.9 = 0.495\,\mu H$ and $L_{2,max} = 0.55\,\mu H \times 1.1 = 0.605\,\mu H$.

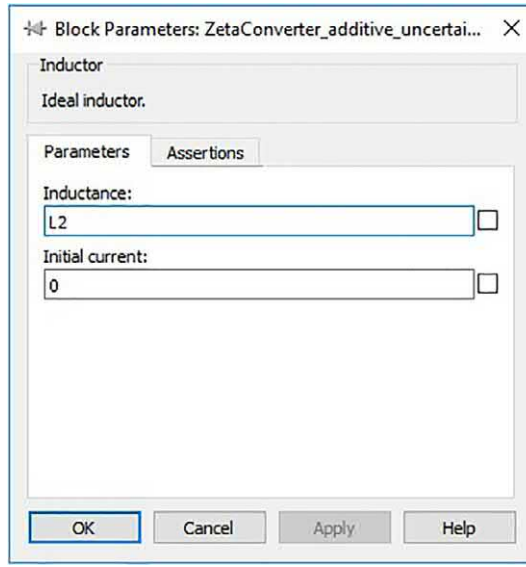


**FIG. 6.30** The "Inductance" box is filed with a variable name.

The following code produces acceptable component values (according to the variations given in Table 6.2) for the upper Zeta converter. The produced components set is copied into the Windows® clipboard, so one can paste it easily in the "Initialization" section of "Simulation Parameters" window and run the simulation with the generated random values.

```
%This program produces random component values
%produced values are copied into the Windows clipboard
%so you can paste them easily into the Initialization
%section of PLECS
clc
clear all


NumberOfIteration=20;   % set the desired number of iteration here.
DesiredOutputVoltage=5; % set the desired output voltage here.


n=0;
for i=1:NumberOfIteration
n=n+1;
%Definition of uncertainity in parameters
VG_unc=ureal('VG_unc',20,'Percentage',[-20 +20]);    % Value of input DC source is in the
range of 16..24
rg=0;                                                % Internal resistance of input DC
source
```

```
rds_unc=ureal('rds_unc',.01,'Percentage',[-20 +20]);     % MOSFET on resistance
C1_unc=ureal('C1_unc',100e-6,'Percentage',[-20 +20]);    % Capacitor C1 value
C2_unc=ureal('C2_unc',220e-6,'Percentage',[-20 +20]);    % Capacitor C2 value
rC1_unc=ureal('rC1_unc',.19,'Percentage',[-10 +90]);     % Capacitor C1
Equivalent Series Resistance(ESR)
rC2_unc=ureal('rC2_unc',.095,'Percentage',[-10 +90]);    % Capacitor C2
Equivalent Series Resistance(ESR)
L1_unc=ureal('L1_unc',100e-6,'Percentage',[-10 +10]);    % Inductor L1 value
L2_unc=ureal('L2_unc',55e-6,'Percentage',[-10 +10]);     % Inductor L2 value
rL1_unc=ureal('rL1_unc',1e-3,'Percentage',[-10 +90]);    % Inductor L1
Equivalent Series Resistance(ESR)
rL2_unc=ureal('rL2_unc',.55e-3,'Percentage',[-10 +90]); % Inductor L2
Equivalent Series Resistance(ESR)
rD_unc=ureal('rD_unc',.01,'Percentage',[-10 +50]);       % Diode series resistance
VD_unc=ureal('VD_unc',.7,'Percentage',[-30 +30]);        % Diode voltage drop
R_unc=ureal('R_unc',6,'Percentage',[-80 +80]);           % Load resistance
IO=0;                                                    % Average value of output current
source
fsw=100e3;                                               % Switching frequency


%Sampling the uncertain set
%for instance usample(VG_unc,1) takes one sample of uncertain
%parameter VG_unc


VG=usample(VG_unc,1);                                    % Sampled value of input
DC source
rds=usample(rds_unc,1);                                  % Sampled MOSFET on resistance
C1=usample(C1_unc,1);                                    % Sampled capacitor C1 value
C2=usample(C2_unc,1);                                    % Sampled capacitor C2 value
rC1=usample(rC1_unc,1);                                  % Sampled capacitor C1
Equivalent Series Resistance(ESR)
rC2=usample(rC2_unc,1);                                  % Sampled capacitor C2
Equivalent Series Resistance(ESR)
L1=usample(L1_unc,1);                                    % Sampled inductor L1 value
L2=usample(L2_unc,1);                                    % Sampled inductor L2 value
rL1=usample(rL1_unc,1);                                  % Sampled inductor L1
Equivalent Series Resistance(ESR)
rL2=usample(rL2_unc,1);                                  % Sampled inductor L2
Equivalent Series Resistance(ESR)
rD=usample(rD_unc,1);                                    % Sampled diode series
resistance
VD=usample(VD_unc,1);                                    % Sampled diode voltage drop
R=usample(R_unc,1);                                      % Sampled load resistance


%output voltage of an IDEAL(i.e. no losses) Zeta converter operating in CCM is given by:
%  D
%VO=--------VG
% 1-D
%where
%VO: average value of output voltage
%D: Duty Ratio
%VG: Input DC voltage
%So, for a IDEAL converter
%  VO
%D=----------
% VO+VG
%Since our converter has losses we use a bigger duty ratio, for instance:
%   VO
%D=1.1 ----------
%  VO+VG
D=1.1*DesiredOutputVoltage/(VG+DesiredOutputVoltage);


%preparing the strings
S1=strcat('VG=',num2str(VG),';');
S2=strcat('rds=',num2str(rds),';');
```

```
S3=strcat('C1=',num2str(C1),';');
S4=strcat('C2=',num2str(C2),';');
S5=strcat('rC1=',num2str(rC1),';');
S6=strcat('rC2=',num2str(rC2),';');
S7=strcat('L1=',num2str(L1),';');
S8=strcat('L2=',num2str(L2),';');
S9=strcat('rL1=',num2str(rL1),';');
S10=strcat('rL2=',num2str(rL2),';');
S11=strcat('rD=',num2str(rD),';');
S12=strcat('VD=',num2str(VD),';');
S13=strcat('R=',num2str(R),';');
S14=strcat('D=',num2str(D),';');

%coping the data into the Windows Clipboard. So, you can paste it into the
%PLECS
data=strcat(S1,S2,S3,S4,S5,S6,S7,S8,S9,S10,S11,S12,S13,S14);
clipboard('copy',data)
disp('Data is copied into clipboard. You can paste it in PLECS initialization section right
now...')
message=strcat('Iteration #',num2str(n),' finished.');
disp(message)
disp('Press any key to produce another value set.')
disp(' ')
pause
end
disp('--------------------------')
disp('Program terminates here...')
```

After running the code (and finishing the first iteration), the message shown in Fig. 6.31 will appear.

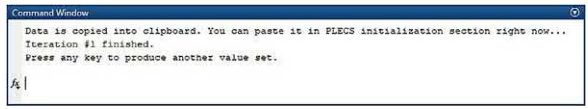


**FIG. 6.31** User is asked to press a key before the next iteration.

Before pressing any key in the MATLAB® environment and starting the next iteration (which generates new random values), the user must go to the "Initialization" tab of "Simulation Parameters" window and paste the produced data (Figs. 6.32 and 6.33).

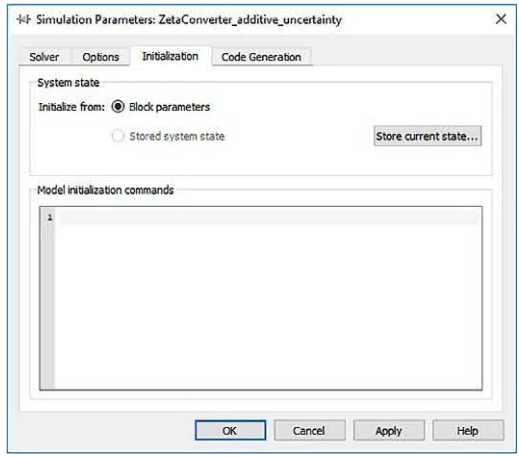


**FIG. 6.32** The "Initialization" tab of "Simulation Parameters" window.

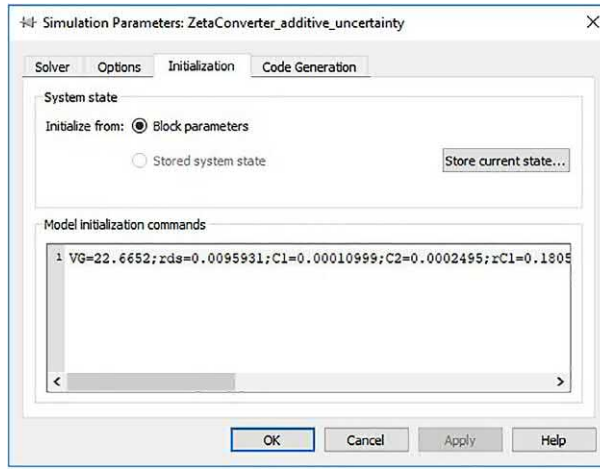


**FIG. 6.33** Produced random values are paste into the "Model initialization commands" section of "Initialization" tab. Click the Model initialization commands section of and press the Ctrl+V to paste the generated values.

Now the user runs the PLECS® simulation with the values produced by the MATLAB® code (Fig. 6.34).

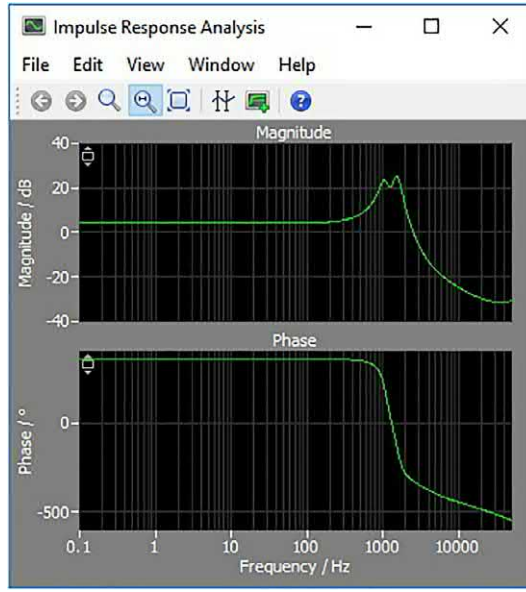


**FIG. 6.34** Simulation result.

The user exports the obtained result as an .csv file (Fig. 6.35). The result is saved under the name of sim1.csv (Fig. 6.36).

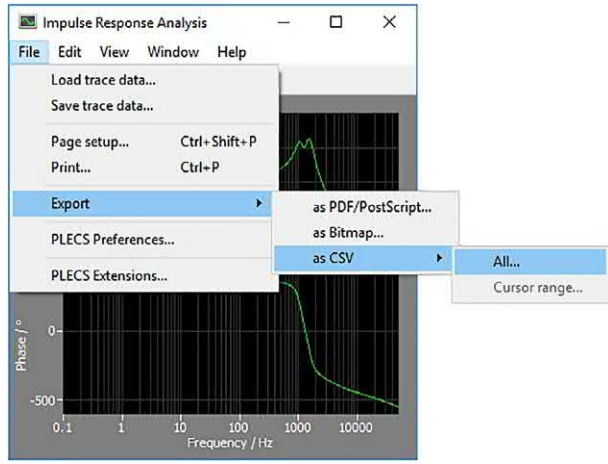


**FIG. 6.35** Obtained result is exported as a .csv file.

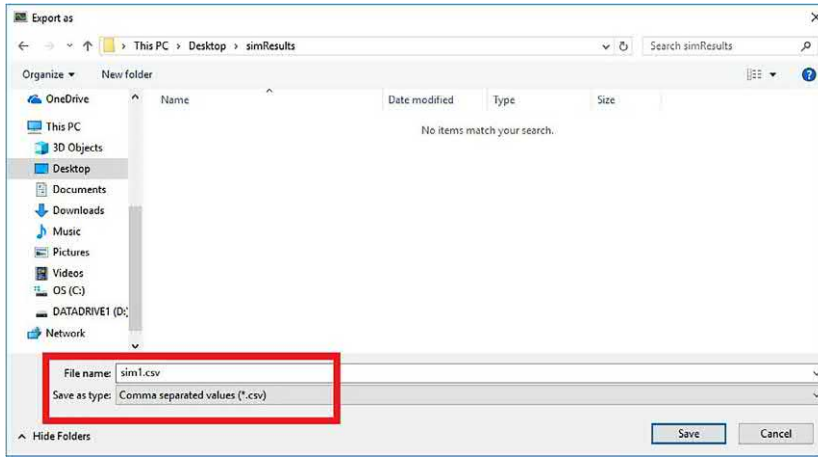


**FIG. 6.36** The simulation result for the first generated random set is saved under the name of sim1.csv.

After saving the result, the user returns to the MATLAB® environment and press any key in order to produce a new random set. After the random set is generated, he/she switches to the PLECS® environment and pastes the produced random set into the Initialization tab of Simulation Parameters window.

The user redoes the aforementioned process until all the iterations are finished. The number of iterations is set by the `NumberOfIteration` variable

defined in the seventh line of the code (Fig. 6.37). `NumberOfIteration` is set to 20 in the shown code. So, the MATLAB® code produces 20 different random sets. All the simulation results are exported as .csv file.

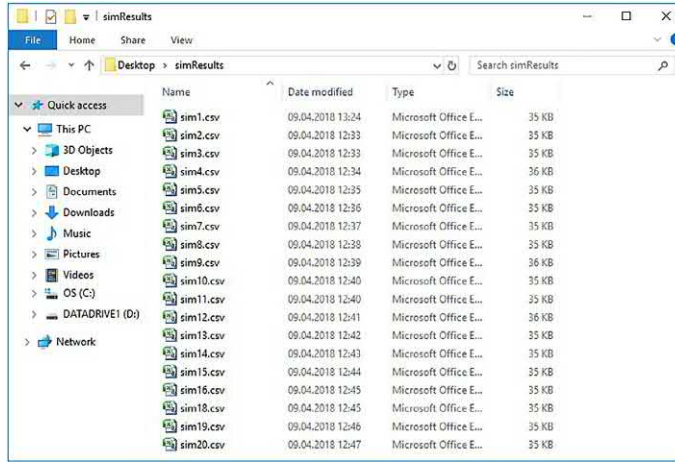


**FIG. 6.37** Analysis results are saved as sim1.csv,sim2.csv, sim3.csv, …, sim20.csv.

All the obtained .csv files are opened in the Notepad and their first line is removed (Figs. 6.38 and 6.39).

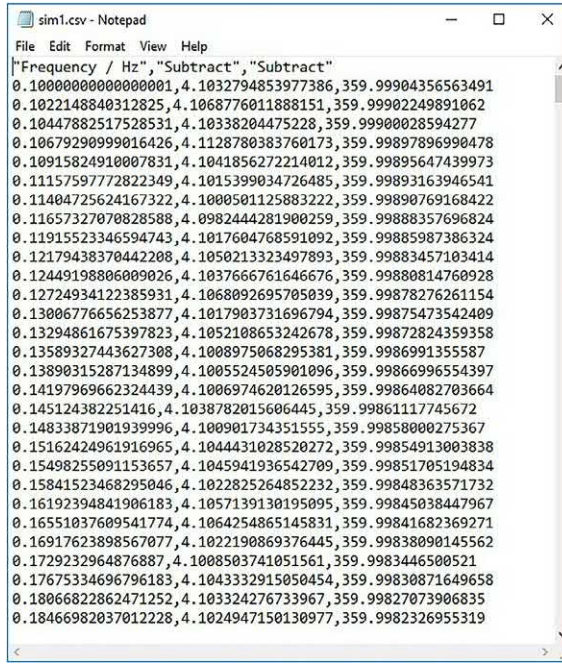


**FIG. 6.38** Opening the "sim1.csv" in Notepad.

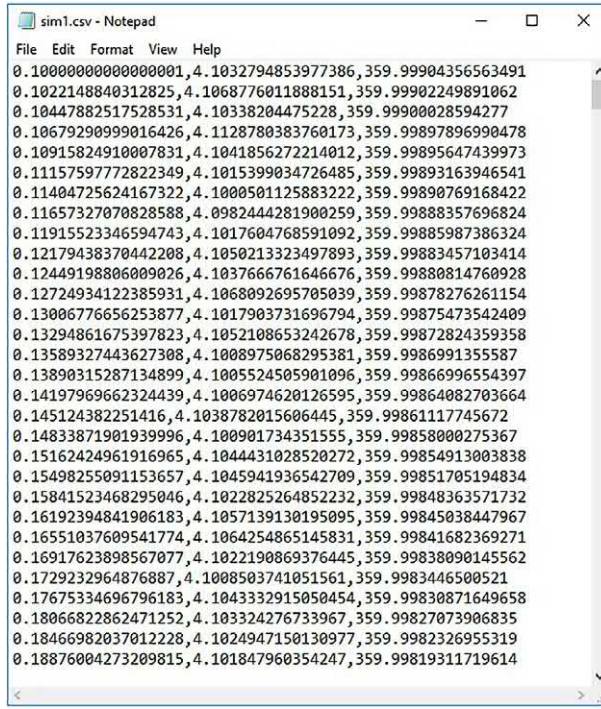


**FIG. 6.39** First line of sim1.csv is removed.

Following MATLAB® code reads all the simulation results (prepared .csv files) and draws them simultaneously on the same graph.

```
%This program draws the results(Additive Uncertainty) produced by PLECS
clc
clear all
NumberOfSimulations=20;


for i=1:NumberOfSimulations
disp('percentage of work done:')
disp(i/NumberOfSimulations*100)
disp(' ')


name=strcat('sim',num2str(i),'.csv');
x=csvread(strcat('C:\Users\Desktop\SimResults\',name)); %reads the csv file
f=x(:,1);
w=2*pi*f;
M=10.^(x(:,2)/20).*exp(j*x(:,3)*pi/180); %Magnitude of freq. resp.(complex form)
H=frd(M/Mnominal,w);
bode(H), grid on
hold on


end
title('Additive uncertainty in vo(s)/d(s)')
```

After running the code, the result shown in Fig. 2.107 is obtained.

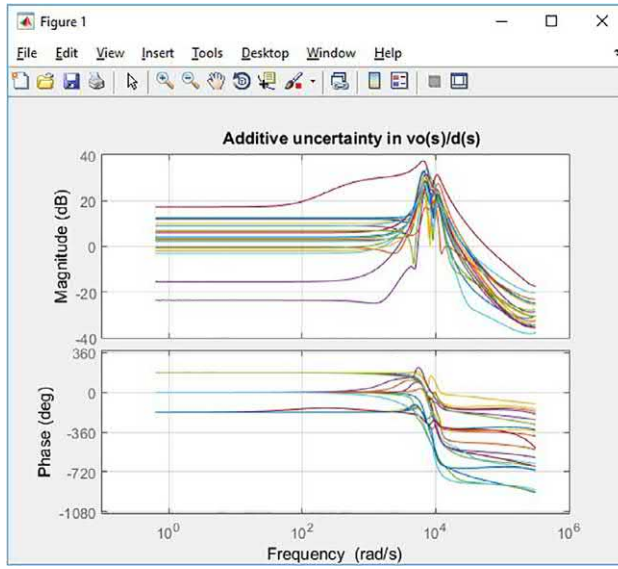


**FIG. 6.40** Additive uncertainty in $\frac{v_o(s)}{d(s)}$.

After the graph shown in Fig. 6.40 is obtained, we need to fit such a weight, which passes above all the transfer functions. The following code is used for this purpose.

```
%Selection of the upper bound for uncertainty
Number_of_points=20;
[freq,resp_dB]=ginput(Number_of_points);
%Reading are in decibel(dB). The following loop find the magnitudes.
for i=1:Number_of_points
    resp(i)=10^(resp_dB(i)/20);
end
selected_points_frd=frd(resp,freq); %Making the frd object.
ord=3; %Order of produced weight
W=fitmagfrd(selected_points_frd,ord); %Fitting a transfer function to the selected data
points.
Wtf=tf(W);
bode(Wtf,'r--')
```

After the code is run, the user clicks 20 points, which are above the highest transfer function. For instance, some of the acceptable points are shown with red stars in Fig. 6.41.

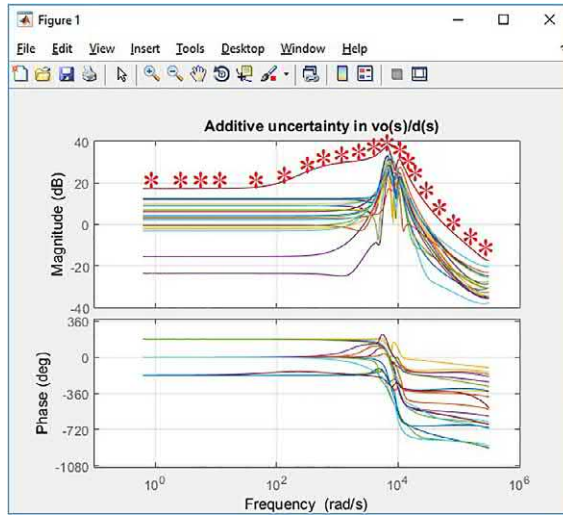


**FIG. 6.41** In order to estimate the uncertainty weight, the user selects points, which are above the highest transfer function. Use points of magnitude plot.

After selection of 20 points is finished, the `fitmagfrd` command estimates a transfer function for the selected points. Order of estimated transfer function is defined by the `ord` variable.

### 6.4.4.2 *Multiplicative uncertainty model*

Schematic shown in Fig. 6.28 can be used to extract the additive uncertainty model of the converter. Following code normalizes (divide the difference to the nominal transfer function) the results of previous analysis. This lets the calculation of multiplicative uncertainty weights.

```
%This program draws the results(Multiplicative Uncertainty) produced by PLECS
%Running this code takes time, please be patient!
clc
clear all
NumberOfSimulations=20;


%Results obtained for nominal system
%see previous analyses
x=csvread(strcat('C:\Users\DekanlikO3\Desktop\nominal_values_freq_resp.csv'));
f=x(:,1);
w=2*pi*f;
M_nominal=10.^(x(:,2)/20).*exp(j*x(:,3)*pi/180); %Magnitude of freq. resp.(complex form)
vo_d_nominal=frd(M_nominal,w);


for i=1:NumberOfSimulations
disp('percentage of work done:')
disp(i/NumberOfSimulations*100)
disp(' ')


name=strcat('sim',num2str(i),'.csv');
x=csvread(strcat('C:\Users\DekanlikO3\Desktop\SimResults\',name)); %reads the csv file
f=x(:,1);
```

```
w=2*pi*f;
M=10.^(x(:,2)/20).*exp(j*x(:,3)*pi/180); %frequency response complex form for the read
.csv file
H=frd(M/M_nominal,w);
bode(H), grid on
hold on
end
title('Multiplicative uncertainty in plant')
```

After running the code, the result shown in Fig. 6.42 is obtained.

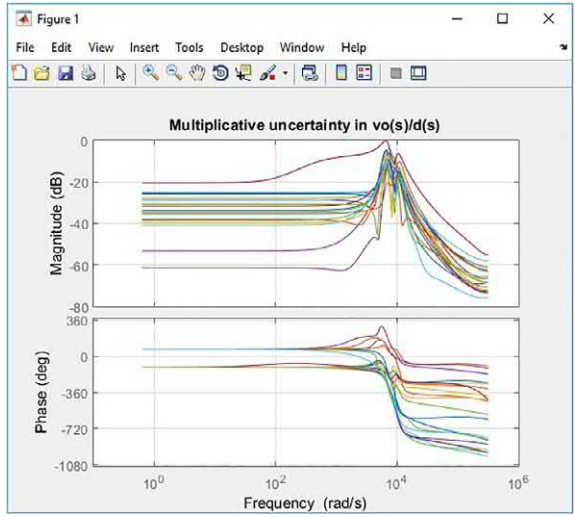


**FIG. 6.42** Multiplicative uncertainty in $\frac{v_o(s)}{d(s)}$.

An upper bound for the transfer functions shown in Fig. 6.42 can be found with the aid of following code. Obtained weight is shown in Fig. 6.43.

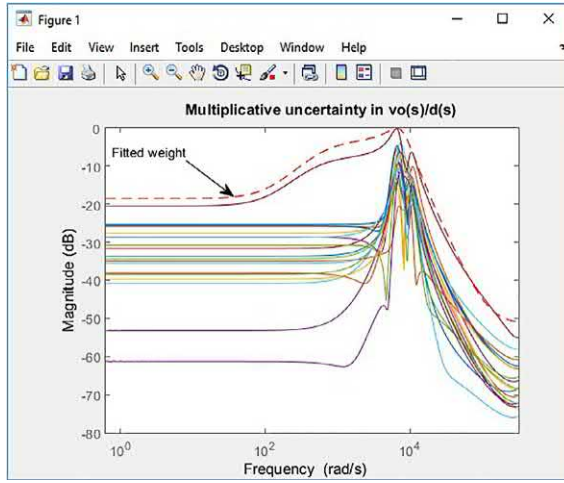


**FIG. 6.43** Fitting a multiplicative uncertainty weight.

```
%This program draws the results(Multiplicative Uncertainty) produced by PLECS
%You can obtain the upper bound of uncertainty as well.
%Running this code takes time, please be patient!
clc
clear all
NumberOfSimulations=20;


%Results obtained for nominal system
%see previous analyses
x=csvread(strcat('C:\Users\Desktop\nominal_values_freq_resp.csv'));
f=x(:,1);
w=2*pi*f;
M_nominal=10.^(x(:,2)/20).*exp(j*x(:,3)*pi/180); %Magnitude of freq. resp.(complex form)
vo_d_nominal=frd(M_nominal,w);


for i=1:NumberOfSimulations
disp('percentage of work done:')
disp(i/NumberOfSimulations*100)
disp(' ')


name=strcat('sim',num2str(i),'.csv');
x=csvread(strcat('C:\Users\Desktop\SimResults\',name)); %reads the csv file
f=x(:,1);
w=2*pi*f;
M=10.^(x(:,2)/20).*exp(j*x(:,3)*pi/180); %frequency response complex form
H=frd(M/M_nominal,w);
bodemag(H), grid on
hold on
end
title('Multiplicative uncertainty in plant')


pause
disp('press any key to continue')


%Selection of the upper bound for uncertainty
Number_of_points=20;
[freq,resp_dB]=ginput(Number_of_points);
%Reading are in desibel(dB). The following loop find the magnitudes.
for i=1:Number_of_points
    resp(i)=10^(resp_dB(i)/20);
end
selected_points_frd=frd(resp,freq); %Making the frd object.
ord=3; %Order of produced weight
W=fitmagfrd(selected_points_frd,ord); %Fitting a transfer function to the selected data
points.
Wtf=tf(W);
bode(Wtf,'r--')
```

One can obtain the calculated weight with the aid of commands shown in Fig. 6.44.

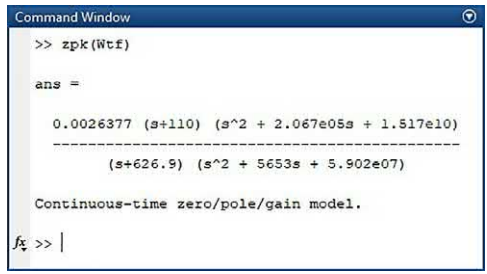


**FIG. 6.44** Equation of obtained weight.

## References


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Chapter 7

# Simulation of magnetic circuits in PLECS

## Chapter outline



## 7.1 Introduction

Magnetic components play an important role in power electronics converters. Using the powerful ready-to-use blocks in the Magnetic section of Library Browser, one can simulate complex magnetic circuits easily. Simulation of nonlinear effects such as hysteresis, saturation, and flux leakage is quite easy with the aid of blocks inside the Magnetic section of Library Browser.

This chapter focuses on the blocks inside the Magnetic section of Library Browser. It is assumed that the reader knows the basics of magnetic circuits. Chapter 1 of [1] is a good reference if you need to review the concepts. It is highly recommended to read the provided help for blocks inside the magnetic library of PLECS in order to learn the details of blocks.

This is the last chapter of book, which educates the software details for simulation of power electronics converters using PLECS. However, the world of simulation of power electronics converters using PLECS is not limited at all. Keeping this in mind, the last part of this chapter shows how you can increase your knowledge of simulation. It doesn't give you any fish, it teaches you fishing!

## 7.2 Magnetic blocks

The Magnetic section of Library Browser is shown in Fig. 7.1.


Simulation of Power Electronics Converters Using PLECS®. https://doi.org/10.1016/B978-0-12-817364-0.00007-2

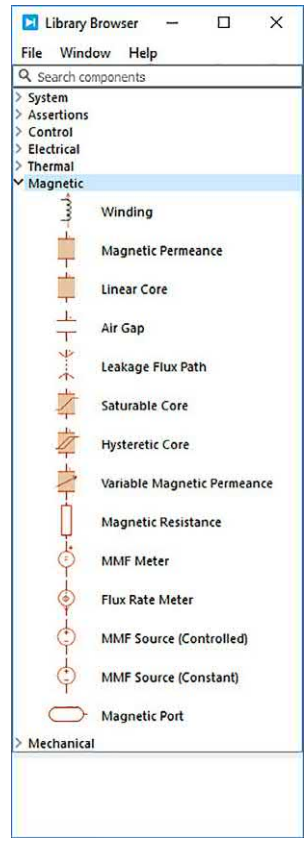



**FIG. 7.1** The Magnetic Section of Library Browser.

The blocks inside the Magnetic section of Library Browser can be combined with components from other domains in order to do the simulation. For instance, notice the simulation shown in Fig. 7.2. The blocks inside the rectangle simulate the flyback transformer. This simulation contains electrical blocks, control blocks, and magnetic blocks.

Some of the important Magnetic blocks are studied here.

### 7.2.1 Winding block

The Winding block is the interface between the electrical and magnetic domains. In order to specify the number of turns, double click the Winding block and fill the Number of turns box (Fig. 7.3). It is quite useful to click the Help button and study the provided information about the block. Note that only the Winding block (see Fig. 7.1) can be connected to components from the power circuit. Other blocks of Magnetic library can't be connected to power circuit.

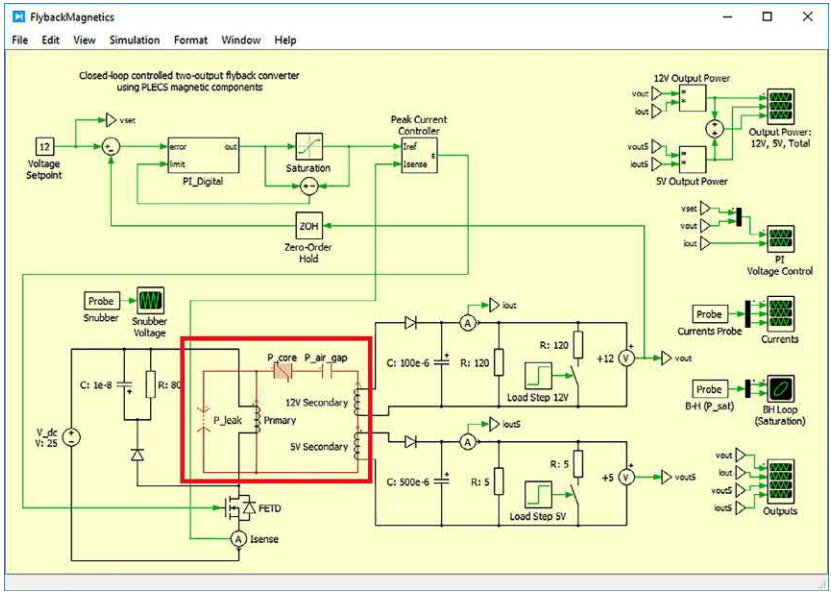



**FIG. 7.2** An example of simulation, which uses the blocks from the Magnetic library. With the aid of blocks from the Magnetic library, more realistic simulations can be done.

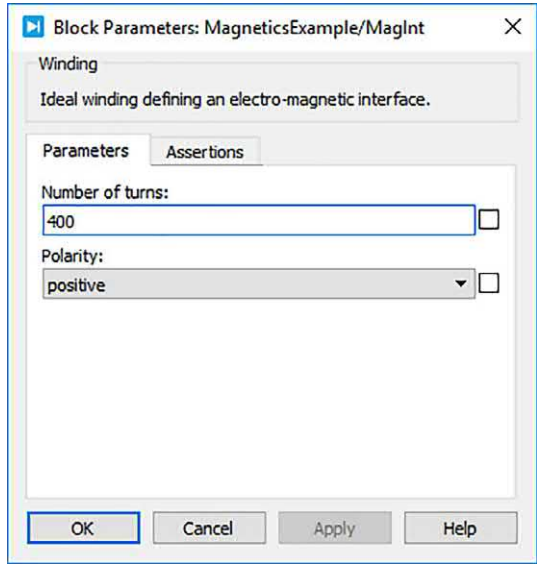



**FIG. 7.3** Parameters of Winding block.

If you want to simulate the winding copper resistance, you must attach a resistor block (selected from Passive Components section of Library Browser) to the electrical side (Fig. 7.4).

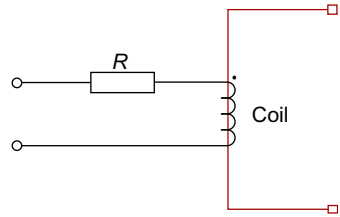



**FIG. 7.4** Copper losses are modeled with a resistor added in series with the winding.

Eddy current losses are modeled by a resistance on the magnetic side.

### 7.2.2 Magnetic permeance block

The Magnetic Permeance block (see Fig. 7.1) establishes a linear relationship between the magnetic flux $\varphi$ and the magnetomotive force $\mathcal{F}$. Magnetomotive permeance $\mathcal{P}$ is the reciprocal of magnetic reluctance $\mathcal{R}$:

$$\mathcal{P} = \frac{1}{\mathcal{R}} = \frac{\varphi}{\mathcal{F}}$$

The Linear Core block, models a segment of magnetic core. It establishes a linear relationship between the magnetic flux $\varphi$ and the magnetomotive force $\mathcal{F}$

$$\frac{\varphi}{\mathcal{F}} = \frac{\mu_0 \mu_r A}{l},$$

where $\mu_0 = 4\pi \times 10^{-7}\ \frac{N}{A^2}$ is the permeability of free space, $\mu_r$ is the relative permeability of the core material, $A$ is the cross-section area, and $l$ is the length of flux path.

### 7.2.3 Saturable core block

Typical $B-H$ curve for a ferrite core is shown in Fig. 7.5. After a certain point, though, further increases in the magnetomotive force produce relatively smaller increases in the flux. Finally, an increase in the magnetomotive force produces almost no change at all. The region of this Fig. in which the curve flattens out is called the saturation region, and the core is said to be saturated. In contrast, the region where the flux changes very rapidly is called the unsaturated region of the curve, and the core is said to be unsaturated. The transition region between the unsaturated region and the saturated region is sometimes called the knee of the curve.

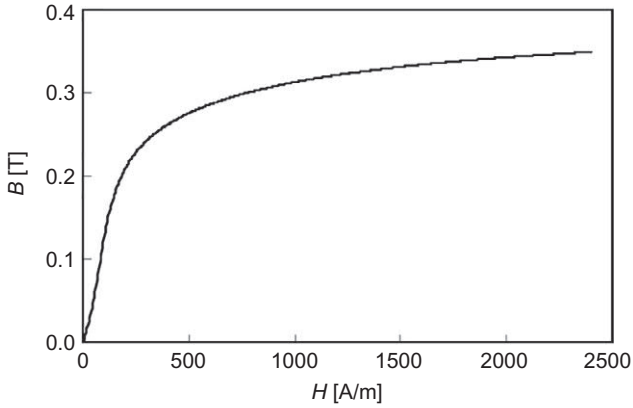



**FIG. 7.5** Typical $B-H$ curve for a ferrite core.

Using the Saturable Core block, you can simulate the saturation. This block defines a nonlinear relationship between the field strength $H$ and the flux density $B$ to model the saturation. PLECS provides two fitting functions: atan fit and coth fit. The $B-H$ equation for arctangent fit has the following equation:

$$B = \frac{2}{\pi} B_{\text{sat}} \tan^{-1}\left(\frac{\pi H}{2a}\right) + \mu_{\text{sat}} H$$

And the $B-H$ equation for cotangent hyperbolic fit is:

$$B = B_{\text{sat}}\left(\coth\frac{3H}{a} - \frac{a}{3H}\right) + \mu_{\text{sat}} H$$

Both fitting functions have three degrees of freedom, which are set by coefficients $\mu_{\text{sat}}$, $B_{\text{sat}}$ and $a$. $\mu_{\text{sat}}$ is the fully saturated permeability, which usually corresponds to the magnetic constant $\mu_0$, i.e., the permeability of air. $B_{\text{sat}}$ defines the knee of the saturation transition between unsaturated and saturated permeability:

$$B_{\text{sat}} = (B - \mu_{\text{sat}} H)|_{H\to\infty}$$

The coefficient $a$ is determind by the unsaturated permeability $\mu_{\text{unsat}}$ at $H = 0$.

$$a = \frac{B_{\text{sat}}}{\mu_{\text{unsat}} - \mu_{\text{sat}}}$$

The typical $B-H$ curve, which is produced by these types of equations, is shown in Fig. 7.6.

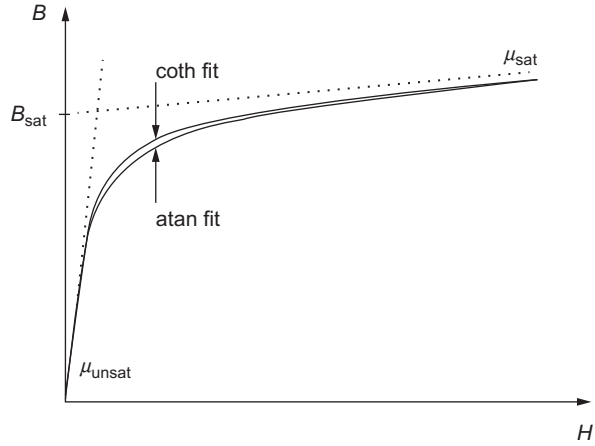



**FIG. 7.6** Typical $B-H$ curves, which are obtainable with the provided fitting functions.

### 7.2.4 Hysteretic core block

Simulation of hysteresis is possible with the aid of Hysteretic Core block. The relationship between the field strength $H$ and the flux density $B$ is nonlinear. The hysteresis characteristics are based on a Preisach model with a Lorentzian distribution function. Fig. 7.7 shows a fully excited major hysteresis curve with some minor reversal loops. The major curve is defined by the saturation point ($H_{sat}$, $B_{sat}$), the coercitive field strength $H_c$, the remanence flux density $B_r$, and the saturated permeability $\mu_{sat}$.

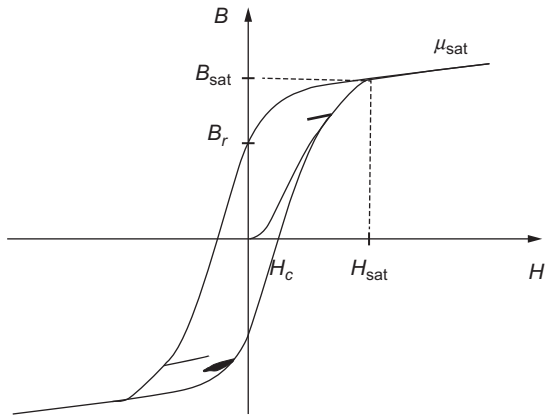



**FIG. 7.7** Hysteresis curve with some minor reversal loops.

### 7.2.5 Air gap block

Air Gap block models an air gap in a magnetic core. The relation between the magnetic flux $\varphi$ and magnetomotive force $\mathcal{F}$ for the block is

$$\frac{\varphi}{\mathcal{F}} = \frac{\mu_0 A}{l},$$

where $\mu_0 = 4\pi \times 10^{-7} \frac{N}{A^2}$ is the permeability of free space, $A$ is the cross-sectional area, and $l$ is the length of the flux path.

### 7.2.6 Leakage flux path block

This component models a magnetic leakage flux path. Leakage Flux Path block is equivalent to the Magnetic Permeance block. The only difference is the symbol. The relation between magnetic flux $\varphi$ and the magnetomotive force $\mathcal{F}$ is linear:

$$\mathcal{P} = \frac{1}{\mathcal{R}} = \frac{\varphi}{\mathcal{F}}$$

Magnetic permeance $\mathcal{P}$ is the reciprocal of magnetic reluctance $\mathcal{R}$.

## 7.3 Implementation of blocks

You can see the implementation details of blocks by right clicking the block and clicking the Look under mask (Fig. 7.8).

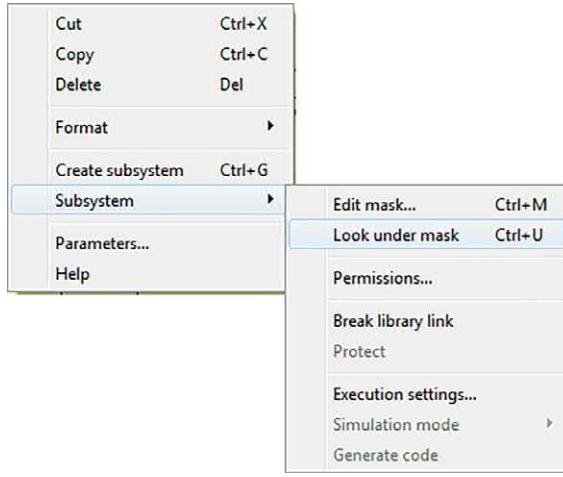



**FIG. 7.8** You can see the implementation of block with the aid of Look under mask.

For instance, if you right click on a Saturable Core block and click the Look under mask, the schematic shown in Fig. 7.9 will appear.

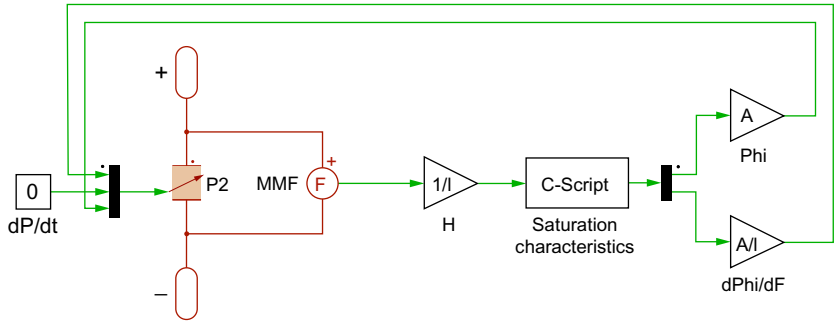



**FIG. 7.9** Implementation of Saturable Core block.

## 7.4 Some commonly used magnetic configuration

We study some of the commonly used configurations in this section. Assume a configuration such as the one shown in Fig. 7.10. This configuration can be modeled as shown in Fig. 7.11.

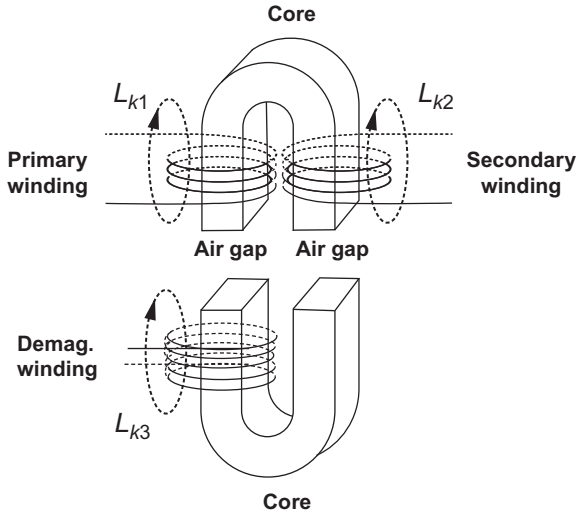



**FIG. 7.10** Mutually coupled inductors.

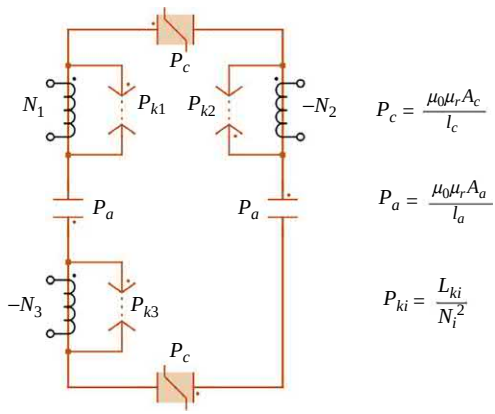



**FIG. 7.11** PLECS model of mutually coupled inductors shown in Fig. 7.10.

Figs. 7.12 and 7.13 give more examples on modeling the magnetic circuits.

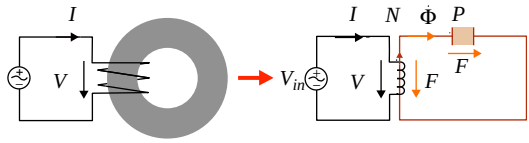



**FIG. 7.12** One winding toroid core and its PLECS model.

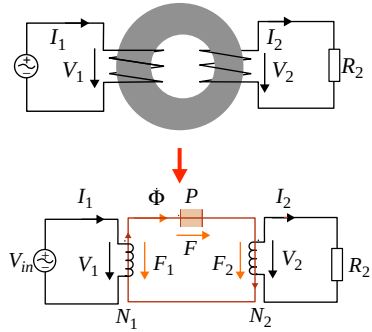



**FIG. 7.13** Two winding toroid cores and its PLECS model.

## 7.5 Case study

Consider a configuration like the one shown in Fig. 7.14. This Fig. shows a ferromagnetic core whose mean path length is 40 cm. There is a small gap of 0.05 cm in the structure of the otherwise whole core. The cross-sectional area

of the core is 12 $cm^2$, the relative permeability of the core is 4000, and the coil of wire on the core has 400 turns. Resistance of wire and input DC current are 10 Ω and 0.6 A, respectively. Fringing in the air gap is ignored. We want to calculate the flux density in the air gap.

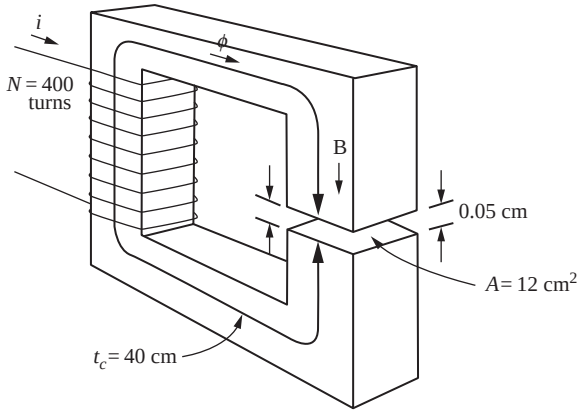



**FIG. 7.14** 400 Turns of wire wound a ferromagnetic core. The core has a small air gap with 0.05-cm length.

Fig. 7.15 shows the electrical equivalent circuit of magnetic circuit shown in Fig. 7.14.

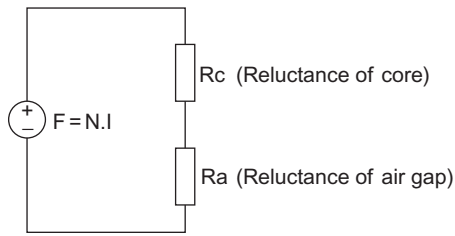



**FIG. 7.15** The magnetic circuit corresponds to Fig. 7.14.

The reluctance of core is:

$$\mathcal{R}_c = \frac{l_c}{\mu_r \mu_0 A_c} = \frac{0.4\,\text{m}}{(4000) \times (4\pi \times 10^{-7}) \times 0.0012\,\text{m}^2} = 66298\,\text{A.turn/Wb}$$

The reluctance of air gap is:

$$\mathcal{R}_a = \frac{l_a}{\mu_r \mu_0 A_c} = \frac{0.0005\,\text{m}}{(4\pi \times 10^{-7}) \times 0.0012\,\text{m}^2} = 331490\,\text{A.turn/Wb}$$

The total reluctance is:

$$\mathcal{R}_t = \mathcal{R}_a + \mathcal{R}_c = 397788\,\text{A.turn/Wb}$$

The MMF distribution can be calculated easily:

$$\mathcal{F}_c = \frac{\mathcal{R}_c}{\mathcal{R}_t} = \frac{\mathcal{R}_c}{\mathcal{R}_a + \mathcal{R}_c} \times N \times I = \frac{66298}{397788} \times 400 \times 0.6 = 40\,\text{A.turn}$$

$$\mathcal{F}_a = \frac{\mathcal{R}_a}{\mathcal{R}_t} = \frac{\mathcal{R}_a}{\mathcal{R}_a + \mathcal{R}_c} \times N \times I = \frac{331490}{397788} \times 400 \times 0.6 = 200\,\text{A.turn}$$

The flux density of air gap is:

$$B = \frac{\varphi}{A} = \frac{\frac{N.I}{\mathcal{R}_t}}{A} = \frac{\frac{400 \times 0.6}{397788}}{0.0012} = 0.5\,\text{T}$$

The inductance can be calculated as:

$$L = \frac{N^2}{\mathcal{R}_t} = \frac{400^2}{397788} = 0.40\,\text{H}$$

In order to analyze the configuration shown in Fig. 7.14 with PLECS, open a new simulation file and add a Winding block to it (Fig. 7.16). After that, double click the Winding block and set the Number of turns box to 400.

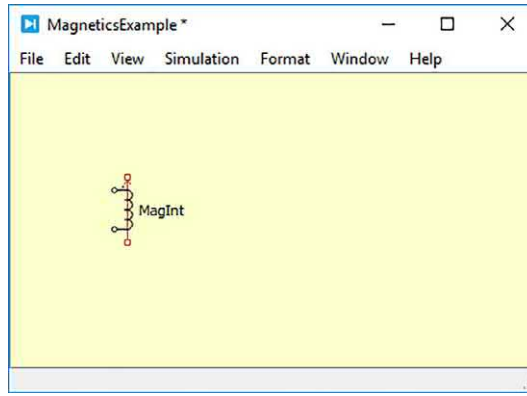



**FIG. 7.16** Addition of a Winding block to the simulation file.

Add Linear Core and Air Gap blocks to the simulation file (Fig. 7.17). Do the settings as shown in Figs. 7.18 and 7.19.

Connect the placed blocks together (Fig. 7.20).

Add the input DC source and a resistor to the schematic (Fig. 7.21). The resistor simulates the effect of winding wire resistance. The input DC voltage source is 6 V, since a 6-V voltage source provides 0.6 A in the steady state.

Add Probe and Scope blocks to the schematic in order to monitor the air gap flux density (Fig. 7.22).

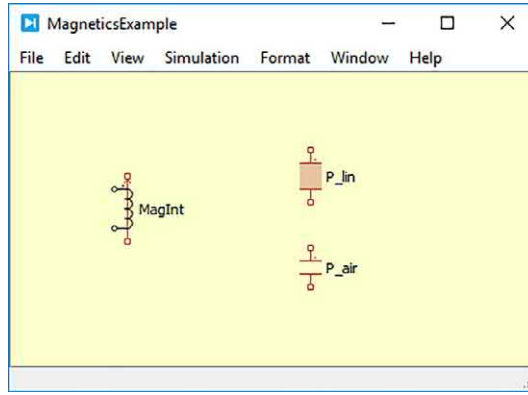



**FIG. 7.17** Addition of Linear Core and Air Gap blocks to the simulation file.

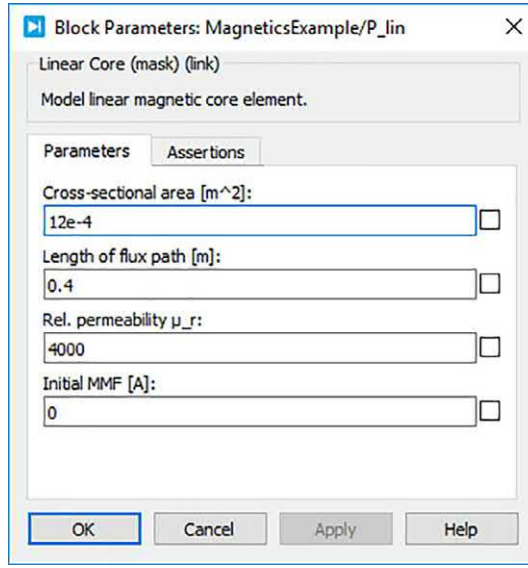



**FIG. 7.18** Settings of Linear Core block.

Drag and drop the Air Gap block onto the Probe block (Fig. 7.23).

After the drag and drop, the Probe Editor window will appear. Select the Flux density (Fig. 7.24).

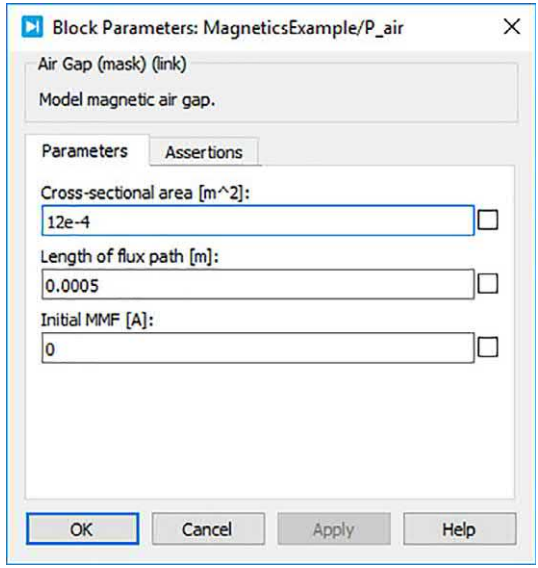



**FIG. 7.19** Setting of Air Gap block.

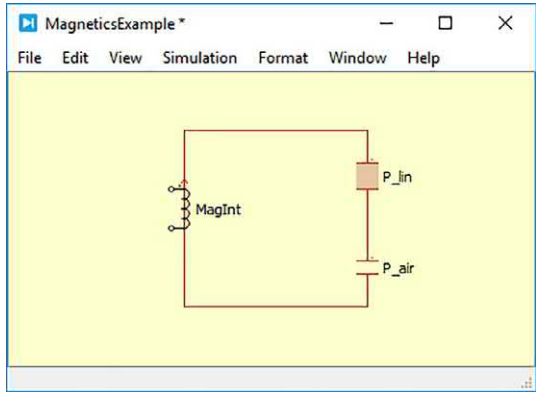



**FIG. 7.20** Components are connected together. When you move the mouse pointer behind the magnetic components terminals, the mouse pointer changes to crosshair, which lets you connect the terminal to other terminals.

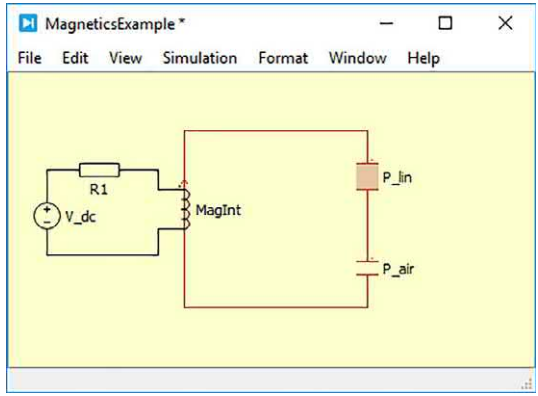



**FIG. 7.21** Addition of input DC source and a resistor. The resistor simulates the copper loss of windings.

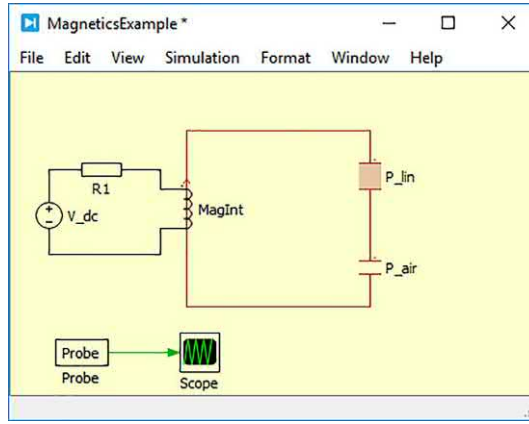



**FIG. 7.22** Signals of the circuit are monitored with the aid of Probe block.

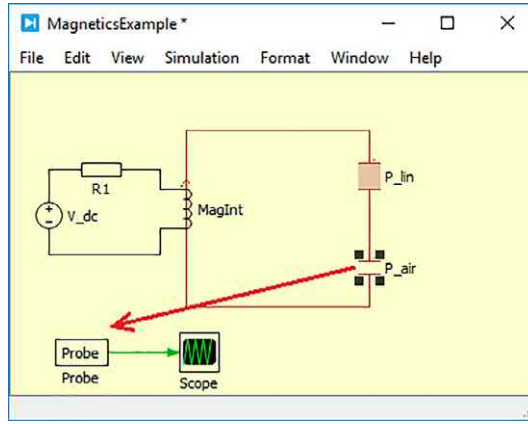



**FIG. 7.23** Drag the Air Gap block onto the Probe block.

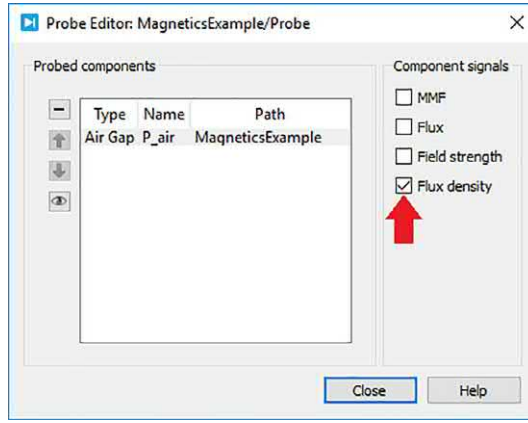



**FIG. 7.24** The Probe Editor block.

Run the simulation with the settings shown in Fig. 7.25. The simulation result is shown in Fig. 7.26. The steady-state flux density of air gap is about 0.5 T.

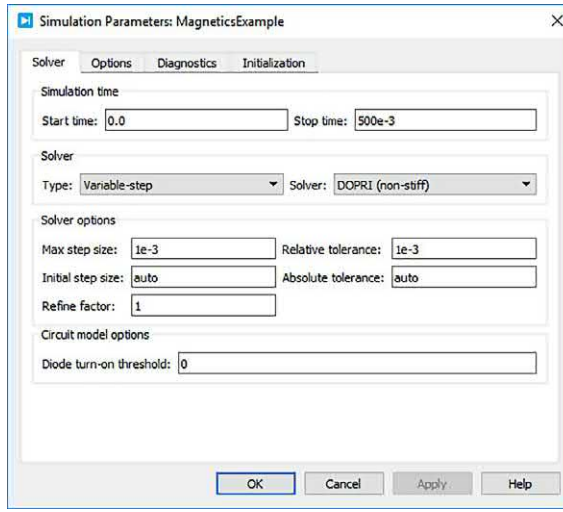



**FIG. 7.25** The simulation is done with the shown settings.

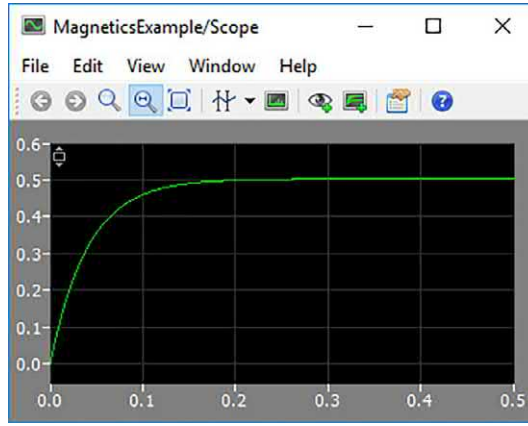



**FIG. 7.26** Flux density in the air gap vs. time.

You can see the circuit current as well. In order to see the circuit current, add another Probe block to the schematic. Connect the placed Probe block to a Scope block (Fig. 7.27). Drag and drop the resistor R1 onto the Probe block. When Probe Editor appears, select the Resistor current.

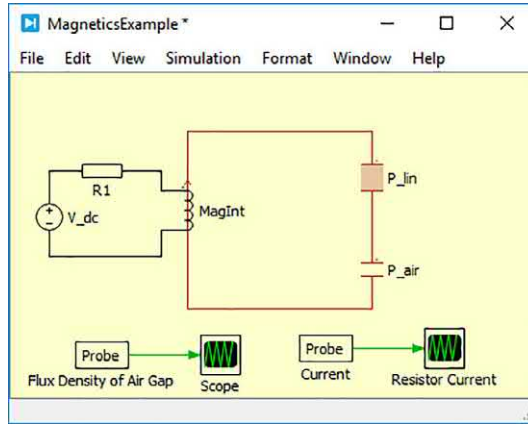



**FIG. 7.27** A Probe block is added to the simulation file in order to monitor the current in the winding.

The resistor current is shown in Fig. 7.28. We can use this Fig. in order to calculate the inductance of the configuration shown in Fig. 7.14. The time constant of current can be found by finding the time where the current reaches 0.63 of final value. The final value is 0.6 A. So, we search for the point, which the current reaches $0.63 \times 0.6 = 0.378$ A. At $t \approx 0.0396$ s, the current reaches 0.378 A (cursors are used to find the time point, which current reaches 0.378 A). So, according to $\tau = \frac{L}{R}$, the inductance is $L = 0.396$ H. Calculated value is quite close to the hand calculations.

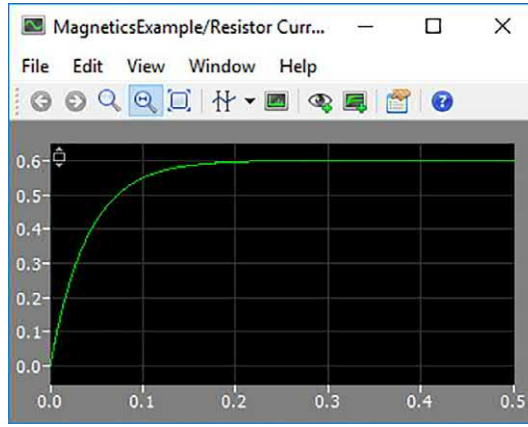



**FIG. 7.28** The current inside the winding.

You can use the MMF Meter block to measure the magnetomotive forces. Two MMF Meter blocks are connected to Linear Core and Air Gap blocks to measure their magnetomotive forces (Fig. 7.29).

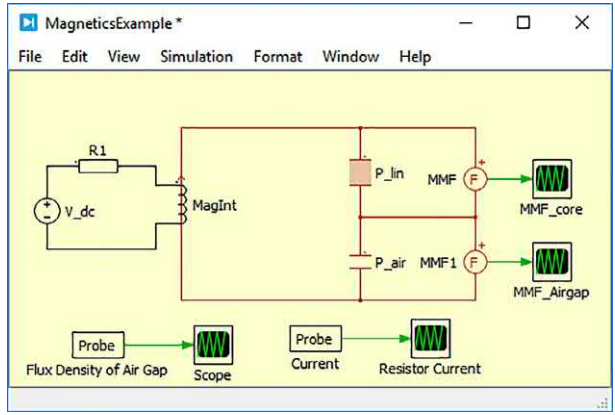



**FIG. 7.29** The magnetomotive forces can be measured with the aid of MMF Meter block.

Measured magnetomotive forces are shown in Figs. 7.30 and 7.31. The steady-state values of magnetomotive forces are the same as hand calculations.

The Flux Rate Meter measures the rate of change of magnetic flux ($\dot{\varphi}$) through the components. We can use this block to measure the voltage induced across the windings. According to Faraday's law of induction, $v = N\frac{d\varphi}{dt}$. The $\frac{d\varphi}{dt}$ is measured with the aid of Flux Rate Meter. So, if we multiply the output of Flux Rate Meter by the number of turns, we obtain the induced voltage across the windings. The schematic shown in Fig. 7.32 uses this technique to measure the induced voltage. The induced voltage is measured with the aid of a volt meter as well (Fig. 7.33). The output of two measurements is the same.

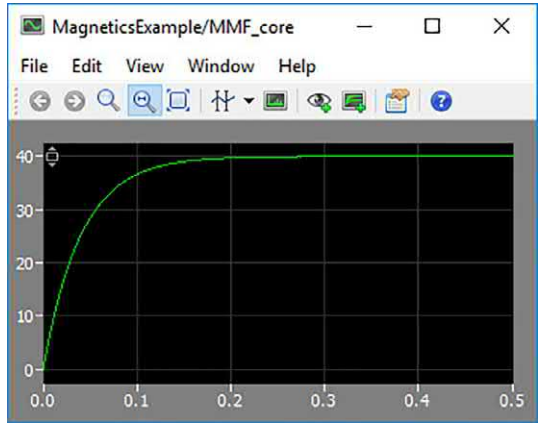



**FIG. 7.30** Magnetomotive force across the Linear Core block.

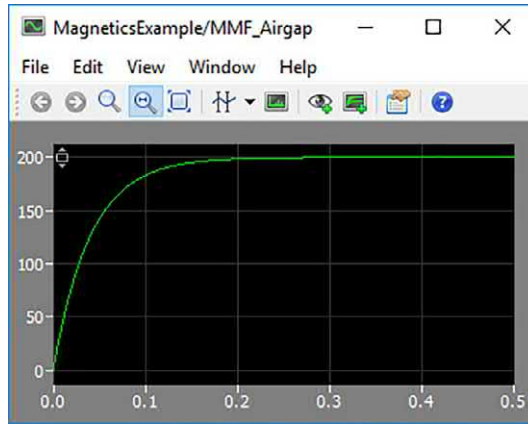



**FIG. 7.31** Magnetomotive force across the Air Gap block.

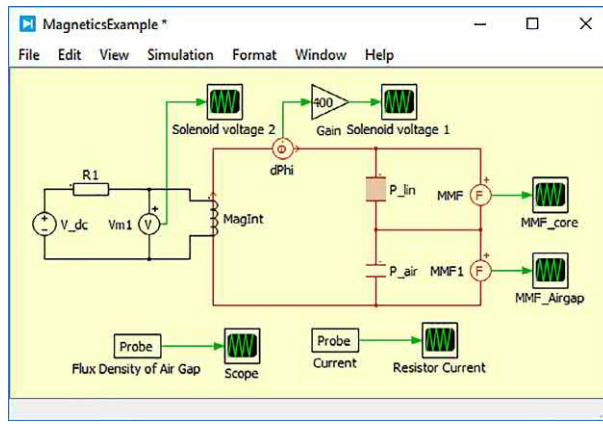



**FIG. 7.32** Measurement of voltage induced across the winding.

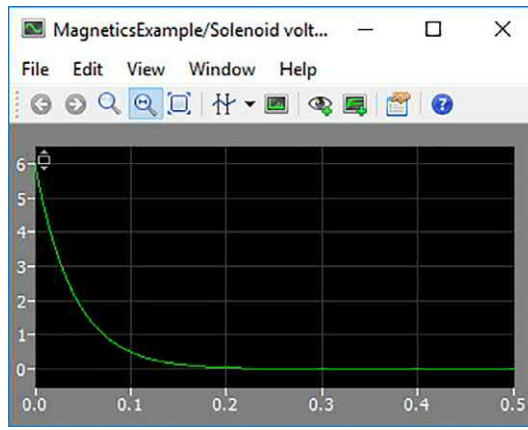



**FIG. 7.33** Graph of produced voltage across the winding.

## 7.6 Where to go next?

PLECS® and world of power electronics simulation seems endless. If you followed the book up to this point, you learned the fundamentals and you can continue. One logical question is: "Where to go next?" Here we try to give you some idea.

PLECS® has a folder named demos (Fig. 7.34). It contains plenty of simulations. It can be a good source of inspiration.

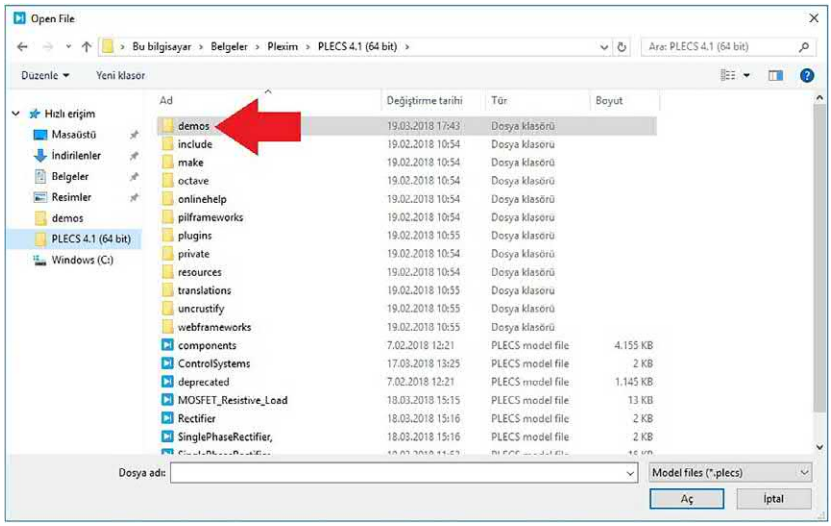



**FIG. 7.34** PLECS comes with plenty of demo simulations placed at the demo folder.

Visit PLECS® website regularly. It contains tutorial videos, academic programs, news, etc. (Figs. 7.35 and 7.36).

Do not forget to refer to PLECS® documentation (Fig. 7.37).

Visit "User forum" to see the question and answers about the PLECS®. You can even ask your questions there (Fig. 7.38)

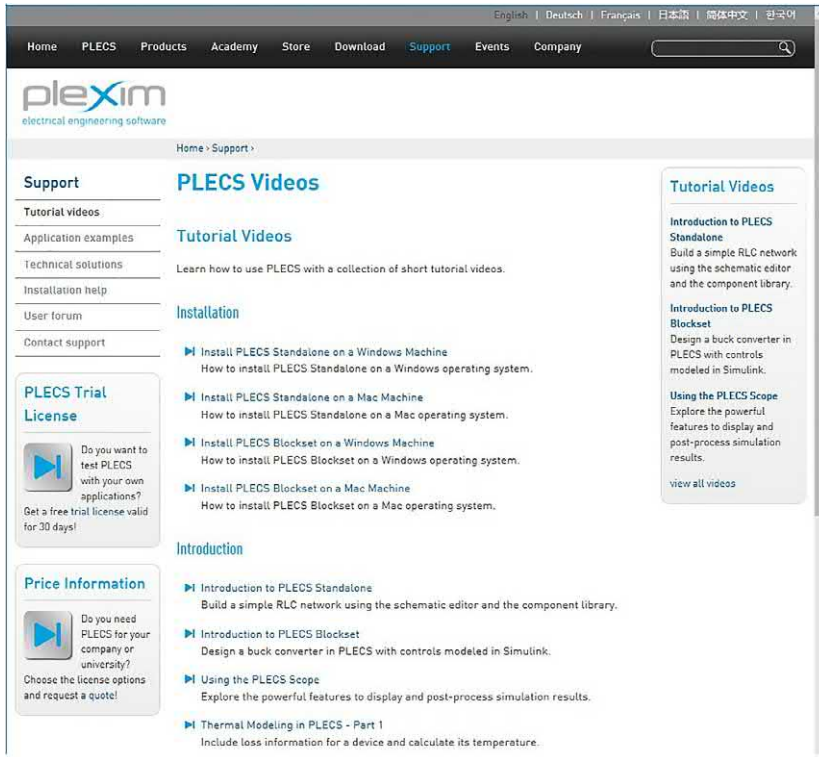



**FIG. 7.35** https://www.plexim.com/support/videos.

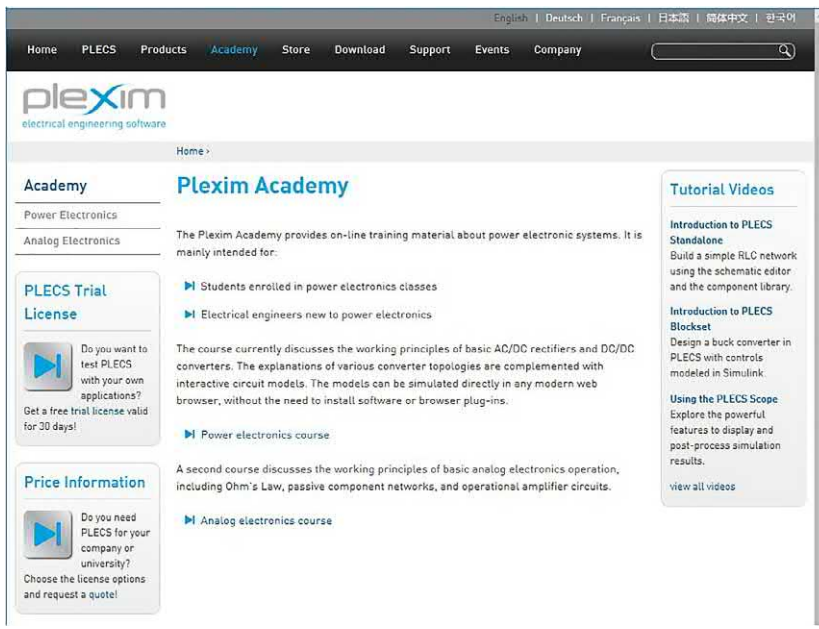



**FIG. 7.36** https://www.plexim.com/academy.

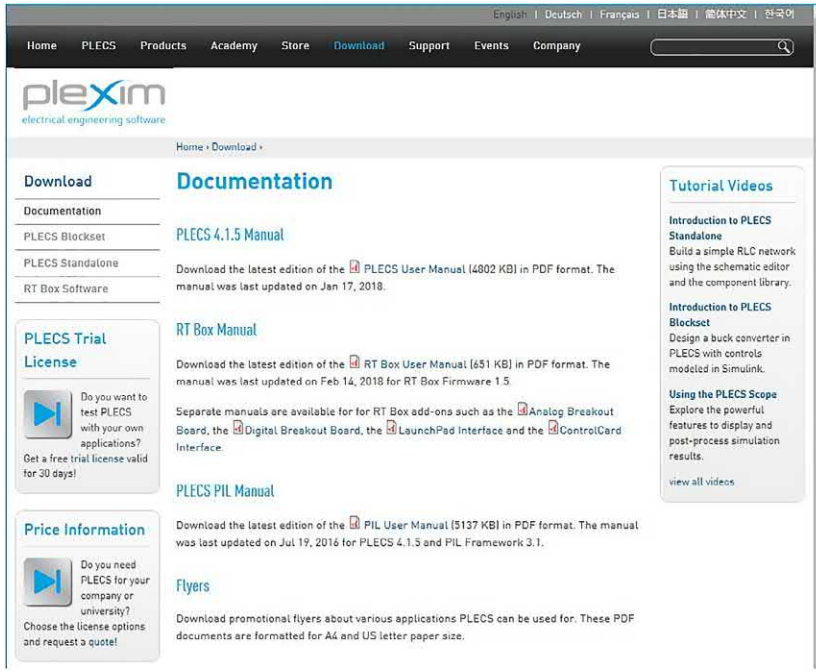



**FIG. 7.37** https://www.plexim.com/download/documentation.


**FIG. 7.38** PLECS® website has a user forum section.

## Reference

[1] S.J. Chapman, Electric Machinery Fundamentals, McGraw Hill, 2011.

## Further reading

[2] K. Watanabe, F. Campelo, Y. Iijima, K. Kawano, T. Matsuo, T. Mifune, H. Igarash, Optimization of inductors using evolutionary algorithms and its experimental validation, IEEE Trans. Magnet. 46 (8) (2010)August.

Chapter 8

# Fundamental concepts of power electronic circuits

## Chapter outline



**Simulation of Power Electronics Converters Using PLECS®. https://doi.org/10.1016/B978-0-12-817364-0.00008-4**

## 8.1 Introduction

In the previous chapters, we showed how PLECS® can be used to analyze different power electronics converters. This is the last chapter of book and it will study some of the important theories of power electronics circuits. We focus on theories, which help the reader understand the example circuits of previous chapters better. Plenty of good power electronics references are available in the market. [1] is a good textbook with plenty of numeric examples. It is quite useful for a first course on power electronics, since the concepts are described clearly. [2-4] are more advanced books and suggested to advanced readers. [5] and [6] are good references for readers interested in DC-DC converters. [7] is a good reference for readers interested in inverters.

It is a good idea to do some hand analysis for the circuit drawn in the simulator environment and compare the simulation result with hand analysis. If the results are different, try to find the source of discrepancy. For instance, when someone analyzes a half-wave rectifier, generally the voltage drop of diodes is neglected. So, the simulation result (which considers the voltage drop of diodes) is not the same as hand analysis. Such practices help you to understand the power electronics concepts better.

## 8.2 Instantaneous power

The instantaneous power of a device ($p(t)$) is defined as:

$$p(t) = v(t) \times i(t), \tag{8.1}$$

where $v(t)$ is the voltage across the device and $i(t)$ is the current through the device. The instantaneous power is generally a time-varying quantity. If the passive sign convention illustrated in Fig. 8.1A is observed, the device is absorbing power if $p(t)$ is positive at a specified value of time $t$. The device is supplying power if $p(t)$ is negative.

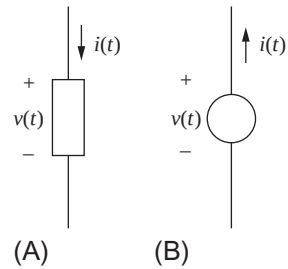



**FIG. 8.1** (A) Passive sign convention: $p(t) > 0$ indicates power is being absorbed; (B) $p(t) > 0$ indicates power is being supplied by the source.

For instance, consider the simple circuit shown in Fig. 8.2. In this circuit, $v_{in}(t) = 311\sin(377t)$ and $R = 50\ \Omega$.

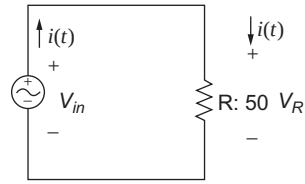



**FIG. 8.2** A simple resistive circuit.

According to Ohm's law, $i(t) = \frac{v_{in}(t)}{R} = 6.22\sin(377t)$ and instantaneous power for resistor $R$ is:

$$p_R(t) = 311\sin(377t) \times 6.22\sin(377t) = 2345\sin^2(377t). \tag{8.2}$$

Obtained result is positive for all the times, i.e., $\forall t$, $\sin^2(377t) > 0$. This is expected since resistor dissipates power.

The instantaneous power of AC source can be calculated with the aid of Fig. 8.3.

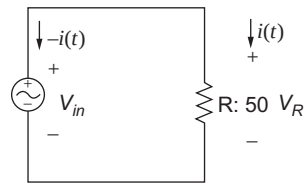



**FIG. 8.3** Calculation of instantaneous power of input AC source.

The instantaneous power of AC source is:

$$p_{V_{in}}(t) = 311\sin(377t) \times -6.22\sin(377t) = -2345\sin^2(377t) \tag{8.3}$$

Obtained result is negative for all the time. We expect this result since the AC source supplies the power into the load. For instance at $t = 12$ ms, $p_{V_{in}}(t) = -2.263$ kW, and $p_R(t) = +2.263$ kW. This means that at $t = 12$ ms, AC source supplies 2.263 kW and resistor absorbs 2.263 kW. Fig. 8.4 shows the instantaneous power waveforms on the same graph.

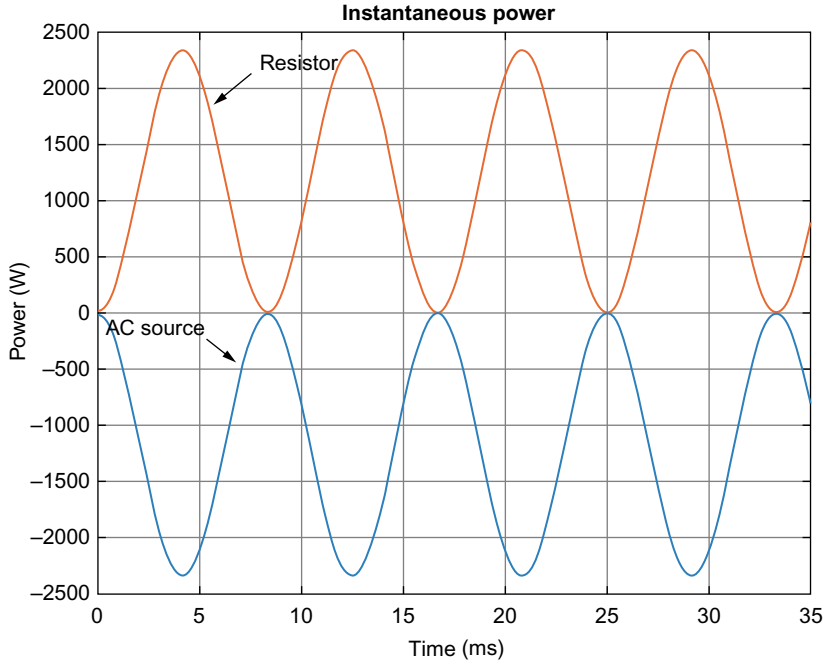



**FIG. 8.4** Graph of instantaneous power for input AC source and load resistor. The instantaneous power of AC source is negative since it supplies power to the resistor. The resistor instantaneous power is positive since it consumes power.

## 8.3 Average power

Function $f(t)$ is periodic if,

$$\exists T > 0, \forall t f(t+T) = f(t) \tag{8.4}$$

T is called the period. For instance, $f(t) = \sin(t)$ is periodic since $f(t+2\pi) = f(t)$.

If device voltage ($v(t)$) and current ($i(t)$) are periodic, i.e., $v(t) = v(t+T)$ and $i(t) = i(t+T)$, then the instantaneous power will be a periodic since

$$p(t) = v(t) \times i(t)$$
$$p(t+T) = v(t+T) \times i(t+T) = v(t) \times i(t) = p(t) \tag{8.5}$$

The average power for such a periodic waveform is defined as:

$$P = \frac{1}{T}\int_{t_0}^{t_0+T} p(t)dt = \frac{1}{T}\int_{t_0}^{t_0+T} v(t) \times i(t)dt \tag{8.6}$$

Assume that $v(t)$ is a constant function, i.e., $v(t) = V_{dc}$. In this case, the average power can be calculated by the

$$P = \frac{1}{T}\int_{t_0}^{t_0+T} v(t) \times i(t)dt = \frac{1}{T}\int_{t_0}^{t_0+T} V_{dc} \times i(t)dt = V_{dc}\left[\frac{1}{T}\int_{t_0}^{t_0+T} i(t)dt\right] = V_{dc}I_{avg} \tag{8.7}$$

The average power for constant $i(t)$, i.e., $i(t)=I_{dc}$ can be found in the same way.

$$P=\frac{1}{T}\int_{t_0}^{t_0+T} v(t)\times i(t)dt=\frac{1}{T}\int_{t_0}^{t_0+T} v(t)\times I_{dc}dt=I_{dc}\left[\frac{1}{T}\int_{t_0}^{t_0+T} v(t)dt\right]=I_{dc}v_{avg} \tag{8.8}$$

## 8.4 Effective value of a signal

Consider the simple circuit shown in Fig. 8.5. The input source is a periodic voltage source, i.e., $v(t+T)=v(t)$. The load is purely resistive.

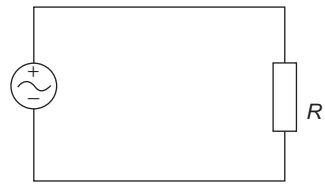



**FIG. 8.5** A resistor is connected to a periodic voltage source.

The power consumed by the resistor is:

$$P=\frac{1}{T}\int_0^T p(t)dt=\frac{1}{T}\int_0^T v(t)\times i(t)dt=\frac{1}{T}\int_0^T \frac{v(t)^2}{R}dt=\frac{1}{R}\left[\frac{1}{T}\int_0^T v(t)^2dt\right] \tag{8.9}$$

Now consider the circuit shown in Fig. 8.6. The input source is a constant DC voltage source, i.e., $v(t)=V_{dc}$.

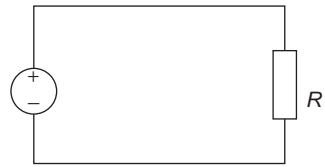



**FIG. 8.6** The same resistor (as the one in Fig. 8.5) is connected to a DC source.

In this case, the power consumed by the resistor is $\frac{{V_{dc}}^2}{R}$. Power consumption of both circuits is the same when $V_{dc}=\sqrt{\frac{1}{T}\int_0^T v(t)^2dt}$. Since,

$$\frac{1}{R}\left[\frac{1}{T}\int_0^T v(t)^2dt\right]=\frac{{V_{dc}}^2}{R}\Longrightarrow V_{dc}=\sqrt{\frac{1}{T}\int_0^T v(t)^2dt} \tag{8.10}$$

The $\sqrt{\frac{1}{T}\int_0^T v(t)^2 dt}$ is called Root Mean Square (RMS) or effective value of signal $v(t)$. So, RMS value of periodic signal $v(t)$ is a DC value, which produces the same amount of heat in the resistive load as the periodic signal $v(t)$.

The RMS can be defined for the current waveforms as well.

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i(t)^2 dt} \tag{8.11}$$

**Example 8.1** Determine the rms value of the periodic pulse waveform shown in Fig. 8.7.

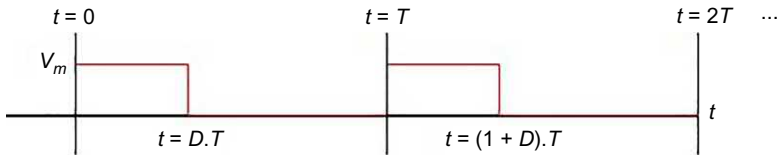



**FIG. 8.7** Waveform of Example 8.1.

**Solution**

$$v(t) = \begin{cases} V_m & 0 < t < DT \\ 0 & DT < t < T \end{cases}$$

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v(t)^2 dt} = \sqrt{\frac{1}{T}\left(\int_0^{DT} {V_m}^2 dt + \int_{DT}^T 0 dt\right)} = \sqrt{\frac{1}{T}\left({V_m}^2 DT\right)} = V_m\sqrt{D}$$

**Example 8.2** Determine the RMS values of the following waveforms $\left(\omega = \frac{2\pi}{T}\right)$.

**(a)** $v(t) = V_m \sin(\omega t)$.

**(b)** $v(t) = |V_m \sin(\omega t)|$.

**(c)** $v(t) = \begin{cases} V_m \sin(\omega t) & 0 < t < \dfrac{T}{2} \\ 0 & \dfrac{T}{2} < t < T \end{cases}$.

**Solution**

**(a)**

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T (V_m \sin(\omega t))^2 dt} = \sqrt{\frac{1}{T} \times {V_m}^2 \int_0^T \sin^2(\omega t) dt} = \sqrt{\frac{{V_m}^2}{T}\int_0^T \frac{1-\cos(2\omega t)}{2} dt}$$

$$= \sqrt{\frac{{V_m}^2}{T}\int_0^T \frac{1}{2} dt - \int_0^T \frac{\cos(2\omega t)}{2} dt}$$

$$= \sqrt{\frac{{V_m}^2}{T} \times \left(\frac{T}{2} - \frac{\sin(2\omega t)}{4\omega}\right)\Big|_0^T}$$

$$= \sqrt{\frac{{V_m}^2}{T} \times \frac{T}{2} - 0}$$

$$= \sqrt{\frac{{V_m}^2}{2}}$$

$$= \frac{V_m}{\sqrt{2}}$$

**(b)** RMS value of $v(t) = |V_m \sin(\omega t)|$ is the same as $v(t) = V_m \sin(\omega t)$. Since $(|V_m \sin(\omega t)|)^2 = (V_m \sin(\omega t))^2$. So, RMS value of $v(t) = |V_m \sin(\omega t)|$ is $\frac{V_m}{\sqrt{2}}$. Graph of $v(t) = |V_m \sin(\omega t)|$ is shown in Fig. 8.8. Such a waveform is called Full-Wave Rectified in power electronics.

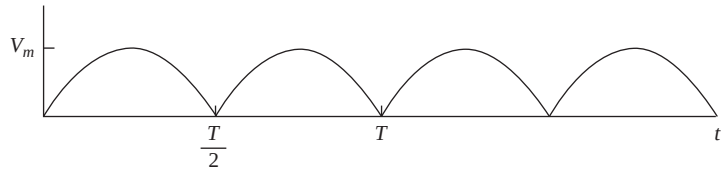



**FIG. 8.8** Full-wave rectified sinusoidal waveform.

**(c)** Graph of $v(t) = \begin{cases} V_m \sin(\omega t) & 0 < t < \frac{T}{2} \\ 0 & \frac{T}{2} < t < T \end{cases}$ is shown in Fig. 8.9. Such a waveform is called Half-Wave Rectified in power electronics.

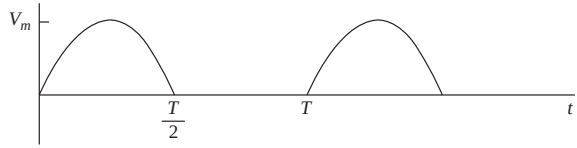



**FIG. 8.9** Half-wave rectified sinusoidal waveform.

$$V_{rms} = \sqrt{\frac{1}{T}\left(\int_0^{\frac{T}{2}} (V_m \sin(\omega t))^2 dt + \int_{\frac{T}{2}}^{T} 0 dt\right)} = \sqrt{\frac{1}{T} \times {V_m}^2 \int_0^{\frac{T}{2}} \sin^2(\omega t) dt}$$

$$= \sqrt{\frac{{V_m}^2}{T} \int_0^{\frac{T}{2}} \frac{1-\cos(2\omega t)}{2} dt} = \sqrt{\frac{{V_m}^2}{T} \int_0^{\frac{T}{2}} \frac{1}{2} dt - \int_0^{\frac{T}{2}} \frac{\cos(2\omega t)}{2} dt}$$

$$= \sqrt{\frac{{V_m}^2}{T} \times \left(\frac{t}{2} - \frac{\sin(2\omega t)}{4\omega}\right)\Big|_0^{\frac{T}{2}}}$$

$$= \sqrt{\frac{{V_m}^2}{T} \times \frac{T}{4} - 0}$$

$$= \sqrt{\frac{{V_m}^2}{4}}$$

$$= \frac{V_m}{2}$$

RMS of triangular waveshapes can be calculated using the formulas shown in Fig. 8.10.

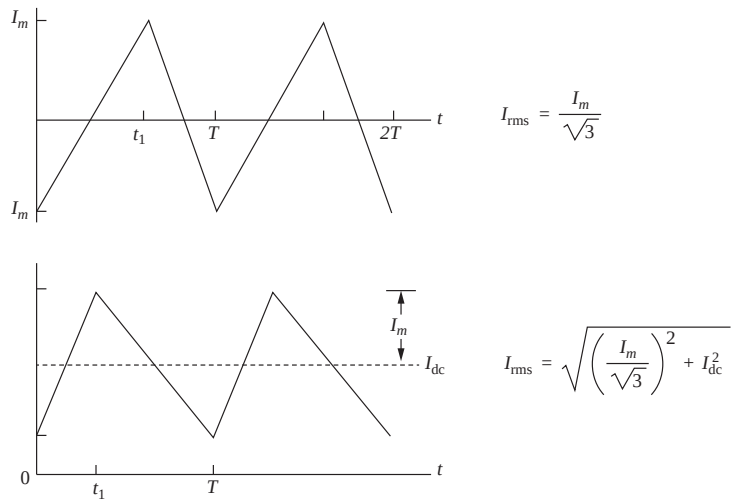



**FIG. 8.10** RMS value of triangular waveforms.

### 8.4.1 Effective value of sum of two periodic signals

Consider two periodic waveforms, i.e., $v_1(t+T)=v_1(t)$, $v_2(t+T)=v_2(t)$. The RMS value of sum of two waveforms ($v(t)=v_1(t)+v_2(t)$) is:

$$\begin{aligned} V_{rms}{}^2 &= \frac{1}{T}\int_0^T (v_1+v_2)^2 dt = \frac{1}{T}\int_0^T \left(v_1{}^2 + 2v_1v_2 + v_2{}^2\right) dt \\ &= \frac{1}{T}\int_0^T v_1{}^2 dt + \frac{1}{T}\int_0^T 2v_1v_2 dt + \frac{1}{T}\int_0^T v_2{}^2 dt \end{aligned} \tag{8.12}$$

Sometime, the $\frac{1}{T}\int_0^T v_1(t)v_2(t)dt$ term is zero. The $\frac{1}{T}\int_0^T v_1(t)v_2(t)dt$ is the inner product of $v_1(t)$ and $v_2(t)$. When $\frac{1}{T}\int_0^T v_1(t)v_2(t)dt = 0$, the signals $v_1(t)$ and $v_2(t)$ are called orthogonal. Table 8.1 shows some of the important orthogonal functions.

**TABLE 8.1** Some of the important orthogonal functions ($\omega=\frac{2\pi}{T}$, $n\neq m$, and $k$ is a constant).

| No | $v_1(t)$ | $v_2(t)$ |
|---|---|---|
| 1 | $\sin(n\times\omega\times t+\varphi_1)$ | $\sin(m\times\omega\times t+\varphi_2)$ |
| 2 | $\sin(n\times\omega\times t+\varphi_1)$ | $\cos(m\times\omega\times t+\varphi_2)$ |
| 3 | $\cos(n\times\omega\times t+\varphi_1)$ | $\cos(m\times\omega\times t+\varphi_2)$ |
| 4 | $\sin(n\times\omega\times t+\varphi_1)$ | $k$ |
| 5 | $\cos(m\times\omega\times t+\varphi_1)$ | $k$ |

For instance according to the second row of the table, $\sin(n\times\omega\times t+\varphi_1)$ and $\cos(m\times\omega\times t+\varphi_2)$ (when $n\neq m$) are orthogonal since $\frac{1}{T}\int_0^T \sin(n\omega t+\varphi_1)\times\cos(m\omega t+\varphi_2)dt = 0$.

For orthogonal functions,

$$V_{rms}{}^2 = \frac{1}{T}\int_0^T (v_1+v_2)^2 dt = \frac{1}{T}\int_0^T \left(v_1{}^2 + 2v_1v_2 + v_2{}^2\right) dt$$

$$V_{rms}{}^2 = \frac{1}{T}\int_0^T v_1{}^2 dt + \frac{1}{T}\int_0^T 2v_1v_2 dt + \frac{1}{T}\int_0^T v_2{}^2 dt$$

$$V_{rms}{}^2 = \frac{1}{T}\int_0^T v_1{}^2 dt + \frac{1}{T}\int_0^T v_2{}^2 dt$$

$$V_{rms} = \sqrt{V_{1,rms}{}^2 + V_{2,rms}{}^2} \tag{8.13}$$

RMS value of sum of more than two orthogonal functions (every two terms are assumed to be orthogonal) can be calculated in the same way:

$$\left(v(t)=\sum_{n=1}^{N}v_n(t)\forall k,\, l\; 1\le k\le N,\, 1\le l\le N,\, k\ne l,\; \frac{1}{T}\int_0^T v_k(t)v_l(t)dt=0\right)\Longrightarrow V_{rms}$$
$$=\sqrt{{V_{1,rms}}^2+{V_{2,rms}}^2+{V_{3,rms}}^2+\ldots}=\sqrt{\sum_{n=1}^{N}{V_{n,rms}}^2} \tag{8.14}$$

**Example 8.3** Determine the RMS value of $v(t)=4+8\sin(\omega_1 t+10°)+5\sin(\omega_2 t+50°)$ under the following conditions.

**(a)** $\omega_2=2\omega_1$
**(b)** $\omega_2=\omega_1$

**Solution**

**(a)** When $\omega_2=2\omega_1$, the $v(t)=4+8\sin(\omega_1 t+10°)+5\sin(2\omega_1 t+50°)$. According to Table 8.1, all the functions are orthogonal to each other, so

$$V_{rms}=\sqrt{{V_{1,rms}}^2+{V_{2,rms}}^2+{V_{3,rms}}^2}=\sqrt{4^2+\left(\frac{8}{\sqrt{2}}\right)^2+\left(\frac{5}{\sqrt{2}}\right)^2}=7.78\,\text{V}$$

**(b)** When $\omega_2=\omega_1$, the $v(t)=4+8\sin(\omega_1 t+10°)+5\sin(\omega_1 t+50°)$. $8\sin(\omega_1 t+10°)$ and $5\sin(\omega_1 t+50°)$ are not orthogonal to each other. So, we can't use the previous formulas. Note that $a\times\sin(\omega t)+b\times\cos(\omega t)=\sqrt{a^2+b^2}\sin\left(\omega t+\tan^{-1}\left(\frac{b}{a}\right)\right)$. So,

$$v(t)=4+8\sin(\omega_1 t+10°)+5\sin(\omega_1 t+50°)=4+12.3\sin(\omega_1 t+25.2°)$$

The two terms of last equation are orthogonal to each other (see Table 8.1). So, the RMS is

$$V_{rms}=\sqrt{4^2+\left(\frac{12.3}{\sqrt{2}}\right)^2}=9.57\,V$$

**Example 8.4** In this example, we show how RMS values can be calculated with the aid of MATLAB®. Assume

$v(t)=311\sin(2\pi\times 60t)+100\sin(2\pi\times 2\times 60t)+20\sin(2\pi\times 3\times 60t)$ is given. The RMS can be calculated easily:

$$V_{rms}=\sqrt{\left(\frac{311}{\sqrt{2}}\right)^2+\left(\frac{100}{\sqrt{2}}\right)^2+\left(\frac{20}{\sqrt{2}}\right)^2}=231.43\,V$$

The commands shown in Fig. 8.11 calculate the RMS value of given signal. The first two lines sample a period of given signal. The sampling time is $\frac{1}{6000} = 166.7\mu s$. The `rms` command is used to calculate the RMS value of sampled signal.

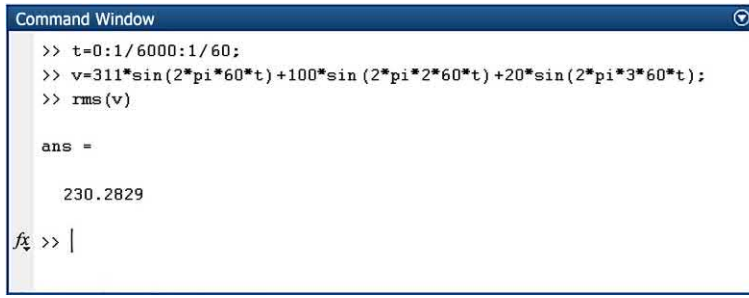



**FIG. 8.11** Calculation of RMS value of $v(t) = 311\sin(2\pi \times 60t) + 100\sin(2\pi \times 2 \times 60t) + 20\sin(2\pi \times 3 \times 60t)$ with $\frac{1}{6000}$ steps.

The result is 230.283, which is a little bit lower than the expected value of 231.43. If you decrease the sampling time from 166.7 μs to 16.67 μs, you get a more accurate result (Fig. 8.12).

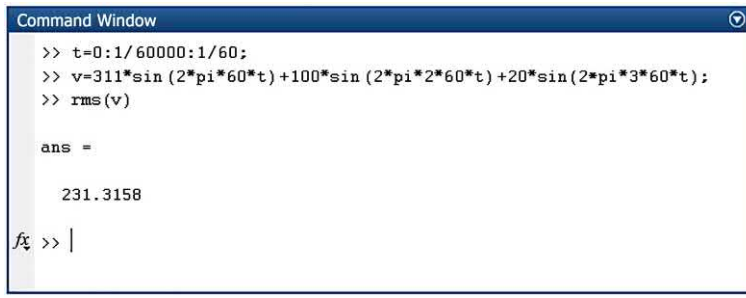



**FIG. 8.12** Calculation of RMS value of $v(t) = 311\sin(2\pi \times 60t) + 100\sin(2\pi \times 2 \times 60t) + 20\sin(2\pi \times 3 \times 60t)$ with $\frac{1}{60000}$ steps.

### 8.4.2 Measurement of RMS of signals

The cheap multimeters are not suitable devices to measure the RMS value of signals inside a power electronics converter. The cheap multimeters are able to measure the RMS value of pure sinusoidal signals, i.e., the one shown in Fig. 8.13.

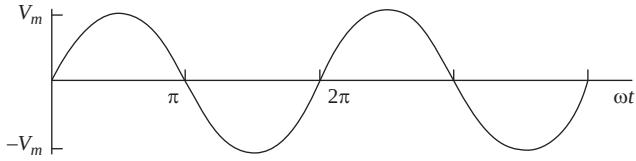



**FIG. 8.13** Pure sinusoidal waveform.

Fig. 8.14 shows one of the methods that a cheap multimeter uses to measure the RMS of a signal. $V_X$ is the signal under measurement. Assume that $V_X$ is a pure sinusoidal waveform, i.e., a signal such as the one shown in Fig. 8.13. Then the capacitor is charged up to Vm Volts (voltage drop of diode is neglected), where Vm is the peak value of voltage under measurement. So, Analog-to-Digital converter reads the maximum of input signal. The read value is simply multiplied by $\frac{1}{\sqrt{2}}$, and the result, i.e., $\frac{Vm}{\sqrt{2}}$, is the RMS value of input signal. This method only works for pure sinusoidal signals and doesn't produce correct result if the input signal is not pure sinusoidal.

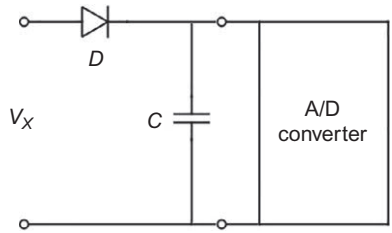



**FIG. 8.14** A simple circuit for detection of input AC signal peak value.

The expensive multimeters sample the input waveform and use a processor to calculate the RMS value. So, the waveshape of input signal doesn't affect the measurements. Such a multimeter has "TRUE RMS" label on it. So, ensure that your multimeter is TRUE RMS type if you want to measure the RMS of a signal of a power electronics converters. Digital oscilloscopes can be used to measure the RMS of signals as well.

## 8.5 Apparent power and power factor

Apparent power ($S$) is the product of RMS of voltage and RMS of current magnitudes.

$$S = V_{rms} \times I_{rms} \tag{8.15}$$

The power factor of a load is defined as the ratio of average power to apparent power:

$$\text{pf} = \frac{P}{S} = \frac{\text{P}}{\text{V}_{\text{rms}}\text{I}_{\text{rms}}} \tag{8.16}$$

The equation can be used to analyze both the linear circuits and nonlinear circuits. In the linear circuit case, $PF = cos(\alpha)$, where $\alpha$ shows the phase angle between the voltage and current sinusoids.

## 8.6 Power computations for linear circuits

The steady-state voltages and currents of a linear circuit, which has sinusoidal AC sources, are sinusoidal. Assume an element with the following voltage and current,

$$\begin{aligned} v(t) &= V_m \cos(\omega t + \theta) \\ i(t) &= I_m \cos(\omega t + \varphi) \end{aligned} \tag{8.17}$$

Then the instantaneous power is:

$$p(t) = v(t)i(t) = [V_m \cos(\omega t + \theta)][I_m \cos(\omega t + \varphi)] \tag{8.18}$$

According to basic trigonometric identities:

$$(\cos A)(\cos B) = \frac{1}{2}[\cos(A+B) + \cos(A-B)] \tag{8.19}$$

So, instantaneous power can be written as:

$$p(t) = \left(\frac{V_m I_m}{2}\right)[\cos(2\omega t + \theta + \varphi) + \cos(\theta - \varphi)] \tag{8.20}$$

The average power can be calculated easily:

$$\begin{aligned} p(t) &= \frac{1}{T}\int_0^T p(t)dt = \left(\frac{V_m I_m}{2}\right)\int_0^T [\cos(2\omega t + \theta + \varphi) + \cos(\theta - \varphi)]dt \\ &= \left(\frac{V_m I_m}{2}\right)\cos(\theta - \varphi) = V_{rms} I_{rms} \cos(\theta - \varphi) \end{aligned} \tag{8.21}$$

So, the power factor of circuit is $\frac{V_{rms} I_{rms} \cos(\theta - \varphi)}{V_{rms} I_{rms}} = \cos(\theta - \varphi)$. The average power (measured with units of Watts, W) is the part of power, which is consumed by the resistors in the circuit. In the steady state, no net power is absorbed by an inductor or a capacitor. The term reactive power (measured with units of Volt Ampere Reactive, VAR) is commonly used in conjunction with voltages and currents for inductors and capacitors. Reactive power is characterized by energy storage during one-half of the cycle and energy retrieval during the other half. Reactive power (Q) is calculated as:

$$Q = V_{rms} I_{rms} \sin(\theta - \varphi) \tag{8.22}$$

By convention, inductors absorb positive reactive power and capacitors absorb negative reactive power.

Complex Power (measured with units of Volt Ampere, VA) is defined as ($j = \sqrt{-1}$):

$$\boldsymbol{S} = P + jQ \tag{8.23}$$

Apparent power is the magnitude of complex power:

$$S = |\boldsymbol{S}| = \sqrt{P^2 + Q^2} \tag{8.24}$$

**Example 8.5** In the following circuit, $v_1(t) = 311\sin(2 \times \pi \times 50 \times t)$, $L = 0.1\ H$ ve $R = 40\ \Omega$. Determine the apparent power, average (active) power, reactive power, and power factor (Fig. 8.15).

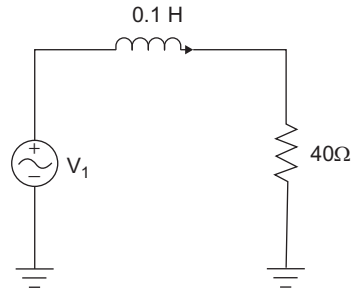



**FIG. 8.15** Circuit of Example 8.5.

**Solution:**

$$\mathrm{Z} = \mathrm{R} + \mathrm{j} \times \mathrm{L} \times \omega = 40 + 31.415\mathrm{j}$$

$$\varphi = \tan^{-1}\left(\frac{L\omega}{\mathrm{R}}\right) = \tan^{-1}\left(\frac{31.415}{40}\right) = 38.14^\circ = 0.666\,\mathrm{Rad}$$

$$\mathbf{V} = \frac{311}{\sqrt{2}} < 0^\circ = 219.92 \measuredangle 0^\circ$$

$$\mathbf{I} = \frac{\mathrm{V}}{\mathrm{Z}} = \frac{219.92\mathrm{e}^{\mathrm{j}0}}{40 + 31.42\mathrm{j}} = 3.4 - 2.67\mathrm{j} = 4.323\mathrm{e}^{-0.666\mathrm{j}}$$

$$\mathrm{S} = |\mathbf{V} \times \mathbf{I}| = 950.824\,\mathrm{VA}$$

$$\mathrm{P} = \mathrm{V} \times \mathrm{I} \times \cos(\varphi) = 747.63\,\mathrm{W}$$

$$\mathrm{Q} = \mathrm{V} \times \mathrm{I} \times \sin(\varphi) = 587.46\,\mathrm{VAR}$$

$$\mathrm{PF} = \cos(\varphi) = 0.786$$

## 8.7 Fourier series

A periodic and nonsinusoidal signal $f(t)$ that satisfy certain conditions (Dirichlet conditions) can be written as the sum of sinusoids. The Fourier series of $f(t) = f(t+T)$ can be written as ($\omega_0 = \frac{2\pi}{T}$):

$$f(t) = a_0 + \sum_{n=1}^{\infty} [a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t)] \tag{8.25}$$

where $a_0$, $a_n$, and $b_n$ are

$$\begin{aligned} a_0 &= \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)dt \\ a_n &= \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)\cos(n\omega_0 t)dt \\ b_n &= \frac{2}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)\sin(n\omega_0 t)dt \end{aligned} \tag{8.26}$$

The $a_0 = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)dt$ is called the average value of $f(t)$. The equations can be written in the following forms as well (remember that $a \times \sin(\omega t) + b \times \cos(\omega t) = \sqrt{a^2 + b^2}\sin\left(\omega t + \tan^{-1}\left(\frac{b}{a}\right)\right)$).

(A) Sum of Sines

$$f(t) = a_0 + \sum_{n=1}^{\infty} C_n \sin(n\omega_0 t + \theta_n)$$

$$C_n = \sqrt{{a_n}^2 + {b_n}^2} \text{ and } \theta_n = \tan^{-1}\left(\frac{a_n}{b_n}\right) \tag{8.27}$$

(B) Sum of Cosines

$$f(t) = a_0 + \sum_{n=1}^{\infty} C_n \cos(n\omega_0 t + \theta_n)$$

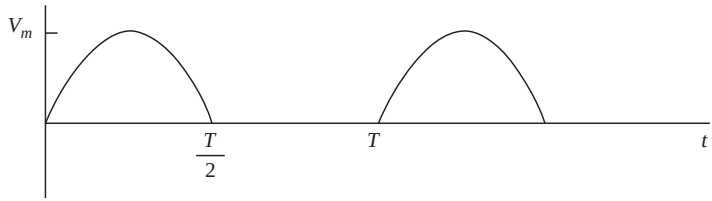
$$C_n = \sqrt{{a_n}^2 + {b_n}^2} \text{ and } \theta_n = \tan^{-1}\left(-\frac{b_n}{a_n}\right) \tag{8.28}$$

The following equation can be used to determine the RMS value of a signal using its Fourier series coefficients.

$$F_{rms} = \sqrt{\sum_{n=0}^{\infty} {F_{n,rms}}^2} = \sqrt{{a_0}^2 + \sum_{n=1}^{\infty}\left(\frac{C_n}{\sqrt{2}}\right)^2} = \sqrt{{a_0}^2 + \sum_{n=1}^{\infty}\left(\frac{{a_n}^2 + {b_n}^2}{2}\right)} \tag{8.29}$$

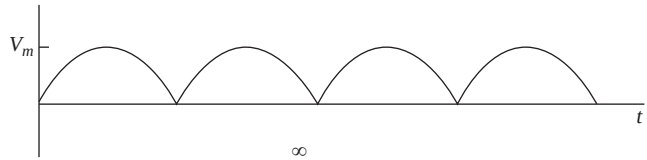
### 8.7.1 Fourier series of important waveshapes

Fourier series of important waveshapes are shown in Figs. 8.16–8.20.




$$v(t) = \frac{V_m}{\pi} + \frac{V_m}{2}\sin(\omega_0 t) - \sum_{n=2,4,6...}^{\infty} \frac{2V_m}{(n^2-1)\pi}\cos(n\omega_0 t)$$

**FIG. 8.16** Fourier series of a half-wave rectified waveform.

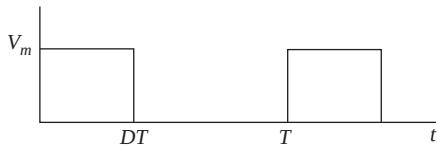



$$v_o(t) = V_o + \sum_{n=2,4,...}^{\infty} V_n \cos(n\omega_0 t + \pi)$$

$$V_o = \frac{2V_m}{\pi}$$

$$V_n = \frac{2V_m}{\pi}\left(\frac{1}{n-1} - \frac{1}{n+1}\right)$$

**FIG. 8.17** Fourier series of a full-wave rectified waveform.



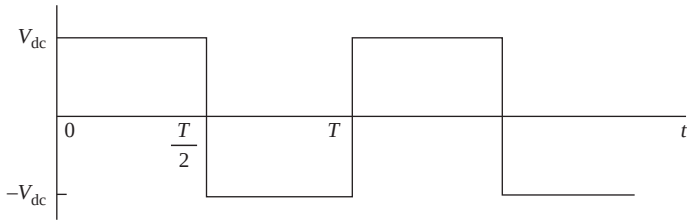

$$v_o(t) = a_0 + \sum_{n=1}^{\infty} [a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t)]$$

$$a_0 = V_m D$$

$$a_n = \left(\frac{V_m}{n\pi}\right)\sin(n2\pi D)$$

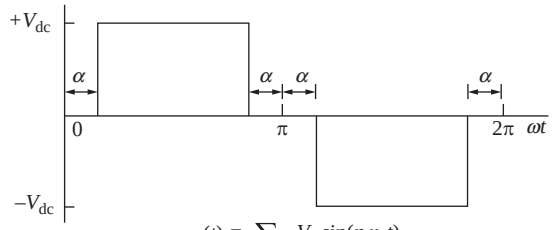
$$b_n = \left(\frac{V_m}{n\pi}\right)[1 - \cos(n2\pi D)]$$

**FIG. 8.18** Fourier series of a pulsed waveform.




$$v_o(t) = \sum_{n=1,3,5,\ldots} \left(\frac{4V_{dc}}{n\pi}\right) \sin(n\omega_0 t)$$

**FIG. 8.19** Fourier series of a square wave.




$$v_o(t) = \sum_{n=1,3,5,\ldots} V_n \sin(n\omega_0 t)$$

$$V_n = \left(\frac{4V_{dc}}{n\pi}\right) \cos(n\alpha)$$

**FIG. 8.20** Fourier series of a modified square wave.

### 8.7.2 Calculation of average power using the Fourier series

Assume that the Fourier series of voltage and current of a element is given as follows

$$v(t) = V_0 + \sum_{n=1}^{\infty} V_n \cos(n\omega_0 t + \theta_n)$$

$$i(t) = I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega_0 t + \varphi_n) \tag{8.30}$$

Then the average power (i.e., $\frac{1}{T}\int_0^T v(t)i(t)dt$) can be calculated as:

$$P = \sum_{n=0}^{\infty} P_n = V_0 I_0 + \sum_{n=1}^{\infty} V_{n,rms} I_{n,rms} \cos(\theta_n - \varphi_n) \tag{8.31}$$

or

$$P = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_{n,\max} I_{n,\max}}{2} \cos(\theta_n - \varphi_n) \tag{8.32}$$

For instance, the average power for $v(t)=10+20\cos(2\pi\times60t)+30\cos(4\pi\times60t+30°)$ and $i(t)=2+2.65\cos(2\pi\times60t-48.5°)+2.43\cos(4\pi\times60t-36.2°)$ is 52.2 W.

## 8.8 Total harmonic distortion (THD)

THD quantifies the nonsinusoidal property of a waveform. THD is often applied in situations where the dc term is zero. Assume that the Fourier series of the signal is given ($f(t)$ can be either voltage or current waveform):

$$f(t)=\sum_{n=1}^{\infty}\left[a_n\cos(n\omega_0 t)+b_n\sin(n\omega_0 t)\right] \tag{8.33}$$

Then the THD of signal is defined as:

$$\text{THD}=\sqrt{\frac{{F_{rms}}^2-{F_{1,rms}}^2}{{F_{1,rms}}^2}}, \tag{8.34}$$

where $F_{rms}$ and $F_{1,\ rms}$ show the RMS value of signal $f(t)$ and RMS value of fundamental harmonic of $f(t)$ (note that $F_{rms}=\sqrt{\sum_{n=1}^{\infty}\frac{\left(a_n{}^2+b_n{}^2\right)}{2}}$ and $F_{1,rms}=\sqrt{\frac{\left(a_1{}^2+b_1{}^2\right)}{2}}$). For instance for a current waveform of $i(t)=4\sin(\omega_0 t)+1.5\sin(3\omega_0 t)+0.64\sin(5\omega_0 t)$, the THD is $\sqrt{\frac{3.0545^2-2.829^2}{2.829^2}}=0.408$. It is quite common to express the THD in percentage, so the THD for aforementioned current waveform is 40.8%.

**Example 8.6** Determine the THD of $v(t)=311\sin(2\pi\times60t)+100\sin(2\pi\times2\times60t)+20\sin(2\pi\times3\times60t)$.

**Solution**

RMS of given waveforms is $V_{rms}=\sqrt{\left(\frac{311}{\sqrt{2}}\right)^2+\left(\frac{100}{\sqrt{2}}\right)^2+\left(\frac{20}{\sqrt{2}}\right)^2}=231.43$ V. Peak value of fundamental harmonic is 311 V. So, the RMS value of fundamental harmonic is $V_{1,rms}=\frac{311}{\sqrt{2}}=219.91$ V. Finally the THD is:

$$\text{THD}=\sqrt{\frac{{V_{rms}}^2-{V_{1,rms}}^2}{{V_{1,rms}}^2}}=\sqrt{\frac{231.43^2-219.91^2}{219.91^2}}=0.33 \text{ or } 33\%$$

**Example 8.7** Determine the THD for the given voltage waveform

$$v(t)=\begin{cases}-100 & -1ms<t<0\\ +100 & 0<t<1ms\end{cases}$$

**Solution**

The graph of one period of given waveform is shown in Fig. 8.21.

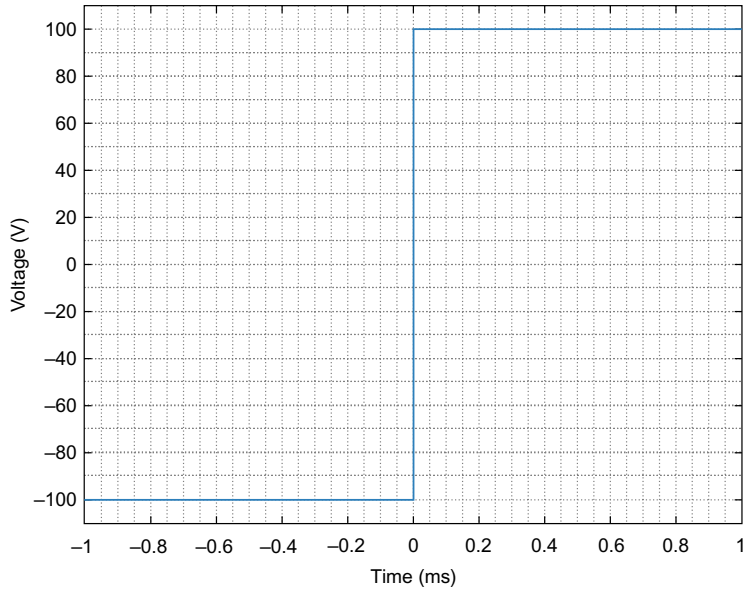



**FIG. 8.21** Graph of given $v(t)$.

Fourier series of $v(t)$ is:

$$v(t) = \sum_{n=1,3,5}^{\infty} \frac{2 \times 200}{n\pi} \sin(n\omega_0 t) \tag{8.35}$$

RMS value of $v(t)$ is:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v(t)^2 dt} = \sqrt{\frac{1}{2m}\int_{-1m}^{0} (-100)^2 dt + \frac{1}{2m}\int_0^{1m} (100)^2 dt} = 100\,V \tag{8.36}$$

Fundamental harmonic (first harmonic) of $v(t)$ has the peak value of $V_1 = \frac{2\times 200}{\pi} = 127.324\,V$. So the RMS value of fundamental harmonic is $V_{1,rms} = \frac{V_1}{\sqrt{2}} = \frac{127.324}{\sqrt{2}} = 90.0325\,V$. Finally the THD is:

$$\text{THD} = \sqrt{\frac{{V_{rms}}^2 - {V_{1,rms}}^2}{{V_{1,rms}}^2}} = \sqrt{\frac{100^2 - 90.0325^2}{90.0325^2}} = 0.4834 \text{ or } 48.34\% \tag{8.37}$$

## 8.9 Volt-second balance

Volt-Second balance is one of the important tools in analyzing the power electronics converters (specially in analyzing the DC-DC converters).

The voltages and currents of a power electronics converter are periodic, i.e., $i(t+T)=i(t)$ and $v(t+T)=v(t)$. The relation between the voltage and current of an inductor is:

$$v_L(t)=L\frac{di_L(t)}{dt} \tag{8.38}$$

So,

$$i(t_0+T)=\frac{1}{L}\int_{t_0}^{t_0+T} v_L(t)dt+i(t_0)\Longrightarrow i(t_0+T)-i(t_0)=\frac{1}{L}\int_{t_0}^{t_0+T} v_L(t)dt \tag{8.39}$$

Since the current is assumed to be periodic, the starting and end values are the same, i.e., $i(t_0+T)-i(t_0)=0$. So,

$$i(t_0+T)-i(t_0)=\frac{1}{L}\int_{t_0}^{t_0+T} v_L(t)dt=0 \tag{8.40}$$

Both sides are multiplied with $\frac{L}{T}$. So,

$$\text{avg}[v_L(t)]=V_L=\frac{1}{T}\int_{t_0}^{t_0+T} v_L(t)dt=0 \tag{8.41}$$

Therefore, for periodic currents, the average voltage across an inductor is zero. This is called Volt-Second Balance.

## 8.10 Ampere-second balance

Dual of previous law can be extracted for capacitors. The relation between the voltage and current of a capacitor is:

$$i_C(t)=C\frac{dv_C(t)}{dt} \tag{8.42}$$

So,

$$v(t_0+T)=\frac{1}{C}\int_{t_0}^{t_0+T} i_C(t)dt+v(t_0)\Longrightarrow v(t_0+T)-v(t_0)=\frac{1}{C}\int_{t_0}^{t_0+T} i_C(t)dt \tag{8.43}$$

Since the voltage is assumed to be periodic, the starting and end values are the same, i.e., $v(t_0+T)-v(t_0)=0$. So,

$$v(t_0+T)-v(t_0)=\frac{1}{C}\int_{t_0}^{t_0+T} i_C(t)dt=0 \tag{8.44}$$

Both sides are multiplied with $\frac{C}{T}$. So,

$$\text{avg}[i_C(t)]=I_C=\frac{1}{T}\int_{t_0}^{t_0+T} i_C(t)dt=0 \tag{8.45}$$

Therefore, for periodic voltages, the average current in a capacitor is zero. This is called Ampere-Second Balance.

## 8.11 MOSFET with resistive load

Consider a MOSFET with a resistive load.

The MOSFET is voltage-controlled switch, i.e., its on/off status is determined with gate voltage. When the gate-source voltage is greater than the threshold voltage, the MOSFET acts as a closed switch; otherwise, the device acts as an open switch.

Assume that the MOSFET M in Fig. 8.22 is supplied with a periodic gate-source voltage with duty ratio $D$. The amplitude of periodic gate-source voltage is large enough to close the MOSFET. Fig. 8.23 shows the circuit waveforms.

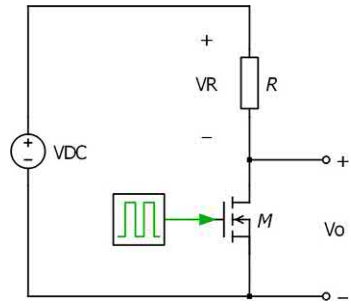



**FIG. 8.22** A MOSFET with purely resistive load.

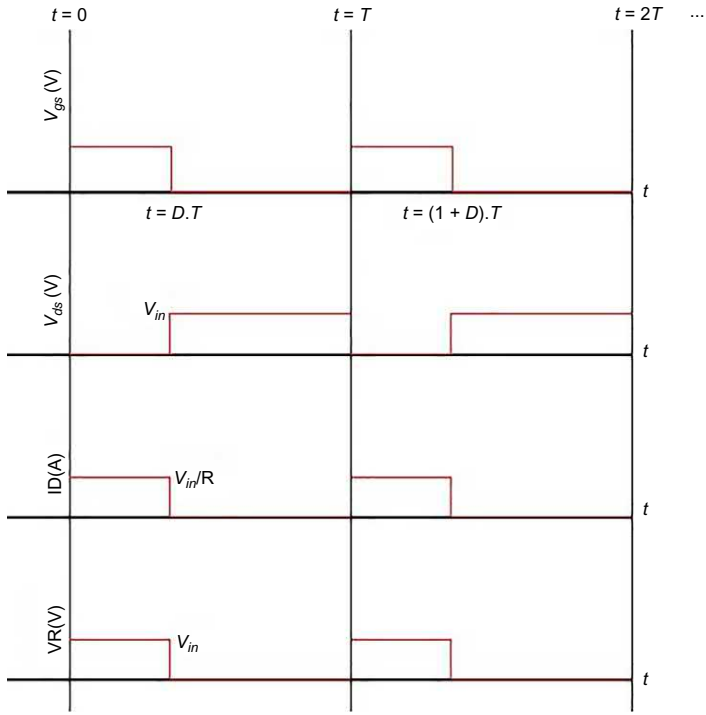



**FIG. 8.23** $V_{gs}$, $V_{ds}$, ID, and VR show the gate-source voltage, drain-source voltage, drain current, and load resistor voltage, respectively. The MOSFET is assumed to be ideal, i.e., drain source resistance is ignored.

The RMS and average of waveforms can be calculated easily using the formulas provided before. For instance, the average and RMS value of load voltage is $D$. Vin and $\sqrt{D}$.Vin, respectively. So, the average power dissipated in the resistor is $\frac{(Vrms)^2}{R}=\frac{\left(\sqrt{D}.\mathrm{Vin}\right)^2}{R}=\frac{D.\mathrm{Vin}^2}{R}$.

The scheme used in Fig. 8.22 is called low-side switching. Note that the source of MOSFET is connected to the ground. The scheme used in Fig. 8.24 is called high-side switching. Note that the source of MOSFET is NOT connected to the ground.

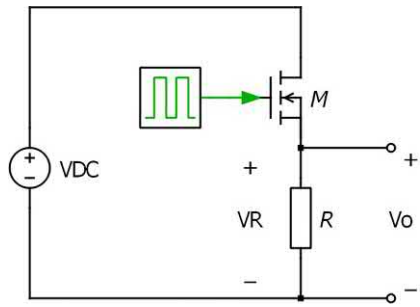



**FIG. 8.24** High-side switching.

The two schemes are the same from load point of view. However, triggering a low-side MOSFET is quite easier than a high-side one. Studying a numeric example is quite helpful for this purpose. Assume that R = 10 Ω, VDC = 20 $V$,$r_{ds,on}=20\,m\Omega$, and $V_{TH}=8\,V$. $r_{ds,on}$ and $V_{TH}$ show the drain-source resistance for a closed MOSFET and threshold voltage of MOSFET, respectively. The gate-source voltage must exceed the threshold voltage in order to turn on the MOSFET. In Fig. 8.22, the source of MOSFET is connected to ground. So, $V_S=0$. The MOSFET in Fig. 8.22 is closed if

$$V_{GS}>V_{TH}\Rightarrow V_G-V_S>V_{TH}\Rightarrow V_G-0>V_{TH}\Rightarrow V_G>V_{TH} \tag{8.46}$$

So, the MOSFET in Fig. 8.22 will be closed if a voltage greater than 8 V is applied to its gate.

When the high-side MOSFET of Fig. 8.24 is closed, the source voltage is:

$$\mathrm{V_S}=\frac{\mathrm{R}}{\mathrm{R}+r_{ds,on}}\times\mathrm{VDC}=\frac{10}{10+0.02}\times 20=19.96\,V \tag{8.47}$$

So, in order to keep the device close, the gate voltage must satisfy the following in equality:

$$V_{GS}>V_{TH}\Rightarrow V_G-V_S>V_{TH}\Rightarrow V_G-19.96>V_{TH}\Rightarrow V_G>19.96+8\Rightarrow V_G>27.96\,V \tag{8.48}$$

So, in order to close the high-side MOSFET of Fig. 8.24, a voltage larger than supply voltage is required. High-side MOSFETs can be triggered with the aid of a technique called bootstrapping. In this technique, the electric charge

is saved in a capacitor and the capacitor is used to trigger the MOSFET in the required time instant. So, there is no need for a voltage bigger than the supply voltage in order to turn on the MOSFET. The IR2101 IC uses the bootstrapping technique to trigger a high-side switch.

## 8.12 Uncontrolled half-wave rectifier

A rectifier is a circuit, which converts the AC input into a DC output. Fig. 8.25 shows the simplest rectifier circuit. It consists of an AC source, a diode, and a load.

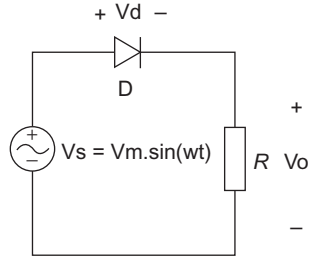



**FIG. 8.25** Simple half-wave rectifier. The output voltage is not controllable.

The waveforms of the circuit are shown in Fig. 8.26. The voltage drop of diode can be ignored if the peak value of input AC source is much bigger than the forward voltage drop of diode.

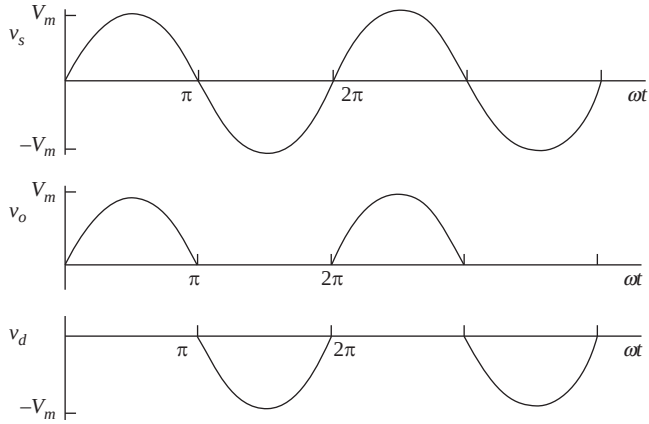



**FIG. 8.26** Typical waveforms of circuit shown in Fig. 8.25. Addition of a capacitor in parallel with the output load decreases the harmonics in load voltage and leads to a more smooth output voltage.

Average value of load voltage is:

$$V_O = V_{avg} = \frac{1}{2\pi}\int_0^{\pi} V_m \sin(\omega t) d(\omega t) = \frac{V_m}{\pi} \tag{8.49}$$

The average value of load current is:

$$I_O = \frac{V_O}{R} = \frac{V_m}{\pi R} \tag{8.50}$$

The average power dissipated in resistor is $P = I^2{}_{rms}R = \frac{V_{rms}{}^2}{R}$. The RMS value of load voltage and current is:

$$\begin{aligned} V_{rms} &= \sqrt{\frac{1}{2\pi}\int_0^{\pi}[V_m \sin(\omega t)]^2 d(\omega t)} = \frac{V_m}{2} \\ I_{rms} &= \frac{V_{rms}}{R} = \frac{V_m}{2R} \end{aligned} \tag{8.51}$$

For instance for $v_s(t) = 120\sqrt{2}\sin(2\pi \times 60 \times t)\,V$ and $R = 5\ \Omega$, $I_{load,avg} = 10.8$ A, $I_{load,rms} = 17$ A, $V_{avg} = 54$ V, $V_{rms} = 84.9$ V and $P = 1440$ W.

## 8.13 Controlled half-wave rectifier

The output voltage of half-wave diode rectifier is not controllable (Fig. 8.27). The output voltage can be controlled if the diode is replaced with a thyristor. The thyristor requires gate signal in order to turn on. Only the turn-on instant is under control. The turn-off instant is not under control; it is governed by the circuit.

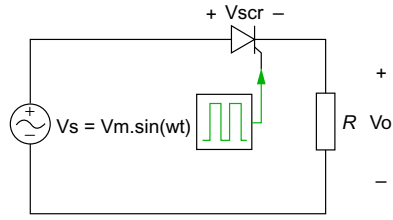



**FIG. 8.27** A simple half-wave rectifier with controllable output voltage.

Fig. 8.28 shows the typical waveforms of circuit shown in Fig. 8.27.

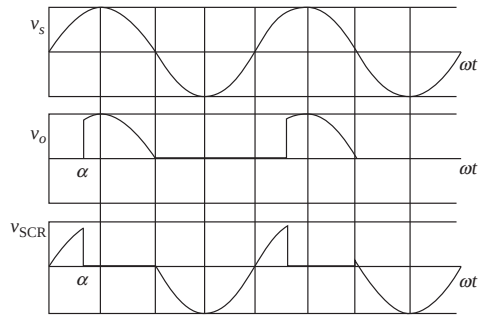



**FIG. 8.28** Typical waveforms of circuit shown in Fig. 8.27.

The thyristor is fired at $\omega t = \alpha$. The thyristor is closed for $\alpha < \omega t < \pi$. The thyristor is off during the $0 < \omega t < \alpha$ (since the gate signal is not applied yet) and $\pi < \omega t < 2\pi$ (since the thyristor is a unidirectional switch, i.e., the current only flows from anode toward the cathode)

The average and RMS value of load voltage can be calculated using the following formulas:

$$V_O = V_{avg} = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_m \sin(\omega t) d(\omega t) = \frac{V_m}{2\pi}(1 + \cos\alpha)$$

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} v_o(\omega t)^2 d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\pi} [V_m \sin(\omega t)]^2 d(\omega t)}$$
$$= \frac{V_m}{2}\sqrt{1 - \frac{\alpha}{\pi} + \frac{\sin(2\alpha)}{2\pi}} \tag{8.52}$$

If we substitute $\alpha = 0$ in the equations, we obtain the formulas for uncontrolled case (Fig. 8.25). The average value and RMS value of output voltage decrease with increasing firing angle ($\alpha$). The average power dissipated in the resistor can be calculated using the $P_R = \frac{V_{rms}^2}{R}$.

For instance for $v_s(t) = 120\sqrt{2}\sin(2\pi \times 60 \times t)\,V$, $R = 100\ \Omega$ and $\alpha = 61.2°$, $I_{load,\,avg} = 0.4\,A$, $I_{load,\,rms} = 0.76$ A, $V_{avg} = 40$ V, $V_{rms} = 75.6$ V,and $P = 57.1$ W.

## 8.14 DC-DC converters

A DC-DC converter, as the name suggests, converts a DC voltage to another DC voltage. The output voltage can be greater than or less than input voltage. The DC-DC converters can be divided into two broad categories:

1. Isolated converters,
2. Nonisolated converters.

The isolated converters contain high-frequency transformers (i.e., a transformer with Ferrite core). So, there is an isolation between the source supply the converter and the load. Flyback, forward or half/full bridge converters are examples of isolated converters.

The nonisolated converters do not contain high-frequency transformers. So, there is no isolation between the input DC source and load. Buck, boost, buck-boost, Cuk, and zeta are examples of nonisolated converters.

The DC-DC converters can operate in two modes: CCM (Continuous Current Mode) and DCM (Discontinuous Current Mode). The operating mode of converter is determined based on the steady-state waveform of inductor current. If the minimum of steady-state inductor current is larger than zero, then the converter operates in CCM (Fig. 8.29).

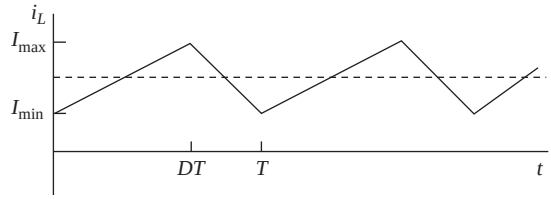



**FIG. 8.29** Typical inductor waveform for a converter operating in CCM. Steady-state minimum value of inductor current is positive.

If steady-state inductor current is zero for some time during the switching period, then the converter operates in DCM (Fig. 8.30).

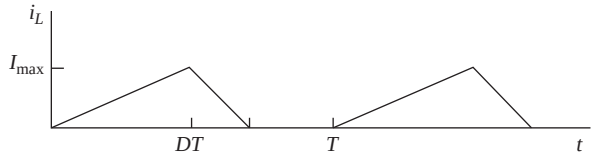



**FIG. 8.30** Typical inductor waveform for a converter operating in CCM.

### 8.14.1 Buck converter

Buck converter decreases the input voltage, i.e., $V_O < V_{IN}$. Fig. 8.31 shows the schematic of a buck converter.

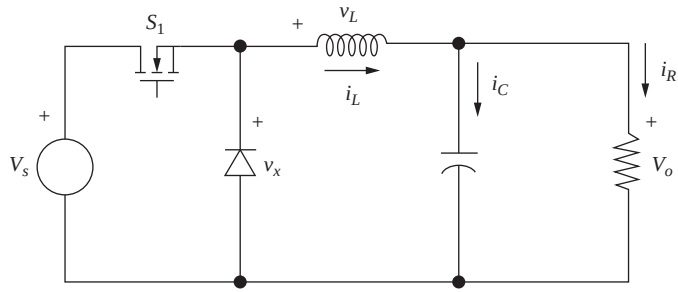



**FIG. 8.31** Schematic of buck converter.

The buck converter is analyzed under the following assumptions:

1. The circuit reaches its steady state, i.e., the transient has been finished.
2. The converter operates in CCM, i.e., minimum of inductor current in steady state is positive.
3. The capacitor is large enough so the output voltage is held constant at $V_O$, i.e., the output ripple is negligible.

4. The switching period is $T$ and the MOSFET is closed for $D$. $T$ interval. $0 < D < 1$ is duty ratio of control signal applied to gate of MOSFET.
5. The components are ideal, i.e., drain-source resistance, forward voltage drop of diode, ESR of capacitor/inductor are zero.

When the MOSFET switch is closed, the diode is revere biased and acts as an open circuit. The equivalent circuit shown in Fig. 8.32 represents this case.

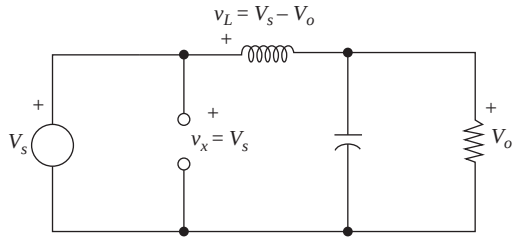



**FIG. 8.32** Equivalent circuit of buck converter for closed MOSFET. MOSFET remains closed for duration of $D \times T$ seconds.

When the MOSFET switch is opened, the diode is forward biased and acts as a short circuit. The equivalent circuit shown in Fig. 8.33 represents this case.

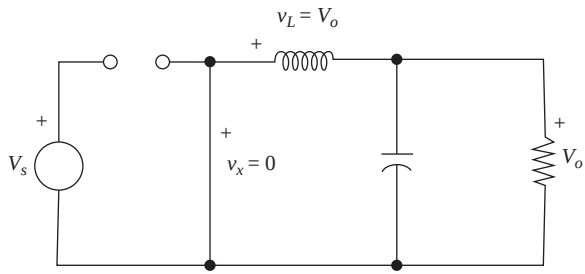



**FIG. 8.33** Equivalent circuit of buck converter for opened MOSFET. MOSFET remains open for duration of $(1 - D) \times T$ seconds.

### *8.14.1.1 Calculation of output voltage*

According to Fig. 8.32, the inductor voltage (for an interval of length $D$. $T$) is:

$$v_L = V_s - V_o \tag{8.53}$$

According to Fig. 8.33, the inductor voltage (for an interval of length $(1 - D)$. $T$) is:

$$v_L = -V_o \tag{8.54}$$

Fig. 8.34 shows the voltage of inductor.

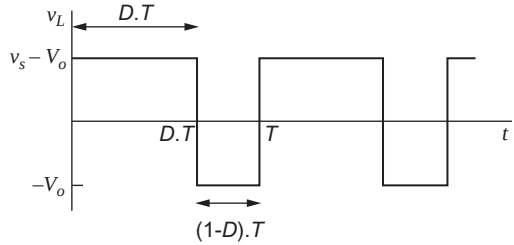



**FIG. 8.34** Waveform of inductor voltage.

The Volt-Second balance can be used to calculate the unknown value of output voltage:

$$(V_s - V_o) \times D \times T - V_o \times (1 - D) \times T = 0 \Rightarrow V_o = D \times V_s \tag{8.55}$$

The output voltage is less than the input voltage (remember that $0 < D < 1$).

The same result can be obtained within a different approach: During the interval, which MOSFET is closed (Fig. 8.32), the inductor voltage can be written as:

$$\begin{aligned} v_L &= V_s - V_o = L\frac{d}{dt}i_L(t) \\ \frac{d}{dt}i_L(t) &= \frac{V_s - V_o}{L} \end{aligned} \tag{8.56}$$

Since the $V_o$ is less than $V_s$, $\frac{V_s - V_o}{L}$ is a positive value and the inductor current increases during the interval MOSFET is closed. The increase in the inductor current during this interval is:

$$\begin{aligned} \frac{d}{dt}i_L(t) &= \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{D \times T} = \frac{V_s - V_O}{L} \\ \Delta i_{L,\text{ Closed MOSFET}} &= \frac{V_s - V_O}{L} \times D \times T \end{aligned} \tag{8.57}$$

During the interval which MOSFET is opened (Fig. 8.33), the inductor voltage can be written as:

$$\begin{aligned} v_L &= -V_o = L\frac{d}{dt}i_L(t) \\ \frac{d}{dt}i_L(t) &= \frac{-V_o}{L} \end{aligned} \tag{8.58}$$

Since $\frac{-V_o}{L}$ is a negative value, the inductor current decreases during this interval. The amount of decrease in the inductor current during this interval is:

$$\begin{aligned} \frac{d}{dt}i_L(t) &= \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1 - D) \times T} = \frac{-V_O}{L} \\ \Delta i_{L,\text{Opened MOSFET}} &= \frac{-V_O}{L} \times (1 - D) \times T \end{aligned} \tag{8.59}$$

Since the inductor current is periodic, i.e., $i_L(t+T)=i_L(t)$, the following equation can be written:

$$\begin{aligned}&\Delta i_{L,\text{Closed MOSFET}}+\Delta i_{L,\text{Opened MOSFET}}=0\\&\frac{V_s-V_O}{L}\times D\times T+\frac{-V_O}{L}\times(1-D)\times T=0\end{aligned}\tag{8.60}$$

which leads to

$$V_O=D\times V_s\tag{8.61}$$

### 8.14.1.2 Calculation of average current drawn from input source

The average input power of converter is $P_{in}=V_s\times I_s$, where $I_s$ is the average current drawn from the input DC source. Since we assumed that converter components are ideal, the efficiency is 100%, i.e., all the input power is dissipated in the output load. So,

$$\begin{aligned}&P_{in}=P_{out}\\&V_s\times I_s=V_o\times I_o\\&I_s=\frac{V_o\times I_o}{V_s}=\frac{{V_o}^2}{R\times V_s}=\frac{(D\times V_s)^2}{R\times V_s}=\frac{D^2\times V_s}{R}\end{aligned}\tag{8.62}$$

### 8.14.1.3 Determining the operating mode of converter

In this section, we want to determine under which condition the converter operates in CCM. Maximum and minimum of inductor current can be written as $I_{max}=I_L+\frac{\Delta i_L}{2}$ and $I_{min}=I_L-\frac{\Delta i_L}{2}$. $I_L$ is the average value of inductor current (Fig. 8.35).

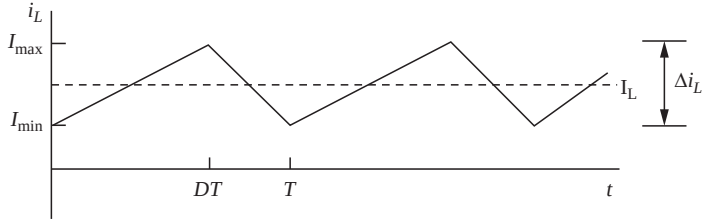



**FIG. 8.35** Maximum and minimum of inductor current is $I_{max}=I_L+\frac{\Delta i_L}{2}$ and $I_{min}=I_L-\frac{\Delta i_L}{2}$. The $I_L$ and $\Delta i_L$ show the average value of inductor current and ripple of inductor current, respectivley.

Value of $\Delta i_L$ is calculated in the previous analysis. Its value can be calcultated using one of the following formulas:

$$\begin{aligned}&\Delta i_L=\Delta i_{L,\text{Opened MOSFET}}=\frac{-V_O}{L}\times(1-D)\times T\\&\Delta i_L=\Delta i_{L,\text{Closed MOSFET}}=\frac{V_s-V_O}{L}\times D\times T\end{aligned}\tag{8.63}$$

We need to determine the value of $I_L$ in order to find the value of $I_{max}$ and $I_{min}$. The value of of $I_L$ can be found with the aid of Fig. 8.31. According to KCL (Kirchhoff's Current Law),

$$i_L = i_C + i_R \tag{8.64}$$

We calculate the average ($\frac{1}{T}\int_{t_0}^{t_0+T} f(\tau)d\tau$) of both sides:

$$\frac{1}{T}\int_{t_0}^{t_0+T} i_L(\tau)d\tau = \frac{1}{T}\int_{t_0}^{t_0+T} i_C(\tau)d\tau + \frac{1}{T}\int_{t_0}^{t_0+T} i_R(\tau)d\tau \tag{8.65}$$

The average value of capacitor voltage is zero (remember the Ampere-Second Balance). So,

$$\frac{1}{T}\int_{t_0}^{t_0+T} i_L(\tau)d\tau = \frac{1}{T}\int_{t_0}^{t_0+T} i_R(\tau)d\tau \tag{8.66}$$

The average value of resistor current can be found easily using Ohm's law

$$\frac{1}{T}\int_{t_0}^{t_0+T} i_R(\tau)d\tau = \frac{V_O}{R} = \frac{D.V_s}{R} \tag{8.67}$$

So, the average value of inductor current is:

$$I_L = \frac{1}{T}\int_{t_0}^{t_0+T} i_L(\tau)d\tau = \frac{V_O}{R} = \frac{D.V_s}{R} \tag{8.68}$$

Once $I_L = \frac{V_O}{R}$ and $\triangle i_L = \left|\triangle i_{L,\text{Opened MOSFET}}\right| = \frac{V_O}{L} \times (1-D) \times T$ are substituted in the $I_{max} = I_L + \frac{\triangle i_L}{2}$ and $I_{min} = I_L - \frac{\triangle i_L}{2}$ equations,

$$\begin{aligned} I_{max} &= I_L + \frac{\Delta i_L}{2} = \frac{V_o}{R} + \frac{1}{2}\left[\frac{V_o}{L}(1-D)T\right] = V_o\left(\frac{1}{R} + \frac{1-D}{2Lf}\right) \\ I_{min} &= I_L - \frac{\Delta i_L}{2} = \frac{V_o}{R} - \frac{1}{2}\left[\frac{V_o}{L}(1-D)T\right] = V_o\left(\frac{1}{R} - \frac{1-D}{2Lf}\right) \end{aligned} \tag{8.69}$$

are obtained. $f$ is the switching frequency and $f = \frac{1}{T}$.

The buck converter operates in CCM if, $I_{min} > 0$. This inequality leads to:

$$L > L_{min} = \frac{(1-D) \times R}{2f} \tag{8.70}$$

So, if the buck converter bobbin is larger than the minimum value, then the converter operates in CCM; otherwise, it operates in DCM.

#### 8.14.1.4 Calculation of output ripple

In the previous analysis, the capacitor was assumed to be very large to keep the output voltage constant. In practice, the output voltage cannot be kept perfectly constant with a finite capacitance. Effect of finite capacitance on output voltage variations (ripple) is studied in this section.

According to Fig. 8.31, the current in capacitor is

$$i_C = i_L - i_R \tag{8.71}$$

The inductor and capacitor currents are shown in Fig. 8.36.

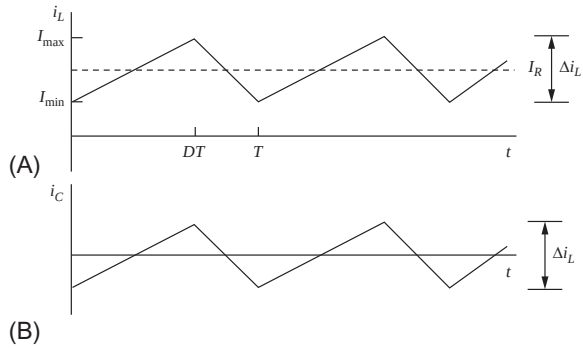



**FIG. 8.36** (A) Inductor current, (B) capacitor current.

The relation between output voltage ripple ($\triangle V_O$) and change in capacitor charge ($\triangle Q$) is

$$\triangle Q = C \times \triangle V_O \Longrightarrow \triangle V_O = \frac{\triangle Q}{C} \tag{8.72}$$

The change in capacitor charge can be calculated easily using Fig. 8.37.

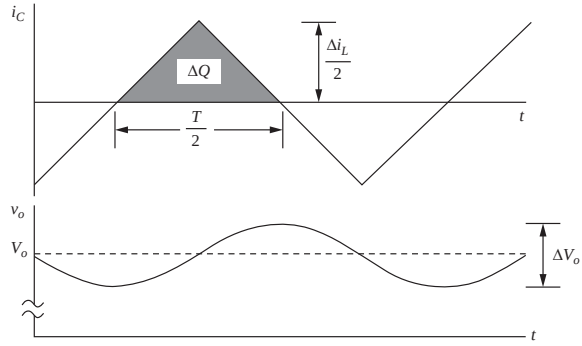



**FIG. 8.37** Waveforms of capacitor current and output voltage of buck converter.

According to Fig. 8.37,

$$\triangle Q = \frac{1}{2} \times \frac{T}{2} \times \frac{\triangle i_L}{2} = \frac{T \times \triangle i_L}{8} \tag{8.73}$$

So,

$$\triangle V_O = \frac{\triangle Q}{C} = \frac{T \times \triangle i_L}{8 \times C} \tag{8.74}$$

Since $\triangle i_L = \frac{V_o}{L} \times (1-D) \times T$,

$$\triangle V_O = \frac{T \times \triangle i_L}{8 \times C} = \frac{T \times V_o}{8 \times C \times L}(1-D)T = \frac{V_o(1-D)}{8LCf^2} \Rightarrow \frac{\triangle V_O}{V_o} = \frac{1-D}{8LCf^2} \quad (8.75)$$

In design, it is useful to rearrange the preceding equation to express required capacitance in terms of specified voltage ripple:

$$C = \frac{1-D}{8L\left(\frac{\triangle V_O}{V_o}\right)f^2} \quad (8.76)$$

For instance, for $V_s = 50$ V, $L = 400$ μH, $R = 20$ Ω, $C = 100$ μF, $f = 10$ kHz, and $D = 0.4$, the converter operates in CCM since $L = 400\,\mu\text{H} > L_{min} = \frac{(1-D)\times R}{2f} = \frac{(1-0.4)\times 20}{2\times 20000} = 300\,\mu\text{H}$, the output voltage is 20 V, $I_{max} = 1.75$ A, $I_{min} = 0.25$ A, and output voltage ripple is 94 mV.

## 8.15 Calculation of output voltage of a buck converter operated in DCM

In this section, we show how the output voltage a buck converter operating in DCM can be calculated. Assume that the buck converter shown in Fig. 8.31 is operated in DCM. The converter waveforms are shown in Fig. 8.38.

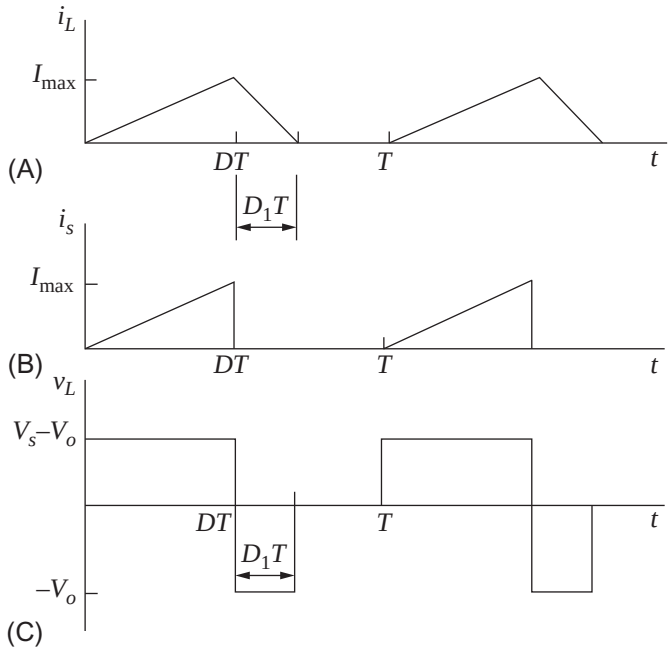



**FIG. 8.38** Different waveforms for a buck converter operating in DCM. $i_L$, $i_s$, and $v_L$ show the inductor current, the current drawn from input DC source, and inductor voltage, respectively.

According to Volt-Second Balance

$$\begin{aligned}(V_s - V_o)DT - V_o D_1 T = 0\\ (V_s - V_o)D = V_o D_1\end{aligned} \tag{8.77}$$

or

$$\frac{V_o}{V_s} = \left(\frac{D}{D + D_1}\right) \tag{8.78}$$

As explained in Section 8.9.3.4, the average value of inductor current ($I_L$) is the same as average value of load current ($I_R$)

$$I_L = I_R = \frac{V_o}{R} \tag{8.79}$$

Average value of resistor current can be found using the $I_R = \frac{V_O}{R}$, where $V_O$ is the average value of output voltage. According to Fig. 8.38A, the average value of inductor current is:

$$I_L = \frac{1}{T}\left(\frac{1}{2} I_{max} DT + \frac{1}{2} I_{max} D_1 T\right) = \frac{1}{2} I_{max}(D + D_1) \tag{8.80}$$

So, $\frac{1}{2} I_{max}(D + D_1) = \frac{V_O}{R}$. When the MOSFET is closed, the inductor current starts increasing from zero. During the interval MOSFET is closed, the inductor voltage is:

$$v_L = V_s - V_o \tag{8.81}$$

So,

$$\frac{di_L}{dt} = \frac{V_s - V_o}{L} = \frac{\triangle i_L}{\triangle t} = \frac{\triangle i_L}{DT} = \frac{I_{max}}{DT} \tag{8.82}$$

Since $V_S = \frac{D + D_1}{D} V_O$,

$$I_{max} = \triangle i_L = \left(\frac{V_s - V_o}{L}\right) DT = \frac{V_o D_1 T}{L} \tag{8.83}$$

If we substitute the $I_{max} = \frac{V_O D_1 T}{L}$ into the $\frac{1}{2} I_{max}(D + D_1) = \frac{V_O}{R}$, we obtain:

$$\begin{aligned}&\frac{1}{2} I_{max}(D + D_1) = \frac{1}{2}\left(\frac{V_o D_1 T}{L}\right)(D + D_1) = \frac{V_o}{R}\\ &{D_1}^2 + D D_1 - \frac{2L}{RT} = 0\\ &D_1 = \frac{-D + \sqrt{D^2 + \frac{8L}{RT}}}{2}\end{aligned} \tag{8.84}$$

So, the output voltage is

$$V_o = V_s\left(\frac{D}{D+D_1}\right) = V_s\left(\frac{2D}{D+\sqrt{D^2+\dfrac{8L}{RT}}}\right) \tag{8.85}$$

For instance, for $V_s = 24\ V$, $L = 200\ \mu H$, $R = 20\ \Omega$, $C = 1000\ \mu F$, $f = 10\ kHz$, and $D = 0.4$, the output voltage is 13.9 V and $D_1 = 0.29$.

## 8.16 Other types of DC-DC converters operating in DCM

Other types of DC-DC converters can be analyzed in the same way like the buck converter. We summarize the important relations for some of the important DC-DC converters in this section.

### 8.16.1 Boost converter

For the boost converter shown in Fig. 8.39,

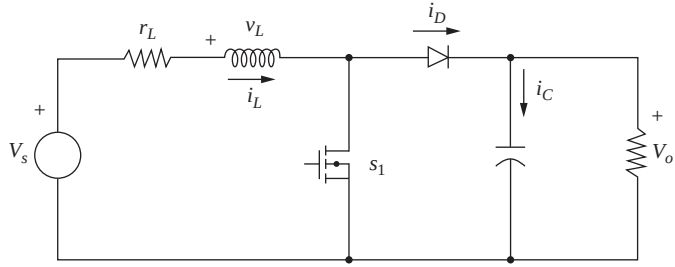



**FIG. 8.39** Schematic of boost converter. $r_L$ shows the inductor ESR.

The output voltage for CCM is

$$V_o = \left(\frac{V_s}{1-D}\right)\left(\frac{1}{1+\dfrac{r_L}{R(1-D)^2}}\right) \tag{8.86}$$

The output voltage for DCM is

$$V_o = \frac{1}{2}\left(1+\sqrt{1+\frac{2D^2RT}{L}}\right)V_s \tag{8.87}$$

$L_{min}$ is ($L_{min}$ is the minimum inductor value for CCM operation, i.e., converter is operated in CCM if $L > L_{min}$)

$$L_{min} = \frac{D(1-D)^2 R}{2f} \tag{8.88}$$

$\frac{\Delta V_o}{V_o}$ is

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} \tag{8.89}$$

### 8.16.2 Buck-boost converter

For the buck-boost converter shown in Fig. 8.40,

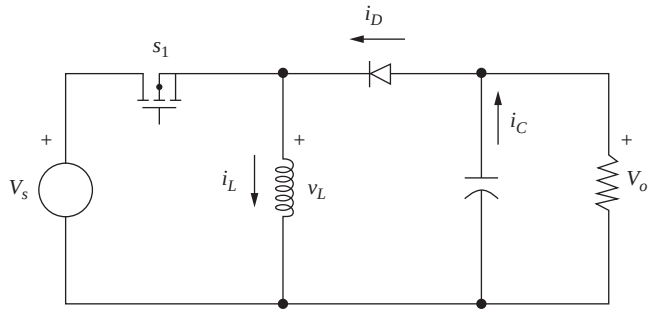



**FIG. 8.40** Schematic of buck-boost converter.

The output voltage for CCM is (note to polarity reversal property of buck-boost converter)

$$V_o = -V_s\left(\frac{D}{1-D}\right) \tag{8.90}$$

$L_{min}$ is

$$L_{min} = \frac{(1-D)^2 R}{2f} \tag{8.91}$$

$\frac{\Delta V_o}{V_o}$ is

$$\frac{\Delta V_o}{V_o} = \frac{D}{RCf} \tag{8.92}$$

### 8.16.3 Cuk converter

For the Cuk converter shown in Fig. 8.41,

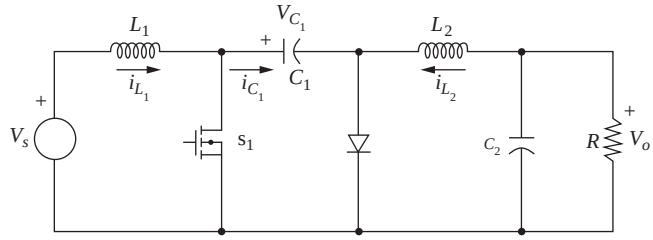



**FIG. 8.41** Schematic of Cuk converter.

The output voltage for CCM is (note to polarity reversal property of Cuk converter)

$$V_o = -V_s\left(\frac{D}{1-D}\right) \tag{8.93}$$

$L_{1,min}$ is

$$L_{1,min} = \frac{(1-D)^2 R}{2Df} \tag{8.94}$$

$L_{2,min}$ is

$$L_{2,min} = \frac{(1-D)R}{2f} \tag{8.95}$$

$\frac{\Delta V_o}{V_o}$ is

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8L_2C_2f^2} \tag{8.96}$$

## 8.16.4 Flyback converter

For the flyback converter shown in Fig. 8.42,

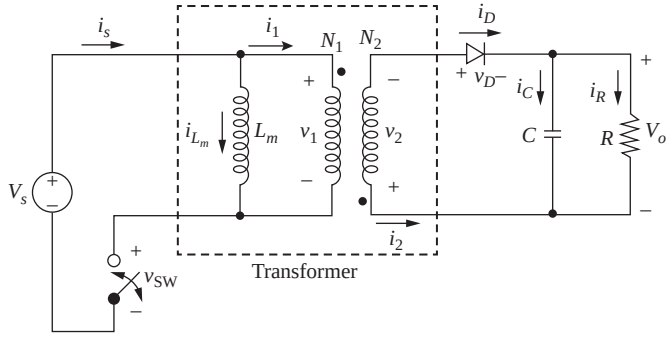



**FIG. 8.42** Schematic of flyback converter.

The output voltage for CCM is

$$V_o = V_s\left(\frac{D}{1-D}\right)\left(\frac{N_2}{N_1}\right) \tag{8.97}$$

The output voltage for DCM is

$$V_o = V_s D\sqrt{\frac{R}{2L_m f}} \tag{8.98}$$

$L_{m,min}$ is ($L_{m,min}$ is the minimum magnetizing inductance required for CCM operation)

$$L_{m,min} = \frac{(1-D)^2 R}{2f}\left(\frac{N_1}{N_2}\right)^2 \tag{8.99}$$

$\frac{\triangle V_o}{V_o}$ is

$$\frac{\triangle V_o}{V_o} = \frac{D}{RCf} \tag{8.100}$$

## 8.17 Dynamics of DC-DC converters

In this section, we will extract the small signal dynamical model of DC-DC converters. This section studies the converters operating in CCM. Generally the converters operate in CCM; however, DCM has its own applications. Refer to [8] in order to extract the dynamical model of converters operate in DCM.

DC-DC converters are variable structure *nonlinear* dynamical systems. So, an LTI model is only an approximation. Although the obtained model is an approximation, it is well enough to start the controller design process.

In this section, we will introduce the State Space Averaging (SSA), which is one of the most important tools to model DC-DC converters. We will show how MATLAB® can do the mathematic machinery of SSA as well.

### 8.17.1 Overview of state space averaging (SSA)

Assume we want to compare two students. Students' marks are shown in Table 8.2.

**TABLE 8.2** Hypothetical students' marks.

| Student | Math (4 credits) | Physics (3 credits) | Biology (2 credits) |
|---|---|---|---|
| A | 75 | 70 | 55 |
| B | 80 | 65 | 60 |

In order to compare them fairly, we must consider all the marks. This is done with the aid of averaging:

$$\begin{aligned} \text{avg}_A &= \frac{75\times 4+70\times 3+55\times 2}{4+3+2} = 68.89 \\ \text{avg}_B &= \frac{80\times 4+65\times 3+60\times 2}{4+3+2} = 70.55 \end{aligned} \tag{8.101}$$

So, second student is more successful since she or he has a higher average. Note that each mark is multiplied by the credits, so importance of the courses is entered into the averaging process.

The logic behind SSA is similar to the logic behind averaging marks. In this case, we average circuits instead of marks. Studying an example is quite helpful. Details and mathematic machinery will be shown in the next sections.

Assume a simple Buck converter like that shown in Fig. 8.43.

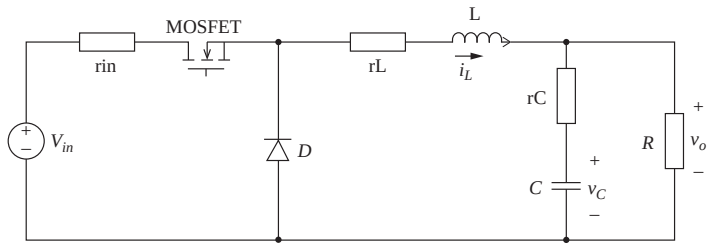



**FIG. 8.43** Schematic of buck converter in presence of components ESRs.

Based on the MOSFET status (on or off ), two equivalent subcircuits can be extracted as shown in Fig. 8.44.

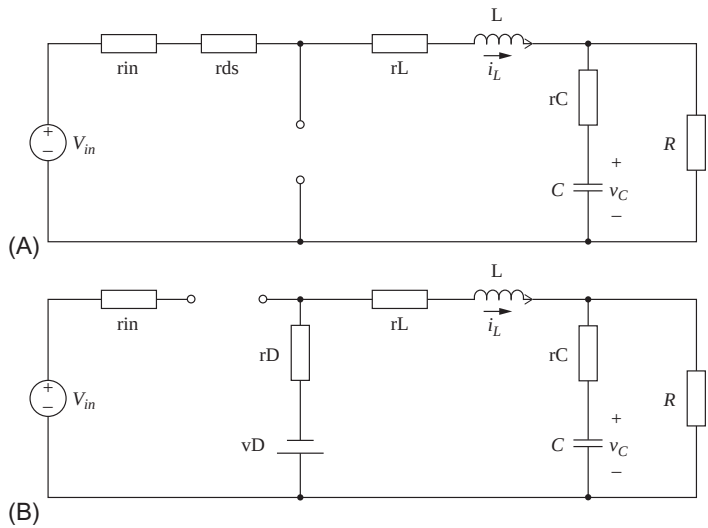



**FIG. 8.44** Equivalent circuit for (A) closed MOSFET, (B) opened MOSFET.

We want to find a model for the Buck converter shown in Fig. 8.3.1, but we have two subcircuits. Each subcircuit has its own dynamic equation. We must find a way to average these two sets of equations.

Assume that the Buck converter shown in Fig. 8.43 spends 80% of the switching period in the MOSFET on state (Fig. 8.44A) and only 20% of switching period in the MOSFET off state (Fig 8.44B). In this case, the Buck converter spends most of its time in the MOSFET on state. So, it is logical to give a higher weight to MOSFET on equation set when averaging is done. It is not logical to average the equations (dynamical equations for MOSFET on and MOSFET off states) using the same weight.

SSA uses the percentage of switching time as the weights (credits in mark*averaging problem). For instance if the Buck converter spend 80% of switching time in the MOSFET on state and 20% of switching time in the MOSFET off state, then the MOSFET on equation set is multiplied by 0.8 and MOSFET off equation set is multiplied by 0.2.

We need an LTI model of the converter. So, the obtained average model must be linearized around the steady-state operating point. Differentiation is used to extract the linear model of converter. So, we can summarize the steps of SSA as below:

- Dynamical equations of all the subcircuits are extracted.
- Equations are averaged using the duty ratio as weight.
- Averaged equations are linearized around the operating point using differentiation.

We use the capital letters for steady-state values and tilde for small-signal perturbations. Small-signal perturbation is much smaller than the steady-state part. For example, the duty ratio of MOSFET gate signal is shown as $d = D + \tilde{d}$. This shows the duty ratio of MOSFET gate signal($d$) is composed of two parts: steady-state part ($D$) and small-signal part ($\tilde{d}$). Small-signal component, as the name suggests, is quite smaller than the steady-state part, i.e., $\tilde{d} \ll D$.

## 8.17.2 Dynamical model of buck converter

Assume a buck converter like that shown in Fig. 8.45. rin, rL, and rC show the input source internal resistance, the inductor series resistance, and the capacitor series resistance, respectively. We assume values of elements are selected such that converter operates in CCM.

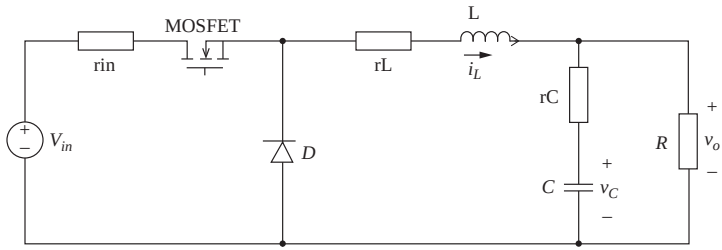



**FIG. 8.45** Buck converter circuit. rin, rL, and rC show the internal resistance of the input DC source, inductor ESR, and capacitor ESR, respectively.

MOSFET is closed and opened with the aid of pulses shown in Fig. 8.46. When gate pulse is high, MOSFET is closed. According to Fig. 8.46, MOSFET is closed for duration of $d \times T$ seconds and is opened for duration of $T - d \times T = (1 - d) \times T$ seconds. $T$ and $d$ show switching period and duty ratio, respectively.

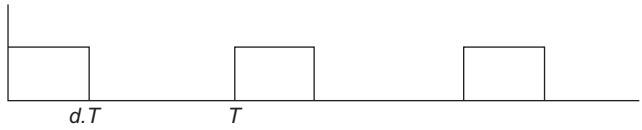



**FIG. 8.46** MOSFET gate pulses.

Figs. 8.47 and 8.48 show the equivalent circuit for closed and opened MOSFET, respectively.

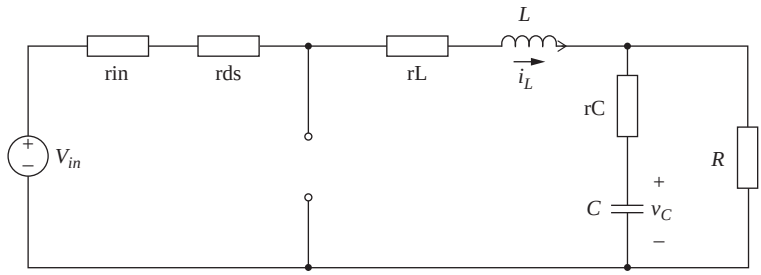



**FIG. 8.47** Equivalent circuit for closed MOSFET. rds shows the resistance between drain and source of a closed MOSFET.

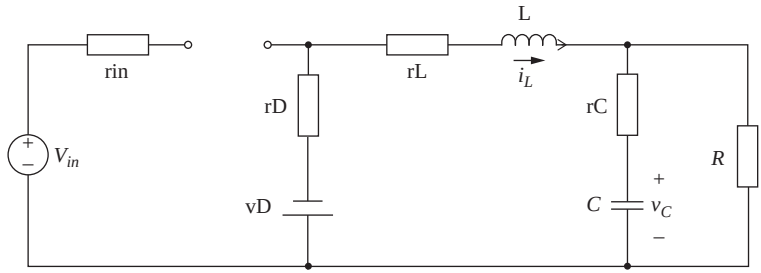



**FIG. 8.48** Equivalent circuit for opened MOSFET. rD and vD show the diode series resistance and diode forward voltage drop, respectively.

These two linear circuits are used to obtain the converters transfer functions. First of all each circuit is analyzed separately.

#### 8.17.2.1 Dynamical equations for closed MOSFET case

When MOSFET is closed, circuit equations can be written as:

$$\begin{cases} (r_{in}+r_{ds}+r_L)i_L+L\dfrac{di_L}{dt}+R\left(i_L-C\dfrac{dv_C}{dt}\right)=v_{in} \\ r_CC\dfrac{dv_C}{dt}+v_C=R\left(i_L-C\dfrac{dv_C}{dt}\right) \end{cases} \tag{8.102}$$

Equations can be simplified using simple algebraic manipulations,

$$\begin{cases} (r_{in}+r_{ds}+r_L+R)i_L+L\dfrac{di_L}{dt}-RC\dfrac{dv_C}{dt}=v_{in} \\ (r_C+R)C\dfrac{dv_C}{dt}+v_C=Ri_L \end{cases} \tag{8.103}$$

$$\begin{cases} (r_{in}+r_{ds}+r_L+R)i_L+L\dfrac{di_L}{dt}-\dfrac{R}{R+r_C}(Ri_L-v_C)=v_{in} \\ C\dfrac{dv_C}{dt}=\dfrac{1}{R+r_C}(Ri_L-v_C) \end{cases} \tag{8.104}$$

$$\begin{cases} L\dfrac{di_L}{dt}=-(r_{in}+r_{ds}+r_L+R)i_L+\dfrac{R^2}{R+r_C}i_L-\dfrac{R}{R+r_C}v_C+v_{in} \\ C\dfrac{dv_C}{dt}=\dfrac{1}{R+r_C}(Ri_L-v_C) \end{cases} \tag{8.105}$$

Equation of output load voltage can be written as,

$$v_o=R\left(i_L-C\frac{dv_C}{dt}\right)=R\left(\frac{r_C}{r_C+R}i_L+\frac{1}{R+r_C}v_C\right) \tag{8.106}$$

#### 8.17.2.2 Dynamical equations for opened MOSFET case

When MOSFET is opened, circuit equation can be written as:

$$\begin{cases} V_D+(r_D+r_L)i_L+L\dfrac{di_L(t)}{dt}+r_CC\dfrac{dv_C}{dt}+v_C=0 \\ r_CC\dfrac{dv_C}{dt}+v_C=R\left(i_L-C\dfrac{dv_C}{dt}\right) \end{cases} \tag{8.107}$$

Equations can be simplified using simple algebraic manipulations,

$$\begin{cases} V_D+(r_D+r_L)i_L+L\dfrac{di_L(t)}{dt}+\dfrac{R.r_C}{R+r_C}i_L+\dfrac{R}{R+r_C}v_C=0 \\ C\dfrac{dv_C}{dt}=\dfrac{R}{R+r_C}i_L-\dfrac{1}{R+r_C}v_C \end{cases} \tag{8.108}$$

$$\begin{cases} L\dfrac{di_L(t)}{dt} = -\left(r_D + r_L + \dfrac{R.r_C}{R+r_C}\right) i_L - \dfrac{R}{R+r_C} v_C - V_D \\ C\dfrac{dv_C}{dt} = \dfrac{R}{R+r_C} i_L - \dfrac{1}{R+r_C} v_C \end{cases} \tag{8.109}$$

Equation of output load voltage can be written as,

$$v_o = R\left(i_L - C\frac{dv_C}{dt}\right) = R\left(\frac{r_C}{r_C+R} i_L + \frac{1}{R+r_C} v_C\right) \tag{8.110}$$

### 8.17.2.3 Averaging

Results of previous analysis are superimposed using averaging. MOSFET is closed for $d.\,T$ seconds and is opened for $(1-d).\,T$ seconds. So, it is fair to multiply the equations obtained for closed MOSFET by $d.\,T$ and the equations obtained for opened MOSFET by $(1-d).\,T$ and average over one periode (duration of one period is $T$ seconds).

We obtain the inductor current equations as:

$$\begin{cases} L\dfrac{di_L}{dt} = -\left(r_{in} + r_{ds} + r_L + R - \dfrac{R^2}{R+r_C}\right) i_L - \dfrac{R}{R+r_C} v_C + v_{in}, & \text{For closed MOSFET} \\ L\dfrac{di_L(t)}{dt} = -\left(r_D + r_L + \dfrac{R.r_C}{R+r_C}\right) i_L - \dfrac{R}{R+r_C} v_C - V_D, & \text{For opened MOSFET} \end{cases} \tag{8.111}$$

Left and right sides of closed MOSFET and opened MOSFET equations are multiplied by $d.\,T$ and $(1-d).\,T$, respectively.

$$\begin{cases} L\dfrac{di_L}{dt} \times d.T = \left(-(r_{in} + r_{ds} + r_L + R) i_L + \dfrac{R^2}{R+r_C} i_L - \dfrac{R}{R+r_C} v_C + v_{in}\right) \times d.T \\ L\dfrac{di_L(t)}{dt} \times (1-d).T = \left(-\left(r_D + r_L + \dfrac{R.r_C}{R+r_C}\right) i_L - \dfrac{R}{R+r_C} v_C - V_D\right) \times (1-d).T \end{cases} \tag{8.112}$$

Corresponding sides are added together:

$$\begin{aligned} & d.T \times L\frac{di_L}{dt} + (1-d).T \times L\frac{di_L}{dt} \\ & \quad = d.T \times \left(-(r_{in} + r_{ds} + r_L + R) i_L + \frac{R^2}{R+r_C} i_L - \frac{R}{R+r_C} v_C + v_{in}\right) + (1-d).T \\ & \qquad \times \left(-\left(r_D + r_L + \frac{R.r_C}{R+r_C}\right) i_L - \frac{R}{R+r_C} v_C - V_D\right) \end{aligned} \tag{8.113}$$

Averaging is realized by multiplying both sides by $\frac{1}{T}$:

$$d\times L\frac{di_L}{dt}+(1-d)\times L\frac{di_L}{dt}$$
$$=d\times\left(-(r_{in}+r_{ds}+r_L+R)i_L+\frac{R^2}{R+r_C}i_L-\frac{R}{R+r_C}v_C+v_{in}\right)$$
$$+(1-d)\times\left(-\left(r_D+r_L+\frac{R.r_C}{R+r_C}\right)i_L-\frac{R}{R+r_C}v_C-V_D\right) \tag{8.114}$$

One can multiply both sides of closed MOSFET and opened MOSFET equations by $d$ and $1-d$, respectively, and add the corresponding sides together. The result is the same as the one obtained above. In the next analysis, we will multiply the equations by $d$ and $1-d$.

After some simple algebraic manipulations,

$$L\frac{di_L}{dt}=-d\times\left(r_{in}+r_{ds}+r_L+R-\frac{R^2}{R+r_C}\right)i_L$$
$$-(1-d)\times\left(r_D+r_L+\frac{R.r_C}{R+r_C}\right)i_L-\frac{R}{R+r_C}v_C-(1-d)V_D+dv_{in}$$
$$L\frac{di_L}{dt}=-d\times R_1i_L-(1-d)\times R_2i_L-\frac{R}{R+r_C}v_C-(1-d)V_D+dv_{in} \tag{8.115}$$

where

$$R_1=r_{in}+r_{ds}+r_L+R-\frac{R^2}{R+r_C} \tag{8.116}$$

and

$$R_2=r_D+r_L+\frac{R.r_C}{R+r_C} \tag{8.117}$$

The same procedure can be applied to the capacitor voltage equations. We obtain the capacitor voltage equations as:

$$\begin{cases} C\dfrac{dv_C}{dt}=\dfrac{R}{R+r_C}i_L-\dfrac{1}{R+r_C}v_C & \text{For closed MOSFET} \\ C\dfrac{dv_C}{dt}=\dfrac{R}{R+r_C}i_L-\dfrac{1}{R+r_C}v_C & \text{For opened MOSFET} \end{cases} \tag{8.118}$$

Left and right sides of closed MOSFET and opened MOSFET equations are multiplied by $d$ and $(1-d)$, respectively, and the corresponding sides are added to each other.

$$d\times C\frac{dv_C}{dt}+(1-d)\times C\frac{dv_C}{dt}=d\times\left(\frac{R}{R+r_C}i_L-\frac{1}{R+r_C}v_C\right)+(1-d)\left(\frac{R}{R+r_C}i_L-\frac{1}{R+r_C}v_C\right)$$
$$C\frac{dv_C}{dt}=\left(\frac{R}{R+r_C}i_L-\frac{1}{R+r_C}v_C\right) \tag{8.119}$$

So the equation of *average* system can be written as:

$$\begin{cases} L\dfrac{di_L}{dt} = -d \times R_1 i_L - (1-d) \times R_2 i_L - \dfrac{R}{R+r_C} v_C - (1-d)V_D + dv_{in} \\ C\dfrac{dv_C}{dt} = \dfrac{R}{R+r_C} i_L - \dfrac{1}{R+r_C} v_C \end{cases} \tag{8.120}$$

where

$$R_1 = r_{in} + r_{ds} + r_L + R - \frac{R^2}{R+r_C}$$

$$R_2 = r_D + r_L + \frac{R.r_C}{R+r_C}$$

This average system can be used to obtain the steady-state currents and voltages. To obtain the steady-state currents and voltages, one must replace the left-hand side with zero (remember that once the system reaches its steady state, the changes, i.e., derivative of states, are zero). Capital letters show the steady-state values. For instance, $I_L$ shows the steady-state inductor current.

$$\begin{cases} 0 = -D \times R_1 I_L - (1-D) \times R_2 I_L + \dfrac{R}{R+r_C} V_C - (1-D)V_D + DV_{IN} \\ 0 = \dfrac{R}{R+r_C} I_L - \dfrac{1}{R+r_C} V_C \end{cases} \tag{8.121}$$

MATLAB can be used to solve the obtained equation set. The following code solves the obtained equation set. Solution is shown in Fig. 8.49.

```
clc
clear all

syms R1 R2 R D IL VC rC rL VD vIN

eq1=-D*R1*IL-(1-D)*R2*IL-R/(R+rC)*VC-(1-D)*VD+D*vIN;
eq2=R/(R+rC)*IL-1/(R+rC)*VC;

DC_operatingPoint=solve(eq1,eq2,'[IL VC]');

disp('IL=')
pretty(simplify(DC_operatingPoint.IL))

disp('VC=')
pretty(simplify(DC_operatingPoint.VC))
```

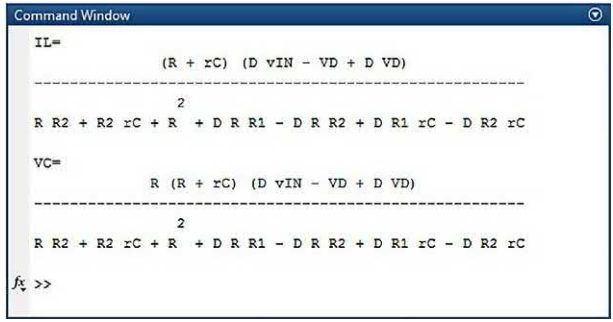



**FIG. 8.49** The steady-state current and voltage.

So the steady-state values of inductor current and capacitor voltage are:

$$\begin{cases} I_L = \dfrac{((R+r_C)(DV_{IN}-(1-D)V_D}{(R+r_C)R_2+R^2+D(R+r_C)(R_1-R_2)} \\ V_C = \dfrac{((R+r_C)(DV_{IN}-(1-D)V_D}{(R+r_C)R_2+(1-2D)R^2+D(R+r_C)(R_1-R_2)} \times R \end{cases} \tag{8.122}$$

If we ignore rin, rds, rD, VD (i.e., rin = rds = rD = VD = 0) steady-state values are obtained as:

$$\begin{cases} I_L = \dfrac{D \times V_{IN}}{R} \\ V_C = D \times V_{IN} \end{cases} \tag{8.123}$$

which is the familiar equations for ideal (i.e., a converter with 100% efficiency) buck converter operating in CCM.

Averaging procedure must be applied to the output equation as well.

$$\begin{aligned} d \times v_o + (1-d) \times v_o \; = d \times R\left(\frac{r_C}{r_C+R} i_L + \frac{1}{R+r_C} v_C\right) + (1-d) \\ \times R\left(\frac{r_C}{r_C+R} i_L + \frac{1}{R+r_C} v_C\right) \end{aligned} \tag{8.124}$$

After some simple algebraic manipulations,

$$v_o = R\left(\frac{r_C}{r_C+R} i_L + \frac{1}{R+r_C} v_C\right) \tag{8.125}$$

is obtained.

### 8.17.2.4 Linearization of averaged equations

Averaged equations are obtained as:

$$\begin{cases} L\dfrac{di_L}{dt} = -d \times R_1 i_L - (1-d) \times R_2 i_L - \dfrac{R}{R+r_C} v_C - (1-d)V_D + dv_{in} \\ C\dfrac{dv_C}{dt} = \dfrac{R}{R+r_C} i_L - \dfrac{1}{R+r_C} v_C \end{cases} \tag{8.126}$$

where

$$R_1 = r_{in} + r_{ds} + r_L + R - \frac{R^2}{R + r_C}$$

$$R_2 = r_D + r_L + \frac{R \times r_C}{R + r_C}$$

Linearization is done using the Taylor series. Assume that,

$$\begin{aligned} i_L &= I_L + \tilde{i}_L \\ v_C &= V_C + \tilde{v}_C \\ d &= D + \tilde{d} \end{aligned} \tag{8.127}$$

where $\tilde{i}_L \ll I_L$, $\tilde{v}_C \ll V_C$ and $\tilde{d} \ll D$. Diode forward voltage drop has been assumed to be constant. These equations show that each variable has a steady steady-state value ($I_L$, $V_C$, and $D$) and a small perturbation ($\tilde{i}_L, \tilde{v}_C$, and $\tilde{d}$). Steady-state values are obtained by solving the averaged equations with left-hand side equal to zero (see Fig. 8.49). Steady-state values are much bigger than the small-signal perturbation part.

We substitute these new variables into the equations,

$$\begin{aligned} L\frac{d\left(I_L + \tilde{i}_L\right)}{dt} = &-\left(D + \tilde{d}\right) \times R_1 \left(I_L + \tilde{i}_L\right) - \left(1 - \left(D + \tilde{d}\right)\right) \times R_2 \left(I_L + \tilde{i}_L\right) \\ &- \frac{R}{R + r_C}\left(V_C + \tilde{v}_C\right) - \left(1 - \left(D + \tilde{d}\right)\right) V_D + \left(D + \tilde{d}\right)\left(V_{IN} + \tilde{v}_{in}\right) \end{aligned} \tag{8.128}$$

$$C\frac{d\left(V_C + \tilde{v}_C\right)}{dt} = \frac{R}{R + r_C}\left(I_L + \tilde{i}_L\right) - \frac{1}{R + r_C}\left(V_C + \tilde{v}_C\right) \tag{8.129}$$

After simple algebraic manipulations,

$$\begin{aligned} L\frac{d\left(I_L + \tilde{i}_L\right)}{dt} = &-\left(D + \tilde{d}\right) \times R_1 \left(I_L + \tilde{i}_L\right) - \left(1 - \left(D + \tilde{d}\right)\right) \times R_2 \left(I_L + \tilde{i}_L\right) \\ &- \frac{R}{R + r_C}\left(V_C + \tilde{v}_C\right) - \left(1 - \left(D + \tilde{d}\right)\right) V_D + \left(D + \tilde{d}\right)\left(V_{IN} + \tilde{v}_{in}\right) \Rightarrow \\ L\frac{d\left(I_L + \tilde{i}_L\right)}{dt} = &-R_1 D I_L - R_1 D \tilde{i}_L - R_1 I_L \tilde{d} - R_1 \tilde{i}_L \tilde{d} + R_2 (D-1) I_L + R_2 (D-1) \tilde{i}_L + R_2 I_L \tilde{d} + R_2 \tilde{i}_L \tilde{d} \\ &- \frac{R}{R + r_C} V_C - \frac{R}{R + r_C} \tilde{v}_c + (D-1) V_D + V_D \tilde{d} + D V_{IN} + D \tilde{v}_{in} + V_{IN} \tilde{d} + \tilde{v}_{in} \tilde{d} \Rightarrow \\ L\frac{d\left(I_L + \tilde{i}_L\right)}{dt} = &-R_1 D I_L + R_2 (D-1) I_L + (D-1) V_D - \frac{R}{R + r_C} V_C + D V_{IN} + \tilde{v}_{in} \tilde{d} + R_2 \tilde{i}_L \tilde{d} \\ &- R_1 \tilde{i}_L \tilde{d} + (R_2 (D-1) - R_1 D) \tilde{i}_L - \frac{R}{R + r_C} \tilde{v}_c + (V_{IN} + V_D + (R_2 - R_1) I_L) \tilde{d} + D \tilde{v}_{in} \end{aligned} \tag{8.130}$$

is obtained. $L\frac{d\left(I_L + \tilde{i}_L\right)}{dt} = L\frac{d\left(\tilde{i}_L\right)}{dt}$ since derivative of a constant term ($I_L$) is zero. Right-hand side can be grouped into three:

- $-R_1 D I_L + R_2(D-1)I_L + (D-1)V_D - \frac{R}{R+r_C}V_C + DV_{IN}$
- $\tilde{v}_{in}\tilde{d} + R_2\tilde{i}_L\tilde{d} - R_1\tilde{i}_L\tilde{d}$
- $(R_2(D-1) - R_1 D)\tilde{i}_L - \frac{R}{R+r_C}\tilde{v}_c + (V_{IN} + V_D + (R_2 - R_1)I_L)\tilde{d} + D\tilde{v}_{in}$

If we substitute the steady-state values obtained before (Fig. 8.49) into the $-R_1 D I_L + R_2(D-1)I_L + (D-1)V_D - \frac{R}{R+r_C}V_C + DV_{IN}$, the result will become 0. Second group can vanish as well because multiplication of two small numbers is a small number, as well. So, only terms of third group are important.

$$L\frac{d\left(\tilde{i}_L\right)}{dt} \approx (R_2(D-1) - R_1 D)\tilde{i}_L - \frac{R}{R+r_C}\tilde{v}_c + (V_{IN} + V_D + (R_2 - R_1)I_L)\tilde{d} + D\tilde{v}_{in} \tag{8.131}$$

The same procedure can be applied to the averaged capacitor voltage equation:

$$\begin{aligned} C\frac{d\left(V_C + \tilde{v}_C\right)}{dt} &= \frac{R}{R+r_C}\left(I_L + \tilde{i}_L\right) - \frac{1}{R+r_C}\left(V_C + \tilde{v}_C\right) \Longrightarrow C\frac{d\left(V_C + \tilde{v}_C\right)}{dt} \\ &= \frac{R}{R+r_C}I_L - \frac{1}{R+r_C}V_C + \frac{R}{R+r_C}\tilde{i}_L - \frac{1}{R+r_C}\tilde{v}_C \end{aligned} \tag{8.132}$$

$V_C$ is constant, so its derivative is zero. So,

$$C\frac{d\left(\tilde{v}_C\right)}{dt} = \frac{R}{R+r_C}I_L - \frac{1}{R+r_C}V_C + \frac{R}{R+r_C}\tilde{i}_L - \frac{1}{R+r_C}\tilde{v}_C \tag{8.133}$$

Right-hand side can be grouped into two groups:

- $\frac{R}{R+r_C}I_L - \frac{1}{R+r_C}V_C$
- $\frac{R}{R+r_C}\tilde{i}_L - \frac{1}{R+r_C}\tilde{v}_C$

If we substitute the steady-state values obtained for $I_L$ and $V_C$ into the $\frac{R}{R+r_C}I_L - \frac{1}{R+r_C}V_C$, the result will be 0. So, only terms of second group are important.

$$C\frac{d\left(\tilde{v}_C\right)}{dt} \approx \frac{R}{R+r_C}\tilde{i}_L - \frac{1}{R+r_C}\tilde{v}_C \tag{8.134}$$

Output equation is linearized in the same way. Output voltage ($v_o$) is decomposed into two components: $v_o = V_o + \tilde{v}_o$. $V_o$ shows the large-signal component and $\tilde{v}_o$ shows the small-signal component

$$\begin{aligned} v_o &= R\left(\frac{r_C}{r_C+R}i_L + \frac{1}{R+r_C}v_C\right) \Rightarrow \\ V_o + \tilde{v}_o &= R\left(\frac{r_C}{r_C+R}\left(I_L + \tilde{i}_L\right) + \frac{1}{R+r_C}\left(V_C + \tilde{v}_C\right)\right) \Rightarrow \\ V_o + \tilde{v}_o &= \frac{R.r_C}{r_C+R}I_L + \frac{R}{R+r_C}V_C + \frac{R.r_C}{r_C+R}\tilde{i}_L + \frac{R}{R+r_C}\tilde{v}_C \end{aligned} \tag{8.135}$$

Steady-state value of load voltage can be obtained as:

$$V_o = \frac{R.r_C}{r_C + R} I_L + \frac{R}{R + r_C} V_C \tag{8.136}$$

The small-signal variation of output voltage is:

$$\tilde{v}_o = \frac{R.r_C}{r_C + R} \tilde{i}_L + \frac{R}{R + r_C} \tilde{v}_C \tag{8.137}$$

So, linearized small-signal model of buck converter can be written as:

$$\begin{cases} \dfrac{d\left(\tilde{i}_L\right)}{dt} \approx \dfrac{1}{L}\left[(R_2(D-1) - R_1 D)\tilde{i}_L - \dfrac{R}{R + r_C}\tilde{v}_c + (V_{IN} + V_D + (R_2 - R_1)I_L)\tilde{d} + D\tilde{v}_{in}\right] \\ \dfrac{d\left(\tilde{v}_C\right)}{dt} \approx \dfrac{1}{C}\left[\dfrac{R}{R + r_C}\tilde{i}_L - \dfrac{1}{R + r_C}\tilde{v}_C\right] \end{cases}$$

$$\tilde{v}_o = \frac{R.r_C}{r_C + R} \tilde{i}_L + \frac{R}{R + r_C} \tilde{v}_C \tag{8.138}$$

where

$$R_1 = r_{in} + r_{ds} + r_L + R - \frac{R^2}{R + r_C}$$

$$R_2 = r_D + r_L + \frac{R \times r_C}{R + r_C}$$

It can be written in the form of a state space equation (we used notation $\mathbb{C}x$ instead of $Cx$, since $C$ is used for capacitor. $\mathbb{C}$ is a matrix.):

$$\begin{cases} \dot{x} = Ax + Bu \\ y = \mathbb{C}x \end{cases} \tag{8.139}$$

where

$$x = \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_c \end{bmatrix}$$

$$u = \begin{bmatrix} \tilde{d} \\ \tilde{v}_{in} \end{bmatrix}$$

$$y = v_o$$

$$A = \begin{bmatrix} \dfrac{R_2(D-1) - R_1 D}{L} & -\dfrac{R}{(R + r_C)L} \\ \dfrac{R}{(R + r_C)C} & -\dfrac{1}{(R + r_C)C} \end{bmatrix} \tag{8.140}$$

$$B = \begin{bmatrix} \dfrac{(V_{IN} + V_D + (R_2 - R_1)I_L)}{L} & \dfrac{D}{L} \\ 0 & 0 \\ \dfrac{}{C} & \dfrac{}{C} \end{bmatrix}$$

$$C = \begin{bmatrix} \dfrac{R.r_C}{r_C + R} & \dfrac{R}{r_C + R} \end{bmatrix}$$

Assume a buck converter with the following parameters:

R= 5 Ω, Vin=50 V, rin=0.1 Ω, L=400 μH, rL=0.1 Ω, C=100 μF, rC=0.05 Ω, D=0.41, rds=0.1 Ω, rD=0.1 Ω, and VD=0.7 V.

Following program calculates the small-signal transfer functions according to the given values. After running the program, $\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{6184s + 1.237\times10^9}{s^2 + 2574s + 2.568\times10^7}$ and $\frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \frac{50.74s + 1.015\times10^7}{s^2 + 2574s + 2.568\times10^7}$ are obtained. Bode plots of these transfer functions are shown in Figs. 8.50 and 8.51.

```
%This program calculate the small signal transfer
%functions for Buck converter
R=5;

VIN=50;
rin=.1;

L=400e-6;
rL=.1;

C=100e-6;
rC=.05;

rD=.01;
VD=.7;

rds=.1;

D=.41;

R1=rin+rds+rL+R*rC/(R+rC);
R2=rD+rL+R*rC/(R+rC);

IL=(R+rC)*(D*VIN-(1-D)*VD)/((R+rC)*R2+R^2+D*(R+rC)*(R1-R2));

A=[(R2*(D-1)-R1*D)/L -R/(R+rC)/L;R/(R+rC)/C -1/(R+rC)/C];
B=[(VIN+VD+(R2-R1)*IL)/L D/L;0 0];
CC=[R*rC/(rC+R) R/(R+rC)]; %C shows the capacitance so CC is used
for matrix
H=tf(ss(A,B,CC,0));
vO_d=H(1)% transfer function between output voltage and duty ratio
vO_vin=H(2) %transfer function between output voltage and input
source
figure(1)
bode(vO_d), grid on
figure(2)
bode(vO_vin), grid on
```

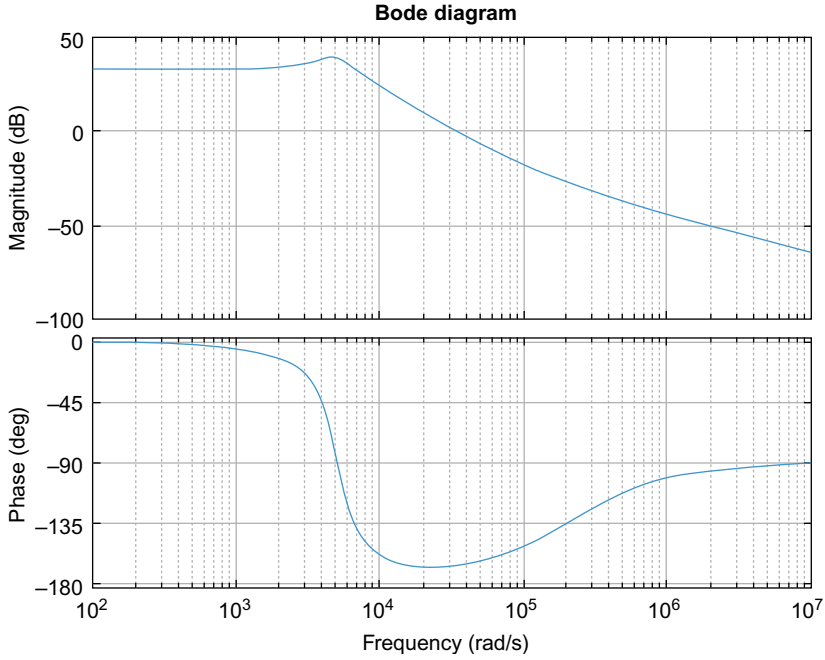



**FIG. 8.50** Bode plot of $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$ for studied buck converter.

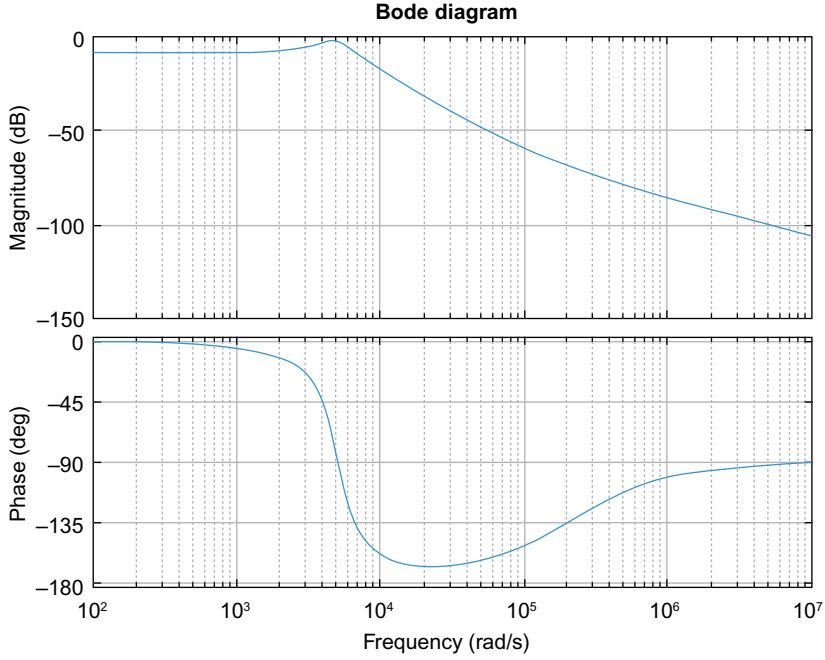



**FIG. 8.51** Bode plot of audio susceptibility ($\frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)}$) for studied buck converter.

#### 8.17.2.5 Obtaining the small-signal transfer functions using MATLAB®

MATLAB® can do the mathematical machinery of SSA easily without any error. Following program shows how MATLAB® can be used to extract the small-signal transfer functions of a buck converter. Outputs are shown in Fig. 8.52. As you see, results are the same with the previous analysis.

```
% This program extract the small signal transfer function
clc
clear all;
% Elements values
R=5;     %Load resistor
VIN=50;  %Input source voltage
rin=.1;  %Input source internal resistance
L=400e-6;%inductor
rL=.1;   %inductor series resistance
C=100e-6;%capacitor
rC=.05;  %capacitor series resistance
rD=.01;  %Diode series resistance
VD=.7;   %Diode forward voltage drop
rds=.1;  %MOSFET on resistance
D=.41;   %Duty ratio

% Symbolic variables
%iL: inductor current
%vC: capacitor voltage
%vin: input voltage source
%vD: diode forward voltage drop
%d: duty cycle
syms iL vC vin vD d

%CLOSED MOSFET EQUATIONS
M1=(-(rin+rds+rL+(R*rC/(R+rC)))*iL-R/(R+rC)*vC+vin)/L;%d(iL)/
dt for closed MOSFET
M2=(R/(R+rC)*iL-1/(R+rC)*vC)/C;            %d(vC)/dt for closed
MOSFET
vO1=R*(rC/(rC+R)*iL+1/(R+rC)*vC);
%OPENED MOSFET EQUATIONS
M3=(-(rD+rL+R*rC/(R+rC))*iL-R/(R+rC)*vC-vD)/L;  %d(iL)/dt for opened
MOSFET
M4=(R/(R+rC)*iL-1/(R+rC)*vC)/C;           %%d(vC)/dt for opened
MOSFET
vO2=R*(rC/(rC+R)*iL+1/(R+rC)*vC);
%AVERAGING
MA1= simplify(d*M1+(1-d)*M3);
```

```
MA2= simplify(d*M2+(1-d)*M4);
vO= simplify(d*vO1+(1-d)*vO2);
% DC OPERATİNG POİNT CALCULATİON
MA_DC_1=subs(MA1,[vin vD d],[VIN VD D]);
MA_DC_2=subs(MA2,[vin vD d],[VIN VD D]);

DC_SOL= solve(MA_DC_1==0,MA_DC_2==0,'iL','vC');

IL=eval(DC_SOL.iL); %IL is the inductor current steady state value
VC=eval(DC_SOL.vC); %VC is the capacitor current steady state value

%LINEARIZATION
% .
% x=Ax+Bu
%vector x=[iL;vC] is assumed. vector x is states.
%u=[vin;d] where vin=input voltage source and d=duty. vector u is
system inputs.
%
A11=subs(simplify(diff(MA1,iL)),[iL vC d vD],[IL VC D VD]);
A12=subs(simplify(diff(MA1,vC)),[iL vC d vD],[IL VC D VD]);

A21=subs(simplify(diff(MA2,iL)),[iL vC d vD],[IL VC D VD]);
A22=subs(simplify(diff(MA2,vC)),[iL vC d vD],[IL VC D VD]);

A=eval([A11 A12;
        A21 A22]); %variable A is matrix A in state space equation

B11=subs(simplify(diff(MA1,vin)),[iL vC d vD vin],[IL VC D VD VIN]);
B12=subs(simplify(diff(MA1,d)),[iL vC d vD vin],[IL VC D VD VIN]);

B21=subs(simplify(diff(MA2,vin)),[iL vC d vD vin],[IL VC D VD VIN]);
B22=subs(simplify(diff(MA2,d)),[iL vC d vD vin],[IL VC D VD VIN]);

B=eval([B11 B12;
        B21 B22]); % variable B is matrix B in state space equation

CC1=subs(simplify(diff(vO,iL)),[iL vC d vD],[IL VC D VD]);
CC2=subs(simplify(diff(vO,vC)),[iL vC d vD],[IL VC D VD]);
CC=eval([CC1 CC2]); %variable CC is matrix C in state space equation
                  % variable D shows duty so DD is used.
DD11=subs(simplify(diff(vO,vin)),[iL vC d vD vin],[IL VC D VD VIN]);
DD12=subs(simplify(diff(vO,d)),[iL vC d vD vin],[IL VC D VD VIN]);

DD=eval([DD11 DD12]); % variable DD is matrix D in state space equation
                    % variable D shows duty so DD is used.

H=tf(ss(A,B,CC,DD));

               %transfer function between input source and load
resistor voltage
```

```
                % ~
vR_vin=H(1,1)   % vR(s)
                % ——
                % ~
                % vin(s)

                %transfer function between duty ratio and load resistor
voltage
                %~
vR_d=H(1,2)     %vR(s)
                %--
                %~
                %d(s)
```

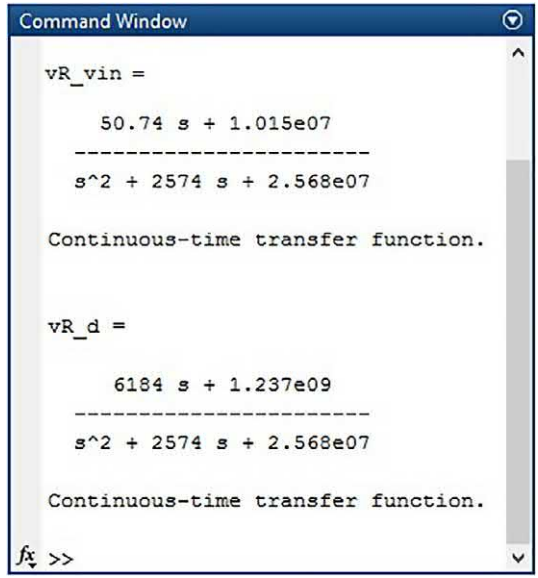



**FIG. 8.52** Calculated transfer functions. `vR_vin` keeps the $\frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)}$ transfer function and `vR_d` keeps the $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$ transfer function. $\tilde{v}_o(s)$ shows the small-signal changes of output load R.

The program is composed of three parts:

- Taking the parameter values,
- Applying averaging and linearization to the converters dynamical equations,
- Extracting transfer functions.

First few lines of code take the parameters values. This is quite useful and is recommended since you can run the code easily for different values of components.

Converters dynamical equations (variables `M1`, `M2`, `vO1`, `M3`, `M4`, and `vO2` in the code) must be extracted manually using KVL and KCL. MATLAB® can do symbolic computation using `syms` command. For more information on the command, type `help syms` in MATLAB's command line.

Variables MA1, MA2, and vO in the code are averaged variables. As stated earlier, the steady-state currents and voltages can be found by equating the derivative terms equal to zero. IL and VC are steady-state values of inductor current and capacitor voltage, respectively. These variables determine the steady-state operating point of converter.

The derivative is used to calculate the matrices of state space representation. State space representation has been converted into transfer function form using `tf` command.

The shown program can be used to extract boost or buck-boost dynamical equations as well. Only dynamical equations (variables `M1`, `M2`, `vO1`, `M3`, `M4`, and `vO2` in the code) must be rewritten according to the selected topology. Other parts of code remain unchanged.

## 8.18 PID controller design for converter

PID controllers are the most important type of controllers. In this section, we show how a PID controller can be designed for obtained control-to-output $(\frac{\tilde{v}_o(s)}{\tilde{d}(s)})$ transfer function. The following small-signal transfer functions are obtained in the previous section:

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \frac{50.74s + 1.015 \times 10^7}{s^2 + 2574s + 2.568 \times 10^7}$$

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{6184s + 1.237 \times 10^9}{s^2 + 2574s + 2.568 \times 10^7}$$

The following block diagram can be drawn for the studied buck converter (Fig. 8.53).

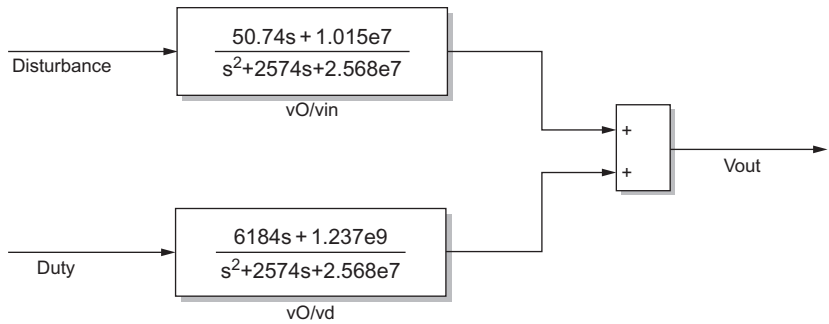



**FIG. 8.53** Dynamical model of buck converter. The changes in duty ratio $(\tilde{d})$ and input voltage $(\tilde{v}_{in})$ affect the output voltage. The output current changes ($\tilde{i}_o$, see next section) will affect the output voltage, as well. However, the output current changes is ignored in the drawn block diagram.

The controller sets the duty cycle of converter, i.e., duty cycle is the control input. The input voltage changes ($\tilde{v}_{in}(s)$) play the role disturbance. Note that in the previous analysis we neglected the output load changes, i.e., we assumed the output load is constant. The change of output load current ($\tilde{i}_o$) is another source of disturbance; however, it is neglected in this section.

Structure of control loop is shown in Fig. 8.54.

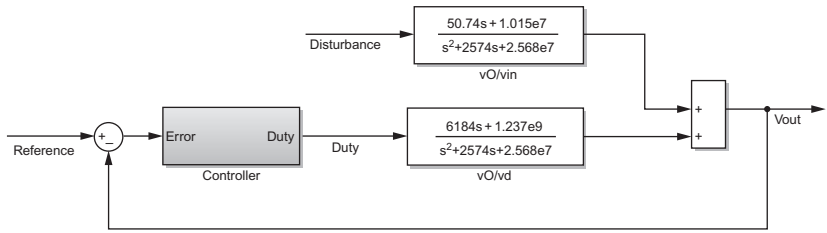



**FIG. 8.54** Closed-loop control of buck converter. Controller block sets the duty ratio. The input voltage changes ($\tilde{v}_{in}(s)$) play the role disturbance.

The schema shown in Fig. 8.54 is called Voltage Mode Control (VMC) since the feedback is taken from output voltage. The feedback can be taken from inductor currents as well. Such a control loop is called Current Mode Control (CMC).

We want to design the controller block shown in the Fig. 8.54. Assume that we want to design a PI controller for this system. Since the control-to-output transfer function has no pole in origin, i.e., $s=0$, the controller must contain an integrator in order to obtain zero steady-state error.

First of all, we must enter the transfer function for plant ($\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$) into the MATLAB® environment. This can be done with the aid of `tf` command (Fig. 8.55).


**FIG. 8.55** Entering the transfer functions into MATLAB with the aid of `tf` command.

We use the `pidTuner` command to tune the PI controller (Fig. 8.56).


**FIG. 8.56** The `pidTuner` command is used to tune the PID controller coefficients.

After pressing the Enter key, the window shown in Fig. 8.57 will appear.

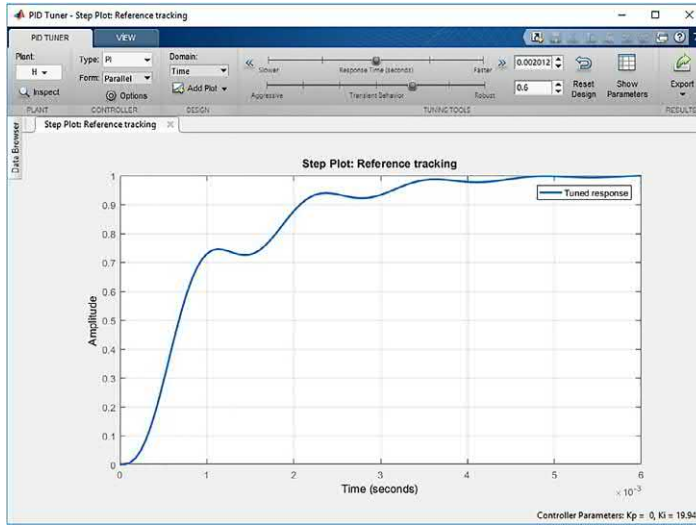



**FIG. 8.57** `pidTuner` application environment.

Select desired controller type from the Type drop down list (Fig. 8.58).

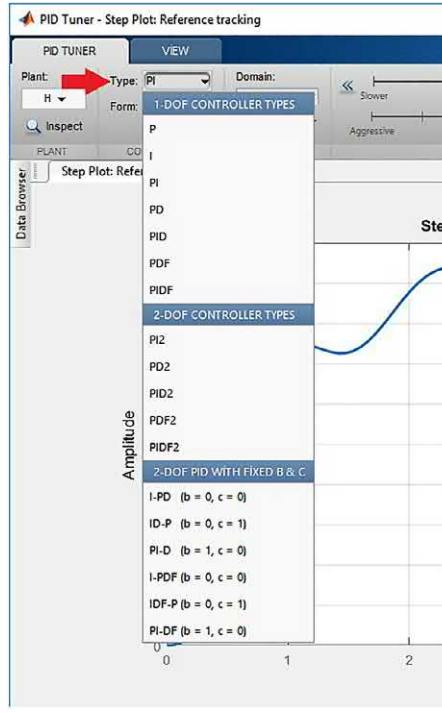



**FIG. 8.58** Different types of controllers, which are tunable by `pidTuner` application.

Use the sliders to obtain the desired time response (Fig. 8.59).

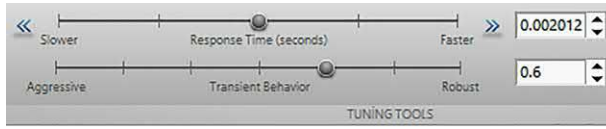



**FIG. 8.59** Sliders are used to obtain the desired response.

You can use the Domain: Frequency (Fig. 8.60) to tune the controller using frequency domain criteria, i.e., bandwidth and phase margin. Generally, phase margin must be greater than 45°.


**FIG. 8.60** Tuning the controller in frequency domain.

The PID Tuner shows the value of gains in the right bottom of the window (Kp is the proportional gain and Ki is integrator gain) (Fig. 8.61).

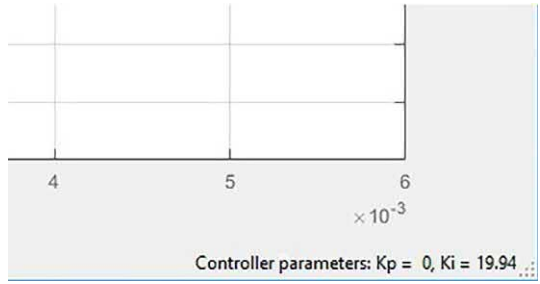



**FIG. 8.61** Kp and Ki show the value of proportional gain and integral gain (for a PI controller), respectively.

You can export the designed controller to MATLAB Workspace by clicking the Export button (Fig. 8.62).

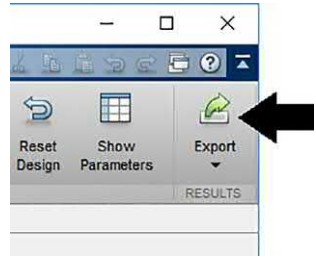



**FIG. 8.62** Transferring the designed controller into MATLAB® Workspace.

## 8.19 Input/output impedance of converter

The input impedance of a DC-DC converter is the impedance seen from the input DC source. The output impedance is defined as the output voltage response of converter for the excitation of current $i_Z$ at constant input voltage $V_G$ and duty ratio $D$. In some descriptions, the output impedance includes the load, in others it does not (Fig. 8.63).

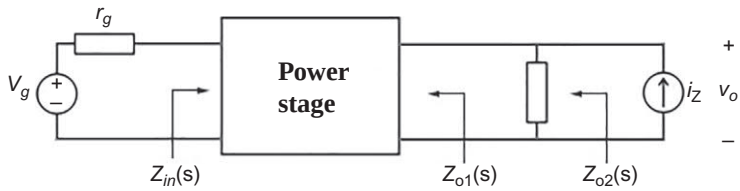



**FIG. 8.63** Input impedance of converter and two variants of the output impedance of converter.

The input/output of converter can be extracted in the same way that control-to-output transfer function ($\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$) extracted. Assume that we want to extract the input and output impedance of the buck converter shown in Fig. 8.64.

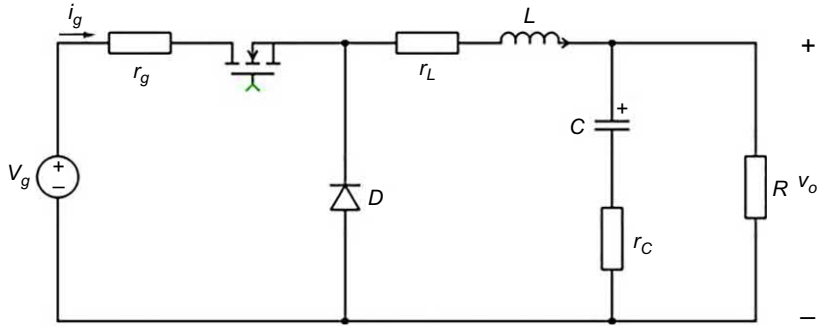



**FIG. 8.64** Schematic of a buck converter. $rg$, $r_L$, and $r_C$ show the internal resistance of input source, inductor ESR, and capacitor ESR, respectively.

As earlier when the MOSFET switch is closed, the diode is reverse-biased. The equivalent circuit of Fig. 8.65 represents this case. io is a fictitious current source added to the circuit in order to measure the output impedance ($Z_o(s) = \frac{\text{vo(s)}}{\text{io(s)}}$).

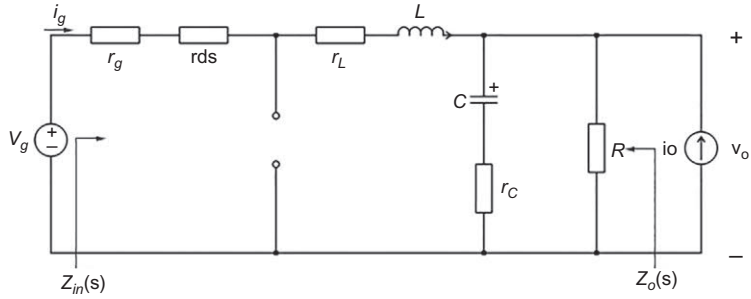



**FIG. 8.65** Equivalent circuit of buck converter with closed MOSFET.

According to Fig. 8.65, the circuit differential equations can be written as:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left(-\left(r_g + r_{ds} + r_L + \dfrac{R \times r_C}{R + r_C}\right) i_L - \dfrac{R}{R + r_C} v_C - \dfrac{R \times r_C}{R + r_C} i_O + v_g\right) \\ \dfrac{dv_C(t)}{dt} = \dfrac{1}{C}\left(\dfrac{R}{R + r_C} i_L - \dfrac{1}{R + r_C} v_C + \dfrac{R}{R + r_C} i_O\right) \end{cases} \tag{8.141}$$

$$i_g = i_L$$

$$v_o = r_C C \frac{dv_C}{dt} + v_C = \frac{R \times r_C}{R + r_C} i_L + \frac{R}{R + r_C} v_C + \frac{R \times r_C}{R + r_C} i_O$$

We need to define two outputs ($i_g$ and $v_o$) in order to calculate the input/output impedance. Applying the SSA to the equations leads to six different transfer functions: $\frac{\tilde{i}_g(s)}{\tilde{d}(s)}$, $\frac{\tilde{i}_g(s)}{\tilde{v}_g(s)}$, $\frac{\tilde{i}_g(s)}{\tilde{i}_o(s)}$, $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$, $\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}$, and $\frac{\tilde{v}_o(s)}{\tilde{i}_o(s)}$. Output impedance of the converter is extracted with the aid of $\frac{\tilde{v}_o(s)}{\tilde{i}_o(s)}$. The input impedance of converter is calculated using $\frac{1}{\frac{\tilde{i}_g(s)}{\tilde{v}_g(s)}}$.

When the MOSFET is open, the diode becomes forward-biased to carry the inductor current. The equivalent circuit shown in Fig. 8.66 represents this case. As before, rD and VD show the diode resistance and diode forward voltage drop, respectively.

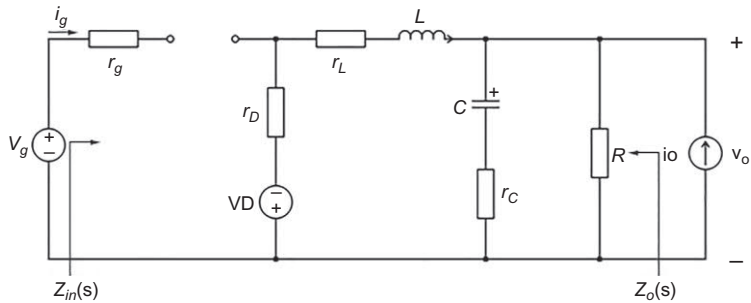



**FIG. 8.66** Equivalent circuit of buck converter with open MOSFET.

According to Fig. 8.66, the circuit differential equations can be written as:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left(-\left(r_D + r_L + \dfrac{R \times r_C}{R + r_C}\right) i_L - \dfrac{R}{R + r_C} v_C - \dfrac{R \times r_C}{R + r_C} i_O - v_D\right) \\ \dfrac{dv_C(t)}{dt} = \dfrac{1}{C}\left(\dfrac{R}{R + r_C} i_L - \dfrac{1}{R + r_C} v_C + \dfrac{R}{R + r_C} i_O\right) \end{cases} \tag{8.142}$$

$$i_g = 0$$

$$v_o = r_C C \frac{dv_C}{dt} + v_C = \frac{R \times r_C}{R + r_C} i_L + \frac{R}{R + r_C} v_C + \frac{R \times r_C}{R + r_C} i_O$$

Consider a buck converter with parameters as shown in Table 8.3.

**TABLE 8.3 The buck converter parameters (see Fig. 8.64).**

| | Nominal Value |
|---|---|
| Output voltage, vo | 20 V |
| Duty ratio, D | 0.4 |
| Input DC source voltage, Vg | 50 V |
| Input DC source internal resistance, rg | 0.01 Ω |
| MOSFET Drain-Source resistance, rds | 40 mΩ |
| Capacitor, C | 100 μF |
| Capacitor ESR, rC | 0.05 Ω |
| Inductor, L | 400 μH |
| Inductor ESR, rL | 50 mΩ |
| Diode voltage drop, vD | 0.7 V |
| Diode forward resistance, rD | 10 mΩ |
| Load resistor, R | 20 Ω |
| Switching Frequency, Fsw | 20 kHz |

The following program extracts the input and output impedance of buck converter with the parameters as shown in Table 8.3. Note that variable `vo_io` keeps the $\frac{\tilde{v}_o(s)}{\tilde{i}_o(s)}$ transfer function, variable `vo_d` keeps the $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$ transfer function, so on.

```
%This program calculates the input and output impedance of the Buck
%converter.

clc

clear all
syms vg rg d rL L rC C R vC iL rds rD vD io

%Converter Dynamical equations
%M1: diL/dt for closed MOSFET.
%M2: dvC/dt for closed MOSFET.
%M3: current of input DC source for closed MOSFET.
%M4: output voltage of converter for closed MOSFET.

%M5: diL/dt for open MOSFET.
%M6: dvC/dt for open MOSFET.
%M7: current of input DC source for open MOSFET.
%M8: output voltage of converter for open MOSFET.

M1=(-(rg+rds+rL+R*rC/(R+rC))*iL-R/(R+rC)*vC-R*rC/(R+rC)*
io+vg)/L;
M2=(R/(R+rC)*iL-1/(R+rC)*vC+R/(R+rC)*io)/C;
M3=iL;
M4=R*rC/(R+rC)*iL+R/(R+rC)*vC+R*rC/(R+rC)*io;

M5=(-(rD+rL+R*rC/(R+rC))*iL-R/(R+rC)*vC-R*rC/(R+rC)*io-vD)/L;
M6=(R/(R+rC)*iL-1/(R+rC)*vC+R/(R+rC)*io)/C;
M7=0;
M8=R*rC/(R+rC)*iL+R/(R+rC)*vC+R*rC/(R+rC)*io;

%Averaged Equations
diL_dt_ave=simplify(M1*d+M5*(1-d));
dvC_dt_ave=simplify(M2*d+M6*(1-d));
ig_ave=simplify(M3*d+M7*(1-d));
vo_ave=simplify(M4*d+M8*(1-d));

%DC Operating Point
DC=solve(diL_dt_ave==0,dvC_dt_ave==0,'iL','vC');
IL=DC.iL;
VC=DC.vC;

%Linearization
A11=simplify(subs(diff(diL_dt_ave,iL),[iL vC io],[IL VC 0]));
A12=simplify(subs(diff(diL_dt_ave,vC),[iL vC io],[IL VC 0]));
A21=simplify(subs(diff(dvC_dt_ave,iL),[iL vC io],[IL VC 0]));
A22=simplify(subs(diff(dvC_dt_ave,vC),[iL vC io],[IL VC 0]));
AA=[A11 A12;A21 A22];

B11=simplify(subs(diff(diL_dt_ave,io),[iL vC io],[IL VC 0]));
B12=simplify(subs(diff(diL_dt_ave,vg),[iL vC io],[IL VC 0]));
B13=simplify(subs(diff(diL_dt_ave,d),[iL vC io],[IL VC 0]));
```

```
B21=simplify(subs(diff(dvC_dt_ave,io),[iL vC io],[IL VC 0]));
B22=simplify(subs(diff(dvC_dt_ave,vg),[iL vC io],[IL VC 0]));
B23=simplify(subs(diff(dvC_dt_ave,d),[iL vC io],[IL VC 0]));

BB=[B11 B12 B13;B21 B22 B23];

C11=simplify(subs(diff(ig_ave,iL),[iL vC io],[IL VC 0]));
C12=simplify(subs(diff(ig_ave,vC),[iL vC io],[IL VC 0]));

C21=simplify(subs(diff(vo_ave,iL),[iL vC io],[IL VC 0]));
C22=simplify(subs(diff(vo_ave,vC),[iL vC io],[IL VC 0]));
CC=[C11 C12; C21 C22];

D11=simplify(subs(diff(ig_ave,io),[iL vC io],[IL VC 0 ]));
D12=simplify(subs(diff(ig_ave,vg),[iL vC io],[IL VC 0]));
D13=simplify(subs(diff(ig_ave,d),[iL vC io],[IL VC 0]));

D21=simplify(subs(diff(vo_ave,io),[iL vC io],[IL VC 0 ]));
D22=simplify(subs(diff(vo_ave,vg),[iL vC io],[IL VC 0]));
D23=simplify(subs(diff(vo_ave,d),[iL vC io],[IL VC 0]));
DD=[D11 D12 D13;D21 D22 D23];

%Components Values
%Variables have underline are used to store the numeric values of
components
%Variables without underline are symbolic variables.
%for example:
%L: symbolic vvariable shows the inductor inductance
%L_: numeric variable shows the inductor inductance value.
L_=400e-6;
rL_=.05;
C_=100e-6;
rC_=.05;
rds_=.04;
rD_=.01;
VD_=.7;
D_=.4;
VG_=50;
rg_=.01;
R_=20;

AA_=eval(subs(AA,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));
BB_=eval(subs(BB,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));
CC_=eval(subs(CC,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));
```

```
DD_=eval(subs(DD,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));

sys=ss(AA_,BB_,CC_,DD_);
sys.stateName={'iL','vC'};
sys.inputname={'io','vg','d'};
sys.outputname={'ig','vo'};

ig_io=sys(1,1);
ig_vg=sys(1,2);
ig_d=sys(1,3);

vo_io=sys(2,1);
vo_vg=sys(2,2);
vo_d=sys(2,3);

Zin=1/ig_vg; %input impedance
Zout=vo_io; %output impedance

%Draws the bode diagram of input/output impedance
figure(1)
bode(Zin), grid minor

figure(2)
bode(Zout), grid minor

%Display the DC operating point of converter
disp('steady state operating point of converter')
disp('IL')
disp(eval(subs(IL,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0])));
disp('VC')
disp(eval(subs(VC,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0])));
```

The program gives the following transfer functions:

$$\begin{aligned}
\frac{\widetilde{v}_o(s)}{\widetilde{d}(s)} &= 6316.8\frac{s+2\times10^5}{s^2+813.4s+2.503\times10^7}\\
Z_{in}(s) = \frac{\widetilde{v}_g(s)}{\widetilde{i}_g(s)} &= 0.0025\frac{s^2+813.4s+2.503\times10^7}{s+498.8}\\
Z_o(s) = \frac{\widetilde{v}_o(s)}{\widetilde{i}_o(s)} &= 0.049875\frac{\left(s+2\times10^5\right)(s+190)}{s^2+813.4s+2.503\times10^7}\\
\frac{\widetilde{v}_o(s)}{\widetilde{v}_g(s)} &= 49.875\frac{\left(s+2\times10^5\right)}{s^2+813.4s+2.503\times10^7}
\end{aligned} \tag{8.143}$$

Bode diagram of control-to-output transfer function ($\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$), input impedance ($Z_{in}(s)=\frac{\tilde{v}_g(s)}{\tilde{i}_g}(s)$), output impedance ($Z_o(s)=\frac{\tilde{v}_o(s)}{\tilde{i}_o}(s)$), and audio susceptibility ($\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}$) are shown in Figs. 8.67, 8.68, 8.69, and 8.70, respectively.

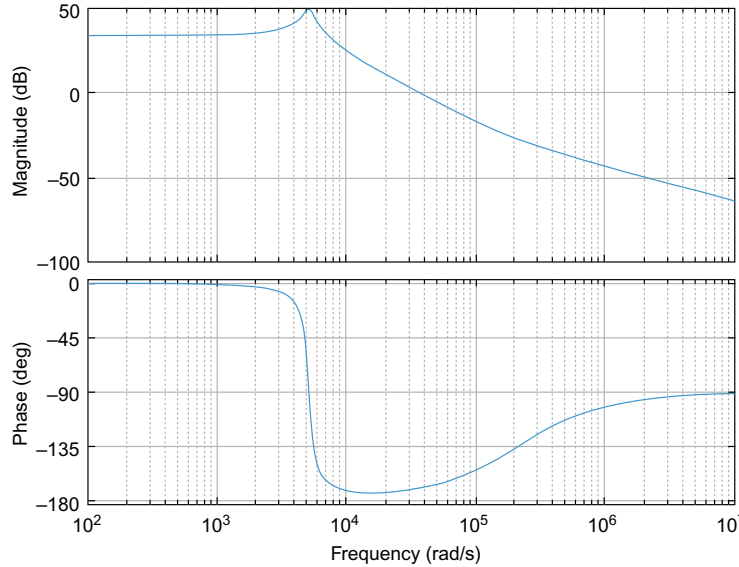



**FIG. 8.67** Bode diagram of control-to-output transfer function ($\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$) for the buck converter with parameters as shown in Table 8.3.

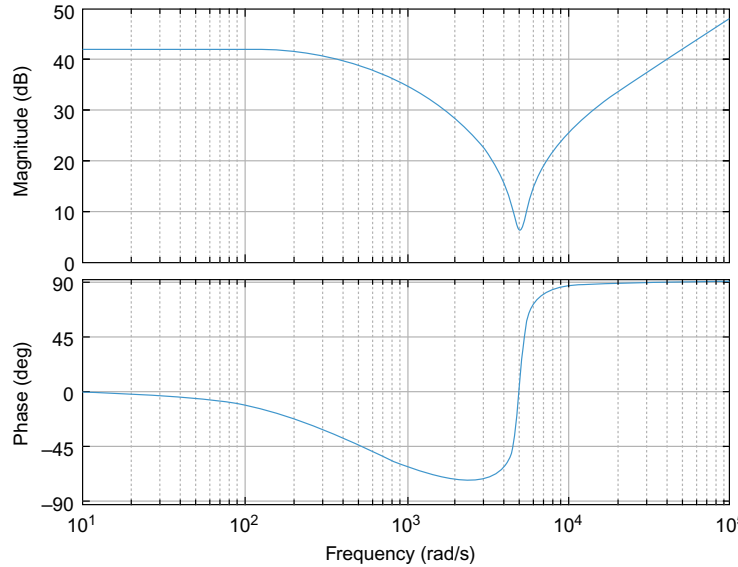



**FIG. 8.68** Bode diagram of input impedance ($Z_{in}(s)$) for the buck converter with parameters as shown in Table 8.3.

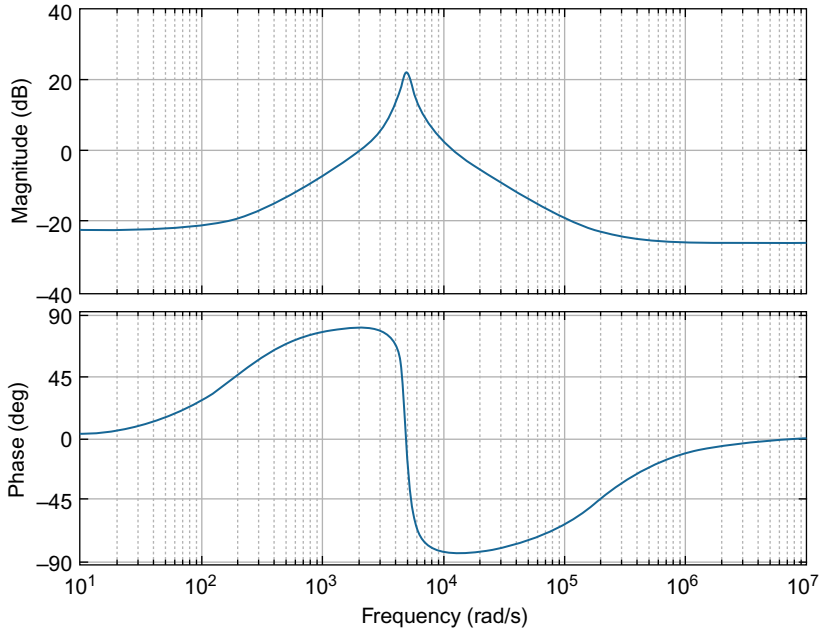



**FIG. 8.69** Bode diagram of output impedance ($Z_o(s)$) for the buck converter with parameters as shown in Table 8.3.

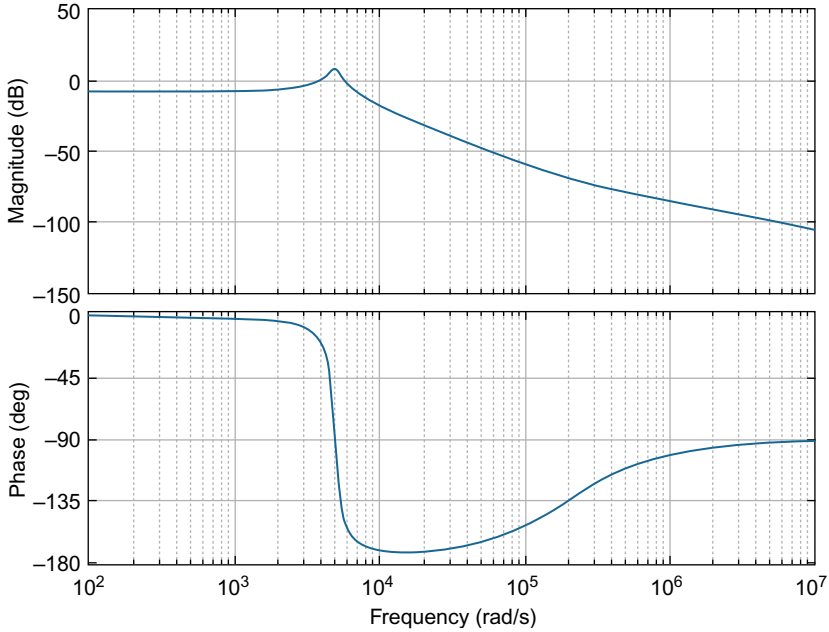



**FIG. 8.70** Bode diagram of audio susceptibility ($\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}$) for the buck converter with parameters as shown in Table 8.3.

The dynamical model shown in Fig. 8.71 can be drawn for the buck converter with parameters as shown in Table 8.3.

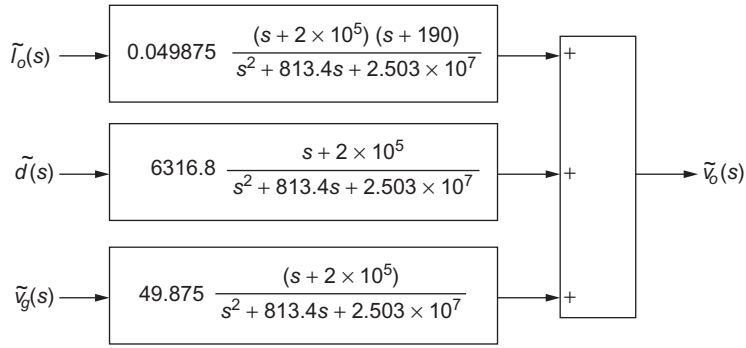



**FIG. 8.71** Dynamical model of the studied buck converter.

## 8.20 Effect of feedback control on output impedance

Fig. 8.71 shows the open loop model of buck converter with the parameters shown in Table 8.3. Consider a simple feedback control system such as the one shown in Fig. 8.72.

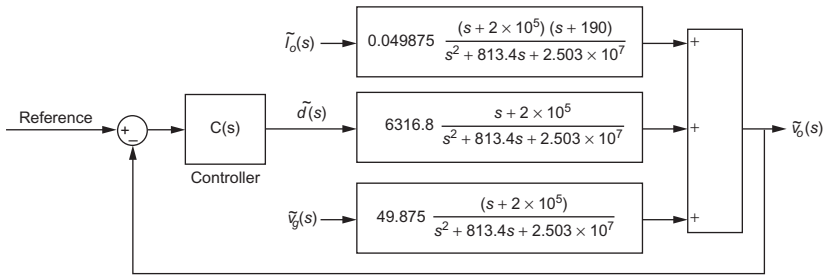



**FIG. 8.72** Voltage Mode (VM) control of the studied buck converter. The $\tilde{i}_o$ and $\tilde{v}_g$ inputs play the role of disturbance.

Assume that the controller is a simple I-type controller ($C(s) = \frac{4.85}{s}$). Fig. 8.73 shows the step response (from Reference input to $\tilde{v}_o$ output) of the closed loop.

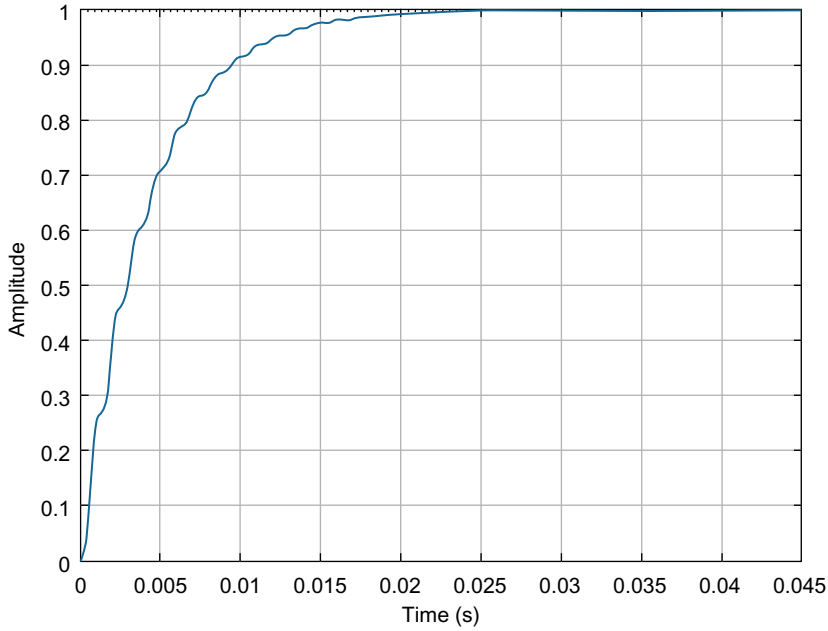



**FIG. 8.73** Step response of closed-loop control system shown in Fig. 8.72 with $C(s)=\frac{4.85}{s}$.

According to Fig. 8.72, the closed-loop output impedance ($Z_{o,CL}(s)$) is:

$$Z_{o,\ CL}(s)=Z_{o,\ OL}(s)\times\frac{1}{1+C(s)\times\dfrac{vo(s)}{d(s)}} \tag{8.144}$$

$$\begin{aligned}Z_{o,\ CL}(s)\ &=0.049875\times\frac{(s+2\times10^5)(s+190)}{s^2+813.4s+2.503\times10^7}\\&\quad\times\frac{1}{1+\dfrac{4.85}{s}\times6316.8\times\dfrac{(s+2\times10^5)}{s^2+813.4s+2.503\times10^7}}\\&=\frac{0.04988s^5+10^4s^4+1.13\times10^7s^3+2.515\times10^{11}s^2+4.744\times10^{13}s}{s^5+1627s^4+5.075\times10^7s^3+4.687\times10^{10}+6.323\times10^{14}s+1.534\times10^{17}}\end{aligned} \tag{8.145}$$

In order to calculate the closed-loop output impedance, set the $\widetilde{v}_g$ and Reference input to zero and calculate the transfer function from $\widetilde{i}_o$ input to $\widetilde{v}_o$ output.

Fig. 8.74 is a comparison between the open-loop output impedance ($Z_{o,OL}(s)$, Eq. (8.143)) and the closed-loop output impedance ($Z_{o,CL}(s)$, Eq. (8.145)).

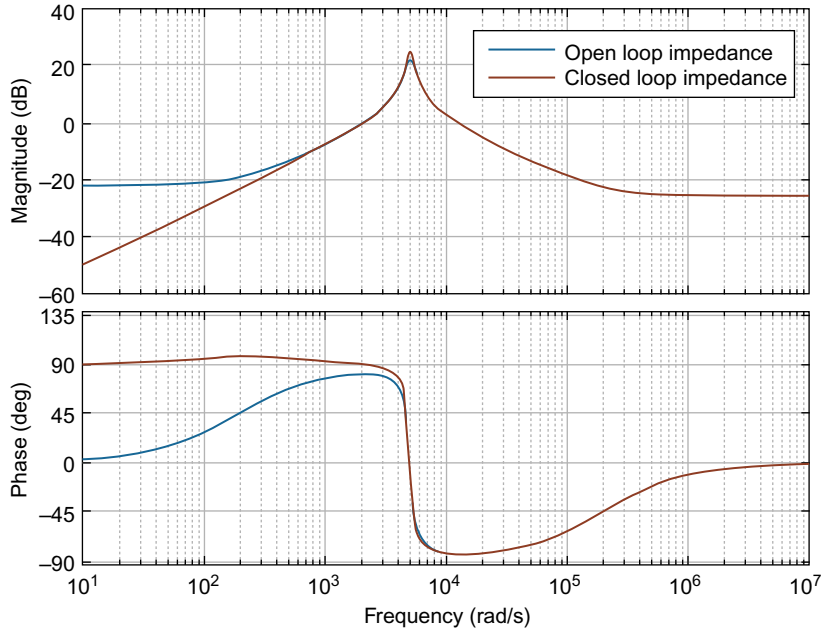



**FIG. 8.74** Comparison between open-loop output impedance and closed-loop output impedance. Feedback reduced the output impedance.

The closed-loop output impedance is reduced at low-frequency portion of the graph. Reduction of output impedance is one of the desired properties of feedback control.

## 8.21 Dynamic of buck-boost converter

Schematic of buck-boost converter is shown in Fig. 8.75.

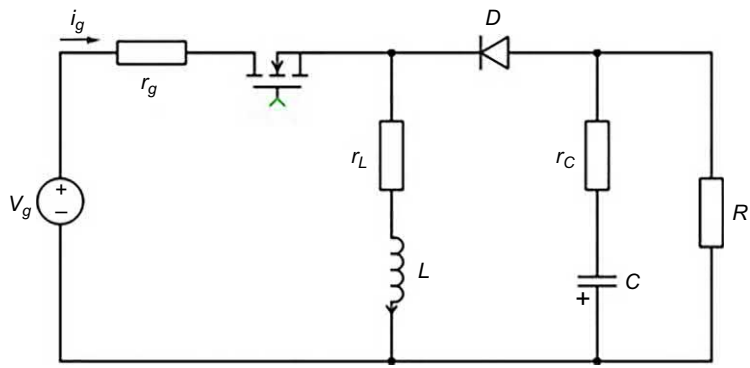



**FIG. 8.75** Schematic of buck-boost converter.

When the MOSFET is closed, the diode is reverse biased. According to Fig. 8.76, the circuit differential equation is:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left(-\left(r_g + r_{ds} + r_L\right) i_L + v_g\right) \\ \dfrac{dv_C(t)}{dt} = \dfrac{1}{C}\left(\dfrac{R}{R + r_C} i_O - \dfrac{1}{R + r_C} v_C\right) \end{cases} \tag{8.146}$$

$$i_g = i_L$$

$$v_o = \frac{R}{R + r_C} v_C + \frac{R \times r_C}{R + r_C} i_O$$

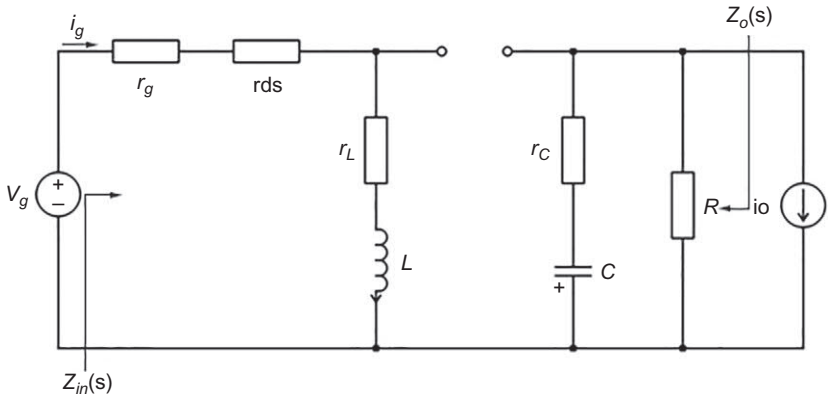



**FIG. 8.76** Equivalent circuit of buck-boost converter with closed MOSFET.

When the MOSFET switch is opened, the diode becomes forward-biased. According to Fig. 8.77, the circuit differential equation is:

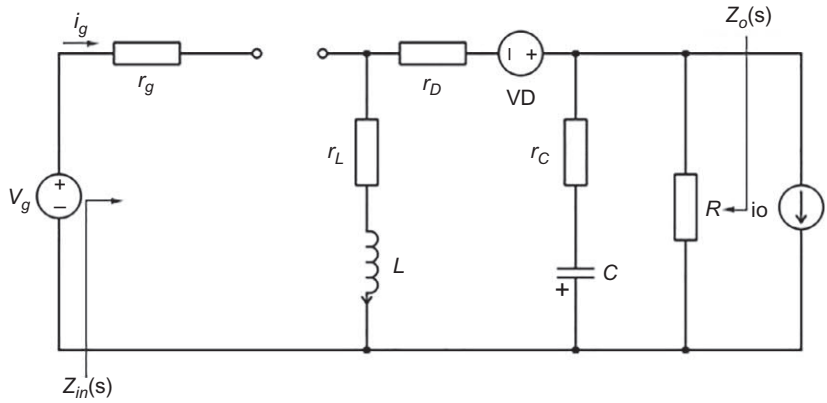



**FIG. 8.77** Equivalent circuit of buck-boost converter with open MOSFET.

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left(-\left(r_D + r_L + \dfrac{R \times r_C}{R + r_C}\right) i_L - \dfrac{R}{R + r_C} v_C - \dfrac{R \times r_C}{R + r_C} i_O - v_D\right) \\ \dfrac{dv_C(t)}{dt} = \dfrac{1}{C}\left(\dfrac{R}{R + r_C} i_L - \dfrac{1}{R + r_C} v_C + \dfrac{R}{R + r_C} i_O\right) \end{cases} \tag{8.147}$$

$$i_g = 0$$

$$v_o = \frac{R \times r_C}{R + r_C} i_L + \frac{R}{R + r_C} v_C + \frac{R \times r_C}{R + r_C} i_O + \mathrm{V_D}$$

Assume a buck-boost converter with the following parameters.

The following program extracts the small-signal transfer functions of a buck-boost converter with component values as shown in Table 8.4.

**TABLE 8.4** The buck-boost converter parameters (see Fig. 8.75).

| | Nominal value |
|---|---|
| Output voltage, vo | −16 V |
| Duty ratio, D | 0.4 |
| Input DC source voltage, Vg | 24 V |
| Input DC source internal resistance, rg | 0.1 Ω |
| MOSFET Drain-Source resistance, rds | 40 mΩ |
| Capacitor, C | 80 μF |
| Capacitor ESR, rC | 0.05 Ω |
| Inductor, L | 20 μH |
| Inductor ESR, rL | 10 mΩ |
| Diode voltage drop, vD | 0.7 V |
| Diode forward resistance, rD | 10 mΩ |
| Load resistor, R | 5 Ω |
| Switching Frequency, Fsw | 100 kHz |

```
%This program calculates the small signal transfer functions of
Buck-Boost
%converter.

clc
```

```
clear all
syms vg rg d rL L rC C R vC iL rds rD vD io

%Converter Dynamical equations
%M1: diL/dt for closed MOSFET.
%M2: dvC/dt for closed MOSFET.
%M3: current of input DC source for closed MOSFET.
%M4: output voltage of converter for closed MOSFET.

%M5: diL/dt for open MOSFET.
%M6: dvC/dt for open MOSFET.
%M7: current of input DC source for open MOSFET.
%M8: output voltage of converter for open MOSFET.

M1=(-(rg+rds+rL)*iL+vg)/L;
M2=(R/(R+rC)*io-vC/(R+rC))/C;
M3=iL;
M4=R*rC/(R+rC)*io+R/(R+rC)*vC;

M5=(-(rL+rD+rC*R/(R+rC))*iL-R/(R+rC)*vC-R*rC/(R+rC)*io-vD)/L;
M6=(R/(R+rC)*iL-1/(R+rC)*vC+R/(R+rC)*io)/C;
M7=0;
M8=rC*R/(rC+R)*iL+R/(R+rC)*vC+R*rC/(R+rC)*io+vD;

%Averaged Equations
diL_dt_ave=simplify(M1*d+M5*(1-d));
dvC_dt_ave=simplify(M2*d+M6*(1-d));
ig_ave=simplify(M3*d+M7*(1-d));
vo_ave=simplify(M4*d+M8*(1-d));

%DC Operating Point
DC=solve(diL_dt_ave==0,dvC_dt_ave==0,'iL','vC');
IL=DC.iL;
VC=DC.vC;

%Linearization
A11=simplify(subs(diff(diL_dt_ave,iL),[iL vC io],[IL VC 0]));
A12=simplify(subs(diff(diL_dt_ave,vC),[iL vC io],[IL VC 0]));
A21=simplify(subs(diff(dvC_dt_ave,iL),[iL vC io],[IL VC 0]));
A22=simplify(subs(diff(dvC_dt_ave,vC),[iL vC io],[IL VC 0]));
AA=[A11 A12;A21 A22];

B11=simplify(subs(diff(diL_dt_ave,io),[iL vC io],[IL VC 0]));
B12=simplify(subs(diff(diL_dt_ave,vg),[iL vC io],[IL VC 0]));
B13=simplify(subs(diff(diL_dt_ave,d),[iL vC io],[IL VC 0]));

B21=simplify(subs(diff(dvC_dt_ave,io),[iL vC io],[IL VC 0]));
B22=simplify(subs(diff(dvC_dt_ave,vg),[iL vC io],[IL VC 0]));
B23=simplify(subs(diff(dvC_dt_ave,d),[iL vC io],[IL VC 0]));
```

```
BB=[B11 B12 B13;B21 B22 B23];

C11=simplify(subs(diff(ig_ave,iL),[iL vC io],[IL VC O]));
C12=simplify(subs(diff(ig_ave,vC),[iL vC io],[IL VC O]));

C21=simplify(subs(diff(vo_ave,iL),[iL vC io],[IL VC O]));
C22=simplify(subs(diff(vo_ave,vC),[iL vC io],[IL VC O]));
CC=[C11 C12; C21 C22];

D11=simplify(subs(diff(ig_ave,io),[iL vC io],[IL VC O ]));
D12=simplify(subs(diff(ig_ave,vg),[iL vC io],[IL VC O]));
D13=simplify(subs(diff(ig_ave,d),[iL vC io],[IL VC O]));

D21=simplify(subs(diff(vo_ave,io),[iL vC io],[IL VC O ]));
D22=simplify(subs(diff(vo_ave,vg),[iL vC io],[IL VC O]));
D23=simplify(subs(diff(vo_ave,d),[iL vC io],[IL VC O]));
DD=[D11 D12 D13;D21 D22 D23];

%Components Values
%Variables have underline are used to store the numeric values of
components
%Variables without underline are symbolic variables.
%for example:
%L: symbolic vvariable shows the inductor inductance
%L_: numeric variable shows the inductor inductance value.
L_=20e-6;
rL_=.01;
C_=80e-6;
rC_=.05;
rds_=.04;
rD_=.01;
VD_=.7;
D_=.4;
VG_=24;
rg_=.1;
R_=5;

AA_=eval(subs(AA,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ O]));
BB_=eval(subs(BB,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ O]));
CC_=eval(subs(CC,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ O]));
DD_=eval(subs(DD,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ O]));

sys=ss(AA_,BB_,CC_,DD_);
sys.stateName={'iL','vC'};
```

```
sys.inputname={'io','vg','d'};
sys.outputname={'ig','vo'};

ig_io=sys(1,1);
ig_vg=sys(1,2);
ig_d=sys(1,3);

vo_io=sys(2,1);
vo_vg=sys(2,2);
vo_d=sys(2,3);

Zin=1/ig_vg; %input impedance
Zout=vo_io; %output impedance

%Draws the bode diagram of input/output impedance
figure(1)
bode(Zin), grid minor

figure(2)
bode(Zout), grid minor

%Display the DC operating point of converter
disp('steady state operating point of converter')
disp('IL')
disp(eval(subs(IL,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0])));
disp('VC')
disp(eval(subs(VC,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0])));
```

The program gives the following results:

$$\frac{v_o(s)}{d(s)} = -0.94123\frac{\left(s+1.267\times10^5\right)\left(s-1.168\times10^5\right)}{s^2+7560s+2.332\times10^8}$$

$$Z_{in}(s) = \frac{v_g(s)}{i_g(s)} = 0.000125\frac{s^2+7560s+2.332\times10^8}{s+2475} \tag{8.148}$$

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} = 0.049505\frac{\left(s+2.5\times10^5\right)(s+4194)}{s^2+7560s+2.332\times10^8}$$

Note that the obtained control-to-output transfer function is nonminimum phase, i.e., has a zero in right half-plane. Bode diagram of control-to-output transfer function, open loop input impedance, and open loop output impedance are shown in Figs. 8.78, 8.79, and 8.80, respectively.

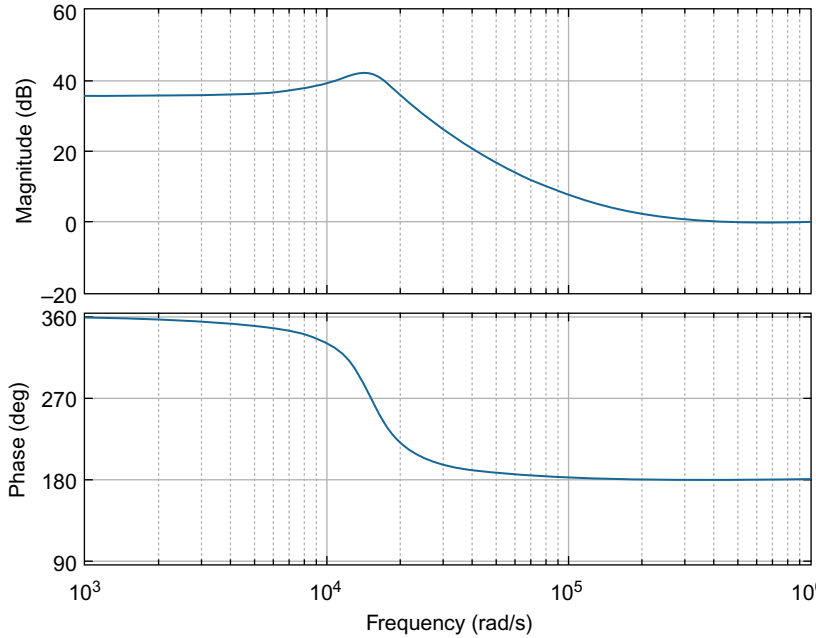



**FIG. 8.78** Bode diagram of control-to-output transfer function $(\frac{v_o(s)}{d(s)})$ for the buck-boost converter with parameters as shown in Table 8.4.

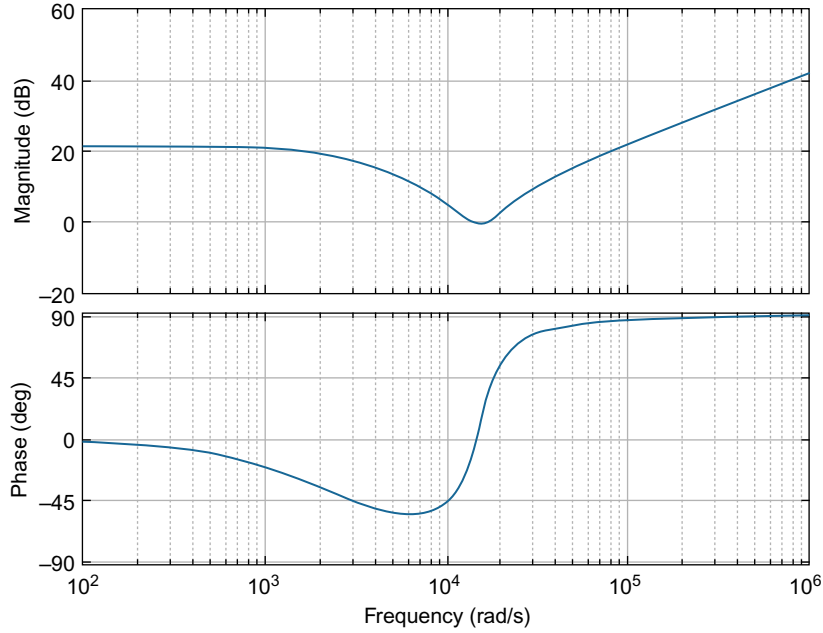



**FIG. 8.79** Bode diagram of input impedance $(\frac{v_g(s)}{i_g(s)})$ for the buck-boost converter with parameters as shown in Table 8.4.

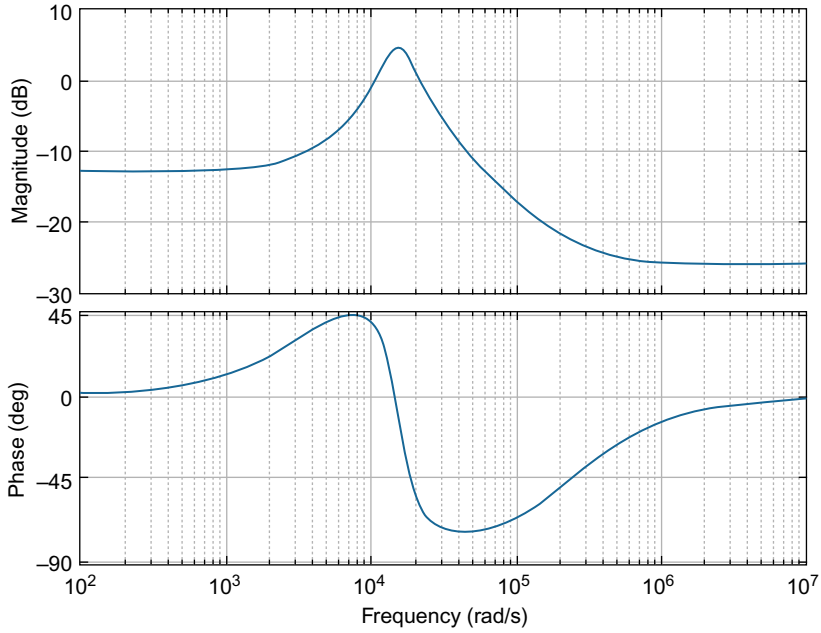



**FIG. 8.80** Bode diagram of output impedance $(\frac{\tilde{v}_o(s)}{\tilde{i}_o(s)})$ for the buck-boost converter with parameters as shown in Table 8.4.

## 8.22 Dynamics of boost converter

Schematic of boost converter is shown in Fig. 8.81.

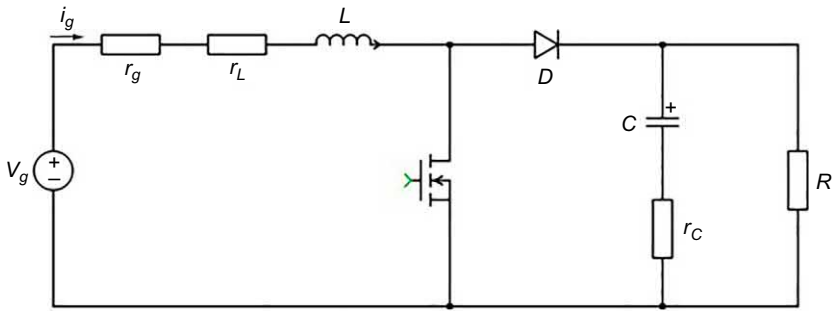



**FIG. 8.81** Schematic of boost converter.

When the MOSFET is closed, the diode is reverse biased.

According to Fig. 8.82, the circuit differential equation is:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left(-\left(r_g + r_{ds} + r_L\right)i_L + v_g\right) \\ \dfrac{dv_C(t)}{dt} = \dfrac{1}{C}\left(-\dfrac{1}{R + r_C}v_C + \dfrac{R}{R + r_C}i_O\right) \end{cases} \tag{8.149}$$

$$i_g = i_L$$

$$v_o = \frac{R}{R + r_C}v_C + \frac{R \times r_C}{R + r_C}i_O$$

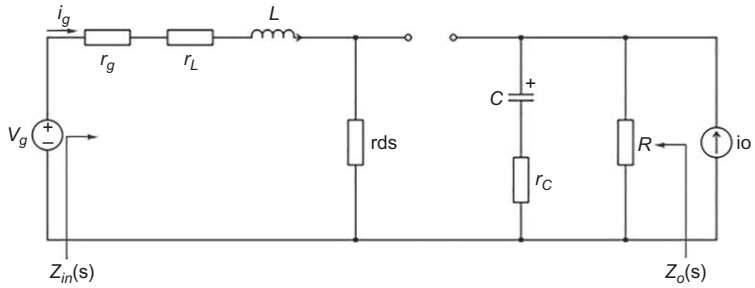



**FIG. 8.82** Equivalent circuit of boost converter with closed MOSFET.

When the MOSFET switch is opened, the diode becomes forward-biased. According to Fig. 8.83, the circuit differential equation is:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left(-\left(r_g + r_L + r_D + \dfrac{R \times r_C}{R + r_C}\right)i_L - \dfrac{R}{R + r_C}v_C - \dfrac{R \times r_C}{R + r_C}i_O + v_g - v_D\right) \\ \dfrac{dv_C(t)}{dt} = \dfrac{1}{C}\left(\dfrac{R}{R + r_C}i_L - \dfrac{1}{R + r_C}v_C + \dfrac{R}{R + r_C}i_O\right) \end{cases}$$

$$i_g = i_L$$

$$v_o = \frac{R \times r_C}{R + r_C}i_L + \frac{R}{R + r_C}v_C + \frac{R \times r_C}{R + r_C}i_O \tag{8.150}$$

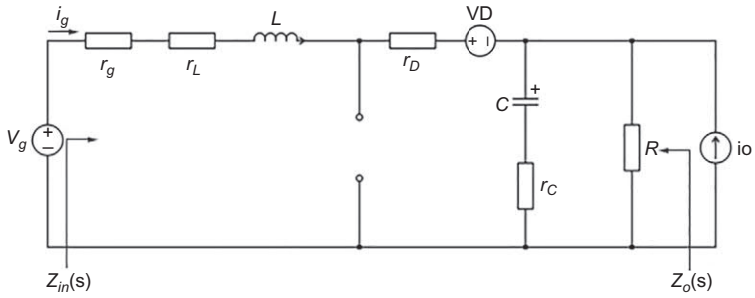



**FIG. 8.83** Equivalent circuit of boost converter with open MOSFET.

Assume a boost converter with the parameters as shown in Table 8.5.

**TABLE 8.5 The boost converter parameters (see Fig. 8.81).**

| | Nominal value |
|---|---|
| Output voltage, vo | 30 V |
| Duty ratio, D | 0.6 |
| Input DC source voltage, Vg | 12 V |
| Input DC source internal resistance, rg | 0.1 Ω |
| MOSFET Drain-Source resistance, rds | 40 mΩ |
| Capacitor, C | 100 μF |
| Capacitor ESR, rC | 0.05 Ω |
| Inductor, L | 120 μH |
| Inductor ESR, rL | 10 mΩ |
| Diode voltage drop, vD | 0.7 V |
| Diode forward resistance, rD | 10 mΩ |
| Load resistor, R | 50 Ω |
| Switching Frequency, Fsw | 25 kHz |

The following program extracts the small-signal transfer functions of a boost converter with component values as shown in Table 8.5.

```
%This program calculates the small signal transfer function of
the Boost
%converter.

clc

clear all
syms vg rg d rL L rC C R vC iL rds rD vD io

%Converter Dynamical equations
%M1: diL/dt for closed MOSFET.
%M2: dvC/dt for closed MOSFET.
%M3: current of input DC source for closed MOSFET.
%M4: output voltage of converter for closed MOSFET.

%M5: diL/dt for open MOSFET.
%M6: dvC/dt for open MOSFET.
```

```
%M7: current of input DC source for open MOSFET.
%M8: output voltage of converter for open MOSFET.

M1=(-(rg+rL+rds)*iL+vg)/L;
M2=(-vC/(R+rC)+R/(R+rC)*io)/C;
M3=iL;
M4=R/(R+rC)*vC+R*rC/(R+rC)*io;

M5=(-(rg+rL+rD+R*rC/(R+rC))*iL-R/(R+rC)*vC-R*rC/(R+rC)*io
+vg-vD)/L;
M6=((R/(R+rC))*iL-vC/(R+rC)+R/(R+rC)*io)/C;
M7=iL;
M8=R*rC/(R+rC)*iL-R/(R+rC)*vC+R*rC/(R+rC)*io;

%Averaged Equations
diL_dt_ave=simplify(M1*d+M5*(1-d));
dvC_dt_ave=simplify(M2*d+M6*(1-d));
ig_ave=simplify(M3*d+M7*(1-d));
vo_ave=simplify(M4*d+M8*(1-d));

%DC Operating Point
DC=solve(diL_dt_ave==0,dvC_dt_ave==0,'iL','vC');
IL=DC.iL;
VC=DC.vC;

%Linearization
A11=simplify(subs(diff(diL_dt_ave,iL),[iL vC io],[IL VC 0]));
A12=simplify(subs(diff(diL_dt_ave,vC),[iL vC io],[IL VC 0]));
A21=simplify(subs(diff(dvC_dt_ave,iL),[iL vC io],[IL VC 0]));
A22=simplify(subs(diff(dvC_dt_ave,vC),[iL vC io],[IL VC 0]));
AA=[A11 A12;A21 A22];

B11=simplify(subs(diff(diL_dt_ave,io),[iL vC io],[IL VC 0]));
B12=simplify(subs(diff(diL_dt_ave,vg),[iL vC io],[IL VC 0]));
B13=simplify(subs(diff(diL_dt_ave,d),[iL vC io],[IL VC 0]));

B21=simplify(subs(diff(dvC_dt_ave,io),[iL vC io],[IL VC 0]));
B22=simplify(subs(diff(dvC_dt_ave,vg),[iL vC io],[IL VC 0]));
B23=simplify(subs(diff(dvC_dt_ave,d),[iL vC io],[IL VC 0]));

BB=[B11 B12 B13;B21 B22 B23];

C11=simplify(subs(diff(ig_ave,iL),[iL vC io],[IL VC 0]));
C12=simplify(subs(diff(ig_ave,vC),[iL vC io],[IL VC 0]));
```

```
C21=simplify(subs(diff(vo_ave,iL),[iL vC io],[IL VC O]));
C22=simplify(subs(diff(vo_ave,vC),[iL vC io],[IL VC O]));
CC=[C11 C12; C21 C22];

D11=simplify(subs(diff(ig_ave,io),[iL vC io],[IL VC O ]));
D12=simplify(subs(diff(ig_ave,vg),[iL vC io],[IL VC O]));
D13=simplify(subs(diff(ig_ave,d),[iL vC io],[IL VC O]));

D21=simplify(subs(diff(vo_ave,io),[iL vC io],[IL VC O ]));
D22=simplify(subs(diff(vo_ave,vg),[iL vC io],[IL VC O]));
D23=simplify(subs(diff(vo_ave,d),[iL vC io],[IL VC O]));
DD=[D11 D12 D13;D21 D22 D23];

%Components Values
%Variables have underline are used to store the numeric values of
components
%Variables without underline are symbolic variables.
%for example:
%L: symbolic vvariable shows the inductor inductance
%L_: numeric variable shows the inductor inductance value.
L_=120e-6;
rL_=.01;
C_=100e-6;
rC_=.05;
rds_=.04;
rD_=.01;
VD_=.7;
D_=.6;
VG_=12;
rg_=.1;
R_=50;

AA_=eval(subs(AA,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));
BB_=eval(subs(BB,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));
CC_=eval(subs(CC,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));
DD_=eval(subs(DD,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0]));

sys=ss(AA_,BB_,CC_,DD_);
sys.stateName={'iL','vC'};
```

```
sys.inputname={'io','vg','d'};
sys.outputname={'ig','vo'};

ig_io=sys(1,1);
ig_vg=sys(1,2);
ig_d=sys(1,3);

vo_io=sys(2,1);
vo_vg=sys(2,2);
vo_d=sys(2,3);

Zin=1/ig_vg; %input impedance
Zout=vo_io; %output impedance

%Draws the bode diagram of input/output impedance
figure(1)
bode(Zin), grid minor

figure(2)
bode(Zout), grid minor

%Display the DC operating point of converter
disp('steady state operating point of converter')
disp('IL')
disp(eval(subs(IL,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0])));
disp('VC')
disp(eval(subs(VC,[vg rg rds rD vD rL L rC C R d io],[VG_ rg_ rds_
rD_ VD_ rL_ L_ rC_ C_ R_ D_ 0])));
```

The program gives the following results:

$$\frac{v_o(s)}{d(s)} = -0.007199\frac{(s+2\times10^6)(s-6.703\times10^4)}{s^2+1367s+1.356\times10^7}$$

$$Z_{in}(s) = \frac{v_g(s)}{i_g(s)} = 0.00012\frac{s^2+1367s+1.356\times10^7}{s+200} \tag{8.151}$$

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} = 0.049995\frac{(s+2\times10^6)(s+1160)}{s^2+1367s+1.356\times10^7}$$

Note that the obtained control-to-output transfer function is nonminimum phase like the buck-boost converter. Bode diagram of control-to-output transfer function, open loop input impedance, and open loop output impedance are shown in Figs. 8.84, 8.85, and 8.86, respectively.

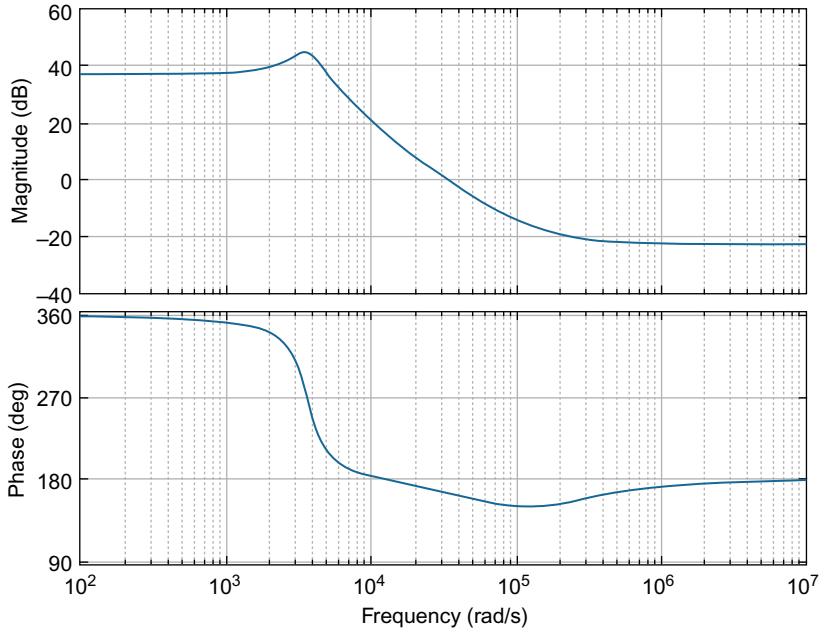



**FIG. 8.84** Bode diagram of control-to-output transfer function $(\frac{v_o(s)}{d(s)})$ for the boost converter with parameters as shown in Table 8.5.

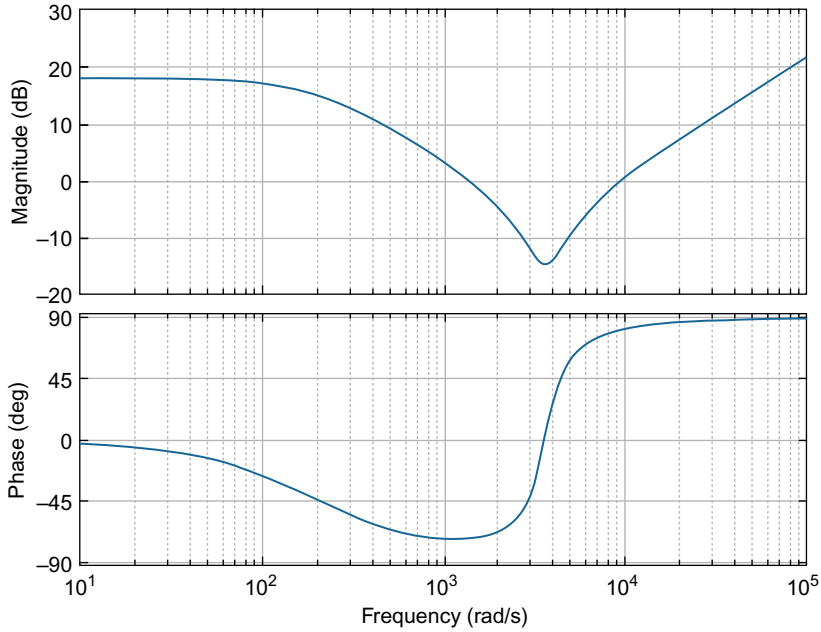



**FIG. 8.85** Bode diagram of input impedance $(\frac{v_g(s)}{i_g(s)})$ for the boost converter with parameters as shown in Table 8.5.

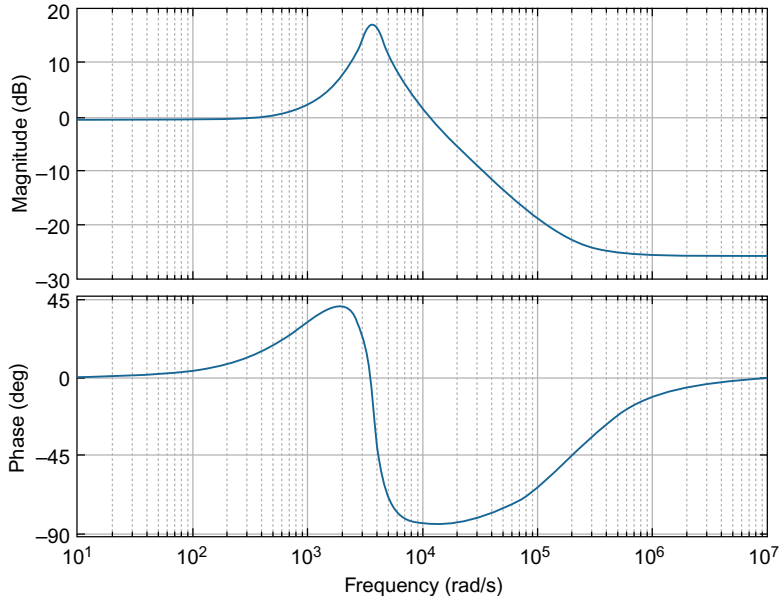



**FIG. 8.86** Bode diagram of output impedance $(\frac{\tilde{v}_o(s)}{\tilde{i}_o(s)})$ for the boost converter with parameters as shown in Table 8.5.

## 8.23 Dynamics of zeta converter

Dynamic model of higher-order converters can be extracted in the same way studied before. In this section, we study the dynamics of a zeta converter, which has fourth-order transfer functions.

Schematic of a zeta converter is shown in Fig. 8.87.

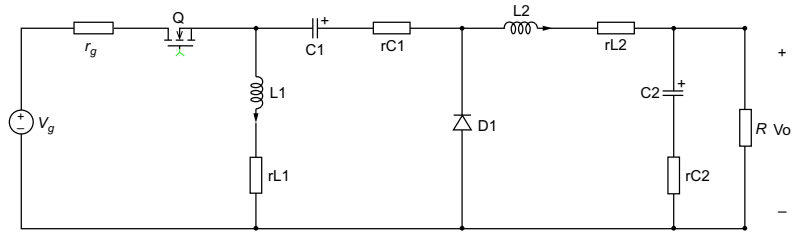



**FIG. 8.87** Schematic of zeta converter.

The zeta converter has two switches: a MOSFET switch and a diode. In this schematic, Vg, rg, Li, rLi, Ci, rCi, and R show the input DC source, internal resistance of input DC source, $i^{th}$ inductor, $i^{th}$ inductor Equivalent Series Resistance (ESR), $i^{th}$ capacitor, $i^{th}$ capacitor ESR, and load of converter, respectively. iO is a fictitious current source added to the schematic in order to calculate the output impedance of converter. We assume that converter operates in CCM. The parameters are as shown in Table 8.6.

**TABLE 8.6 The zeta converter parameters (see Fig. 8.87).**

| | Nominal value |
|---|---|
| Output voltage, Vo | 5.2 V |
| Duty ratio, D | 0.23 |
| Input DC source voltage, Vg | 20 V |
| Input DC source internal resistance, rg | 0.0 Ω |
| MOSFET Drain-Source resistance, rds | 10 mΩ |
| Capacitor, C1 | 100 μF |
| Capacitor Equivalent Series Resistance(ESR), rC1 | 0.19 Ω |
| Capacitor, C2 | 220 μF |
| Capacitor Equivalent Series Resistance(ESR), rC2 | 0.095 Ω |
| Inductor, L1 | 100 μH |
| Inductor ESR, rL1 | 1 mΩ |
| Inductor, L2 | 55 μH |
| Inductor ESR, rL2 | 0.55 mΩ |
| Diode voltage drop, vD | 0.7 V |
| Diode forward resistance, rD | 10 mΩ |
| Load resistor, R | 6 Ω |
| Switching Frequency, Fsw | 100 kHz |

MOSFET switch is closed for $D$. $T$ seconds and is open for duration of $(1-D)$. $T$ seconds. $D$ and $T$ show duty ratio and switching period, respectively.

When MOSFET is closed, the diode is reverse biased.

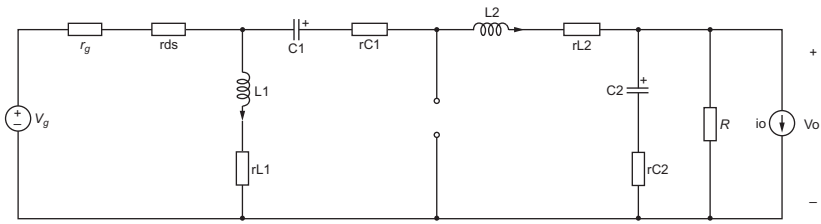



**FIG. 8.88** Equivalent circuit of zeta converter when MOSFET is closed.

In this case, the circuit differential equations can be written as:

$$\begin{cases} L_1\dfrac{di_{L_1}}{dt} = -\left(r_{L_1}+r_g+r_{ds}\right)i_{L_1} - \left(r_g+r_{ds}\right)i_{L_2} + v_g \\ L_2\dfrac{di_{L_2}}{dt} = -\left(r_g+r_{ds}\right)i_{L_1} - \left(r_g+r_{ds}+r_{C_1}+r_{L_2}+\dfrac{R\times r_{C_2}}{R+r_{C_2}}\right)i_{L_2} + v_{C_1} \\ \qquad\qquad -\dfrac{R}{R+r_{C_2}}v_{C_2} + \dfrac{R\times r_{C_2}}{R+r_{C_2}}i_o + v_g \\ C_1\dfrac{dv_{C_1}}{dt} = -i_{L_2} \\ C_2\dfrac{dv_{C_2}}{dt} = \dfrac{R}{R+r_{C_2}}i_{L_2} - \dfrac{1}{R+r_{C_2}}v_{C_2} - \dfrac{R}{R+r_{C_2}}i_o \end{cases}$$

$$v_o = r_{C_2}C_2\frac{dv_{C_2}}{dt} + v_{C_2} = \frac{R\times r_{C_2}}{R+r_{C_2}}i_{L_2} + \frac{R}{R+r_{C_2}}v_{C_2} - \frac{R\times r_{C_2}}{R+r_{C_2}}i_o \tag{8.152}$$

When MOSFET is opened, the diode is forward biased.

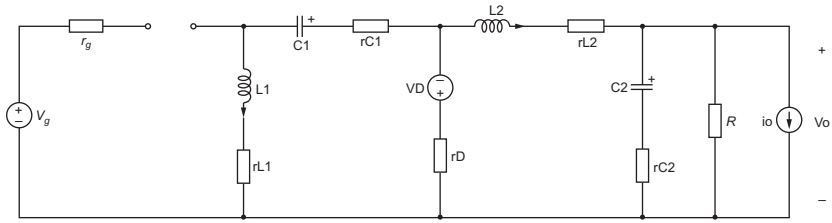



**FIG. 8.89** Equivalent circuit of zeta converter when MOSFET is opened. Forward-biased diode is modeled with a voltage source (VD) and a series resistance (rD).

In this case, the circuit differential equations can be written as:

$$\begin{cases} L_1\dfrac{di_{L_1}}{dt} = -\left(r_{L_1}+r_{C_1}+r_D\right)i_{L_1} - r_D i_{L_2} - v_{C_1} - v_D \\ L_2\dfrac{di_{L_2}}{dt} = -r_D i_{L_1} - \left(r_D+r_{L_2}+\dfrac{R\times r_{C_2}}{R+r_{C_2}}\right)i_{L_2} - \dfrac{R}{R+r_{C_2}}v_{C_2} + \dfrac{R\times r_{C_2}}{R+r_{C_2}}i_o - v_D \\ C_1\dfrac{dv_{C_1}}{dt} = i_{L_1} \\ C_2\dfrac{dv_{C_2}}{dt} = \dfrac{R}{R+r_{C_2}}i_{L_2} - \dfrac{1}{R+r_{C_2}}v_{C_2} - \dfrac{R}{R+r_{C_2}}i_o \end{cases}$$

$$v_o = r_{C_2}C_2\frac{dv_{C_2}}{dt} + v_{C_2} = \frac{R\times r_{C_2}}{R+r_{C_2}}i_{L_2} + \frac{R}{R+r_{C_2}}v_{C_2} - \frac{R\times r_{C_2}}{R+r_{C_2}}i_o \tag{8.153}$$

Following code extracts the converter transfer functions of a zeta converter with parameters as shown in Table 8.6.

```
% This program calculates the small signal transfer functions of
Zeta converter
clc
clear all

VG=20;       % Average value of input DC source
rg=0;        % Internal resistance of input DC source
rds=.01;     % MOSFET on resistance
C1=100e-6;   % Capacitor C1 value
C2=220e-6;   % Capacitor C2 value
rC1=.19;     % Capacitor C1 Equivalent Series Resistance(ESR)
rC2=.095;    % Capacitor C2 Equivalent Series Resistance(ESR)
L1=100e-6;   % Inductor L1 value
L2=55e-6;    % Inductor L2 value
rL1=1e-3;    % Inductor L1 Equivalent Series Resistance(ESR)
rL2=.55e-3;  % Inductor L2 Equivalent Series Resistance(ESR)
rD=.01;      % Diode series resistance
VD=.7;       % Diode voltage drop
R=6;         % Load resistance
D=.23;       % Duty cylcle
IO=0;        % Average value of output current source
fsw=100e3;   % Switching frequency

syms iL1 iL2 vC1 vC2 io vg vD d
% iL1: Inductor L1 current
% iL2: Inductor L2 current
% vC1: Capacitor C1 voltage
% vC2: Capacitor C2 voltage
% io : Output current source
% vg : Input DC source
% vD : Diode voltage drop
% d  : Duty cycle

%Closed MOSFET Equations
diL1_dt_MOSFET_close=(-(rL1+rg+rds)*iL1-(rg+rds)*iL2+vg)/L1;
diL2_dt_MOSFET_close=(-(rg+rds)*iL1-(rg+rds+rC1+rL2+R*rC2/(R
+rC2))*iL2+vC1-R/(R+rC2)*vC2+R*rC2/(R+rC2)*io+vg)/L2;
dvC1_dt_MOSFET_close=(-iL2)/C1;
dvC2_dt_MOSFET_close=(R/(R+rC2)*iL2-1/(R+rC2)*vC2-R/(R+rC2)
*io)/C2;
vo_MOSFET_close=R*rC2/(R+rC2)*iL2+R/(R+rC2)*vC2-R*rC2/
(R+rC2)*io;

%Opened MOSFET Equations
diL1_dt_MOSFET_open=(-(rL1+rC1+rD)*iL1-rD*iL2-vC1-vD)/L1;
diL2_dt_MOSFET_open=(-rD*iL1-(rD+rL2+R*rC2/(R+rC2))*iL2-R/(R
+rC2)*vC2+R*rC2/(R+rC2)*io-vD)/L2;
```

```
dvC1_dt_MOSFET_open=(iL1)/C1;
dvC2_dt_MOSFET_open=(R/(R+rC2)*iL2-1/(R+rC2)*vC2-R/(R+rC2)
*io)/C2;
vo_MOSFET_open=R*rC2/(R+rC2)*iL2+R/(R+rC2)*vC2-R*rC2/(R+rC2)*io;

%Averaging
averaged_diL1_dt=simplify(d*diL1_dt_MOSFET_close+(1-d)
*diL1_dt_MOSFET_open);
averaged_diL2_dt=simplify(d*diL2_dt_MOSFET_close+(1-d)
*diL2_dt_MOSFET_open);
averaged_dvC1_dt=simplify(d*dvC1_dt_MOSFET_close+(1-d)
*dvC1_dt_MOSFET_open);
averaged_dvC2_dt=simplify(d*dvC2_dt_MOSFET_close+(1-d)
*dvC2_dt_MOSFET_open);
averaged_vo=simplify(d*vo_MOSFET_close+(1-d)*vo_MOSFET_open);

%Substituting the steady values of input DC voltage source, Diode
voltage
%drop, Duty cycle and output current source and calculating the DC
%operating point
right_side_of_averaged_diL1_dt=subs(averaged_diL1_dt,[vg  vD  d
io],[VG VD D IO]);
right_side_of_averaged_diL2_dt=subs(averaged_diL2_dt,[vg  vD  d
io],[VG VD D IO]);
right_side_of_averaged_dvC1_dt=subs(averaged_dvC1_dt,[vg  vD  d
io],[VG VD D IO]);
right_side_of_averaged_dvC2_dt=subs(averaged_dvC2_dt,[vg  vD  d
io],[VG VD D IO]);

DC_OPERATING_POINT=
solve(right_side_of_averaged_diL1_dt==0,right_side_of_avera-
ged_diL2_dt==0,right_side_of_averaged_dvC1_dt==0,right_side_of_
averaged_dvC2_dt==0,'iL1','iL2','vC1','vC2');

IL1=eval(DC_OPERATING_POINT.iL1);
IL2=eval(DC_OPERATING_POINT.iL2);
VC1=eval(DC_OPERATING_POINT.vC1);
VC2=eval(DC_OPERATING_POINT.vC2);
VO=eval(subs(averaged_vo,[iL1 iL2 vC1 vC2 io],[IL1 IL2 VC1
VC2 IO]));

disp('Operating point of converter')
disp('--------------------------')
disp('IL1(A)=')
disp(IL1)
disp('IL2(A)=')
```

```
disp(IL2)
disp('VC1(V)=')
disp(VC1)
disp('VC2(V)=')
disp(VC2)
disp('VO(V)=')
disp(VO)
disp('------------------------------')

%Linearizing the averaged equations around the DC operating point.
%We want to obtain the matrix A,B,C and D
%     .
%     x=Ax+Bu
%     y=Cx+Du
%
%where,
%     x=[iL1 iL2 vC1 vC2]'
%     u=[io vg d]'
%Since we used the variables D for steady state duty ratio and
C to
%show the capacitors values we use AA, BB, CC and DD instead of A,
%B, C and D.

% Calculating the matrix A
A11=subs(simplify(diff(averaged_diL1_dt,iL1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A12=subs(simplify(diff(averaged_diL1_dt,iL2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A13=subs(simplify(diff(averaged_diL1_dt,vC1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A14=subs(simplify(diff(averaged_diL1_dt,vC2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);

A21=subs(simplify(diff(averaged_diL2_dt,iL1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A22=subs(simplify(diff(averaged_diL2_dt,iL2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A23=subs(simplify(diff(averaged_diL2_dt,vC1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A24=subs(simplify(diff(averaged_diL2_dt,vC2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);

A31=subs(simplify(diff(averaged_dvC1_dt,iL1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
```

```
A32=subs(simplify(diff(averaged_dvC1_dt,iL2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A33=subs(simplify(diff(averaged_dvC1_dt,vC1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A34=subs(simplify(diff(averaged_dvC1_dt,vC2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);

A41=subs(simplify(diff(averaged_dvC2_dt,iL1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A42=subs(simplify(diff(averaged_dvC2_dt,iL2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A43=subs(simplify(diff(averaged_dvC2_dt,vC1)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);
A44=subs(simplify(diff(averaged_dvC2_dt,vC2)),[iL1 iL2 vC1 vC2 d
io],[IL1 IL2 VC1 VC2 D IO]);

AA=eval([A11 A12 A13 A14;
         A21 A22 A23 A24;
         A31 A32 A33 A34;
         A41 A42 A43 A44]);

% Calculating the matrix B
B11=subs(simplify(diff(averaged_diL1_dt,io)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
B12=subs(simplify(diff(averaged_diL1_dt,vg)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
B13=subs(simplify(diff(averaged_diL1_dt,d)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);

B21=subs(simplify(diff(averaged_diL2_dt,io)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
B22=subs(simplify(diff(averaged_diL2_dt,vg)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
B23=subs(simplify(diff(averaged_diL2_dt,d)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);

B31=subs(simplify(diff(averaged_dvC1_dt,io)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
B32=subs(simplify(diff(averaged_dvC1_dt,vg)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
B33=subs(simplify(diff(averaged_dvC1_dt,d)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);

B41=subs(simplify(diff(averaged_dvC2_dt,io)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
B42=subs(simplify(diff(averaged_dvC2_dt,vg)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
```

```
B43=subs(simplify(diff(averaged_dvC2_dt,d)),[iL1 iL2 vC1 vC2 d
vD io vg],[IL1 IL2 VC1 VC2 D VD IO VG]);

BB=eval([B11 B12 B13;
         B21 B22 B23;
         B31 B32 B33;
         B41 B42 B43]);

% Calculating the matrix C
C11=subs(simplify(diff(averaged_vo,iL1)),[iL1 iL2 vC1 vC2 d io],
[IL1 IL2 VC1 VC2 D IO]);
C12=subs(simplify(diff(averaged_vo,iL2)),[iL1 iL2 vC1 vC2 d io],
[IL1 IL2 VC1 VC2 D IO]);
C13=subs(simplify(diff(averaged_vo,vC1)),[iL1 iL2 vC1 vC2 d io],
[IL1 IL2 VC1 VC2 D IO]);
C14=subs(simplify(diff(averaged_vo,vC2)),[iL1 iL2 vC1 vC2 d io],
[IL1 IL2 VC1 VC2 D IO]);

CC=eval([C11 C12 C13 C14]);

D11=subs(simplify(diff(averaged_vo,io)),[iL1 iL2 vC1 vC2 d vD io
vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
D12=subs(simplify(diff(averaged_vo,vg)),[iL1 iL2 vC1 vC2 d vD io
vg],[IL1 IL2 VC1 VC2 D VD IO VG]);
D13=subs(simplify(diff(averaged_vo,d)),[iL1 iL2 vC1 vC2 d vD io
vg],[IL1 IL2 VC1 VC2 D VD IO VG]);

% Calculating the matrix D
DD=eval([D11 D12 D13]);

% Producing the State Space Model and obtaining the small signal
transfer
% functions
sys=ss(AA,BB,CC,DD);
sys.inputname={'io';'vg';'d'};
sys.outputname={'vo'};

vo_io=tf(sys(1,1)); % Output impedance transfer function vo(s)/io(s)
vo_vg=tf(sys(1,2)); % vo(s)/vg(s)
vo_d=tf(sys(1,3));  % Control-to-output(vo(s)/d(s))

%drawing the Bode diagrams
figure(1)
bode(vo_io),grid minor,title('vo(s)/io(s)')

figure(2)
bode(vo_vg),grid minor,title('vo(s)/vg(s)')

figure(3)
bode(vo_d),grid minor,title('vo(s)/d(s)')
```

After running the code, following results are obtained:

$$\frac{\widetilde{v}_o(s)}{\widetilde{i}_o(s)} = -.093519\frac{\left(s+4.785\times10^4\right)(s+1163)\left(s^2+1396s+6.882\times10^7\right)}{\left(s^2+2239s+4.76\times10^7\right)\left(s^2+2767s+1.026\times10^8\right)}$$
$$\frac{\widetilde{v}_o(s)}{\widetilde{v}_g(s)} = 391.08\frac{\left(s+4.785\times10^4\right)\left(s^2+1473s+7.7\times10^7\right)}{\left(s^2+2239s+4.76\times10^7\right)\left(s^2+2767s+1.026\times10^8\right)}$$
$$\frac{\widetilde{v}_o(s)}{\widetilde{d}(s)} = 43775\frac{\left(s+4.785\times10^4\right)\left(s^2+1371s+7.696\times10^7\right)}{\left(s^2+2239s+4.76\times10^7\right)\left(s^2+2767s+1.026\times10^8\right)} \tag{8.154}$$

Bode diagrams of these transfer functions are shown in Figs. 8.90–8.92.

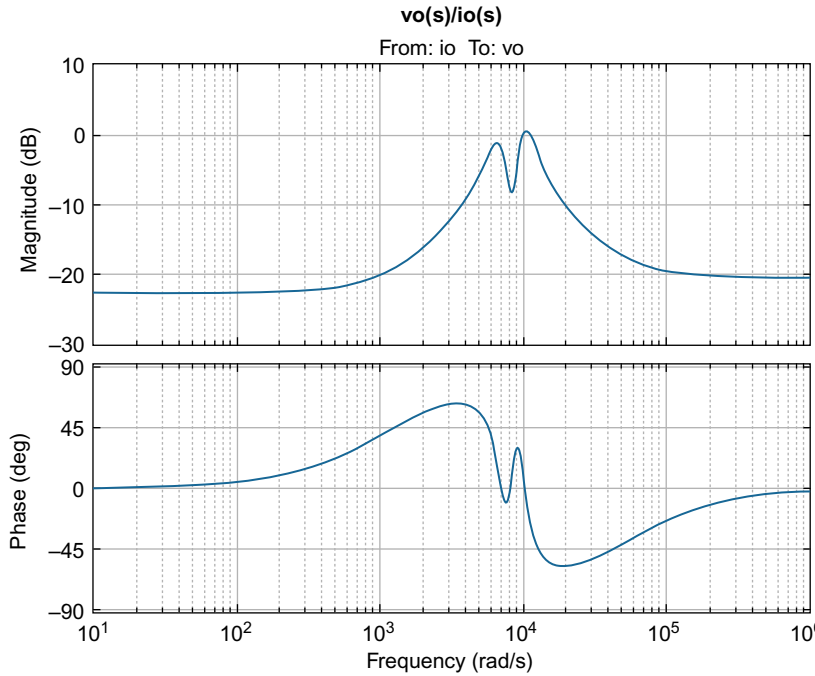



**FIG. 8.90** Bode diagram of output impedance ($\frac{\widetilde{v}_o(s)}{\widetilde{i}_o(s)}$) for the zeta converter with parameters as shown in Table 8.6.

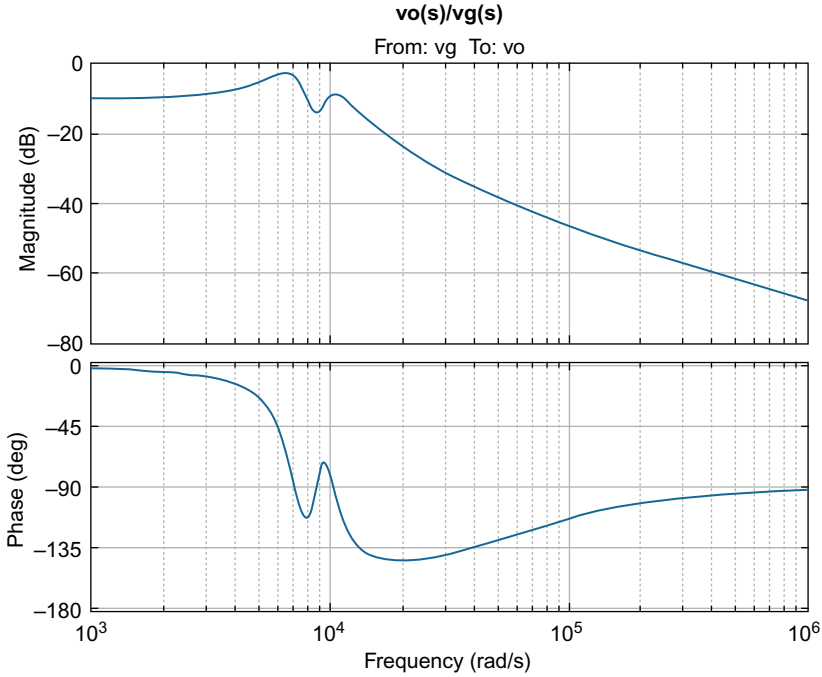



**FIG. 8.91** Bode diagram of audio susceptibility $(\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)})$ for the zeta converter with parameters as shown in Table 8.6.

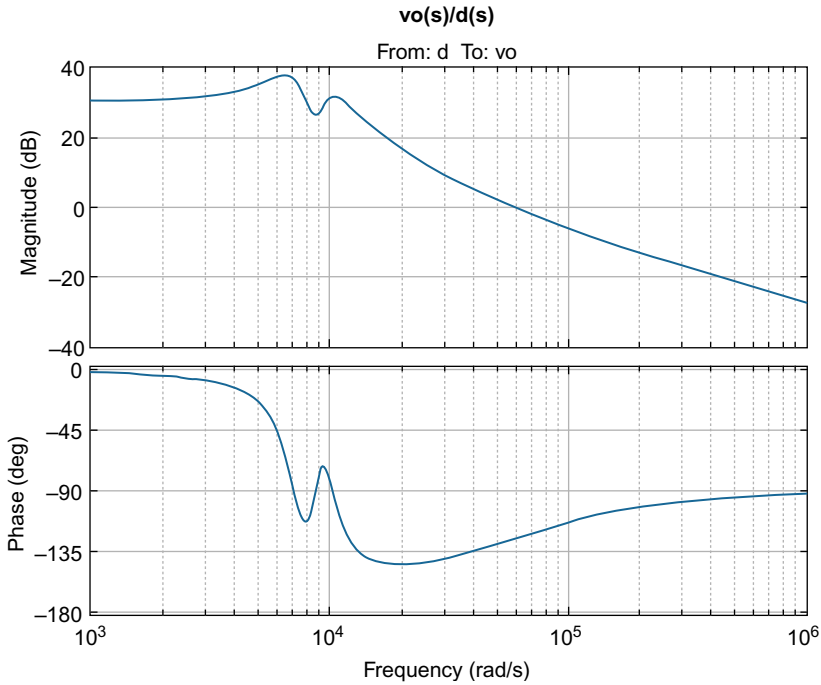



**FIG. 8.92** Bode diagram of control-to-output transfer function $(\frac{\tilde{v}_o(s)}{\tilde{d}(s)})$ for the zeta converter with parameters as shown in Table 8.6.

Fig. 8.93 shows the dynamic block diagram of converter.

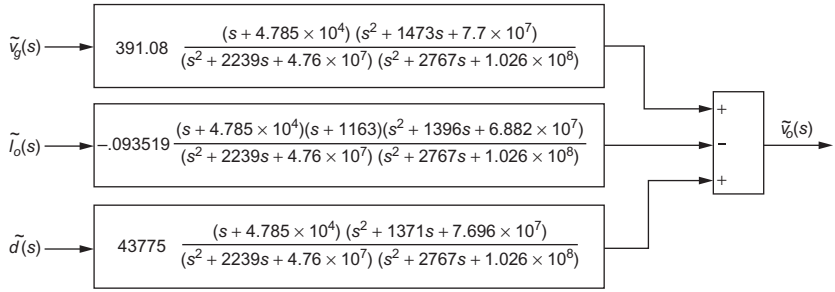



**FIG. 8.93** Dynamical model of zeta converter with parameters given in Table 8.6.

Since the injected test current (io in Figs. 8.88 and 8.89) does not enter the positive end of output voltage, the obtained transfer function for output impedance must be multiplied by −1 in order to be converted to the correct form of output impedance.

PLECS can be used to verify the obtained results. The schematic shown in Fig. 8.94 extracts the output impedance. Extracted output impedance is shown in Fig. 8.95. Obtained result is the same as the one shown in Fig. 8.90 (use cursors to compare different points of two graphs).

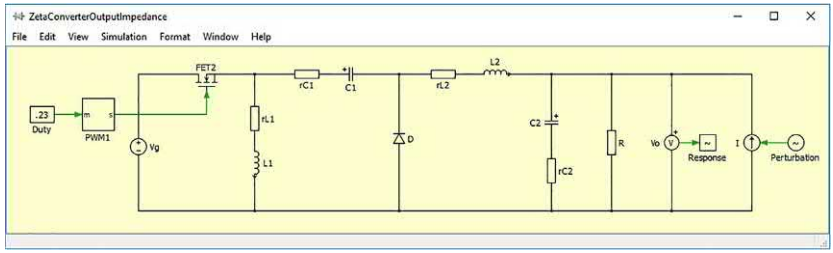



**FIG. 8.94** Simulation diagram to extract the output impedance ($\frac{\tilde{v}_o(s)}{\tilde{i}_o(s)}$).

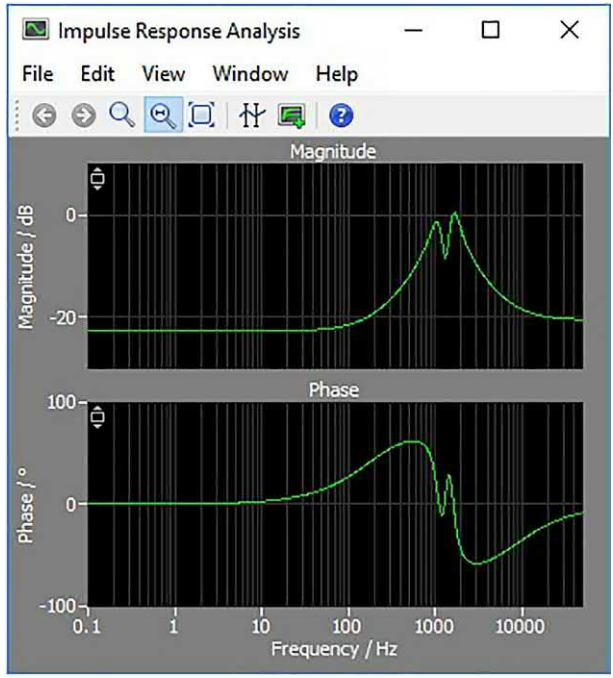



**FIG. 8.95** Output impedance of the studied zeta converter (0.1 Hz-50 kHz range). Note that horizontal axis has the unit of Hz. Horizontal axis of Fig. 8.90 has the unit of $\frac{Rad}{s}$.

Schematics to extract the audio susceptibility ($\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}$) and control-to-output ($\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$) transfer functions are shown in Figs. 8.96 and 8.97, respectively. Analysis results are shown in Figs. 8.98 and 8.99. Obtained results are the same as ones shown in Figs. 8.91 and 8.92.

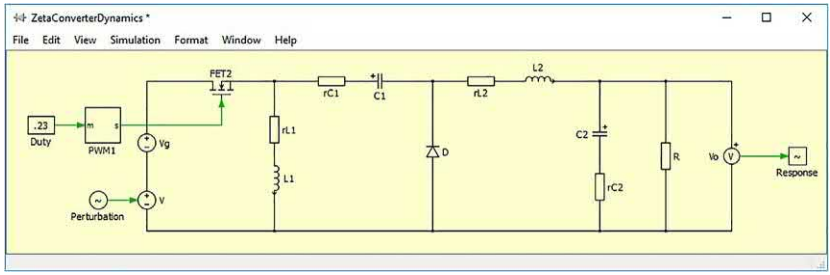



**FIG. 8.96** Simulation diagram to extract the audio susceptibility ($\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}$).

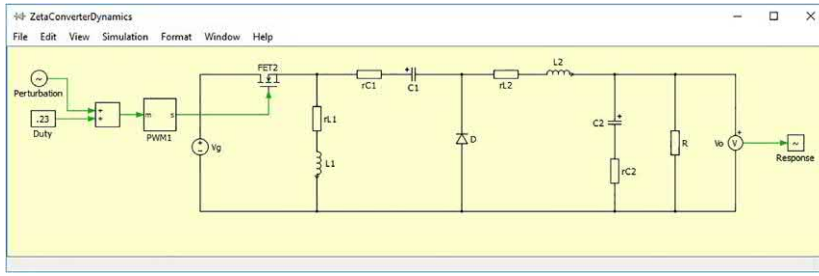



**FIG. 8.97** Simulation diagram to extract the control-to-output ($\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$).

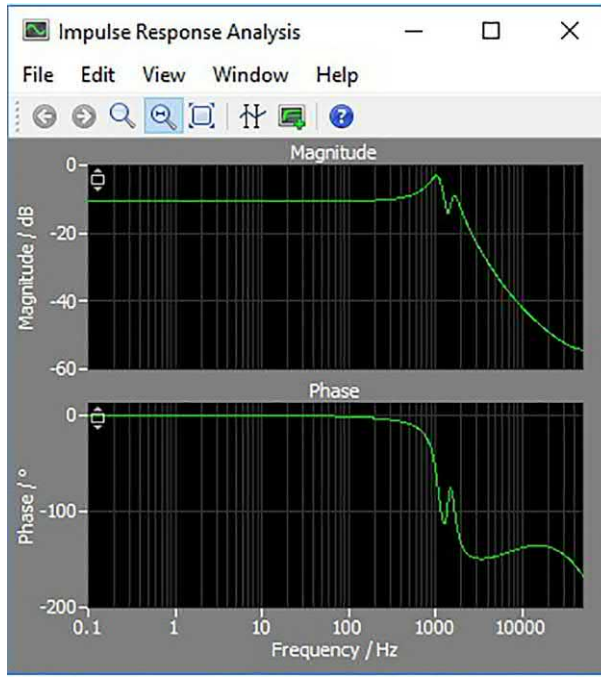



**FIG. 8.98** Bode diagram of audio susceptibility ($\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}$) transfer function for studied zeta converter.

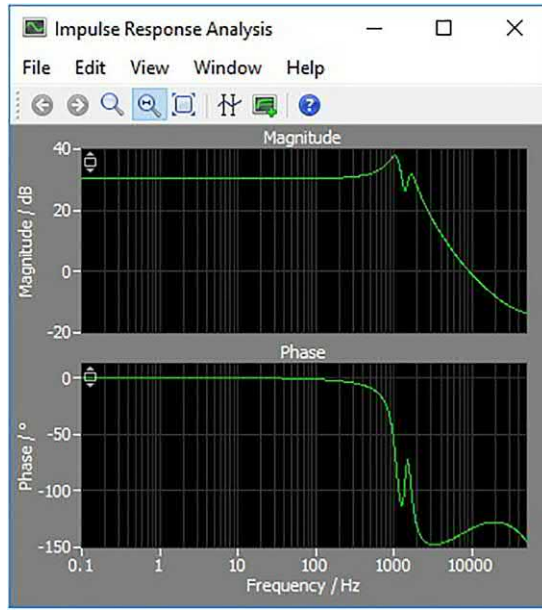



**FIG. 8.99** Bode diagram of control-to-output ($\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$) transfer function for studied zeta converter.

## 8.24 Inverters

Inverters converts DC to AC. They can be found in applications such as adjustable-speed ac motor drives, uninterruptible power supplies (UPS), and running ac appliances from an automobile battery. The concept of THD (which is studied before) is a good tool to quantify the degree of closeness to a purely sinusoidal waveform. As the THD of inverter decreases, the price of inverter increases.

Fig. 8.100 shows the most basic circuit to convert DC to AC.

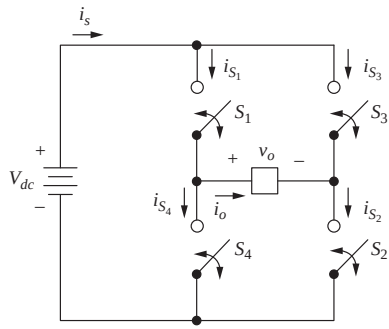



**FIG. 8.100** The H bridge inverter.

The circuit is composed of four switches. When the $S_1$ and $S_2$ are closed, the load voltage is $+V_{dc}$. When the $S_3$ and $S_4$ are closed, the load voltage is $-V_{dc}$. When the $S_1$ and $S_3$ (or $S_2$ and $S_4$) are closed, the load voltage is 0. $S_1$ and $S_4$ should not be closed at the same time (since it produces short circuit), nor should $S_2$ and $S_3$.

The simplest way to produce an AC output is closing the $S_1$ and $S_2$ for duration of $\frac{T}{2}$ seconds and $S_3$ and $S_4$ for the remaining $\frac{T}{2}$ seconds. In this case, the output voltage will be a square wave (Fig. 8.101). Although the output voltage is nonsinusoidal, it may be adequate for some application.

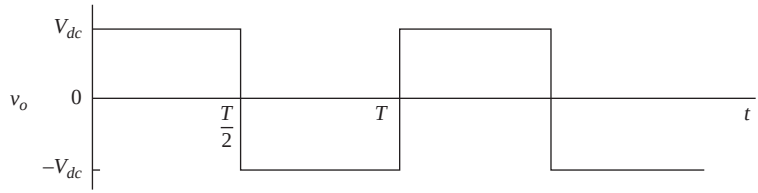



**FIG. 8.101** Production of a square wave with the aid of circuit shown in Fig. 8.100. Fourier series of shown waveform is $v_o(t) = \sum_{n\ odd} \frac{4V_{dc}}{n\pi} \sin(n\omega_0 t)$. Amplitude of fundamental harmonic is $\frac{4V_{dc}}{\pi}$. THD of voltage is $THD_V = \frac{\sqrt{V_{rms}{}^2 - V_{1,rms}{}^2}}{V_{1,rms}} = \frac{\sqrt{V_{dc}{}^2 - \left(\frac{4V_{dc}}{\sqrt{2}\pi}\right)^2}}{\frac{4V_{dc}}{\sqrt{2}\pi}} = 0.483$ or 48.3%.

Nature of load current depends on the type of load. For purely resistive loads, the load current will be a square wave. For *RL* type of loads, the current has more of a sinusoidal quality than the voltage because of filtering property of inductance (Fig. 8.102).

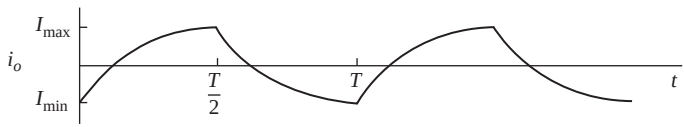



**FIG. 8.102** Load current waveform for RL type of loads. Using basic circuit analysis theory, it is quite easy to show that $I_{max} = -I_{min} = \frac{V_{dc}}{R}\left(\frac{1-e^{-\frac{T}{2\tau}}}{1+e^{-\frac{T}{2\tau}}}\right).\tau = \frac{L}{R}$.

When the load is *RL*, the switches must be bidirectional (Fig. 8.103A). Fig 8.103B shows which pair carries the load current in each instant of time.

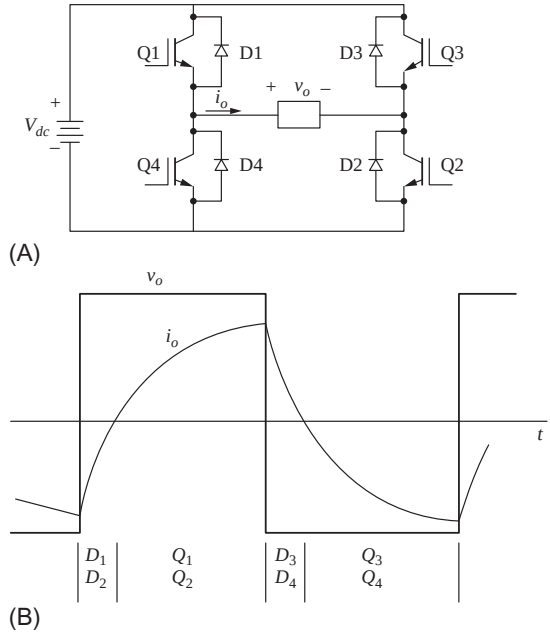



**FIG. 8.103** (A) The switches must be bidirectional, i.e., carry current in both directions, when the load is *RL*. (B) Load current in each instant of time is carried by two switches.

The amplitude of fundamental harmonic of square wave shown in Fig. 8.101 is constant and is determined by the input DC source ($V_1 = \frac{4V_{dc}}{\pi}$). The circuit is capable of producing the 0 V in its output. This can provide a way to control the amplitude of fundamental harmonic of output voltage (Fig. 8.104).

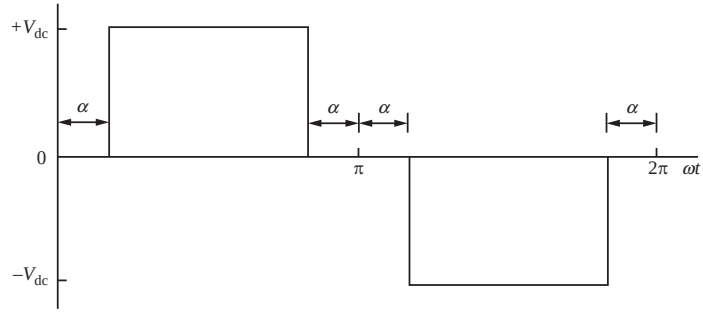



**FIG. 8.104** Output voltage can be controlled by adjusting the interval $\alpha$ on each side of the pulse where the output is zero. Fourier series of shown waveforms is $v_o(t) = \sum_{n=1,3,5,\ldots} \left(\frac{4V_{dc}}{n\pi}\right) \cos(n\alpha) \sin(n\omega_0 t)$. RMS of shown waveform is $V_{rms} = V_{dc}\sqrt{1 - \frac{2\alpha}{\pi}}$.

Harmonic content can also be controlled by adjusting $\alpha$. For instance for $\alpha = 30°$, third harmonic will be zero. In this case, the amplitude of fundamental harmonic will be $V_1 = \frac{4V_{dc}}{\pi}\cos(30°) = 1.1V_{dc}$. $n$th harmonic can be eliminated by selection of $\alpha = \frac{90}{n}$.

### 8.24.1 Series H bridge inverters

The THD of output voltage of inverter can be decreased by increasing the number of voltage levels, which the inverter can produce. The H bridge inverters can be connected in series in order to produce more output voltage levels. For instance, Fig. 8.105 shows two H bridge inverters, which are connected in series. Each H bridge inverter produces three different voltage levels ($-V_{dc}$, $0, +V_{dc}$). The output voltage levels of inverter, which is composed of two series H bridge inverters, are $-2V_{dc}, -V_{dc}, 0, +V_{dc}, +2V_{dc}$. So, the number of output voltage levels increased to five (Fig. 8.106). If we connect five H bridge inverters together, the number of output voltage levels increases to eleven ($-5V_{dc}, -4V_{dc}, -3V_{dc}, -2V_{dc}, -V_{dc}, \quad 0, +V_{dc}, +2V_{dc}, +3V_{dc}, +4V_{dc}, +5V_{dc}$). Note that each H bridge inverter has its own independent DC source. This is a disadvantage for series of H bridge inverters.

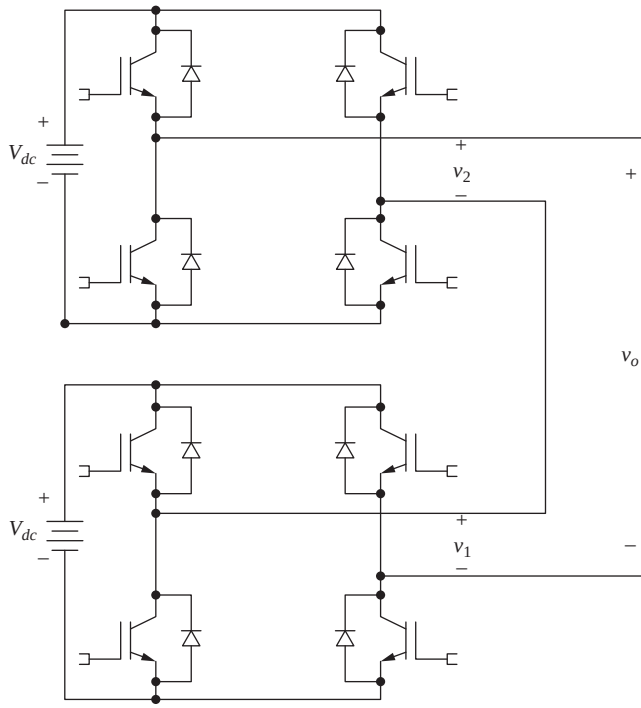



**FIG. 8.105** A multilevel inverter composed of series connection of two H bridge inverters.

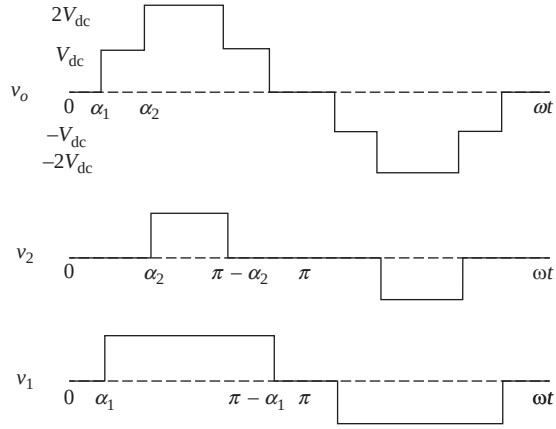



**FIG. 8.106** Waveforms of circuit shown in Fig. 8.105. Fourier series of output voltage is $v_o(t) = \frac{4V_{dc}}{\pi} \sum_{n=1,3,5,7,\ldots} [\cos(n\alpha_1) + \cos(n\alpha_2)] \frac{\sin(n\omega_0 t)}{n}$.

### 8.24.2 Diode-clamped multilevel inverters

Fig. 8.107 shows a diode-clamped multilevel inverter. Note that this circuit uses only one DC source.

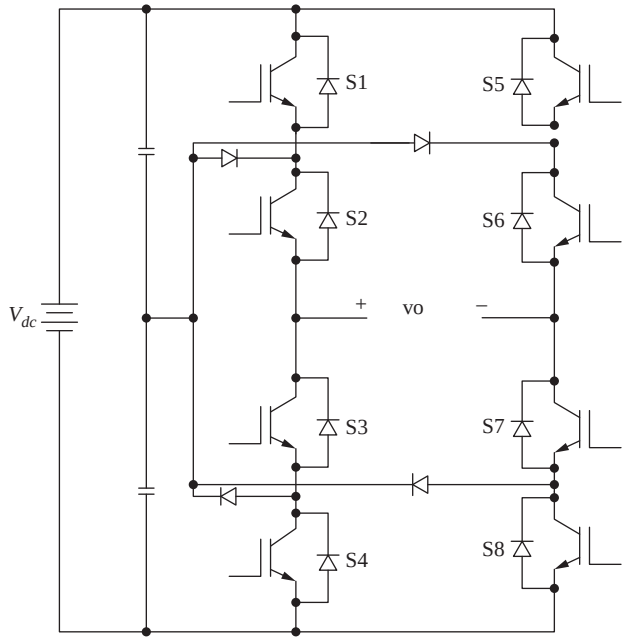



**FIG. 8.107** A diode-clamped multilevel inverter implemented with IGBT. The output voltage ($v_o = v_1 - v_2$) can have five different levels.

The output voltage of this circuit can have the $-V_{dc}$, $-\frac{V_{dc}}{2}$, 0, $+\frac{V_{dc}}{2}$, and $+V_{dc}$ levels. We will show how these levels are produced. For the analysis, consider only the left half of the bridge, as shown in Fig. 8.108.

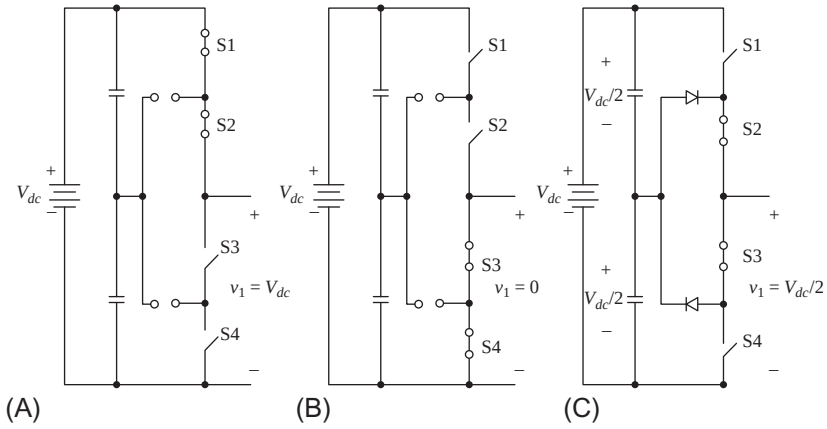



**FIG. 8.108** Analysis of one-half of circuit shown in Fig. 8.107 for (A) $v_1 = V_{dc}$, (B) $v_1 = 0$, (C) $v_1 = \frac{V_{dc}}{2}$.

When $S_1$ and $S_2$ are closed and $S_3$ and $S_4$ are open (Fig. 8.107A), $v_1 = V_{dc}$. The diodes are off for this condition. When $S_1$ and $S_2$ are open and $S_3$ and $S_4$ are closed (Fig. 8.107B), $v_1 = 0$. The diodes are off in this condition also. When $S_1$ and $S_3$ are closed and $S_2$ and $S_4$ are open (Fig. 8.107C), $v_1 = \frac{V_{dc}}{2}$.

Using a similar analysis, the right half of the circuit can also produce the voltages $V_{dc}$, 0, and $\frac{V_{dc}}{2}$. The output voltage is the difference of the voltages between each half-bridge ($v_o = v_1 - v_2$), resulting in the five levels

$$v_o \in \left\{ -V_{dc}, -\frac{V_{dc}}{2}, 0, +\frac{V_{dc}}{2}, +V_{dc} \right\}$$

More output voltage levels are achieved with additional capacitors and switches. Fig. 8.109 shows the dc source divided across three series capacitors (the voltage across each capacitor is $\frac{V_{dc}}{3}$). The output voltage of this circuit can have seven different levels

$$v_o \in \left\{ -V_{dc}, -\frac{2}{3}V_{dc}, -\frac{1}{3}V_{dc}, 0, +\frac{1}{3}V_{dc}, +\frac{2}{3}V_{dc}, +V_{dc} \right\}$$

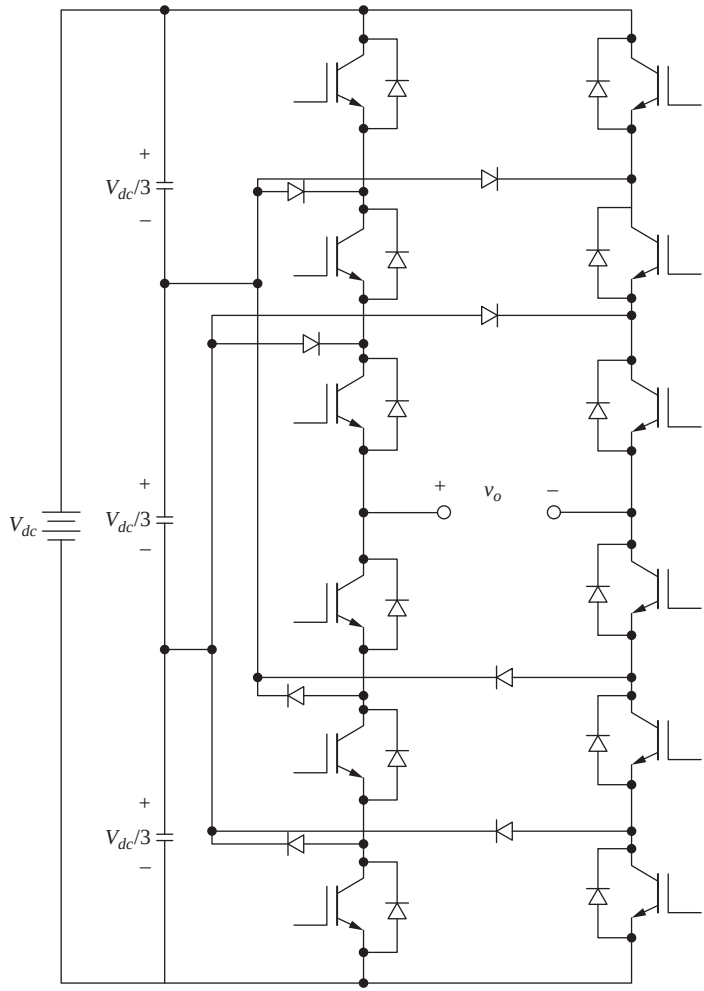



**FIG. 8.109** A diode-clamped multilevel inverter, which produces seven output voltage levels.

## 8.25 Heatsink

Electronic switches dissipate some energy (due to switching and conduction losses) in the form of heat. The produced heat must be removed from the switch in order to keep the internal temperature of device below its maximum.

The produced heat can be removed from the switch more easily with the aid of heatsinks (Figs. 8.110 and 8.111). When the amount of produced heat energy is considerable (for instance, in the inverters, which are used for induction heating), water cooling is used (Fig. 8.112).

**FIG. 8.110** A typical heatsink.

**FIG. 8.111** A heatsink equipped with a fan.

**FIG. 8.112** When the amount of produced heat in the switch is considerable, water cooling is used.

The heat transfer problem is quite a complex problem. Exact solution of heat transfer problem requires finite element softwares. However, for the purpose of power electronics converters, there are simplified estimations, which can be used to get rid of complex heat transfer mathematics.

The heat can be transferred in three ways:

1. Conduction
2. Convection
3. Radiation

We assume that produced heat in the switch is transferred to the ambient using the conduction only. This is simplifying assumption and in real world, the produced heat is transferred using convection and radiations as well.

In general, the temperature difference between two points is a function of thermal power and thermal resistance. Thermal resistance is defined as

$$R_\theta = \frac{T_1 - T_2}{P} \tag{8.155}$$

where $R_\theta$ = thermal resistance ($°C/W$), $T_1 - T_2$ = temperature difference ($°C$), and $P$ = thermal power ($W$).

Fig. 8.113 shows the electric circuit equivalent of the equation. The thermal power is modeled as a current source, thermal resistance is modeled as a electrical resistance, and temperature difference is modeled as the voltage difference.

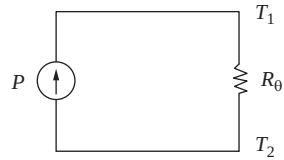



**FIG. 8.113** An electric circuit equivalent of Eq. (8.155).

The internal temperature of an electronic switching device is referred to as the junction temperature. Although devices such as MOSFETs do not have a junction per se when conducting, the term is still used. In an electronic device without a heat sink, the junction temperature is determined by thermal power and the junction-to-ambient thermal resistance $R_{\theta,JA}$. The ambient temperature is that of the air in contact with the case. The $R_{\theta,JA}$ can be found in the datasheet of MOSFET.

For instance, assume that $R_{\theta,JA} = 62\,°\text{C/W}$, ambient temperature is $40\,°\text{C}$, and the maximum junction temperature ($T_{J,max}$) is $175\,°\text{C}$. The maximum power that MOSFET can absorb is 2.177 $W$ since (see Fig. 8.114).

$$P = \frac{T_1 - T_2}{R_\theta} = \frac{T_J - T_A}{R_{\theta,JA}} = \frac{175 - 40}{62} = 2.177\,W \tag{8.156}$$

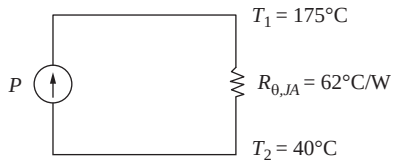



**FIG. 8.114** Electric circuit equivalent of heat transfer in a MOSFET without heatsink. The temperature of junction is allowed to reach its maximum.

Assume that we wish the junction temperature not to increase above 150 °C for increased reliablity. In this case, the maximum power that MOSFET can absorb decreases to 1.77 *W* since (see Fig. 8.115)

$$P = \frac{T_1 - T_2}{R_\theta} = \frac{T_J - T_A}{R_{\theta,JA}} = \frac{150 - 40}{62} = 1.77\,W \tag{8.157}$$

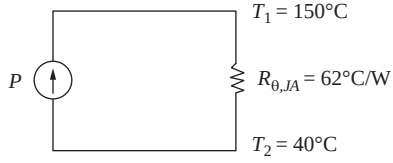



**FIG. 8.115** Electric circuit equivalent of heat transfer in a MOSFET without heatsink. The temperature of junction is limited to 150 °C.

So, a device without any heatsink can dissipate a little power. Generally, a heatsink is required to dissipate the produced heat safely. A heatsink reduces the thermal resistance from the junction to ambient. The heatsinks are produced in all sizes. Generally, the heatsinks are produced from aluminum (Fig. 8.116).

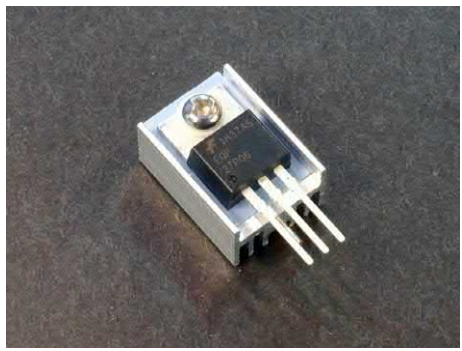


**FIG. 8.116** A MOSFET switch with heatsink. The case of the device is often attached to the heat sink with a thermal compound to fill the small voids between the imperfect surfaces of the case and sink.

When the switch is mounted on heatsink, the thermal power flows from the junction to the case, from the case to the heat sink, and then from the heat sink to ambient. The corresponding thermal resistances are $R_{\theta,JC}$, $R_{\theta,CS}$, and $R_{\theta,SA}$ as shown in Fig. 8.117. Value of $R_{\theta,JC}$, $R_{\theta,CS}$ can be found in the switch (MOSFET, IGBT, …) datasheet. $R_{\theta,SA}$ can be found in the heatsink datasheet.

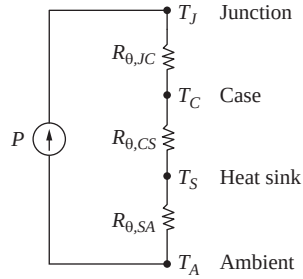



**FIG. 8.117** The electrical-equivalent circuit for a switch mounted on a heatsink.

The voltage of different nodes of Fig. 8.117 (which represents temperatures) can be calculated easily:

$$\begin{aligned} T_S &= P \times R_{\theta,SA} + T_A \\ T_C &= P \times R_{\theta,CS} + T_S = P \times (R_{\theta,CS} + R_{\theta,SA}) + T_A \\ T_J &= P \times R_{\theta,JC} + T_C = P \times (R_{\theta,JC} + R_{\theta,CS} + R_{\theta,SA}) + T_A \end{aligned} \tag{8.158}$$

For instance, assume that $R_{\theta,JC} = 1.87\,^\circ$C/W, $R_{\theta,CS} = 0.5\,^\circ$C/W, $R_{\theta,SA} = 7.2\,^\circ$C/W, $T_{Ambient} = 40\,^\circ$C, and $T_{J,max} = 150\,^\circ$C. The equivalent electric circuit shown in Fig. 8.118 can be drawn for this case.

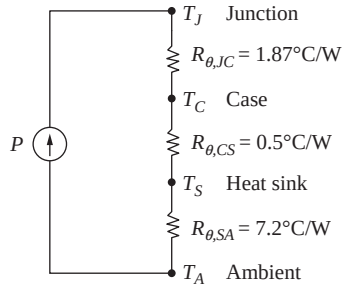



**FIG. 8.118** Equivalent electric circuit for the studied example.

The maximum power, which can be absorbed by the switch is:

$$P = \frac{T_J - T_A}{R_{\theta,JC} + R_{\theta,CS} + R_{\theta,SA}} = \frac{150 - 40}{1.87 + 0.5 + 7.2} = \frac{110}{9.57} = 11.5\,W \tag{8.159}$$

So, with the aid of a heatsink with thermal resistance of $R_{\theta,SA} = 7.2\,^{\circ}\text{C/W}$, maximum of 11.5 $W$ is dissipatable. Assume that the power to be dissipated is 15 $W$. In this case, the junction temperature is

$$T_J = P(R_{\theta,JC} + R_{\theta,CS} + R_{\theta,SA}) + T_A = 15(1.87 + 0.5 + 7.2) + 40 = 184°C \tag{8.160}$$

So, the switch will burn out since the junction temperature is above the maximum allowed temperature. In order to dissipate 15 W safely, a heatsink with thermal resistance of $R_{\theta,SA} = 4.96\,^{\circ}\text{C/W}$ is required:

$$R_{\theta,SA} = \frac{T_J - T_A}{P} - R_{\theta,JC} - R_{\theta,CS} = \frac{150 - 40}{15} - 1.87 - 0.5 = 4.96°\text{C/W} \tag{8.161}$$

## Further reading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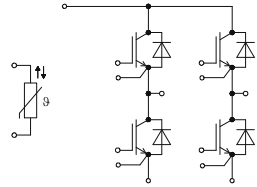
# Appendix A

Technische Information / technical information

IGBT-Module
IGBT-modules

## F4-50R06W1E3

EasyPACK Modul mit Trench/Feldstopp IGBT3 und Emitter Controlled 3 Diode und NTC
EasyPACK module with Trench/Fieldstop IGBT3 and Emitter Controlled 3 diode and NTC

$V_{CES}$ = 600V
$I_{C\ nom}$ = 50A / $I_{CRM}$ = 100A

**Typische Anwendungen**
- Hilfsumrichter
- Induktives Erwärmen und Schweißen
- Servoumrichter
- USV-Systeme

**Typical Applications**
- Auxiliary Inverters
- Inductive Heating and Welding
- Servo Drives
- UPS Systems

**Elektrische Eigenschaften**
- Niederinduktives Design
- Niedrige Schaltverluste
- Trench IGBT 3
- niedriges $V_{CEsat}$

**Electrical Features**
- Low inductive design
- Low Switching Losses
- Trench IGBT 3
- Low $V_{CEsat}$

**Mechanische Eigenschaften**
- $Al_2O_3$ Substrat für kleinen thermischen Widerstand
- Kompaktes Design
- Lötverbindungs Technologie
- Robuste Montage durch integrierte Befestigungsklammern

**Mechanical Features**
- $Al_2O_3$ Substrate for Low Thermal Resistance
- Compact Design
- Solder Contact Technology
- Rugged mounting due to integrated mounting clamps

### Module Label Code

**Barcode Code 128**

00000123456000000000000

**DMX - Code**

| Content of the Code | Digit |
|---|---|
| Module Serial Number | 1 - 5 |
| Module Material Number | 6 - 11 |
| Production Order Number | 12 - 19 |
| Datecode (Production Year) | 20 - 21 |
| Datecode (Production Week) | 22 - 23 |

| | | |
|---|---|---|
| prepared by: DK | date of publication: 2010-01-06 | material no: 28311 |
| approved by: MB | revision: 3.0 | UL approved (E83335) |

Technische Information / technical information

IGBT-Module
IGBT-modules

# F4-50R06W1E3

## IGBT-Wechselrichter / IGBT-inverter

### Höchstzulässige Werte / maximum rated values

| | | | | |
|---|---|---|---|---|
| Kollektor-Emitter-Sperrspannung<br>collector-emitter voltage | $T_{vj}$ = 25°C | $V_{CES}$ | 600 | V |
| Kollektor-Dauergleichstrom<br>DC-collector current | $T_C$ = 80°C, $T_{vj}$ = 175°C<br>$T_C$ = 25°C, $T_{vj}$ = 175°C | $I_{C\ nom}$<br>$I_C$ | 50<br>75 | A<br>A |
| Periodischer Kollektor Spitzenstrom<br>repetitive peak collector current | $t_P$ = 1 ms | $I_{CRM}$ | 100 | A |
| Gesamt-Verlustleistung<br>total power dissipation | $T_C$ = 25°C, $T_{vj}$ = 175°C | $P_{tot}$ | 225 | W |
| Gate-Emitter-Spitzenspannung<br>gate-emitter peak voltage | | $V_{GES}$ | +/-20 | V |

### Charakteristische Werte / characteristic values

| | | | min. | typ. | max. | |
|---|---|---|---|---|---|---|
| Kollektor-Emitter Sättigungsspannung<br>collector-emitter saturation voltage | $I_C$ = 50 A, $V_{GE}$ = 15 V, $T_{vj}$ = 25°C<br>$I_C$ = 50 A, $V_{GE}$ = 15 V, $T_{vj}$ = 125°C<br>$I_C$ = 50 A, $V_{GE}$ = 15 V, $T_{vj}$ = 150°C | $V_{CE\ sat}$ | | 1,45<br>1,60<br>1,70 | 1,90 | V<br>V<br>V |
| Gate-Schwellenspannung<br>gate threshold voltage | $I_C$ = 0,80 mA, $V_{CE}$ = $V_{GE}$, $T_{vj}$ = 25°C | $V_{GEth}$ | 4,9 | 5,8 | 6,5 | V |
| Gateladung<br>gate charge | $V_{GE}$ = -15 V ... +15 V | $Q_G$ | | 0,50 | | µC |
| Interner Gatewiderstand<br>internal gate resistor | $T_{vj}$ = 25°C | $R_{Gint}$ | | 0,0 | | Ω |
| Eingangskapazität<br>input capacitance | f = 1 MHz, $T_{vj}$ = 25°C, $V_{CE}$ = 25 V, $V_{GE}$ = 0 V | $C_{ies}$ | | 3,10 | | nF |
| Rückwirkungskapazität<br>reverse transfer capacitance | f = 1 MHz, $T_{vj}$ = 25°C, $V_{CE}$ = 25 V, $V_{GE}$ = 0 V | $C_{res}$ | | 0,095 | | nF |
| Kollektor-Emitter Reststrom<br>collector-emitter cut-off current | $V_{CE}$ = 600 V, $V_{GE}$ = 0 V, $T_{vj}$ = 25°C | $I_{CES}$ | | | 1,0 | mA |
| Gate-Emitter Reststrom<br>gate-emitter leakage current | $V_{CE}$ = 0 V, $V_{GE}$ = 20 V, $T_{vj}$ = 25°C | $I_{GES}$ | | | 400 | nA |
| Einschaltverzögerungszeit (ind. Last)<br>turn-on delay time (inductive load) | $I_C$ = 50 A, $V_{CE}$ = 300 V, $T_{vj}$ = 25°C<br>$V_{GE}$ = ±15 V, $T_{vj}$ = 125°C<br>$R_{Gon}$ = 8,2 Ω, $T_{vj}$ = 150°C | $t_{d\ on}$ | | 0,023<br>0,023<br>0,023 | | µs<br>µs<br>µs |
| Anstiegszeit (induktive Last)<br>rise time (inductive load) | $I_C$ = 50 A, $V_{CE}$ = 300 V, $T_{vj}$ = 25°C<br>$V_{GE}$ = ±15 V, $T_{vj}$ = 125°C<br>$R_{Gon}$ = 8,2 Ω, $T_{vj}$ = 150°C | $t_r$ | | 0,015<br>0,018<br>0,02 | | µs<br>µs<br>µs |
| Abschaltverzögerungszeit (ind. Last)<br>turn-off delay time (inductive load) | $I_C$ = 50 A, $V_{CE}$ = 300 V, $T_{vj}$ = 25°C<br>$V_{GE}$ = ±15 V, $T_{vj}$ = 125°C<br>$R_{Goff}$ = 8,2 Ω, $T_{vj}$ = 150°C | $t_{d\ off}$ | | 0,20<br>0,22<br>0,23 | | µs<br>µs<br>µs |
| Fallzeit (induktive Last)<br>fall time (inductive load) | $I_C$ = 50 A, $V_{CE}$ = 300 V, $T_{vj}$ = 25°C<br>$V_{GE}$ = ±15 V, $T_{vj}$ = 125°C<br>$R_{Goff}$ = 8,2 Ω, $T_{vj}$ = 150°C | $t_f$ | | 0,10<br>0,13<br>0,14 | | µs<br>µs<br>µs |
| Einschaltverlustenergie pro Puls<br>turn-on energy loss per pulse | $I_C$ = 50 A, $V_{CE}$ = 300 V, $L_S$ = 45 nH, $T_{vj}$ = 25°C<br>$V_{GE}$ = ±15 V, di/dt = 2600 A/µs ($T_{vj}$=150°C), $T_{vj}$ = 125°C<br>$R_{Gon}$ = 8,2 Ω, $T_{vj}$ = 150°C | $E_{on}$ | | 0,46<br>0,56<br>0,65 | | mJ<br>mJ<br>mJ |
| Abschaltverlustenergie pro Puls<br>turn-off energy loss per pulse | $I_C$ = 50 A, $V_{CE}$ = 300 V, $L_S$ = 45 nH, $T_{vj}$ = 25°C<br>$V_{GE}$ = ±15 V, du/dt = 4200 V/µs ($T_{vj}$=150°C), $T_{vj}$ = 125°C<br>$R_{Goff}$ = 8,2 Ω, $T_{vj}$ = 150°C | $E_{off}$ | | 1,20<br>1,50<br>1,60 | | mJ<br>mJ<br>mJ |
| Kurzschlussverhalten<br>SC data | $V_{GE}$ ≤ 15 V, $V_{CC}$ = 360 V, $t_P$ ≤ 8 µs, $T_{vj}$ = 25°C<br>$V_{CEmax}$ = $V_{CES}$ -$L_{sCE}$ ·di/dt, $t_P$ ≤ 6 µs, $T_{vj}$ = 150°C | $I_{SC}$ | | 350<br>250 | | A<br>A |
| Innerer Wärmewiderstand<br>thermal resistance, junction to case | pro IGBT / per IGBT | $R_{thJC}$ | | 0,60 | 0,66 | K/W |
| Übergangs-Wärmewiderstand<br>thermal resistance, case to heatsink | pro IGBT / per IGBT<br>$\lambda_{Paste}$ = 1 W/(m·K) / $\lambda_{grease}$ = 1 W/(m·K) | $R_{thCH}$ | | 0,70 | | K/W |

| | |
|---|---|
| prepared by: DK | date of publication: 2010-01-06 |
| approved by: MB | revision: 3.0 |

Technische Information / technical information

IGBT-Module
IGBT-modules

# F4-50R06W1E3

## Diode-Wechselrichter / diode-inverter

### Höchstzulässige Werte / maximum rated values

| | | | | | |
|---|---|---|---|---|---|
| Periodische Spitzensperrspannung<br>repetitive peak reverse voltage | $T_{vj}$ = 25°C | $V_{RRM}$ | | 600 | V |
| Dauergleichstrom<br>DC forward current | | $I_F$ | | 50 | A |
| Periodischer Spitzenstrom<br>repetitive peak forward current | $t_P$ = 1 ms | $I_{FRM}$ | | 100 | A |
| Grenzlastintegral<br>I²t - value | $V_R$ = 0 V, $t_P$ = 10 ms, $T_{vj}$ = 125°C<br>$V_R$ = 0 V, $t_P$ = 10 ms, $T_{vj}$ = 150°C | I²t | | 370<br>330 | A²s<br>A²s |

### Charakteristische Werte / characteristic values

| | | | | min. | typ. | max. | |
|---|---|---|---|---|---|---|---|
| Durchlassspannung<br>forward voltage | $I_F$ = 50 A, $V_{GE}$ = 0 V<br>$I_F$ = 50 A, $V_{GE}$ = 0 V<br>$I_F$ = 50 A, $V_{GE}$ = 0 V | $T_{vj}$ = 25°C<br>$T_{vj}$ = 125°C<br>$T_{vj}$ = 150°C | $V_F$ | | 1,55<br>1,50<br>1,45 | 1,95 | V<br>V<br>V |
| Rückstromspitze<br>peak reverse recovery current | $I_F$ = 50 A, - $di_F/dt$ = 2600 A/µs ($T_{vj}$=150°C)<br>$V_R$ = 300 V<br>$V_{GE}$ = -15 V | $T_{vj}$ = 25°C<br>$T_{vj}$ = 125°C<br>$T_{vj}$ = 150°C | $I_{RM}$ | | 60,0<br>68,0<br>72,0 | | A<br>A<br>A |
| Sperrverzögerungsladung<br>recovered charge | $I_F$ = 50 A, - $di_F/dt$ = 2600 A/µs ($T_{vj}$=150°C)<br>$V_R$ = 300 V<br>$V_{GE}$ = -15 V | $T_{vj}$ = 25°C<br>$T_{vj}$ = 125°C<br>$T_{vj}$ = 150°C | $Q_r$ | | 2,10<br>3,40<br>3,95 | | µC<br>µC<br>µC |
| Abschaltenergie pro Puls<br>reverse recovery energy | $I_F$ = 50 A, - $di_F/dt$ = 2600 A/µs ($T_{vj}$=150°C)<br>$V_R$ = 300 V<br>$V_{GE}$ = -15 V | $T_{vj}$ = 25°C<br>$T_{vj}$ = 125°C<br>$T_{vj}$ = 150°C | $E_{rec}$ | | 0,42<br>0,71<br>0,83 | | mJ<br>mJ<br>mJ |
| Innerer Wärmewiderstand<br>thermal resistance, junction to case | pro Diode / per diode | | $R_{thJC}$ | | 0,80 | 0,90 | K/W |
| Übergangs-Wärmewiderstand<br>thermal resistance, case to heatsink | pro Diode / per diode<br>$\lambda_{Paste}$ = 1 W/(m·K) / $\lambda_{grease}$ = 1 W/(m·K) | | $R_{thCH}$ | | 0,70 | | K/W |

## NTC-Widerstand / NTC-thermistor

### Charakteristische Werte / characteristic values

| | | | min. | typ. | max. | |
|---|---|---|---|---|---|---|
| Nennwiderstand<br>rated resistance | $T_C$ = 25°C | $R_{25}$ | | 5,00 | | kΩ |
| Abweichung von $R_{100}$<br>deviation of $R_{100}$ | $T_C$ = 100°C, $R_{100}$ = 493 Ω | $\Delta R/R$ | -5 | | 5 | % |
| Verlustleistung<br>power dissipation | $T_C$ = 25°C | $P_{25}$ | | | 20,0 | mW |
| B-Wert<br>B-value | $R_2 = R_{25} \exp [B_{25/50}(1/T_2 - 1/(298,15\ K))]$ | $B_{25/50}$ | | 3375 | | K |
| B-Wert<br>B-value | $R_2 = R_{25} \exp [B_{25/80}(1/T_2 - 1/(298,15\ K))]$ | $B_{25/80}$ | | 3411 | | K |
| B-Wert<br>B-value | $R_2 = R_{25} \exp [B_{25/100}(1/T_2 - 1/(298,15\ K))]$ | $B_{25/100}$ | | 3433 | | K |

Angaben gemäß gültiger Application Note.
Specification according to the valid application note.

| | |
|---|---|
| prepared by: DK | date of publication: 2010-01-06 |
| approved by: MB | revision: 3.0 |

Technische Information / technical information

IGBT-Module
IGBT-modules

F4-50R06W1E3

## Modul / module

| | | | | | | |
|---|---|---|---|---|---|---|
| Isolations-Prüfspannung<br>insulation test voltage | RMS, f = 50 Hz, t = 1 min. | $V_{ISOL}$ | | 2,5 | | kV |
| Material für innere Isolation<br>material for internal insulation | | | | $Al_2O_3$ | | |
| Kriechstrecke<br>creepage distance | Kontakt - Kühlkörper / terminal to heatsink<br>Kontakt - Kontakt / terminal to terminal | | | 11,5<br>6,3 | | mm |
| Luftstrecke<br>clearance distance | Kontakt - Kühlkörper / terminal to heatsink<br>Kontakt - Kontakt / terminal to terminal | | | 10,0<br>5,0 | | mm |
| Vergleichszahl der Kriechwegbildung<br>comparative tracking index | | CTI | | > 200 | | |
| | | | min. | typ. | max. | |
| Modulinduktivität<br>stray inductance module | | $L_{sCE}$ | | 20 | | nH |
| Modulleitungswiderstand,<br>Anschlüsse - Chip<br>module lead resistance,<br>terminals - chip | $T_C$ = 25°C, pro Schalter / per switch | $R_{CC'+EE'}$ | | 8,00 | | mΩ |
| Höchstzulässige Sperrschichttemperatur<br>maximum junction temperature | Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper | $T_{vj\ max}$ | | | 175 | °C |
| Temperatur im Schaltbetrieb<br>temperature under switching conditions | Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper | $T_{vj\ op}$ | -40 | | 150 | °C |
| Lagertemperatur<br>storage temperature | | $T_{stg}$ | -40 | | 125 | °C |
| Anpresskraft für mech. Bef. pro Feder<br>mountig force per clamp | | F | 20 | - | 50 | N |
| Gewicht<br>weight | | G | | 24 | | g |

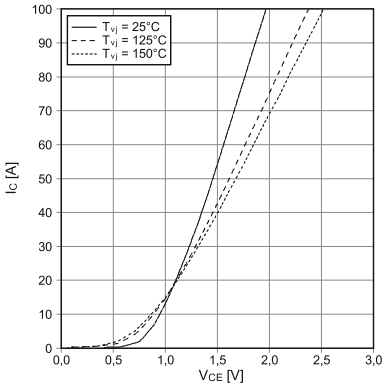
Der Strom im Dauerbetrieb ist auf 30 A effektiv pro Anschlusspin begrenzt.
The current under continuous operation is limited to 30 A rms per connector pin.

Technische Information / technical information

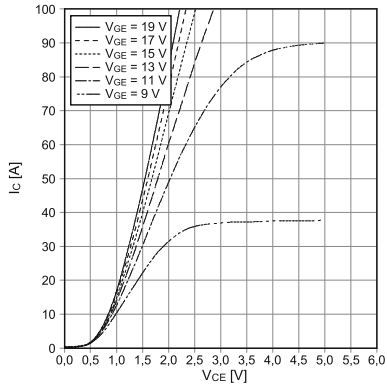
IGBT-Module
IGBT-modules

# F4-50R06W1E3

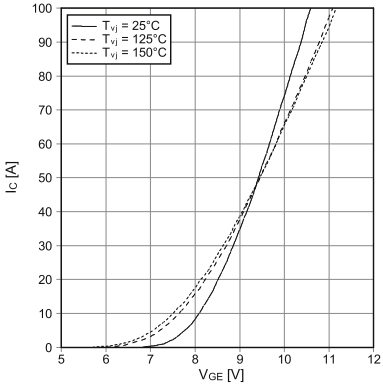
**Ausgangskennlinie IGBT-Wechselr. (typisch)**
**output characteristic IGBT-inverter (typical)**
**$I_C = f(V_{CE})$**
**$V_{GE}$ = 15 V**



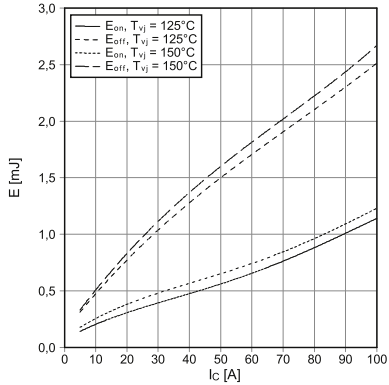

**Ausgangskennlinienfeld IGBT-Wechselr. (typisch)**
**output characteristic IGBT-inverter (typical)**
**$I_C = f(V_{CE})$**
**$T_{vj}$ = 150°C**




**Übertragungscharakteristik IGBT-Wechselr. (typisch)**
**transfer characteristic IGBT-inverter (typical)**
**$I_C = f(V_{GE})$**
**$V_{CE}$ = 20 V**




**Schaltverluste IGBT-Wechselr. (typisch)**
**switching losses IGBT-inverter (typical)**
**$E_{on} = f(I_C)$, $E_{off} = f(I_C)$**
**$V_{GE}$ = ±15 V, $R_{Gon}$ = 8.2 Ω, $R_{Goff}$ = 8.2 Ω, $V_{CE}$ = 300 V**



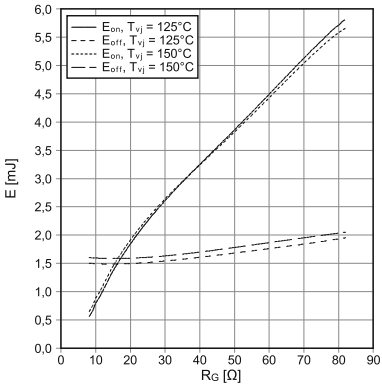

| | |
|---|---|
| prepared by: DK | date of publication: 2010-01-06 |
| approved by: MB | revision: 3.0 |

Technische Information / technical information

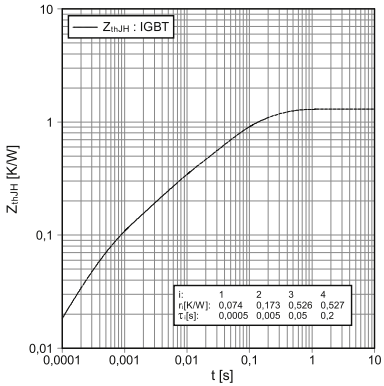
IGBT-Module
IGBT-modules

# F4-50R06W1E3

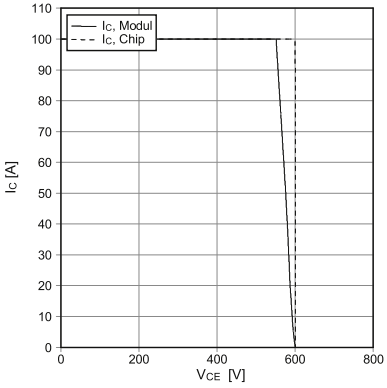
**Schaltverluste IGBT-Wechselr. (typisch)**
**switching losses IGBT-Inverter (typical)**
**$E_{on} = f(R_G)$, $E_{off} = f(R_G)$**
**$V_{GE}$ = ±15 V, $I_C$ = 50 A, $V_{CE}$ = 300 V**



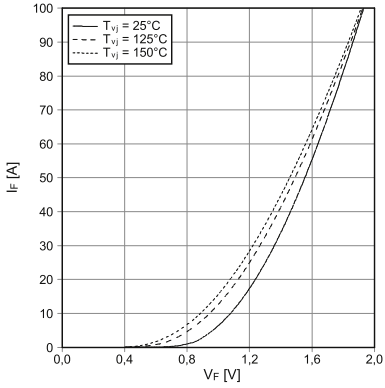

**Transienter Wärmewiderstand IGBT-Wechselr.**
**transient thermal impedance IGBT-inverter**
**$Z_{thJH} = f(t)$**




**Sicherer Rückwärts-Arbeitsbereich IGBT-Wr. (RBSOA)**
**reverse bias safe operating area IGBT-inv. (RBSOA)**
**$I_C = f(V_{CE})$**
**$V_{GE}$ = ±15 V, $R_{Goff}$ = 8.2 Ω, $T_{vj}$ = 150°C**




**Durchlasskennlinie der Diode-Wechselr. (typisch)**
**forward characteristic of diode-inverter (typical)**
**$I_F = f(V_F)$**

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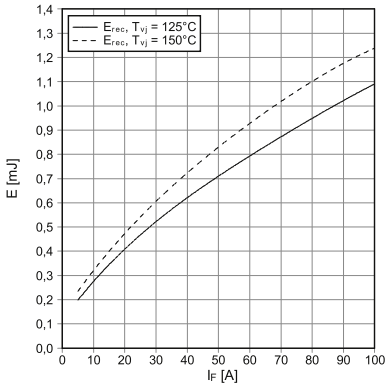
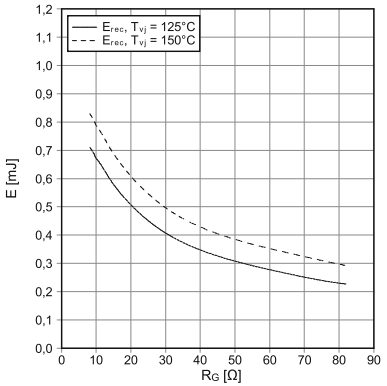
# F4-50R06W1E3

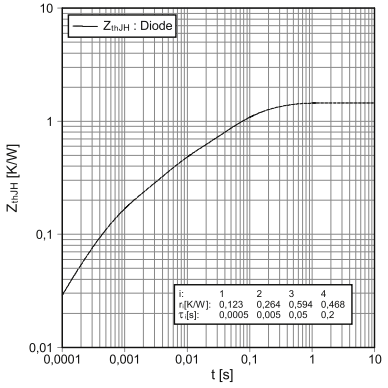
**Schaltverluste Diode-Wechselr. (typisch)**
**switching losses diode-inverter (typical)**
**$E_{rec} = f(I_F)$**
**$R_{Gon} = 8.2\ \Omega$, $V_{CE} = 300$ V**



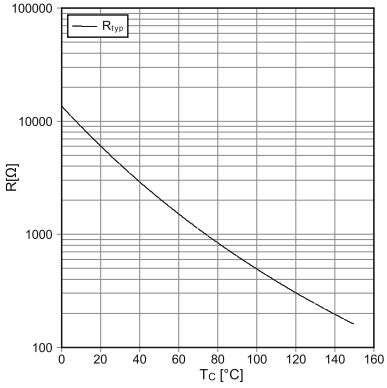

**Schaltverluste Diode-Wechselr. (typisch)**
**switching losses diode-inverter (typical)**
**$E_{rec} = f(R_G)$**
**$I_F = 50$ A, $V_{CE} = 300$ V**




**Transienter Wärmewiderstand Diode-Wechselr.**
**transient thermal impedance diode-inverter**
**$Z_{thJH} = f(t)$**




**NTC-Temperaturkennlinie (typisch)**
**NTC-temperature characteristic (typical)**
**R = f (T)**

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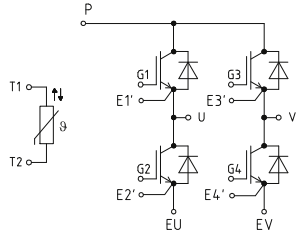
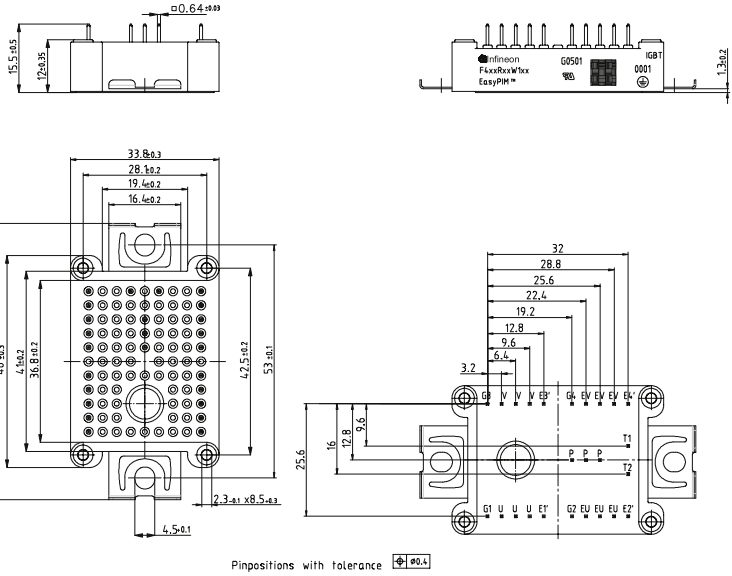
# F4-50R06W1E3

## Schaltplan / circuit diagram




## Gehäuseabmessungen / package outlines

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# SIMULATION OF POWER ELECTRONICS CONVERTERS USING PLECS®

## FARZIN ASADI AND KEI EGUCHI

- Unique examples are included in the simulation of power electronics converters using PLECS®maybe say why PLECs is better/unique?
- Include explanations and guidance for all included simulations for redoing the simulations in own areas of application.
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Power electronic systems are widely used today to provide power processing for applications ranging from computing and communications, appliance control, transportation, and high-power transmission. *Simulation of Power Electronics Converters Using PLECS®* is a guide to simulating a power electronics circuit using the powerful new? Widely used? Most advanced? software for power electronics circuit simulation purposes.

Modeling and simulation are essential ingredients of the analysis and design process in power electronics. This book assists engineers to gain an increased understanding of circuit operation so that they can, for a given set of specifications, choose a topology, select appropriate circuit component types and values, estimate circuit performance, and complete the design by ensuring that the circuit performance will meet specifications even with the anticipated variations in operating conditions and circuit component values.

This book covers the fundamentals of power electronics converter simulation along with analysis of power electronics converters using PLECS® and concludes with real-world simulation examples for applied content making this book useful for all those in the electrical and electronics engineering field.

- Digital Power Electronics and Applications, Luo, 2005, 464p, 9780120887576
- Alternative Energy in Power Electronics, Rashid, 2014, 378p, 9780124167148
- Power Electronics Handbook 4ed, Rashid, 2017, 1522p, 9780128114070

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