

Teuvo Suntio

Tuomas Messo

Joonas Puukko

Power Electronic Converters

Power Electronic Converters

Dynamics and Control in Conventional and
Renewable Energy Applications

Teuvo Suntio, Tuomas Messo, and Joonas Puukko

WILEY-VCH
Verlag GmbH & Co. KGaA

Authors

Dr. Teuvo Suntio

Tampere University of Technology
Laboratory of Electrical Energy Engineering
Korkeakoulunkatu 3
33101 Tampere
Finland

Assist. Prof. Dr. Tuomas Messo

Tampere University of Technology
Laboratory of Electrical Energy Engineering
Korkeakoulunkatu 3
33101 Tampere
Finland

Dr. Joonas Puukko

ABB Oy
Drives
Hiomotie 13
00380 Helsinki
Finland

Cover

iStock ID 536657616/matejmo

All books published by **Wiley-VCH** are carefully produced. Nevertheless, authors, editors, and publisher do not warrant the information contained in these books, including this book, to be free of errors. Readers are advised to keep in mind that statements, data, illustrations, procedural details or other items may inadvertently be inaccurate.

Library of Congress Card No.: applied for

British Library Cataloguing-in-Publication Data

A catalogue record for this book is available from the British Library.

Bibliographic information published by the Deutsche Nationalbibliothek

The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available on the Internet at <<http://dnb.d-nb.de>>.

© 2018 Wiley-VCH Verlag GmbH & Co. KGaA, Boschstr. 12, 69469 Weinheim, Germany

All rights reserved (including those of translation into other languages). No part of this book may be reproduced in any form – by photoprinting, microfilm, or any other means – nor transmitted or translated into a machine language without written permission from the publishers. Registered names, trademarks, etc. used in this book, even when not specifically marked as such, are not to be considered unprotected by law.

Print ISBN: 978-3-527-34022-4

ePDF ISBN: 978-3-527-69851-6

ePub ISBN: 978-3-527-69853-0

Mobi ISBN: 978-3-527-69854-7

oBook ISBN: 978-3-527-69852-3

Cover Design Wiley

Typesetting Thomson Digital, Noida, India

Printing and Binding Weinheim

Printed on acid-free paper

Table of Contents

Preface *xiii*

About the Authors *xv*

Part One Introduction *1*

1 Introduction *3*

1.1 Introduction *3*

1.2 Implementation of Current-Fed Converters *6*

1.3 Dynamic Modeling of Power Electronic Converters *7*

1.4 Linear Equivalent Circuits *8*

1.5 Impedance-Based Stability Assessment *12*

1.6 Time Domain-Based Dynamic Analysis *14*

1.7 Renewable Energy System Principles *17*

1.8 Content Review *19*

References *20*

2 Dynamic Analysis and Control Design Preliminaries *27*

2.1 Introduction *27*

2.2 Generalized Dynamic Representations – DC–DC *27*

2.2.1 Introduction *27*

2.2.2 Generalized Dynamic Representations *29*

2.2.3 Generalized Closed-Loop Dynamics *30*

2.2.4 Generalized Cascaded Control Schemes *33*

2.2.5 Generalized Source and Load Interactions *38*

2.2.6 Generalized Impedance-Based Stability Assessment *40*

2.3 Generalized Dynamic Representations: DC–AC, AC–DC, and AC–AC *42*

2.3.1 Introduction *42*

2.3.2 Generalized Dynamic Representations *44*

2.3.3 Generalized Closed-Loop Dynamics *48*

2.3.4 Generalized Cascaded Control Schemes *50*

2.3.5 Generalized Source and Load Interactions *54*

2.3.6 Generalized Impedance-Based Stability Assessment *56*

2.4	Small-Signal Modeling	57
2.4.1	Introduction	57
2.4.2	Average Modeling and Linearization	60
2.4.3	Modeling Coupled-Inductor Converters	64
2.4.4	Modeling in Synchronous Reference Frame	66
2.5	Control Design Preliminaries	77
2.5.1	Introduction	77
2.5.2	Transfer Functions	77
2.5.3	Stability	84
2.5.4	Transient Performance	95
2.5.5	Feedback-Loop Design Constraints	100
2.5.6	Controller Implementations	103
2.5.7	Optocoupler Isolation	108
2.5.8	Application of Digital Control	109
2.6	Resonant LC-Type Circuits	110
2.6.1	Introduction	110
2.6.2	Single-Section LC Filter	112
2.6.3	LCL Filter	113
2.6.4	CLCL Filter	115
	References	117

Part Two Voltage-Fed DC–DC Converters 123

3	Dynamic Modeling of Direct-on-Time Control	125
3.1	Introduction	125
3.2	Direct-on-Time Control	127
3.3	Generalized Modeling Technique	129
3.3.1	Buck Converter	131
3.3.2	Boost Converter	134
3.3.3	Buck–Boost Converter	136
3.3.4	Superbuck Converter	140
3.4	Fixed-Frequency Operation in CCM	142
3.4.1	Buck Converter	143
3.4.2	Boost Converter	146
3.4.3	Buck–Boost Converter	149
3.4.4	Superbuck Converter	153
3.4.5	Coupled-Inductor Superbuck Converter	157
3.5	Fixed-Frequency Operation in DCM	163
3.5.1	Buck Converter	164
3.5.2	Boost Converter	167
3.5.3	Buck–Boost Converter	170
3.6	Source and Load Interactions	173
3.6.1	Source Interactions	173
3.6.2	Input Voltage Feedforward	174
3.6.3	Load Interactions	176
3.6.4	Output-Current Feedforward	177

3.7	Impedance-Based Stability Issues	179
3.8	Dynamic Review	181
	References	186
4	Dynamic Modeling of Current-Mode Control	189
4.1	Introduction	189
4.2	Peak Current Mode Control	190
4.2.1	PCM Control Principles	190
4.2.2	Development of Duty-Ratio Constraints in CCM	192
4.2.3	Development of Duty-Ratio Constraints in DCM	195
4.2.4	Origin and Consequences of Mode Limits in CCM and DCM	196
4.2.5	Duty-Ratio Constraints in CCM	201
4.2.5.1	Buck Converter	201
4.2.5.2	Boost Converter	201
4.2.5.3	Buck–Boost Converter	202
4.2.5.4	Superbuck Converter	204
4.2.5.5	Coupled-Inductor Superbuck Converter	205
4.2.6	Duty-Ratio Constraints in DCM	205
4.2.6.1	Buck Converter	205
4.2.6.2	Boost Converter	206
4.2.6.3	Buck–Boost Converter	206
4.2.7	General PCM Transfer Functions in CCM	207
4.2.8	PCM State Spaces and Transfer Functions in CCM	209
4.2.8.1	Buck Converter	209
4.2.8.2	Boost Converter	211
4.2.8.3	Buck–Boost Converter	213
4.2.8.4	Superbuck Converter	215
4.2.8.5	Coupled-Inductor Superbuck Converter	219
4.2.9	PCM State Spaces in DCM	222
4.2.9.1	Buck Converter	222
4.2.9.2	Boost Converter	222
4.2.9.3	Buck–Boost Converter	223
4.3	Average Current-Mode Control	224
4.3.1	Introduction	224
4.3.2	ACM Control Principle	225
4.3.3	Modeling with Full Ripple Inductor Current Feedback	226
4.4	Variable-Frequency Control	230
4.4.1	Introduction	230
4.4.2	Self-Oscillation Modeling – DOT and PCM Control	231
4.5	Source and Load Interactions	239
4.5.1	Output Current Feedforward	240
4.6	Impedance-Based Stability Issues	243
4.7	Dynamic Review	244
4.8	Critical Discussions on PCM Models and Their Validation	249
4.8.1	Ridley’s Models	249
4.8.2	The Book PCM Model in CCM	252

4.8.3	Evaluation of PCM-Controlled Buck in CCM	253
4.8.4	Evaluation of PCM-Controlled Boost in CCM	258
4.8.5	Concluding Remarks	259
References		260
5	Dynamic Modeling of Current-Output Converters	265
5.1	Introduction	265
5.2	Dynamic Modeling	267
5.3	Source and Load Interactions	269
5.3.1	Source Interactions	269
5.3.2	Load Interactions	270
5.4	Impedance-Based Stability Issues	271
5.5	Dynamic Review	272
References		275
6	Control Design Issues in Voltage-Fed DC–DC Converters	277
6.1	Introduction	277
6.2	Developing Switching and Average Models	279
6.2.1	Switching Models	279
6.2.2	Averaged Models	287
6.3	Factors Affecting Transient Response	291
6.3.1	Output Voltage Undershoot	292
6.3.2	Settling Time	294
6.4	Remote Sensing	304
6.4.1	Introduction	304
6.4.2	Remote Sensing Dynamic Effect Analysis Method	304
6.4.3	Remote Sensing Impedance Block Examples	306
6.4.4	Experimental Evidence	307
6.5	Simple Control Design Method	310
6.5.1	DDR-Controlled Buck Converter	312
6.5.2	PCM-Controlled Buck Converter	315
6.5.3	DDR-Controlled Boost Converter	321
6.5.4	PCM-Controlled Boost Converter	325
6.6	PCM-Controlled Superbuck Converter: Experimental Examples	330
6.6.1	Introduction	330
6.6.2	Discrete-Inductor Superbuck	331
6.6.3	Coupled-Inductor Superbuck	332
6.7	Concluding Remarks	334
References		334
 Part Three Current-Fed Converters 339		
7	Introduction to Current-Fed Converters	341
7.1	Introduction	341
7.2	Duality Transformation Basics	341
7.3	Duality-Transformed Converters	345

7.4	Input Capacitor-Based Converters	351
	References	352
8	Dynamic Modeling of DDR-Controlled CF Converters	355
8.1	Introduction	355
8.2	Dynamic Models	356
8.2.1	Duality Transformed Converters	358
8.2.1.1	Buck Converter	358
8.2.1.2	Boost Converter	365
8.2.1.3	Noninverting Buck–Boost Converter	368
8.2.1.4	CF Superbuck Converter	372
8.2.2	Input Capacitor-Based Converters	376
8.2.2.1	Buck Power-Stage Converter	377
8.2.2.2	Boost Power-Stage Converter	383
8.2.2.3	Noninverting Buck–Boost Power-Stage Converter	387
8.3	Source and Load Interactions	390
8.3.1	CF-CO Converters	390
8.3.1.1	Source Interactions	390
8.3.1.2	Load Interactions	391
8.3.2	CF-VO Converters	392
8.3.2.1	Source Interactions	392
8.3.2.2	Load Interactions	393
8.4	Impedance-Based Stability Assessment	394
8.5	Output-Voltage Feedforward	394
8.6	Dynamic Review	397
	References	400
9	Dynamic Modeling of PCM/PVM-Controlled CF Converters	403
9.1	Introduction	403
9.2	Duty-Ratio Constraints and Dynamic Models under PCM Control	404
9.2.1	Buck Power-Stage Converter	405
9.2.2	Boost Power-Stage Converter	410
9.3	Duty-Ratio Constraints and Dynamic Models under PVM Control	413
9.3.1	CF Buck Converter	414
9.3.2	CF Superbuck Converter	418
9.4	Concluding Remarks	420
	References	420
10	Introduction to Photovoltaic Generator	423
10.1	Introduction	423
10.2	Solar Cell Properties	424
10.3	PV Generator	429
10.4	MPP Tracking Methods	432
10.5	MPP Tracking Design Issues	436
10.5.1	Introduction	436
10.5.2	General Dynamics of PV Power	437
10.5.3	PV Interfacing Converter Operating at Open Loop	439

- 10.5.4 PV Interfacing Converter Operating at Closed Loop 447
 - 10.5.4.1 Reduced-Order Models: Intuitive Model Reduction 452
 - 10.5.4.2 Reduced-Order Models: Control-Engineering-Based Method 454
 - 10.5.4.3 Reduced-Order Model Verification 455
- 10.6 Concluding Remarks 461
- References 461

- 11 Photovoltaic Generator Interfacing Issues 465**
 - 11.1 Introduction 465
 - 11.2 Centralized PV System Architecture 465
 - 11.3 Distributed PV System Architectures 465
 - 11.4 PV Generator-Induced Effects on Interfacing-Converter Dynamics 470
 - 11.4.1 Introduction 470
 - 11.4.2 PV Generator Effects on Converter Dynamics 474
 - 11.4.2.1 Buck Power-Stage Converter 476
 - 11.4.2.2 Boost Power-Stage Converter 477
 - 11.4.2.3 CF Superbuck Converter 480
 - 11.5 Stability Issues in PV Generator Interfacing 482
 - 11.5.1 Buck Power-Stage Converter 483
 - 11.5.2 CF Superbuck Converter 485
 - 11.5.3 Concluding Remarks 488
 - 11.6 Control Design Issues 488
 - References 488

Part Four Three-Phase Grid-Connected Converters 491

- 12 Dynamic Modeling of Three-Phase Inverters 493**
 - 12.1 Introduction 493
 - 12.2 Dynamic Model of Voltage-Fed Inverter 494
 - 12.2.1 Average Model of Voltage-Fed Inverter 494
 - 12.2.2 Linearized State-Space and Open-Loop Dynamics 499
 - 12.2.3 Control Block Diagrams of Voltage-Fed Inverter 503
 - 12.2.4 Verification of Open-Loop Model 503
 - 12.3 Dynamic Model of Current-Fed Inverter 507
 - 12.3.1 Average Model of Current-Fed Inverter 507
 - 12.3.2 Linearized Model and Open-Loop Dynamics 510
 - 12.3.3 Control Block Diagrams of Current-Fed Inverter 512
 - 12.3.4 Verification of Open-Loop Model 512
 - 12.4 Source-Affected Dynamics of Current-Fed Inverter 515
 - 12.4.1 Source Effect: Photovoltaic Generator 517
 - 12.4.2 Source Effect: Experimental Validation 520
 - 12.5 Dynamic Model of Current-Fed Inverter with LCL-Filter 524
 - 12.5.1 Average Model of Current-Fed Inverter with LCL-Filter 525

12.5.2	Linearized State-Space and Open-Loop Dynamics	527
12.6	Summary	528
	Appendix 12.A	528
	References	530
13	Control Design of Grid-Connected Three-Phase Inverters	533
13.1	Introduction	533
13.2	Synchronous Reference Frame Phase-Locked-Loop	533
13.2.1	Linearized Model of SRF-PLL	536
13.2.2	Control Design of SRF-PLL	538
13.2.3	Damping Ratio and Undamped Natural Frequency	541
13.2.4	Control Design Example and Experimental Verification	541
13.2.5	The Effect of Unbalanced Grid Voltages	544
13.3	AC Current Control	547
13.3.1	Current Control in the dq-Domain	548
13.3.2	Current Control in Voltage-Fed Inverters	548
13.4	Decoupling Gains	559
13.5	Grid Voltage Feedforward	562
13.6	Cascaded Control Scheme in Current-Fed Inverters	563
13.6.1	Control Block Diagrams	564
13.6.2	Control Design of Cascaded Loops	566
13.6.3	Instability Caused by RHP-Pole	570
13.6.4	Stability Assessment Using the Nyquist Stability Criterion	574
13.6.5	Design Example: Three-Phase Photovoltaic Inverter	574
13.7	Case Study: Instability Due to RHP-Pole	581
13.8	Summary	583
	References	583
14	Reduced-Order Closed-Loop Modeling of Inverters	587
14.1	Introduction	587
14.2	Reduced-Order Model of Voltage-Fed Inverter	587
14.2.1	Closed-Loop Model with AC Current Control	588
14.2.2	Closed-Loop Model with SRF-PLL	591
14.2.3	Closed-Loop Input Admittance	595
14.2.4	Output Impedance with Grid Voltage Feedforward	596
14.2.5	Impedance Characteristics of Voltage-Fed Inverters	602
14.3	Reduced-Order Model of Current-Fed Inverter with L-Type Filter	602
14.3.1	Closed-Loop Model with Cascaded Control Scheme	602
14.3.2	Effect of Input Voltage Control Bandwidth	605
14.3.3	Effect of AC Current Control Bandwidth	606
14.3.4	Experimental Verification: Measured Impedance d-Component	608
14.3.5	Effect of SRF-PLL	609
14.3.6	Effect of Grid Voltage Feedforward on Impedance d-Component	610
14.3.7	Effect of Grid Voltage Feedforward on Impedance q-Component	615

14.4	Closed-Loop Model of Current-Fed Inverter with LC-Type Filter	619
14.4.1	Experimental Verification of Impedance Model	625
14.4.2	Impedance Characteristics of Inverter with LC-Filter and Feedforward	630
14.5	Summary	630
	References	630
15	Multivariable Closed-Loop Modeling of Inverters	633
15.1	Introduction	633
15.2	Full-Order Model of Current-Fed Inverter with L-Type Filter	633
15.2.1	Verification of Dynamic Model	643
15.3	Experimental Verification of Admittance Model	646
15.4	Full-Order Model of Current-Fed Inverter with LCL-Type Filter	648
15.4.1	Verification of Closed-Loop Model	653
15.4.2	Measured Output Impedance of PV Inverter	656
15.5	Summary	659
	References	660
16	Impedance-Based Stability Assessment	663
16.1	Introduction	663
16.2	Modeling of Three-Phase Load Impedance in the dq -Domain	664
16.3	Impedance-Based Stability Criterion	667
16.4	Case Studies	669
16.4.1	Instability Due to High-Bandwidth PLL in Weak Grid	669
16.4.2	Instability Due to Control Delay in Feedforward Path	674
16.5	Summary	678
	References	678
17	Dynamic Modeling of Three-Phase Active Rectifiers	681
17.1	Introduction	681
17.2	Open-Loop Dynamics	681
17.3	Verification of Open-Loop Model	688
17.4	Experimental Results	691
17.5	Summary	695
	References	695
	Index	697

Preface

Rigid voltage sources, such as an ideal grid, an output-voltage feedback-controlled converter, and a storage battery, have dominated as input sources for a long time. As a consequence, the scholars and engineers have learned every detail and developed a multitude of power stages and control methods for the voltage domain. A common characteristic of these sources is that their output impedance is low in magnitude at low frequencies. From time to time, a term current-sourced converter has been used with a voltage-sourced converter in case there is an inductor connected in series with the voltage-type source. Unfortunately, such a converter has no explicit relation to the current source as an input source. However, duality implies that there also exist sources that can be classified as real current sources, that is, sources that have an output impedance, which is high in magnitude.

Since the last decade, people have started paying more and more attention on renewable energy sources for providing pollution-free energy and ensuring energy availability also in the future. Usually, most of the power electronic converters applied in interfacing the renewable energy sources into power grid in grid-feeding mode are to be considered as current-fed converters due to the feedback control of DC voltage. Despite the real nature of the input source, the scholars and engineers still like to consider them as voltage sources and justify their opinions by means of Norton–Thevenin transformation. The dual nature of the photovoltaic generators (i.e., current and voltage at specific operation points of their current–voltage curve) makes them an input source that may be too confusing for an engineer to analyze and thus the analysis will be performed in the familiar voltage domain even though such a power source will significantly affect the dynamic behavior of the converters connected at their output terminals. The long history of voltage sources as the dominating input source has created a situation, which has prevented the full understanding of the special features introduced by the current sources as input sources. This is quite understandable, because the most difficult learning process is to learn out from the past.

This book contains material from both of the domains by using the same power stage powered either by the rigid voltage or the current source. The differences in the dynamic behavior of the converters in different domains are explicitly shown including also comprehensive analyses of the source and load interactions in DC–DC converter as well as in grid-connected three-phase converters. Similar material cannot be found from any available book and the material in scientific

papers is scarce and may be hard to identify from the vast number of published papers.

Many individuals have helped us to create the book during the past 20 years in academy. Most of those individuals are our past Ph.D. students and colleagues at TUT, who have created new knowledge during the research projects we have conducted together. We appreciate very much the Finnish industry and funding organizations, who have helped us to fund the research.

Tampere University of Technology
Tampere, Finland

Teuvo Suntio

Tampere University of Technology
Tampere, Finland

Tuomas Messo

ABB Oy
Helsinki, Finland

Joonas Puukko

About the Authors



Teuvo Suntio received his Ph.D. degree in electrical engineering in 1992 from Helsinki University of Technology, Finland. After several R&D engineering and managerial positions during the 22 years in Power Electronics Industry, he accepted a post as a Professor in 1998 in the Electronics Laboratory at University of Oulu, Finland, before moving to Department of Electrical Engineering, Tampere University of Technology in 2004, which is the post he still holds. Professor Suntio's current research interests include dynamic characterization and control of power electronic converters and systems, especially in renewable energy applications. He holds several international patents and has authored or coauthored over 230 international journal and conference publications. He is a Senior Member of IEEE, and has served as an associate editor in *IEEE Transactions on Power Electronics* since 2010.



Tuomas Messo was born in 1985 in Hämeenlinna, Finland. He finalized his M.Sc. and Ph.D. degrees in electrical engineering at Tampere University of Technology (TUT), Tampere, Finland in 2011 and 2014, respectively.

In 2014–2015, he worked as Post-Doctoral Researcher at TUT and in 2016 he was appointed as an Assistant Professor (Tenure Track) in the field of power electronics. He is currently working at the Laboratory of Electrical Energy Engineering at TUT where he carries out lecturing, research, and supervision of electrical engineering students of all degrees.

His main research interests include dynamic modeling of power converters in renewable energy applications and smart grids, impedance-based stability analysis, frequency-domain measurements, control design, and stability analysis of control systems.



Joonas Puukko was born in Helsinki, Finland. He has M.Sc. and Ph.D. degrees (both with distinction) in electrical engineering from the Tampere University of Technology, Tampere, Finland.

He was previously working at ABB Solar Inverters in Helsinki, Finland and ABB Corporate Research Raleigh, NC, USA. At the moment, he is with ABB High Power Drives in Helsinki, Finland. His research interests include power electronics in a range of applications from drives to interfacing of renewable energy systems with the utility grid. He has design experience in wide-bandgap semiconductors, high-frequency magnetics, and frequency-domain modeling/verification.

Part One

Introduction

1

Introduction

1.1 Introduction

For a long time, voltage-type sources such as storage battery, AC grid, and output-voltage-regulated converters have dominated as an input source for power electronic converters [1,2]. These sources are usually referred to as rigid sources, since the load has limited influence on their operating voltage. Both awareness on the depletion of fossil fuel reserves and their impact on the observed climate changes have accelerated the utilization of renewable energy sources, for example, wind and solar [3]. Effective large-scale utilization of these energy sources requires the use of grid-interfaced power electronic converters [4,5]. It has been recently concluded [6,7] that the power electronic converters used in the photovoltaic (PV) systems are essentially current-sourced converters because of the current-source properties of PV generator [8,9] forced by the input-side voltage feedback control [10,11]. At open loop, the static and dynamic properties of the integrating converter are determined by the operating region of the PV generator. The same also applies for the converters in wind energy systems. Another example of a perfect current source is superconducting magnetic energy storage (SMES) system, where a very large inductor serves as the energy storage element [12,13]. Even though the properties of the mentioned sources are already well known [14,15], they are still typically considered as voltage sources when designing the interfacing converter power stages [16,17] or analyzing their underlying dynamics [18–21] despite their current-type properties. The analysis method is usually justified by Norton/Thevenin transformation [20].

The existence of two different input source types implies that two different families of power electronic converters shall also exist, where the converters shall be referred to as voltage-fed (VF) (Figure 1.1) and current-fed (CF) (Figure 1.2) converters, possessing different steady-state and dynamic properties even though the power stage can be the same in both of the cases [7,22]. The term current source has already been widely used, for example, in Ref. [23–28], denoting a voltage-fed converter, where an inductor is placed on the input-side current path such as a boost-type converter [29] or two-inductor (super)buck converter [30]. Fuel cells as renewable energy sources [31] are such an input source, which can be considered to be either voltage or current sources due to their rather constant

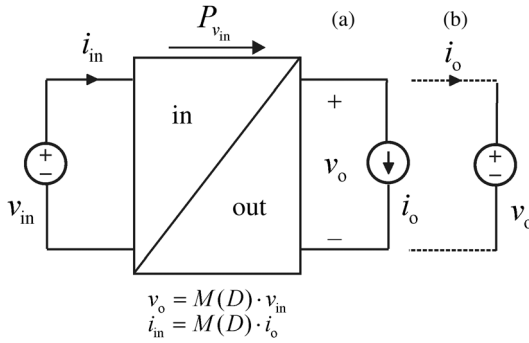


Figure 1.1 VF converter. (a) VO mode. (b) CO mode. *Source:* Suntio 2014. Reproduced with permission of IEEE.

output impedance [32] and operation at the voltages less than the maximum power point [33]. Therefore, the elimination of the harmful low-frequency ripple can be performed by using either input current (i.e., voltage source) or input voltage (i.e., current source) feedback control [34].

On the load side, the output voltage of a converter shall not be taken automatically as an output variable, since this is true only when the converter serves as a typical power supply, regulating its output voltage. In case, the converter is used, for example, as a battery charger or grid-connected inverter, the output voltage is determined by the load-side source and hence output current shall be treated as an output variable. Therefore, the static input-to-output ratio $M(D)$, where D denotes the steady-state duty cycle, shall be actually determined as the ratio of the input-terminal variable characterizing the input source and the same variable at the output terminal, that is, the voltage ratio in a VF converter and the current ratio in a CF converter. According to Figures 1.1 and 1.2, the converter may serve either as a VF or as a CF converter with voltage (VO) or current (CO) as its main output variable, depending on the application. In all the cases, the terminal constraints in terms of voltage and current levels remain unchanged. Reference [22] shows explicitly in theory and by experimental measurements that the dynamic behavior changes significantly application by application as demonstrated in Figure 1.3, where the measured frequency responses of the control-to-output transfer functions with different terminal source configurations are shown. Therefore, it is very important to identify the correct nature of the terminal sources when analyzing the dynamics of the

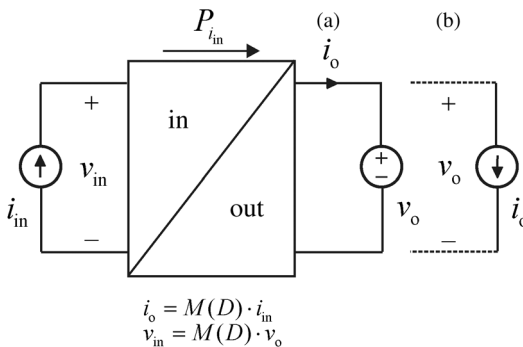


Figure 1.2 CF converter. (a) CO mode. (b) VO mode. *Source:* Suntio 2014. Reproduced with permission of IEEE.

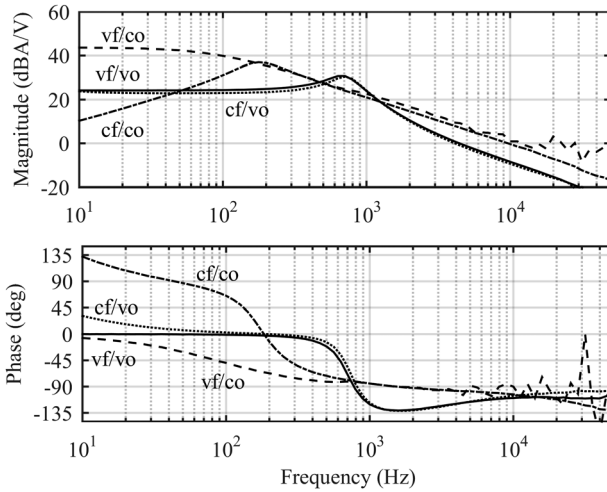


Figure 1.3 The frequency responses of a buck power stage converter when the terminal sources are varied (i.e., voltage-fed converters at voltage (vf/vo) and current (vf/co) output modes and current-fed converters at current (cf/co) and voltage (cf/vo) modes).

converter, for example, for control design purposes, which is obvious when studying the frequency responses in Figure 1.3.

Every power electronic converter has unique internal dynamics, which will determine the obtainable transient dynamics and robustness of stability as well as its sensitivity to the external source and load impedances [35–37]. The internal dynamics can be represented by a certain set or sets of transfer functions, which are classified in circuit theory according to the network parameters [38] known as G (Figure 1.1a), Y (Figure 1.1b), H (Figure 1.2a), and Z (Figure 1.2b), respectively. The specific transfer functions can be directly modeled and measured as frequency responses only when the used terminal sources correspond to the ideal terminal sources given for each of the sets in Figures 1.1 and 1.2. Even if the concept of internal dynamics is basically well known (i.e., all effects from the source and load impedances are removed) [7,35], the tendency is still to use a resistor as a load [39] yielding load-affected models or measured frequency responses. A power stage fed by a certain input source under direct duty ratio (DDR) control tends to maintain the output mode the same as the input source (i.e., VF converters are inherently voltage sources at their output, and CF converters are current sources at their output). As a consequence, the internal transfer functions of such converters can be measured directly at open loop. The other possible output mode does not work at open loop due to violation of Kirchhoff's voltage or current law. The same also applies for the current-mode control, which changes the converter to be a current-output converter [40]. In such a case, the use of resistive load is well justified, but the internal transfer functions have to be computed from the load-affected transfer functions for being useful [7].

A large number of excellent power electronics textbooks are available, such as Refs [5,7,25,39,41–47], which are dedicated to the converters providing either

DC–DC or DC–AC (AC–DC) conversion, or even both. None of these textbooks presents topics that treat the CF converters even if they exist or may even dominate within the specific application area covered in the specific books. The inclusion of the effect of source and load impedances on the converter dynamics is also usually left out by the topics covered in the books even if they are considered very important in practical applications.

The main goal of this book is to provide the missing information in order to complement the other textbooks as well as to present the base for the dynamic analysis of the converters in a general form, which can be utilized with both analytically derived transfer functions and the experimentally measured transfer functions. As a consequence, the potentials of the theoretical work are extended into practice and for the usage of practicing engineers.

The topics covered in the book are briefly discussed and clarified in the subsequent sections in order to familiarize the reader with the secrets of dynamic modeling, analysis, and control designs in both DC-voltage/current source and AC-voltage/current source domains. The mastering of these items requires quite consistent thinking ability as well as flexibility to change from one set of dynamic descriptions to another while moving on.

1.2 Implementation of Current-Fed Converters

There are actually three different methods to implement CF converters: (i) applying capacitive switching cells to construct CF converters [48] similarly as the inductive switching cells are applied, for example, in Refs [1,2], (ii) applying duality transformation methods [49–53], and (iii) adding a capacitor to the input terminal of a VF converter [54] to satisfy the terminal constraints imposed by the input current source [55]. The duality transformation yields CF converters, which retain the main static and dynamic properties characterizing the original VF converter [52]. The adding of a capacitor at the input terminal of a VF converter yields a CF converter having static and dynamic properties resembling the dual of the original converter, that is, a VF buck converter will have characteristics resembling a boost converter and vice versa [54].

As an example, the power stage of a VF buck converter and its dual, that is, the corresponding power stage of a CF buck converter, are given in Figures 1.4 and 1.5. In the original buck converter, the high-side switch S_{HS} conducts during the

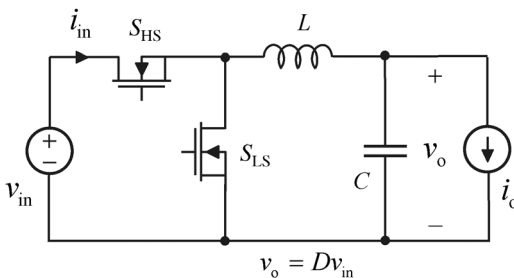


Figure 1.4 VF buck converter.

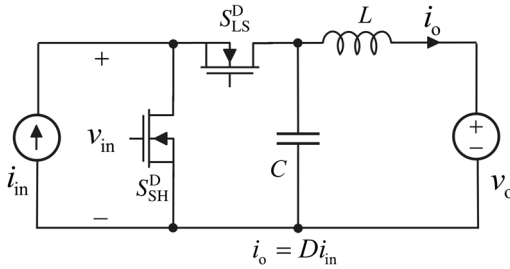


Figure 1.5 CF buck converter.

on-time and the low-side switch S_{LS} during the off-time. In the CF buck converter, the low-side switch S_{LS}^D conducts during the on-time and the high-side switch S_{HS}^D during the off-time. As both of the converters are buck-type converters, the ideal input-to-output relation or modulo $M(D) = D$.

It has been observed earlier that the VF-converter power stages used in the interfacing of PV generators exhibit peculiar properties, such as appearing of right-half-plane (RHP) zero in the control dynamics of buck power stage converter [56], unstable operation when the output voltage or current is tightly controlled [57], necessity to reduce the pulsewidth for increasing the output variables [58,59], and appearing of RHP pole when peak-current-mode (PCM) control is applied in a buck power-stage converter [60,61], and even the impedance-based stability assessment has to be performed differently compared to the VF converters [62]. The observed phenomena are good evidence for the necessity to fully take into account the used terminal sources as discussed in Ref. [22].

1.3 Dynamic Modeling of Power Electronic Converters

The methods to develop the required small-signal or dynamic models for the power electronic converters date back to the early 1970s [63] when the foundation for the state space averaging (SSA) method was laid down [64] and later modified to correctly capture the dynamics associated with the discontinuous conduction mode (DCM) of operation [65,66] as well as with the variable frequency operation [67,68]. The same methods also apply equally to modeling the dynamics of three-phase grid-connected power converters [69]. The SSA method is observed to produce accurate models up to half the switching frequency.

One of the most fundamental issues in performing the modeling in addition to the recognition of the correct input and output variables is that the state variables are to be considered as the time-varying average values within one switching cycle of the corresponding instantaneous values [66]. In continuous conduction mode (CCM), this is also true in the instantaneous state variables and, therefore, the averaged state space can be constructed by computing the required items directly by applying circuit theory. The continuity is also reflected as the known length of the on-time and off-time. In DCM, the instantaneous variables are not anymore necessarily continuous signals but rather pulsating signals, which is also reflected as the unknown length of off-time. Therefore, their time-varying average values

have to be computed based on the wave shapes of their instantaneous values and used for computing the length of the unknown off-time. A number of variants are available for the basic SSA method in continuous time as well as in discrete time, which can also be used for obtaining the dynamic models but they do not offer usually such benefits, which would justify their usage in practical applications.

The original SSA method can be applied as such only to the converters, which operate in CCM under DDR control, which is also known as voltage-mode (VM) control [39]. The last term is not recommended, however, to be used, because it will mean in the future the internal control methods in a CF converter, where the feedback is taken from the capacitor voltage (i.e., peak voltage mode (PVM) or average voltage mode (AVM)) similarly as the current-mode controls (i.e., peak current (PCM) or average current (ACM)) in a VF converter. The dynamic models (i.e., the small-signal state space) induced by the DDR control will serve as the base for the modeling of the converters, where the internal feedback loops are used to affect the duty ratio generation, that is, the dynamics associated with the duty ratio. The modeling of those converters can be simply done by developing proper duty-ratio constraints, where the perturbed duty ratio is expressed as a function of the state and input variables of the converter [7]. In case of variable-frequency operation, the duty ratio is nonlinear and, therefore, the on-time of the switches has to be used as the control variable instead of duty ratio [7,68].

1.4 Linear Equivalent Circuits

As an outcome of the SSA modeling method [64], the dynamics of the associated converter was represented by means of the canonical equivalent circuit given in Figure 1.6, which is valid for a second-order or two-memory-element converter operating in CCM under DDR control. The structure and the circuit elements of the equivalent circuit can be found from the corresponding small-signal state space. Similar equivalent circuit can also be constructed for the higher order converters as well as for CF converters (see Figure 1.7) applying the same methodology. Figures 1.6 and 1.7 provide clear physical insight into the dynamic processes inside the converters as well as clearly indicate the differences the

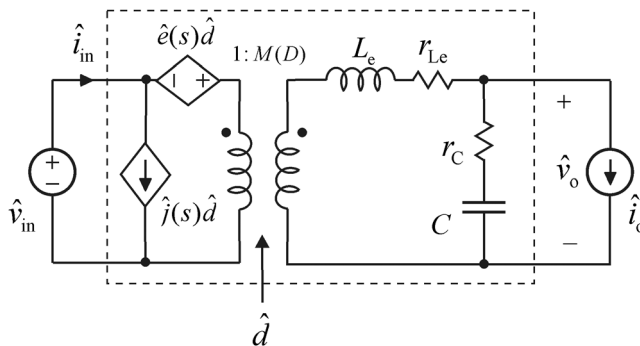


Figure 1.6 Canonical equivalent circuit for a second-order VF/VO converter.

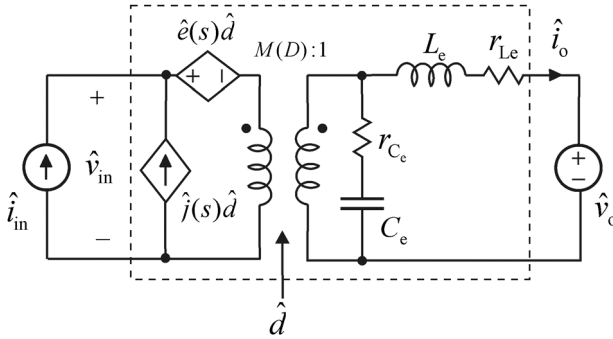


Figure 1.7 Canonical equivalent circuit for a second-order CF/CO converter.

duality transformation produces in the converter. As being a linear representation of the converter, the effect of the source and load impedances can be computed by applying circuit theory, which is very important for understanding the dynamic behavior of the practical systems.

Similar equivalent circuits as in Figures 1.6 and 1.7 cannot be, however, constructed for the converters operating in DCM or containing internal feedbacks, for example, PCM control. More general equivalent circuit can be constructed based on the set of transfer functions comprising the network parameters G , Y , H , and Z , which can be utilized similarly as the canonical equivalent circuits in Figures 1.6 and 1.7 to assess the effect of nonideal source and load [7,70]. Figures 1.8 and 1.9 show such a generic equivalent circuit representing the dynamics of VF/VO DC–DC and a VF/CO DC–DC converters, respectively. On comparing the equivalent circuits in Figures 1.6 and 1.7 with the equivalent circuits in Figures 1.8 and 1.9, the main difference found between them is that the latter equivalent circuits present explicitly the main terminal characteristics of a converter. This information is actually very important for being able to fulfill the terminal constraints stipulated by the different input and output sources.

Similar equivalent circuits as in Figures 1.6 and 1.7 can also be constructed for the three-phase grid-connected converters by means of their small-signal state space given in the synchronous reference frame applying power invariant transformation (i.e., power-invariant d–q state space), as shown in Figures 1.10 and 1.11 [71,72]. The corresponding physical schematics are given in Figures 1.12

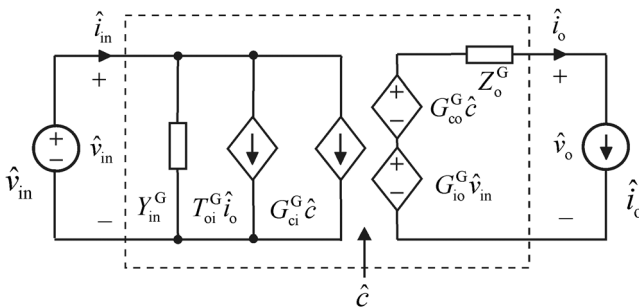


Figure 1.8 Generic equivalent circuit for a VF/VO converter.

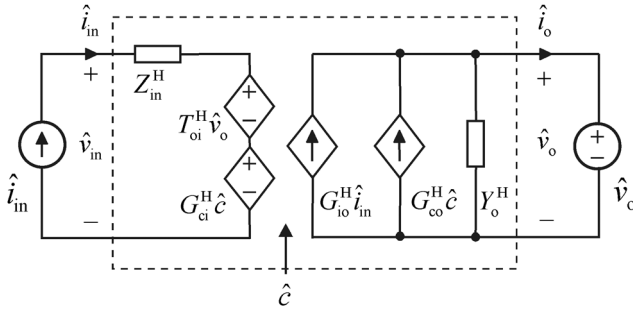


Figure 1.9 Generic equivalent circuit for a CF/CO converter.

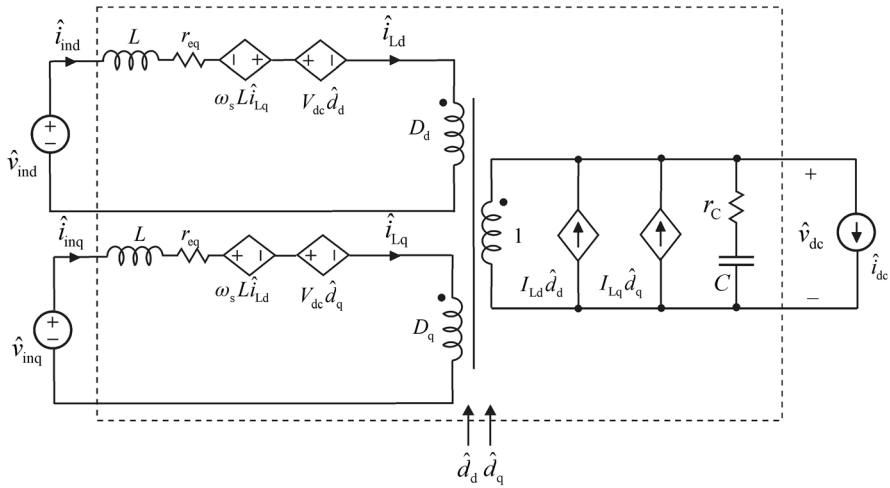


Figure 1.10 Canonical equivalent circuit for a three-phase AC-DC converter.

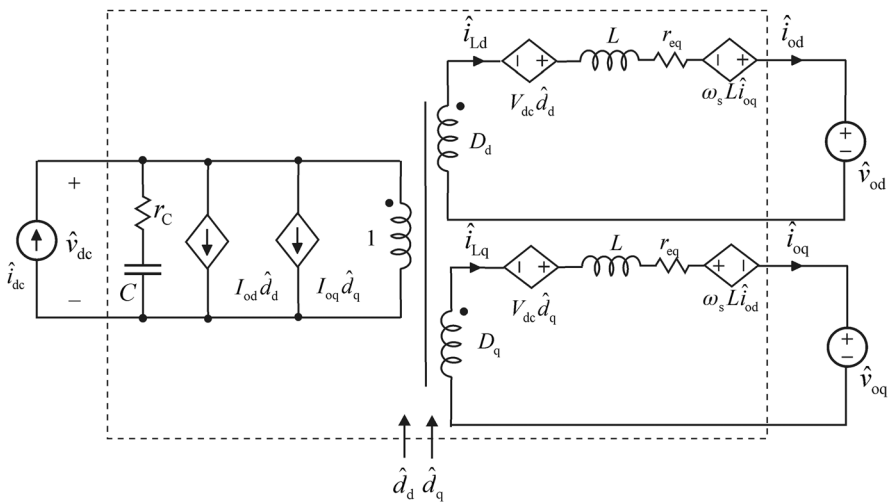


Figure 1.11 Canonical equivalent circuit for a current-fed three-phase DC-AC converter.

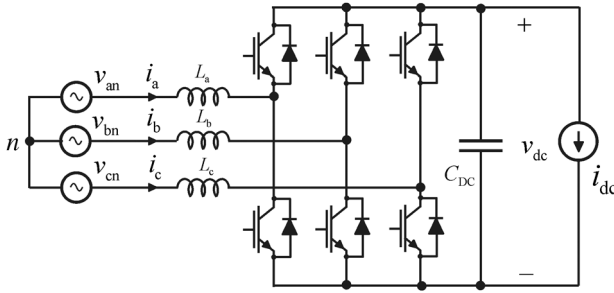


Figure 1.12 Three-phase grid-connected rectifier.

and 1.13, respectively. According to Figures 1.12 and 1.13, the converters can be constructed from each other by changing the direction of power flow. This similarity is also visible in the corresponding equivalent circuits. These equivalent circuits would give the same physical insight as the corresponding DC–DC equivalent circuits.

Similar equivalent circuits as in Figures 1.10 and 1.11 cannot be, however, constructed for the converters operating in DCM or containing internal feedbacks. Similarly, as in the case of DC–DC converters, the more general equivalent circuits can be constructed based on the set of transfer functions comprising the network parameters G , Y , H , and Z , which can be utilized similarly as the canonical equivalent circuits in Figures 1.10 and 1.11 to assess the effect of nonideal source and load [7,73]. Figure 1.14 shows such a generic equivalent circuit representing the dynamics of a three-phase grid-connected AC–DC converter, and Figure 1.15 shows a generic equivalent circuit representing the dynamics of a three-phase grid-connected current-fed inverter. On comparing the equivalent circuits in Figures 1.10 and 1.11 with the equivalent circuits in Figures 1.14 and 1.15, the main difference found between them is that the latter equivalent circuits present explicitly the main terminal characteristics of a converter. This information is actually very important for being able to fulfill the terminal constraints stipulated by the different input and output sources.

The variables of the equivalent circuits with a superscript s denote the three-phase variables transformed into the synchronous reference frame (SRF) composed of direct (d) and quadrature (q) components of the variables, respectively. The

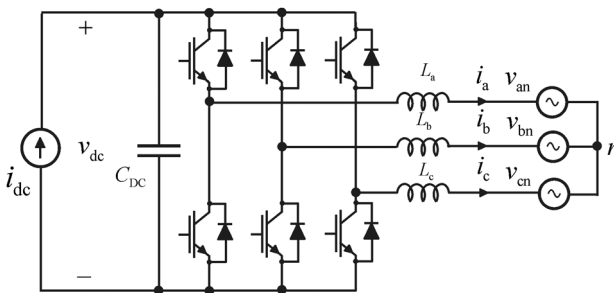


Figure 1.13 Three-phase grid-connected current-fed inverter.

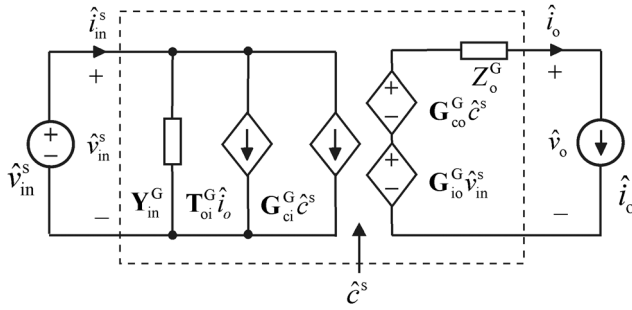


Figure 1.14 Generic equivalent circuit for a three-phase grid-connected VF/VO converter.

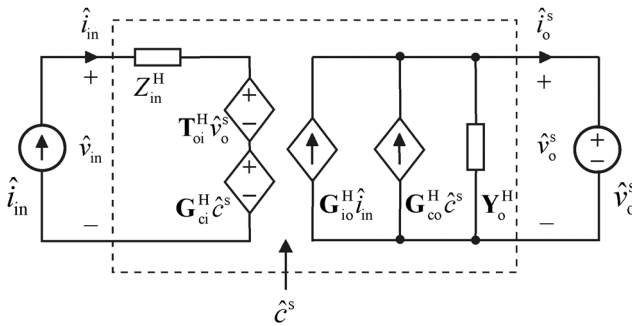


Figure 1.15 Generic equivalent circuit for a three-phase grid-connected CF/CO converter.

transfer functions represented with boldface letters denote a transfer function matrix composed of two or four discrete transfer functions. The computation of the effect of nonideal source and load has to be performed by applying matrix manipulation techniques instead of circuit theoretical methods [73].

The generic equivalent circuits are very flexible tools for solving the dynamic problems associated with the impedance-based interactions [37,71,74] as well as for assessing the stability in the practical interconnected systems [75,76]. The dynamic equivalent circuits as well as the corresponding matrix-form representations can be equally utilized by means of the model-based analytic transfer functions and the corresponding measured frequency responses or even by their combination.

1.5 Impedance-Based Stability Assessment

Stability assessment of a system composed of interconnected power electronic converters as well as passive impedance-like elements can be effectively performed at any interface within the system by means of the ratio of upstream and downstream impedances measured or predicted at the interface [7,22,63,75–84].

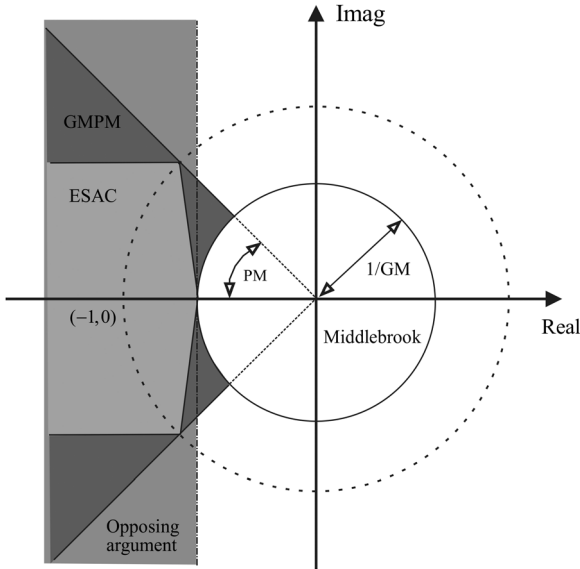


Figure 1.16 Collection of forbidden regions in the complex plane according to Refs [77–84]. Source: Vesti 2013. Reproduced with permission of IEEE.

The method was originally launched in Refs [77,78] for designing stable input-filter converter systems. The ratio was named as minor loop gain, where the input-filter output impedance is the upstream impedance and the input impedance of the converter is the downstream impedance. The minor loop gain denotes the ratio of the upstream and downstream impedances. The stability of the interconnected system is retained when the minor loop gain satisfies *Nyquist* stability criterion. It has been later observed that the original minor loop gain is only valid for a certain type of interfaces, that is, the upstream subsystem is a voltage-type system and the downstream system a current-type system. A general definition for the construction of the minor loop gain is such that the numerator impedance shall be the internal impedance of the voltage-type subsystem and the denominator impedance shall be the internal impedance of the current-type subsystem [22,62,78].

The minor loop gain concept is nowadays applied commonly in assessing the stability and transient performance in interconnected power electronic systems. The concept of forbidden region was launched in Ref. [79], which ensures robust stability of the system if the minor loop gain stays out of the forbidden region. The forbidden region launched by Middlebrook in Refs [77,78] is a circle having radius of inverse of gain margin (GM) and the center at origin, as shown in Figure 1.16. Middlebrook's forbidden region was deemed to be too conservative, that is, occupying unnecessary amount of area in the complex plain [79]. As a consequence, new forbidden regions were developed for reducing the conservatism [79–84] such as ESAC (energy systems analysis consortium) [79], GMPM (gain margin phase margin) [80], and opposing argument [81] criteria illustrated in Figure 1.16.

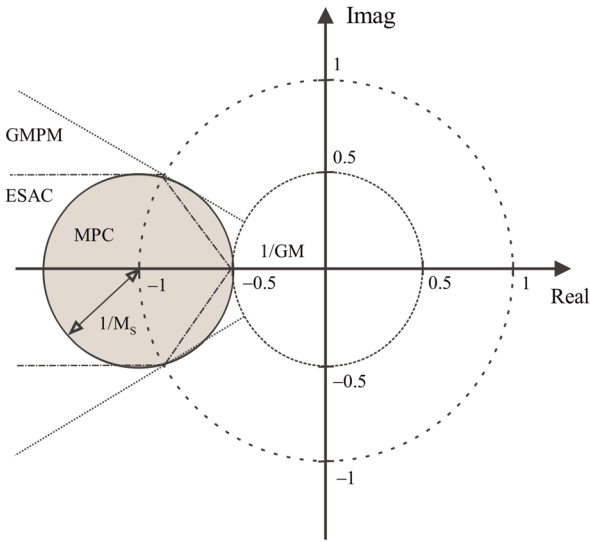


Figure 1.17 Maximum peak criteria (MPC)-based forbidden region versus EASC and GMPM regions [75]. *Source:* Vesti 2013. Reproduced with permission of IEEE.

According to Figure 1.16, all the different criteria aim to maintain robust stability (i.e., acceptable transient performance) by requiring the minor loop gain to satisfy certain PM and GM conditions. Reference [75] proposed a new forbidden region by means of a circle having radius of inverse of maximum peak value allowed in the affected system transfer functions and the center at the point $(-1,0)$ as depicted in Figure 1.17, which outperforms the other earlier launched forbidden regions in terms of occupied area in the complex plain. The forbidden region concept is applicable to DC and AC domain systems as well.

1.6 Time Domain-Based Dynamic Analysis

Time domain-based dynamic analysis and control design are quite common in control engineering [85,86] and are also utilized in conjunction with the grid-connected power electronics applications [87]. The time domain responses do not, however, reveal the origin of the observed transient behavior or how close the system is for instability. Figure 1.18 shows the output-voltage transient behavior of a buck converter when a step change is applied in the load current without (Figure 1.18a) and with the input LC or EMI filters (Figure 1.18b and c). If both the original and EMI filter-affected responses were not known, then it would be very difficult to distinguish between the poor controller design and other external reasons, because the decaying oscillation at the output-voltage response would be similar with low margins (i.e., PM and GM) in the feedback loop.

Figure 1.19 shows the measured output-voltage feedback loop without and with the input EMI filter. According to Figure 1.19, the EMI filter has not caused

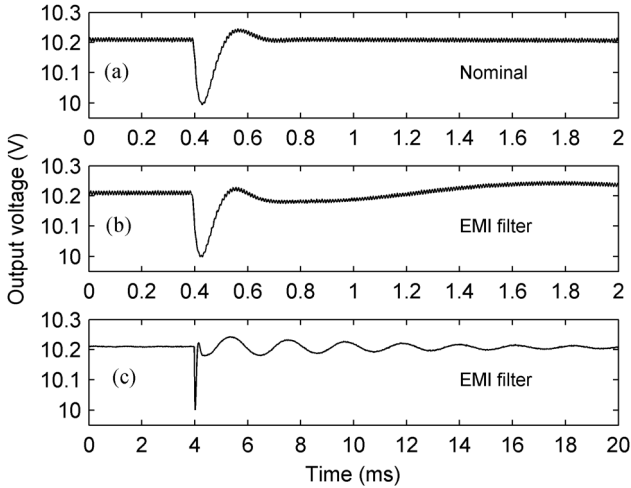


Figure 1.18 Output-voltage response of a buck converter to a step change in load current.

such a change in the feedback loop, which would affect the transient response, that is, the PM and GM are not changed. Figure 1.20 shows the measured closed-loop output impedance of the converter, where the EMI filter has created a resonance, which actually initiates the decaying oscillation at the output-voltage response [88,89]. More specifically, the resonance at the output impedance is caused by the interacting EMI-filter output impedance and short-circuit input impedance of the converter [90].

Figure 1.21 shows that the grid-connected inverter may become unstable when the control bandwidth of the phase locked loop (PLL) is increased under certain grid impedance conditions. PLL is used for synchronizing the inverter to grid. The

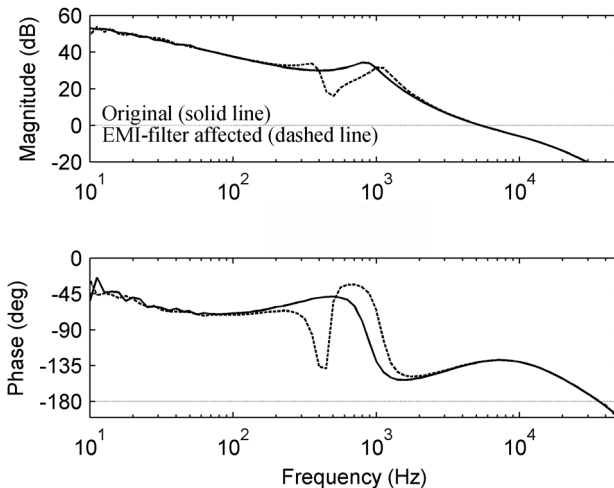


Figure 1.19 The measured original and EMI-filter-affected output-voltage feedback loops.

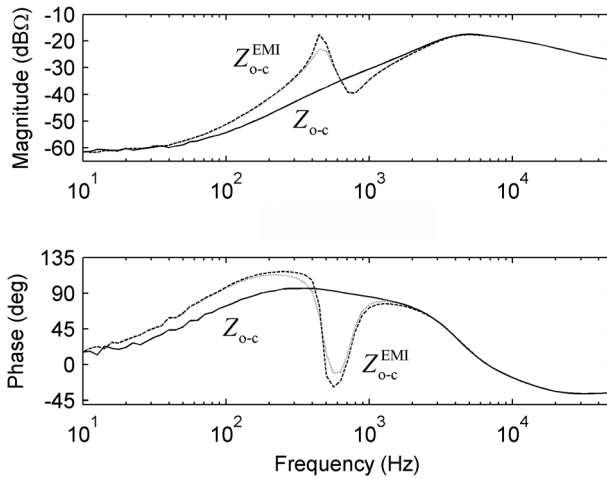


Figure 1.20 Original and EMI-filter-affected closed-loop output impedances.

reason for the instability is the tendency of the inverter output impedance to have negative resistor-like behavior at low frequencies, that is, at the frequencies lower than the PLL crossover frequency [91]. The frequency responses of the inverter output impedance and the grid impedance (Figure 1.22) can be used to reveal explicitly the problems associated with instability phenomenon. The time domain plot does not tell anything about the reasons behind the problem or how much the condition has to change that the instability will vanish or occur again.

It may be quite obvious that the time domain evidence does not suffice to proving the quality of design or the validity of the modifications for removing the problem. The frequency domain evidence will provide a medium to assess the robustness of the design as well as to reveal the risks left in the design for reoccurrence of the “removed” problem.

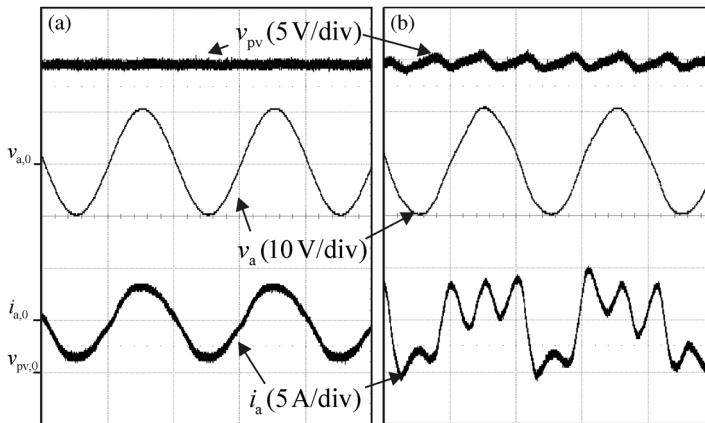


Figure 1.21 Instability of three-phase grid-connected inverter induced by PLL control bandwidth.

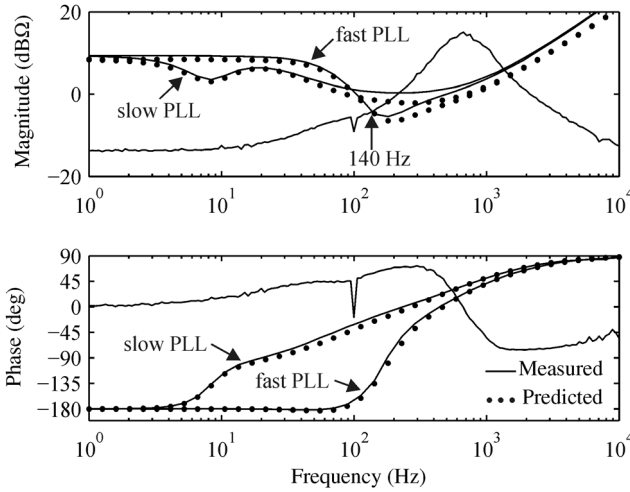


Figure 1.22 Effect of the PLL bandwidth on the inverter output impedance.

1.7 Renewable Energy System Principles

Large-scale utilization of the renewable energy sources such as solar PV, wind, and fuel cells necessitates the use of power electronic converters for providing the grid integration [4]. The solar PV power plants are either constructed by using one DC–AC stage (i.e., single stage) (Figure 1.23) or cascaded by using DC–DC and DC–AC stages (i.e., double stage) (Figure 1.24) [92]. The full-power converter wind energy and fuel cell systems are most often constructed by using double-stage converter schemes according to Figure 1.24 [31,93–95].

The basic operation mode of these systems in terms of grid connection is either grid-parallel (i.e., grid-feeding, grid-supporting) or grid-forming mode [96–98]. In grid-parallel operation mode, the inverter serves as current source, and the grid

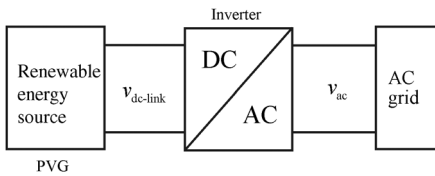


Figure 1.23 Single-stage renewable energy system principle.

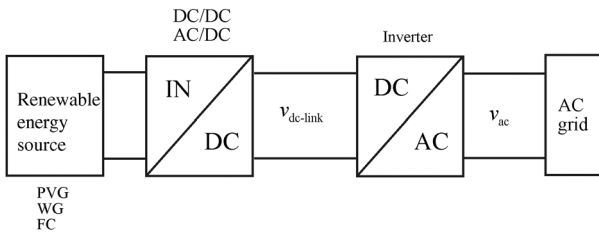


Figure 1.24 Cascaded renewable energy system principle.

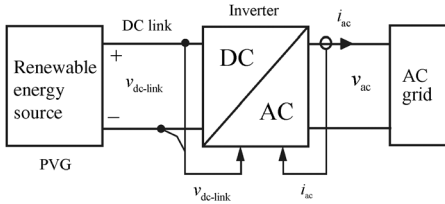


Figure 1.25 Single-stage grid-parallel energy system.

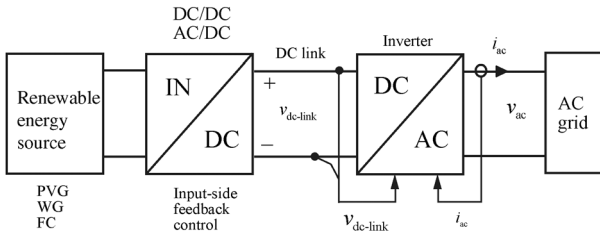


Figure 1.26 Cascaded grid-parallel renewable energy system.

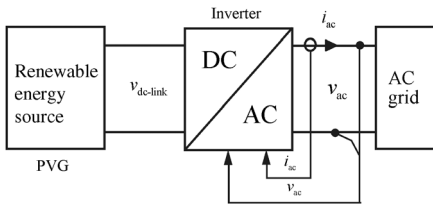


Figure 1.27 Single-stage grid-forming energy system.

determines the level of AC voltage and frequency (Figures 1.25 and 1.26). Usually maximum available power in the renewable energy source is supplied into the grid applying different maximum power point (MPP) tracking algorithms [99–102]. A characteristic of the grid-parallel operation mode is that the outmost feedback loops of the power electronic converters are taken from the input terminal of the converters (see Figures 1.25 and 1.26).

In grid-forming operation mode (i.e., standalone, off-grid, or islanding), the inverter serves as a voltage source taking care of both the voltage level and the frequency (Figures 1.27 and 1.28). The level of output power supplied into the

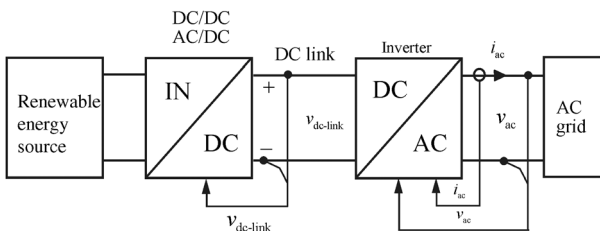


Figure 1.28 Cascaded grid-forming renewable energy system.

system depends on the load of the system. A characteristic of the grid-forming mode is that the outmost feedback loops are taken from the output terminal of the power electronics converters (see Figures 1.27 and 1.28).

The feedback arrangements mean that the power electronic converters in grid-parallel mode are CF/CO converters and in grid-forming mode VF/VO converters. The change of operating mode is usually required in renewable energy systems (i.e., from grid-parallel to grid-forming mode and back). The dynamic behavior of the converters will profoundly change depending on the operation mode, which has to be carefully considered when designing the control systems for ensuring stable operation [97].

1.8 Content Review

The book is divided into four parts as follows: Part One, comprising Chapters 1 and 2, is dedicated to the introduction as well as to the dynamic analysis and control design preliminaries in a generalized manner. Part Two, comprising Chapters 3–6, is dedicated to the dynamics of voltage-fed DC–DC converters. Part Three, comprising Chapters 7–11, is dedicated to the dynamics of current-fed DC–DC converters as well as to the properties of photovoltaic generator and its effects on the interfacing converter dynamics. Part Four, comprising Chapters 12–17, is dedicated to the dynamics and control of grid-connected three-phase VSI-type converters. The content of the subsequent chapters is briefly reviewed in order to clarify the message, which each chapter will deliver.

The conceptual and theoretical basis of the book is provided in Chapter 2 in a simple and practical manner without using difficult mathematical treatments, but at the same time in general form. The same theoretical formulas are repeated in explicit modes in the associated chapters if deemed to be necessary for understanding the message.

In Part Two, the dynamic modeling, analysis, and control of VF converters are treated. Chapter 3 provides the unified dynamic modeling of direct-on-time-controlled converters applied to the basic converters (i.e., buck, boost, and buck–boost) as well as to the superbuck or two-inductor buck converter in the fixed-frequency mode of operation. The dynamic models provided by Chapter 3 are utilized to model the dynamic behavior of the current-mode-controlled converters in Chapter 4. The similarity between PCM and ACM controls is clearly pointed out. The modeling of PCM control is also introduced in case of several simultaneous inductor-current-feedback arrangements as well as when coupled inductors are utilized. The source and load interactions in PCM- and DDR-controlled converters are compared and the origin of the differences is explained. Chapter 5 introduces the modeling of current-output converters based on the models of the VF/VO converters. The source and load interactions as well as impedance-based stability analysis are introduced and compared with the VF/VO converters. Chapter 6 is dedicated for the control design issues in VF converters. The factors affecting the load transient response are explicitly explained, which would facilitate the control design.

In Part Three, the implementation, dynamic modeling, analysis, and control of CF converters are treated. Chapter 7 provides the methods to implement CF

converters applying duality transformation and adding necessary components at the input terminal for satisfying the terminal constraints imposed by the current-type input source. Chapter 8 provides the dynamic models of DDR-controlled basic CF converters implemented by duality-transformation methods or by adding a capacitor at the input terminal of a VF converter. Chapter 9 introduces the dynamic modeling of PCM- and PVM-controlled CF converters. Observed stability problems in conjunction with PCM control applied in PV interfacing converters are explicitly explained. The influence of the PCM and PVM controls in source and load interactions as well as impedance-base stability assessment are explicitly explained. Chapter 10 introduces the characteristics of PV generator as well as the MPP tracking methods and design constraints. Chapter 11 is dedicated to the photovoltaic generator interfacing problematics from the power electronics converter viewpoint, including the PV generator-induced effects on the dynamics of the interfacing converters as well as the associated stability issues.

In Part Four, the dynamic modeling, analysis, and control of grid-connected three-phase VSI-type converters are treated. Chapter 12 provides consistent methods to develop the dynamic models of voltage- and current-fed three-phase PWM inverters in synchronous reference frame (or dq-domain) by utilizing space vector theory. Chapter 13 is dedicated to applying the dynamic models to design the required control functions in an inverter. The effect of different control anomalies caused by the input terminal sources are explicitly treated as well. Chapter 14 introduces reduced-order dynamic modeling of the inverters to relax the high complexity of the inverter dynamics for achieving satisfactory dynamic descriptions applicable for control design. Chapter 15 provides the detailed models for analyzing the closed-loop dynamics of the inverter in multivariable environment. Chapter 16 provides detailed information on the impedance-ratio-based stability assessment methods applying generalized *Nyquist* stability criterion. Chapter 17 is dedicated to the dynamic modeling and control design of three-phase active rectifiers.

References

- 1 Tymerski, R. and Vorpérian, V. (1986) Generation, classification and analysis of switched-mode DC-to-DC converters by the use of converter cells. Proceedings of the IEEE INTELEC, pp. 181–195.
- 2 Tymerski, R. and Vorpérian, V. (1988) Generation and classification of PWM DC-to-DC converters. *IEEE Trans. Aerosp. Electron. Syst.*, **24** (6), 743–754.
- 3 Bose, B.K. (2010) Global warming: energy, environmental pollution, and the impact of power electronics. *IEEE Ind. Electron. Mag.*, **4** (1), 6–17.
- 4 Blaabjerg, F., Chen, Z., and Kjaer, S.B. (2004) Power electronics as efficient interface in dispersed power generation. *IEEE Trans. Power Electron.*, **19** (5), 1184–1194.
- 5 Teodorescu, R., Liserre, M., and Rodriguez, P. (2011) *Grid Converters for Photovoltaic and Wind Power Systems*, John Wiley & Sons, Ltd, Chichester, UK.
- 6 Suntio, T., Puukko, J., Nousiainen, L., Messo, T., and Huusari, J. (2011) Change of paradigm in power electronic converters used in renewable energy

- applications. Proceedings of the IEEE 33rd International Telecommunications Energy Conference, pp. 1–9.
- 7 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters: Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.
 - 8 Lyi, S. and Dougal, R.A. (2002) Dynamic multiphysics model for solar array. *IEEE Trans. Energy Convers.*, **17** (2), 285–294.
 - 9 Nousiainen, L., Puuko, J., Mäki, A., Messo, T., Huusari, J., Jokipii, J., Viinamäki, J., Torres Lobera, D., Valkealahti, S., and Suntio, T. (2013) Photovoltaic generator as an input source for power electronic converters. *IEEE Trans. Power Electron.*, **28** (6), 3028–3038.
 - 10 Suntio, T., Leppäaho, J., Huusari, J., and Nousiainen, L. (2010) Issues on solar-generator interfacing with current-fed MPP-tracking converters. *IEEE Trans. Power Electron.*, **25** (9), 2409–2419.
 - 11 Suntio, T., Huusari, J., and Leppäaho, J. (2010) Issues on solar-generator interfacing with voltage-fed MPP-tracking converters. *Eur. Power Electron. Drives J.*, **20** (3), 40–47.
 - 12 Ali, M.H., Wu, B., and Dougal, R.A. (2010) An overview of SMES applications in power and energy systems. *IEEE Trans. Sustain. Energy*, **1** (1), 38–45.
 - 13 Shmilovitz, D. and Singer, S. (2002) A switched mode converter suitable for superconductive magnetic energy (SMES) systems. Proceedings of the IEEE APEC, pp. 630–634.
 - 14 Suntio, T. (2013) Editorial: special issue on power electronics in photovoltaic applications. *IEEE Trans. Power Electron.*, **28** (6), 2647–2648.
 - 15 Viinamäki, J., Kivimäki, J., Suntio, T., and Hietalahti, L. (2014) Design of boost-power-stage converter for PV generator interfacing. Proceedings of the EPE-ECCE, pp. 1–10.
 - 16 Ho, C., Breuninger, H., Pettersson, S., Escobar, G., Serpa, L.A., and Coccia, A. (2012) Practical design and implementation of an interleaved boost converter using SiC diodes for PV application. *IEEE Trans. Power Electron.*, **27** (6), 2835–2845.
 - 17 Ho, C., Breuninger, H., Pettersson, S., Escobar, G., and Canales, F. (2013) A comparative performance study of an interleaved boost converter using commercial Si and SiC diodes for PV application. *IEEE Trans. Power Electron.*, **28** (1), 289–299.
 - 18 Deboni, H., Lee, S.R., and Nehrir, H. (2009) Direct energy transfer for high efficiency photovoltaic Part I: concepts and hypothesis. *IEEE Trans. Aerosp. Electron. Syst.*, **45** (1), 31–45.
 - 19 Villalva, M.G., de Siqueira, T.G., and Ruppert, E. (2010) Voltage regulation of photovoltaic arrays: small-signal analysis and control design. *IET Power Electron.*, **3** (6), 869–880.
 - 20 Chen, Y.-M., Huang, A.Q., and Yu, X. (2013) A high step-up three-port DC–DC converter for stand-alone PV/battery power systems. *IEEE Trans. Power Electron.*, **28** (11), 5049–5062.
 - 21 Figueros, E., Garcerá, G., Sandía, J., González-Espín, F., and Rubio, J.C. (2009) Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter. *IEEE Trans. Ind. Electron.*, **56** (3), 706–717.

- 22 Suntio, T., Viinamäki, J., Jokipii, J., Messo, T., and Kuperman, A. (2014) Dynamic characteristics of power electronic interfaces. *IEEE J. Emerg. Sel. Top. Power Electron.*, **2** (4), 949–961.
- 23 Williams, B.W. (2013) DC-to-DC converters with continuous input and output power. *IEEE Trans. Power Electron.*, **28** (5), 2307–2316.
- 24 Williams, B.W. (2014) Generation and analysis of canonical switching cell DC-to-DC converters. *IEEE Trans. Ind. Electron.*, **61** (1), 329–346.
- 25 Krein, P. (1998) *Elements of Power Electronics*, Oxford University Press, New York, NY.
- 26 Sahan, B., Vergara, A.N., Henze, N., Engler, A., and Zacharias, P. (2008) A single-stage PV module integrated converter based on a low-power current-source inverter. *IEEE Trans. Ind. Electron.*, **55** (7), 2602–2609.
- 27 Wolfs, P.J. (1993) A current-sourced DC–DC converter derived via the duality principle from half-bridge converter. *IEEE Trans. Ind. Electron.*, **40** (1), 139–144.
- 28 Weaver, W.W. and Krein, P.T. (2007) Analysis and applications of a current-sourced buck converter. Proceedings of the IEEE APEC, pp. 1664–1670.
- 29 Chen, Y. and Smedley, K. (2008) Three-phase boost-type grid-connected inverter. *IEEE Trans. Power Electron.*, **23** (5), 2301–2309.
- 30 Karppanen, M., Arminen, J., Suntio, T., Savela, K., and Simola, J. (2008) Dynamical modeling and characterization of peak-current-mode-controlled superbuck converter. *IEEE Trans. Power Electron.*, **23** (3), 1370–1380.
- 31 Thounthong, P., Davat, B., Raël, S., and Sethakul, P. (2009) Fuel cell high-power applications: an overview of power converters for clean energy conversion technology. *IEEE Ind. Electron. Mag.*, **3** (1), 32–46.
- 32 Marquezini, D.D., Ramos, D.B., Machado, R.Q., and Farret, F.A. (2008) Interaction between proton exchange membrane fuel cells and power converters for AC integration. *IET Renew. Power Gen.*, **2** (3), 151–161.
- 33 Giustiniani, A., Petrone, G., Spagnuolo, G., and Vitelli, M. (2010) Low-frequency current oscillations and maximum power point tracking in grid-connected fuel-cell-based systems. *IEEE Trans. Ind. Electron.*, **57** (6), 2042–2053.
- 34 Gemmen, R.S. (2003) Analysis for the effect of inverter ripple current on fuel cell operating condition. *J. Fluids Eng.*, **125** (3), 576–585.
- 35 Suntio, T., Hankaniemi, M., and Karppanen, M. (2006) Analysing the dynamics of regulated converters. *IEE Proc. Electric Power Appl.*, **153** (6), 905–910.
- 36 Hankaniemi, M., Karppanen, M., and Suntio, T. (2006) Load imposed instability and performance degradation in a regulated converter. *IEE Proc. Electric Power Appl.*, **153** (6), 781–786.
- 37 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Effect of control method on impedance-based interactions in a buck converter. *IEEE Trans. Power Electron.*, **28** (11), 5311–5322.
- 38 Tse, C.K. (1998) *Linear Circuit Analysis*, Addison-Wesley, Harlow, UK.
- 39 Erickson, R.W. and Maksimovic, D. (2001) *Fundamentals of Power Electronics*, Kluwer Academic Publishers, Norwell, MA.
- 40 Suntio, T., Karppanen, M., and Sippola, M. (2008) Methods to characterize open-loop dynamics of current-mode-controlled converters. Proceedings of the IEEE Power Electron, pp. 636–642.

- 41 Batarseh, I. (2004) *Power Electronic Circuits*, John Wiley & Sons, Inc., Hoboken, NJ.
- 42 Choi, B. (2013) *Pulsewidth Modulated DC-to-DC Power Conversion: Circuits, Dynamics, and Control Designs*, John Wiley & Sons, Inc., Hoboken, NJ.
- 43 Ioinovici, A. (2013) *Power Electronics and Energy Conversion Systems, Volume 1, Fundamentals and Hard-Switching Converters*, John Wiley & Sons, Ltd, Chichester, UK.
- 44 Kazimierzczuk, M.K. (2008) *Pulse-Width Modulated DC-DC Power Converters*, John Wiley & Sons, Ltd, Chichester, UK.
- 45 Yazdani, A. and Iravani, R. (2010) *Voltage-Sourced Converters in Power Systems*, John Wiley & Sons, Inc., Hoboken, NJ.
- 46 Bacha, S., Munteanu, I., and Bratcu, A.I. (2014) *Power Electronic Converter Modeling and Control*, Springer, London, UK.
- 47 Zhong, Q.-C. and Hornik, T. (2013) *Control of Inverters in Renewable Energy and Smart Grid Integration*, John Wiley & Sons, Ltd, Chichester, UK.
- 48 Shmilovitz, D. (2006) Gyrator realization based on a capacitive switched cell. *IEEE Trans. Circuits Syst. II Express Briefs*, **53** (12), 1418–1422.
- 49 Desoer, C.A. and Kuh, E.S. (1969) *Basic Circuit Theory*, McGraw-Hill Kogasha, Tokyo, Japan, pp. 444–449.
- 50 Luenberger, D.G. (1992) A double look at duality. *IEEE Trans. Automat. Contr.*, **37** (10), 1474–1482.
- 51 Cuk, S. (1979) General topological properties of switching structures. Proceedings of the IEEE PESC, pp. 109–130.
- 52 Leppäaho, J. and Suntio, T. (2011) Dynamic characteristics of current-fed superbuck converter. *IEEE Trans. Power Electron.*, **26** (1), 200–209.
- 53 Shmilovitz, D. (2005) Application of duality for deriving of current converter topologies. *HAIT J. Science Eng. B*, **2** (3–4), 529–557.
- 54 Leppäaho, J., Nousiainen, L., Puukko, J., Huusari, J., and Suntio, T. (2010) Implementing current-fed converters by adding an input capacitor at the input of voltage-fed converter for interfacing solar generator. Proceedings of the EPE-PEMC'10, pp. 81–88.
- 55 Huusari, J. and Suntio, T. (2012) Interfacing constraints of distributed maximum power point tracking converters in photovoltaic applications. Proceedings of the EPE-PEMC'12, pp. DS3d.1-1–DS31-7.
- 56 Glass, M.C. (1977) Advancements in the design of solar array to battery charge current regulators. Proceedings of the IEEE PESC, pp. 346–350.
- 57 Capel, A., Marpinard, J.C., Jalade, J., and Valentin, M. (1983) Current fed and voltage fed switching dc/dc converters: steady state and dynamic models, their applications in space technology, Proceedings of the IEEE INTELEC, pp. 421–430.
- 58 Kuwabara, K. and Suzuki, T. (1984) A pulse-width controlled dc–dc converter powered by a constant-current source. Proceedings of the IEEE INTELEC, pp. 468–472.
- 59 Xiao, W., Ozog, N., and Dunford, W.G. (2007) Topology study of photovoltaic interface for maximum power point tracking. *IEEE Trans. Ind. Electron.*, **54** (3), 1696–1704.
- 60 Siri, K. (2000) Study of system instability in solar-array-based power systems. *IEEE Trans. Aerosp. Electron. Syst.*, **36** (3), 957–964.

- 61 Leppäaho, J. and Suntio, T. (2014) Characterizing the dynamics of peak-current-mode-controlled buck-power-stage converter in photovoltaic applications. *IEEE Trans. Power Electron.*, **29** (7), 3840–3847.
- 62 Leppäaho, J., Huusari, J., Nousiainen, L., Puukko, J., and Suntio, T. (2011) Dynamic properties and stability assessment of current-fed converters in photovoltaic applications. *IEEE Trans. Ind. Appl.*, **131** (8), 976–984.
- 63 Wester, G.W. and Middlebrook, R.D. (1973) Low-frequency characterization of switched dc–dc converters. *IEEE Trans. Aerosp. Electron. Syst.*, **AES-9** (3), 376–385.
- 64 Middlebrook, R.D. and Čuk, S. (1977) A general unified approach to modeling switching-converter power stages. *Int. J. Electron.*, **42** (6), 521–550.
- 65 Sun, J., Mitchell, D.M., Greuel, M.F., Krein, P.T., and Bass, R.M. (2001) Average modeling of PWM converters in discontinuous modes. *IEEE Trans. Power Electron.*, **16** (4), 482–492.
- 66 Suntio, T. (2006) Unified average and small-signal modeling of direct-on-time control. *IEEE Trans. Ind. Electron.*, **21** (2), 287–295.
- 67 Sun, J. (2002) Small-signal modeling of variable-frequency pulsewidth modulators. *IEEE Trans. Aerosp. Electron. Syst.*, **38** (3), 1104–1108.
- 68 Suntio, T. (2006) Average and small-signal modeling of self-oscillating flyback converter with applied switching delay. *IEEE Trans. Power Electron.*, **21** (2), 479–486.
- 69 Puukko, J. and Suntio, T. (2012) Dynamic properties of a voltage source inverter-based three-phase inverter in photovoltaic application. *IET Renew. Power Gen.*, **6** (6), 381–391.
- 70 Maranesi, P.G., Tavazzi, V., and Varoli, V. (1988) Two-port characterization of PWM voltage regulators at low frequencies. *IEEE Trans. Ind. Electron.*, **35** (3), 444–450.
- 71 Figueres, E., Garcerá, G., Sandia, J., González-Espín, F., and Calvo Rubio, J. (2009) Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter. *IEEE Trans. Ind., Electron.*, **56** (3), 706–717.
- 72 Cvetkovic, I., Jaksic, M.M., Boroyevich, D., Mattavelli, P., Lee, F.C., Shen, Z., Ahmed, S., and Dong, D. (2011) Un-terminated, low-frequency terminal-behavioral d–q model of three-phase converters. Proceedings of the IEEE ECCE, pp. 791–798.
- 73 Puukko, J. and Suntio, T. (2012) Modelling the effect of a non-ideal load in three-phase converter dynamics. *IET Electron. Lett.*, **48** (7), 402–404.
- 74 Messo, T., Jokipii, J., Puukko, J., and Suntio, T. (2014) Determining the value of DC-link capacitance to ensure stable operation of three-phase photovoltaic inverter. *IEEE Trans. Power Electron.*, **29** (2), 665–673.
- 75 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Impedance-based stability and transient-performance assessment applying maximum peak criteria. *IEEE Trans. Power Electron.*, **28** (5), 2099–2104.
- 76 Sun, J. (2011) Impedance-based stability criterion for grid-connected inverters. *IEEE Trans. Power Electron.*, **26** (11), 3075–3078.
- 77 Middlebrook, R.D. (1976) Input filter considerations in design and applications of switching regulators. Proceedings of the IEEE Industry Applications Society Annual Meeting, pp. 91–107.

- 78 Middlebrook, R.D. (1978) Design techniques for preventing input-filter oscillations in switched-mode regulators. Proceedings of the Power Conversion Conference, pp. A3.–A3.16.
- 79 Sudhoff, S.D., Glover, S.F., Lamm, P.T., Schmucker, D.H., and Delisle, D.-E. (2000) Admittance space stability analysis of power electronic systems. *IEEE Trans. Aerosp. Electron. Syst.*, **36** (3), 965–973.
- 80 Wildrick, C.M., Lee, F.C., Cho, B.H., and Choi, B. (1995) A method for defining the load impedance specifications for a stable distributed power system. *IEEE Trans. Power Electron.*, **10** (3), 280–285.
- 81 Feng, X., Liu, J., and Lee, F.C. (2002) Impedance specification for stable DC distributed system. *IEEE Trans. Power Electron.*, **17** (2), 157–162.
- 82 Liu, J., Feng, X., Lee, F.C., and Borojevich, D. (2002) PEBB system stability margin monitoring. *J. Vib. Control*, **8** (2), 261–276.
- 83 Liu, J., Feng, X., Lee, F.C., and Borojevich, D. (2002) Stability margin monitoring using voltage perturbation for DC distributed power systems. *J. Vib. Control*, **8** (2), 277–288.
- 84 Liu, J., Feng, X., Lee, F.C., and Borojevich, D. (2003) Stability margin monitoring for distributed power systems via perturbation approaches. *IEEE Trans. Power Electron.*, **18** (6), 1254–1261.
- 85 Hang, C.C., Åström, K.J., and Ho, W.K. (1991) Refinements of the Ziegler–Nichols tuning formula. *IEE Proc. D*, **138** (2), 11–118.
- 86 Basilio, J.C. and Matos, S.R. (2002) Design of PI and PID controllers with transient performance specification. *IEEE Trans. Educ.*, **45** (4), 364–370.
- 87 Peña-Alzola, R., Liserre, M., Blaabjerg, F., Ordóñez, M., and Yang, Y. (2014) LCL-filter design for robust active damping in grid-connected converters. *IEEE Trans. Ind. Inform.*, **10** (4), 2192–2203.
- 88 Suntio, T. and Karppanen, M. (2009) The short-circuit input impedance as a main source of input-filter interactions in a regulated converter. *Eur. Power Electron. Drives J.*, **19** (3), 31–40.
- 89 Suntio, T. and Kivimäki, J. (2014) Physical insight into the factors affecting the load transient response of a buck converter. Proceedings of the European Conference on Power Electronics and Applications, pp. 1–10.
- 90 Choi, B. (1997) Step load response of a current-mode-controlled DC-to-DC converter. *IEEE Trans. Aerosp. Electron. Syst.*, **33** (4), 1115–1121.
- 91 Messo, T., Jokipii, J., Aapro, A., and Suntio, T. (2014) Time and frequency-domain evidence on the instability caused by impedance-based interactions in three-phase inverters. Proceedings of the European Conference on Power Electronics and Applications, pp. 1–9.
- 92 Blaabjerg, F. and Ma, K. (2013) Future on power electronics for wind turbine systems. *IEEE J. Emerg. Sel. Top. Power Electron.*, **1** (3), 139–152.
- 93 Blaabjerg, F., Liserre, M., and Ma, K. (2012) Power electronics converters for wind turbine systems. *IEEE Trans. Ind. Appl.*, **48** (2), 708–719.
- 94 Chen, Z., Guerrero, J.M., and Flaabjerg, F. (2009) A review of the state of the art of power electronics for wind turbines. *IEEE Trans. Power Electron.*, **24** (8), 1859–1875.

- 95 Romero-Cadaval, E., Spagnuolo, G., Franquelo, L.G., Ramos-Paja, C.-A., Suntio, T., and Xiao, W.-M. (2013) Grid-connected photovoltaic generation plants: components and operation. *IEEE Ind. Electron. Mag.*, 7 (3), 6–20.
- 96 Vasquez, J.C., Guerrero, J.M., Luna, A., Rodríguez, P., and Teodorescu, R. (2009) Adaptive droop control applied to voltage-source inverters operating in grid-connected and islanding modes. *IEEE Trans. Ind. Electron.*, 56 (10), 4088–4096.
- 97 Kwon, J., Yoon, S., and Choi, S. (2012) Indirect current control for seamless transfer of three-phase utility interactive inverters. *IEEE Trans. Power Electron.*, 27 (2), 773–781.
- 98 Serban, E. and Serban, H. (2010) A control strategy for a distributed power generation micro grid applications with voltage- and current-controlled source converter. *IEEE Trans. Power Electron.*, 25 (12), 2981–2992.
- 99 Blaabjerg, F., Teodorescu, R., Liserre, M., and Timbus, A. (2006) Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.*, 53 (5), 1398–1409.
- 100 Konstantopoulos, G.C. and Alexadridis, A.T. (2014) Full-scale modeling, control, and analysis of grid-connected wind turbine induction generators with back-to-back AC/DC/AC converters. *IEEE J. Emerg. Sel. Top. Power Electron.*, 2 (4), 739–748.
- 101 Jain, S. and Agarwal, V. (2007) Comparison of the performance of maximum power point tracking schemes applied to single-stage grid-connected photovoltaic systems. *IET Electr. Power Appl.*, 1 (5), 753–762.
- 102 Subudhi, B. and Pradhan, R. (2013) A comparative study on maximum power point tracking techniques for photovoltaic power systems. *IEEE Trans. Sustain. Energy*, 4 (1), 89–98.

2

Dynamic Analysis and Control Design Preliminaries

2.1 Introduction

This chapter introduces the basics behind the dynamic analysis and control dynamics, defines the concepts of open- and closed-loop systems, and presents the general sets of transfer functions for single-terminal input or output converters as well as for multiterminal input or output converters in matrix, linear network, and control-engineering block diagram forms. The basic dynamic representations are given to correspond to the true internal dynamics of the associated converters. The methods to address the effect of nonideal source and load are introduced in general forms yielding a number of impedance-like special parameters explaining the sensitivity/insensitivity of the associated converter to the source and load interactions. The control-engineering block diagrams are used in their general forms to derive the closed-loop representations for output and input dynamics. The stability and performance indices such as control bandwidth, loop crossover frequency, phase and gain margins, sensitivity and complementary sensitivity functions, and instability, conditional stability, marginal stability, and unconditional stability are reviewed. The stability assessment is also expanded to the impedance-based stability assessment in general form. The meaning and consequences of zeros and poles in the transfer functions are explained. Especially, the right-half-plane zeros and poles are discussed in the light of the control bandwidth constraints they impose.

2.2 Generalized Dynamic Representations – DC–DC

2.2.1 Introduction

The first linear equivalent circuit of a power electronic converter (Figure 2.1) was proposed in the late 1970s in Ref. [1] by Middlebrook. This equivalent circuit is valid only for the voltage-fed second-order DC–DC converters operating in CCM under direct duty ratio control. Similar equivalent circuits can also be developed for higher order converters and for current-fed converters under similar operating conditions. The circuit gives physical insight into the dynamic processes taken place in the converter, and explains well why, for example, the input filter will

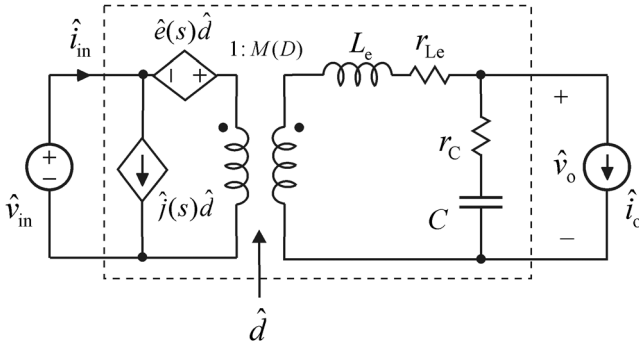


Figure 2.1 Canonical equivalent circuit of a DRR-controlled second-order DC-DC converter.

affect the dynamics of the converter (i.e., the dependent current source at the input terminal). As a consequence, the equivalent circuit was later utilized effectively to develop the input-filter design rules published in Refs [2,3] to prevent the input filter to degrade the transient performance and to cause instability. Middlebrook has later revealed that the design rules were developed utilizing the extra element theorem introduced in Ref. [4].

The above-discussed limitations in its applicability make this kind of equivalent circuits, however, quite useless despite their very attractive properties. Actually, the most important impacts the original design rules have created can be traced to the application of the extra element theorem in terms of the interaction formulation. This formulation reveals that there are a number of special ohmic parameters explaining the dynamic behavior of the power electronic converters [5].

In order to overcome the applicability limitations, a more general equivalent circuit was proposed in Ref. [6] (Figure 2.2) based on the transfer functions of a power electronic converter, that is, on the circuit-theoretic two-port network parameters [7]. It was later noticed [8] that the equivalent circuit shall be constructed in such a way that the source and load effects are removed in the corresponding set of transfer functions for improving the applicability of the equivalent circuit [5]. The usefulness of the network parameter-based equivalent circuits is well recognized [9,10] and their applicability is also well

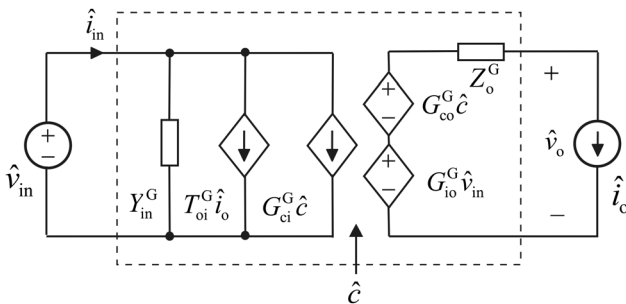


Figure 2.2 Equivalent circuit of a DC-DC converter based on two-port network parameters.

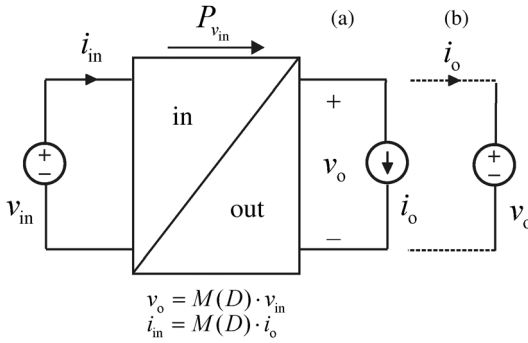


Figure 2.3 VF converter. (a) Voltage-output mode. (b) Current-output mode. Source: Suntio 2014. Reproduced with permission of IEEE.

demonstrated [11–15]. It is also noticed that the same kind of equivalent circuits can be equally utilized in the dynamic analysis of three-phase grid-connected power electronic converters [16–19].

2.2.2 Generalized Dynamic Representations

The generalized treatment of the dynamics of the DC–DC converters is presented in Ref. [20], covering the VF and CF DC–DC converters at voltage- and current-output modes. The dynamic effects that the change of the terminal sources will produce are demonstrated with both developed analytical transfer functions and practical measurements by using a buck power stage as an example.

The set of transfer functions or two-port network parameters describing the small-signal dynamic behavior of the converters in Figures 2.3 and 2.4 is unique for each of the converters as follows [5,7]: The converter in Figure 2.3a shall be represented by G -parameters, the converter in Figure 2.3b by Y -parameters, the converter in Figure 2.4a by H -parameters, and the converter in Figure 2.4b by Z -parameters.

In general, a set of transfer functions of a converter with single-input and single-output terminals can be represented according to Eq. (2.1) using matrix notation with three-variable input vector $[\hat{u}_{in} \ \hat{u}_{out} \ \hat{u}_c]^T$ and two-variable output vector $[\hat{y}_{in} \ \hat{y}_{out}]^T$, where the subscript “in” denotes an input-terminal

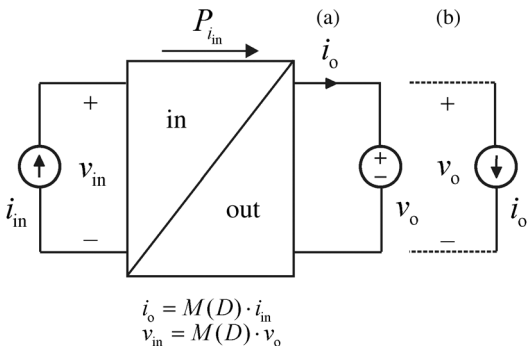


Figure 2.4 CF converter. (a) Current-output mode. (b) Voltage-output mode. Source: Suntio 2014. Reproduced with permission of IEEE.

variable, the subscript “out” designates an output-terminal variable, and the subscript “c” symbolizes the control variable:

$$\begin{bmatrix} \hat{y}_{in} \\ \hat{y}_{out} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & -G_{22} & G_{23} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_{out} \\ \hat{u}_c \end{bmatrix} \quad (2.1)$$

The “^” over the variables denotes small-signal behavior and the Laplace variable is dropped for brevity. Input and output variables can be either voltages or currents depending on the converter application. The sign of the entry corresponding to G_{22} is negative, since the output current flows out of the terminal (opposed to classical definition for the two-port networks [7]). To clarify, consider a battery-powered converter, feeding a microprocessor. Then, \hat{y}_{in} would be battery current, \hat{y}_{out} – microprocessor voltage (controlled variable), \hat{u}_{in} – battery voltage, and \hat{u}_{out} – microprocessor current.

The physical transfer functions in (2.1) can be stated as follows:

$$\begin{aligned} G_{11} &= \frac{\hat{y}_{in}}{\hat{u}_{in}} : \text{Converter input impedance } (Z_{in}) \text{ or admittance } (Y_{in}) \\ G_{12} &= \frac{\hat{y}_{in}}{\hat{u}_{out}} : \text{Reverse transfer function } (T_{oi}) \\ G_{13} &= \frac{\hat{y}_{in}}{\hat{u}_c} : \text{Control-to-input transfer function } (G_{ci}) \\ G_{21} &= \frac{\hat{y}_{out}}{\hat{u}_{in}} : \text{Forward transfer function } (G_{io}) \text{ (also known as audiosusceptibility)} \\ G_{22} &= \frac{\hat{y}_{out}}{\hat{u}_{out}} : \text{Converter output impedance } (Z_o) \text{ or admittance } (Y_o) \\ G_{23} &= \frac{\hat{y}_{out}}{\hat{u}_c} : \text{Control-to-output transfer function } (G_{co}) \end{aligned}$$

The set of the generalized network parameters in Eq. (2.1) cannot be represented as a generalized linear equivalent circuit corresponding to Figure 2.2 since the entry elements G_{11} and G_{22} are either impedance or admittance types requiring their connection either in series or parallel with the corresponding controlled source elements, as illustrated in Figure 2.2.

2.2.3 Generalized Closed-Loop Dynamics

According to control engineering principles [5], only one of the output system variables may be independently controlled since there is a single control input. This yields two different sets of closed-loop transfer functions as follows: Under input-side feedback control, the closed-loop system (cf. Figure 2.5) can be represented as

$$\begin{bmatrix} \hat{y}_{in} \\ \hat{y}_{out} \end{bmatrix} = \begin{bmatrix} \frac{G_{11-o}}{1+L_{in}} & \frac{G_{12-o}}{1+L_{in}} & \frac{L_{in}}{G_{se-in}(1+L_{in})} \\ \frac{G_{21-o}+L_{in}G_{21-\infty}}{1+L_{in}} & -\frac{G_{22-o}+L_{in}G_{22-\infty}}{1+L_{in}} & \frac{G_{23-o}L_{in}}{G_{se-in}G_{13-o}(1+L_{in})} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_{out} \\ \hat{u}_{r-in} \end{bmatrix}, \quad (2.2)$$

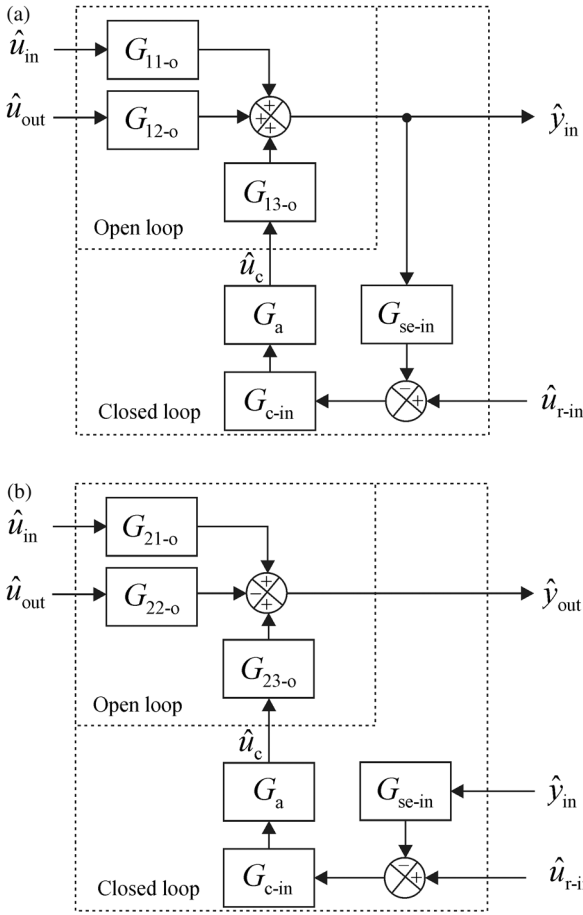


Figure 2.5 General control-engineering block diagrams for the input-side feedback control. (a) Input dynamics. (b) Output dynamics. Source: Suntio 2014. Reproduced with permission of IEEE.

with

$$G_{21-\infty} = G_{21-o} - \frac{G_{11-o}G_{23-o}}{G_{13-o}} \quad (2.3)$$

and

$$G_{22-\infty} = G_{22-o} + \frac{G_{12-o}G_{23-o}}{G_{13-o}}, \quad (2.4)$$

where $L_{in} = G_{se-in}G_aG_{c-in}G_{13-o}$ is the input-side loop gain, G_{se-in} the input-side sensor gain, G_a the modulator gain, G_{c-in} the input-side controller transfer function, and the input-variable \hat{u}_{r-in} is the reference for the controlled variable (see Figure 2.5). Transfer functions $G_{21-\infty}$ and $G_{22-\infty}$ are referred to as “ideal” output-side transfer functions. The subscript extension “-o” denotes the open-loop transfer function.

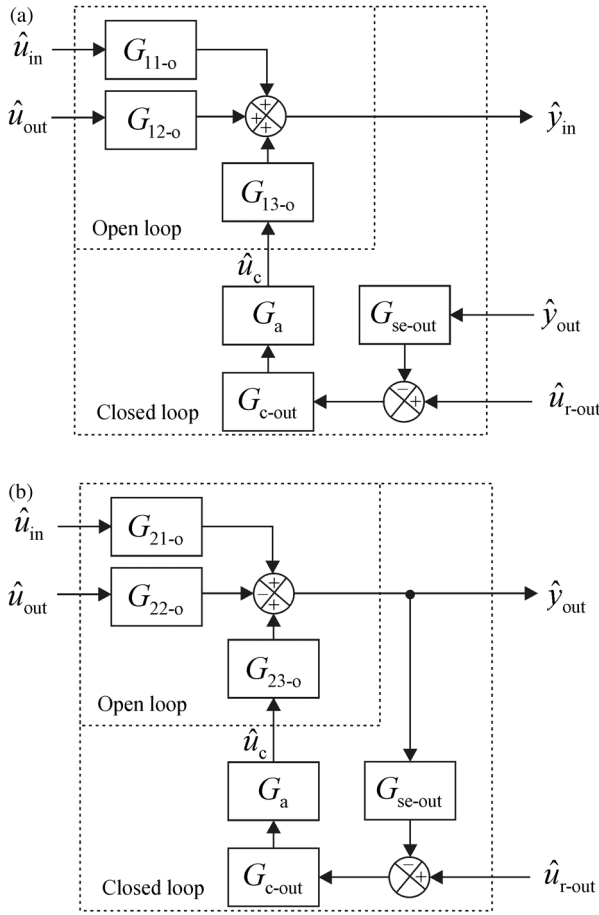


Figure 2.6 General control-engineering block diagrams for the output-side feedback control. (a) Input dynamics. (b) Output dynamics. Source: Suntiö 2014. Reproduced with permission of IEEE.

Under output-side feedback control, the closed-loop system (cf. Figure 2.6) can be represented as follows:

$$\begin{bmatrix} \hat{y}_{in} \\ \hat{y}_{out} \end{bmatrix} = \begin{bmatrix} \frac{G_{11-o} + L_{out}G_{11-\infty}}{1 + L_{out}} & \frac{G_{12-o} + L_{out}G_{12-\infty}}{1 + L_{out}} & \frac{G_{13-o}L_{out}}{G_{se-out}G_{23-o}(1 + L_{out})} \\ \frac{G_{21-o}}{1 + L_{out}} & -\frac{G_{22-o}}{1 + L_{out}} & \frac{L_{out}}{G_{se-out}(1 + L_{out})} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_{out} \\ \hat{u}_{r-out} \end{bmatrix}, \quad (2.5)$$

with

$$G_{11-\infty} = G_{11-o} - \frac{G_{21-o}G_{13-o}}{G_{23-o}} \quad (2.6)$$

and

$$G_{12-\infty} = G_{12-o} + \frac{G_{22-o}G_{13-o}}{G_{23-o}}, \quad (2.7)$$

where $L_{\text{out}} = G_{\text{se-out}} G_a G_{\text{c-out}} G_{23-0}$ is the output-side loop gain, $G_{\text{se-out}}$ is the output-side sensor gain, $G_{\text{c-out}}$ is the output-side controller transfer function, and the output-variable $\hat{u}_{\text{r-out}}$ denotes the reference for the controlled variable (cf. Figure 2.6). Transfer functions $G_{11-\infty}$ and $G_{12-\infty}$ are referred to as “ideal” input-side transfer functions.

“Ideal” transfer functions defined in Eqs. (2.3, 2.4, 2.6) and (2.7) preserve their values regardless of the state of feedback (i.e., they can be formed by open-loop quantities only). According to Eqs. (2.2) and (2.5), the ideal transfer functions determine the low-frequency behavior of the corresponding closed-loop transfer functions (or generally in the frequency range, where the corresponding loop gains are sufficiently high). The low-frequency value of the ideal transfer function defined in Eq. (2.4) resembles a pure resistor due to the constant-type power output of the converter [20]. The low-frequency value of the ideal transfer function defined in Eq. (2.6) resembles a negative resistor due to the constant-type power input [5]. The constant-type power input or output means that an increase or a decrease in the corresponding terminal voltage causes such a decrease or increase in the terminal current that the terminal power will remain the same due to the feedback control of the other terminal. It is interesting to note that $G_{11-\infty}$ is usually the reason for the input filter instability phenomenon [5].

2.2.4 Generalized Cascaded Control Schemes

In many applications, cascaded control schemes are used, where, for example, the output-current feedback loop forms the inner feedback loop, and the input-voltage feedback loop forms the outer feedback loop [19,21,22]. In the rectifier operation, the input-current feedback loop forms the inner feedback loop, and the output-voltage feedback loop forms the outer feedback loop, as shown in Figure 2.7 (i.e., the DC–DC converter). The general formulations for the above-described cases are given in this section.

The analysis of cascaded control schemes is twofold: First the closed-loop transfer functions induced by the closed inner feedback loop have to be developed. The set of these transfer functions forms the open-loop set of transfer functions for developing the closed-loop transfer functions induced by the closing of the outer feedback loop.

For the case where the output-side feedback loop forms the inner loop and the input-side feedback loop forms the outer loop, the inner-loop-induced set of

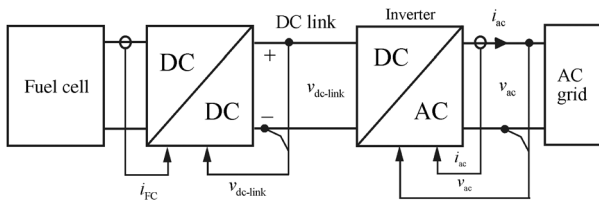


Figure 2.7 Cascade-controlled fuel-cell grid integration.

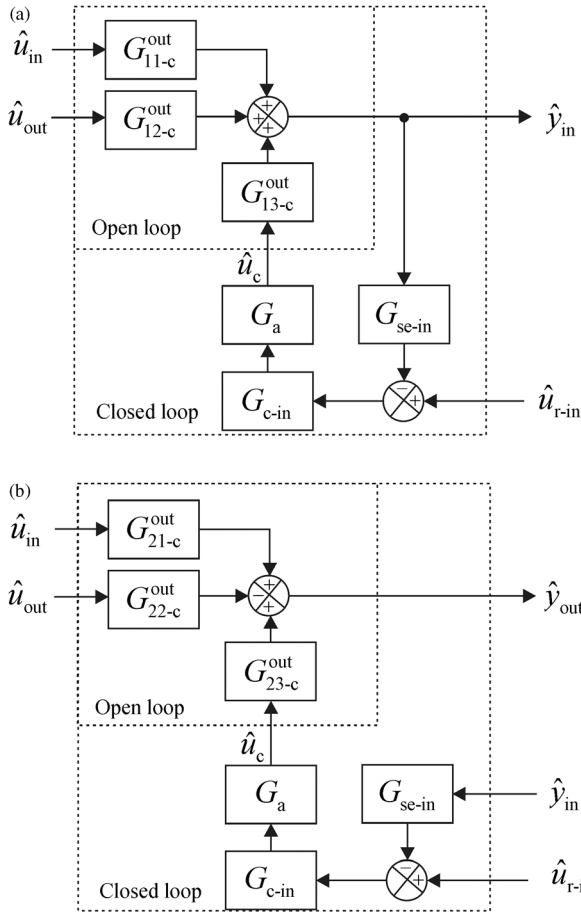


Figure 2.8 General control-engineering block diagrams for the cascaded input-output-side feedback control. (a) Input dynamics. (b) Output dynamics.

transfer functions are given in Section 2.2.3 in Eqs. (2.5)–(2.7), and illustrated in Figure 2.6. The corresponding set of closed-loop transfer functions, when both of the feedback loops are closed, yields (cf. Figure 2.8)

$$\begin{bmatrix} \hat{y}_{in} \\ \hat{y}_{out} \end{bmatrix} = \begin{bmatrix} \frac{G_{11-c}^{out}}{1+L_{in}} & \frac{G_{12-c}^{out}}{1+L_{in}} & \frac{L_{in}}{G_{se-in}(1+L_{in})} \\ \frac{G_{21-c}^{out} + L_{in}G_{31-\infty}^{out}}{1+L_{in}} & -\frac{G_{22-o}^{out} + L_{in}G_{22-\infty}^{out}}{1+L_{in}} & \frac{G_{23-c}^{out}L_{in}}{G_{se-in}G_{13-c}^{out}(1+L_{in})} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_{out} \\ \hat{u}_{r-in} \end{bmatrix}, \quad (2.8)$$

$$\begin{bmatrix} \hat{y}_{in} \\ \hat{y}_{out} \end{bmatrix} = \begin{bmatrix} \frac{G_{11-o} + L_{out}G_{11-\infty}}{(1+L_{out})(1+L_{in})} & \frac{G_{12-o} + L_{out}G_{12-\infty}}{(1+L_{out})(1+L_{in})} & \frac{L_{in}}{G_{se-in}(1+L_{in})} \\ \frac{(G_{21-o}/1+L_{out}) + L_{in}G_{21-\infty}}{1+L_{in}} & -\frac{(G_{22-o}/(1+L_{out})) + L_{in}G_{22-\infty}}{1+L_{in}} & \frac{G_{23-o}L_{in}}{G_{se-in}G_{13-o}(1+L_{in})} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_{out} \\ \hat{u}_{r-in} \end{bmatrix}, \quad (2.9)$$

with

$$G_{11-\infty} = G_{11-o} - \frac{G_{21-o}G_{13-o}}{G_{23-o}}, \quad (2.10)$$

$$G_{12-\infty} = G_{12-o} + \frac{G_{22-o}G_{13-o}}{G_{23-o}}, \quad (2.11)$$

$$G_{21-\infty} = G_{21-o} - \frac{G_{11-o}G_{23-o}}{G_{13-o}}, \quad (2.12)$$

and

$$G_{22-\infty} = G_{22-o} + \frac{G_{12-o}G_{23-o}}{G_{13-o}}, \quad (2.13)$$

where $L_{in} = G_{se-in}G_aG_{c-in}(G_{13-o}/G_{se-out}G_{23-o}) \cdot (L_{out}/(1+L_{out}))$ is the input-side loop gain, G_{se-in} is the input-side sensor gain, G_a is the modulator gain, G_{c-in} is the input-side controller transfer function, and the input-variable \hat{u}_{r-in} is the reference for the controlled variable (cf. Figure 2.8). The transfer functions G_{ij-o} are the original open-loop transfer functions derived for the converter. The ideal transfer functions $G_{ij-\infty}$ in Eqs. (2.10)–(2.13) are same as defined earlier in Section 2.2.3.

For the case, where the input-side feedback loop forms the inner loop and the output-side feedback loop forms the outer loop, the inner-loop-induced set of transfer functions are given in Section 2.2.3 in Eqs. (2.2)–(2.4) and illustrated in Figure 2.5. The corresponding set of closed-loop transfer functions, when both of the feedback loops are closed, yields (cf. Figure 2.9)

$$\begin{bmatrix} \hat{y}_{in} \\ \hat{y}_{out} \end{bmatrix} = \begin{bmatrix} \frac{G_{11-c}^{in} + L_{out}G_{11-\infty}^{in}}{1+L_{out}} & \frac{G_{12-o}^{in} + L_{out}G_{12-\infty}^{in}}{1+L_{out}} & \frac{G_{13-o}^{in}L_{out}}{G_{se-out}G_{23-o}^{in}(1+L_{out})} \\ \frac{G_{21-c}^{in}}{1+L_{out}} & -\frac{G_{22-c}^{in}}{1+L_{out}} & \frac{L_{out}}{G_{se-out}(1+L_{out})} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_{out} \\ \hat{u}_{r-out} \end{bmatrix}, \quad (2.14)$$

$$\begin{bmatrix} \hat{y}_{in} \\ \hat{y}_{out} \end{bmatrix} = \begin{bmatrix} \frac{(G_{11-o}/1+L_{in}) + L_{out}G_{11-\infty}}{1+L_{out}} & \frac{(G_{12-o}/(1+L_{in})) + L_{out}G_{12-\infty}}{1+L_{out}} & \frac{G_{13-o}L_{out}}{G_{se-out}G_{23-o}(1+L_{out})} \\ \frac{G_{21-o} + L_{out}G_{21-\infty}}{(1+L_{out})(1+L_{in})} & -\frac{G_{22-o} + L_{out}G_{22-\infty}}{(1+L_{out})(1+L_{in})} & \frac{L_{out}}{G_{se-out}(1+L_{out})} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_{out} \\ \hat{u}_{r-out} \end{bmatrix}, \quad (2.15)$$

where $L_{out} = G_{se-out}G_aG_{c-out}(G_{23-o}/G_{se-in}G_{13-o}) \cdot (L_{in}/(1+L_{in}))$ is the input-side loop gain, G_{se-out} is the output-side sensor gain, G_a is the modulator gain, G_{c-out} is the input-side controller transfer function, and the input variable \hat{u}_{r-out} is the reference for the controlled variable (cf. Figure 2.9). The transfer functions G_{ij-o} are the original open-loop transfer functions derived for the converter. The ideal transfer functions $G_{ij-\infty}$ are same as defined earlier in Eqs. (2.10)–(2.13) and in Section 2.2.3.

The above-described cascaded control schemes assumed that the cascaded feedback variables are located at the opposite terminals. There are, however, situations, where both of the feedback-controlled variables locate at the same terminals. Such applications are, for example, the different storage battery charging applications, where the charging current and also the charging voltage have to be limited for preventing the storage battery or the charging converter

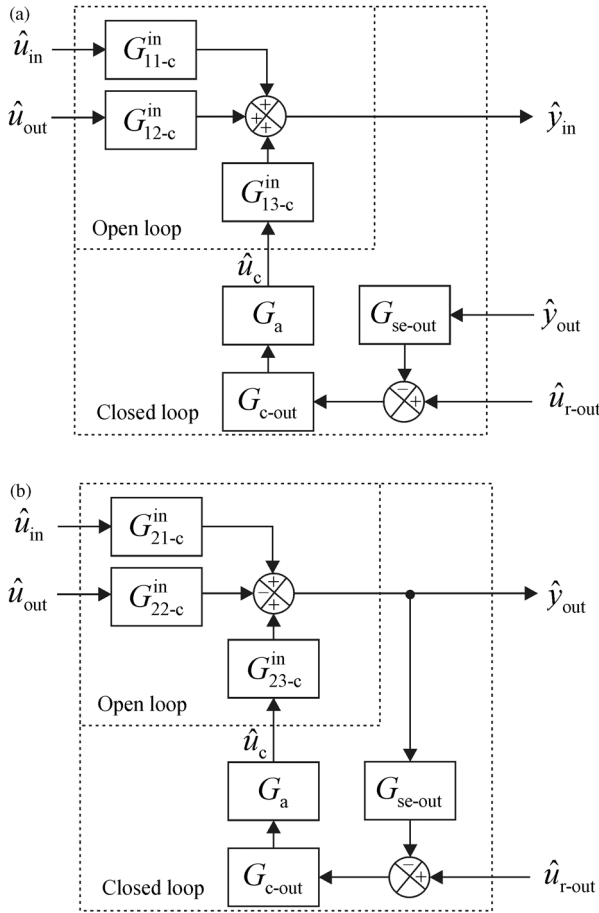


Figure 2.9 General control-engineering block diagrams for the cascaded output-input-side feedback control. (a) Input dynamics. (b) Output dynamics.

from being damaged (cf. Figures 2.10 and 2.11) [5,21–23]. The controlling of such application can be implemented in two ways: There can be two separate controllers (i.e., one for the current and another for the voltage) running at the same time in such a way that the controller determining the minimum pulsewidth would overdrive the other controller and thus perform the control action. In such a case, the control system is always a single-loop system treated in detail in Section 2.3.3. If the control system is implemented in a cascaded manner

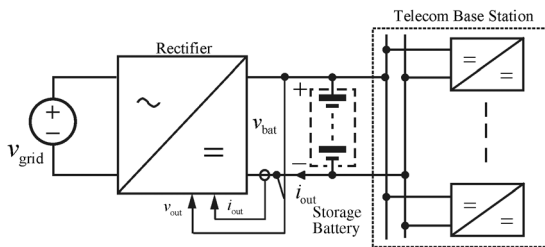


Figure 2.10 Telecom DC UPS system.

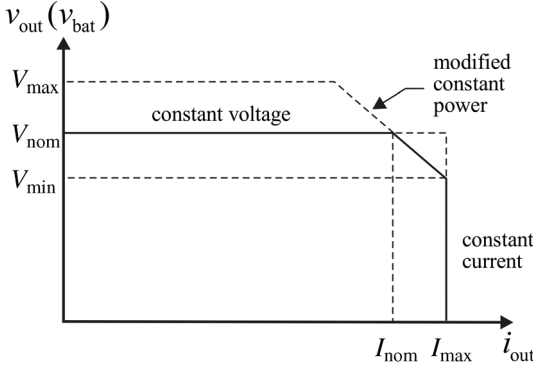


Figure 2.11 Rectifier output voltage characteristics, where the inner feedback loop is the output voltage, and the outer feedback loop is the output current.

as described in Ref. [21], then the dynamic analysis is more complicated, because the output modes of the converter under both of the feedback arrangements are not the same. Therefore, the dynamic representation induced by the closed inner feedback loop has to be transformed to correspond to the output mode of the outer feedback loop before computing the overall closed-loop transfer functions.

The set of closed-loop transfer functions induced by the closed inner feedback loop is given in Eq. (2.16), where the superscript “A” denotes the output mode of the converter when the inner feedback loop is only active (i.e., the mode is voltage). The outer feedback loop requires the change of the output mode, because it will use the feedback variable, which is the input variable of the other mode (i.e., the output mode is current). The mode change can be performed changing the named variables as follows: $\hat{y}_{out}^B = \hat{u}_{out}^A$ and $\hat{u}_{out}^B = \hat{y}_{out}^A$, where the superscript “B” denotes the output mode determined by the outer feedback loop. By performing the change of variables, the new set of transfer functions can be given as described in Eqs. (2.17) and (2.18) as function of the original closed-loop transfer functions. The overall closed-loop set of transfer functions can be obtained as defined earlier in Section 2.2.3 (i.e., Eqs. (2.5)–(2.7) and Figure 2.5) based on the transfer functions given in Eq. (2.18).

$$\begin{bmatrix} \hat{y}_{in}^A \\ \hat{y}_{out}^A \end{bmatrix} = \begin{bmatrix} G_{11}^A & G_{12}^A & G_{13}^A \\ G_{21}^A & -G_{22}^A & G_{23}^A \end{bmatrix} \begin{bmatrix} \hat{u}_{in}^A \\ \hat{u}_{out}^A \\ \hat{u}_c^A \end{bmatrix}. \quad (2.16)$$

$$\begin{bmatrix} \hat{y}_{in}^B \\ \hat{y}_{out}^B \end{bmatrix} = \begin{bmatrix} G_{11}^B & G_{12}^B & G_{13}^B \\ G_{21}^B & -G_{22}^B & G_{23}^B \end{bmatrix} \begin{bmatrix} \hat{u}_{in}^B \\ \hat{u}_{out}^B \\ \hat{u}_c^B \end{bmatrix}. \quad (2.17)$$

$$\begin{bmatrix} \hat{y}_{in}^B \\ \hat{y}_{out}^B \end{bmatrix} = \begin{bmatrix} G_{11}^A + \frac{G_{21}^A G_{12}^A}{G_{22}^A} & -\frac{G_{12}^A}{G_{22}^A} & G_{13}^A + \frac{G_{23}^A G_{12}^A}{G_{22}^A} \\ \frac{G_{21}^A}{G_{22}^A} & -\frac{1}{G_{22}^A} & \frac{G_{23}^A}{G_{22}^A} \end{bmatrix} \begin{bmatrix} \hat{u}_{in}^B \\ \hat{u}_{out}^B \\ \hat{u}_c^B \end{bmatrix}. \quad (2.18)$$

2.2.5 Generalized Source and Load Interactions

The input and output terminal sources contain, in practice, finite-source impedance, which may significantly affect the dynamic performance of the converter in terms of transient behavior and stability [5]. The formulation of the source–load interactions given below follows the formulation introduced in the extra element method described in Ref. [4], which actually reveals the explicit ohmic special parameters and which are vital for understanding the existence of the interactions.

The general form of source–converter interaction can be determined based on Figure 2.12, where the converter subsystem **C** is connected in series with the source subsystem **S**, containing either voltage or current source with an internal impedance/admittance denoted by S_{22} . Input, output, and intermediate system variables of the cascaded connection are denoted by $(\hat{u}_{in1}, \hat{u}_{out2}, \hat{u}_c)$, $(\hat{y}_{in1}, \hat{y}_{out2})$, and (\hat{u}_s, \hat{y}_s) , respectively, while input, output, and intermediate electrical variables are symbolized by $(\hat{v}_{in1}, \hat{i}_{in1})$, $(\hat{v}_{out1} = \hat{v}_{in2}, \hat{i}_{out1} = \hat{i}_{in2})$, and $(\hat{v}_{out2}, \hat{i}_{out2})$, respectively. Each electrical variable may serve as either input or output system variable.

Dynamic representations of the source and the converter are given by (see the end of this section for developing the source model)

$$\begin{aligned} \begin{bmatrix} \hat{y}_{in1} \\ \hat{y}_s \end{bmatrix} &= \begin{bmatrix} 0 & 1 \\ 1 & -S_{22} \end{bmatrix} \begin{bmatrix} \hat{u}_{in1} \\ \hat{u}_s \end{bmatrix} \\ \begin{bmatrix} \hat{u}_s \\ \hat{y}_{out2} \end{bmatrix} &= \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & -G_{22} & G_{23} \end{bmatrix} \begin{bmatrix} \hat{y}_s \\ \hat{u}_{out2} \\ \hat{u}_c \end{bmatrix} \end{aligned} \quad (2.19)$$

and the source–converter coupled system dynamics is then obtained as

$$\begin{bmatrix} \hat{y}_{in1} \\ \hat{y}_{out2} \end{bmatrix} = \begin{bmatrix} \frac{G_{11}}{1 + S_{22}G_{11}} & \frac{G_{12}}{1 + S_{22}G_{11}} & \frac{G_{13}}{1 + S_{22}G_{11}} \\ \frac{G_{21}}{1 + S_{22}G_{11}} & -\frac{1 + S_{22}G_{11-xo}}{1 + S_{22}G_{11}}G_{22} & \frac{1 + S_{22}G_{11-\infty}}{1 + S_{22}G_{11}}G_{23} \end{bmatrix} \begin{bmatrix} \hat{u}_{in1} \\ \hat{u}_{out2} \\ \hat{u}_c \end{bmatrix} \quad (2.20)$$

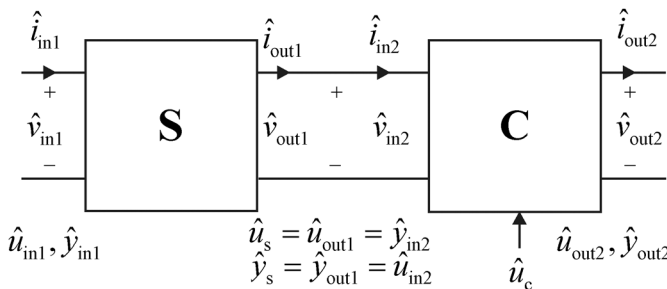


Figure 2.12 Cascaded connection of source **S** and converter **C**. *Source:* Suntio 2014. Reproduced with permission of IEEE.

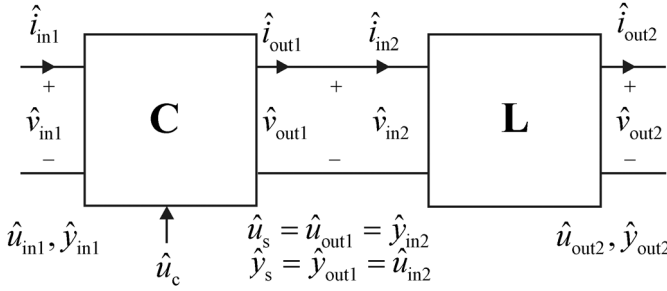


Figure 2.13 Cascaded connection of converter **C** and load **L**. *Source:* Suntio 2014. Reproduced with permission of IEEE.

with

$$G_{11-xo} = G_{11-sco} = G_{11-oco} = G_{11} + \frac{G_{12}G_{21}}{G_{22}}. \quad (2.21)$$

Transfer function G_{11-xo} denotes the impedance/admittance characteristics of the input terminal, when the output terminal is either short circuited (sco) or open circuit (oco) depending on the nature of the ideal load (i.e., the output is terminated with the inverse of the internal impedance of the ideal output load).

The general form of converter–load interaction can be determined based on Figure 2.13, where the converter subsystem **C** is connected in series with the load subsystem **L** containing either voltage or current sink with an internal impedance/admittance denoted by L_{11} .

The coupled system input, output, and intermediate variables are the same as defined above. Dynamic representation of the converter and the load are given by (see the end of this section for developing the load model)

$$\begin{aligned} \begin{bmatrix} \hat{y}_{in1} \\ \hat{y}_s \end{bmatrix} &= \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & -G_{22} & G_{23} \end{bmatrix} \begin{bmatrix} \hat{u}_{in1} \\ \hat{u}_s \\ \hat{u}_c \end{bmatrix} \\ \begin{bmatrix} \hat{u}_s \\ \hat{y}_{out2} \end{bmatrix} &= \begin{bmatrix} L_{11} & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \hat{y}_s \\ \hat{u}_{out2} \end{bmatrix} \end{aligned} \quad (2.22)$$

and the converter–load coupled system dynamics is then obtained as

$$\begin{bmatrix} \hat{y}_{in1} \\ \hat{y}_{out2} \end{bmatrix} = \begin{bmatrix} \frac{1 + L_{11}G_{22-xi}}{1 + L_{11}G_{22}} G_{11} & \frac{G_{12}}{1 + L_{11}G_{22}} & \frac{1 + L_{11}G_{22-\infty}}{1 + L_{11}G_{22}} G_{13} \\ \frac{G_{21}}{1 + L_{11}G_{22}} & -\frac{G_{22}}{1 + L_{11}G_{22}} & \frac{G_{23}}{1 + L_{11}G_{22}} \end{bmatrix} \begin{bmatrix} \hat{u}_{in1} \\ \hat{u}_{out2} \\ \hat{u}_c \end{bmatrix} \quad (2.23)$$

with

$$G_{22-xi} = G_{22-sci} = G_{22-oci} = G_{22} + \frac{G_{12}G_{21}}{G_{11}}. \quad (2.24)$$

Transfer function G_{22-xi} denotes the impedance/admittance characteristics of the output terminal, when the input terminal is either short circuited (sci) or open

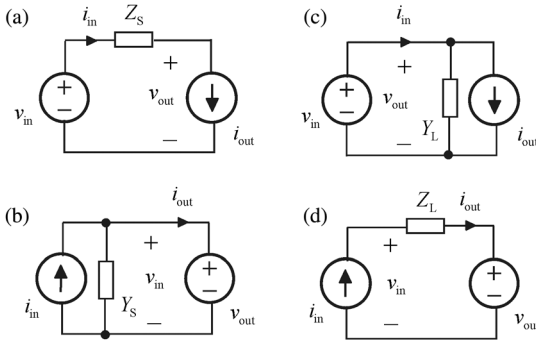


Figure 2.14 Different nonideal input sources (a) and (b) as well as output loads (c) and (d). Source: Suntio 2014. Reproduced with permission of IEEE.

circuit (oci) depending on the nature of the ideal input source (i.e., the output is terminated with the inverse of the internal impedance of the ideal input source).

The nonideal source and load arrangements used in Eqs. (2.19) and (2.22) for obtaining the general dynamic descriptions for source- and load-affected transfer functions are shown in Figure 2.14. The simultaneous equations for solving the output variables as a function of the input variables can be given based on Figure 2.14 as follows: (a) Eq. (2.25), (b) Eq. (2.26), (c) Eq. (2.27), and (d) Eq. (2.28):

$$\begin{cases} i_{in} = i_{out} \\ v_{out} = v_{in} - Z_s i_{out} \end{cases} \rightarrow \begin{bmatrix} i_{in} \\ v_{out} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & -Z_s \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{out} \end{bmatrix}. \quad (2.25)$$

$$\begin{cases} v_{in} = v_{out} \\ i_{out} = i_{in} - Y_s v_{out} \end{cases} \rightarrow \begin{bmatrix} v_{in} \\ i_{out} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & -Y_s \end{bmatrix} \begin{bmatrix} i_{in} \\ v_{out} \end{bmatrix}. \quad (2.26)$$

$$\begin{cases} i_{in} = Y_L v_{in} + i_{out} \\ v_{out} = v_{in} \end{cases} \rightarrow \begin{bmatrix} i_{in} \\ v_{out} \end{bmatrix} = \begin{bmatrix} Y_L & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{out} \end{bmatrix}. \quad (2.27)$$

$$\begin{cases} v_{in} = Z_L i_{in} + v_{out} \\ i_{out} = i_{in} \end{cases} \rightarrow \begin{bmatrix} v_{in} \\ i_{out} \end{bmatrix} = \begin{bmatrix} Z_L & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_{in} \\ v_{out} \end{bmatrix}. \quad (2.28)$$

2.2.6 Generalized Impedance-Based Stability Assessment

A general interconnected system is given in Figure 2.15, where **S** denotes the source-side subsystem, merging the dynamics of the upstream system, and **L** is

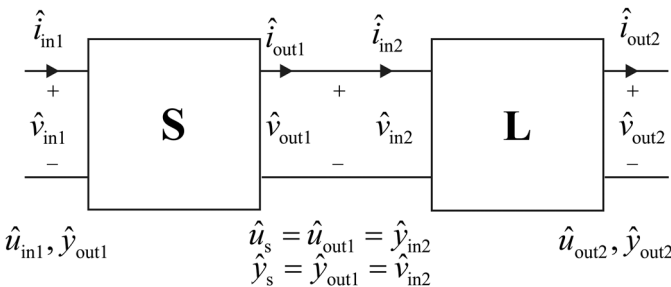


Figure 2.15 Cascaded connection of general-source **S** and load **L** subsystems. Source: Suntio 2014. Reproduced with permission of IEEE.

the load-side subsystem, merging the dynamics of the downstream system. The subsystems can be represented as

$$\begin{bmatrix} \hat{y}_{in\ 1} \\ \hat{y}_s \\ \hat{u}_s \\ \hat{y}_{out\ 2} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & -S_{22} \\ L_{11} & L_{12} \\ L_{21} & -L_{22} \end{bmatrix} \begin{bmatrix} \hat{u}_{in\ 1} \\ \hat{u}_s \\ \hat{y}_s \\ \hat{u}_{out\ 2} \end{bmatrix} \quad (2.29)$$

and the control variable \hat{u}_c is set to zero without loss of generality.

Stability of the interconnected system can be assessed by first computing the mappings from the system input variables ($\hat{u}_{in\ 1}$, $\hat{u}_{out\ 2}$) to the intermediate variables (\hat{u}_s , \hat{y}_s):

$$\begin{bmatrix} \hat{u}_s \\ \hat{y}_s \end{bmatrix} = \begin{bmatrix} \frac{S_{21}L_{11}}{1 + S_{22}L_{11}} & \frac{L_{12}}{1 + S_{22}L_{11}} \\ \frac{S_{21}}{1 + S_{22}L_{11}} & -\frac{S_{22}L_{12}}{1 + S_{22}L_{11}} \end{bmatrix} \begin{bmatrix} \hat{u}_{in\ 1} \\ \hat{u}_{out\ 2} \end{bmatrix} \quad (2.30)$$

and then to the system output variables ($\hat{y}_{in\ 1}$, $\hat{y}_{out\ 2}$)

$$\begin{bmatrix} \hat{y}_{in\ 1} \\ \hat{y}_{out\ 2} \end{bmatrix} = \begin{bmatrix} S_{11} + \frac{S_{12}S_{21}L_{11}}{1 + S_{22}L_{11}} & \frac{S_{12}L_{12}}{1 + S_{22}L_{11}} \\ \frac{S_{21}L_{21}}{1 + S_{22}L_{11}} & -\left(L_{12} + \frac{S_{12}S_{22}L_{12}}{1 + S_{22}L_{11}}\right) \end{bmatrix} \begin{bmatrix} \hat{u}_{in\ 1} \\ \hat{u}_{out\ 2} \end{bmatrix}. \quad (2.31)$$

If the original subsystems are stable, the stability of the interconnected system depends on $1/(1 + S_{22}L_{11})$ [5,24]. Consequently, the stability is ensured when the product $S_{22}L_{11}$ satisfies *Nyquist* stability criterion, where the boundary condition for instability corresponds to $S_{22}L_{11} = -1$. If the subsystems are conventional VF systems (cf. Figure 2.4a), then $S_{22}L_{11}$ is the impedance ratio known as *minor loop gain* both at the input terminal (i.e., Z_S/Z_{in}) and output terminal (i.e., Z_{out}/Z_L) interfaces [2,3], where Z_S denotes the source output impedance, Z_{in} the converter input impedance, Z_{out} the converter output impedance, and Z_L the load input impedance, respectively. If the subsystems are of CF type (cf. Figure 2.5a), then $S_{22}L_{11}$ is the *inverse minor loop gain* both at the input terminal (i.e., Z_{in}/Z_S) and output terminal (i.e., Z_L/Z_{out}) interfaces [12]. Note that in Figures 2.4b and 2.5b, the output mode does not comply with the input source. Therefore, stability assessment has to be performed at the output terminal interface based on the inverse minor loop gain in the case of Figure 2.4b, and on the minor loop gain in the case of Figure 2.5b. Stability assessment at the input terminal interface has to be performed as in the cases of Figures 2.4a and 2.5a, respectively. In general, it can be stated that the numerator impedance in the impedance ratio has to be the impedance of the voltage-source-type element, and the denominator impedance the impedance of the current-source-type element.

2.3 Generalized Dynamic Representations: DC-AC, AC-DC, and AC-AC

2.3.1 Introduction

In a similar manner as in the case of DC-DC converters (cf. Figure 2.1), an equivalent circuit can be constructed for the grid-connected converters, where the memory elements are visible, and the primary and secondary sides of the converter are connected together by using a transformer [16,25]. Such an equivalent circuit is given in Figure 2.16, which represents the dynamic behavior of a grid-connected rectifier (cf. Figure 2.17) in synchronous reference frame with power-invariant $\alpha\beta$ -transformation [18,19,26-29]. The equivalent circuit (cf. Figure 2.18) of a current-fed grid-connected inverter (cf. Figure 2.19) resembles the equivalent circuit given in Figure 2.16 when the input and output terminals as well as the power flow are interchanged. Similar physical insight into the dynamic processes inside the three-phase converter as in Figure 2.1 is obvious, but the real nature of the terminal properties is missing.

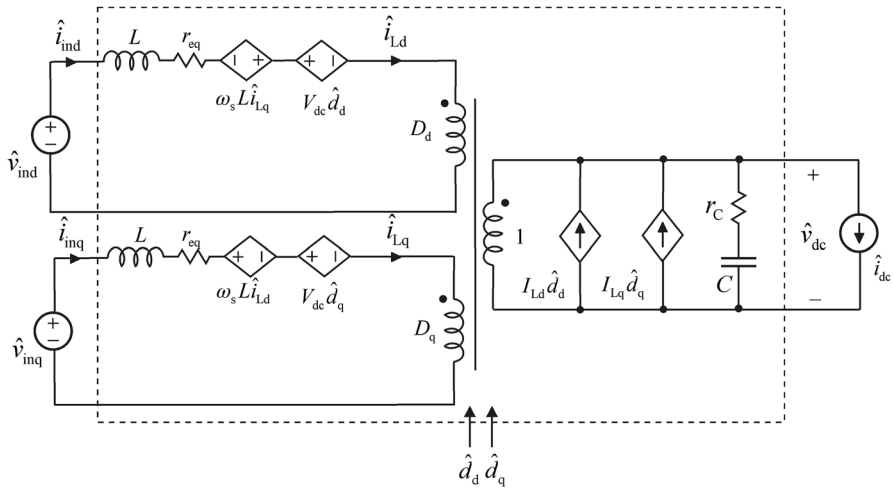


Figure 2.16 Canonical equivalent circuit for a three-phase voltage-fed AC-DC converter.

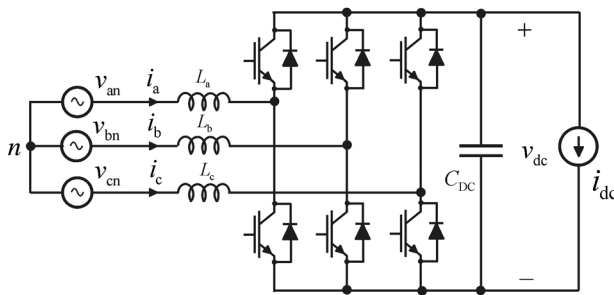


Figure 2.17 Three-phase grid-connected rectifier.

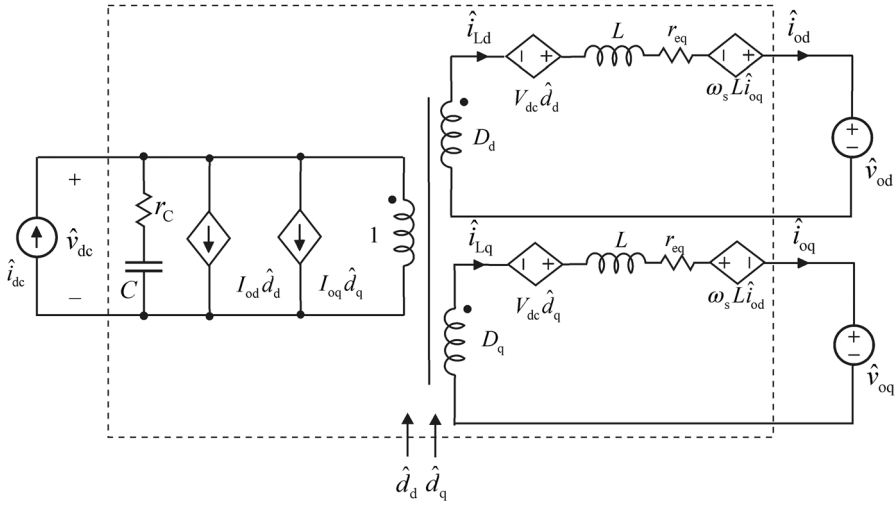


Figure 2.18 Canonical equivalent circuit for a three-phase current-fed DC-AC converter.

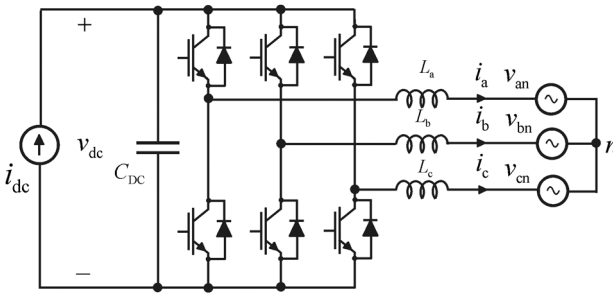


Figure 2.19 Three-phase grid-connected current-fed inverter.

An equivalent circuit resembling the equivalent circuit of a DC-DC converter in Figure 2.2 (i.e., G -parameter representation) can also be constructed for the grid-connected three-phase converters, as shown in Figure 2.20, where the converter dynamic modeling is carried out in synchronous reference frame

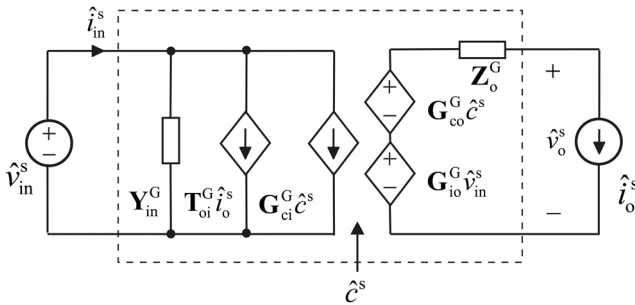


Figure 2.20 A generic equivalent circuit for a three-phase grid-connected AC-AC VF/VO converter.

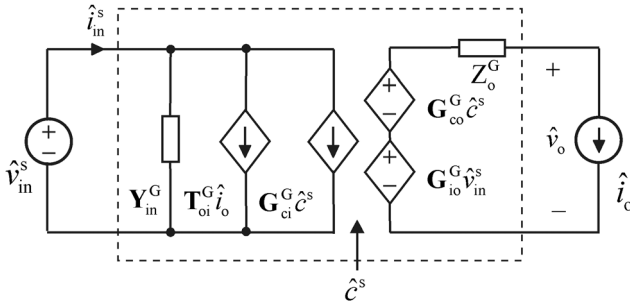


Figure 2.21 A generic equivalent circuit for a three-phase grid-connected AC–DC VF/VO converter.

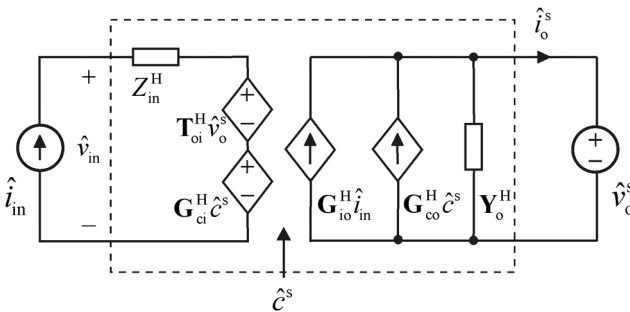


Figure 2.22 A generic equivalent circuit for a three-phase grid-connected DC–AC CF/CO converter.

(i.e., the superscript “s” of the circuit variables denotes the synchronous reference frame). This equivalent circuit is constructed for a three-phase voltage-fed converter producing three-phase output voltage, that is, an AC–AC converter, where both of the terminals are assumed to be three-phase AC networks, that is, the converter is a real MIMO system. If either of the terminals is a DC terminal as in Figures 2.17 and 2.19, then the corresponding terminal variables are also scalars as shown in Figures 2.21 and 2.22.

2.3.2 Generalized Dynamic Representations

In a similar manner as the DC–DC converters were classified to VF and CF converters in Figures 2.3 and 2.4, the AC–DC (i.e., rectifiers) and DC–AC (i.e., inverters) as well as AC–AC converters (i.e., matrix converters) can be classified into VF and CF converters, as shown in Figures 2.23 and 2.24, respectively. In a manner similar to the DC–DC converters, the sets of transfer functions or network parameters describing their dynamic properties are unique for each pair of input and output terminal sources: The converter in Figure 2.23a shall be represented by G -parameters, the converter in Figure 2.23b by Y -parameters, the converter in Figure 2.24a by H -parameters, and the converter in Figure 2.24b by Z -parameters.

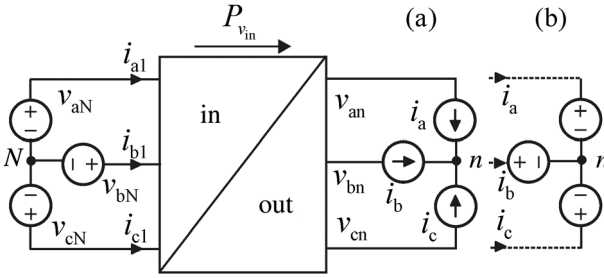


Figure 2.23 Three-phase VF converter (a) at voltage-output mode and (b) at current-output mode.

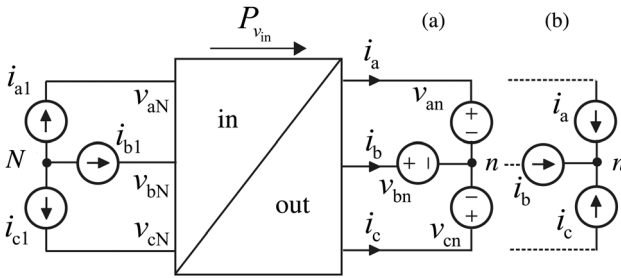


Figure 2.24 Three-phase CF converter (a) at current-output mode and (b) at voltage-output mode.

In general, the set of transfer functions of a multi-input–multi-output (MIMO) converter can be represented as given in Eq. (2.32) using matrix notation with three-variable input vector $[\mathbf{U}_{\text{in}} \ \mathbf{U}_{\text{out}} \ \mathbf{U}_c]^T$ and two-variable output vector $[\mathbf{Y}_{\text{in}} \ \mathbf{Y}_{\text{out}}]^T$, where the subscript “in” denotes an input terminal variable, the subscript “out” the output terminal variable, and the subscript “c” the general control variable.

$$\begin{bmatrix} \mathbf{Y}_{\text{in}} \\ \mathbf{Y}_{\text{out}} \end{bmatrix} = \begin{bmatrix} \mathbf{G}_{11} & \mathbf{G}_{12} & \mathbf{G}_{13} \\ \mathbf{G}_{21} & -\mathbf{G}_{22} & \mathbf{G}_{23} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{\text{in}} \\ \mathbf{U}_{\text{out}} \\ \mathbf{U}_c \end{bmatrix} \quad (2.32)$$

The dynamic modeling of the three-phase converters is usually performed in the synchronous reference frame [16–18,25–29]. As a consequence, the input and output-variable vectors in Eq. (2.32) consist of submatrices with two elements (i.e., the d and q components of the three-phase variables) as shown in Eqs. (2.33) and (2.34). The transfer function elements in Eq. (2.32) are also submatrices with four elements as described in Eq. (2.35), where the elements G_{qd} and G_{dq} denote the cross-couplings between the d and q channels. The negative sign of the element \mathbf{G}_{22} denotes that the output current direction is assumed to be opposite what is usually defined in circuit theory for such

networks [7]. As a consequence, the matrix element \mathbf{G}_{22} has to be constructed according to Eq. (2.36).

$$\mathbf{U}_x = [\hat{u}_{x-d} \quad \hat{u}_{x-q}]^T \quad (2.33)$$

$$\mathbf{Y}_x = [\hat{y}_{x-d} \quad \hat{y}_{x-q}]^T \quad (2.34)$$

$$\mathbf{G}_{xy} = \begin{bmatrix} G_d & G_{qd} \\ G_{dq} & G_q \end{bmatrix} \quad (2.35)$$

$$\mathbf{G}_{22} = \begin{bmatrix} G_d^{22} & G_{qd}^{22} \\ G_{dq}^{22} & G_q^{22} \end{bmatrix} \quad (2.36)$$

If the cross-coupling elements G_{qd} and G_{dq} in \mathbf{G}_{xy} (cf. Eq. (2.35)) are very small, then the MIMO system in Eq. (2.32) can be represented by two separate SISO systems according to Eqs. (2.37) and (2.38). As a consequence, all the analysis presented for the DC–DC converters in Section 2.2 can be applied equally to the systems described in Eqs. (2.37) and (2.38):

$$\begin{bmatrix} \hat{y}_{ind} \\ \hat{y}_{od} \end{bmatrix} = \begin{bmatrix} G_{d-11} & G_{d-12} & G_{d-13} \\ G_{d-21} & -G_{d-22} & G_{d-23} \end{bmatrix} \begin{bmatrix} \hat{u}_{ind} \\ \hat{u}_{outd} \\ \hat{u}_{cd} \end{bmatrix} \quad (2.37)$$

$$\begin{bmatrix} \hat{y}_{inq} \\ \hat{y}_{oq} \end{bmatrix} = \begin{bmatrix} G_{q-11} & G_{q-12} & G_{q-13} \\ G_{q-21} & -G_{q-22} & G_{q-23} \end{bmatrix} \begin{bmatrix} \hat{u}_{inq} \\ \hat{u}_{outq} \\ \hat{u}_{cq} \end{bmatrix} \quad (2.38)$$

The transfer function matrices and the physical transfer functions in Eq. (2.32) can be named according to the same principles as used in Section 2.2.2:

$\mathbf{G}_{11} = \frac{\mathbf{Y}_{in}}{\mathbf{U}_{in}}$: Converter input impedances ($Z_{ind,q}$) or admittance ($Y_{ind,q}$) and the cross-coupling elements

$\mathbf{G}_{12} = \frac{\mathbf{Y}_{in}}{\mathbf{U}_{out}}$: Reverse transfer functions ($T_{oid,q}$) and the cross-coupling elements

$\mathbf{G}_{13} = \frac{\mathbf{Y}_{in}}{\mathbf{U}_c}$: Control-to-input transfer functions ($G_{cid,q}$) and the cross-coupling elements

$\mathbf{G}_{21} = \frac{\mathbf{Y}_{out}}{\mathbf{U}_{in}}$: Forward transfer functions ($G_{iod,q}$) and the cross-coupling elements

$\mathbf{G}_{22} = \frac{\mathbf{Y}_{out}}{\mathbf{U}_{out}}$: Converter output impedances ($Z_{od,q}$) or admittances ($Y_{od,q}$) and the cross-coupling elements

$\mathbf{G}_{23} = \frac{\mathbf{Y}_{out}}{\mathbf{U}_c}$: Control-to-output transfer functions ($G_{cod,q}$) and the cross-coupling elements

The set of the generalized network parameters in Eq. (2.32) cannot be represented as a generalized linear equivalent circuit corresponding to Figure 2.20, since the matrix entries \mathbf{G}_{11} and \mathbf{G}_{22} are either impedance- or admittance-type elements requiring

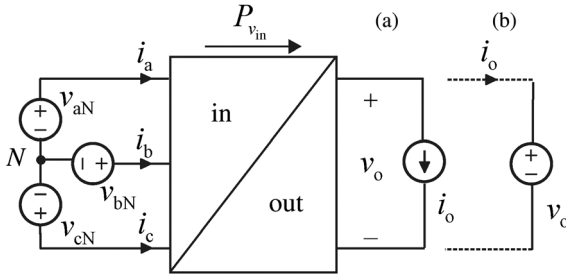


Figure 2.25 Grid-connected three-phase rectifier.

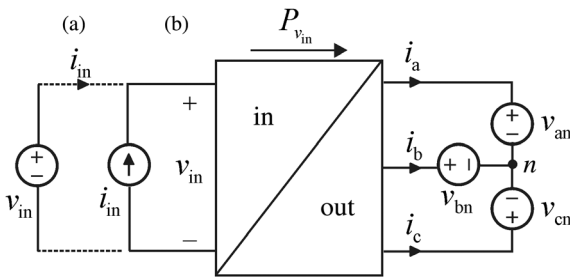


Figure 2.26 Grid-connected three-phase inverter in grid-parallel mode.

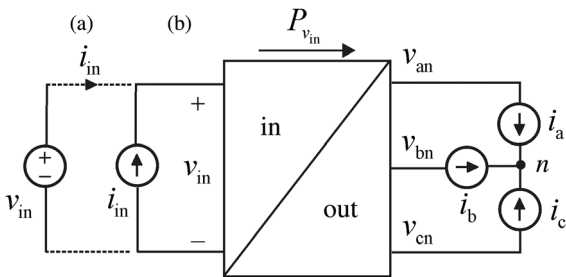


Figure 2.27 Grid-connected three-phase inverter in grid-forming mode.

their connection either in series or in parallel to the corresponding controlled source elements (i.e., either voltage or current type), as illustrated in Figure 2.20.

Within the context of the book, the grid-connected power electronic converters are always either three-phase rectifiers supplied by a three-phase voltage source (Figure 2.25) or inverters connected to a three-phase grid (Figures 2.26 and 2.27). Therefore, the multivariable nature is limited either to the input terminal (Figure 2.24; that is, a SIMO system) or to the output terminal (Figures 2.26 and 2.27; MISO systems). As a consequence, some of the entries in Eq. (2.32) may be single-valued entries, which usually makes the overall analysis easier compared to the full-scale MIMO systems [19,20].

2.3.3 Generalized Closed-Loop Dynamics

In a converter, there are usually two output variables – one at the input side and another at the output side, respectively. Therefore, there are also two different sets of closed-loop transfer functions as follows: Under input-side multivariable feedback control, the closed-loop system can be presented as (cf. Figure 2.28)

$$\begin{bmatrix} Y_{in} \\ Y_{out} \end{bmatrix} = \begin{bmatrix} [I+L_{in}]^{-1}G_{11-o} & [I+L_{in}]^{-1}G_{12-o} & [I+L_{in}]^{-1}L_{in}G_{se-in}^{-1} \\ [I+L_{in}]^{-1}(G_{22-o}+G_{21-\infty}L_{in}) & -[I+L_{in}]^{-1}(G_{22-o}+G_{22-\infty}L_{in}) & G_{23-o}G_{13-o}^{-1}G_{se-in}^{-1}L_{in}[I+L_{in}]^{-1} \end{bmatrix} \begin{bmatrix} U_{in} \\ U_{out} \\ U_{r-in} \end{bmatrix} \quad (2.39)$$

with

$$G_{21-\infty} = G_{21-o} - G_{11-o}G_{23-o}G_{13-o}^{-1} \quad (2.40)$$

and

$$G_{22-\infty} = G_{22-o} + G_{12-o}G_{23-o}G_{13-o}^{-1}, \quad (2.41)$$

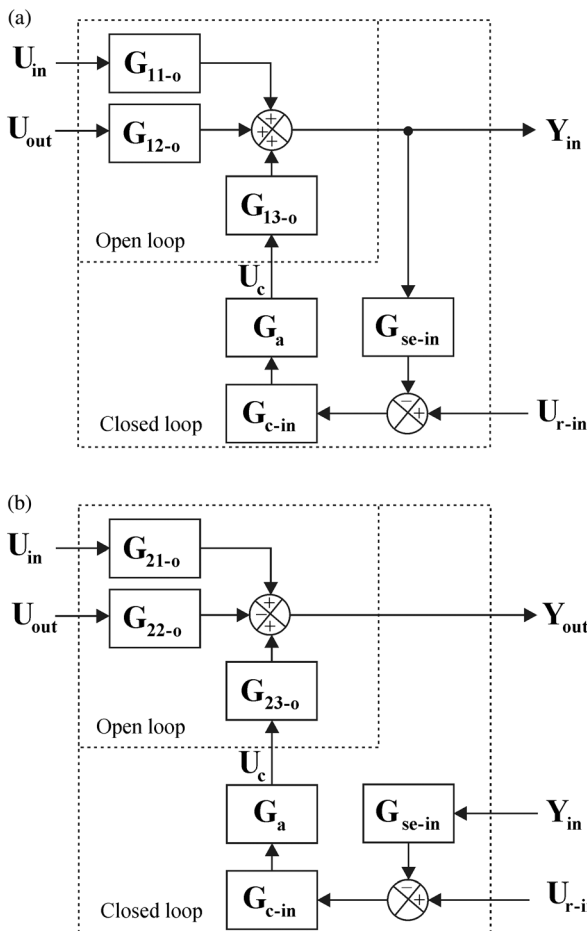


Figure 2.28 General multi-variable control-engineering block diagrams for the input-side feedback control. (a) Input dynamics. (b) Output dynamics.

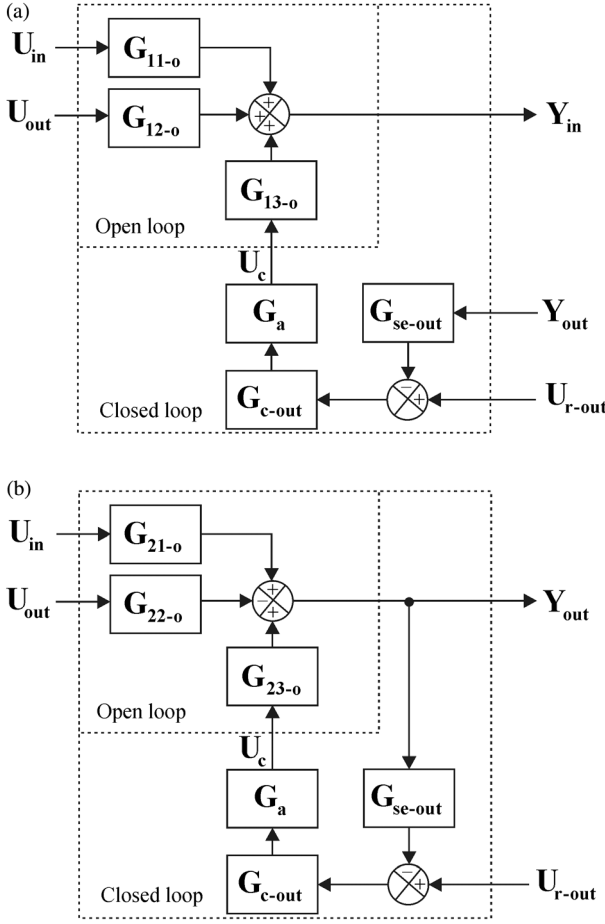


Figure 2.29 General multivariable control-engineering block diagrams for the output-side feedback control. (a) Input dynamics. (b) Output dynamics.

where $\mathbf{L}_{in} = \mathbf{G}_{se-in} \mathbf{G}_a \mathbf{G}_{c-in} \mathbf{G}_{13-o}$ is the input-side multivariable loop gain, and the other multivariable elements are, in principle, the same as defined in the SISO case in Section 2.2.3. Transfer function matrices $\mathbf{G}_{21-\infty}$ and $\mathbf{G}_{22-\infty}$ contain the transfer functions, which are referred to as “ideal” output-side transfer functions in Section 2.2.3.

Under output-side multivariable feedback control, the closed-loop system can be presented (cf. Figure 2.29) as

$$\begin{bmatrix} \mathbf{Y}_{in} \\ \mathbf{Y}_{out} \end{bmatrix} = \begin{bmatrix} [\mathbf{I} + \mathbf{L}_{out}]^{-1} (\mathbf{G}_{11-o} + \mathbf{G}_{11-\infty} \mathbf{L}_{out}) & [\mathbf{I} + \mathbf{L}_{out}]^{-1} (\mathbf{G}_{12-o} + \mathbf{G}_{12-\infty} \mathbf{L}_{out}) & \mathbf{G}_{13-o} \mathbf{G}_{23-o}^{-1} \mathbf{G}_{se-out}^{-1} \mathbf{L}_{out} [\mathbf{I} + \mathbf{L}_{out}]^{-1} \\ [\mathbf{I} + \mathbf{L}_{out}]^{-1} \mathbf{G}_{21-o} & -[\mathbf{I} + \mathbf{L}_{out}]^{-1} \mathbf{G}_{22-o} & [\mathbf{I} + \mathbf{L}_{out}]^{-1} \mathbf{L}_{out} \mathbf{G}_{se-out}^{-1} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in} \\ \mathbf{U}_{out} \\ \mathbf{U}_{r-out} \end{bmatrix} \quad (2.42)$$

with

$$\mathbf{G}_{11-\infty} = \mathbf{G}_{11-o} - \mathbf{G}_{21-o} \mathbf{G}_{13-o} \mathbf{G}_{23-o}^{-1} \quad (2.43)$$

and

$$\mathbf{G}_{12-\infty} = \mathbf{G}_{12-o} + \mathbf{G}_{22-o} \mathbf{G}_{13-o} \mathbf{G}_{23-o}^{-1}, \quad (2.44)$$

where $\mathbf{L}_{\text{out}} = \mathbf{G}_{\text{se-out}} \mathbf{G}_a \mathbf{G}_{\text{c-out}} \mathbf{G}_{23-0}$ is the output-side multivariable loop gain, and the other multivariable elements are, in principle, the same as defined in the SISO case in Section 2.2.3. Transfer function matrices $\mathbf{G}_{11-\infty}$ and $\mathbf{G}_{12-\infty}$ contain the transfer functions, which are referred to as “ideal” output-side transfer functions in Section 2.2.3.

2.3.4 Generalized Cascaded Control Schemes

It is quite common, especially, in renewable energy applications, that the inverter control is arranged in a cascaded manner (cf. Figure 2.30), where the inverter output current control forms the inner loop, and the DC-link voltage control (Figure 2.30a) or the output-voltage control (Figure 2.30b) forms the outer loop [17–19]. The general dynamic formulations for the above-described cases are given in this section.

The analysis of the cascaded control schemes is twofold: (i) First the closed-loop transfer functions induced by the closed inner feedback loop have to be developed. (ii) The set of these transfer functions forms the “open-loop” set of transfer functions for developing the set of closed-loop transfer functions induced by the outer feedback loop. The procedure is more complicated if both of the feedback loops are taken from the same terminal as in Figure 2.30b, because the output or input mode of the converter would change necessitating to modify accordingly also the set of transfer functions induced by the inner loop. Such a situation is valid when the operation mode of the inverter has to be changed from the grid-parallel mode (Figure 2.30a) to the grid-forming mode (Figure 2.30b) (see, for example, Ref. [30]).

For the case, where the output-side feedback loop forms the inner loop and the input-side feedback loop forms the outer loop, the inner-loop-induced set of transfer functions are given in Section 2.3.3 in Eqs. (2.42)–(2.44) and illustrated in Figure 2.22. The corresponding set of transfer functions when both of the

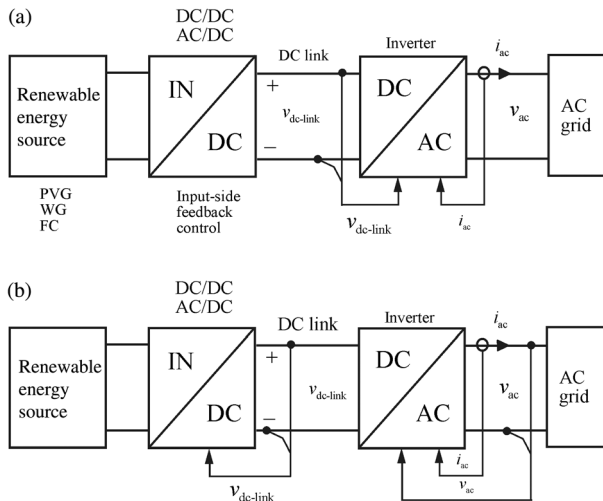


Figure 2.30 Grid-connected inverter control schemes in (a) grid-parallel operation, and (b) grid-forming operation.

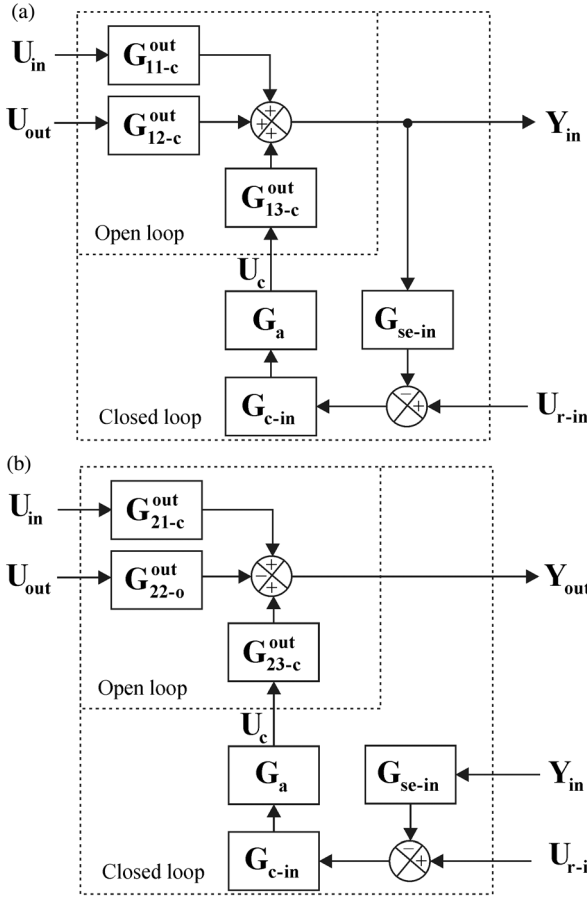


Figure 2.31 General multi-variable control-engineering block diagrams for the cascaded input-output feedback control. (a) Input dynamics. (b) Output dynamics.

feedback loops are closed yields (cf. Figure 2.31)

$$\begin{bmatrix} Y_{in} \\ Y_{out} \end{bmatrix} = \begin{bmatrix} [I+L_{in}]^{-1}G_{11-c}^{out} & [I+L_{in}]^{-1}G_{12-c}^{out} & [I+L_{in}]^{-1}L_{in}G_{se-in}^{-1} \\ [I+L_{in}]^{-1}(G_{22-c}^{out}+G_{21-\infty}^{out}L_{in}) & -[I+L_{in}]^{-1}(G_{22-c}^{out}+G_{22-\infty}^{out}L_{in}) & G_{23-c}^{out}G_{13-c}^{out-1}G_{se-in}^{-1}L_{in}[I+L_{in}]^{-1} \end{bmatrix} \begin{bmatrix} U_{in} \\ U_{out} \\ U_{r-in} \end{bmatrix} \quad (2.45)$$

with

$$G_{21-\infty}^{out} = G_{21-c}^{out} - G_{11-c}^{out}G_{23-c}^{out}G_{13-c}^{out-1} \quad (2.46)$$

and

$$G_{22-\infty}^{out} = G_{22-c}^{out} + G_{12-c}^{out}G_{23-c}^{out}G_{13-c}^{-1} \quad (2.47)$$

where $L_{in} = G_{se-in}G_aG_{c-in}G_{13-c}^{out}$ is the input-side loop gain and G_{13-c}^{out} is the closed inner-loop-induced control-to-input transfer function matrix. The other elements are the same as matrices as defined for the SISO systems in Section 2.2.4.

For the case, where the input-side feedback loop forms the inner loop and the output-side feedback loop forms the outer loop, the inner-loop-induced set of transfer functions are given in Section 2.3.3 in Eqs. (2.39)–(2.41), and illustrated in

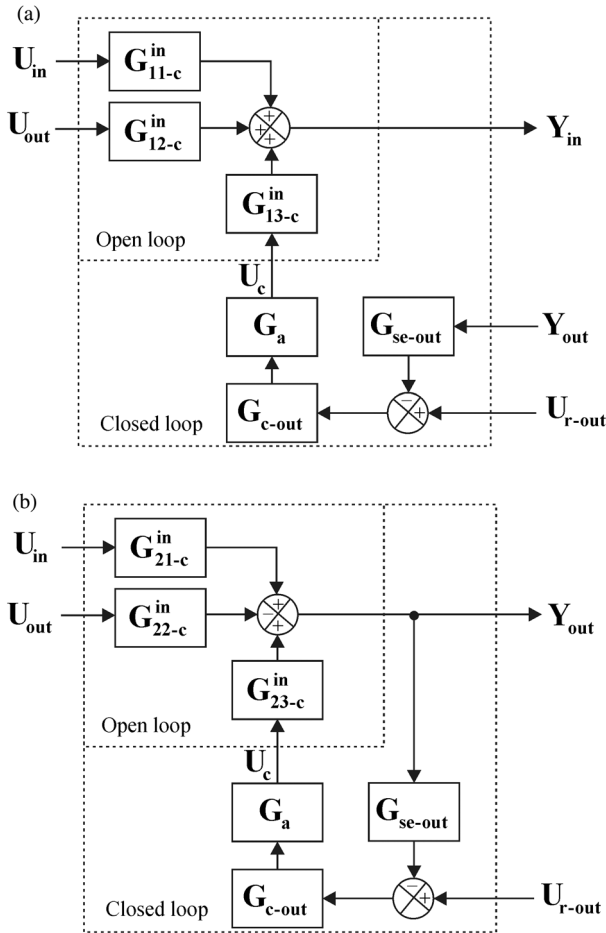


Figure 2.32 General multivariable control-engineering block diagrams for the cascaded output-input feedback control. (a) Input dynamics. (b) Output dynamics.

Figure 2.21. The corresponding set of transfer functions when both of the feedback loops are closed yields (cf. Figure 2.32)

$$\begin{bmatrix} Y_{in} \\ Y_{out} \end{bmatrix} = \begin{bmatrix} [I+L_{out}]^{-1}(G_{11-c}^{in} + G_{11-\infty}^{in} L_{out}) & [I+L_{out}]^{-1}(G_{12-c}^{in} + G_{12-\infty}^{in} L_{out}) & G_{13-c}^{in} G_{23-c}^{in-1} G_{se-out}^{-1} L_{out} [I+L_{out}]^{-1} \\ [I+L_{out}]^{-1} G_{21-c}^{in} & -[I+L_{out}]^{-1} G_{22-c}^{in} & [I+L_{out}]^{-1} L_{out} G_{se-out}^{-1} \end{bmatrix} \begin{bmatrix} U_{in} \\ U_{out} \\ U_{r-out} \end{bmatrix} \quad (2.48)$$

with

$$G_{11-\infty}^{in} = G_{11-c}^{in} - G_{21-c}^{in} G_{13-c}^{in} G_{23-c}^{in-1} \quad (2.49)$$

and

$$G_{12-\infty}^{in} = G_{12-c}^{in} + G_{22-c}^{in} G_{13-c}^{in} G_{23-c}^{in-1}, \quad (2.50)$$

where $L_{out} = G_{se-out} G_a G_{c-out} G_{23-c}^{in}$ is the output-side feedback loop gain and G_{23-c}^{in} is the closed inner-loop-induced control-to-output transfer function matrix. The other elements are the same as matrices as defined for the SISO systems in Section 2.2.4.

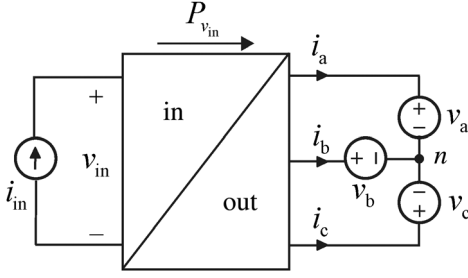


Figure 2.33 Grid-connected converter in grid-parallel mode, that is, current-output mode.

The case where both of the input terminal variables are controlled at the same time in a cascaded manner is not very probable and, therefore, the output-side cascaded control is treated in detail only. In grid-parallel (GP) operation mode, the output of the converter is current source as illustrated in Figure 2.33, and its dynamics can be given by

$$\begin{cases} \mathbf{Y}_{\text{in}}^{\text{GP}} = \mathbf{G}_{11}^{\text{GP}} \mathbf{U}_{\text{in}}^{\text{GP}} + \mathbf{G}_{12}^{\text{GP}} \mathbf{U}_{\text{out}}^{\text{GP}} + \mathbf{G}_{13}^{\text{GP}} \mathbf{U}_{\text{c}}^{\text{GP}} \\ \mathbf{Y}_{\text{out}}^{\text{GP}} = \mathbf{G}_{21}^{\text{GP}} \mathbf{U}_{\text{in}}^{\text{GP}} - \mathbf{G}_{22}^{\text{GP}} \mathbf{U}_{\text{out}}^{\text{GP}} + \mathbf{G}_{23}^{\text{GP}} \mathbf{U}_{\text{c}}^{\text{GP}} \end{cases} \quad (2.51)$$

In the grid-forming (GF) mode, the output and input variables at the output terminal will be interchanged, that is, $\mathbf{Y}_{\text{out}}^{\text{GF}} = \mathbf{U}_{\text{out}}^{\text{GP}}$ and $\mathbf{U}_{\text{out}}^{\text{GF}} = \mathbf{Y}_{\text{out}}^{\text{GP}}$, respectively. The other input variables will remain the same. Therefore, the transformed dynamic representation, which corresponds to the voltage-output mode (Figure 2.34), can be given by

$$\begin{cases} \mathbf{Y}_{\text{in}}^{\text{GF}} = (\mathbf{G}_{11}^{\text{GP}} - \mathbf{G}_{12}^{\text{GP}} \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{21}^{\text{GP}}) \mathbf{U}_{\text{in}}^{\text{GP}} + \mathbf{G}_{12}^{\text{GP}} \mathbf{G}_{22}^{\text{GP-1}} \mathbf{U}_{\text{out}}^{\text{GF}} + (\mathbf{G}_{13}^{\text{GP}} - \mathbf{G}_{12}^{\text{GP}} \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{23}^{\text{GP}}) \mathbf{U}_{\text{c}}^{\text{GF}} \\ \mathbf{Y}_{\text{out}}^{\text{GF}} = \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{21}^{\text{GP}} \mathbf{U}_{\text{in}}^{\text{GF}} - \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{22}^{\text{GP}} \mathbf{U}_{\text{out}}^{\text{GF}} + \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{23}^{\text{GP}} \mathbf{U}_{\text{c}}^{\text{GF}} \end{cases} \quad (2.52)$$

or

$$\begin{bmatrix} \mathbf{Y}_{\text{in}}^{\text{GF}} \\ \mathbf{Y}_{\text{out}}^{\text{GF}} \end{bmatrix} = \begin{bmatrix} \mathbf{G}_{11}^{\text{GP}} - \mathbf{G}_{12}^{\text{GP}} \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{21}^{\text{GP}} & -\mathbf{G}_{12}^{\text{GP}} \mathbf{G}_{22}^{\text{GP-1}} & \mathbf{G}_{13}^{\text{GP}} - \mathbf{G}_{12}^{\text{GP}} \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{23}^{\text{GP}} \\ \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{21}^{\text{GP}} & -\mathbf{G}_{22}^{\text{GP-1}} & \mathbf{G}_{22}^{\text{GP-1}} \mathbf{G}_{23}^{\text{GP}} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{\text{in}}^{\text{GF}} \\ \mathbf{U}_{\text{out}}^{\text{GF}} \\ \mathbf{U}_{\text{c}}^{\text{GF}} \end{bmatrix} \quad (2.53)$$

where the matrices $\mathbf{G}_{xy}^{\text{GP}}$ denote the closed-inner-loop transfer function matrices given in (2.39)–(2.41) and illustrated in Figure 2.21. The final set of closed-loop

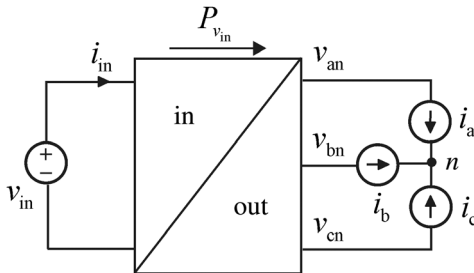


Figure 2.34 Grid-connected converter in grid-forming mode, that is, voltage-output mode.

transfer functions can be obtained by performing the computations in Eqs. (2.39)–(2.41), again with the transfer functions given in Eq. (2.53).

2.3.5 Generalized Source and Load Interactions

The input and output terminal sources contain, in practice, finite source impedances, which may affect the dynamic performance of the converter in terms of transient behavior and stability [5]. The formulation of the source–load interactions given below follows basically the formulation introduced in the extra element method described in Ref. [4], similarly as in the case of DC–DC converters in Section 2.2.5. The source and load interactions are computed by using a simple internal impedance/admittance representing the source/load. It is equally possible to use full dynamic representation with four matrix elements.

The general form of the source–converter interactions can be determined based on Figure 2.35, where the converter subsystem **C** is connected in series with the source subsystem **S**, containing either voltage or current source with an internal impedance/admittance matrix denoted by \mathbf{S}_{22} . The input, output, and intermediate system variable vectors of the cascaded connection are denoted by $(\mathbf{U}_{in1}, \mathbf{U}_{out2}, \mathbf{U}_c)$, $(\mathbf{Y}_{in1}, \mathbf{Y}_{out2})$, and $(\mathbf{U}_s, \mathbf{Y}_s)$, respectively. The corresponding electrical variables can be either voltage or current depending on application.

Dynamic representations of the source and converter are given by

$$\begin{aligned} \begin{bmatrix} \mathbf{Y}_{in1} \\ \mathbf{Y}_{out1} \end{bmatrix} &= \begin{bmatrix} \mathbf{O} & \mathbf{I} \\ \mathbf{I} & -\mathbf{S}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in1} \\ \mathbf{U}_{out1} \end{bmatrix} \\ \begin{bmatrix} \mathbf{Y}_{in2} \\ \mathbf{Y}_{out2} \end{bmatrix} &= \begin{bmatrix} \mathbf{G}_{11} & \mathbf{G}_{12} & \mathbf{G}_{13} \\ \mathbf{G}_{21} & -\mathbf{G}_{22} & \mathbf{G}_{23} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in2} \\ \mathbf{U}_{out2} \\ \mathbf{U}_c \end{bmatrix} \end{aligned} \quad (2.54)$$

and the source–converter coupled system dynamics is then obtained as

$$\begin{bmatrix} \mathbf{Y}_{in1} \\ \mathbf{Y}_{out2} \end{bmatrix} = \begin{bmatrix} [\mathbf{I} + \mathbf{G}_{11}\mathbf{S}_{22}]^{-1}\mathbf{G}_{11} & [\mathbf{I} + \mathbf{G}_{11}\mathbf{S}_{22}]^{-1}\mathbf{G}_{12} & [\mathbf{I} + \mathbf{G}_{11}\mathbf{S}_{22}]^{-1}\mathbf{G}_{13} \\ \mathbf{G}_{21}[\mathbf{I} + \mathbf{S}_{22}\mathbf{G}_{11}]^{-1} & -[\mathbf{I} + \mathbf{S}_{22}\mathbf{G}_{11}]^{-1}(\mathbf{I} + \mathbf{S}_{22}\mathbf{G}_{11-\infty})\mathbf{G}_{22} & [\mathbf{I} + \mathbf{S}_{22}\mathbf{G}_{11}]^{-1}(\mathbf{I} + \mathbf{S}_{22}\mathbf{G}_{11-\infty})\mathbf{G}_{23} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in1} \\ \mathbf{U}_{out2} \\ \mathbf{U}_c \end{bmatrix} \quad (2.55)$$

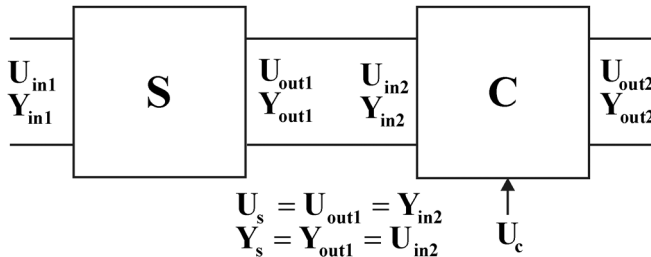


Figure 2.35 Cascaded connection of multivariable source **S** and converter **C**.

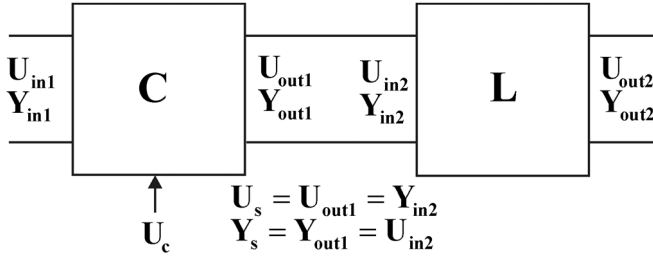


Figure 2.36 Cascaded connection of multivariable converter C and load L .

with

$$\mathbf{G}_{11-x0} = \mathbf{G}_{11} + \mathbf{G}_{21}\mathbf{G}_{12}\mathbf{G}_{22}^{-1} \quad (2.56)$$

and

$$\mathbf{G}_{11-\infty} = \mathbf{G}_{11} - \mathbf{G}_{21}\mathbf{G}_{13}\mathbf{G}_{23}^{-1} \quad (2.57)$$

Transfer function matrix \mathbf{G}_{11-x0} denotes the impedance/admittance characteristics of the converter input terminal when the output terminal is either short circuited (sco) or open circuit (oco) depending on the nature of the ideal load (i.e., the output is terminated with inverse of the internal impedance of the ideal output load).

The general form of converter-load interaction can be determined based on Figure 2.36, where the converter subsystem C is connected in series with the load subsystem L containing either voltage or current sink with an internal impedance/admittance denoted by L_{11} . The coupled system input, output, and intermediate variables are the same as above as denoted in Figure 2.36.

Dynamic representation of the converter and load are given by

$$\begin{bmatrix} \mathbf{Y}_{in1} \\ \mathbf{Y}_{out1} \end{bmatrix} = \begin{bmatrix} \mathbf{G}_{11} & \mathbf{G}_{12} & \mathbf{G}_{13} \\ \mathbf{G}_{21} & -\mathbf{G}_{22} & \mathbf{G}_{23} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in1} \\ \mathbf{U}_{out1} \\ U_c \end{bmatrix} \quad (2.58)$$

$$\begin{bmatrix} \mathbf{Y}_{in2} \\ \mathbf{Y}_{out2} \end{bmatrix} = \begin{bmatrix} \mathbf{L}_{11} & \mathbf{I} \\ \mathbf{I} & \mathbf{O} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in2} \\ \mathbf{U}_{out2} \end{bmatrix}$$

and the converter-load coupled system dynamics is then obtained as

$$\begin{bmatrix} \mathbf{Y}_{in1} \\ \mathbf{Y}_{out2} \end{bmatrix} = \begin{bmatrix} [\mathbf{I} + \mathbf{L}_{11}\mathbf{G}_{22}]^{-1}(\mathbf{I} + \mathbf{L}_{11}\mathbf{G}_{22-xi})\mathbf{G}_{11} & \mathbf{G}_{12}[\mathbf{I} + \mathbf{L}_{11}\mathbf{G}_{22}]^{-1} & [\mathbf{I} + \mathbf{L}_{11}\mathbf{G}_{22}]^{-1}(\mathbf{I} + \mathbf{L}_{11}\mathbf{G}_{22-\infty})\mathbf{G}_{13} \\ [\mathbf{I} + \mathbf{G}_{22}\mathbf{L}_{11}]^{-1}\mathbf{G}_{21} & -[\mathbf{I} + \mathbf{G}_{22}\mathbf{L}_{11}]^{-1}\mathbf{G}_{22} & [\mathbf{I} + \mathbf{G}_{22}\mathbf{L}_{11}]^{-1}\mathbf{G}_{23} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in1} \\ \mathbf{U}_{out2} \\ U_c \end{bmatrix} \quad (2.59)$$

with

$$\mathbf{G}_{22-xi} = \mathbf{G}_{22} + \mathbf{G}_{21}\mathbf{G}_{12}\mathbf{G}_{11}^{-1} \quad (2.60)$$

and

$$\mathbf{G}_{22-\infty} = \mathbf{G}_{22} - \mathbf{G}_{12}\mathbf{G}_{23}\mathbf{G}_{13}^{-1} \quad (2.61)$$

The transfer function matrix \mathbf{G}_{22-xi} denotes the impedance/admittance characteristics of the output terminal, when the input terminal is either open circuit (oci) or short circuited (sci) depending on the nature of the ideal input source (i.e., the output is terminated with the inverse of the internal impedance of the ideal input source).

2.3.6 Generalized Impedance-Based Stability Assessment

A general interconnected multivariable system is given in Figure 2.37, where \mathbf{S} denotes the source-side subsystem, merging the dynamics of the upstream system, and \mathbf{L} denotes the load-side subsystem, merging the dynamics of the downstream system. The subsystems can be represented as

$$\begin{aligned} \begin{bmatrix} \mathbf{Y}_{in\ 1} \\ \mathbf{Y}_{out\ 1} \end{bmatrix} &= \begin{bmatrix} \mathbf{S}_{11} & \mathbf{S}_{21} \\ \mathbf{S}_{21} & -\mathbf{S}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in\ 1} \\ \mathbf{U}_{out\ 1} \end{bmatrix} \\ \begin{bmatrix} \mathbf{Y}_{in\ 2} \\ \mathbf{Y}_{out\ 2} \end{bmatrix} &= \begin{bmatrix} \mathbf{L}_{11} & \mathbf{L}_{21} \\ \mathbf{L}_{21} & -\mathbf{L}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in\ 2} \\ \mathbf{U}_{out\ 2} \end{bmatrix} \end{aligned} \quad (2.62)$$

where the control variables \mathbf{U}_{c-i} are set to zero without loss of generality. The input, output, and intermediate variable vectors are the same as given in Section 2.3.5. The matrix entries \mathbf{X}_{11} and \mathbf{X}_{22} denote the impedance/admittance-like properties measured at the input and output terminals of the subsystems in Eq. (2.62).

Stability of the interconnected system can be assessed by first computing the mappings from the system input variables ($\mathbf{U}_{in\ 1}$, $\mathbf{U}_{out\ 2}$) to the intermediate variables (\mathbf{U}_s , \mathbf{Y}_s),

$$\begin{bmatrix} \mathbf{U}_s \\ \mathbf{Y}_s \end{bmatrix} = \begin{bmatrix} [\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]^{-1}\mathbf{L}_{11}\mathbf{S}_{21} & [\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]^{-1}\mathbf{L}_{12} \\ [\mathbf{I} + \mathbf{S}_{22}\mathbf{L}_{11}]^{-1}\mathbf{S}_{21} & -[\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]^{-1}\mathbf{S}_{22}\mathbf{L}_{12} \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in\ 1} \\ \mathbf{U}_{out\ 2} \end{bmatrix} \quad (2.63)$$

and then the mapping from the system input variables ($\mathbf{U}_{in\ 1}$, $\mathbf{U}_{out\ 2}$) to the system output variables ($\mathbf{Y}_{in\ 1}$, $\mathbf{Y}_{out\ 2}$):

$$\begin{bmatrix} \mathbf{Y}_{in\ 1} \\ \mathbf{Y}_{out\ 2} \end{bmatrix} = \begin{bmatrix} \mathbf{S}_{11} + \mathbf{S}_{12}[\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]^{-1}\mathbf{L}_{11}\mathbf{S}_{21} & \mathbf{S}_{12}[\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]^{-1}\mathbf{L}_{12} \\ \mathbf{L}_{21}[\mathbf{I} + \mathbf{S}_{22}\mathbf{L}_{11}]^{-1}\mathbf{S}_{21} & -(\mathbf{L}_{22} + \mathbf{L}_{21}[\mathbf{I} + \mathbf{S}_{22}\mathbf{L}_{11}]^{-1}\mathbf{S}_{22}\mathbf{L}_{12}) \end{bmatrix} \begin{bmatrix} \mathbf{U}_{in\ 1} \\ \mathbf{U}_{out\ 2} \end{bmatrix} \quad (2.64)$$

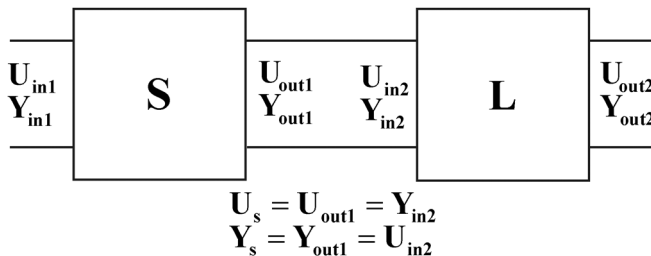


Figure 2.37 Cascaded connection of general multivariable source \mathbf{S} and load \mathbf{L} .

If the original subsystems are stable, then the stability of interconnected system depends on $[\mathbf{I} + \mathbf{S}_{22}\mathbf{L}_{11}]^{-1}$ and $[\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]^{-1}$ [24,31,32]. Consequently, the stability is ensured when the determinants $\det[\mathbf{I} + \mathbf{S}_{22}\mathbf{L}_{11}]$ and $\det[\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]$ satisfy the generalized *Nyquist* stability criterion [33,34]: Let P denote the number of RHP poles of the matrix product $\mathbf{S}_{22}\mathbf{L}_{11}$ or $\mathbf{L}_{11}\mathbf{S}_{22}$, then the system is stable if the *Nyquist* plot of $\det[\mathbf{I} + \mathbf{S}_{22}\mathbf{L}_{11}]$ and $\det[\mathbf{I} + \mathbf{L}_{11}\mathbf{S}_{22}]$ will make P anticlockwise encirclements of the origin, and the curve does not pass through the origin.

2.4 Small-Signal Modeling

2.4.1 Introduction

The material presented in Sections 2.2 and 2.3 can be equally utilized by substituting the basic matrix element (i.e., transfer functions) with the predicted analytical transfer functions expressed in *Laplace* domain or with the measured transfer functions, which are transformed into complex numbers. The use of both analytical predictions and measured transfer functions at the same time is also possible when both of them are expressed as frequency-dependent complex numbers.

In this section, the methods to develop the analytical transfer functions are introduced. The dynamic modeling was laid down in the early 1970s when the switched-mode converter average modeling was introduced [35]. The method was later streamlined into the famous state-space averaging (SSA) method in Ref. [1], which was valid for the converters operating in continuous conduction mode (CCM) under direct duty ratio (DDR) control. The method was later extended to model also the converter dynamics in discontinuous conduction mode (DCM), where the inductor current is zero during a part of the switching cycle [36]. The modeling in Ref. [36] failed because of the wrong assumption on the existence of the inductor current derivative. Valid DCM modeling has been introduced much later in the early 2000s [37,38]. The dynamic models for the converters under the other control methods such as peak-current mode, average-current, and self-oscillation control can be developed from the basic dynamic model by modifying the perturbed duty ratio or on-time with a proper duty ratio or on-time constraints [5,39–42]. The DDR control is the basic control mode also in modeling of the current-fed converters [43].

As implied above, the recognition of the correct operational mode of the converter is very important because of its significant effect on the modeling technique. Figure 2.38 shows the waveforms of inductor current and capacitor voltage illustrating the definition of the different modes. In voltage-fed (i.e., conventional) applications, the capacitors are usually designed to have low ripple content. Therefore, the conduction modes are related to the behavior of the inductor currents. In current-fed applications, the inductors are usually designed to have low ripple content. Therefore, the conduction modes are related to the behavior of the capacitor voltages. As a consequence, the CCM operation mode is such that the inductor current or capacitor voltage contains two different derivatives within the cycle (cf. Figure 2.38: CCM-1 and CCM-2). The mode, where instantaneous waveform touches the zero level, is known as

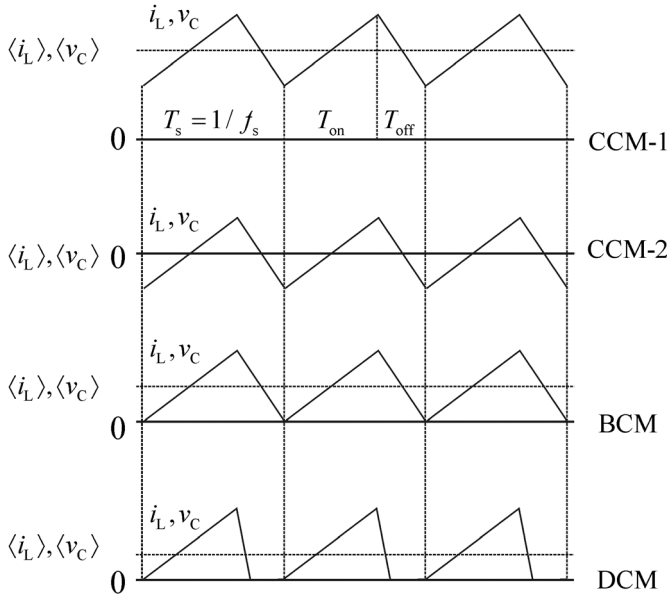


Figure 2.38 Definition of conduction modes.

boundary conduction mode (BCM) (cf. Figure 2.38: BCM). The other names for this conduction mode are critical conduction mode and transition mode. It should be observed that BCM belongs also to CCM class. In DCM, the inductor current or capacitor voltage is zero during a part of the off-time (cf. Figure 2.38: DCM).

In order to model the dynamic behavior of the converter, we have to recognize and choose the proper input (u_{in-i}), output (y_{in-i}), control (u_{c-i}), and state (x_i) variables (cf. Figure 2.39). In multivariable case, there can be several variables within each class of variables. The input and output variables

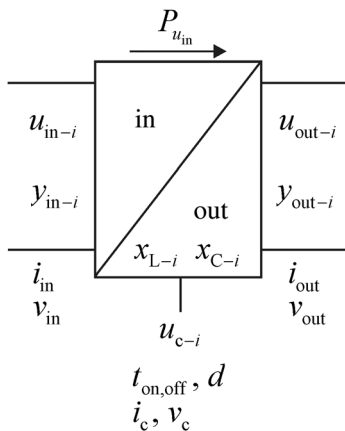


Figure 2.39 Dynamic modeling constellation.

will change depending on the electrical sources connected to the input and output terminals as explicitly demonstrated in Ref. [20]. The input variables are most often the main electrical variables of ideal electrical sources connected to the input and output terminals. The output variables are the duals of the input variables (i.e., voltage↔current). If the converter is terminated at the output by means of a resistor, then the output variable is the variable, which is to be regulated constant. This is generally valid, because the output variable of regulated sources cannot be anymore regulated. As a consequence, those variables are always input variables. The inductor currents and capacitor voltages are most often taken as state variables because of their memory-element nature. The control variables are basically input variables but due to their special nature they are considered as separate variables. Physically, the input and output variables are always voltages and currents. The control variables can be the on- or off-time or duty ratios of the controlled switches as well as voltage and current (cf. Figure 2.39).

The SSA method produces an average model of the corresponding converter, where the variables are the time-varying averages of the instantaneous variables within one switching cycle. The derivatives of the state variables and the output variables are expressed as functions of state, input, and control variables applying Kirchhoff's voltage and current laws. The small-signal model will be obtained from the average model by means of linearizing techniques at a certain operating point. Due to nature of the averaging, the small-signal models are valid only up to half the switching frequency or half the frequency, which corresponds to the averaging cycle time. The obtained derivatives and output variables are presented in a state-space form as follows:

$$\begin{aligned} \left[\frac{d\hat{x}_i(t)}{dt} \right] &= [A][\hat{x}_i(t)] + [B][\hat{u}_i(t)], \\ \hat{y}_i(t) &= [C][\hat{x}_i(t)] + [D][\hat{u}_i(t)], \end{aligned} \quad (2.65)$$

where the variables are expressed in the time-domain and coefficient matrices are time invariant. The “hat” over the variables denotes the small-signal nature of the variables (i.e., small variation around the corresponding steady-state value). For solving the transfer functions, the time-domain state space has to be transformed into *Laplace* (i.e., frequency) domain as follows:

$$\begin{aligned} [s\hat{x}_i(s)] &= [A][\hat{x}_i(s)] + [B][\hat{u}_i(s)], \\ \hat{y}_i(s) &= [C][\hat{x}_i(s)] + [D][\hat{u}_i(s)], \end{aligned} \quad (2.66)$$

which can be solved for obtaining the input-to-state transfer functions:

$$[\hat{x}_i(s)] = [sI - [A]]^{-1}[B][\hat{u}_i(s)] \quad (2.67)$$

and for the input-to-output transfer functions:

$$[\hat{y}_i(s)] = [[C][sI - [A]]^{-1}[B] + [D]][\hat{u}_i(s)]. \quad (2.68)$$

In the case of SISO system, the identity matrix I equals 1. The denominator of the transfer functions will be the determinant of the matrix $[sI - A]$.

2.4.2 Average Modeling and Linearization

The required derivatives can be found based on the well-known relations between the voltage and current in the memory elements as follows:

$$\begin{aligned}\frac{di_{L-i}}{dt} &= \frac{1}{L_i} v_{L-i} \\ \frac{dv_{C-i}}{dt} &= \frac{1}{C_i} i_{C-i}\end{aligned}\quad (2.69)$$

The averaged state space can be found by computing the voltages across the inductors and currents flowing through the capacitors during the on-time and off-time and multiplying the on-time equations with the corresponding duty ratio and the off-time equations with the complement of the duty ratio and summing these together (cf. Eq. (2.70)). The averaged output variables are found in a similar manner (cf. Eq. (2.70)):

$$\begin{aligned}\frac{d\langle i_{L-i} \rangle}{dt} &= \frac{1}{L_i} (d_i v_{L-i-\text{on}} + d' i v_{L-i-\text{off}}), \\ \frac{d\langle v_{C-i} \rangle}{dt} &= \frac{1}{C_i} (d_i i_{C-i-\text{on}} + d' i_{C-i-\text{off}}), \\ \langle \hat{y}_i \rangle &= d_i \hat{y}_{i-\text{on}} + d' \hat{y}_{i-\text{off}}.\end{aligned}\quad (2.70)$$

The averaged state space can be highly nonlinear (i.e., it contains products of different variables or their inverses) and needs to be linearized. In power electronics, the recommended method is to substitute the averaged values by means of the sum of a DC value and small perturbation [44]. This method works well when the averaged model is only slightly nonlinear as in the case of continuous mode of operation but usually fails when the averaged model is highly nonlinear as in the case of discontinuous mode of operation. In control engineering [45], the linearization is typically carried out by computing the *Jacobian* matrix of the function $y = f(t, x)$, where x contains the state and input variables. The *Jacobian* matrix represents the partial derivatives of the function with respect to all the variables as follows:

$$\begin{aligned}\hat{y} &= \frac{\partial y}{\partial x_1} \cdot \hat{x}_1 + \cdots + \frac{\partial y}{\partial x_n} \cdot \hat{x}_n, \\ \hat{y} &= \begin{bmatrix} \frac{\partial f}{\partial x_1}(t, X) & \cdots & \frac{\partial f}{\partial x_n}(t, X) \end{bmatrix} \begin{bmatrix} \hat{x}_1 \\ \cdot \\ \cdot \\ \cdot \\ \hat{x}_n \end{bmatrix},\end{aligned}\quad (2.71)$$

where X in the Jacobian matrix contains the steady-state values of the corresponding variables at the operating point. As an example, we consider the function $y = v_{\text{in}}^2 i_{L-i} / v_{C-i}$, which is highly nonlinear function. We consider that

the steady-state values of the variables are V_{in} , I_L , and V_C , respectively. According to these assumptions, the linearized function \hat{y} can be given by

$$\hat{y} = \frac{V_{in}^2}{V_C} \cdot \hat{i}_L - \frac{V_{in}^2 I_L}{V_C^2} \cdot \hat{v}_C + \frac{2V_{in} I_L}{V_C} \cdot \hat{v}_{in}. \quad (2.72)$$

In practice, this means that we treat each variable at a time and consider the other variables to be constant when developing the required derivative applying basic mathematics.

DC-DC Converter Modeling Example

Figure 2.40 shows an ideal synchronous buck or stepdown converter, which will always operate in CCM due to the property of the MOSFET switches allowing also negative current to flow in the low-side switch (S_{LS}). The VF buck converter operates in such a way that the high-side MOSFET (S_{HS}) is turned on during the on-time (cf. Figure 2.41a), and the low-side MOSFET (S_{LS}) is turned on during the off-time (cf. Figure 2.41b). The input variables of the converter are v_{in} and i_o , the state variables are v_C and i_L and the output variables are v_o and i_{in} .

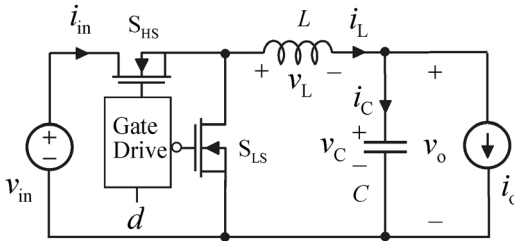


Figure 2.40 Synchronous buck converter.

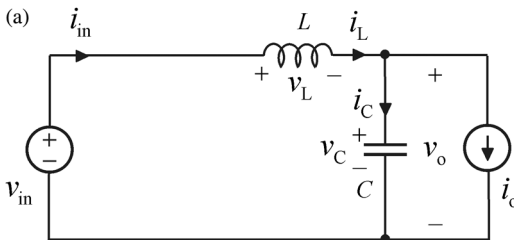
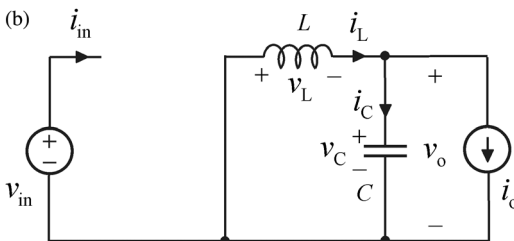


Figure 2.41 The subcircuits of the buck converter during (a) the on-time, and (b) the off-time.



In order to construct the averaged derivatives and output variables given in Eq. (2.70), we have to compute them first for the on- and off-time separately applying Kirchhoff's voltage and current laws. We can assume that i_L represents the time-varying average current directly because of CCM mode of operation (i.e., the charge distribution incorporated in the inductor current during the on- and off-times is directly related to the duty ratio d and its complement d' (i.e., $1 - d$) [5]). The ripple of the output capacitor is assumed to be small and, therefore, v_C represents directly the time-varying average voltage.

On-Time

$$\begin{aligned} v_L &= v_{in} - v_C, \\ i_C &= i_L - i_o, \\ i_{in} &= i_L, \\ v_o &= v_C. \end{aligned} \tag{2.73}$$

Off-Time

$$\begin{aligned} v_L &= -v_C, \\ i_C &= i_L - i_o, \\ i_{in} &= 0, \\ v_o &= v_C. \end{aligned} \tag{2.74}$$

The averaging is performed by multiplying the equations in Eq. (2.73) by d and the equations in Eq. (2.74) by $d'(1 - d)$ and adding them together, which yields

$$\begin{aligned} \langle v_L \rangle &= d \langle v_{in} \rangle - \langle v_C \rangle \\ \langle i_C \rangle &= \langle i_L \rangle - \langle i_o \rangle \\ \langle i_{in} \rangle &= d \langle i_L \rangle \\ \langle v_o \rangle &= \langle v_C \rangle \end{aligned} \tag{2.75}$$

and by applying Eq. (2.69)

$$\begin{aligned} \frac{d \langle i_L \rangle}{dt} &= \frac{d \langle v_{in} \rangle - \langle v_C \rangle}{L}, \\ \frac{d \langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle - \langle i_o \rangle}{C}, \\ \langle i_{in} \rangle &= d \langle i_L \rangle, \\ \langle v_o \rangle &= \langle v_C \rangle. \end{aligned} \tag{2.76}$$

The operating point of the converter can be solved from Eq. (2.76) by equating the derivatives to zero, and substituting the averaged variables by the corresponding DC values (i.e., capital letters). This procedure yields

$$\begin{aligned} V_C &= DV_{in}, \\ V_o &= V_C, \\ I_L &= I_o, \\ I_{in} &= DI_o. \end{aligned} \tag{2.77}$$

The averaged state space in Eq. (2.76) is nonlinear because of the products $d\langle v_{in} \rangle$ and $d\langle i_L \rangle$. It can be linearized applying Eq. (2.71), which yields

$$\begin{aligned}\frac{d\hat{i}_L}{dt} &= \frac{-\hat{v}_C + D\hat{v}_{in} + V_{in}\hat{d}}{L}, \\ \frac{d\hat{v}_C}{dt} &= \frac{\hat{i}_L - \hat{i}_o}{C}, \\ \hat{i}_{in} &= D\hat{i}_L + I_L\hat{d}, \\ \hat{v}_o &= \hat{v}_C.\end{aligned}\quad (2.78)$$

According to Eq. (2.65), the linearized state space in Eq. (2.78) can be presented in the time-domain matrix form (i.e., the variable vectors are denoted by superscript t) as follows:

$$\begin{aligned}\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix}^t &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix}^t + \begin{bmatrix} \frac{D}{L} & 0 & \frac{V_{in}}{L} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^t \\ \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix}^t &= \begin{bmatrix} D & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix}^t + \begin{bmatrix} 0 & 0 & I_L \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^t\end{aligned}\quad (2.79)$$

and in the frequency-domain matrix form (i.e., *Laplace* form, that is, the variable vectors are denoted by superscript s) as follows:

$$\begin{aligned}\begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix}^s &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix}^s + \begin{bmatrix} \frac{D}{L} & 0 & \frac{V_{in}}{L} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^s, \\ \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix}^s &= \begin{bmatrix} D & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix}^s + \begin{bmatrix} 0 & 0 & I_L \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^s.\end{aligned}\quad (2.80)$$

The transfer functions from the input variables to the state variables can be solved according to Eq. (2.67) yielding

$$\begin{aligned}\begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix}^s &= \left[s \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} - \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \right]^{-1} \begin{bmatrix} \frac{D}{L} & 0 & \frac{V_{in}}{L} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^s, \\ \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix}^s &= \frac{\begin{bmatrix} \frac{Ds}{L} & \frac{1}{LC} & \frac{V_{in}s}{L} \\ \frac{D}{LC} & -\frac{s}{C} & \frac{V_{in}}{LC} \end{bmatrix}}{s^2 + \frac{1}{LC}} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^s,\end{aligned}\quad (2.81)$$

where the transfer functions can be concluded based on the corresponding output and input variable pairs. The transfer functions from the input variables to the output variables can be solved according to Eq. (2.68) yielding

$$\begin{aligned} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix}^s &= \begin{bmatrix} D & 0 \\ 0 & 1 \end{bmatrix} \frac{\begin{bmatrix} \frac{Ds}{L} & \frac{1}{LC} & \frac{V_{in}s}{L} \\ \frac{D}{LC} & -\frac{s}{C} & \frac{V_{in}}{LC} \end{bmatrix}}{s^2 + \frac{1}{LC}} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^s + \begin{bmatrix} 0 & 0 & I_L \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^s \\ \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix}^s &= \frac{\begin{bmatrix} \frac{D^2s}{L} & \frac{D}{LC} & s^2I_L + s\frac{DV_{in}}{L} + \frac{I_L}{LC} \\ \frac{D}{LC} & -\frac{s}{C} & \frac{V_{in}}{LC} \end{bmatrix}}{s^2 + \frac{1}{LC}} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}^s \end{aligned} \quad (2.82)$$

where the transfer functions can be concluded based on the corresponding input- and output-variable pairs. The denominator of the transfer functions in Eqs. (2.81) and (2.82) is the determinant of $sI - A$, where I denotes the identity matrix (cf. the upper equation in Eq. (2.81)) and indicates also the order of the system (i.e., the maximum power of s corresponds to the number of memory elements in the system).

2.4.3 Modeling Coupled-Inductor Converters

In the converters, where the power stage contains two or more inductors such as the current-sourced or two-inductor buck converter [46–48] (cf. Figure 2.42), the input or output current can be made almost ripple-free by applying integrated magnetics technique [49]. When coupling the discrete inductors together, the flexibility of choosing the inductor values freely is naturally also lost. This can have detrimental effects on the converter dynamic behavior as explicitly described in Ref. [48] in case of PCM control.

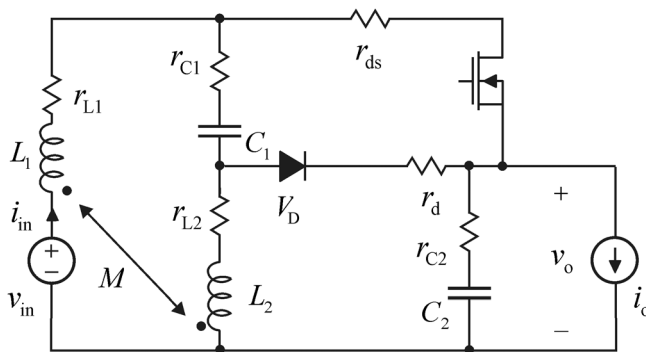


Figure 2.42 Coupled-inductor superbuck converter.

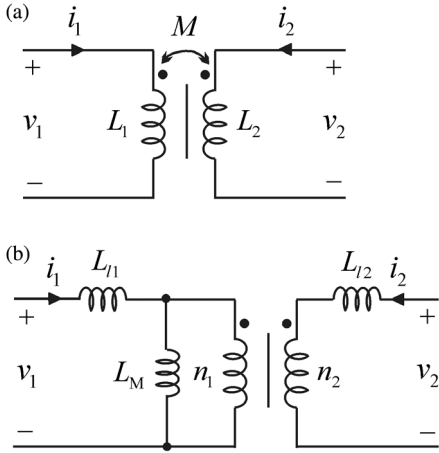


Figure 2.43 Definition of (a) a two-winding transformer and (b) its equivalent circuit.

The analysis of the coupled-inductor effects on the converter dynamics is based on the basic terminal equations of a nonideal transformer [50] (cf. Figure 2.43) given by

$$\begin{aligned} v_1 &= L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}, \\ v_2 &= M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}, \end{aligned} \quad (2.83)$$

where L_1 and L_2 are the self-inductances measured from the primary (v_1) and secondary (v_2) ports, respectively, when the other port is an open circuit, and M is the mutual inductance governing the transfer of energy between the primary and secondary as defined in Figure 2.43a. The equivalent circuit of such a transformer is given in Figure 2.43b, where L_{l1} and L_{l2} are the primary- and secondary-side leakage inductances, L_M is the primary-side magnetizing inductance, and n_1 and n_2 are the primary- and secondary-side number of turns in the corresponding windings of the ideal transformer. From Figure 2.43b, we can define that

$$\begin{aligned} L_1 &= L_{l1} + L_M, \\ L_2 &= L_{l2} + \left(\frac{n_2}{n_1}\right)^2 L_M, \\ M &= \frac{n_2}{n_1} L_M. \end{aligned} \quad (2.84)$$

The coupling coefficient (k) of a transformer is usually defined as $k = M/\sqrt{L_1 L_2}$ based on the total energy stored in the transformer [50]. Perfect coupling between the primary and secondary (i.e., $k = 1$) means that leakage inductances (L_{li}) are zero.

The small-signal representation of the coupled-inductor converter can be constructed from the small-signal state space of the original converter defined with the discrete inductors L_1 and L_2 taking into account that the voltages across the inductors do not change. Therefore, if we denote the original derivatives of the

inductor currents by \hat{D}_{L1} and \hat{D}_{L2} and apply the information given in Eq. (2.83), the coupled-inductor-affected derivatives can be given by [5]

$$\begin{aligned}\frac{d\hat{i}_{L1}}{dt} &= \frac{\hat{D}_{L1} - (M/L_1)\hat{D}_{L2}}{1 - (M^2/L_1L_2)} = \frac{\hat{D}_{L1} - (M/L_1)\hat{D}_{L2}}{1 - k^2}, \\ \frac{d\hat{i}_{L2}}{dt} &= \frac{\hat{D}_{L2} - (M/L_2)\hat{D}_{L1}}{1 - (M^2/L_1L_2)} = \frac{\hat{D}_{L2} - (M/L_2)\hat{D}_{L1}}{1 - k^2}.\end{aligned}\quad (2.85)$$

From Eq. (2.85), we may conclude that the perfect coupling ($k = 1$) would lead to infinite derivatives indicating the existence of high-current spikes during the transients.

2.4.4 Modeling in Synchronous Reference Frame

The dynamic modeling of three-phase grid-connected converters is a little bit more complicated than the modeling of the DC–DC converters, but basically obey the same principles described in Section 2.4.1 and follows the same steps as described in Section 2.4.2. The main problem is that the sinusoidal signals are time-varying signals, and, therefore, there is no time-invariant steady-state operation point to be defined. Such a situation can be, however, created by transforming the three-phase signals first into stationary reference frame (i.e., $\alpha\beta$ or *Clarke* transformation) applying space vectors [27], where the three-phase variables are transformed into two-phase variables rotating at the same angular frequency ω_s as the three-phase variables. The stationary frame variables can be further transformed into the synchronous reference frame (i.e., dqz or *Park* transformation) [28], where the variables are DC variables, and, therefore, the steady-state operating point can be defined explicitly. This actually means that the synchronous reference frame is rotating at the angular frequency ω_s and, therefore, the variables are effectively DC variables. This also means that the grid frequency is shifted to origin. In order to understand and perform the dynamic modeling of three-phase converters, the above-described transformation methods are described in the following sections.

Space Vector Theory

Space vector theory was originally developed as a tool to analyze the transient states in electrical machines [28]. According to the theory, the three-phase quantities can be modeled as equivalent two-phase quantities using space vectors [29]. The complex space vector associated with a set of phase quantities $\{x_a, x_b, x_c\}$ is given by

$$\underline{x} = \frac{2K}{3}(x_a + e^{j2\pi/3}x_b + e^{j3\pi/4}x_c) = x_\alpha + jx_\beta \quad (2.86)$$

and the corresponding zero or common-mode component by

$$x_z = \frac{1}{3}(x_a + x_b + x_c), \quad (2.87)$$

where the scaling factor K is chosen as $\{1, \sqrt{1/2}, \sqrt{3/2}\}$ for peak value, root mean square value, and power invariant scaling [29]. If the peak amplitude of the

sinusoidal signal transformed into space vector equals \underline{X} , then the space vector $\underline{x} = \underline{KX}e^{j\omega_s t}$. The instantaneous power p of a three-phase system can be given by means of the stationary components of voltage and current as follows [51]:

$$\begin{aligned} p_{\text{abc}} &= v_a i_a + v_b i_b + v_c i_c, \\ p_{\alpha\beta} &= \frac{3}{2K^2} (v_\alpha i_\alpha + v_\beta i_\beta) + 3v_z i_z. \end{aligned} \quad (2.88)$$

The *Clarke* transformation in Eq. (2.86) can be given in matrix form as follows:

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_z \end{bmatrix} = \frac{2K}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2K} & \frac{1}{2K} & \frac{1}{2K} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (2.89)$$

The space vectors can be transformed back into the three-phase variables by using the inverse of *Clarke* transformation as follows:

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \frac{3}{2K} \begin{bmatrix} \frac{2}{3} & 0 & \frac{2K}{3} \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} & \frac{2K}{3} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} & \frac{2K}{3} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_z \end{bmatrix} \quad (2.90)$$

The two-phase signals in stationary reference can be transformed into the synchronous reference frame as follows:

$$\begin{aligned} \underline{x}^s &= \underline{x} e^{-j\omega_s t}, \\ x_z &= \frac{1}{3}(x_a + x_b + x_c), \end{aligned} \quad (2.91)$$

which can be expressed in matrix form as follows:

$$\begin{bmatrix} x_d \\ x_q \\ x_z \end{bmatrix} = \begin{bmatrix} \cos \omega_s t & \sin \omega_s t & 0 \\ -\sin \omega_s t & \cos \omega_s t & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_z \end{bmatrix} \quad (2.92)$$

The synchronous reference frame signals can be transferred back to the stationary reference frame as follows:

$$\begin{aligned} \underline{x} &= \underline{x}^s e^{j\omega_s t}, \\ x_z &= \frac{1}{3}(x_a + x_b + x_c), \end{aligned} \quad (2.93)$$

which can be given in matrix form as follows:

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_z \end{bmatrix} = \begin{bmatrix} \cos \omega_s t & -\sin \omega_s t & 0 \\ \sin \omega_s t & \cos \omega_s t & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_z \end{bmatrix} \quad (2.94)$$

The Clarke and Park transformations and their inverses can be combined as follows:

$$\begin{bmatrix} x_d \\ x_q \\ x_z \end{bmatrix} = \frac{2K}{3} \begin{bmatrix} \cos \omega_s t & \cos \left(\omega_s t - \frac{2\pi}{3} \right) & \cos \left(\omega_s t - \frac{4\pi}{3} \right) \\ -\sin \omega_s t & -\sin \left(\omega_s t - \frac{2\pi}{3} \right) & -\sin \left(\omega_s t - \frac{4\pi}{3} \right) \\ \frac{1}{2K} & \frac{1}{2K} & \frac{1}{2K} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (2.95)$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \frac{3}{2K} \begin{bmatrix} \cos \omega_s t & -\sin \omega_s t & \frac{2K}{3} \\ \cos \left(\omega_s t - \frac{2\pi}{3} \right) & -\sin \left(\omega_s t - \frac{2\pi}{3} \right) & \frac{2K}{3} \\ \cos \left(\omega_s t - \frac{4\pi}{3} \right) & \sin \left(\omega_s t - \frac{4\pi}{3} \right) & \frac{2K}{3} \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_z \end{bmatrix} \quad (2.96)$$

The transformations of the phase voltages (v_a , v_b , v_c) to the corresponding $\alpha\beta$ - and dq -components are shown in Figures 2.44–2.46 applying amplitude invariance (Figure 2.44), RMS invariance (Figure 2.45), and power invariance (Figure 2.46), respectively. It is obvious that the different invariances yield as the peak of the $\alpha\beta$ -components as $x = KXe^{j\omega_s t}$ [29], where K equals $\{1, \sqrt{1/2}, \sqrt{3/2}\}$ for the invariances in the order they are named above. When the three-phase system is balanced (i.e., the amplitudes of the variables are the same), the quadrature (q) component will be mapped to zero as is visible in Figures 2.44–2.46. The figures also indicate that the direct (d) component is mapped always to the peak of the $\alpha\beta$ -components, which are varying in terms of the used invariance scheme.

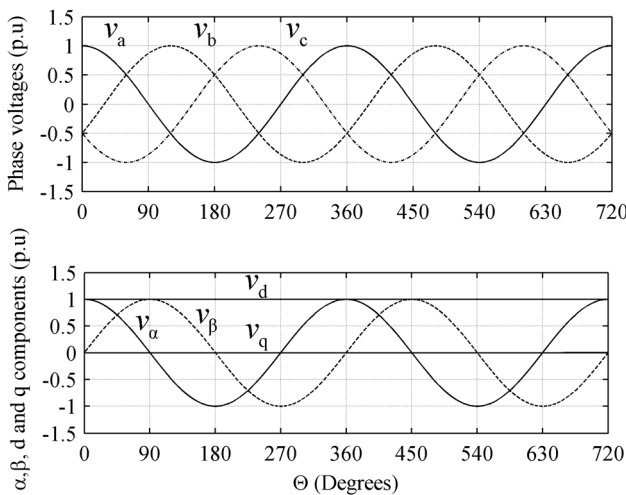


Figure 2.44 Amplitude-invariant transformations.

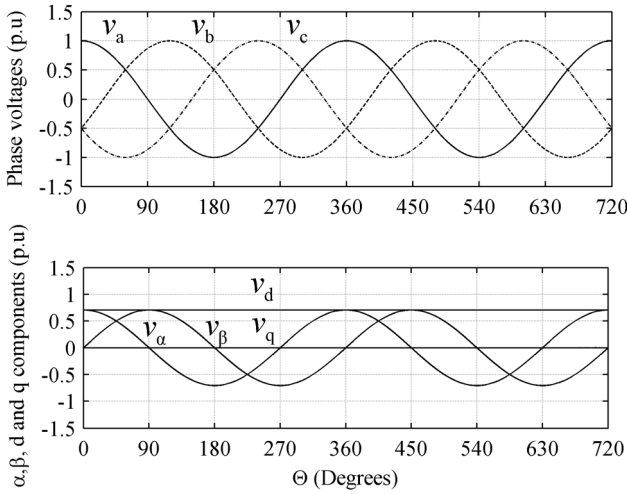


Figure 2.45 RMS-invariant transformations.

Three-Phase Converter Modeling Example

Figure 2.47 shows a three-phase grid-connected rectifier or AC–DC converter, which is basically boost- or step-up-type converter. The converter is assumed to operate in CCM. The input variables are the three-phase grid voltages $\{v_{an}, v_{bn}, v_{cn}\}$ and the output current i_{dc} , the state variables are the inductor currents $\{i_{La}, i_{Lb}, i_{Lc}\}$, and the output variables the three-phase grid currents $\{i_{ina}, i_{inb}, i_{inc}\}$ and the output voltage v_{dc} . The control variables are the duty ratios $\{d_a, d_b, d_c\}$ of the high-side IGBT switches as depicted in Figure 2.47.

In a similar manner as in the case of DC–DC converter dynamic modeling, we have to construct the time-averaged derivatives of state variables and the time-averaged values of the output variables (cf. Eq. (2.70)). Therefore, we consider

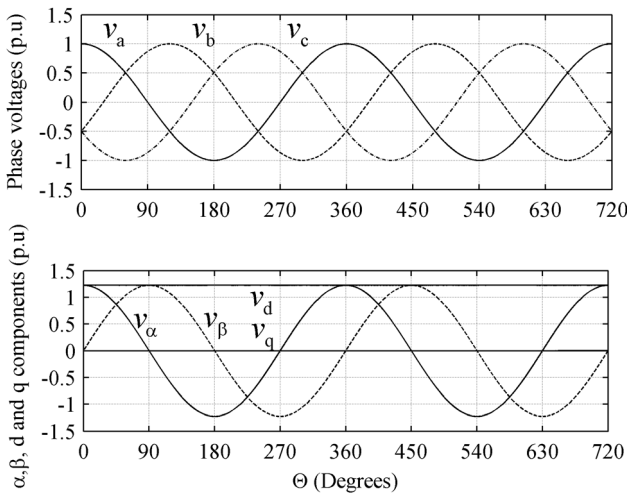


Figure 2.46 Power-invariant transformations.

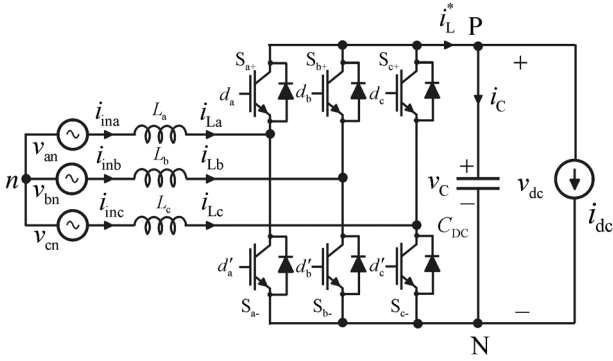


Figure 2.47 Ideal three-phase grid-connected rectifier.

each of the phase legs {a, b, c} of IGBT bridge separately. We assume also that the inductors $L_{a,b,c} = L$.

On-Time

$$\begin{aligned} v_{La} &= v_{an} - v_C + v_{Nn}, \\ v_{Lb} &= v_{bn} - v_C + v_{Nn}, \\ v_{Lc} &= v_{cn} - v_C + v_{Nn}, \end{aligned}$$

$$\begin{aligned} i_L^* &= i_{La} + i_{Lb} + i_{Lc}, \\ i_C &= i_L^* - i_{dc}, \end{aligned} \quad (2.97)$$

$$\begin{aligned} i_{ina} &= i_{La}, \\ i_{inb} &= i_{Lb}, \\ i_{inc} &= i_{Lc}, \\ v_{dc} &= v_C. \end{aligned}$$

Off-Time

$$\begin{aligned} v_{La} &= v_{an} + v_{Nn}, \\ v_{Lb} &= v_{bn} + v_{Nn}, \\ v_{Lc} &= v_{cn} + v_{Nn}, \end{aligned}$$

$$\begin{aligned} i_L^* &= 0, \\ i_C &= -i_{dc}, \end{aligned} \quad (2.98)$$

$$\begin{aligned} i_{ina} &= i_{La}, \\ i_{inb} &= i_{Lb}, \\ i_{inc} &= i_{Lc}, \\ v_{dc} &= v_C. \end{aligned}$$

The averaging is performed by multiplying the equations in Eq. (2.97) by $d_{a,b,c}$ and the equations in Eq. (2.98) by $d'_{a,b,c}$ and summing them together, which yields

$$\begin{aligned}
 \langle v_{La} \rangle &= \langle v_{an} \rangle - d_a \langle v_C \rangle + \langle v_{Nn} \rangle, \\
 \langle v_{Lb} \rangle &= \langle v_{bn} \rangle - d_b \langle v_C \rangle + \langle v_{Nn} \rangle, \\
 \langle v_{Lc} \rangle &= \langle v_{cn} \rangle - d_c \langle v_C \rangle + \langle v_{Nn} \rangle, \\
 \langle i_L^* \rangle &= d_a \langle i_{La} \rangle + d_b \langle i_{Lb} \rangle + d_c \langle i_{Lc} \rangle, \\
 \langle i_C \rangle &= \langle i_L^* \rangle - \langle i_{dc} \rangle,
 \end{aligned} \tag{2.99}$$

$$\begin{aligned}
 \langle i_{ina} \rangle &= \langle i_{La} \rangle, \\
 \langle i_{inb} \rangle &= \langle i_{Lb} \rangle, \\
 \langle i_{inc} \rangle &= \langle i_{Lc} \rangle, \\
 \langle v_{dc} \rangle &= \langle v_C \rangle,
 \end{aligned}$$

and by applying Eq. (2.69)

$$\begin{aligned}
 \frac{d\langle i_{La} \rangle}{dt} &= \frac{\langle v_{an} \rangle - d_a \langle v_C \rangle + \langle v_{Nn} \rangle}{L}, \\
 \frac{d\langle i_{Lb} \rangle}{dt} &= \frac{\langle v_{bn} \rangle - d_b \langle v_C \rangle + \langle v_{Nn} \rangle}{L}, \\
 \frac{d\langle i_{Lc} \rangle}{dt} &= \frac{\langle v_{cn} \rangle - d_c \langle v_C \rangle + \langle v_{Nn} \rangle}{L}, \\
 \frac{d\langle v_C \rangle}{dt} &= \frac{d_a \langle i_{La} \rangle + d_b \langle i_{Lb} \rangle + d_c \langle i_{Lc} \rangle - \langle i_{dc} \rangle}{C},
 \end{aligned} \tag{2.100}$$

$$\begin{aligned}
 \langle i_{ina} \rangle &= \langle i_{La} \rangle, \\
 \langle i_{inb} \rangle &= \langle i_{Lb} \rangle, \\
 \langle i_{inc} \rangle &= \langle i_{Lc} \rangle, \\
 \langle v_{dc} \rangle &= \langle v_C \rangle.
 \end{aligned}$$

The averaged state space in Eq. (2.100) can be presented in a more convenient form for facilitating the transformation from the phase domain to the $\alpha\beta$ domain as follows:

$$\frac{d}{dt} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} = -\frac{1}{L} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} \langle v_C \rangle + \frac{1}{L} \begin{bmatrix} \langle v_{an} \rangle \\ \langle v_{bn} \rangle \\ \langle v_{cn} \rangle \end{bmatrix} + \frac{1}{L} \begin{bmatrix} \langle v_{Nn} \rangle \\ \langle v_{Nn} \rangle \\ \langle v_{Nn} \rangle \end{bmatrix}, \tag{2.101}$$

$$\frac{d\langle v_C \rangle}{dt} = \frac{1}{C} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} - \frac{\langle i_{dc} \rangle}{C}, \tag{2.102}$$

$$\begin{aligned} \begin{bmatrix} \langle i_{in-a} \rangle \\ \langle i_{in-b} \rangle \\ \langle i_{in-c} \rangle \end{bmatrix} &= \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} \\ \langle v_{dc} \rangle &= \langle v_C \rangle \end{aligned} \quad (2.103)$$

If the grid voltages and currents are in balance, then the common-mode components of voltages and currents (cf. Eq. (2.87)) are zero. As a consequence, the Clarke transformation matrix can be given by

$$T_{\alpha\beta} = \frac{2K}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \quad (2.104)$$

The inductor-current derivatives in Eq. (2.101) are transferred into $\alpha\beta$ -domain or as rotating space vectors as follows:

$$\begin{aligned} \underbrace{\frac{d}{dt} T_{\alpha\beta} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix}}_{\mathbf{i}_L^{\alpha\beta}} &= -\frac{1}{L} \underbrace{T_{\alpha\beta} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}}_{\mathbf{d}^{\alpha\beta}} \langle v_C \rangle + \frac{1}{L} \underbrace{T_{\alpha\beta} \begin{bmatrix} \langle v_{an} \rangle \\ \langle v_{bn} \rangle \\ \langle v_{cn} \rangle \end{bmatrix}}_{\mathbf{v}_{in}^{\alpha\beta}} + \frac{1}{L} \underbrace{T_{\alpha\beta} \begin{bmatrix} \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \end{bmatrix}}_0, \\ \frac{d}{dt} \langle \mathbf{i}_L^{\alpha\beta} \rangle &= -\frac{\mathbf{d}^{\alpha\beta} \langle v_C \rangle}{L} + \frac{\langle \mathbf{v}_{in}^{\alpha\beta} \rangle}{L}. \end{aligned} \quad (2.105)$$

The transformation of the capacitor-voltage derivative in Eq. (2.102) requires considering the product of two space vectors similarly as the active power in Eq. (2.88). According to Eq. (2.88), we can write

$$\begin{aligned} \frac{d\langle v_C \rangle}{dt} &= \frac{3}{2K^2} \frac{(d_\alpha \langle i_{L\alpha} \rangle + d_\beta \langle i_{L\beta} \rangle)}{C} - \frac{\langle i_{dc} \rangle}{C}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{3}{2K^2} \frac{\text{Re}(\langle \mathbf{d}^{\alpha\beta} \rangle \langle \mathbf{i}_L^{\alpha\beta} \rangle^*)}{C} - \frac{\langle i_{dc} \rangle}{C}, \end{aligned} \quad (2.106)$$

where the superscript “*” denotes the complex conjugate of the corresponding variable.

The transformation of the output variables will yield as follows:

$$\begin{aligned} T_{\alpha\beta} \begin{bmatrix} \langle i_{ina} \rangle \\ \langle i_{inb} \rangle \\ \langle i_{inc} \rangle \end{bmatrix} &= T_{\alpha\beta} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix}, \\ \langle \mathbf{i}_{in}^{\alpha\beta} \rangle &= \langle \mathbf{i}_L^{\alpha\beta} \rangle, \\ \langle v_{dc} \rangle &= \langle v_C \rangle. \end{aligned} \quad (2.107)$$

The transformation to the rotating reference frame or dq -domain will be performed by multiplying the rotating space vectors by $e^{-j\omega_s t}$ that yields

$\underline{x}^{\alpha\beta} = \underline{x}^{dq} e^{j\omega_s t}$. As a consequence of this, the averaged state space in dq -domain can be given by as follows:

$$\begin{aligned} \frac{d}{dt}(\langle \mathbf{i}_{\mathbf{L}}^{dq} \rangle e^{j\omega_s t}) &= -\frac{\mathbf{d}^{dq} e^{j\omega_s t} \langle v_C \rangle}{L} + \frac{\langle \mathbf{v}_{\mathbf{in}}^{dq} \rangle e^{j\omega_s t}}{L}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{3}{2K^2} \frac{(d_d \langle i_{Ld} \rangle + d_q \langle i_{Lq} \rangle)}{C} - \frac{\langle i_{dc} \rangle}{C}, \\ \langle \mathbf{i}_{\mathbf{in}}^{dq} \rangle e^{j\omega_s t} &= \langle \mathbf{i}_{\mathbf{L}}^{dq} \rangle e^{j\omega_s t}, \\ \langle v_{dc} \rangle &= \langle v_C \rangle. \end{aligned} \quad (2.108)$$

The term $e^{j\omega_s t}$ is inside the derivative in the upper equation in Eq. (2.108) and, therefore, the derivation operation has to be performed, which yields

$$\begin{aligned} \frac{d\langle \mathbf{i}_{\mathbf{L}}^{dq} \rangle}{dt} &= -j\omega_s \langle \mathbf{i}_{\mathbf{L}}^{dq} \rangle - \frac{\mathbf{d}^{dq} \langle v_C \rangle}{L} + \frac{\langle \mathbf{v}_{\mathbf{in}}^{dq} \rangle}{L}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{3}{2K^2} \frac{(d_d \langle i_{Ld} \rangle + d_q \langle i_{Lq} \rangle)}{C} - \frac{\langle i_{dc} \rangle}{C}, \\ \langle \mathbf{i}_{\mathbf{in}}^{dq} \rangle &= \langle \mathbf{i}_{\mathbf{L}}^{dq} \rangle, \\ \langle v_{dc} \rangle &= \langle v_C \rangle. \end{aligned} \quad (2.109)$$

By collecting the d and q components separately into the state space, the averaged state space can be given as follows:

$$\begin{aligned} \frac{d\langle i_{Ld} \rangle}{dt} &= \omega_s \langle i_{Lq} \rangle - \frac{d_d \langle v_C \rangle}{L} + \frac{\langle v_{ind} \rangle}{L}, \\ \frac{d\langle i_{Lq} \rangle}{dt} &= -\omega_s \langle i_{Ld} \rangle - \frac{d_q \langle v_C \rangle}{L} + \frac{\langle v_{inq} \rangle}{L}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{3}{2K^2} \frac{(d_d \langle i_{Ld} \rangle + d_q \langle i_{Lq} \rangle)}{C} - \frac{\langle i_{dc} \rangle}{C}, \\ \langle i_{ind} \rangle &= \langle i_{Ld} \rangle, \\ \langle i_{inq} \rangle &= \langle i_{Lq} \rangle, \\ \langle v_{dc} \rangle &= \langle v_C \rangle. \end{aligned} \quad (2.110)$$

The steady-state values of the operating point variables can be solved from Eq. (2.110) by equating the derivatives to zero, which yields

$$\begin{cases} \omega_s L I_{Lq} - D_d V_C + V_{ind} = 0 \\ -\omega_s L I_{Ld} - D_q V_C + V_{inq} = 0 \\ \frac{3}{2K^2} (D_d I_{Ld} + D_q I_{Lq}) - I_{dc} = 0 \\ I_{ind} = I_{Ld} \\ I_{inq} = I_{Lq} \\ V_{dc} = V_C \end{cases} \quad (2.111)$$

In the case of balanced grid, $V_{inq} = 0$ and if we assume that the converter is operating at unity power factor, then $I_{inq} = 0$. Thus, the operating point can be

further manipulated to be as follows:

$$\begin{cases} V_{dc} = V_C = \frac{V_{ind}}{D_d} \\ I_{ind} = I_{Ld} = \frac{2K^2 I_{dc}}{3 D_d} \end{cases} \quad (2.112)$$

or if V_{dc} is known, then

$$\begin{cases} D_d = \frac{V_{ind} + (2K^2/3)I_{dc}\omega_s L}{V_{dc}} \\ I_{ind} = I_{Ld} = \frac{2K^2 I_{dc} V_{dc}}{3 V_{ind} + (2K^2/3)I_{dc}\omega_s L} \end{cases} \quad (2.113)$$

where $K = \{1, \sqrt{1/2}, \sqrt{3/2}\}$ depending on the chosen invariance (see Section 2.4.4) and V_{ind} as well as I_{ind} equal their corresponding grid phase values as KX , where X is the peak amplitude of the corresponding grid variable.

The state space in Eq. (2.110) is nonlinear and it has to be linearized by applying Eq. (2.71,) which yields

$$\begin{aligned} \frac{d\hat{i}_{Ld}}{dt} &= \omega_s \hat{i}_{Lq} - \frac{D_d}{L} \hat{v}_C + \frac{1}{L} \hat{v}_{ind} - \frac{V_C}{L} \hat{d}_d, \\ \frac{d\hat{i}_{Lq}}{dt} &= -\omega_s \hat{i}_{Ld} - \frac{D_q}{L} \hat{v}_C + \frac{1}{L} \hat{v}_{inq} - \frac{V_C}{L} \hat{d}_q, \\ \frac{d\hat{v}_C}{dt} &= \frac{3}{2K^2} \frac{D_d}{C} \hat{i}_{Ld} + \frac{3}{2K^2} \frac{D_q}{C} \hat{i}_{Lq} - \frac{1}{C} \hat{i}_{dc} + \frac{3}{2K^2} \frac{I_{Ld}}{C} \hat{d}_d + \frac{3}{2K^2} \frac{I_{Lq}}{C} \hat{d}_q, \\ \hat{i}_{ind} &= \hat{i}_{Ld}, \\ \hat{i}_{inq} &= \hat{i}_{Lq}, \\ \hat{v}_{dc} &= \hat{v}_C. \end{aligned} \quad (2.114)$$

The state space can also be given in the standard matrix form in time domain (i.e., the variable vectors are denoted by the superscript t) according to Eq. (2.65) as follows:

$$\begin{aligned} \begin{bmatrix} \frac{d\hat{i}_{Ld}}{dt} \\ \frac{d\hat{i}_{Lq}}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix}^t &= \begin{bmatrix} 0 & \omega_s & -\frac{D_d}{L} \\ -\omega_s & 0 & -\frac{D_q}{L} \\ \frac{3}{2K^2} \frac{D_d}{C} & \frac{3}{2K^2} \frac{D_q}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix}^t + \begin{bmatrix} \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} & 0 \\ 0 & \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} \\ 0 & 0 & -\frac{1}{C} & \frac{3}{2K^2} \frac{I_{Ld}}{C} & \frac{3}{2K^2} \frac{I_{Lq}}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{dc} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}^t \\ \begin{bmatrix} \hat{i}_{ind} \\ \hat{i}_{inq} \\ \hat{v}_{dc} \end{bmatrix}^t &= \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix}^t + \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{dc} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}^t \end{aligned} \quad (2.115)$$

and in frequency domain (in *Laplace* form) (i.e., the variable vectors are denoted by the superscript s) as follows:

$$\begin{aligned}
 s \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} &= \begin{bmatrix} 0 & \omega_s & -\frac{D_d}{L} \\ -\omega_s & 0 & -\frac{D_q}{L} \\ \frac{3 D_d}{2K^2 C} & \frac{3 D_q}{2K^2 C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} & 0 \\ 0 & \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} \\ 0 & 0 & -\frac{1}{C} & \frac{3 I_{Ld}}{2K^2 C} & \frac{3 I_{Lq}}{2K^2 C} \end{bmatrix} \begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{dc} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}^s \\
 \begin{bmatrix} \hat{i}_{ind} \\ \hat{i}_{inq} \\ \hat{v}_{dc} \end{bmatrix}^s &= \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix}^s + \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{dc} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}^s
 \end{aligned} \tag{2.116}$$

The transfer functions from the input variables to the state variables can be solved according to Eq. (2.67) yielding

$$\begin{aligned}
 \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix}^s &= s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} - \begin{bmatrix} 0 & \omega_s & -\frac{D_d}{L} \\ -\omega_s & 0 & -\frac{D_q}{L} \\ \frac{3 D_d}{2K^2 C} & \frac{3 D_q}{2K^2 C} & 0 \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} & 0 \\ 0 & \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} \\ 0 & 0 & -\frac{1}{C} & \frac{3 I_{Ld}}{2K^2 C} & \frac{3 I_{Lq}}{2K^2 C} \end{bmatrix} \begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{dc} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}^s \\
 \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix}^s &= \begin{bmatrix} G_{11} & G_{12} & G_{13} & G_{14} & G_{15} \\ G_{21} & G_{22} & G_{23} & G_{24} & G_{25} \\ G_{31} & G_{32} & -G_{33} & G_{34} & G_{35} \end{bmatrix} \begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{dc} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}^s
 \end{aligned} \tag{2.117}$$

where the inductor-current d -component-related transfer functions are given by

$$\begin{aligned}
 \Delta G_{11} &= \frac{1}{L} \left(s^2 + \frac{3 D_q^2}{2K^2 LC} \right), \\
 \Delta G_{12} &= \frac{\omega_s}{L} \left(s - \frac{3 D_d D_q}{2K^2 \omega_s LC} \right), \\
 \Delta G_{13} &= \frac{D_d}{LC} \left(s + \frac{D_q \omega_s}{D_d} \right), \\
 \Delta G_{14} &= -\frac{V_C}{L} \left(s^2 + s \frac{3 D_d I_{Ld}}{2K^2 C V_C} + \frac{3 D_q}{2K^2 C} \left(\frac{D_q}{L} + \frac{I_{Ld} \omega_s}{V_C} \right) \right), \\
 \Delta G_{15} &= -\frac{V_C}{L} \left(s \left(\frac{3 D_d I_{Lq}}{2K^2 V_C C} + \omega_s \right) + \frac{3}{2K^2 C} \left(\frac{D_q I_{Lq} \omega_s}{V_C} - \frac{D_d D_q}{L} \right) \right),
 \end{aligned} \tag{2.118}$$

and the inductor-current q -component-related transfer functions by

$$\begin{aligned}
 \Delta G_{21} &= -\frac{\omega_s}{L} \left(s + \frac{3 D_d D_q}{2K^2 LC \omega_s} \right), \\
 \Delta G_{22} &= \frac{1}{L} \left(s^2 + \frac{3 D_d^2}{2K^2 LC} \right), \\
 \Delta G_{23} &= \frac{D_q}{LC} \left(s - \frac{D_d \omega_s}{D_q} \right), \\
 \Delta G_{24} &= -\frac{V_C}{L} \left(s \left(\frac{3 D_q I_{Ld}}{2K^2 C V_C} - \omega_s \right) - \frac{3D_d}{2K^2 C} \left(\frac{D_q}{L} + \frac{L_{Ld} \omega_s}{V_C} \right) \right), \\
 \Delta G_{25} &= -\frac{V_C}{L} \left(s^2 + s \frac{3 D_q I_{Lq}}{2K^2 V_C} - \frac{3D_d}{2K^2 C} \left(\frac{D_d}{L} - \frac{I_{Lq} \omega_s}{V_C} \right) \right),
 \end{aligned} \tag{2.119}$$

as well as the output-side dynamics-related transfer functions by

$$\begin{aligned}
 \Delta G_{31} &= \frac{3D_d}{2K^2 LC} \left(s - \frac{D_q \omega_s}{D_d} \right), \\
 \Delta G_{32} &= \frac{3D_q}{2K^2 LC} \left(s + \frac{D_d \omega_s}{D_q} \right), \\
 \Delta G_{33} &= \frac{1}{C} (s^2 + \omega_s^2), \\
 \Delta G_{34} &= \frac{3I_{Ld}}{2K^2 C} \left(s^2 - s \frac{D_d V_C}{L I_{Ld}} + \omega_s \left(\omega_s + \frac{D_q V_C}{L I_{Ld}} \right) \right), \\
 \Delta G_{35} &= \frac{3I_{Lq}}{2K^2 C} \left(s^2 - s \frac{D_q V_C}{L I_{Lq}} + \omega_s \left(\omega_s - \frac{D_d V_C}{L I_{Lq}} \right) \right).
 \end{aligned} \tag{2.120}$$

Δ in Eqs. (2.118)–(2.120) is the denominator of the transfer functions, which can be given by

$$\Delta = s^3 + s \left(\frac{3}{2K^2} \frac{(D_d^2 + D_q^2)}{LC} + \omega_s^2 \right) \tag{2.121}$$

where the individual transfer functions can be concluded based on the corresponding output- and input-variable pairs. The transfer functions from the input variables to the output variables can be solved according to Eq. (2.68) yielding actually the same sets of transfer functions as given in Eqs. (2.118)–(2.120), because

$$\begin{bmatrix} \hat{i}_{\text{ind}} \\ \hat{i}_{\text{inq}} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix}. \tag{2.122}$$

It is quite obvious that the state space of three-phase converters cannot be anymore solved manually in practice, but proper software packages such as Matalab™ Symbolic Toolbox having capability to solve symbolic equations are needed.

2.5 Control Design Preliminaries

2.5.1 Introduction

Control engineering is usually quite poorly understood and mastered in power electronics. The control engineering textbooks and especially, the advanced control engineering books, are quite difficult to understand for those who are not experts in control engineering. This is because the control engineering professionals and scholars utilize effectively linear algebra (e.g., matrix properties) to justify the results. If not fully familiar with those items, the text is not transparent for understanding the given point. We have tried to give simple and explicit information for performing effective control design and understanding, especially the frequency responses and the limitations imposed by certain anomalies. In this constellation, the behavior of different transfer functions, the concept of stability in SISO and MIMO systems, and its evaluation as well as the limitations the abnormal (i.e., RHP) poles and zeros will impose on control design are very vital to understand. In addition to these, we also introduce certain items related to the transient performance.

2.5.2 Transfer Functions

A transfer function is usually given as a ratio of two polynomials in s (cf. Eq. (2.123)), where s is the *Laplace* variable. The roots of the numerator polynomial ω_{zi} are called zeros, and the roots of the denominator polynomial ω_{pi} poles. The zeros and poles may be real or complex numbers, and they are given with respect to angular frequency ω (rad/s). The frequency (f) in Hz and the angular frequency (ω) in rad/s are related by $f = \omega/2\pi$:

$$G(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \dots + a_0}{b_m s^m + b_{m-1} s^{m-1} + \dots + b_0}, \quad (2.123)$$

$$G(s) = K \cdot \frac{(s + \omega_{z1})(s + \omega_{z2}) \dots (s + \omega_{zn})}{(s + \omega_{p1})(s + \omega_{p2}) \dots (s + \omega_{pm})},$$

The magnitude of the transfer function ($|G(s)|$) is commonly expressed in dB, that is, $|G(s)|_{\text{dB}} = 20 \log_{10}|G(s)|$, and the phase ($\angle G(s)$) in degrees. The logarithmic magnitude means that the combined effect of zeros and poles can be found by adding together the dB values of the zeros and subtracting the dB values of the poles, respectively. The phase of the transfer function can be found similarly adding together the phase contributions of the zeros, and subtracting the phase contributions of the poles. The zeros and poles located closest to the origin (i.e., zero frequency) are called dominant zeros and poles having the strongest effect on the time-domain behavior of the corresponding system. As a consequence of this, the time-domain responses do not give accurate information on the dynamic properties of the system. In order to understand the effect of different types of transfer functions in the dynamic behavior and especially on the control design, the normal (i.e., the zeros and poles locate on the left half plane (LHP) of the complex plane) and abnormal (i.e., the zeros and poles locate on the right half plane (RHP) of the complex plane) behaviors shall be able to be recognized in the behavior of the transfer functions as described in the following subsections.

Single Zero

Let us consider the single-zero transfer function of the form $G(s) = 1 + s/\omega_z$. Its magnitude (i.e., $|G(s)| = \sqrt{1 + (\omega^2/\omega_z^2)}$) and phase (i.e., $\angle G(s) = \arctan(\omega/\omega_z)$) may be given at certain interesting angular frequency points as follows:

$$\begin{aligned} \omega &= \frac{\omega_z}{10}, \\ |G(s)|_{\text{dB}} &= 20 \log_{10}(\sqrt{1.01}) = 0.04 \text{ dB}, \\ \angle G(s) &= \arctan(0.1) = 5.7^\circ, \\ \omega &= \omega_z, \\ |G(s)|_{\text{dB}} &= 20 \log_{10}(\sqrt{2}) = 3 \text{ dB}, \\ \angle G(s) &= \arctan(1) = 45^\circ, \\ \omega &= 10\omega_z, \\ |G(s)|_{\text{dB}} &= 20 \log_{10}(\sqrt{101}) \approx 20 \text{ dB}, \\ \angle G(s) &= \arctan(10) = 84.3^\circ. \end{aligned}$$

As a consequence, the behavior of the single-zero transfer functions (cf. Figure 2.48) is typically considered to be such that its magnitude is unity (i.e., 0 dB) up to $\omega = \omega_z$, and starts increasing at a slope of +20 dB/decade (i.e., +20 dB for a 10 times increase in frequency) from $\omega = \omega_z$. Its phase is zero up to $\omega = \omega_z/10$, and starts increasing at a slope of +45°/decade up to $\omega = 10\omega_z$, and stays constant at 90° thereafter. The phase equals exactly +45° at $\omega = \omega_z$. This is the best point to locate exactly ω_z . If $G(s) = 1 - s/\omega_z$, the magnitude behavior is same, but the phase has the negative sign compared to $G(s) = 1 + s/\omega_z$ (i.e., the slope is -45°/decade and it will finally stay at -90°). If $s = -\omega_z$, then the zero is called LHP zero. If $s = \omega_z$, then the zero is called RHP zero. The RHP zeros would have a profound effect on the control design, and would exist also in certain type of power electronic converters.

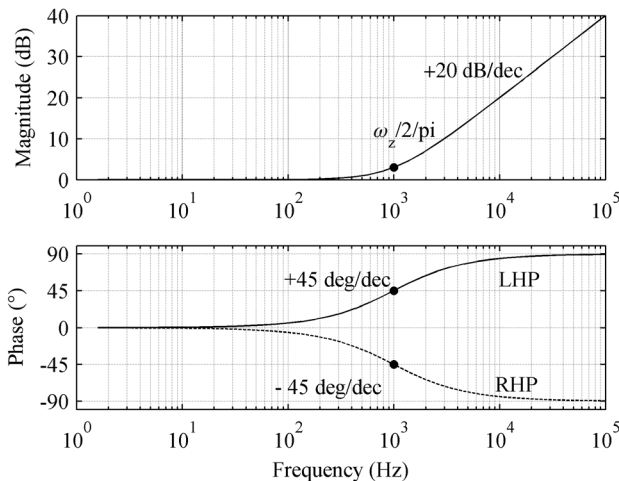


Figure 2.48 Behavior of single-zero transfer function in frequency domain.

Single Pole

Let us consider the single-pole transfer function of the form $G(s) = (1 + s/\omega_p)^{-1}$. Its magnitude (i.e., $|G(s)| = 1/\sqrt{1 + (\omega^2/\omega_p^2)}$) and phase (i.e., $\angle G(s) = -\arctan(\omega/\omega_p)$), may be given at certain interesting angular frequency points as follows:

$$\begin{aligned} \omega &= \frac{\omega_p}{10}, \\ |G(s)|_{\text{dB}} &= 20 \log_{10}(1/\sqrt{1.01}) = -0.04 \text{ dB}, \\ \angle G(s) &= -\arctan(0.1) = -5.7^\circ, \\ \omega &= \omega_p, \\ |G(s)|_{\text{dB}} &= 20 \log_{10}(1/\sqrt{2}) = -3 \text{ dB}, \\ \angle G(s) &= -\arctan(1) = -45^\circ, \\ \omega &= 10\omega_p, \\ |G(s)|_{\text{dB}} &= 20 \log_{10}(1/\sqrt{101}) \approx -20 \text{ dB}, \\ \angle G(s) &= -\arctan(10) = -84.3^\circ. \end{aligned}$$

As a consequence, the behavior of the single-zero transfer functions (cf. Figure 2.49) is typically considered to be such that its magnitude is unity (i.e., 0 dB) up to $\omega = \omega_p$, and starts decreasing at a slope of -20 dB/decade (i.e., -20 dB for a 10 times increase in frequency) from $\omega = \omega_p$. Its phase is zero up to $\omega = \omega_p/10$, and starts decreasing at a slope of -45° /decade up to $\omega = 10\omega_p$, and stays constant at -90° thereafter. The phase equals exactly -45° at $\omega = \omega_p$. This is the best point to locate exactly ω_p . If $G(s) = (1 - s/\omega_z)^{-1}$, the magnitude behavior is same but the phase has the positive sign compared to $G(s) = (1 + s/\omega_p)^{-1}$ (i.e., the slope is $+45^\circ$ /decade and it will finally stay at $+90^\circ$). If $s = -\omega_p$, then the zero is called LHP pole; if $s = \omega_p$, then the zero is called RHP pole. An RHP pole in the system means that it is unstable, and requires certain actions in control design to eliminate its effect.

Most important is to recognize that (i) the zeros and poles in the transfer functions are given as angular frequency and $\omega \approx 6.28f$, (ii) the phase starts

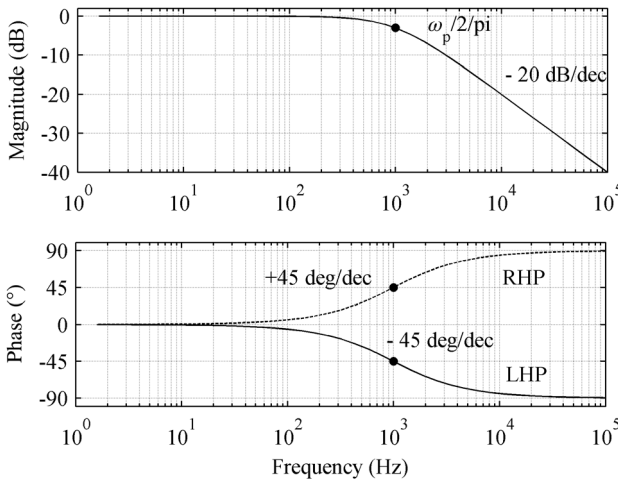


Figure 2.49 Behavior of single-pole transfer function in frequency domain.

affecting the system behavior already 10 times earlier than the location of the zero and pole, and (iii) keep on affecting up to 10 times higher frequencies than the location of the zero and pole. These facts are forgotten very often.

Second-Order Transfer Function

The second-order polynomial is typically expressed as $s^2 + s \cdot 2\zeta\omega_n + \omega_n^2$ or as $s^2 + s \cdot (\omega_n/Q) + \omega_n^2$, comprising either zeros or poles in the corresponding transfer function, where ζ is called *damping factor*, ω_n *undamped natural frequency*, and Q *quality factor*. Based on the coefficients of s , we can state that $Q = 1/2\zeta$. The second-order polynomials are common in power electronics, and shall be recognized because of their special influence on the control design as well as the source and load-impedance effects on the converter dynamic behavior.

The roots of the second-order polynomial can be expressed as $s_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$. The system characterized by it (i.e., $G(s)$ is of the form $\omega_n^2/s^2 + s \cdot 2\zeta\omega_n + \omega_n^2$) may be classified according to the value of the damping factor as (i) *underdamped*, when $0 < \zeta < 1$, (ii) *critically damped*, when $\zeta = 1$, (iii) *overdamped*, when $\zeta > 1$, (iv) *marginally stable or oscillatory*, when $\zeta = 0$, and (v) *unstable*, when $\zeta < 0$:

1) Underdamped Case: $0 < \zeta < 1$

The roots of the second-order polynomial are complex conjugates of each other, which can be expressed by $s_{1,2} = -\zeta\omega_n \pm j\omega_d$, where $\omega_d = \omega_n\sqrt{1 - \zeta^2}$ is called *damped natural frequency*. Step response of such a system applied to the reference input includes decaying oscillatory behavior, where the oscillation frequency is ω_d . The transfer function exhibits rapid change of magnitude and phase at ω_d (cf. Figures 2.50–2.52, $\zeta = 0.01$). The corresponding unit-step time-domain function can be given by

$$1 - \frac{\exp(-\zeta\omega_n t)}{\sqrt{1 - \zeta^2}} \sin\left(\omega_d t + \tan^{-1}\left(\frac{\sqrt{1 - \zeta^2}}{\zeta}\right)\right). \quad (2.124)$$

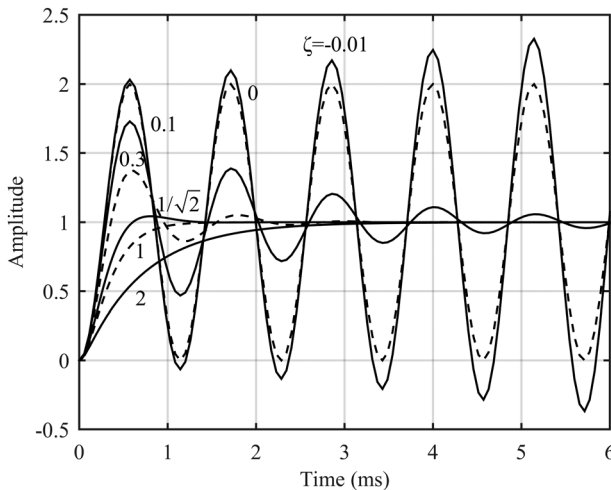


Figure 2.50 Unit-step response of a second-order system when the damping factor is varied.

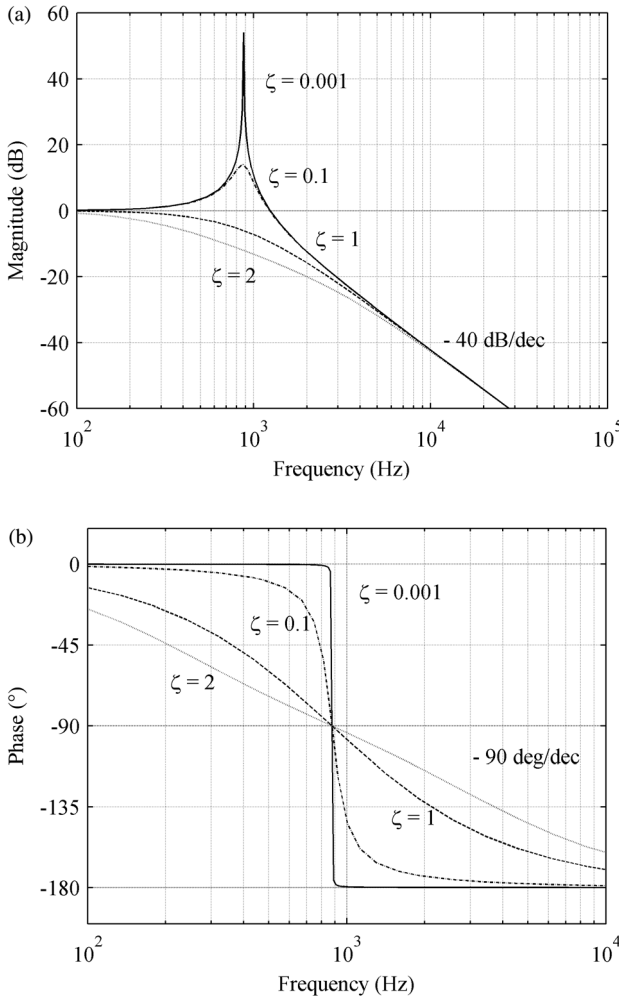


Figure 2.51 The magnitude (a) and phase (b) behavior of a second-order transfer function of the form $\omega_n^2/(s^2 + s \cdot 2\zeta\omega_n + \omega_n^2)$.

The maximum peak value of the second-order resonant system $\left(1/(2\zeta\sqrt{1-\zeta^2})\right)$ will take place at $\omega_{\text{res}} = \omega_n\sqrt{1-2\zeta^2}$, which means that the overshoot takes place only if $\zeta \leq 1/\sqrt{2}$. ω_{res} is known as the *resonant frequency*.

2) *Critically Damped Case:* $\zeta = 1$

The second-order polynomial has a real double root, which can be expressed by $s_{1,2} = -\zeta\omega_n$. The step response resembles an exponential response but is faster. The same applies also for the behavior of the transfer functions (cf. Figures 2.50–2.52; $\zeta = 1$). The corresponding unit-step time-domain function can be given by

$$1 - \exp(-\omega_n t)(1 + \omega_n t) \quad (2.125)$$

3) *Overdamped Case:* $\zeta > 1$

The second-order polynomial has two real roots, which can be expressed by $s_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$. The greater the damping factor, the more the roots

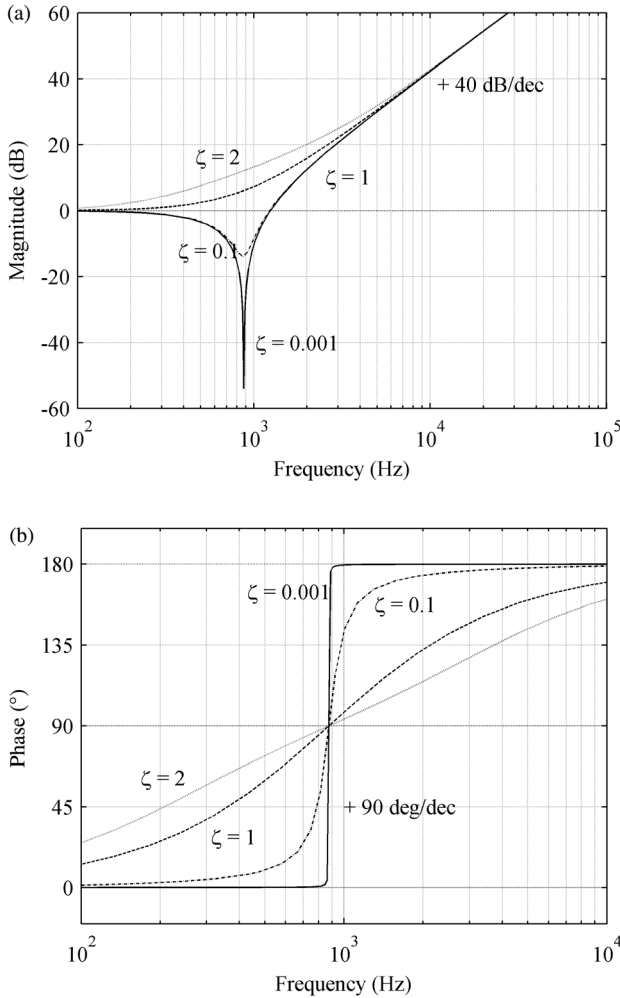


Figure 2.52 The magnitude (a) and phase (b) behavior of a second-order transfer function of the form $(s^2 + s \cdot 2\zeta\omega_n + \omega_n^2)/\omega_n^2$.

separated from each other. The step response contains only exponential behavior. The same applies also to the behavior of the transfer functions (cf. Figures 2.50–2.52: $\zeta = 2$). The corresponding unit-step time-domain function can be given by

$$1 + \frac{\exp\left(-\left(\zeta + \sqrt{\zeta^2 - 1}\right)\omega_n t\right)}{2\sqrt{\zeta^2 - 1}\left(\zeta + \sqrt{\zeta^2 - 1}\right)} - \frac{\exp\left(-\left(\zeta - \sqrt{\zeta^2 - 1}\right)\omega_n t\right)}{2\sqrt{\zeta^2 - 1}\left(\zeta - \sqrt{\zeta^2 - 1}\right)}. \quad (2.126)$$

4) Oscillatory Case: $\zeta = 0$

The second-order polynomial has two pure imaginary roots, which can be expressed by $s_{1,2} = \pm j\omega_n$. The system will oscillate at the undamped natural frequency ω_n (cf. Figure 2.50; $\zeta = 0$). The magnitude of the transfer function is

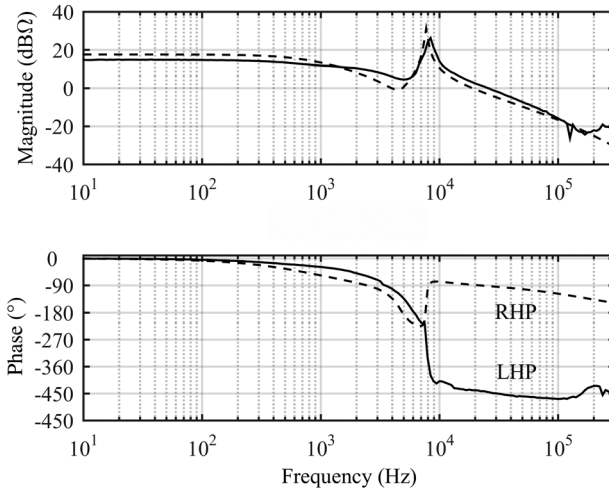


Figure 2.53 Control-to-output transfer function of a PCM-controlled superboost converter at stable (solid line, LHP) and unstable (dashed line, RHP) mode of operation.

infinitely high or low at ω_n , and its phase changes $\pm 180^\circ$ at ω_n . The corresponding unit-step time-domain function can be given by

$$1 - \cos \omega_n t. \quad (2.127)$$

5) *Unstable Case: $\zeta < 0$*

The second-order polynomial has roots in the RHP of the complex plane, which means that the transfer functions have positive real part and, therefore, the step response exhibits amplifying behavior in contrast to the decaying behavior in the stable system (cf. Figure 2.50; $\zeta = -0.01$). The behavior of transfer functions is such that the phase will be negative compared to the corresponding stable system. Figures 2.53 and 2.54 show such an open-loop

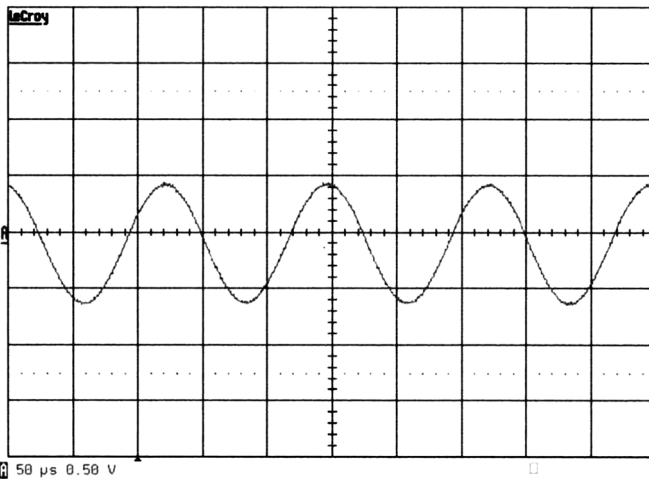


Figure 2.54 Output-voltage waveform due to the unstable pole.

behavior of a certain power electronic converter (i.e., PCM-controlled super-boost converter) reported in Ref. [52]. The corresponding unit-step time-domain function, when $|\zeta| < 1$, can be given by

$$1 - \frac{\exp(\zeta\omega_n t)}{\sqrt{1-\zeta^2}} \sin\left(\omega_d t + \tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right). \quad (2.128)$$

2.5.3 Stability

In general, the closed-loop output dynamics of a converter, when assuming the feedback taken from the output variable, can be given for a SISO-type power electronic converter (cf. Figure 2.6 and Eq. (2.5)) by

$$\hat{y}_{\text{out}} = \frac{G_{21-o}}{1+L_{\text{out}}}\hat{u}_{\text{in}} - \frac{G_{22-o}}{1+L_{\text{out}}}\hat{u}_{\text{out}} + \frac{L_{\text{out}}}{G_{\text{se-out}}(1+L_{\text{out}})}\hat{u}_{\text{c}} \quad (2.129)$$

and for a MIMO-type power electronic converter (cf. Figure 2.28 and Eq. (2.42)) by

$$\mathbf{Y}_{\text{out}} = [\mathbf{I} + \mathbf{L}_{\text{out}}]^{-1} \mathbf{G}_{21-o} \mathbf{U}_{\text{in}} - [\mathbf{I} + \mathbf{L}_{\text{out}}]^{-1} \mathbf{G}_{22-o} \mathbf{U}_{\text{out}} + \mathbf{G}_{\text{se-out}}^{-1} \mathbf{L}_{\text{out}} [\mathbf{I} + \mathbf{L}_{\text{out}}]^{-1} \mathbf{U}_{\text{c}}, \quad (2.130)$$

where L_{out} and \mathbf{L}_{out} denote the output-side feedback loop gains or as known in control engineering *return ratio* and *return-ratio matrix*, respectively, and $1 + L_{\text{out}}$ and $\det[\mathbf{I} + \mathbf{L}_{\text{out}}]$ are called the closed-loop system's characteristic polynomials. The inverse of the characteristic polynomial are called sensitivity function $S(\mathbf{S})$, and $L_{\text{out}}S$ or $\mathbf{L}_{\text{out}}\mathbf{S}$ the complementary sensitivity function $T(\mathbf{T})$. It is obvious that $S + T = 1$ and $\mathbf{S} + \mathbf{T} = \mathbf{I}$ [31,32,53,54]. Therefore, the output dynamics can be given by

$$\begin{aligned} \hat{y}_{\text{out}} &= S \cdot G_{21-o} \hat{u}_{\text{in}} - S \cdot G_{22-o} \hat{u}_{\text{out}} + \frac{1}{G_{\text{se-out}}} \cdot \mathbf{T} \cdot \hat{u}_{\text{c}}, \\ \mathbf{Y}_{\text{out}} &= \mathbf{S} \cdot \mathbf{G}_{21-o} \cdot \mathbf{U}_{\text{in}} - \mathbf{S} \cdot \mathbf{G}_{22-o} \cdot \mathbf{U}_{\text{out}} + \mathbf{G}_{\text{se-out}}^{-1} \cdot \mathbf{T} \cdot \mathbf{U}_{\text{c}}. \end{aligned} \quad (2.131)$$

In the SISO case, the system can be stated to be *unconditionally stable*, when all the roots of $1 + L$ lie in the open LHP of complex plane, where L denotes the loop gain in general context. In practice, this means that the power of the exponential function in Eq. (2.124) has to be less than zero. A system having roots at the imaginary axis (i.e., the power of the exponential function in Eq. (2.124) is zero) is considered to be *marginally stable* in control engineering, but in power electronics, a system with pure imaginary roots is deemed to be unstable. The system is *unstable*, when the roots of the characteristic polynomial lie in the RHP of the complex plane (i.e., the power of the exponential function is higher than zero) (cf. Eq. (2.128)).

In the MIMO case, the system can be stated to be *unconditionally stable*, when all the poles of $\det[\mathbf{I} + \mathbf{L}]$ lie in the open LHP of complex plane, where \mathbf{L} denotes the loop-gain matrix in general context. The definitions of marginally stable and unstable are the same as in the SISO case.

If an accurate analytical expression for the loop gain L is available, then the study of the location of the roots of the characteristic polynomial can be made either by solving the roots or applying *Routh-Hurwitz* test [52,53] to study the existence and number of RHP roots of a polynomial. If an RHP pole exists, it

means that the control bandwidth has to be designed to be higher than the location of the pole. The roots of the higher order (i.e., the order is higher than 2) cannot be solved easily in symbolic form to verify their locations in complex plane, but the *Routh–Hurwitz* method will then solve the problem. According to the method, the *Routh* array is to be constructed based on the coefficients of the polynomial ($P(s)$) under considerations

$$P(s) = a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \cdots a_1 s + a_0 \quad (2.132)$$

as follows:

$$\begin{array}{l} s^n : a_n \quad a_{n-2} \quad a_{n-4} \quad \cdots \quad 0 \\ s^{n-1} : a_{n-1} \quad a_{n-3} \quad a_{n-5} \quad \cdots \quad 0 \\ s^{n-2} : b_1 \quad b_2 \quad b_3 \quad \cdots \quad 0 \\ s^{n-3} : c_1 \quad c_2 \quad c_3 \quad \cdots \quad 0 \\ s^{n-4} : d_1 \quad d_2 \quad d_3 \quad \cdots \quad 0 \\ \vdots \\ s^0 : \quad \quad \quad \quad \quad \quad 0 \end{array} \quad (2.133)$$

where the first row (s^n) starts with the highest-order coefficient a_n , the second row (s^{n-1}) with the second-highest-order coefficient a_{n-1} , and the next elements within the rows are defined in Eq. (2.133), the elements of the third and subsequent rows follow the algorithm defined as follows:

$$\begin{aligned} b_1 &= \frac{-\begin{vmatrix} a_n & a_{n-2} \\ a_{n-1} & a_{n-3} \end{vmatrix}}{a_{n-1}} & b_2 &= \frac{-\begin{vmatrix} a_n & a_{n-4} \\ a_{n-1} & a_{n-5} \end{vmatrix}}{a_{n-1}} & b_3 &= \frac{-\begin{vmatrix} a_n & a_{n-6} \\ a_{n-1} & a_{n-7} \end{vmatrix}}{a_{n-1}} \\ c_1 &= \frac{-\begin{vmatrix} a_{n-1} & a_{n-3} \\ b_1 & b_2 \end{vmatrix}}{b_1} & c_2 &= \frac{-\begin{vmatrix} a_{n-1} & a_{n-5} \\ b_1 & b_3 \end{vmatrix}}{b_1} & c_3 &= \frac{-\begin{vmatrix} a_{n-1} & a_{n-7} \\ b_1 & b_4 \end{vmatrix}}{b_1} \\ d_1 &= \frac{-\begin{vmatrix} b_1 & b_2 \\ c_1 & c_2 \end{vmatrix}}{c_1} & d_2 &= \frac{-\begin{vmatrix} b_1 & b_3 \\ c_1 & c_3 \end{vmatrix}}{c_1} & d_3 &= \frac{-\begin{vmatrix} b_1 & b_4 \\ c_1 & c_4 \end{vmatrix}}{c_1} \end{aligned} \quad (2.134)$$

The number of RHP roots of $P(s)$ is the number of algebraic sign changes in the elements of the left column of the array in Eq. (2.133) proceeding from the top to the bottom. The first- or second-order polynomial has all roots in LHP if and only if all the coefficients have the same algebraic sign. In the case of higher order polynomial, the same does not guarantee the absence of RHP roots but the *Routh–Hurwitz* test has to be applied to confirm the situation. The sign changes in the polynomial coefficients indicate, however, the existence of at least one RHP root. The missing of one or several coefficients means that the polynomial has either complex imaginary axis or RHP roots or both. The existence of imaginary axis roots is reflected as an all-zero row in the Routh array. The location of the roots can be studied by computing the roots of the directly previous existing row

known as auxiliary polynomial. The repeating of the roots can be studied by differentiating the auxiliary polynomial and computing its roots. If repeating roots exist, then the system is unstable. The existence of the imaginary axis roots means anyway that the system is marginally stable, which is not allowed in power electronics.

The *Routh–Hurwitz* test can be equally applied to verify the existence of RHP zeros in the control dynamics (i.e., the loop gain). The existence of the RHP zeros requires to design the control bandwidth less than the location of the RHP zero for stability to exist.

In practice, the frequency responses of the loop gain L or the loop gain matrix \mathbf{L} may be only available, from which the poles and zeros cannot be reliably extracted. Therefore, other methods based directly on the loop frequency responses have to be applied. The usual visualization methods of the loop frequency behavior are polar and *Bode* plots. The polar plot (Figure 2.55a, solid

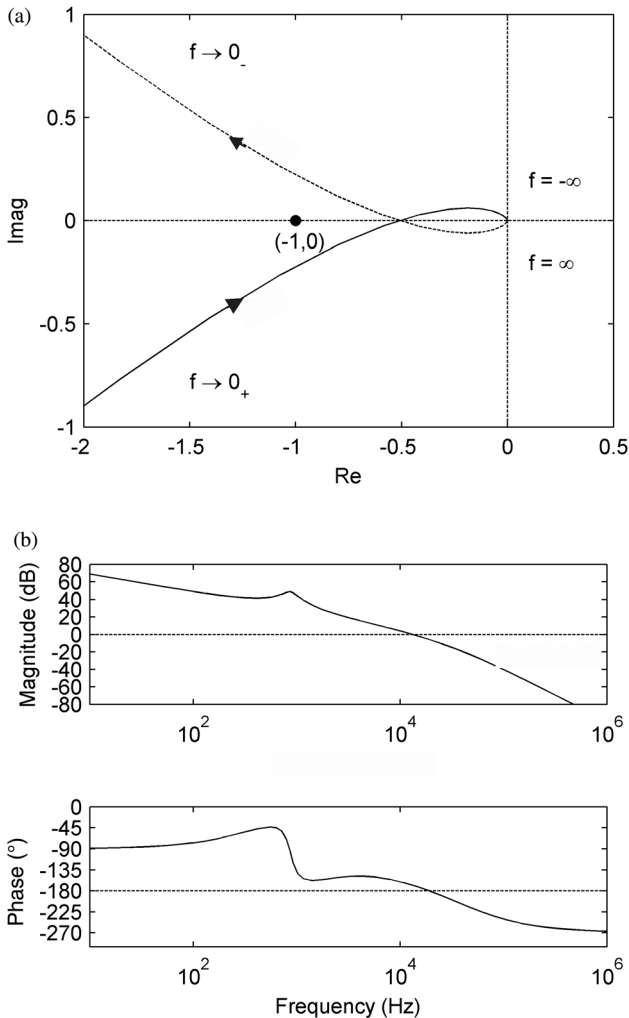


Figure 2.55 Frequency-response visualization methods. (a) Polar plot. (b) Bode plot.

line) is constructed by plotting the locus of the magnitude of the loop gain in the complex plane with the x -axis containing the real part of the loop gain and the y -axis containing the imaginary part. Usually the locus tends to zero when the frequency approaches infinity. The frequency is not explicitly shown in the polar plot, but only the direction of the increasing frequency. In order to study the stability of a SISO system, the plot is constructed for both the positive (Figure 2.55a, solid line) and negative (Figure 2.55a, dashed line) frequencies. In practice, this means that the imaginary part is as it is in the original loop gain, and its sign is changed negative for the negative frequencies producing a mirror effect with respect to x -axis. The *Bode* plot (Figure 2.55b) is constructed by plotting the magnitude in decibels and the phase in degrees usually in the separate subplots with respect to frequency, where x -axis is the frequency in logarithmic scale and y -axis is the magnitude and phase in linear scale. The polar and *Bode* plots in Figure 2.54 are drawn for the same loop gain, but the polar plot shows only the frequencies higher than 10 kHz when the *Bode* plot shows much higher frequency range.

In SIMO case, the stability of the closed-loop system can be studied by applying the *Nyquist* stability criterion [52,53] to the loop gain L by means of a polar plot constructed for the positive and negative frequencies, as shown in Figure 2.55a. Such a plot is called *Nyquist* plot. If the open-loop system contains N RHP poles, the system is stable and if and only if the locus of the loop gain encircles anticlockwise the points $(-1,0)$ N times, it does not pass through the point $(-1,0)$ or encircle it in clockwise direction when both of the loci are considered. In practice, the situation can be more complicated, as discussed in Ref. [53] (cf. pp. 521–542).

Consider the following loop gain L and characteristic polynomial $1 + L$ of the forms:

$$\begin{aligned} L &= \frac{K}{s(s^2 \times 10^{-5} + s \times 10^{-3} + 1)}, \\ 1 + L &= \frac{s(s^2 \times 10^{-5} + s \times 10^{-3} + 1) + K}{s(s^2 \times 10^{-5} + s \times 10^{-3} + 1)}, \end{aligned} \quad (2.135)$$

where K is a constant. According to Figure 2.56a, the closed-loop system having the loop gain according to (2.131) will become unstable for high-enough values of K because of either passing through the point $(-1,0)$ or encircling it in the clockwise direction. Figure 2.56b shows the same situation as a *Bode* plot as in Figure 2.56a. The numerator polynomial in Eq. (2.136) of the characteristic equation $(1 + L)$ in Eq. (2.135) contains the system poles as its roots:

$$s^3 \times 10^{-5} + s^2 \times 10^{-3} + s + K \quad (2.136)$$

The existence of the RHP poles can be studied constructing the *Routh* array as follows:

$$\begin{array}{l} s^3 : 10^{-5} \quad 1 \quad 0 \\ s^2 : 10^{-3} \quad K \quad 0 \\ s : 1 - 10^{-2}K \quad 0 \quad 0 \\ s^0 : K \quad 0 \quad 0 \end{array}$$

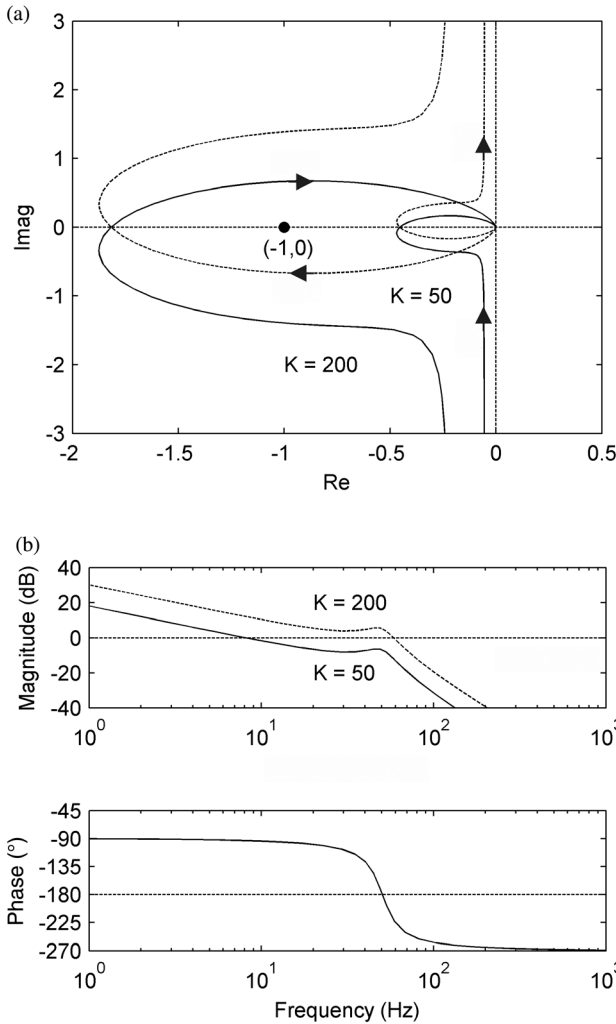


Figure 2.56 Stable ($K = 50$) and unstable ($K = 200$) systems. (a) Nyquist plot. (b) Bode plot.

According to the elements of the left column of the *Routh* array, the RHP poles appear when $1 - 10^{-2}K < 0$ or $K > 100$. This means actually that the loop gain will pass through the point $(-1,0)$ when K equals 100. According to the *Routh* array row s , the row will contain all zeros, when K equals 100. The polynomial in Eq. (2.136) can be developed to be $(s + 10^2)(s^2 10^{-5} + 1)$, which indicates that the complex conjugate roots equal $\pm j10^5$ and thus lie on imaginary axis as discussed earlier.

Closed-loop system may also be *conditionally stable*. The *Nyquist* plot illustrating such as loop gain behavior is shown in Figure 2.57, where the encirclement of the point $(-1,0)$ is anticlockwise indicating stability. The system may, however, become unstable when the gain is slightly increased or decreased. Such a situation may take place, for instance, when the converter starts up due to the reduction of gain in the associated control circuitry.

Figure 2.58a shows bode plots of a closed-loop system containing RHP pole in its open-loop system, where the solid line denotes a stable system (i.e., the

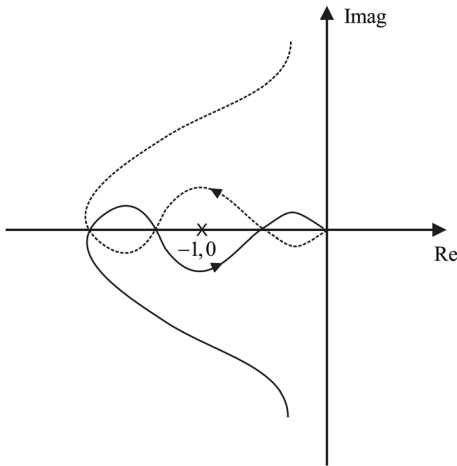


Figure 2.57 Conditionally stable system.

feedback-loop crossover frequency is higher than the RHP pole frequency), and the dashed line denotes an unstable system (i.e., the feedback-loop crossover frequency is lower than the RHP pole frequency). As discussed earlier, the Nyquist plot (solid line) has to encircle the critical point $(-1,0)$ anticlockwise as shown in Figure 2.58b for the system to be stable. Figure 2.58c shows that the Nyquist plot (dashed line) does not encircle the critical point and, therefore, the system is unstable.

In MIMO case, the stability of the closed-loop system can be studied by applying the *Nyquist* stability criterion [31,32] to $\det[\mathbf{I} + \mathbf{L}]$ by means of a polar plot constructed for the positive and negative frequencies similarly, as shown in Figure 2.55a. If the open-loop system contains N RHP poles, then the system is stable if the locus of $\det[\mathbf{I} + \mathbf{L}]$ encircles anticlockwise the origin N times, does not pass through the origin, or encircle it in clockwise direction when both of the loci are considered. In practice, the situation can be more complicated, as discussed in Ref. [31] (cf. pp. 37–74).

The robustness of stability is typically related to phase (PM) and gain (GM) margins, and the dynamic transient performance is related to the control bandwidth. The closed-loop systems usually employ negative feedback, which is also taken into account when constructing the characteristic polynomials (i.e., $1 + L$): If the loop gain is physically measured, the overall phase change for unstable operation is 360° , which is also the typical reading (i.e., 0°) in the frequency response analyzers. For complying with the control engineering domain, 180° is subtracted from the reading or data produced by the analyzers. According to this, the PM (Figure 2.59a) is defined by

$$\text{PM} = \angle L + 180^\circ \quad (2.137)$$

at the frequency where $|L| = 1$ (i.e., the loop-gain crossover frequency ω_{gco} or f_{gco}). Similarly, the GM (Figure 2.59a) is defined by

$$\text{GM} = \frac{1}{|L|} \quad (2.138)$$

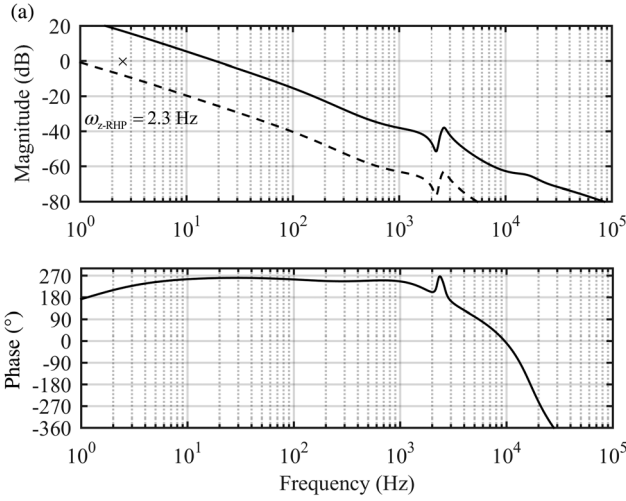
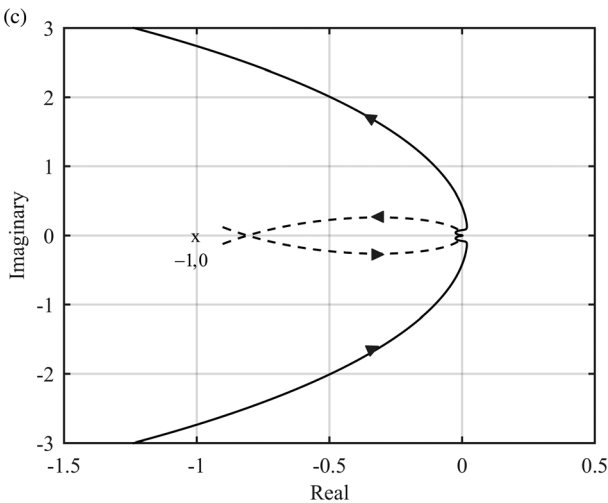
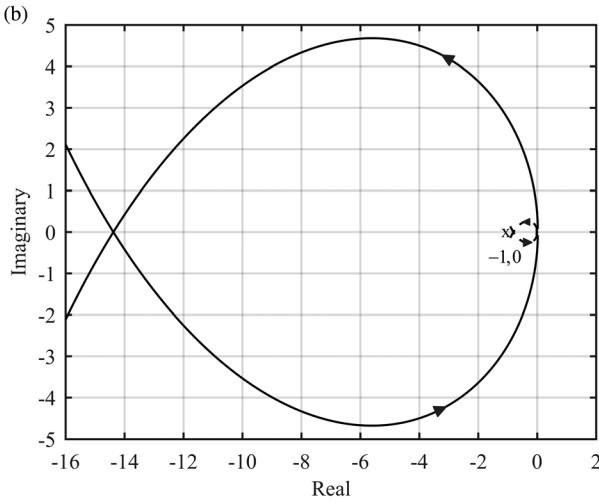


Figure 2.58 System containing RHP pole at open loop. (a) Bode plot. (b) Nyquist plot. (c) Extended Nyquist plot (solid line denotes stable closed-loop system, and dashed line denotes unstable closed-loop system).



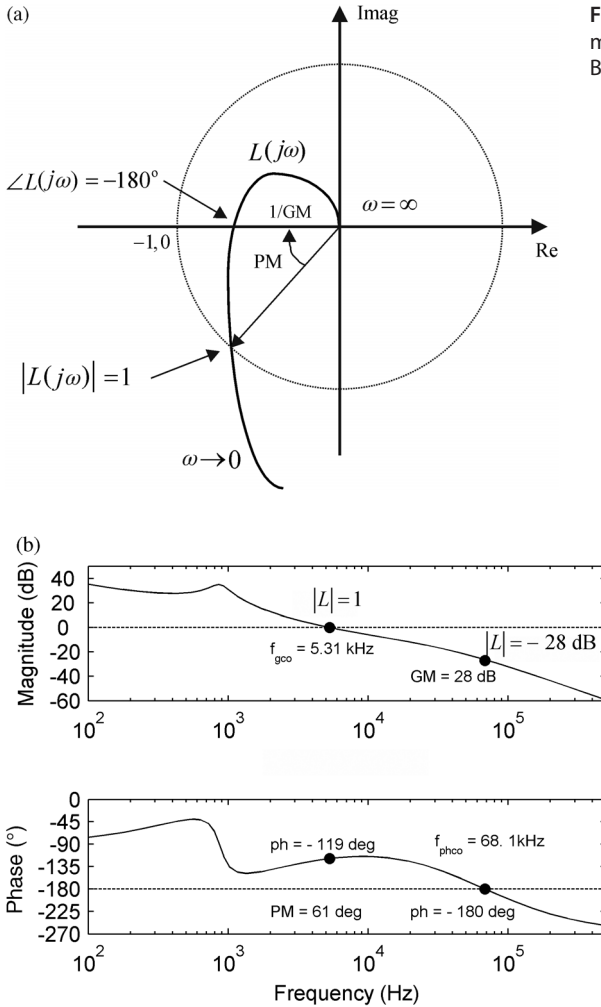


Figure 2.59 Phase and gain margins. (a) Nyquist plot. (b) Bode plot.

at the frequency where $\angle L = -180^\circ$ (i.e., the phase crossover frequency ω_{phco} or f_{phco}). Figure 2.59b shows the same definitions using the *Bode* plot.

In power electronics, the loop crossover frequency (f_{gco}) (Figure 2.60) is typically called control bandwidth. In control engineering, the control bandwidth is defined as the frequency range from zero to the frequency where the sensitivity function (S) equals -3 dB (i.e., $|S| = 1/\sqrt{2}$) (cf. Figure 2.60). The loop crossover frequency is naturally higher than the theoretical control bandwidth (i.e., Figure 2.59: $f_{\text{gco}} = 2.36$ kHz and $f_{s-3\text{dB}} = 1.79$ kHz). The amount of the difference is dependent on the gain behavior of the loop in the vicinity of its crossover frequency. If the gain is small, then the theoretical control bandwidth can be much shorter than the loop crossover frequency.

The effect of the PM and GM on the converter dynamic behavior does not only come from the robustness of stability but also via their effect on the transient behavior of the converters: Eq. (2.139) shows a typical formulation for the output

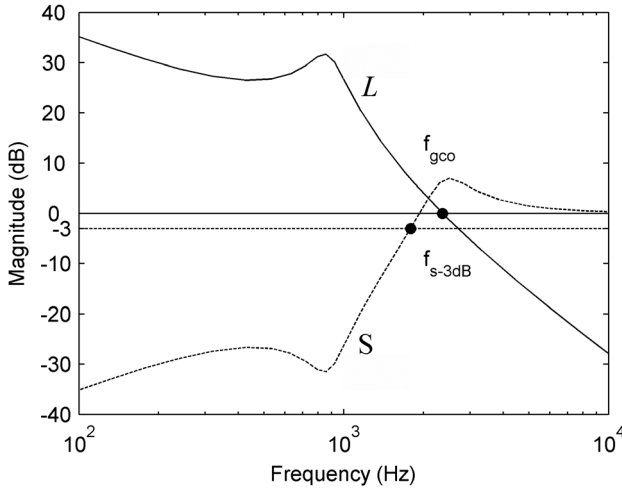


Figure 2.60 Control bandwidth ($f_{s-3\text{ dB}}$) versus loop crossover frequency (f_{gco}).

dynamics of a converter where the sensitivity functions (S) and complementary sensitivity function (T) are visible. The low margins can cause peaking in S (cf. Figure 2.61), which is reflected as an increase of the closed-loop transfer function influencing the transient response (i.e., increased undershoot or overshoot). The peaking is also clearly visible in Figure 2.60.

$$\hat{y}_{\text{out}} = S \cdot G_{21-0} \hat{u}_{\text{in}} - S \cdot G_{22-0} \hat{u}_{\text{out}} + \frac{1}{G_{\text{se-out}}} \cdot T \cdot \hat{u}_{\text{c}}. \quad (2.139)$$

The magnitude of the sensitivity function can be given at the loop crossover frequency by $|S|_{|L|=1} = 1/\sqrt{2(1 - \cos(\text{PM}))} = 1/2\sin(\text{PM}/2)$ and at the phase crossover frequency by $|S|_{\angle L=-180^\circ} = |\text{GM}/(\text{GM} - 1)|$. Therefore, it can be observed that the peaking takes place if $\text{PM} < 60^\circ$ (cf. Figure 2.58a) or $\text{GM} < 18\text{ dB}$. The typically used gain margin of 6 dB would actually cause peaking of 6 dB (i.e., doubling the value). As a consequence, the loop gain-related margins should be maintained adequate for preventing the excess peaking and deterioration of transient performance.

The impedance-based stability assessment (cf. Sections 2.25 and 2.3.6) is commonly applied in assessing the stability and transient performance in interconnected DC and AC power electronic systems [54–62]. The concept of forbidden region was launched in Ref. [56] (cf. Figure 2.62), which ensures robust stability of the system when the minor loop gain (i.e., an impedance ratio, where the numerator impedance is the internal impedance of the voltage-type source and the denominator impedance the internal impedance of the current-type source [54]) stays out of the forbidden region. The concept of minor loop was originally launched in Ref. [2,3] by Middlebrook. The corresponding forbidden region is a circle having radius of inverse of gain margin (GM) and the center at origin as shown in Figure 2.61. Middlebrook's forbidden region was deemed to be too large, that is, to occupy unnecessary large amount of area in the complex plane [56]. As a consequence, new forbidden regions have been developed for

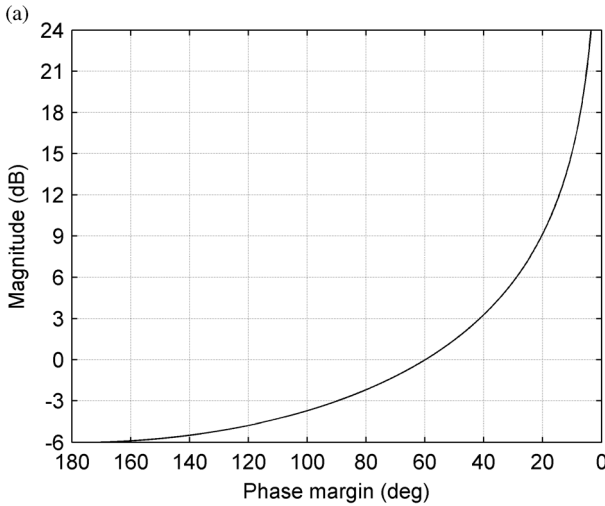
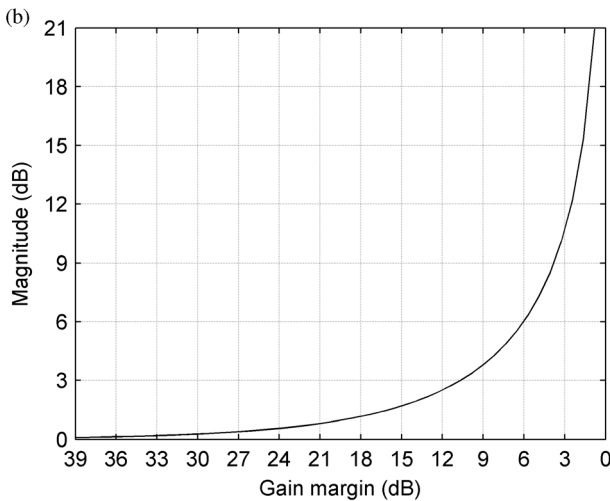


Figure 2.61 The peak value of the sensitivity function (a) at the feedback-loop gain crossover frequency (f_{gco}) and (b) at the phase crossover frequency (f_{phco}).



reducing the occupied area such as ESAC (Energy Systems Analysis Consortium) [56], GMPM (gain margin phase margin) [57], and opposing argument [58] criteria, as illustrated in Figure 2.62.

It may be obvious that all the forbidden regions aim at maintaining robust stability (i.e., acceptable transient performance) by requiring the minor loop gain to satisfy certain PM and GM conditions. Basically, the forbidden region criteria apply also for the conventional loop gain. A new forbidden region has been proposed in Ref. [54] by means of a circle having radius of the inverse of the allowed maximum peaking in the affected transfer functions and the center at the point $(-1,0)$, as depicted in Figure 2.63.

The MPC forbidden region in Figure 2.63 can be derived as follows based on Figure 2.64: The distance between the loop gain $L(j\omega)$ and the point $(-1,0)$ can be always given as $-1 - L(j\omega)$ according to Figure 2.64. By denoting $|S_{\max}| = M_S$ and

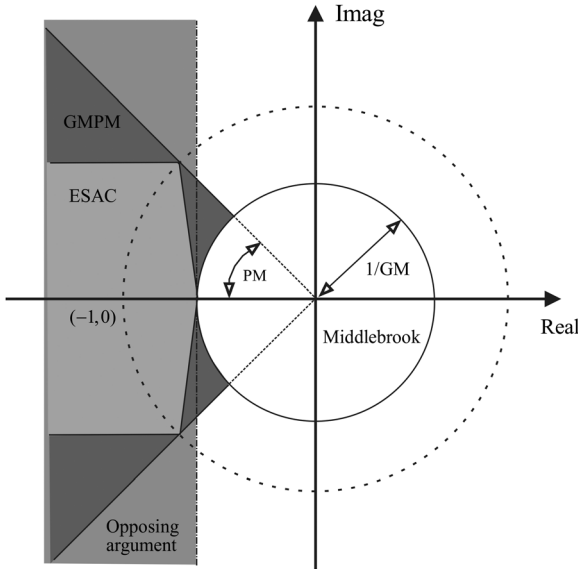


Figure 2.62 Collection of forbidden regions in the complex plane. *Source:* Vesti 2013. Reproduced with permission of IEEE.

$L(j\omega) = \alpha + j\beta$, then $(1 + \alpha)^2 + \beta^2 = 1/M_S^2$ forms a circle in the complex plane having the center at $(-1, 0)$ and the radius of $1/M_S$. This criterion also takes into account the combined effects of both the margins regardless of the frequency of occurrence. It is clear that the selection of the allowed peaking determines the area of the forbidden region. In Figure 2.63, the MPC-based forbidden region (gray area) is drawn assuming that $M_S = 2$, which corresponds to $PM \approx 29.0^\circ$ and $GM = 6$ dB.

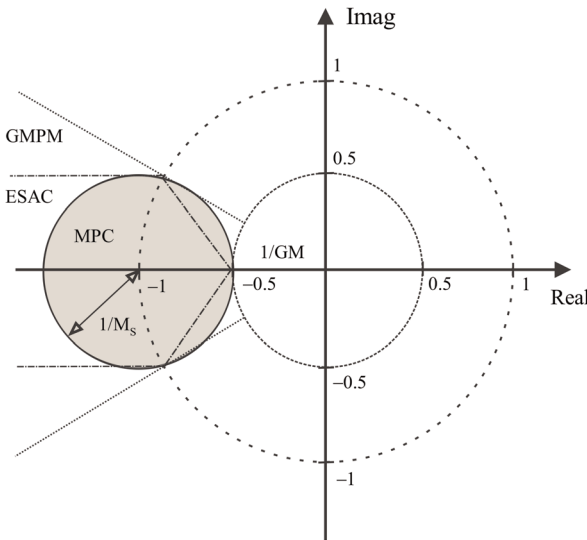


Figure 2.63 Maximum peak criteria (MPC)-based forbidden region versus ESAC and GMPM regions. *Source:* Vesti 2013. Reproduced with permission of IEEE.

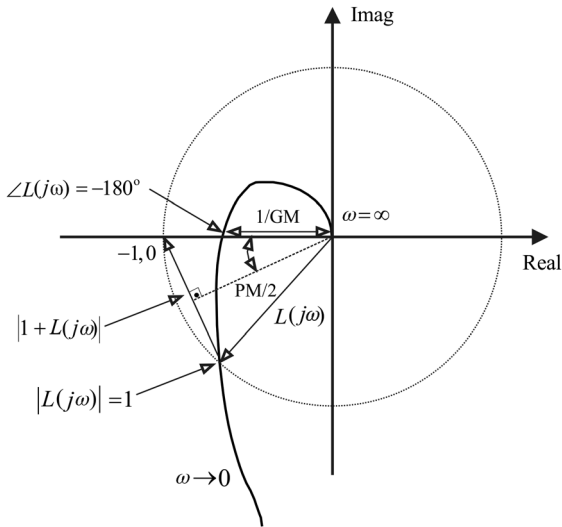


Figure 2.64 Loop gain robustness indices. *Source:* Vesti 2013. Reproduced with permission of IEEE.

For robust stability to exist, the minor loop gain shall stay out of the defined MPC-based forbidden region and shall also satisfy the *Nyquist* stability criterion in terms of encirclements around the point $(-1,0)$. The state of stability extractable from the behavior of the minor loop gain is invariant to the interface at which the minor loop gain is determined as discussed, for example, in Ref. [56]. The state of the robustness of stability depends, however, on the interface at which the minor loop gain is determined because of the hiding effects of the passive components such as capacitors and LC filters between the direct interface of the converter power stage and the applied interface. As a consequence, the robustness can be reliably determined only at the direct interface of a regulated converter as in assessing the effect of the input filter in Refs [2,3]. When the MPC forbidden region is applied to the conventional loop gain, the robustness information is always perfect.

The above discussions related to the feedback control loops are also equally valid for the impedance-based minor loops introduced first time in the 1970s in Refs [2,3].

2.5.4 Transient Performance

The transient performance is usually addressed to the load-transient behavior of the output terminal voltage of a power electronic converter [63,54], but can equally cover also the transient behavior of the other output variables such as input current and voltage as well as the output current. There are always several factors that can affect the behavior of the output variable in question. In control engineering, the transient behavior is usually addressed to the behavior of the controlled variable when a step change in its reference signal is excited [53]. In this case, the transient behavior reflects the properties of the feedback loop purely,

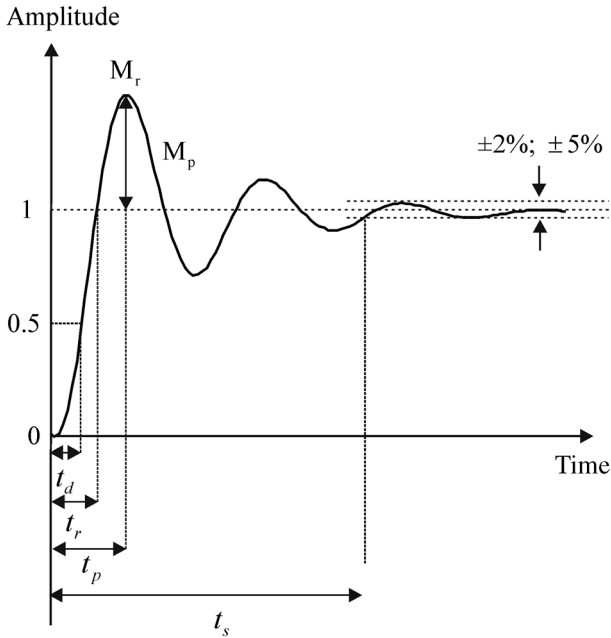


Figure 2.65 Typical parameters specifying the transient response in the control engineering textbooks.

because (cf. Figure 2.6 and Eq. (2.5))

$$\hat{y} = \frac{1}{G_{se}} \cdot \frac{L}{1+L} \cdot \hat{u}_r. \quad (2.140)$$

Consequently, the typical transient behavior indices are given for a second-order system by (cf. Figure 2.65)

$$\begin{aligned} t_r &= \frac{1}{\omega_d} \cdot \arctan\left(-\frac{\omega_d}{\zeta\omega_n}\right), \\ t_p &= \frac{\pi}{\omega_d}, \\ t_s &= \frac{4}{\zeta\omega_d} (\pm 2.5\%); \frac{3}{\zeta\omega_d} (\pm 5\%), \\ M_p &= e^{-(\zeta/\sqrt{1-\zeta^2})\pi} \times 100\%, \\ M_r &= \frac{1}{2\zeta\sqrt{1-\zeta^2}}, \\ PM &= \tan^{-1}\left(\frac{2\zeta}{\sqrt{\sqrt{1+4\zeta^4}-2\zeta^2}}\right), \end{aligned} \quad (2.141)$$

where t_r denotes rise time, t_p time to peak, t_s settling time, M_p maximum overshoot, M_r maximum peak value, and PM the phase margin of the feedback-loop gain. The other variables (ω_n , ω_d , ζ) are as defined in Section 2.5.2. The

relation between the PM and the closed-loop system ζ (i.e., Eq. (2.140)) can be estimated to be $\zeta \approx \text{PM}(\text{deg})/100$ up to PM of 50° . PM of 65° corresponds to the optimal damping factor of $1/\sqrt{2}$ (cf. the last equation in Eq. (2.141)).

In case of the other transients, there are always other elements too, which can have an effect on the transient behavior as follows (cf. Figure 2.6 and Eq. (2.5)):

$$\begin{aligned}\hat{y} &= \frac{G_{xy-o}}{1+L} \cdot \hat{u}, \\ \hat{y} &= \frac{G_{xy-o} + L \cdot G_{xy-\infty}}{1+L} \cdot \hat{u},\end{aligned}\quad (2.142)$$

where G_{xy-o} is a certain open-loop transfer function related to the considered output variable, and $G_{xy-\infty}$ is the corresponding ideal transfer function. As already stated, the most important transient response is usually the load-current transient response. It can be given in *Laplace* domain by (cf. Section 2.2.3: Figure 2.6, and Eq. (2.5))

$$\begin{aligned}\Delta\hat{v}_o &= \frac{Z_{o-o}}{1+L_{\text{out}}} \cdot \Delta\hat{i}_o, \\ L_{\text{out}} &= G_{\text{se-out}}G_aG_{\text{cc-out}}G_{\text{co-o}},\end{aligned}\quad (2.143)$$

where Z_{o-o} denotes the open-loop output impedance of a voltage-fed converter, L_{out} the output-voltage feedback-loop gain, $\Delta\hat{i}_o$ the injected load-current transient, and $\Delta\hat{v}_o$ the response at the output voltage. The ideas presented below concerning the output-voltage transient behavior would be valid also for the other transient when properly adjusted for the transient in question. The example buck converter used for producing subsequent figures is introduced in Figure 2.66. The applied load-current change is from 1 to 2.5 A. The modulator gain ($1/V_M$) (i.e., the inverse of the peak-to-peak voltage of the modulator ramp) is varied from 1 to $1/3 \text{ V}^{-1}$. The resulting output-voltage and inductor-current transient behaviors are shown in Figure 2.67.

The maximum dip of the output voltage (cf. Figure 2.67), when the load current is changed stepwise, can be computed based on the value of the output impedance (cf. Figure 2.68) at crossover frequency of the output-voltage feedback loop (cf. Figure 2.69) and the step change in the output current (i.e., the product) as the corresponding figures clearly indicate.

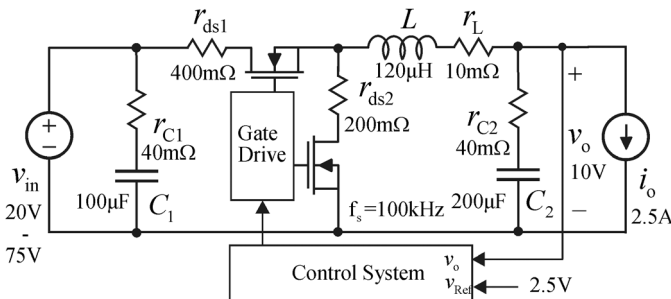


Figure 2.66 An example buck converter.

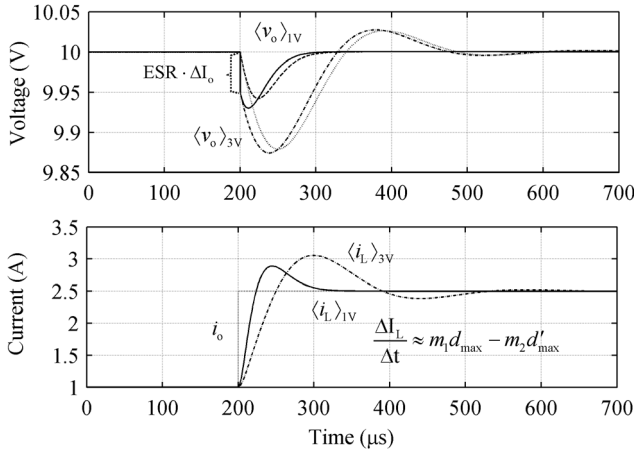


Figure 2.67 Output-voltage transient responses to a step change from 1 to 2.5 A in output current when the modulator gain ($1/V_M$) is varied.

It is stated in Ref. [63] that the location of the zeros of the output-voltage feedback controller determines the settling time because they form the poles of the transient function. At the low frequencies, the output-voltage loop gain is usually high, and therefore, the load transient response in Eq. (2.143) can be given by

$$\Delta v_o(s) \approx \frac{Z_{o-o-num}}{G_{se-out} G_a G_{cc-out} G_{co-o-num}} \cdot \frac{\Delta I_o}{s}, \quad (2.144)$$

which indicates that the zeros of G_{cc-out} forms the poles of $\Delta \hat{v}_o$ response and, consequently, the time constants of the related exponential functions and the settling behavior. Therefore, the higher the frequencies the zeros are placed, the faster the settling process. This is a very good explanation but does not exactly tell

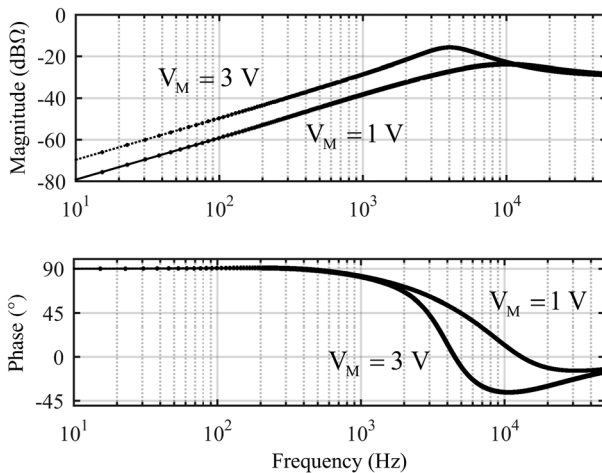


Figure 2.68 Closed-loop output impedances when the modulator gain ($1/V_M$) is varied.

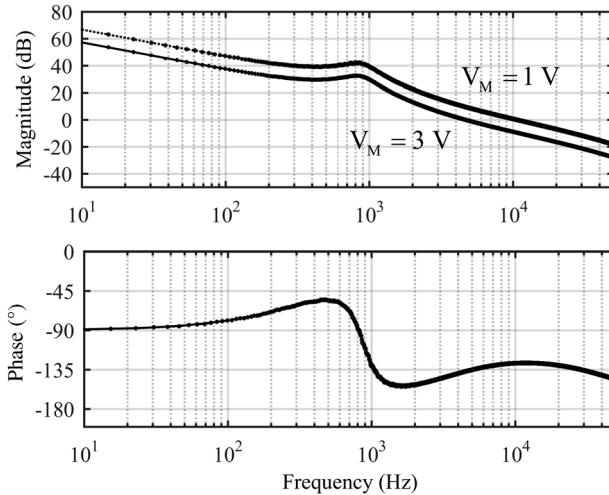


Figure 2.69 Output-voltage feedback-loop gains when the modulator gain ($1/V_M$) is varied.

the physical reason behind the improvement: The settling process is actually very much dependent on the behavior of the duty ratio when the output voltage approaches its final set value. In this respect, the low-frequency controller gain is decisive, because the controller error signal will decrease all the time when the voltage set value is coming closer. If the low-frequency gain is small, then the duty ratio will also stay close to its steady-state value and the settling process is slow, as shown in Figure 2.70 (cf. Figure 2.68). In practice, the location of the controller zeros affects the low-frequency gain of the feedback controller and, consequently, the settling time similarly as the change of the modulator gain in this example. Therefore, all the controller design methods increasing the low-frequency gain would improve the settling time [64]. The output-current feedforward, reported

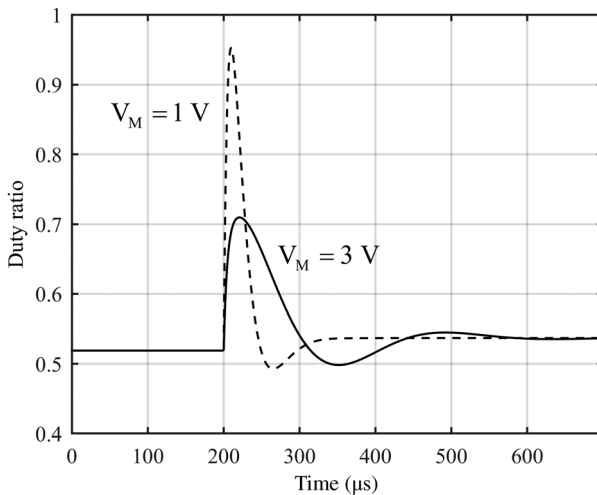


Figure 2.70 Behavior of averaged duty ratio when the modulator gain ($1/V_M$) is varied.

in Ref. [65], produces highly improved load transient behavior by changing quickly the duty ratio directly without affecting the feedback controller.

2.5.5 Feedback-Loop Design Constraints

An optimum feedback-loop design according to Ref. [66] is the one with highest gain below the loop crossover frequency and lowest gain above the crossover frequency. According to Ref. [67], the optimal controller would be quickly responsive to substantial changes in output voltage and also provide precise steady-state control. The first definition of the optimum design [66] is actually in line with the requirements of robust stability and fast transient response even if the external interactions were quite unknown during the writing of Ref. [66]: The optimum design might be expressed, as illustrated in Figure 2.71, where the loop gain is as high as possible up to the loop crossover frequency, and as small as possible after loop crossover frequency with constant phase margin of 60° for all the frequencies.

The reasoning behind the optimality is the fact that such a converter would be highly invariant to impedance-based load interactions and would have fast transient response: The high-loop gain means that the closed-loop output impedance of the converter is extremely small up to the feedback loop crossover frequency, which means that the load impedance would not easily affect the internal dynamics of the converter [13–15], and the transient settling time is very short, as discussed in

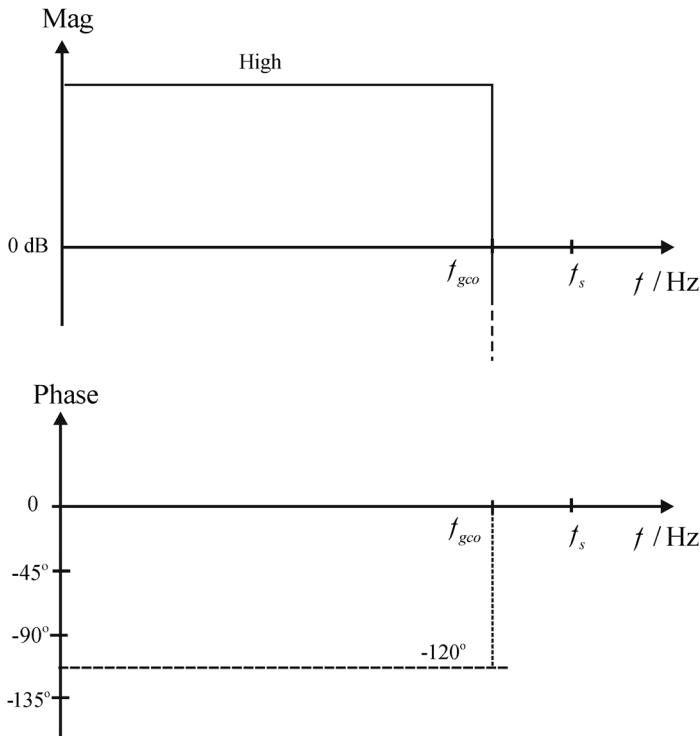


Figure 2.71 Theoretically optimal loop shape.

Section 2.5.4. In practice, the load transient is dictated by the properties of the output capacitor and the other parasitic elements at the output of the converter and along the current-carrying path between the converter and the load. The load impedance does not affect the converter input impedance due to the extremely high input-to-output attenuation provided by the input-to-output transfer function [15]. Therefore, the stability of the converter due to the source interactions would be determined by the ideal input impedance in such a way that no impedance overlap is tolerated at the direct input of the converter [15].

In reality, such a feedback-loop behavior cannot be accomplished due to the practical constraints involved in the components such as operational amplifiers, and A/D converters as well as duty-ratio generation.

RHP Zeros and Poles

The existence of RHP zeros and poles in power electronics converters is quite common [5,17,47,48,51]. A converter having an RHP pole in its control dynamics is known to exhibit a non-minimum phase behavior. The existence of the RHP zero means that the maximum control bandwidth has to be limited to the frequency of the RHP zero and in practice below it [68]. A typical recommended design margin is half the frequency of the zero. The location of the RHP zero can be dependent on the conduction mode of the converter, which shall be carefully considered [5].

Sometimes, the open-loop converter may even contain unstable pole that is caused by the power stage itself [51] or, for example, the applied cascaded control scheme [17]. This means that the minimum control bandwidth has to be designed higher than the frequency of the RHP pole [68]. A typical recommended design margin is twice the frequency of the RHP pole. The location of the RHP pole can be highly dependent on the operation point variables and some circuit elements in power stage, which shall be carefully considered [17].

The destabilizing effect of improper control design, when RHP zeros and poles exist in the control dynamics (G_{co-o}) of the converter, can be illustrated by means of the closed-loop output impedance (Z_{o-c}) given in Eq. (2.145) based on the fact that the system is unstable if RHP poles appear as follows:

$$Z_{o-c} = \frac{Z_{o-o}}{1 + L_{out}}, \quad (2.145)$$

$$L_{out} = G_{se-out} G_a G_{cc-out} G_{co-o}.$$

Let us assume that an RHP zero exist in G_{co-o} and the control bandwidth is designed to be higher than the frequency of the zero. Thus, Z_{o-c} in the vicinity of f_{RHP-z} can be given by

$$f_{|L_{out}|=1} > f_{RHP-z} \rightarrow Z_{o-c} \approx \frac{\text{Num}(Z_{o-o})}{G_{se-out} G_a G_{cc-out} \text{Num}(G_{co-o})}. \quad (2.146)$$

According to Eq. (2.146), the system is unstable, because the RHP zero of G_{co-o} has turned to an RHP pole of the system. If the control bandwidth is designed to be less than the zero, then Z_{o-c} can be given by

$$f_{|L_{out}|=1} < f_{RHP-z} \rightarrow Z_{o-c} \approx Z_{o-o}. \quad (2.147)$$

According to Eq. (2.147), the system is stable if the open-loop system is stable.

Let us assume that an RHP pole exists in the open-loop system and the control bandwidth has been designed to be less than the frequency of the pole. Thus, Z_{o-c} in the vicinity of $f_{\text{RHP-pole}}$ can be given by

$$f_{|L_{\text{out}}|=1} < f_{\text{RHP-p}} \rightarrow Z_{o-c} \approx Z_{o-o}. \quad (2.148)$$

According to Eq. (2.148), the system is unstable because the open-loop system is unstable. If the control bandwidth is designed to be higher than the zero, then Z_{o-c} can be given in the vicinity of $f_{\text{RHP-pole}}$ by

$$f_{|L_{\text{out}}|=1} > f_{\text{RHP-pole}} \rightarrow Z_{o-c} \approx \frac{\text{Num}(Z_{o-o})}{G_{\text{se-out}} G_a G_{\text{cc-out}} \text{Num}(G_{\text{co-o}})}. \quad (2.149)$$

According to Eq. (2.149), the system is stable because the RHP pole has disappeared.

Minimum and Maximum Feedback-Loop Crossover Frequencies

In practice, the usable feedback-loop crossover frequencies (f_{gco}) without the limitations imposed by the RHP poles and zeros are defined according to Ref. [69] to be as follows:

- $f_{\text{gco}} > 3 \cdot f_n$, where f_n is the resonant frequency of the converter: The resonant pole will cause ringing and control has to eliminate this ringing. For doing so, the control has to have adequate gain at the resonant frequency.
- $f_{\text{gco}} < f_s/5$, where f_s denotes the switching frequency: The high gain at the high frequencies would also amplify the switching ripple, which may affect the pulsewidth generation and lead to instability (cf. Ref. [69]).

Maximum High-Frequency Feedback-Loop Gain

The use of ceramic capacitors at the output of converters [70] may allow using resonant frequencies of the output LC filter approaching the switching frequency of the converter. In case of analog controllers, the internal gain of the used operational amplifiers may pose a stability problem if the feedback loop gain becomes higher than the internal gain of the operational amplifier especially at high frequencies. A typical operational amplifier gain behavior is shown in Figure 2.72, where the GBW (i.e., gain–bandwidth product) equals 1.5 MHz. The differential operational amplifier circuit, which can be used as a feedback controller, is shown in Figure 2.73. Based on Figure 2.73, the feedback-controller transfer function including the effect of the internal gain (G_{OPA}) can be given by

$$G_{\text{cc}}^{\text{OPA}} = \frac{Z_f}{Z_{\text{in}}} \cdot \frac{G_{\text{OPA}}}{1 + G_{\text{OPA}} + (Z_f/Z_{\text{in}})}. \quad (2.150)$$

If the controller is designed in such a way that $Z_f/Z_{\text{in}} > G_{\text{OPA}}$, then $G_{\text{cc}}^{\text{OPA}} \approx G_{\text{OPA}}$, which implies dynamic problems especially if the frequency of occurrence is at high frequencies. If $Z_f/Z_{\text{in}} < G_{\text{OPA}}$, then $G_{\text{cc}}^{\text{OPA}} \approx R_f/R_{\text{in}}$ as it is assumed to be.

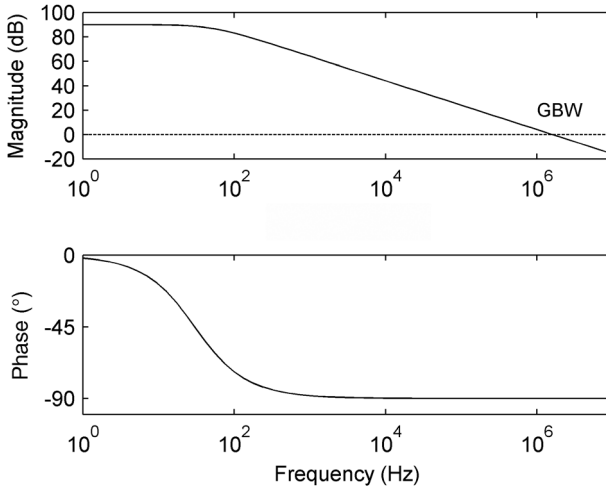


Figure 2.72 The open loop (i.e., internal gain) of an operational amplifier with 1.5-MHz GBW product.

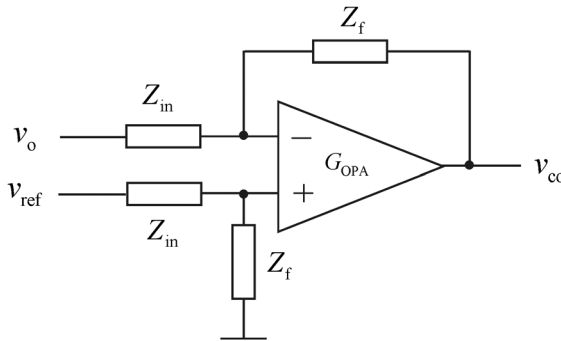


Figure 2.73 Feedback controller based on differential operational amplifier circuit.

2.5.6 Controller Implementations

A general simple feedback controller applied usually in DC–DC power electronic converters based on the circuitry included in the pulse-width modulators (PWM) can be given as shown in Figure 2.74. Resistor R_b is known as a bias resistor, which contributes only to the level of output DC voltage. The transfer function of the general controller can be given by

$$G_{cc} = \frac{Z_f}{Z_{in}}. \quad (2.151)$$

Depending on the impedances Z_f and Z_{in} , the controller can be proportional (P ; type-1) (Figure 2.75a), proportional integral (PI; type-2) (Figure 2.75b), proportional integral derivative (PID; type-3) (Figure 2.75c), or integral (I; type-4) (Figure 2.75d). The P , PI , and PID controllers most often include one high-

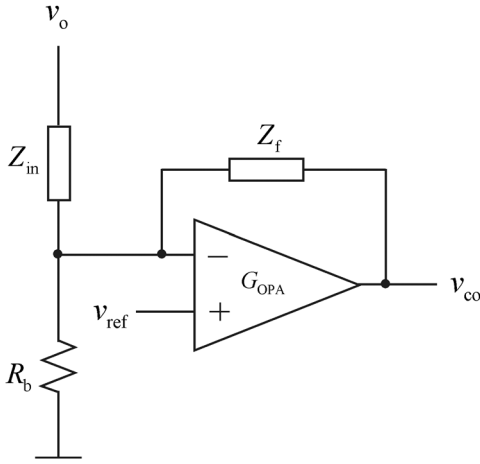


Figure 2.74 Simple analog general control circuitry.

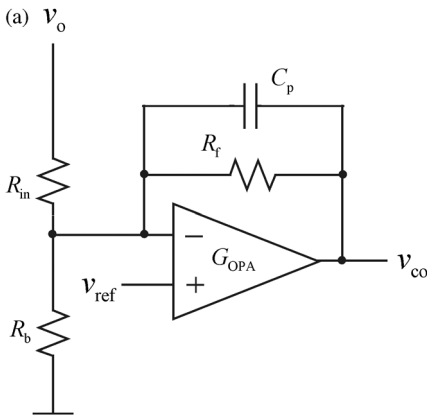
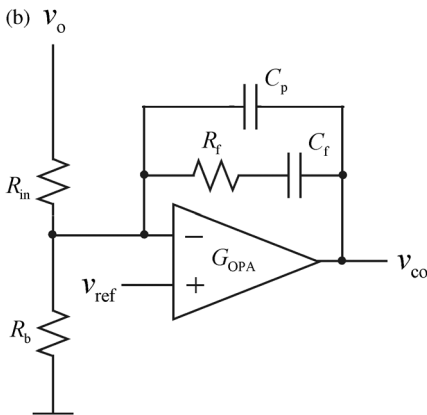


Figure 2.75 Simple analog controller implementations. (a) P. (b) PI. (c) PID. (d) I.



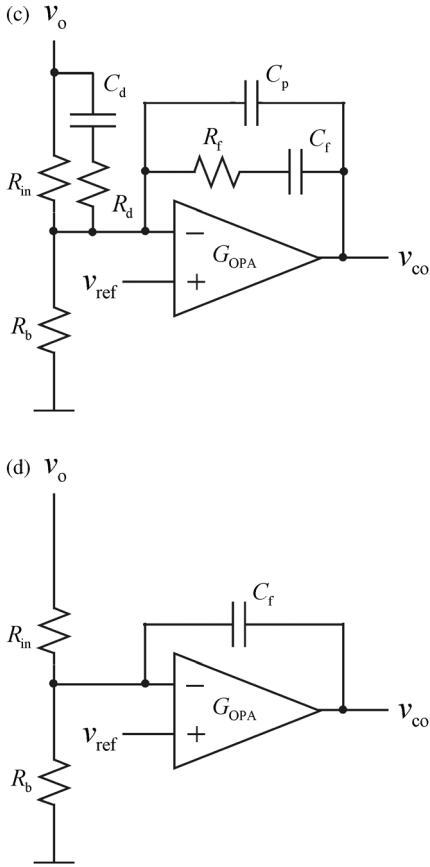


Figure 2.75 (Continued)

frequency pole, which reduces the high-frequency gain of the controller in order to make the control system proper.

The transfer function of the PID controller can be computed from Figure 2.75c yielding

$$G_{cc} = \frac{(1 + sR_f C_f)(1 + s(R_{in} + R_d C_d))}{R_{in} C_f s(1 + sR_d C_d)(1 + sR_f (C_f C_p / (C_f + C_p)))}. \quad (2.152)$$

Typically, $C_p \ll C_f$. Therefore, G_{cc} simplifies to

$$G_{cc} = \frac{(1 + sR_f C_f)(1 + s(R_{in} + R_d C_d))}{R_{in} C_f s(1 + sR_d C_d)(1 + sR_f C_p)}. \quad (2.153)$$

Therefore, the above-mentioned high-frequency pole can be given by $\omega_p \approx 1/R_f C_p$. The frequency response of a PID controller is given in Figure 2.76, where the zeros and poles are denoted based on the generalized representation of the PID controller transfer function given by

$$G_{cc} = \frac{K_{cc}(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s(1 + s/\omega_{p1})(1 + s/\omega_{p2})}, \quad (2.154)$$

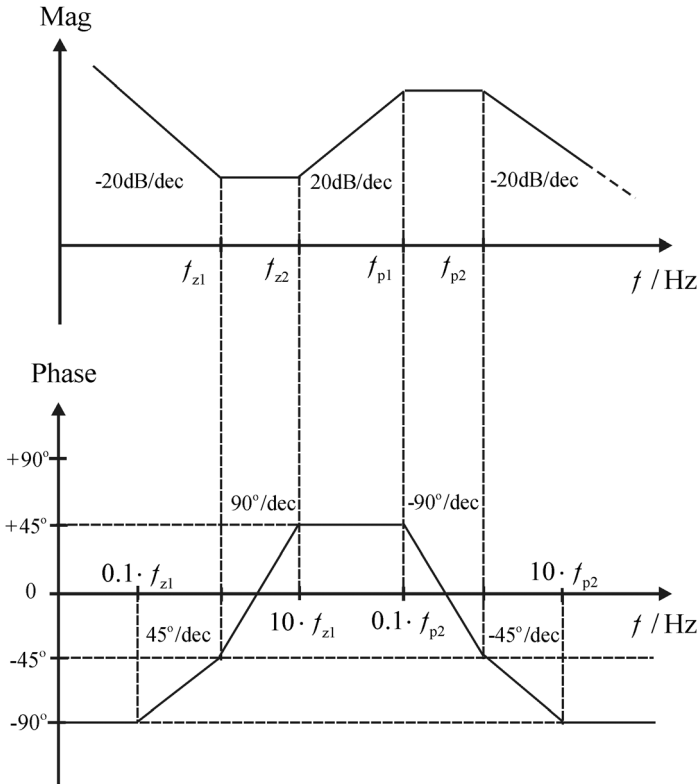


Figure 2.76 Frequency response of a PID controller.

where the different zeros, poles, and K_{cc} can be easily identified based on Eq. (2.154).

The transfer function of a PI controller can be computed from Figure 2.75b yielding

$$G_{cc} = \frac{1 + sR_f C_f}{R_{in} C_f s (1 + sR_f C_p)} = \frac{K_{cc}(1 + s/\omega_{z1})}{s(1 + s/\omega_{p1})} \quad (2.155)$$

and the corresponding frequency response is given in Figure 2.77.

The transfer function of a P controller can be computed from Figure 2.75a yielding

$$G_{cc} = \frac{R_f}{R_{in}(1 + sR_f C_p)} = \frac{K_{cc}}{(1 + s/\omega_{p1})} \quad (2.156)$$

and the corresponding frequency response is given in Figure 2.78.

The transfer function of an I controller can be computed from Figure 2.73d yielding

$$G_{cc} = \frac{1}{sR_{in} C_f} = \frac{K_{cc}}{s} \quad (2.157)$$

and the corresponding frequency response is given in Figure 2.79.

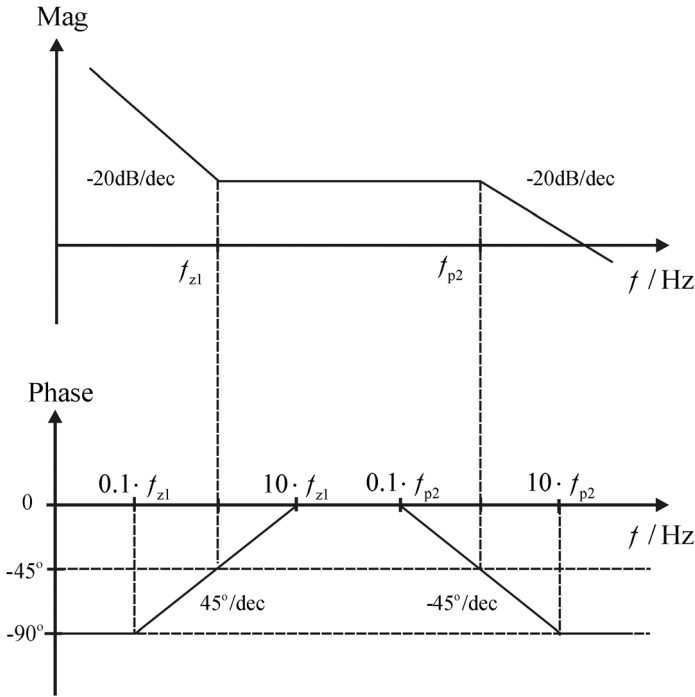


Figure 2.77 Frequency response of a PI controller.

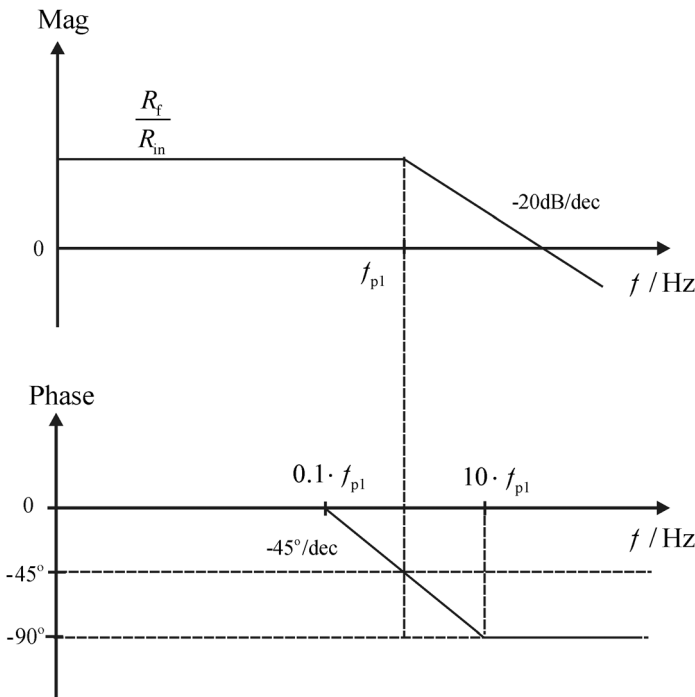


Figure 2.78 Frequency response of a P controller.

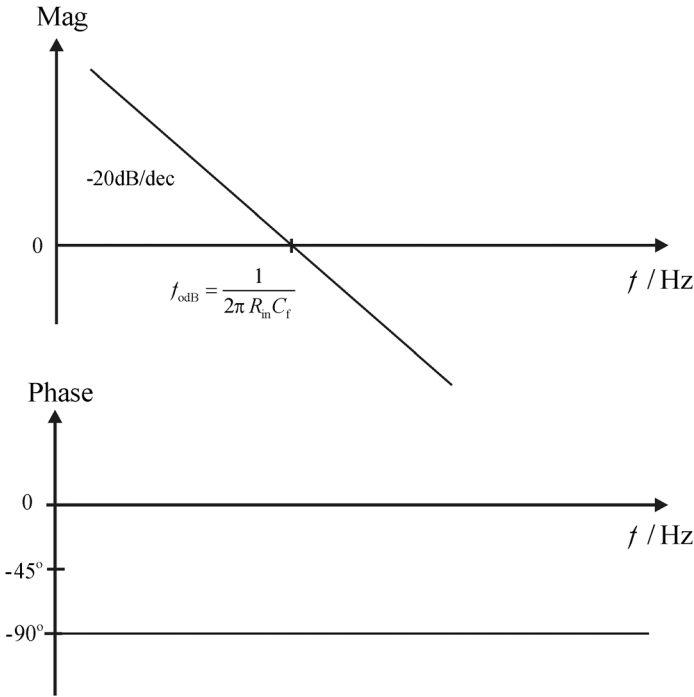


Figure 2.79 Frequency response of an I controller.

2.5.7 Optocoupler Isolation

The feedback loop of the transformer-isolated converters should also be isolated [72]. The most common medium for performing the isolation is an optocoupler [73]. The optocoupler would also be a critical component in the loop, because its current transfer ratio (CTR) can vary substantially depending on the temperature, level of diode current, age, type, and manufacture; it may incorporate an RC circuit-like behavior highly dependent on the collector/emitter resistance. The transfer function describing its dynamic behavior [23] can be given by

$$G_{\text{opto}} \approx \text{CTR} \cdot \frac{(1 - s(t_d/2))}{(1 + s/\omega_{-3\text{dB}})(1 + s(t_d/2))}, \quad (2.158)$$

where the effect of the delay (t_d) is approximated by using the first-order *Padé* approximation of e^{-st_d} . In theory, the delay increases only the phase lag by $-\omega t_d$ (in radians) but does not affect the magnitude at all (i.e., $e^{-st_d} = 1 \angle -\omega t_d$). The delay is usually given explicitly in the data sheet. Section 2.5.8 gives more information on the different *Padé* approximations and their validity. The cutoff frequency ($\omega_{-3\text{dB}}$) can be found from the frequency responses typically given by the manufacturer at different collector resistors or from the time-domain response given at a certain collector resistor (R_{c1}): The rise time (t_r) and the corresponding cutoff frequency are related by $\omega_{-3\text{dB}} \approx 2.2/t_r$, from which the equivalent $C_{\text{opto}} \approx 0.455 \cdot t_r/R_{c1}$. The corresponding $\omega_{-3\text{dB}}$ at the used collector resistor (R_{c2}) equals $(R_{c1}/R_{c2})(2.2/t_r)$.

2.5.8 Application of Digital Control

The control design can be performed completely in continuous time based on the frequency-domain transfer functions even if the practical control is implemented in discrete time or Z -domain by using digital signal processor. The feedback/feedforward variables are sampled by using analog–digital converters, which introduce a delay (T_d) in the feedback/feedforward loops, which has to be also added in the continuous-time feedback/feedforward loops when performing the controller design [74]. Figure 2.80 shows the location of the delay block G_d in the input and output dynamics of the converter, that is, it is connected to the control signal U_c . The same procedures apply despite the number of feedback/feedforward loops in the converter. Usually the sampling of the variables takes place once

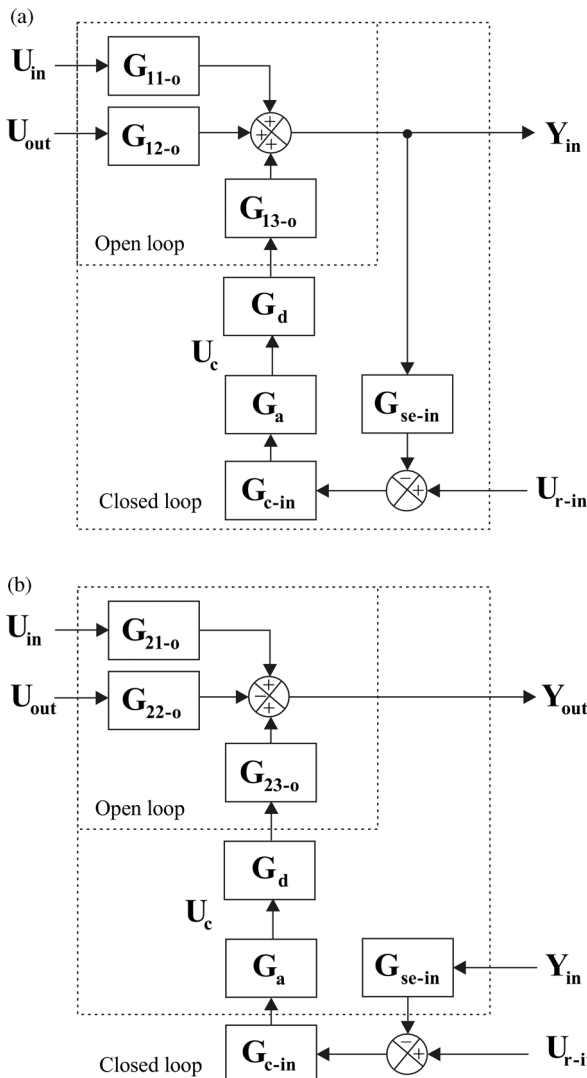


Figure 2.80 The adding of the delay block into (a) the input and (b) output dynamics.

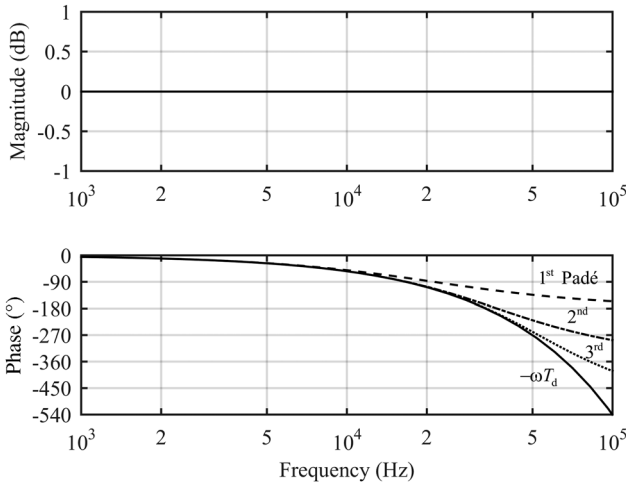


Figure 2.81 The effect of control delay on the phase shift of the feedback loop when $T_d \approx 1.5T_s$.

in a switching cycle T_s , and the typically used delay $T_d \approx 1.5T_s$. In *Laplace* domain, the delay equals $e^{-T_d s}$, which is usually approximated by using the first-order Padé approximation by

$$e^{-T_d s} \approx \frac{1 - s(T_d/2)}{1 + s(T_d/2)}. \quad (2.159)$$

Figure 2.81 shows the validity of the first-order (Eq. (2.159)), the second-order (Eq. (2.160)), and the third-order (Eq. (2.161)) Padé approximations when the switching frequency (f_s) is 100 kHz and, therefore, $T_d \approx 15 \mu s$. As stated earlier, the maximum recommended feedback-loop crossover frequency should be limited to $f_s/5$. Figure 2.81 indicates that the first-order *Padé* approximation does not correctly model the phase behavior of the delay (i.e., -86° versus -108°) at $f_s/5$. The second- and third-order approximations coincide with the real phase of the delay. If $T_d \leq T_s$, then the first-order approximation predicts correctly the phase shift imposed by the control delay at $f_s/5$.

$$e^{-T_d s} \approx \frac{1 - s(T_d/2) + s^2(T_d^2/12)}{1 + s(T_d/2) + s^2(T_d^2/12)} \quad (2.160)$$

$$e^{-T_d s} \approx \frac{1 - s(T_d/2) + s^2(T_d^2/10) - s^3(T_d^3/120)}{1 + s(T_d/2) + s^2(T_d^2/10) + s^3(T_d^3/120)}. \quad (2.161)$$

2.6 Resonant LC-Type Circuits

2.6.1 Introduction

In power electronics, the resonant circuits have a significant effect on control design but their behavior seems to be quite poorly understood. Therefore, we will present here some fundamental basics related to the LC (Figure 2.82), LCL (Figure 2.83), and CLCL (Figure 2.84) circuits. In DC–DC converters, an LC-type

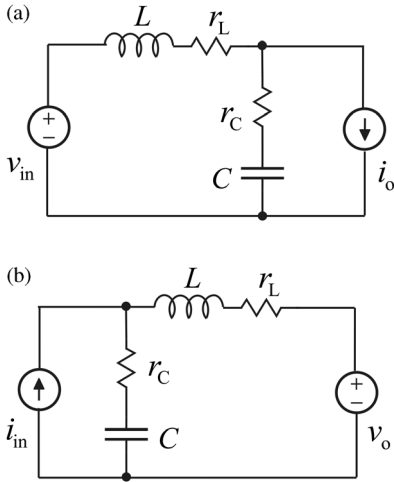


Figure 2.82 Single-section LC filters. (a) Voltage-fed filter. (b) Current-fed filter.

input filter has to be usually added at the input terminals of the converters for suppressing the power-stage input-current ripple (cf. Figure 2.82a) or input-voltage ripple (cf. Figure 2.82b) to an acceptable level stipulated by the relevant EMC standards. The first-filter topology is used in the conventional or voltage-fed applications, and the last topology in the current-fed applications. The filters are actually the dual of each other. In the voltage-fed inverters, the LCL-type filter (cf. Figure 2.83) is usually added to the output terminals of the converter for suppressing the ripples of the inverter output current to an acceptable level. In the current-fed applications, an input capacitor has to be added at the input terminal of the power stage of the inverter for enabling its use in the current-fed applications. As a consequence, the overall filter including the output LCL filter

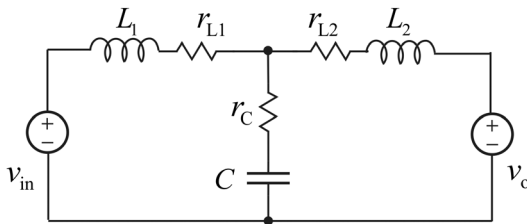


Figure 2.83 LCL-type output filter of the grid-connected voltage-fed inverter.

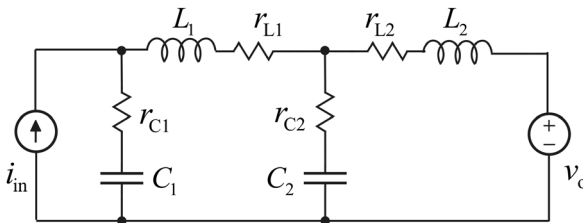


Figure 2.84 CLCL-type filter of the grid-connected current-fed inverter.

and the input capacitor resembles the CLCL filter depicted in Figure 2.84. All the filter topologies contain both series and parallel resonant behaviors having characteristic features, which have to be known for understanding their effects on the overall dynamics of the associated systems.

2.6.2 Single-Section LC Filter

The dynamic representations of the voltage-fed and current-fed LC filters can be given as G and H parameter sets by

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \frac{\begin{bmatrix} sC & 1 + sr_C C \\ 1 + sr_C C & -(r_L + sL)(1 + sr_C C) \end{bmatrix}}{s^2 LC + s(r_L + r_C)C + 1} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix}, \quad (2.162)$$

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \frac{\begin{bmatrix} (r_L + sL)(1 + sr_C C) & 1 + sr_C C \\ 1 + sr_C C & -sC \end{bmatrix}}{s^2 LC + s(r_L + r_C)C + 1} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix}, \quad (2.163)$$

where all the elements would exhibit parallel resonant characteristics, that is, peaking at the resonant frequency $\omega_{res} = \omega_n \sqrt{1 - 2\zeta^2} = \frac{1}{\sqrt{LC}} \sqrt{1 - [(r_L + r_C)^2 C / (2L)]}$. The elements G_{11} and G_{22} in both of the sets have ohmic characteristics. If both of these elements are given as impedances, we can observe that the series resonant features are related to

$$\frac{s^2 LC + s(r_L + r_C)C + 1}{sC} \quad (2.164)$$

and the parallel resonant features to

$$\frac{(r_L + sL)(1 + sr_C C)}{s^2 LC + s(r_L + r_C)C + 1}. \quad (2.165)$$

The frequency responses of the series (Eq. (2.164)) and parallel (Eq. (2.165)) impedances are shown in Figure 2.85. The magnitudes of the impedances at the resonant frequency can be computed by substituting $s = j\omega_{res}$ and developing the magnitudes of the resulting complex numbers. Following these procedures, we can obtain

$$Z_{par-max} = \frac{R_o^2 \sqrt{1 + (r_L^2 / 2R_o^2)} \sqrt{1 + (r_C^2 / R_o^2)(1 - (r_L^2 / 2R_o^2))}}{r_L + r_C} \approx \frac{R_o^2}{r_L + r_C} \quad (2.166)$$

and

$$Z_{ser-min} = (r_L + r_C) \frac{\sqrt{1 - [(r_L + r_C)^2 / 4R_o^2]}}{\sqrt{1 - [(r_L + r_C)^2 / 2R_o^2]}} \approx r_L + r_C, \quad (2.167)$$

where $R_o = \sqrt{L/C}$ denotes the characteristic impedance of a resonant circuit, that is, $\omega_n L = 1/\omega_n C = R_o$. As discussed in detail in Section 2.5.2, the damping

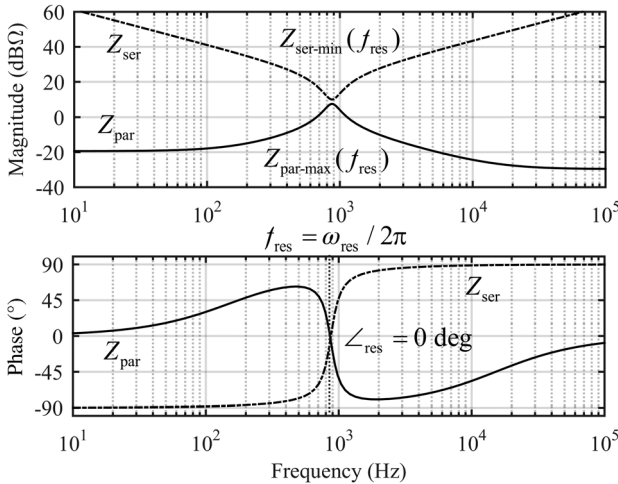


Figure 2.85 Bode plots of parallel (solid line) and series (dash-dotted line) impedances.

factor $\zeta = (r_L + r_C)/2R_o$ and the quality factor $Q = R_o/(r_L + r_C)$. The changes in the damping as long as the circuit retains its resonant nature do not affect the magnitude dip of the series resonant circuit, but significantly the peak magnitude of the parallel resonant circuit. It should be noticed that the peak magnitude of the series resonant circuit is dependent on the characteristic impedance (R_o) by square. This means that if the inductance value increases, then the peak value increases in direct relation to the inductance value. The opposite takes place with respect to the changes in the capacitance value. As a summary, the changes in the inductance and capacitance values affect always the resonant frequency and also the peak magnitude of the parallel resonant circuit. It shall be noticed that peaking in the parallel resonant circuit takes place only when $\zeta < 1/\sqrt{2}$.

The maximum value of the other parallel resonant circuits in Eqs. (2.162) and (2.163) (i.e., the matrix elements (1,2) and (2,1)) can be given by

$$G_{\max} = \frac{R_o}{r_L + r_C} = Q, \quad (2.168)$$

which indicates that the quality factor corresponds directly to the maximum value of these output-to-input and input-to-output transfer functions.

2.6.3 LCL Filter

The dynamic representation of the LCL filter as a set of Y parameters can be given by

$$\begin{bmatrix} \hat{i}_{\text{in}} \\ \hat{i}_{\text{o}} \end{bmatrix} = \frac{\begin{bmatrix} s^2 L_2 C + s(r_{L2} + r_C)C + 1 & -(1 + sr_C C) \\ 1 + sr_C C & -(s^2 L_1 C + s(r_{L1} + r_C)C + 1) \end{bmatrix}}{\Delta} \begin{bmatrix} \hat{v}_{\text{in}} \\ \hat{v}_{\text{o}} \end{bmatrix}, \quad (2.169)$$

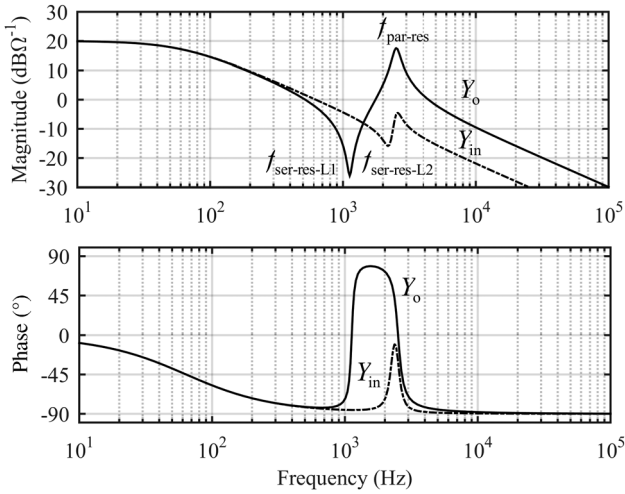


Figure 2.86 The frequency responses of the input admittance (dash–dotted line) and output admittance (solid line).

where

$$\Delta = s^3 L_1 L_2 C + s^2 (L_1 (r_{L2} + r_C) + L_2 (r_{L1} + r_C)) C + s (L_1 + L_2 + (r_{L1} r_{L2} + r_C (r_{L1} + r_{L2})) C) + r_{L1} + r_{L2}. \quad (2.170)$$

According to the denominator of the system in Eq. (2.170), there is one pole close to the origin (i.e., approximately at $(r_{L1} + r_{L2}) / (L_1 + L_2)$) and a resonant double pole approximately at $1 / \sqrt{(L_1 \parallel L_2) C}$. The double pole represents naturally the parallel resonance involved in the system. According to Eq. (2.169), the circuit

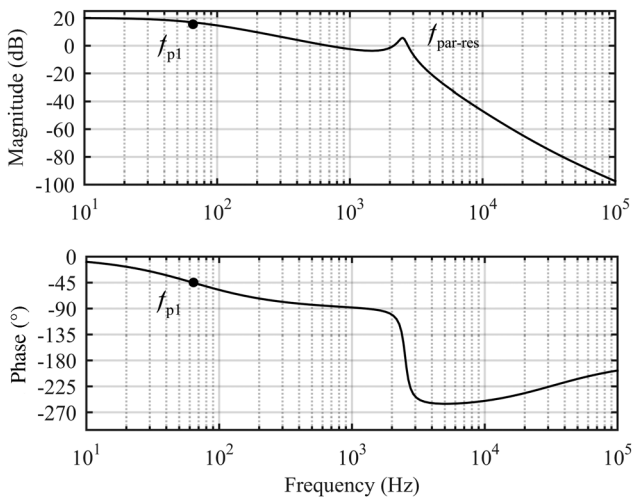


Figure 2.87 The frequency response of the input-to-output transfer function (G_{io}).

inductors form with the circuit capacitor separate series resonances having double zeros at $1/L_1C$ and $1/L_2C$, respectively. According to the symbolic forms of the resonances, the series resonances locate always at the lower frequency than the parallel resonance as clearly visible in Figure 2.85, where the frequency responses of the input (i.e., the element G_{11}) and output (i.e., element G_{22}) admittances of the LCL filter are shown. In the other two transfer functions, only the parallel resonance and the low-frequency pole are clearly visible, as shown in Figures 2.86 and 2.87.

2.6.4 CLCL Filter

The dynamic representation of the CLCL filter as a set of H parameters can be given by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \frac{\begin{bmatrix} \Delta Z_{in} & \Delta T_{oi} \\ \Delta G_{io} & -\Delta Y_o \end{bmatrix}}{\Delta} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix}, \quad (2.171)$$

where

$$\begin{aligned} \Delta Z_{in} &= (s^3 L_1 L_2 C_2 + s^2((r_{L2} + r_{C2})L_1 + (r_{L1} + r_{C2})L_2)C_2 \\ &\quad + s(L_1 + L_2 + (r_{L1}(r_{L2} + r_{C2}) + r_{L2}r_{C2})C_2) + r_{L1} + r_{L2})(1 + sr_{C1}C_1), \\ \Delta G_{io} &= \Delta T_{oi} = (1 + sr_{C1}C_1)(1 + sr_{C2}C_2), \\ \Delta Y_o &= (C_1 + C_2) \left(s^2 L_2 \frac{C_1 C_2}{C_1 + C_2} + s(r_{L1} + r_{C1} + r_{C2}) \frac{C_1 C_2}{C_1 + C_2} + 1 \right), \end{aligned} \quad (2.172)$$

and the denominator of the system

$$\begin{aligned} \Delta &= s^4 L_1 L_2 C_1 C_2 + s^3 (L_1(r_{L2} + r_{C2}) + L_2(r_{L1} + r_{C1} + r_{C2}))C_1 C_2 \\ &\quad + s^2 (L_1 C_1 + L_2(C_1 + C_2) + (r_{L1} + r_{C1})(r_{L2} + r_{C2}) + r_{L2}r_{C2})C_1 C_2 \\ &\quad + s((r_{L1} + r_{L2} + r_{C1})C_1 + (r_{L2} + r_{C2})C_2) + 1. \end{aligned} \quad (2.173)$$

The system is of fourth order as Eq. (2.173) clearly indicates. Therefore, it is quite difficult to exactly define the resonant frequencies the circuit contains. We can state that there are two complex conjugate pole pairs in the system, which locate approximately at

$$\omega_{res1,2} \approx \sqrt{\frac{1}{2} \cdot \left(\frac{1}{L_2 C_2} + \frac{C_1 + C_2}{L_1 C_1 C_2} \right) \pm \sqrt{\left(\frac{1}{2} \cdot \left(\frac{1}{L_2 C_2} + \frac{C_1 + C_2}{L_1 C_1 C_2} \right) \right)^2 - \frac{1}{L_1 L_2 C_1 C_2}}}, \quad (2.174)$$

which are clearly visible in the plot of the frequency response of the input-to-output transfer function (G_{io}) given in Figure 2.88.

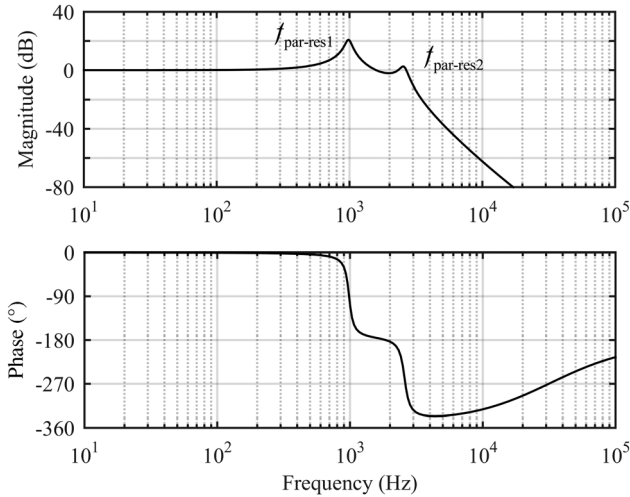


Figure 2.88 The frequency response of the input-to-output transfer function (G_{io}).

The output admittance (Y_o) (cf. Figure 2.89) and input impedance (Z_{in}) (cf. Figure 2.88) also contain one series resonance, which can be easily derived for Y_o from the corresponding symbolic form given in Eq. (2.172) (i.e., $\omega_{\text{ser-res}} = 1/\sqrt{L_2[C_1C_2/(C_1 + C_2)]}$) but not so easily for Z_{in} due to the third-order nature of the numerator term: Z_{in} also contains one single zero approximately at $\omega_{z1} = (r_{L1} + r_{L2})/(L_1 + L_2)$ in addition to the resonant zero approximately at $\omega_{\text{ser-res}} = 1/\sqrt{L_1L_2/(L_1 + L_2)} \times C_2$ as indicated in Figure 2.90.

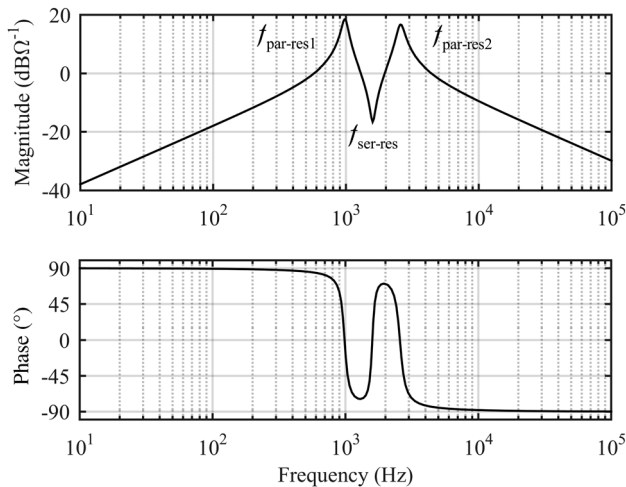


Figure 2.89 The frequency response of the output impedance (Y_o).

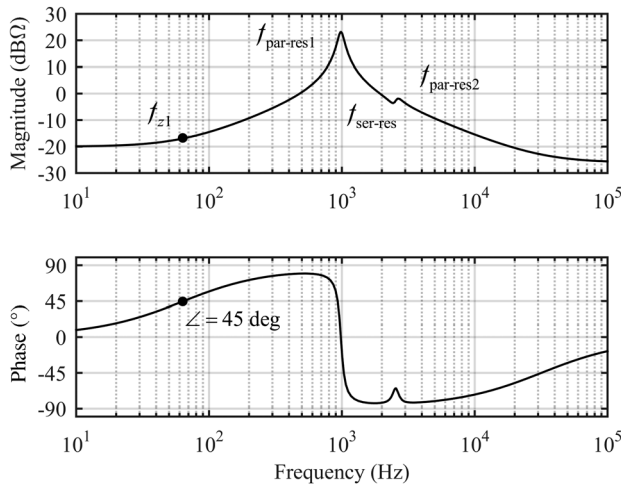


Figure 2.90 The frequency response of the input impedance (Z_{in}).

References

- 1 Middlebrook, R.D. and Čuk, S. (1977) A general unified approach to modeling switching-converter power stages. *Int. J. Electron.*, **42** (6), 521–550.
- 2 Middlebrook, R.D. (1976) Input filter considerations in design and applications of switching regulators. Proceedings of the IEEE Industrial and Applied Society Annual Meeting, pp. 91–107.
- 3 Middlebrook, R.D. (1978) Design techniques for preventing input-filter oscillations in switched-mode regulators. Proceedings of the Power Conversion Conference, pp. A3.1–A3.16.
- 4 Middlebrook, R.D. (1989) Null double injection and the extra element theorem. *IEEE Trans. Educ.*, **32** (3), 167–180.
- 5 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters: Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.
- 6 Maranesi, P.G., Tavazzi, V., and Varoli, V. (1988) Two-port characterization of PWM voltage regulators at low frequencies. *IEEE Trans. Ind. Electron.*, **35** (3), 444–450.
- 7 Tse, C.K. (1998) *Linear Circuit Analysis*, Addison-Wesley, Harlow, UK.
- 8 Shoyama, M., Hamafuku, Y., Matsuzaki, N., and Ninomiya, T. (1995) Simplification of transfer functions in switching converter with generalized load impedance. Proceedings of the IEEE PEDS, pp. 155–161.
- 9 Suntio, T. and Gadoura, I. (2002) Use of unterminated two-port modeling technique in analysis of input filter interactions in telecom DPS systems, Proceedings of the IEEE INTELEC, pp. 560–565.
- 10 Cvetkovic, I. *et al.* (2013) Unterminated small-signal behavioral model of DC–DC converters. *IEEE Trans. Power Electron.*, **28** (4), 1870–1879.
- 11 Hankaniemi, M. and Suntio, T. (2006) Small-signal models for constant-current regulated converters. Proceedings of the IEEE IECON, pp. 2037–2042.

- 12 Leppäaho, J., Huusari, J., Nousiainen, L., Puukko, J., and Suntio, T. (2011) Dynamic properties and stability assessment of current-fed converters in photovoltaic applications. *IEEE Trans. Ind. Appl.*, **131** (8), 976–984.
- 13 Suntio, T., Hankaniemi, M., and Karppanen, M. (2006) Analysing the dynamics of regulated converters. *IEE Proc. Electric Power Appl.*, **153** (6), 905–910.
- 14 Hankaniemi, M., Karppanen, M., and Suntio, T. (2006) Load imposed instability and performance degradation in a regulated converter. *IEE Proc. Electric Power Appl.*, **153** (6), 781–786.
- 15 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Effect of control method on impedance-based interactions in a buck converter. *IEEE Trans. Power Electron.*, **28** (11), 5311–5322.
- 16 Cvetkovic, I., Jaksic, M.M., Boroyevich, D., Mattavelli, P., Lee, F.C., Shen, Z., Ahmed, S., and Dong, D. (2011) Unterminated, low-frequency terminal-behavioral d - q model of three-phase converters. Proceedings of the IEEE ECCE, pp. 791–798.
- 17 Puukko, J. and Suntio, T. (2012) Dynamic properties of a voltage source inverter-based three-phase inverter in photovoltaic application. *IET Renew. Power Gen.*, **6** (6), 381–391.
- 18 Puukko, J. and Suntio, T. (2012) Modelling the effect of a non-ideal load in three-phase converter dynamics. *IET Electron. Lett.*, **48** (7), 402–404.
- 19 Messo, T., Jokipii, J., Puukko, J., and Suntio, T. (2014) Determining the value of DC-link capacitance to ensure stable operation of three-phase photovoltaic inverter. *IEEE Trans. Power Electron.*, **29** (2), 665–673.
- 20 Suntio, T., Viinamäki, J., Jokipii, J., Messo, T., and Kuperman, A. (2014) Dynamic characteristics of power electronic interfaces. *IEEE J. Emerg. Sel. Topics Power Electron.*, **2** (4), 949–961.
- 21 Suntio, T., Gadoura, I., Lempinen, J., and Zenger, K. (2000) Practical design issues of multi-loop controller for a telecom rectifier. Proceedings of the IEEE TELESCON, pp. 197–201.
- 22 Hankaniemi, M. and Suntio, T. (2006) Small-signal models for constant-current regulated converters. Proceedings of the IEEE IECON, pp. 2037–2042.
- 23 Lempinen, J. and Suntio, T. (2001) Modeling and analysis of a self-oscillating peak-current controlled flyback converter. Proceedings of the IEEE IECON, pp. 960–965.
- 24 Zenger, K., Altowati, A., and Suntio, T. (2006) Dynamic properties of interconnected power systems: a system theoretic approach. Proceedings of the IEEE ICIEA, pp. 835–840.
- 25 Figueres, E., Garcerá, G., Sandia, J., González-Espín, F., and Calvo Rubio, J. (2009) Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter. *IEEE Trans. Ind., Electron.*, **56** (3), 706–717.
- 26 Blaabjerg, F., Teodorescu, R., Liserre, M., and Timbus, A. (2006) Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.*, **53** (5), 1398–1409.
- 27 Duesterhoeft, W.C., Schulz, M.W., and Clarke, E. (1951) Determination of instantaneous currents and voltages by means of alpha, beta, and zero components. *AIEE Trans.*, **70** (2), 1248–1255.
- 28 Park, R.H. (1929) Two-reaction theory of synchronous machines: generalized method of analysis – Part I. *AIEE Trans.*, **48** (3), 716–727.

- 29 Harnefors, L. (2007) Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices. *IEEE Trans. Ind. Electron.*, **54** (4), 2239–2248.
- 30 Kwon, J., Yoon, S., and Choi, S. (2012) Indirect current control for seamless transfer of three-phase utility interactive inverters. *IEEE Trans. Power Electron.*, **27** (2), 773–781.
- 31 Maciejowski, J.M. (1989) *Multivariable Feedback Design*, Addison-Wesley, Wokingham, UK.
- 32 Skogestad, S. and Postlethwaite, I. (1996) *Multivariable Feedback Control: Analysis and Design*, John Wiley & Sons, Inc., Chichester, UK.
- 33 Desoer, C.A. and Wang, Y.-T. (1980) On the generalized Nyquist stability criterion. *IEEE Trans. Autom. Control*, **AC-25** (2), 187–196.
- 34 MacFarlane, A.G.J. and Postlethwaite, I. (1977) The generalized Nyquist stability criterion and multivariable root loci. *Int. J. Control*, **25** (1), 81–127.
- 35 Wester, G.W. and Middlebrook, R.D. (1973) Low-frequency characterization of switched-mode DC–DC converters. *IEEE Trans. Aerosp. Electron. Syst.*, **AES-9** (3), 376–385.
- 36 Ćuk, S. and Middlebrook, R.D. (1977) A general unified approach to modelling switching DC-to-DC converters in discontinuous conduction mode. Proceedings of the IEEE PESC, pp. 36–57.
- 37 Sun, J., Mitchell, D.M., Gruel, M.F., Krein, P.T., and Bass, R.M. (2001) Average modeling of PWM converters in discontinuous modes. *IEEE Trans. Power Electron.*, **16** (4), 482–492.
- 38 Suntio, T. (2006) Unified average and small-signal modeling of direct-on-time control. *IEEE Trans. Ind. Electron.*, **53** (1), 287–295.
- 39 Suntio, T., Hankaniemi, M., and Roinila, T. (2007) Dynamical modelling of peak-current-mode controlled converter in continuous conduction mode. *J. Simul. Model. Pract. Theory*, **15** (10), 1320–1337.
- 40 Suntio, T. (2001) Analysis and modelling of peak-current-mode controlled buck converter in DICM. *IEEE Ind. Electron.*, **48** (1), 127–135.
- 41 Suntio, T., Lempinen, J., Gadoura, I., and Zenger, K. (2001) Dynamic effects of inductor current ripple in average current mode control. Proceedings of the IEEE PESC, pp. 1259–1264.
- 42 Suntio, T. (2006) Average and small-signal modelling of self-oscillating flyback converter with applied switching delay. *IEEE Trans. Power Electron.*, **21** (2), 479–486.
- 43 Leppäaho, J. and Suntio, T. (2011) Dynamic characteristics of current-fed superbuck converter. *IEEE Trans. Power Electron.*, **26** (1), 200–209.
- 44 Erickson, R.W. and Maksimović, D. (2001) *Fundamentals of Power Electronics*, Kluwer Academic Publishers, Norwell, MA.
- 45 Antsaklis, P.J. and Michel, A.N. (1977) *Linear Systems*, McGraw-Hill, New York.
- 46 Weaver, W.W. and Krein, P.T. (2007) Analysis and applications of a current-source buck converter. Proceedings of the IEEE APEC, pp. 1664–1670.
- 47 Veerachary, M. (2005) Two-loop voltage-mode control of coupled inductor step-down buck converter. *IET Proc. Electric Power Appl.*, **152** (6), 1516–1524.

- 48 Huusari, J., Leppäaho, J., and Suntio, T. (2010) Dynamic properties of PCM-controlled superbuck converter: discrete vs. coupled inductor implementation. *Eur. Power Electron. Drives J.*, **20** (2), 8–15.
- 49 Ćuk, S. (1983) A new zero-ripple DC-to-DC converter and integrated magnetics. *IEEE Trans. Magn.*, **MAG-19** (2), 57–75.
- 50 Bobrow, L.S. (1987) *Elementary Linear Circuit Analysis*, Oxford University Press, Oxford, NY. Akagi, H., Watanabe, E.H. and Aredes, M., (2007) *Instantaneous Power Theory and Applications to Power Conditioning*, John Wiley & Sons, Inc., Hoboken, NY.
- 51 Sammaljärvi, T., Lakhdari, F., Karppanen, M., and Suntio, T. (2008) Modelling and dynamic characterisation of peak-current-mode-controlled superboost converter. *IET Power Electron.*, **1** (4), 527–536.
- 52 Dorf, R.C. and Bishop, R.H. (1998) *Modern Control Systems*, Addison-Wesley, Menlo Park, CA.
- 53 Ogata, K. *Modern Control Engineering*, Prentice-Hall, Upper Saddle River, NJ.
- 54 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Impedance-based stability and transient-performance assessment applying maximum peak criteria. *IEEE Trans. Power Electron.*, **28** (5), 2099–2104.
- 55 Sun, J. (2011) Impedance-based stability criterion for grid-connected inverters. *IEEE Trans. Power Electron.*, **26** (11), 3075–3078.
- 56 Sudhoff, S.D., Glover, S.F., Lamm, P.T., Schmucker, D.H., and Delisle, D.-E. (2000) Admittance space stability analysis of power electronic systems. *IEEE Trans. Aerosp. Electron. Syst.*, **36** (3), 965–973.
- 57 Wildrick, C.M., Lee, F.C., Cho, B.H., and Choi, B. (1995) A method for defining the load impedance specifications for a stable distributed power system. *IEEE Trans. Power Electron.*, **10** (3), 280–285.
- 58 Feng, X., Liu, J., and Lee, F.C. (2002) Impedance specification for stable DC distributed system. *IEEE Trans. Power Electron.*, **17** (2), 157–162.
- 59 Liu, J., Feng, X., Lee, F.C., and Borojevich, D. (2002) PEBB system stability margin monitoring. *J. Vib. Control*, **8** (2), 261–276.
- 60 Liu, J., Feng, X., Lee, F.C., and Borojevich, D. (2002) Stability margin monitoring using voltage perturbation for DC distributed power system. *J. Vib. Control*, **8** (2), 277–288.
- 61 Liu, J., Feng, X., Lee, F.C., and Borojevich, D. (2003) Stability margin monitoring for distributed power systems via perturbation approaches. *IEEE Trans. Power Electron.*, **18** (6), 1254–1261.
- 62 Liu, Z., Liu, J., Bao, W., and Zhao, Y. (2015) Infinity-norm of impedance-based stability criterion for three-phase AC distributed power systems with constant power loads. *IEEE Trans. Power Electron.*, **30** (6), 3030–3043.
- 63 Choi, B. (2013) *Pulsewidth Modulated DC-to-DC Power Conversion – Circuits, Dynamics, and Control Designs*, John Wiley & Sons, Inc., Hoboken, NJ.
- 64 Suntio, T. and Kivimäki, J. (2014) Physical insight into the factors affecting the load-transient response of a buck converter. Proceedings of the EPE-ECCE, pp. 1–10.
- 65 Karppanen, M., Hankaniemi, M., Suntio, T., and Sippola, M. (2007) Dynamical characterization of peak-current-mode-controlled buck converter with output-current feedforward. *IEEE Trans. Power Electron.*, **22** (2), 444–451.

- 66 Venable, D. (1997) Optimum feedback amplifier design for control systems. Technical Report 3, Venable Industries, Inc., Austin, TX. Available at www.venable.biz.
- 67 Jacobs, M.E. (2006) Optimal feedback control of switched-mode. Proceedings of the IEEE INTELEC, pp. 239–253.
- 68 Freudenberg, J.S. and Looze, D.P. (1995) Right half plane poles and zeros and design tradeoffs in feedback systems. *IEEE Trans. Automat. Contr.*, **AC-30** (6), 555–565.
- 69 Ridley, R. (2006) Loop gain crossover frequency. *Switching Power Magazine*. Available at www.switchingpowermagazine.com.
- 70 Banerjee, S. and Verghese, G.C. (2001) *Nonlinear Phenomena in Power Electronics*, IEEE Press, Inc., New York, NY.
- 71 Miftakhutdinov, R. (2004) Compensating DC/DC converters with ceramic output capacitors. Proceedings of the Power Supply Design Seminar (SEM 1600), Texas Instruments, Dallas, TX, pp. 7-1–7-15.
- 72 Mammano, R. (1994) Isolating the control loop. Proceedings of the Power Supply Design Seminar (SEM-100), Unitrode Corp., Merrimack, NH, pp. C2-1–C2-15.
- 73 Panov, Y. and Jovanovic, M.M. (2005) Small-signal analysis and control design of isolated power supplies with optocoupler feedback. *IEEE Trans. Power Electron.*, **20** (4), 823–832.
- 74 Buso, S. and Mattavelli, P. (2006) *Digital Control in Power Electronics*, Morgan & Claypool.

Part Two

Voltage-Fed DC-DC Converters

3

Dynamic Modeling of Direct-on-Time Control

3.1 Introduction

This chapter provides the unified basis for the average and small-signal modeling of voltage-fed switched-mode converters under direct-on-time (DOT) control in continuous (CCM) and discontinuous (DCM) conduction modes [1]. In case of fixed switching frequency, the control mode will be referred as direct duty ratio (DDR) control, because the same dynamics associated with the on-time is also present in the duty ratio (i.e., $d = t_{\text{on}}/T_s$). If the switching frequency is varying, then the dynamic modeling has to be performed applying the DOT control method, because the duty ratio is then a nonlinear function of on-time and cycle time (i.e., $d = t_{\text{on}}/t_s$) and cannot be used as the control variable [1]. The DDR control is also known widely as voltage-mode control (VMC) [2]. The name VMC should be, however, reserved for the capacitor voltage-based internal control methods in current-fed converters (cf. Chapter 4), similarly as the inductor current-based internal control methods are known generally as current-mode control (CMC). The DOT and DDR models are important, because they form the basis for the other internal control methods such as peak-current-mode (PCM), average-current-mode (ACM), hysteretic current-mode (HCM), and self-oscillation control [1]. The modeling of the dynamics of the converters under the named internal control methods can be performed by finding the dynamics associated with the on-time and duty ratio when the new control method is applied. The relation is known as on-time or duty-ratio constraints [1,2].

The dynamic modeling of the switched-mode converters dates back to early 1970s, when first attempts to produce such models were published in Ref. [3]. The famous state-space averaging (SSA) technique, introduced in Ref. [4], is actually an extension and improvement of Ref. [3]. It was first developed for CCM and later also extended to DCM [5]. The DCM modeling failed to produce accurate models because of considering the inductor current to lose its derivative at the end of a switching cycle. The accurate models for the DCM operation were developed about 20 years later, where the inductor current derivative is correctly addressed to the input and output voltages as well as to the inductor value and switching frequency [6,7]. The basic finding of the unified modeling method introduced in Ref. [7] is that the dynamics of the

converter was associated with the time-averages of the instantaneous circuit variables. As a consequence, all the variables are continuous functions of time regardless of the operational mode of the converter. In practice, this means that the dynamic behavior of the converter seen from its input and output terminals is mainly contributed by the time-averaged variables, where the averaging is performed over one switching cycle. If feedback or feedforward signals are applied either to implementing the usual feedback signals or to producing different modes such as current-mode control, the ripple components superimposed on the time-averaged signals may produce ripple effects on the converter dynamics, which may even lead to instability under certain conditions [8,9].

The pulse width modulators (PWM), which are used to produce the switching actions in power electronic converters, are noticed to affect the dynamics of the converter at the frequencies close to the switching frequency when using internal inductor current-based feedback schemes [10]. Under DOT or DDR control, the response of the PWM to the sinusoidal injection is found to be, however, linear [11] without causing any extra phase shift or affecting the magnitude of the signal.

The modeling is still usually carried out by using resistive loading, as in Ref. [2], even if it is well known already [1] that such models are load affected and do not really represent the dynamics incorporated into the power electronic converters. In case of DOT or DDR control, the major effect of the load resistor can be addressed to the extra damping of the converter internal resonances. In CMC-controlled converters, the resistor will totally hide the real dynamic behavior of the converter [1]. Therefore, it is highly recommended to use the corresponding ideal load (i.e., a current source for the voltage-output converters, and a voltage source for the current-output converters) when performing the analytic modeling. The same also applies for measuring the corresponding frequency responses. The CMC-controlled converters are actually current-output converters at open loop. The output-voltage feedback transforms them into the voltage-output mode. They cannot supply constant current loads without violating Kirchhoff's current law, as discussed in Ref. [12]. Therefore, the CMC converters are to be characterized by using resistive loading but the real internal dynamics shall be then revealed by computationally using the load-interaction formulas presented in Section 3.6.

The average and small-signal models presented in this chapter are always the real internal models. We derive and present the state spaces in general form first in DOT control domain. Thus, they are applicable for both fixed- and variable-frequency operations. In addition, the generalized modeling technique enables the modeling of converter dynamics when a part of the inductors is in DCM and a part of them in CCM. This kind of situation may take place in the higher order converters. The transfer functions are derived only for the fixed-frequency operation. The variable-frequency operation is treated more in detail in Section 4.4. The converters we treat in more detail are the basic converters – buck, boost, and buck–boost. As an example of the higher order converters, the superbuck or two-inductor buck converter is modeled as discrete-inductor and coupled-inductor implementations.

3.2 Direct-on-Time Control

The DOT control is the basic control method of the power electronic converters (cf. Figure 3.1), where the length of on-time is controlled to keep the associated output variable at the output or input terminal constant at the predefined level. In this chapter, the output variable is the output voltage but it can also be input current. As an example, the synchronous buck converter is shown in Figure 3.1, where the high-side switch S_{HS} conducts during the on-time (cf. Figure 3.1b, t_{on}), and the low-side switch S_{LS} during the off-time (cf. Figure 3.1b, t_{off}), respectively. This process is repeated in a sequential manner, that is, the operation is periodical. When the PWM switch is implemented by using MOSFETs as in Figure 3.1a, the operation of the converter is all the time in CCM due to the properties of the MOSFETs. If the low-side switch S_{LS} is substituted with a diode,

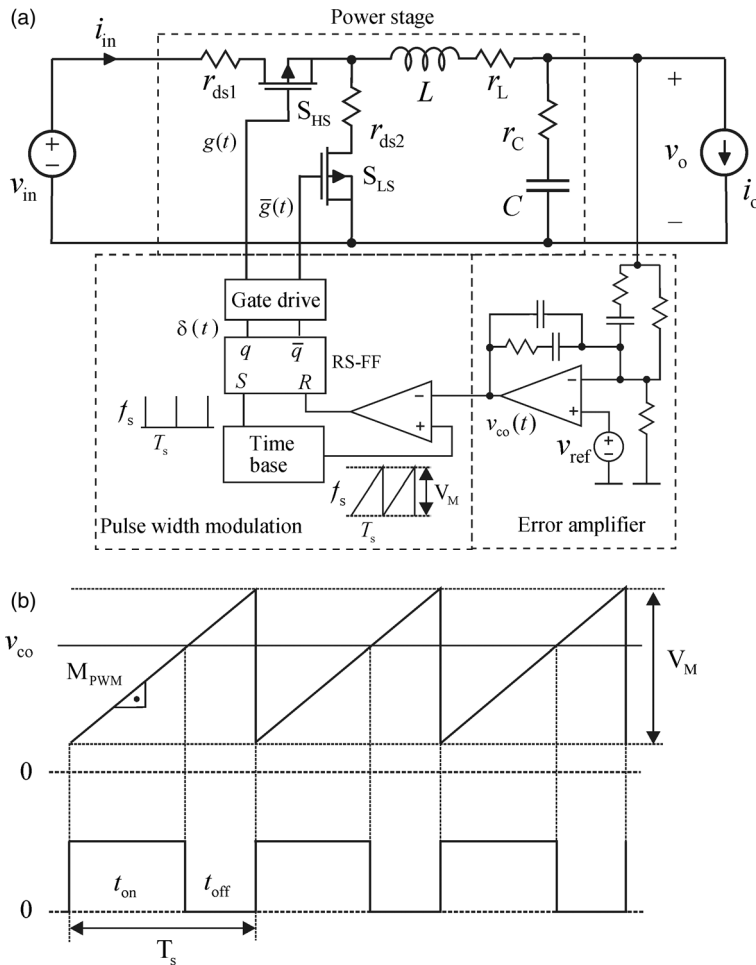


Figure 3.1 DDR-controlled synchronous buck converter. (a) Schematics. (b) Pulse-width generation.

where the anode is pointing up, the diode will be turned automatically off, when its current reaches the zero level leading to DCM operation. If the switching frequency f_s (cf. Figure 3.1a) is constant, then the DOT control equals the DDR control, where the duty ratio (d) can be expressed by t_{on}/T_s , and its complement ($d' = 1 - d$) by t_{off}/T_s . The inverse of the switching frequency (f_s) T_s (Figure 3.1b, $T_s = t_{on} + t_{off}$) is called cycle time.

The on-time or pulse width under fixed-frequency operation is implemented (cf. Figure 3.1b) by comparing the voltage provided by the controller (i.e., v_{co}) to a constant-slope PWM signal (i.e., $M_{PWM} = (V_M/T_s)t$) provided by the modulator. The gate pulse is switched on in the beginning of the cycle by means of the pace signal applied to the set input (S) of the RS flip-flop. The pace signal also determines the switching frequency (f_s). The gate pulse is terminated when the PWM ramp exceeds the control voltage (v_{co}) by turning the comparator output high and resetting the RS flip-flop. The flip-flop controls the gate drivers, which in turn provides the gate-control signals of the associated switches.

When considering the situation from the dynamic point of view, the slope of the PWM ramp would affect the gain (i.e., G_a , Figure 3.2) of the dynamic actions through the modulator. The gain is usually called *modulator gain*. It can be found by constructing the comparator equation (cf. Figure 3.1a), which determines the length of the on-time as follows:

$$v_{co} = \frac{V_M}{T_s} \cdot t_{on}, \tag{3.1}$$

and when developing the partial derivatives of (3.1) (i.e., linearizing), which yields

$$\hat{t}_{on} = \frac{T_s}{V_M} \cdot \hat{v}_{co}. \tag{3.2}$$

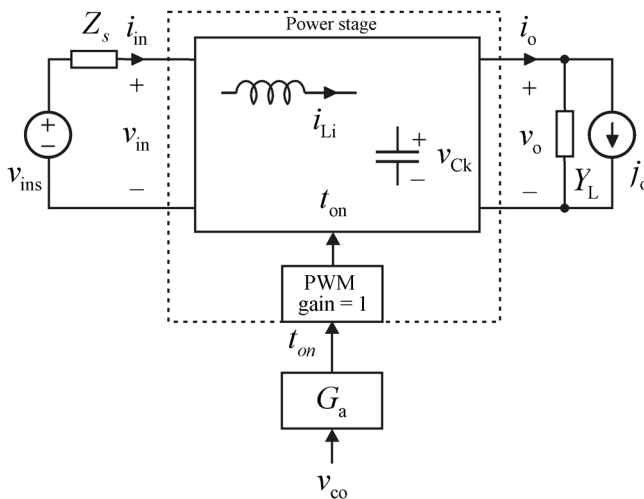


Figure 3.2 DOT-controlled converter at open loop with a PWM modulator.

Under the fixed-frequency operation, Eq. (3.2) becomes

$$\hat{d} = \frac{1}{V_M} \cdot \hat{v}_{co}, \quad (3.3)$$

and consequently, the modulator gain (G_a) equals V_M^{-1} . Due to the PWM process, the modulator gain may also contain some frequency-dependent components [10] in addition to the constant gain already defined.

When defining the dynamic models for the DOT-controlled converters in the subsequent sections, we assume that the modulator gain equals unity (1) as illustrated in Figure 3.2. The derived models are also the internal or unterminated models, that is, the source impedance (i.e., Z_s , Figure 3.2) and the load admittance (i.e., Y_L , Figure 3.2) are assumed to be infinite (i.e., impedance) and zero (i.e., admittance), respectively, when deriving the corresponding state spaces.

3.3 Generalized Modeling Technique

The power electronic converters are nonlinear variable structure systems, where different topological structures are periodically switched on and off. The non-linearity can be removed by averaging the converter operation within one switching cycle. Linearizing the obtained averaged model by developing the associated partial derivatives with respect to the state, input, and control variables at a certain operating point would yield the desired dynamic representation of the converter. It is obvious that the models are valid only up to the half of the switching frequency due to the nature of the averaging. In order to construct the averaged state space, we have to consider the variables as the time-varying averages of the corresponding instantaneous values x , which we denote by $\langle x \rangle$.

The behavior of time-averaged inductor current $\langle i_{Li} \rangle$ would determine most of the dynamics in a voltage-fed converter. The portion of the inductor current having positive up-slope (m_{1i}) and negative down-slope (m_{2i}) are shown in Figure 3.3 for an arbitrary switching cycle. The corresponding portions of the cycle time (t_s) are denoted by t_{on} and t_{off1} . It should be noted that $t_s = t_{on} + t_{off1}$ in CCM but $t_s > t_{on} + t_{off1}$ in DCM (cf. Figure 2.37; Section 2.4). The slopes m_{1i} and m_{2i} are the local averages within the on-time or off-time, respectively.

The time-averaged inductor current $\langle i_{Li} \rangle$ is a continuous signal of time regardless of the conduction mode (i.e., in CCM and DCM) but its charging

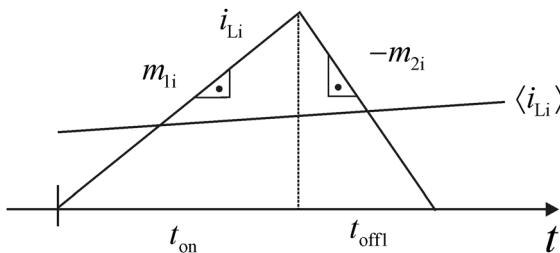


Figure 3.3 Waveforms of inductor current at an arbitrary switching cycle.

potential within those subcycles is distributed as

$$\begin{aligned}\langle i_{Li} \rangle_{\text{on}} &= \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}1}} \cdot \langle i_{Li} \rangle, \\ \langle i_{Li} \rangle_{\text{off}} &= \frac{t_{\text{off}1}}{t_{\text{on}} + t_{\text{off}1}} \cdot \langle i_{Li} \rangle.\end{aligned}\quad (3.4)$$

For developing the state space, the derivatives of the time-averaged state variables have to be defined. The derivative of time-averaged inductor current can be approximated according to the average slope of the instantaneous inductor current (cf. Figure 3.3) by

$$\frac{d\langle i_{Li} \rangle}{dt} = \frac{t_{\text{on}}}{t_s} \cdot m_{1i} - \frac{t_{\text{off}1}}{t_s} \cdot m_{2i}, \quad (3.5)$$

where $m_{1i} = \bar{v}_{\text{Li-on}}/L_i$ and $m_{2i} = -\bar{v}_{\text{Li-off}1}/L_i$ as well as $v_{\text{Li-on}}$ the voltage across the inductor during the on-time (t_{on}) and $v_{\text{Li-off}1}$ the voltage across the inductor during the part ($t_{\text{off}1}$) of the off-time (t_{off}) when the inductor current is nonzero. These relations may be obvious, because $v_L = L(di_L/dt)$. The bar over the voltages denotes the variables constituting the voltages that are the corresponding local averages during the corresponding subcycles.

The derivative of the time-averaged capacitor voltage can be approximated (cf. Figure 3.4) by

$$\frac{d\langle v_{Ck} \rangle}{dt} = \frac{\langle i_+ \rangle}{C_k} - \frac{\langle i_- \rangle}{C_k}, \quad (3.6)$$

where $\langle i_+ \rangle$ is the time-averaged current charging the capacitor, and $\langle i_- \rangle$ is the time-averaged current discharging the capacitor within a switching cycle, respectively. This relation is obvious, because $i_C = C(dv_C/dt)$ and $\langle i_C \rangle = \langle i_+ \rangle - \langle i_- \rangle$ according to *Kirchhoff's* current law.

The output of the converter is most often provided with an output capacitor as illustrated in Figure 3.5. Therefore, the average output voltage can be given by

$$\langle v_o \rangle = \langle v_{Ck} \rangle + r_{Ck} \langle i_+ \rangle - r_{Ck} \langle i_- \rangle, \quad (3.7)$$

or by

$$\langle v_o \rangle = \langle v_{Ck} \rangle + r_{Ck} C_k \frac{d\langle v_{Ck} \rangle}{dt}, \quad (3.8)$$

which is a useful form in the final state space for the output voltage.

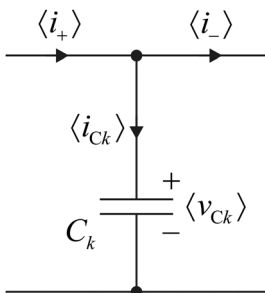


Figure 3.4 Capacitor charge balance.

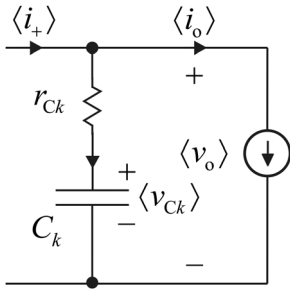


Figure 3.5 Converter output stage.

The time-varying averaged input current (i_{in}) is usually the current of a certain power-stage inductor or part of it. In the higher order converters, the input current can also be a sum of the power-stage inductor currents or a part of them. In all the cases, the value of time-varying averaged inductor current can be determined based on Eq. (3.4). The input (v_{in}) and output (v_o) voltages may affect the slopes of the inductor currents. In such cases, the input and output voltages have to be taken as their local averages over the corresponding subcycles when solving the slopes (m_{ij}). The usual error in modeling is to consider the variables as the averages over the whole switching cycle.

3.3.1 Buck Converter

The power stages of a buck or step-down converter with two different implementation principles – the diode (cf. Figure 3.6a) and synchronous (cf. Figure 3.6b) switched – are shown in Figure 3.6. In practice, the buck converter cannot work without an input capacitor because of its pulsating input current as shown in Figure 3.6c. In a buck converter, the input terminal voltage has to be higher than the output terminal voltage, and consequently, the input terminal current has to be lower than the output terminal current in order to maintain the power balance. The steady-state input-to-output modulo $M(D) = D$.

We perform the modeling for all the three power stages shown in Figure 3.6 differing from each other with respect to the implementation of the PWM switch scheme or the input capacitor. The use of diode in the PWM switch scheme means that the converter can operate either in CCM or DCM depending on the level of output current. The use of MOSFETs means that the converter operates only in CCM without any special control arrangements down to the no load. The internal parasitic resistances (i.e., r_{dsi} and r_d) in the associated switches also include the switching losses. As shown in Figure 3.6, the high-side switch conducts during the on-time, and the low-side switch during the off-time or a part of the off-time.

According to the generalized method, we divide the switching cycle into two subcycles: During the on-time (cf. Figure 3.7a), the topological structures are exactly the same. During the off-time1 (i.e., during the part of the off-time when the inductor current slope is negative), the topological structures differ only in terms of the losses (cf. Figure 3.7b and c). We have not added the input capacitor

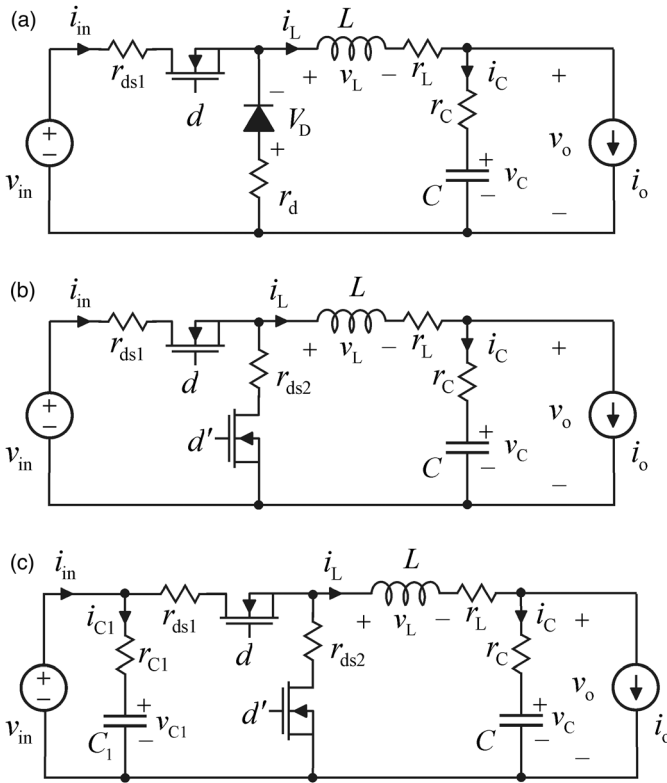


Figure 3.6 Buck-converter power stages. (a) Diode switching. (b) Synchronous switching. (c) With an input capacitor.

C_1 into Figure 3.7 but we take its effect, however, into account in the generalized state space.

According to Figure 3.7, we may conclude that the current $\langle i_+ \rangle$ charging the output capacitor equals the time-averaged inductor current $\langle i_L \rangle$ because the inductor current charges the output capacitor during both of the subcycles. For the same reason, the local average of the output voltage during the on-time and off-time¹ can be given by

$$\bar{v}_{o\text{-on/off}} = r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle. \quad (3.9)$$

The time-averaged input current $\langle i_{in} \rangle$ equals the on-time inductor current, and therefore, the first equation in (3.4) applies. The contribution of the input capacitor can be taken into account as follows:

$$\frac{d\langle v_{C1} \rangle}{dt} = \frac{-v_{C1} + v_{in}}{r_{C1} C_1}, \quad (3.10)$$

because $i_{C1} = (v_{in} - v_{C1})/r_{C1}$. It may be obvious that the contribution of an ideal input capacitor cannot be taken into account as presented here because of infinite input capacitor current, which indicates that the derivative of the capacitor is not

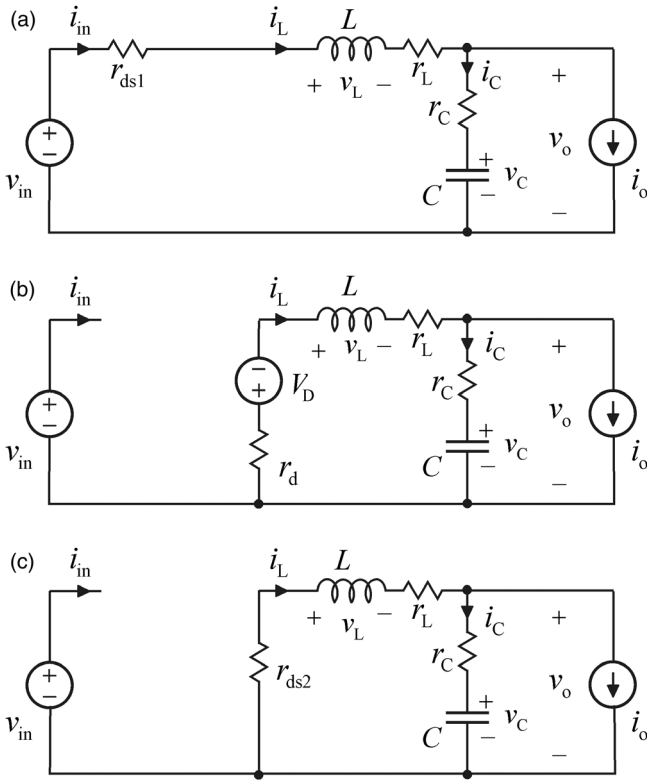


Figure 3.7 The topological subcircuit structures of a buck converter during the (a) on-time and off-time1 with (b) diode-switching and (c) synchronous-switching schemes.

independent but perfectly dependent on the input voltage. In such a case, other methods have to be considered. We come up to this problem later when deriving the system transfer functions.

According to these conclusions and applying Eqs. (3.4–3.10), the general state space with the input capacitor can be given for the buck converter by

$$\begin{aligned}
 \frac{d\langle i_L \rangle}{dt} &= \frac{t_{\text{on}}}{t_s} \cdot m_1 - \frac{t_{\text{off1}}}{t_s} \cdot m_2, \\
 \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\
 \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{\langle v_{C1} \rangle}{r_{C1}C_1} + \frac{\langle v_{in} \rangle}{r_{C1}C_1}, \\
 \langle i_{in} \rangle &= \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off1}}} \cdot \langle i_L \rangle, \\
 \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt},
 \end{aligned} \tag{3.11}$$

where the up-slope

$$m_1 = \frac{\langle v_{in} \rangle - (r_L + r_{ds1} + r_C)\langle i_L \rangle - \langle v_C \rangle + r_C\langle i_o \rangle}{L}, \quad (3.12)$$

the down-slope of the diode-switched scheme

$$m_2 = \frac{(r_L + r_d + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle + V_D}{L}, \quad (3.13)$$

and the down-slope of the synchronous-switched scheme

$$m_2 = \frac{(r_L + r_{ds2} + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle}{L}. \quad (3.14)$$

If the input capacitor is not to be considered, the corresponding derivative shall be removed from the state space.

3.3.2 Boost Converter

The power stages of a boost or step-up converter with two different implementation principles – the diode (cf. Figure 3.8a) and synchronous (cf. Figure 3.8b)

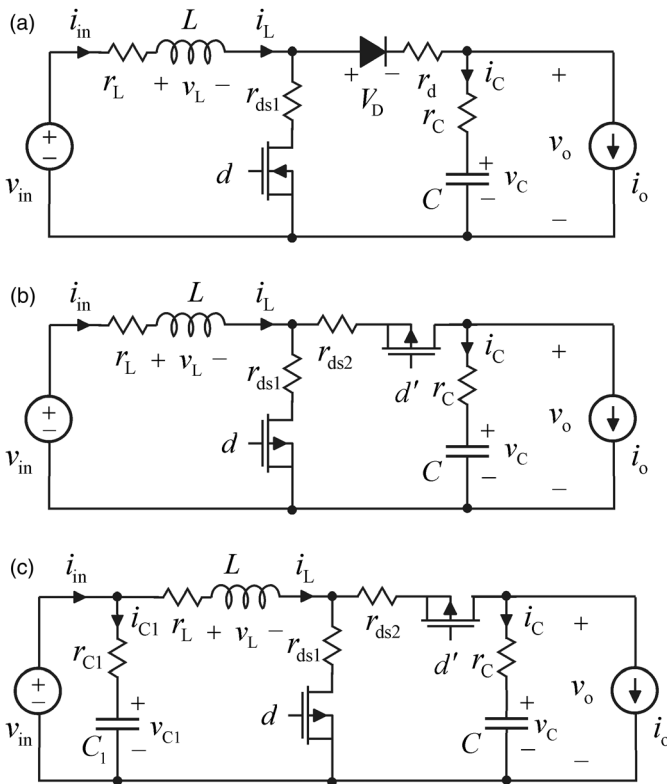


Figure 3.8 Boost-converter power stages. (a) Diode switching. (b) Synchronous switching. (c) With an input capacitor.

switched – are shown in Figure 3.8. In practice, the boost converter can work without an input capacitor because of its continuous input current but we consider also the case, where the input capacitor is connected at the input terminal as shown in Figure 3.8c. In a boost converter, the input terminal voltage has to be lower than the output terminal voltage, and consequently, the input terminal current has to be higher than the output terminal current in order to maintain the power balance. The steady-state input-to-output modulo $M(D) = 1/D'$.

Similarly as in the case of the buck converter in Section 3.3.1, we perform the modeling for all the power stages shown in Figure 3.8. Under the synchronous-switching scheme, the converter operates all the time in CCM. Under the diode-switching scheme, the converter operates both in CCM and DCM depending on the level of the output current and the input voltage. The parasitic resistances (i.e., r_{dsi} and r_d) of the associated switching components also include the switching losses. As indicated in Figure 3.8, the low-side switch conducts during the on-time and the high-side switch during the off-time or a part of the off-time.

According to the generalized method, we divide the switching cycle into two subcycles: During the on-time (cf. Figure 3.9a), the topological structures are exactly the same. During the off1-time (i.e., during the part of the off-time when the inductor current slope is negative), the topological structures differ only in terms of the losses (cf. Figure 3.9b and c). We have not added the input capacitor C_1 into Figure 3.9, but we take its effect, however, into account in the generalized state space.

According to Figure 3.8, we may conclude that the current $\langle i_+ \rangle$ charging the output capacitor equals the time-averaged off-time inductor current $\langle i_L \rangle_{\text{off}}$ defined in the last equation of Eq. (3.4), because the inductor current charges the output capacitor during the off-time only. For the same reason, the local average of the output voltage during the on-time and off-time1 can be given by

$$\begin{aligned}\bar{v}_{\text{o-on}} &= \langle v_C \rangle - r_C \langle i_o \rangle, \\ \bar{v}_{\text{o-off}} &= r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle.\end{aligned}\quad (3.15)$$

The time-averaged input current $\langle i_{\text{in}} \rangle$ equals the on-time inductor current $\langle i_L \rangle_{\text{on}}$ given as the first equation in (3.4). The contribution of the input capacitor can be taken into account as presented in Section 3.3.2 (Eq. (3.10)).

According to these conclusions and applying Eqs (3.4–3.8), (3.10), and (3.15), the general state space with the input capacitor can be given for the buck converter by

$$\begin{aligned}\frac{d\langle i_L \rangle}{dt} &= \frac{t_{\text{on}}}{t_s} \cdot m_1 - \frac{t_{\text{off1}}}{t_s} \cdot m_2, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{t_{\text{off1}}}{t_{\text{on}} + t_{\text{off1}}} \cdot \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\ \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{\langle v_{C1} \rangle}{r_{C1}C} - \frac{\langle v_{\text{in}} \rangle}{r_{C1}C}, \\ \langle i_{\text{in}} \rangle &= \langle i_L \rangle, \\ \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt},\end{aligned}\quad (3.16)$$

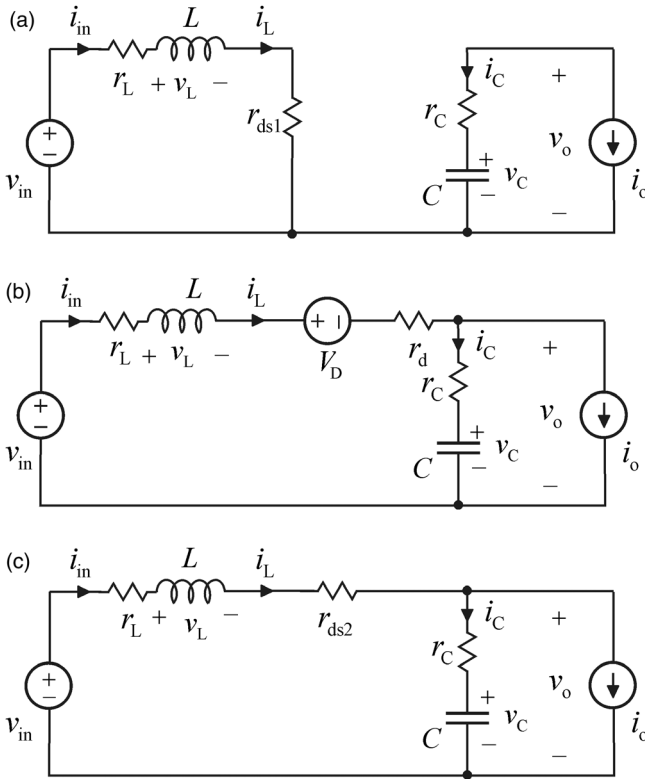


Figure 3.9 The topological subcircuit structures of a boost converter during the (a) on-time and off-time1 with (b) diode-switching and (c) synchronous-switching schemes.

where the up-slope

$$m_1 = \frac{\langle v_{in} \rangle - (r_L + r_{ds1})\langle i_L \rangle}{L}, \quad (3.17)$$

the down-slope of the diode switching converter

$$m_2 = \frac{(r_L + r_d + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle + V_D - \langle v_{in} \rangle}{L}, \quad (3.18)$$

and the down-slope of the synchronous switching converter

$$m_2 = \frac{(r_L + r_{ds2} + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle - \langle v_{in} \rangle}{L}. \quad (3.19)$$

3.3.3 Buck-Boost Converter

The power stages of a buck–boost or step-up/down converter with three different implementation principles – the diode (cf. Figure 3.10a) and synchronous (cf. Figure 3.10b) switched and its noninverting version (cf. Figure 3.10c) – are shown in Figure 3.10. It should be noted that the polarity of the output voltage in the

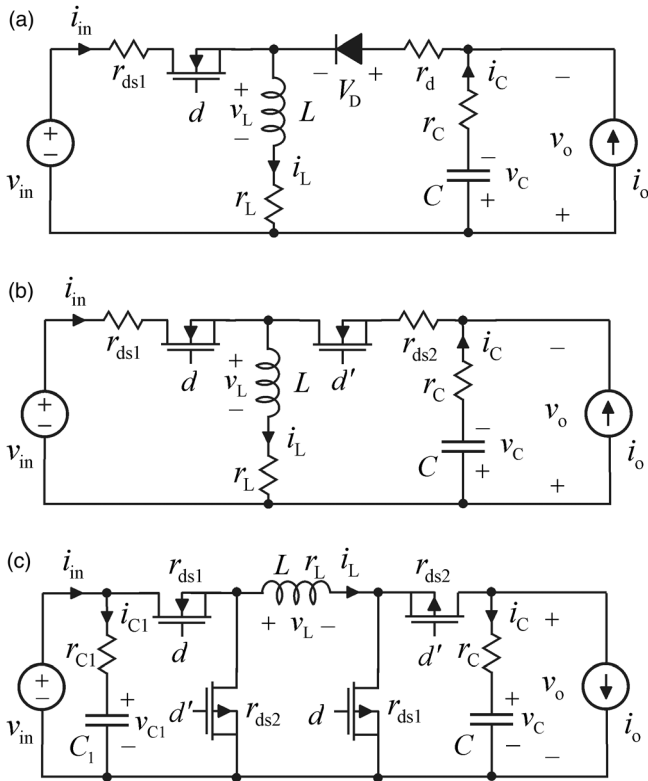


Figure 3.10 Buck–Boost power stages. (a) Inverting converter with diode switching. (b) Inverting converter with synchronous switching. (c) Noninverting converter with synchronous-switching and with an input capacitor.

inverting buck–boost converter (cf. Figure 3.10a and b) is considered in the schematics. Therefore, there will not appear a minus sign in the converter input-to-output modulo $M(D) = D/D'$. In practice, the buck–boost converter cannot work properly without an input capacitor because of its pulsating input current as shown in Figure 3.10c. In a buck–boost converter, the levels of terminal voltages and currents are not constrained similarly as in the buck and boost converters but they can be higher or lower in respect to each other depending on the operating point.

Similarly as in the case of the buck converter in Section 3.3.1, we perform the modeling for all the power stages shown in Figure 3.10. Under the synchronous-switching scheme, the converter operates all the time in CCM. Under the diode-switching scheme, the converter operates both in CCM and DCM depending on the level of the output current and the input voltage. The parasitic resistances (i.e., r_{dsi} and r_d) of the associated switching components also include the switching losses. As indicated in Figure 3.10a and b, the left high-side switch conducts during the on-time and the right high-side switch during the off-time or a part of the off-time. In the noninverting converter, the left high-side switch and the

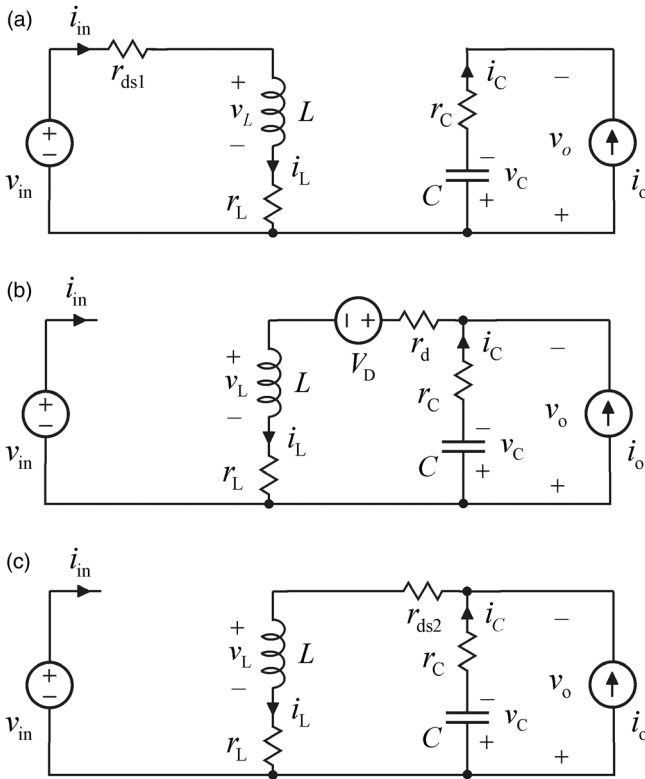


Figure 3.11 The topological subcircuit structures of an inverting buck–boost converter during the (a) on-time and off-time1 with (b) diode-switching, and (c) synchronous-switching schemes.

right-low side switch conduct during the on-time and the right high-side switch and the left low-side switch conduct during the off-time or a part of off-time as indicated in Figure 3.10c.

According to the generalized method, we divide the switching cycle into two subcycles: During the on-time (cf. Figure 3.11a), the topological structures of the inverting converter are exactly the same in the inverting converter. During the off1-time (i.e., during the part of the off-time when the inductor current slope is negative), the topological structures differ only in terms of the losses (cf. Figure 3.11b and c). The topological structures of the noninverting converter are shown during the on-time in Figure 3.12a, and during the off-time in Figure 3.12b, respectively. We have not added the input capacitor C_1 into Figures 3.11 and 3.12, but we take its effect, however, into account in the generalized state space.

According to Figure 3.10, we may conclude that the current $\langle i_+ \rangle$ charging the output capacitor equals the time-averaged off-time inductor current $\langle i_L \rangle_{off}$ defined in the last equation of Eq. (3.4), because the inductor current charges the output capacitor during the off-time only. For the same reason, the

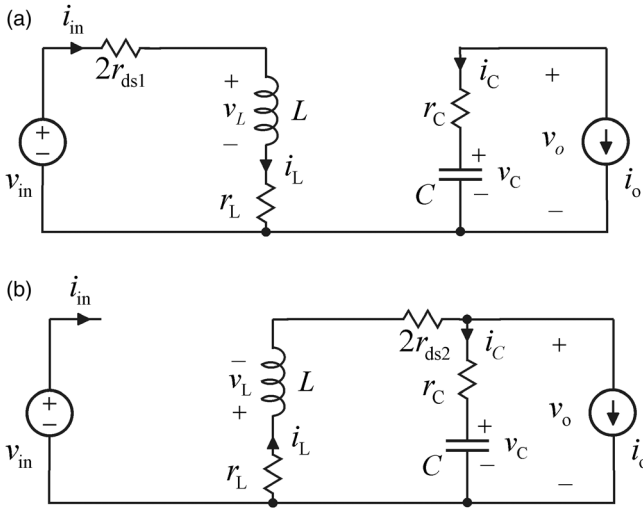


Figure 3.12 The topological subcircuit structures of a noninverting buck-boost converter during the (a) on-time and (b) off-time1 with the synchronous-switching scheme.

local average of the output voltage during the on-time and off-time1 can be given by

$$\begin{aligned}\bar{v}_{o\text{-on}} &= \langle v_C \rangle - r_C \langle i_o \rangle, \\ \bar{v}_{o\text{-off}} &= r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle.\end{aligned}\quad (3.20)$$

The time-averaged input current $\langle i_{in} \rangle$ equals the inductor current $\langle i_L \rangle$. The contribution of the input capacitor can be taken into account as presented in Section 3.3.2 (Eq. (3.10)). According to these conclusions and applying Eqs (3.4–3.8), (3.10), and (3.20), the general state space with the input capacitor can be given for the buck-boost converter by

$$\begin{aligned}\frac{d\langle i_L \rangle}{dt} &= \frac{t_{on}}{t_s} \cdot m_1 - \frac{t_{off1}}{t_s} \cdot m_2, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{t_{off1}}{t_{on} + t_{off1}} \cdot \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\ \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{\langle v_{C1} \rangle}{r_{C1} C_1} + \frac{\langle v_{in} \rangle}{r_{C1} C}, \\ \langle i_{in} \rangle &= \frac{t_{on}}{t_{on} + t_{off1}} \cdot \langle i_L \rangle, \\ \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt},\end{aligned}\quad (3.21)$$

where the up-slope of the inverting converter can be given by

$$m_1 = \frac{\langle v_{in} \rangle - (r_L + r_{ds1}) \langle i_L \rangle}{L}, \quad (3.22)$$

the up-slope of the noninverting converter by

$$m_1 = \frac{\langle v_{in} \rangle - (r_L + 2r_{ds1})\langle i_L \rangle}{L}, \quad (3.23)$$

as well as the down-slope of the inverting converter with diode switching scheme by

$$m_2 = \frac{(r_L + r_d + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle + V_D}{L}, \quad (3.24)$$

the down-slope of the inverting converter with synchronous switching scheme by

$$m_2 = \frac{(r_L + r_{ds2} + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle}{L}, \quad (3.25)$$

and the down-slope of the noninverting converter by

$$m_2 = \frac{(r_L + 2r_{ds2} + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle}{L}. \quad (3.26)$$

3.3.4 Superbuck Converter

The buck converter known as superbuck [13], current-sourced buck [14], and two-inductor buck [15] converter is a fourth-order buck-type converter (cf. Figure 3.13), where the input current is also continuous in contrast to the pulsating input current of the conventional second-order buck converter. This feature makes the superbuck converter to be very suitable to interfacing, for instance, the photovoltaic generator into the rest of the power system [16]. The power stage of the converter is shown in Figure 3.13, where the resistive losses (i.e., r_{ds} and r_d) assigned to the power-stage switching components also include the switching losses. The diode in the power stage could be replaced by a MOSFET, which would make the converter to operate all the time in CCM. According to the modeling of the basic converters, the state space of such a power stage can be easily derived from the state space of the diode-switched converter by considering the resistive and voltage losses carefully. The steady-state input-to-output modulo of the converter $M(D) = D$.

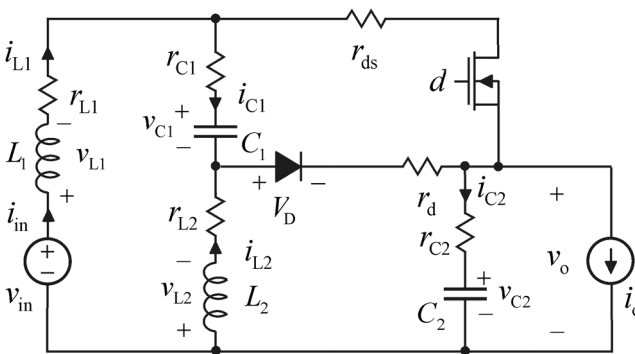


Figure 3.13 Superbuck converter.

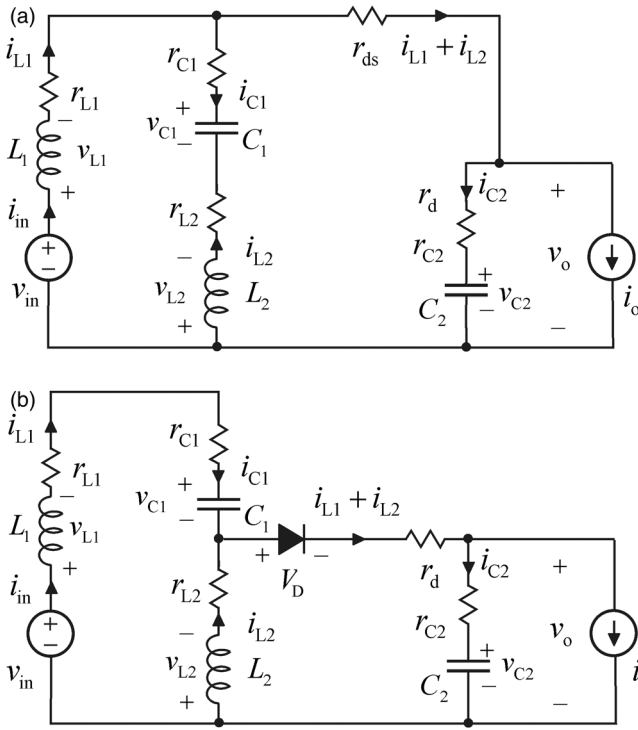


Figure 3.14 Superbuck topological structures during the (a) on-time and (b) off-time.

According to the generalized modeling method, we divide the switching cycle into two subcycles: During the on-time, the MOSFET conducts and the topological circuit structure is as shown in Figure 3.14a. During the off-time or during a part of the off-time when the inductor current slopes are negative, the diode conducts and the topological circuit structure is as shown in Figure 3.14b.

According to Figure 3.14, we may conclude that the current $\langle i_+ \rangle$ charging the output capacitor C_2 equals the sum of the time-averaged inductor currents $\langle i_{L1} \rangle$ and $\langle i_{L2} \rangle$, because they charge the output capacitor during the on-time and off-time. The current $\langle i_+ \rangle$ charging the capacitor C_1 is the off-time inductor current $\langle i_{L1} \rangle_{\text{off}}$ defined in the last equation of Eq. (3.4). The current $\langle i_- \rangle$ discharging the output capacitor is naturally the time-averaged output current $\langle i_o \rangle$. The current $\langle i_- \rangle$ discharging the capacitor C_1 is the on-time inductor current $\langle i_{L1} \rangle_{\text{on}}$ defined in the first equation of Eq. (3.4). Because of continuous supply of inductor currents into the output capacitor, the local averages of the output voltage during the on-time and off-time1 can be given by

$$\bar{v}_{o\text{-on,off}} = r_{C2} \langle i_{L1} \rangle + r_{C2} \langle i_{L2} \rangle + v_{C2} - r_{C2} \langle i_o \rangle. \quad (3.27)$$

According to Figure 3.13, the time-averaged input current $\langle i_{in} \rangle$ equals the inductor current $\langle i_{L1} \rangle$. The contribution of the input capacitor C_3 can be taken into account as presented in Section 3.3.2 (Eq. (3.10)).

According to these conclusions and applying Eqs. (3.4–3.8), (3.10), and (3.27), the general state space can be given by

$$\begin{aligned}
\frac{d\langle i_{L1} \rangle}{dt} &= \frac{t_{\text{on}}}{t_s} \cdot m_{11} - \frac{t_{\text{off1}}}{t_s} \cdot m_{12}, \\
\frac{d\langle i_{L2} \rangle}{dt} &= \frac{t_{\text{on}}}{t_s} \cdot m_{21} - \frac{t_{\text{off1}}}{t_s} \cdot m_{22}, \\
\frac{d\langle v_{C1} \rangle}{dt} &= \frac{t_{\text{off1}}}{t_{\text{on}} + t_{\text{off1}}} \cdot \frac{\langle i_{L1} \rangle}{C_1} - \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off1}}} \cdot \frac{\langle i_{L2} \rangle}{C_1}, \\
\frac{d\langle v_{C2} \rangle}{dt} &= \frac{\langle i_{L1} \rangle}{C_2} + \frac{\langle i_{L2} \rangle}{C_2} - \frac{\langle i_o \rangle}{C_2}, \\
\frac{d\langle v_{C3} \rangle}{dt} &= -\frac{\langle v_{C3} \rangle}{r_{C3}C_3} + \frac{\langle v_{\text{in}} \rangle}{r_{C3}C_3}, \\
\langle i_{\text{in}} \rangle &= \langle i_L \rangle, \\
\langle v_o \rangle &= \langle v_{C2} \rangle + r_{C2}C_2 \frac{d\langle v_{C2} \rangle}{dt},
\end{aligned} \tag{3.28}$$

where the up-slopes

$$\begin{aligned}
m_{11} &= \frac{-(r_{L1} + r_{\text{ds}} + r_{C2})\langle i_{L1} \rangle - (r_{\text{ds}} + r_{C2})\langle i_{L2} \rangle - v_{C2} + v_{\text{in}} + r_{C2}\langle i_o \rangle}{L_1}, \\
m_{21} &= \frac{-(r_{\text{ds}} + r_{C2})\langle i_{L1} \rangle - (r_{L2} + r_{\text{ds}} + r_{C1} + r_{C2})\langle i_{L2} \rangle + v_{C1} - v_{C2} + r_{C2}\langle i_o \rangle}{L_2},
\end{aligned} \tag{3.29}$$

and the down-slopes

$$\begin{aligned}
m_{12} &= \frac{(r_{L1} + r_d + r_{C1} + r_{C2})\langle i_{L1} \rangle + (r_d + r_{C2})\langle i_{L2} \rangle + \langle v_{C1} \rangle + \langle v_{C2} \rangle - v_{\text{in}} - r_{C2}\langle i_o \rangle + V_D}{L_1}, \\
m_{22} &= \frac{(r_d + r_{C2})\langle i_{L1} \rangle + (r_{L2} + r_d + r_{C2})\langle i_{L2} \rangle + \langle v_{C2} \rangle - r_{C2}\langle i_o \rangle + V_D}{L_2}.
\end{aligned} \tag{3.30}$$

As stated earlier, the state space in (3.28) enables the modeling of the converter dynamics also in an operation mode, where one of the inductors operates in CCM and the other in DCM. The possibility to perform the dynamic modeling in a mixed conduction mode indicates the powerfulness and flexibility incorporated in the introduced generalized modeling method in addition that it also harmonizes the CCM and DCM modeling.

3.4 Fixed-Frequency Operation in CCM

The method to perform the average modeling and to obtain the linearized state space is described in Chapter 2 with a detailed example based on a buck converter. In this section, we provide the averaged and linearized state spaces as well as the definition of the operation points and the corresponding transfer

functions for the converters treated in Section 3.3. The detailed modeling is left for the reader. In addition to the basic transfer functions, we also derive the set of special transfer functions based on the generalized special transfer functions derived in Section 2.2. The set of basic transfer functions forms the G-parameter representation of the converter dynamics, where the input variables are the input voltage (v_{in}) and output current (i_o), the output variables the input current (i_{in}) and output voltage (v_o), the state variables the inductor currents (i_{Li}) and capacitor voltages (v_{Ci}), and the control variable is the duty ratio (d). The set of the transfer functions given in this section is

$$\begin{bmatrix} \hat{i}_{in} \\ v_o \end{bmatrix} = \begin{bmatrix} Y_{in} & T_{oi} & G_{ci} \\ G_{io} & -Z_o & G_{co} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}, \quad (3.31)$$

and the special transfer functions

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ Z_{o-oci} & Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} Y_{in} + \frac{G_{io}T_{oi}}{Z_o} & Y_{in} - \frac{G_{io}G_{ci}}{G_{co}} & T_{oi} + \frac{Z_oG_{ci}}{G_{co}} \\ Z_o + \frac{G_{io}T_{oi}}{Y_{in}} & Z_o + \frac{T_{oi}G_{co}}{G_{ci}} & G_{io} - \frac{Y_{in}G_{co}}{G_{ci}} \end{bmatrix}. \quad (3.32)$$

The special transfer functions denoted by $G_{xy-\infty}$ in Eq. (3.32) determine either the low-frequency value of the corresponding closed-loop transfer function (cf. Sections 2.2.3 and 2.2.4) or the source and load interactions (cf. Section 2.2.5). The other two special transfer functions in Eq. (3.32) determine the source and load interactions propagating through the converter (cf. Section 2.2.5).

3.4.1 Buck Converter

The averaged state space of the diode-switched buck converter (cf. Figure 3.6a) is given in Eq. (3.33) and the averaged state space of the synchronous-switched converter (cf. Figure 3.6b) in Eq. (3.35). The corresponding operation points are given in Eqs. (3.34) and (3.36), respectively.

$$\begin{aligned} \frac{d\langle i_L \rangle}{dt} &= -\frac{r_L + dr_{ds1} + d'r_d + r_C}{L} \langle i_L \rangle - \frac{1}{L} \langle v_C \rangle + \frac{d}{L} \langle v_{in} \rangle + \frac{r_C}{L} \langle i_o \rangle - \frac{d'V_D}{L}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\ \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_{in} \rangle, \\ \langle i_{in} \rangle &= d\langle i_L \rangle - \frac{1}{r_{C1}} \langle v_{C1} \rangle + \frac{1}{r_{C1}} \langle v_{in} \rangle, \\ \langle v_o \rangle &= r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle = \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}. \end{aligned} \quad (3.33)$$

$$\begin{aligned}
I_L &= I_o, \\
I_{in} &= DI_o, \\
V_o &= V_C, \\
V_o &= DV_{in} - D'V_D - (r_L + Dr_{ds1} + D'r_d)I_o, \\
D &= \frac{V_o + V_D + (r_L + r_d)I_o}{V_{in} + V_D + (r_d - r_{ds1})I_o}.
\end{aligned} \tag{3.34}$$

$$\begin{aligned}
\frac{d\langle i_L \rangle}{dt} &= -\frac{r_L + dr_{ds1} + d'r_{ds2} + r_C}{L} \langle i_L \rangle - \frac{1}{L} \langle v_C \rangle + \frac{d}{L} \langle v_{in} \rangle + \frac{r_C}{L} \langle i_o \rangle, \\
\frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\
\frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_{in} \rangle, \\
\langle i_{in} \rangle &= d\langle i_L \rangle - \frac{1}{r_{C1}} \langle v_{C1} \rangle + \frac{1}{r_{C1}} \langle v_{in} \rangle, \\
\langle v_o \rangle &= r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle = \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.
\end{aligned} \tag{3.35}$$

$$\begin{aligned}
I_L &= I_o, \\
I_{in} &= DI_o, \\
V_o &= V_C, \\
V_o &= DV_{in} - (r_L + Dr_{ds1} + D'r_{ds2})I_o, \\
D &= \frac{V_o + (r_L + r_{ds2})I_o}{V_{in} + (r_{ds2} - r_{ds1})I_o}.
\end{aligned} \tag{3.36}$$

The linearized state space for both of the converters is given in Eq. (3.37):

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} &= -\frac{r_e}{L} \hat{i}_L - \frac{1}{L} \hat{v}_C + \frac{D}{L} \hat{v}_{in} + \frac{r_C}{L} \hat{i}_o + \frac{V_e}{L} \hat{d}, \\
\frac{d\hat{v}_C}{dt} &= \frac{\hat{i}_L}{C} - \frac{\hat{i}_o}{C}, \\
\frac{d\hat{v}_{C1}}{dt} &= -\frac{\hat{v}_{C1}}{r_{C1}C_1} + \frac{\hat{v}_{in}}{r_{C1}C_1}, \\
\hat{i}_{in} &= D\hat{i}_L - \frac{\hat{v}_{C1}}{r_{C1}} + \frac{\hat{v}_{in}}{r_{C1}} + I_o \hat{d}, \\
\hat{v}_o &= \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt},
\end{aligned} \tag{3.37}$$

where r_e and V_e are for the diode-switched buck converter:

$$\begin{aligned}
r_e &= r_L + Dr_{ds1} + D'r_d + r_C, \\
V_e &= V_{in} + V_D + (r_d - r_{ds1})I_o,
\end{aligned} \tag{3.38}$$

and for the synchronous-switched buck converter

$$\begin{aligned} r_e &= r_L + Dr_{ds1} + D'r_{ds2} + r_C, \\ V_e &= V_{in} + (r_{ds2} - r_{ds1})I_o. \end{aligned} \quad (3.39)$$

The transfer functions corresponding to Eq. (3.31) can be derived from Eq. (3.37) by transforming the state space into Laplace domain and applying linear algebra (cf. Section 2.4), which yields

$$\begin{bmatrix} \hat{i}_{in} \\ v_o \end{bmatrix} = \left(\begin{bmatrix} \frac{D^2s}{L} & \frac{D(1+sr_C C)}{LC} & \frac{DV_e s}{L} + \left(s^2 + s\frac{r_e}{L} + \frac{1}{LC}\right)I_o \\ \frac{D(1+sr_C C)}{LC} & -\frac{(r_e - r_C + sL)(1+sr_C C)}{LC} & \frac{V_e(1+sr_C C)}{LC} \end{bmatrix} \bigg/ \left[s^2 + s\frac{r_e}{L} + \frac{1}{LC} \right] \right) * \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}. \quad (3.40)$$

The special transfer functions can be computed based on Eq. (3.40) and applying Eq. (3.32), which yields

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ Z_{o-oci}^o & Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} \frac{D^2}{sL + r_e - r_C} & -\frac{DI_o}{V_e} & D + \frac{I_o L}{V_e} \left(s + \frac{r_e - r_C}{L} \right) \\ \frac{1 + sr_C C}{sC} & \frac{(sL + r_e - r_C + (DV_e/I_o))(1 + sr_C C)}{LC(s^2 + s(r_e/L) + (DV_e/I_oL) + (1/LC))} & \frac{D(1 + sr_C C)}{LC(s^2 + s(r_e/L) + (DV_e/LI_o) + (1/LC))} \end{bmatrix}. \quad (3.41)$$

The special output impedance Z_{o-oci} is dependent on the state of output-voltage feedback. Its open-loop value is given in Eq. (3.41). In general, its value can be given by [17]

$$Z_{o-oci}^x = \frac{Z_{o-x}}{Y_{in-x}} Y_{in-sco}, \quad (3.42)$$

where the superscript and subscript extension x denotes either the open-“o” or closed-“c” loop transfer function. The short circuit input admittance (Y_{in-sco}) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.41).

The effect of the input capacitor C_1 (cf. Figure 3.6c) can be taken into account in such a manner that it is actually in parallel with the impedances measured from the input terminal without the input capacitor. It has no other effects on the dynamics of the converter. As a consequence,

$$\begin{aligned} Y_{in-x}^{C_1} &= Y_{in-x} + \frac{sC_1}{1 + sr_{C1}C_1}, \\ Y_{in-sco}^{C_1} &= Y_{in-sco} + \frac{sC_1}{1 + sr_{C1}C_1}, \end{aligned} \quad (3.43)$$

where the subscript x means open- “o” or closed- “c” loop transfer function, respectively.

According to the denominator of the transfer functions in Eq. (3.40) and the resonant nature of the converter, natural frequency (ω_n), resonant or damped natural frequency (ω_d), damping factor (ζ), and quality factor (Q) can be given by (cf. Section 2.5.2)

$$\omega_n = \frac{1}{\sqrt{LC}}, \quad \omega_d = \frac{1}{\sqrt{LC}} \sqrt{1 - \left(\frac{r_e}{2} \sqrt{\frac{C}{L}}\right)^2}, \quad \zeta = \frac{r_e}{2} \sqrt{\frac{C}{L}}, \quad Q = \frac{1}{r_e} \sqrt{\frac{L}{C}}, \quad (3.44)$$

where $\sqrt{L/C}$ is known as the characteristic impedance (Z_o) of resonant circuit.

3.4.2 Boost Converter

The averaged state space of the diode-switched boost converter (cf. Figure 3.8a) is given in Eq. (3.45) and the averaged state space of the synchronous-switched converter (cf. Figure 3.8b) in Eq. (3.47). The corresponding operation points are given in Eqs (3.46) and (3.48), respectively.

$$\begin{aligned} \frac{d\langle i_L \rangle}{dt} &= -\frac{r_L + dr_{ds1} + d'r_d + d'r_C}{L} \langle i_L \rangle - \frac{d'}{L} \langle v_C \rangle + \frac{1}{L} \langle v_{in} \rangle + \frac{d'r_C}{L} \langle i_o \rangle - \frac{d'V_D}{L}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{d'}{C} \langle i_L \rangle - \frac{1}{C} \langle i_o \rangle, \\ \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_{in} \rangle, \\ \langle i_{in} \rangle &= \langle i_L \rangle - \frac{1}{r_{C1}} \langle v_{C1} \rangle + \frac{1}{r_{C1}} \langle v_{in} \rangle, \\ \langle v_o \rangle &= d'r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle = \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}. \end{aligned} \quad (3.45)$$

$$I_L = \frac{I_o}{D'},$$

$$I_{in} = I_L,$$

$$V_o = V_C, \quad (3.46)$$

$$V_o = \frac{V_{in} - D'V_D}{D'} - \frac{r_L + Dr_{ds1} + D'r_d + DD'r_C}{D'^2} \cdot I_o,$$

$$(V_o + V_D - r_C I_o)D'^2 - (V_{in} - (r_d - r_{ds1} + r_C)I_o)D' + (r_L + r_{ds1})I_o = 0.$$

$$\begin{aligned}
\frac{d\langle i_L \rangle}{dt} &= -\frac{r_L + dr_{ds1} + d'r_{ds2} + d'r_C}{L} \langle i_L \rangle - \frac{d'}{L} \langle v_C \rangle + \frac{1}{L} \langle v_{in} \rangle + \frac{d'r_C}{L} \langle i_o \rangle, \\
\frac{d\langle v_C \rangle}{dt} &= \frac{d'}{C} \langle i_L \rangle - \frac{1}{C} \langle i_o \rangle, \\
\frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_{in} \rangle, \\
\langle i_{in} \rangle &= \langle i_L \rangle - \frac{1}{r_{C1}} \langle v_{C1} \rangle + \frac{1}{r_{C1}} \langle v_{in} \rangle, \\
\langle v_o \rangle &= d'r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle = \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.
\end{aligned} \tag{3.47}$$

$$\begin{aligned}
I_L &= \frac{I_o}{D'}, \\
I_{in} &= I_L, \\
V_o &= V_C, \\
V_o &= \frac{V_{in}}{D'} - \frac{r_L + Dr_{ds1} + D'r_{ds2} + DD'r_C}{D'^2} \cdot I_o, \\
(V_o - r_C I_o) D'^2 - (V_{in} - (r_{ds2} - r_{ds1} + r_C) I_o) D' + (r_L + r_{ds1}) I_o &= 0.
\end{aligned} \tag{3.48}$$

The linearized state space for both of the converters is given in Eq. (3.49):

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} &= -\frac{r_e}{L} \hat{i}_L - \frac{D'}{L} \hat{v}_C + \frac{1}{L} \hat{v}_{in} + \frac{D'r_C}{L} \hat{i}_o + \frac{V_e}{L} \hat{d}, \\
\frac{d\hat{v}_C}{dt} &= \frac{D'\hat{i}_L}{C} - \frac{\hat{i}_o}{C} - \frac{I_L}{C} \hat{d}, \\
\frac{d\hat{v}_{C1}}{dt} &= -\frac{\hat{v}_{C1}}{r_{C1}C_1} + \frac{\hat{v}_{in}}{r_{C1}C_1}, \\
\hat{i}_{in} &= \hat{i}_L - \frac{\hat{v}_{C1}}{r_{C1}} + \frac{\hat{v}_{in}}{r_{C1}}, \\
\hat{v}_o &= \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt},
\end{aligned} \tag{3.49}$$

where r_e and V_e are for the diode-switched boost converter:

$$\begin{aligned}
r_e &= r_L + Dr_{ds1} + D'r_d + D'r_C, \\
V_e &= V_o + V_D + (r_d - r_{ds1} + Dr_C) \frac{I_o}{D'},
\end{aligned} \tag{3.50}$$

and for the synchronous-switched boost converter

$$\begin{aligned} r_e &= r_L + Dr_{ds1} + D'r_{ds2} + D'r_C, \\ V_e &= V_o + (r_{ds2} - r_{ds1} + Dr_C) \frac{I_o}{D}. \end{aligned} \quad (3.51)$$

The transfer functions corresponding to Eq. (3.31) can be derived from Eq. (3.49) by transforming the state space into *Laplace* domain and applying linear algebra (cf. Section 2.4), which yields

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \left(\begin{bmatrix} \frac{s}{L} & \frac{D(1+sr_C C)}{LC} & \frac{V_e \left(s + \frac{I_o}{V_e C} \right)}{L} \\ \frac{D(1+sr_C C)}{LC} & \frac{(r_e - D^2 r_C + sL)(1+sr_C C)}{LC} & \frac{I_o}{DLC} \left(\frac{D^2 V_e}{I_o} - r_e - sL \right) (1+sr_C C) \end{bmatrix} \right) / \left[s^2 + s \frac{r_e}{L} + \frac{D^2}{LC} \right] * \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}. \quad (3.52)$$

The special transfer functions can be computed based on Eq. (3.52) and applying Eq. (3.32), which yields

$$\begin{aligned} & \begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ Z_{o-oci}^o & Z_{o-\infty} & G_{io-\infty} \end{bmatrix} \\ &= \begin{bmatrix} \frac{1}{sL + r_e - D^2 r_C} & \frac{1}{sL + r_e - (D^2 V_e / I_o)} & \frac{D(r_C - (V_e / I_o))}{sL + r_e - (D^2 V_e / I_o)} \\ \frac{1 + sr_C C}{sC} & \frac{(V_e - r_C I_o)(1 + sr_C C)}{D V_e (sC + (I_o / V_e))} & \frac{I_o(1 + sr_C C)}{D V_e (sC + (I_o / V_e))} \end{bmatrix}. \end{aligned} \quad (3.53)$$

The special output impedance Z_{o-oci} is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.53). In general, its value can be given by [17]

$$Z_{o-oci}^x = \frac{Z_{o-x}}{Y_{in-x}}, \quad (3.54)$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance (Y_{in-sco}) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.53).

The effect of the input capacitor C_1 (cf. Figure 3.8c) can be taken into account in such a manner that it is actually in parallel with the impedances measured from the input terminal without the input capacitor. It has no other effects on the dynamics of the converter. As a consequence,

$$\begin{aligned}
Y_{\text{in-}x}^{C_1} &= Y_{\text{in-}x} + \frac{sC_1}{1 + sr_{C_1}C_1}, \\
Y_{\text{in-sco}}^{C_1} &= Y_{\text{in-sco}} + \frac{sC_1}{1 + sr_{C_1}C_1},
\end{aligned} \tag{3.55}$$

where the subscript x means open- “o” or closed- “c” loop transfer function, respectively.

According to the denominator of the transfer functions in Eq. (3.52) and the resonant nature of the converter, undamped natural frequency (ω_n), resonant or damped natural frequency (ω_d), damping factor (ζ), and quality factor (Q) can be given by (cf. Section 2.5.2)

$$\omega_n = \frac{D'}{\sqrt{LC}}, \quad \omega_d = \frac{D'}{\sqrt{LC}} \sqrt{1 - \left(\frac{r_e}{2D'} \sqrt{\frac{C}{L}}\right)^2}, \quad \zeta = \frac{r_e}{2D'} \sqrt{\frac{C}{L}}, \quad Q = \frac{D'}{r_e} \sqrt{\frac{L}{C}}, \tag{3.56}$$

where $\sqrt{L/C}$ is known as the characteristic impedance (Z_o) of resonant circuit. It should be observed that the undamped natural frequency and damping factor vary with the operating point, and the control-to-output transfer function ($G_{\text{co-o}}$) in Eq. (3.52) contains an RHP zero at

$$\omega_{\text{RHP-z}} = \frac{D'^2 V_e - r_e J_o}{LI_o}, \tag{3.57}$$

causing design limitation to the maximum control bandwidth as discussed in Chapter 2 (Section 2.5.5). According to Eq. (3.57), the RHP zero is closest to origin when the load power is at its maximum, and the input voltage at its minimum.

3.4.3 Buck–Boost Converter

The averaged state space of the diode-switched boost converter (cf. Figure 3.10a) is given in Eq. (3.58), the averaged state space of the synchronous-switched converter (cf. Figure 3.10b) in Eq. (3.60), and the averaged state space of the noninverting buck–boost converter (cf. Figure 3.10c) in Eq. (3.62). The corresponding operation points are given in Eqs (3.59), (3.61), and (3.63), respectively.

$$\begin{aligned}
\frac{d\langle i_L \rangle}{dt} &= -\frac{(r_L + dr_{\text{ds1}} + d'r_d + d'r_C)}{L} \langle i_L \rangle - \frac{d'}{L} \langle v_C \rangle + \frac{d}{L} \langle v_{\text{in}} \rangle + \frac{d'r_C}{L} \langle i_o \rangle - \frac{d'V_D}{L}, \\
\frac{d\langle v_C \rangle}{dt} &= \frac{d'}{C} \langle i_L \rangle - \frac{i_o}{C} \langle i_o \rangle, \\
\frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_{\text{in}} \rangle, \\
\langle i_{\text{in}} \rangle &= d\langle i_L \rangle - \frac{1}{r_{C1}} \langle v_{C1} \rangle + \frac{1}{r_{C1}} \langle v_{\text{in}} \rangle, \\
\langle v_o \rangle &= d'r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle = \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.
\end{aligned} \tag{3.58}$$

$$\begin{aligned}
I_L &= \frac{I_o}{D'}, \\
I_{in} &= \frac{D}{D'} I_o, \\
V_o &= V_C, \\
V_o &= \frac{DV_{in}}{D'} - V_D - \frac{(r_L + Dr_{ds1} + D'r_d + DD'r_C)}{D'^2} \cdot I_o, \\
(V_{in} + V_o + V_D - r_C I_o)D'^2 - (V_{in} - (r_d - r_{ds1} + r_C)I_o)D' + (r_L + r_{ds1})I_o &= 0.
\end{aligned} \tag{3.59}$$

$$\begin{aligned}
\frac{d\langle i_L \rangle}{dt} &= -\frac{(r_L + dr_{ds1} + d'r_{ds2} + d'r_C)}{L} \langle i_L \rangle - \frac{d'}{L} \langle v_C \rangle + \frac{d}{L} \langle v_{in} \rangle + \frac{d'r_C}{L} \langle i_o \rangle, \\
\frac{d\langle v_C \rangle}{dt} &= \frac{d'}{C} \langle i_L \rangle - \frac{i_o}{C} \langle i_o \rangle, \\
\frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_{in} \rangle, \\
\langle i_{in} \rangle &= d\langle i_L \rangle - \frac{1}{r_{C1}} \langle v_{C1} \rangle + \frac{1}{r_{C1}} \langle v_{in} \rangle, \\
\langle v_o \rangle &= d'r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle = \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.
\end{aligned} \tag{3.60}$$

$$\begin{aligned}
I_L &= \frac{I_o}{D'}, \\
I_{in} &= \frac{D}{D'} I_o, \\
V_o &= V_C, \\
V_o &= \frac{DV_{in}}{D'} - V_D - \frac{(r_L + Dr_{ds1} + D'r_{ds2} + DD'r_C)}{D'^2} \cdot I_o, \\
(V_{in} + V_o - r_C I_o)D'^2 - (V_{in} - (r_{ds2} - r_{ds1} + r_C)I_o)D' + (r_L + r_{ds1})I_o &= 0.
\end{aligned} \tag{3.61}$$

$$\begin{aligned}
\frac{d\langle i_L \rangle}{dt} &= -\frac{(r_L + d2r_{ds1} + d'2r_{ds2} + d'r_C)}{L} \langle i_L \rangle - \frac{d'}{L} \langle v_C \rangle + \frac{d}{L} \langle v_{in} \rangle + \frac{d'r_C}{L} \langle i_o \rangle, \\
\frac{d\langle v_C \rangle}{dt} &= \frac{d'}{C} \langle i_L \rangle - \frac{i_o}{C} \langle i_o \rangle, \\
\frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_{in} \rangle, \\
\langle i_{in} \rangle &= d\langle i_L \rangle - \frac{1}{r_{C1}} \langle v_{C1} \rangle + \frac{1}{r_{C1}} \langle v_{in} \rangle, \\
\langle v_o \rangle &= d'r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle = \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.
\end{aligned} \tag{3.62}$$

$$\begin{aligned}
I_L &= \frac{I_o}{D'}, \\
I_{in} &= \frac{D}{D'} I_o, \\
V_o &= V_C, \\
V_o &= \frac{D V_{in}}{D'} - V_D - \frac{(r_L + D 2r_{ds1} + D' 2r_{ds2} + D D' r_C)}{D^2} \cdot I_o, \\
(V_{in} + V_o - r_C I_o) D'^2 - (V_{in} - (2r_{ds2} - 2r_{ds1} + r_C) I_o) D' + (r_L + 2r_{ds1}) I_o &= 0.
\end{aligned} \tag{3.63}$$

The linearized state space for both of the converters is given in (3.64):

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} &= -\frac{r_e}{L} \hat{i}_L - \frac{D'}{L} \hat{v}_C + \frac{D}{L} \hat{v}_{in} + \frac{D' r_C}{L} \hat{i}_o + \frac{V_e}{L} \hat{d}, \\
\frac{d\hat{v}_C}{dt} &= \frac{D'}{C} \hat{i}_L - \frac{1}{C} \hat{i}_o - \frac{I_L}{C} \hat{d}, \\
\frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{r_{C1} C} \hat{v}_{C1} + \frac{1}{r_{C1} C_1} \hat{v}_{in}, \\
\hat{i}_{in} &= D \hat{i}_L - \frac{\hat{v}_{C1}}{r_{C1}} + \frac{\hat{v}_{in}}{r_{C1}} + I_L \hat{d}, \\
\hat{v}_o &= \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt},
\end{aligned} \tag{3.64}$$

where r_e and V_e are for the diode-switched buck–boost converter

$$\begin{aligned}
r_e &= r_L + D r_{ds1} + D' r_d + D' r_C, \\
V_e &= V_{in} + V_o + V_D + (r_d - r_{ds1} + D r_C) \frac{I_o}{D'},
\end{aligned} \tag{3.65}$$

and for the synchronous-switched buck–boost converter

$$\begin{aligned}
r_e &= r_L + D r_{ds1} + D' r_{ds2} + D' r_C, \\
V_e &= V_{in} + V_o + (r_{ds2} - r_{ds1} + D r_C) \frac{I_o}{D'},
\end{aligned} \tag{3.66}$$

and for the noninverting buck–boost

$$\begin{aligned}
r_e &= r_L + D 2r_{ds1} + D' 2r_{ds2} + D' r_C, \\
V_e &= V_{in} + V_o + (2r_{ds2} - 2r_{ds1} + D r_C) \frac{I_o}{D'}.
\end{aligned} \tag{3.67}$$

The transfer functions corresponding to Eq. (3.31) can be derived from Eq. (3.64) by transforming the state space into *Laplace* domain and applying linear algebra (cf. Section 2.4), which yields

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \left(\begin{bmatrix} \frac{D^2 s}{L} & \frac{DD'(1+sr_C C)}{LC} & \frac{DV_e \left(s + \frac{I_o}{V_e C} \right)}{L} \\ \frac{DD'(1+sr_C C)}{LC} & \frac{(r_e - D^2 r_C + sL)(1+sr_C C)}{LC} & \frac{I_o \left(\frac{D^2 V_e}{I_o} - r_e - sL \right) (1+sr_C C)}{D'LC} \end{bmatrix} \Big/ \left[s^2 + s \frac{r_e}{L} + \frac{D^2}{LC} \right] * \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix} \right). \quad (3.68)$$

The special transfer functions can be computed based on Eq. (3.68) and applying Eq. (3.32), which yields

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ Z_{o-oci}^o & Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} \frac{D^2}{sL + r_e - D^2 r_C} & \frac{D^2}{sL + r_e - (D^2 V_e / I_o)} & \frac{DD'(r_C - (V_e / I_o))}{sL + r_e - (D^2 V_e / I_o)} \\ \frac{1 + sr_C C}{sC} & \frac{(1 - (I_o r_C / V_e))(1 + sr_C C)}{sC + (I_o / V_e)} & \frac{DI_o(1 + sr_C C)}{D'V_e(sC + (I_o / V_e))} \end{bmatrix}. \quad (3.69)$$

The special output impedance Z_{o-oci} is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.69). In general, its value can be given by [17]

$$Z_{o-oci}^x = \frac{Z_{o-x}}{Y_{in-x}}, \quad (3.70)$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance (Y_{in-sco}) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.69).

The effect of the input capacitor C_1 (cf. Figure 3.10c) can be taken into account in such a manner that it is actually in parallel with the impedances measured from the input terminal without the input capacitor. It has no other effects on the dynamics of the converter. As a consequence,

$$\begin{aligned} Y_{in-x}^{C_1} &= Y_{in-x} + \frac{sC_1}{1 + sr_{C1} C_1}, \\ Y_{in-sco}^{C_1} &= Y_{in-sco} + \frac{sC_1}{1 + sr_{C1} C_1}, \end{aligned} \quad (3.71)$$

where the subscript x means open- “o” or closed- “c” loop transfer function, respectively.

According to the denominator of the transfer functions in Eq. (3.68) and the resonant nature of the converter, undamped natural frequency (ω_n), resonant or damped natural frequency (ω_d), damping factor (ζ), and quality factor (Q) can be given by (cf. Section 2.5.2)

$$\omega_n = \frac{D'}{\sqrt{LC}}, \quad \omega_d = \frac{D'}{\sqrt{LC}} \sqrt{1 - \left(\frac{r_e}{2D'} \sqrt{\frac{C}{L}} \right)^2}, \quad \zeta = \frac{r_e}{2D'} \sqrt{\frac{C}{L}}, \quad Q = \frac{D'}{r_e} \sqrt{\frac{L}{C}}, \quad (3.72)$$

where $\sqrt{L/C}$ is known as the characteristic impedance (Z_o) of resonant circuit. It should be observed that the undamped natural frequency and damping factor vary with the operating point, and the control-to-output transfer function (G_{co-o}) in Eq. (3.68) contains an RHP zero at

$$\omega_{\text{RHP-z}} = \frac{D^2 V_e - r_e I_o}{L I_o}, \quad (3.73)$$

causing design limitation to the maximum control bandwidth as discussed in Chapter 2 (Section 2.5.5). According to Eq. (3.73), the RHP zero is closest to origin when the load power is at its maximum, and the input voltage at its minimum.

3.4.4 Superbuck Converter

The averaged state space of the superbuck converter (cf. Figure 3.13) is given in Eq. (3.74), and the corresponding operation point in Eq. (3.75), respectively.

$$\begin{aligned} \frac{d\langle i_{L1} \rangle}{dt} &= -\frac{r_{L1} + r_{C2} + dr_{ds} + d'r_d + d'r_{C1}}{L_1} \cdot \langle i_{L1} \rangle - \frac{r_{C2} + dr_{ds} + d'r_d}{L_1} \cdot \langle i_{L2} \rangle \\ &\quad - \frac{d'\langle v_{C1} \rangle}{L_1} - \frac{\langle v_{C2} \rangle}{L_1} + \frac{\langle v_{in} \rangle}{L_1} + \frac{r_{C2}}{L_1} \cdot \langle i_o \rangle - \frac{d'V_D}{L_1}, \\ \frac{d\langle i_{L2} \rangle}{dt} &= -\frac{r_{C2} + dr_{ds} + d'r_d}{L_2} \langle i_{L1} \rangle - \frac{r_{L2} + r_{C2} + dr_{ds} + dr_{C1} + d'r_d}{L_2} \langle i_{L2} \rangle \\ &\quad + \frac{d'\langle v_{C1} \rangle}{L_2} - \frac{\langle v_{C2} \rangle}{L_2} + \frac{r_{C2}}{L_2} \langle i_o \rangle - \frac{d'V_D}{L_2}, \\ \frac{d\langle v_{C1} \rangle}{dt} &= \frac{d'\langle i_{L1} \rangle}{C_1} - \frac{d'\langle i_{L2} \rangle}{C_1}, \\ \frac{d\langle v_{C2} \rangle}{dt} &= \frac{\langle i_{L1} \rangle}{C_2} + \frac{\langle i_{L2} \rangle}{C_2} - \frac{\langle i_o \rangle}{C_2}, \\ \langle i_{in} \rangle &= \langle i_{L1} \rangle, \\ \langle v_o \rangle &= r_{C2} \langle i_{L1} \rangle + r_{C2} \langle i_{L2} \rangle + \langle v_{C2} \rangle - r_{C2} \langle i_o \rangle = \langle v_{C2} \rangle + r_{C2} C_2 \frac{d\langle v_{C2} \rangle}{dt}. \end{aligned} \quad (3.74)$$

$$\begin{aligned}
I_{L1} &= DI_o, \\
I_{L2} &= D'I_o, \\
I_{in} &= DI_o, \\
V_o &= DV_{in} - D'V_D - (Dr_{ds} + DD'r_{C1} + D'r_d + D^2r_{L1} + D^2r_{L2})I_o, \\
V_{C2} &= V_o, \\
V_{C1} &= V_{in} - D'V_D - (Dr_{L1} - D'r_{L2})I_o.
\end{aligned} \tag{3.75}$$

The linearized state space is given by

$$\begin{aligned}
\frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1}\hat{i}_{L1} - \frac{r_{e2}}{L_1}\hat{i}_{L2} - \frac{D'}{L_1}\hat{v}_{C1} - \frac{1}{L_1}\hat{v}_{C2} + \frac{1}{L_1}\hat{v}_{in} + \frac{r_{C2}}{L_1}\hat{i}_o + \frac{V_{e1}}{L_1}\hat{d}, \\
\frac{d\hat{i}_{L2}}{dt} &= -\frac{r_{e2}}{L_2}\hat{i}_{L1} - \frac{r_{e3}}{L_2}\hat{i}_{L2} + \frac{D}{L_2}\hat{v}_{C1} - \frac{1}{L_2}\hat{v}_{C2} + \frac{r_{C2}}{L_2}\hat{i}_o + \frac{V_{e2}}{L_2}\hat{d}, \\
\frac{d\hat{v}_{C1}}{dt} &= \frac{D'}{C_1}\hat{i}_{L1} - \frac{D}{C_1}\hat{i}_{L2} - \frac{I_o}{C_1}\hat{d}, \\
\frac{d\hat{v}_{C2}}{dt} &= \frac{1}{C_2}\hat{i}_{L1} + \frac{1}{C_2}\hat{i}_{L2} - \frac{1}{C_2}\hat{i}_o, \\
\hat{i}_{in} &= \hat{i}_{L1}, \\
\hat{v}_o &= \hat{v}_{C2} + r_{C2}C_2 \frac{d\hat{v}_{C2}}{dt},
\end{aligned} \tag{3.76}$$

where

$$\begin{aligned}
r_{e1} &= r_{L1} + r_{C2} + Dr_{ds} + D'(r_d + r_{C1}), \\
r_{e2} &= r_{C2} + Dr_{ds} + D'r_d, \\
r_{e3} &= r_{L2} + r_{C2} + D(r_{ds} + r_{C1}) + D'r_d, \\
V_{e1} &= V_{in} + V_D + (r_d - r_{ds} + Dr_{C1} - Dr_{L1} + D'r_{L2})I_o, \\
V_{e2} &= V_{e1} - r_{C1}I_o, \\
D^2 - \frac{V_{in} + V_D + (r_{C1} + r_{ds} - r_d - 2r_{L2})I_o}{(r_{L1} + r_{L2} - r_{C1})I_o} \cdot D + \frac{V_o + V_D + (r_{L2} + r_d)I_o}{(r_{L1} + r_{L2} - r_{C1})I_o} &= 0.
\end{aligned} \tag{3.77}$$

The transfer functions corresponding to Eq. (3.31) can be derived from Eq. (3.76) by transforming the state space into *Laplace* domain and applying linear algebra (cf. Section 2.4), which yields

Input dynamics (i.e., the top row of transfer functions in Eq. (3.31))

$$\begin{aligned}
\Delta Y_{in-o} &= \frac{s}{L_1} \left(s^2 + s \frac{r_{e3}}{L_2} + \frac{C_1 + D^2C_2}{L_2C_1C_2} \right), \\
\Delta T_{oi-o} &= \frac{1}{L_1C_2} \left(s^2 + s \frac{r_{e3} - r_{e2}}{L_2} + \frac{D}{L_2C_1} \right) (1 + sr_{C2}C_2), \\
\Delta G_{ci-o} &= \frac{U_1}{L_1} \left(s^3 + s^2 \frac{D'I_oL_2 + (r_{e3}V_{e1} - r_{e1}V_{e2})C_1}{U_1L_2C_1} \right. \\
&\quad \left. + s \frac{(V_{e1} - V_{e2})C_1 + (D^2V_{e1} + DD'V_{e2} + (Dr_{e2} + D'r_{e3})I_o)C_2}{U_1L_2C_1C_2} + \frac{I_o}{U_1L_2C_1C_2} \right).
\end{aligned} \tag{3.78}$$

Output dynamics (i.e., the bottom row of transfer functions in Eq. (3.31))

$$\begin{aligned}
 \Delta G_{i_0-o} &= \frac{1}{L_1 C_2} \left(s^2 + s \frac{r_{e3} - r_{e2}}{L_2} + \frac{D}{L_2 C_1} \right) (1 + s r_{C2} C_2), \\
 \Delta Z_{o-o} &= \frac{1}{C_2} \left(s^3 + s^2 \frac{(r_{e3} - r_{C2}) L_1 + (r_{e1} - r_{C2}) L_2}{L_1 L_2} \right. \\
 &\quad \left. + s \frac{D^2 L_1 + D^2 L_2 + (r_{e1} r_{e3} - r_{e2}^2 - r_{C2} (r_{e1} - 2r_{e2} + r_{e3})) C_1}{L_1 L_2 C_1} \right. \\
 &\quad \left. + \frac{D^2 r_{e1} + 2DD' r_{e2} + D^2 r_{e3} - r_{C2}}{L_1 L_2 C_1} \right) (1 + s r_{C2} C_2), \\
 \Delta G_{c_0-o} &= \frac{(V_{e1} L_2 + V_{e2} L_1)}{L_1 L_2 C_2} \\
 &\quad \times \left(s^2 + s \frac{C_1 (V_{e1} (r_{e3} - r_{e2}) + V_{e2} (r_{e1} - r_{e2})) + (D' L_2 - D L_1) I_0}{C_1 (U_1 L_2 + U_2 L_1)} \right. \\
 &\quad \left. + \frac{D V_{e1} + D' V_{e2} - (D (r_{e1} - r_{e2}) + D' (r_{e2} - r_{e3})) I_0}{C_1 (V_{e1} L_2 + V_{e2} L_1)} \right) (1 + s r_{C2} C_2),
 \end{aligned} \tag{3.79}$$

where the determinant Δ is

$$\begin{aligned}
 s^4 + s^3 \frac{r_{e3} L_1 + r_{e1} L_2}{L_1 L_2} + s^2 \frac{(L_1 + L_2) C_1 + (D^2 L_1 + D^2 L_2) C_2 + (r_{e1} r_{e3} - r_{e2}^2) C_1 C_2}{L_1 L_2 C_1 C_2} \\
 + s \frac{(r_{e1} - 2r_{e2} + r_{e3}) C_1 + (D^2 r_{e1} + 2DD' r_{e2} + D^2 r_{e3}) C_2}{L_1 L_2 C_1 C_2} + \frac{1}{L_1 L_2 C_1 C_2}.
 \end{aligned} \tag{3.80}$$

The determinant has two complex conjugate or resonant LHP roots approximately at

$$\begin{aligned}
 \omega_{\text{res1}} &\approx \sqrt{\frac{1}{(L_1 + L_2) C_1}}, \\
 \omega_{\text{res2}} &\approx \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_2}}.
 \end{aligned} \tag{3.81}$$

The control-to-output transfer function (G_{c_0-o}) in Eq. (3.79) contains resonant zeros approximately at the frequency given in Eq. (3.82). The resonant zeros will be RHP zeros if the coefficient of first-order term in the numerator becomes negative as given in Eq. (3.83). The other terms in Eq. (3.38) except $D' L_2 - D L_1$ are always positive. Therefore, if designing the inductors such that $L_2 \geq (D_{\text{max}}/1 - D_{\text{max}}) L_1$, the RHP zeros do not appear when the duty ratio $D \leq D_{\text{max}}$ within the specified operation range. Typically, the inductors are designed to have equal value for the logistic reason and for reducing the costs [18].

$$\omega_{\text{res}} \approx \sqrt{\frac{1}{(L_1 + L_2) C_1}}, \tag{3.82}$$

$$C_1(V_{e1}(r_{e3} - r_{e2}) + V_{e2}(r_{e1} - r_{e2})) + (D'L_2 - DL_1)I_o < 0. \quad (3.83)$$

The special transfer functions can be computed based on Eqs. (3.78–3.80) by applying Eq. (3.32). The resulting transfer functions including the parasitic elements are extremely long preventing their publication as such in this book. The solving requires the use of software packages capable of symbolic computation such as Matlab™ Symbolic Toolbox. The special transfer functions are given omitting the parasitic elements as follows:

$$\begin{aligned} Y_{\text{in-sco}} &= \frac{s^2 + (D^2/L_2C_1)}{L_1s(s^2 + ((D^2L_2 + D^2L_1)/L_1L_2C_1))}, \\ Y_{\text{in-}\infty} &= \frac{s - (DI_o/C_1V_{e1})}{(L_1 + L_2)(s^2 + s[((D'L_2 + DL_1)I_o)/C_1(L_1 + L_2)V_{e1}] + [1/(C_1(L_1 + L_2))])}, \\ T_{\text{oi-}\infty} &= \frac{L_2(s^2 + s(D'I_o/C_1V_{e1}) + (D/L_2C_1))}{(L_1 + L_2)(s^2 + s[((D'L_2 + DL_1)I_o)/C_1(L_1 + L_2)V_{e1}] + [1/(C_1(L_1 + L_2))])}, \\ Z_{\text{o-oci}}^o &= \frac{s^2 + (D^2/L_2C_1)}{C_2s(s^2 + ((C_1 + D^2C_2)/L_2C_1C_2))}, \\ Z_{\text{o-}\infty} &= \frac{s^2 + s(D'I_o/C_1V_{e1}) + (D/L_2C_1)}{C_2(s^3 + s^2(D'I_o/C_1V_{e1}) + s(D/L_2C_1) + (I_o/L_2C_1C_2V_{e1}))}, \\ G_{\text{io-}\infty} &= \frac{-(s - (DI_o/C_1V_{e1}))}{L_2C_2(s^3 + s^2(D'I_o/C_1V_{e1}) + s(D/L_2C_2) + (I_o/L_2C_1C_2V_{e1}))}. \end{aligned} \quad (3.84)$$

The special output impedance $Z_{\text{o-oci}}$ is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.84). In general, its value can be given by [17]

$$Z_{\text{o-oci}}^x = \frac{Z_{\text{o-x}}}{Y_{\text{in-x}}}, \quad (3.85)$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance ($Y_{\text{in-sco}}$) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.84).

The effect of the input capacitor C_3 (i.e., if connected at the input terminal) can be taken into account in such a manner that it is actually in parallel with the impedances measured from the input terminal without the input capacitor. It has no other effects on the dynamics of the converter. As a consequence,

$$\begin{aligned} Y_{\text{in-x}}^{C_3} &= Y_{\text{in-x}} + \frac{sC_3}{1 + sr_{C_3}C_3}, \\ Y_{\text{in-sco}}^{C_1} &= Y_{\text{in-sco}} + \frac{sC_3}{1 + sr_{C_3}C_3}. \end{aligned} \quad (3.86)$$

Boundary Conduction Mode

The peak-to-peak ripple currents of the inductors L_1 and L_2 can be computed according to the on-time derivatives of the corresponding currents from Figure 3.14a at a certain operating point in Eq. (3.77) to be as follows:

$$\begin{aligned}\Delta i_{L1\text{-pp}} &= \frac{DT_s(V_{\text{in}} - V_o - (Dr_{L1} + r_{\text{ds}})I_o)}{L_1}, \\ \Delta i_{L2\text{-pp}} &= \frac{DT_s(V_{\text{in}} - V_o - (Dr_{L1} + D'r_{C1})I_o)}{L_2}.\end{aligned}\quad (3.87)$$

The mode boundary between the CCM and DCM conduction modes would take place [2] when the output current equals half the sum of the inductor current peak-to-peak ripples given in Eq. (3.87) or $\Delta i_{L1\text{-pp}} + \Delta i_{L2\text{-pp}} = 2I_o$, because the sum of the inductor currents is supplied to the output capacitor (cf. Figure 3.14) via the MOSFET during the on-time and via the diode during the off-time. The critical K -value based on the sum of inductor currents yields $K_{\text{crit}} = D'$, which is the same as defined for the conventional buck converter in Ref. [2]. The K -value for analyzing the operation mode (i.e., CCM: $K > K_{\text{crit}}$, DCM: $K < K_{\text{crit}}$, and BCM: $K = K_{\text{crit}}$) can be given by $2L_p/T_s R_{\text{eq}}$, where $L_p = L_1 L_2 / (L_1 + L_2)$ and $R_{\text{eq}} = V_o / I_o$, respectively.

3.4.5 Coupled-Inductor Superbuck Converter

By means of the coupling of the inductors, the input current ripple in the superbuck converter can be reduced down to zero [19,20]. The application of the coupled-inductor technique will, however, also affect the dynamics of the converter profoundly. The methods to model the converter dynamic behavior, when the coupled inductor is used, are presented in Section 2.4.3. Following the presented steps and applying the linearized state space of the discrete inductor converter in Eq. (3.76), the coupled-inductor state space can be given by

$$\begin{aligned}\frac{d\hat{i}_{L1}}{dt} &= -\frac{L_2 r_{e1} - Mr_{e2}}{L_1 L_2 - M^2} \hat{i}_{L1} - \frac{L_2 r_{e2} - Mr_{e3}}{L_1 L_2 - M^2} \hat{i}_{L2} - \frac{L_2 D' + MD}{L_1 L_2 - M^2} \hat{v}_{C1} - \frac{L_2 - M}{L_1 L_2 - M^2} \hat{v}_{C2} \\ &\quad + \frac{L_2}{L_1 L_2 - M^2} \hat{v}_{\text{in}} + \frac{L_2 r_{c2}}{L_1 L_2 - M^2} \hat{i}_o + \frac{L_2 V_{e1} - MV_{e2}}{L_1 L_2 - M^2} \hat{d}, \\ \frac{d\hat{i}_{L2}}{dt} &= -\frac{L_1 r_{e2} - Mr_{e1}}{L_1 L_2 - M^2} \hat{i}_{L1} - \frac{L_1 r_{e3} - Mr_{e2}}{L_1 L_2 - M^2} \hat{i}_{L2} + \frac{DL_1 + MD'}{L_1 L_2 - M^2} \hat{v}_{C1} - \frac{L_1 - M}{L_1 L_2 - M^2} \hat{v}_{C2} \\ &\quad - \frac{M}{L_1 L_2 - M^2} \hat{v}_{\text{in}} + \frac{(L_1 - M)r_{c2}}{L_1 L_2 - M^2} \hat{i}_o + \frac{L_1 V_{e2} - MV_{e1}}{L_1 L_2 - M^2} \hat{d}, \\ \frac{d\hat{v}_{C1}}{dt} &= \frac{D'}{C_1} \hat{i}_{L1} - \frac{D}{C_1} \hat{i}_{L2} - \frac{I_o}{C_1} \hat{d}, \\ \frac{d\hat{v}_{C2}}{dt} &= \frac{1}{C_2} \hat{i}_{L1} + \frac{1}{C_2} \hat{i}_{L2} - \frac{1}{C_2} \hat{i}_o, \\ \hat{i}_{\text{in}} &= \hat{i}_{L1}, \\ \hat{v}_o &= \hat{v}_{C2} + r_{C2} C_2 \frac{d\hat{v}_{C2}}{dt}.\end{aligned}\quad (3.88)$$

The transfer functions corresponding to Eq. (3.31) can be derived from Eq. (3.88) by transforming the state space into *Laplace* domain and applying linear algebra (cf. Section 2.4), which yields

Input dynamics (i.e., the top row of transfer functions in Eq. (3.31))

$$\begin{aligned}\Delta Y_{\text{in-o}} &= \frac{sL_2}{L_1L_2 - M^2} \left(s^2 + s \frac{r_{e3}}{L_2} + \frac{C_1 + D^2C_2}{L_2C_1C_2} \right), \\ \Delta T_{\text{oi-o}} &= \frac{1}{(L_1L_2 - M^2)C_2} \left(s^2(L_2 - M) + s(r_{e3} - r_{e2}) + \frac{D}{C_1} \right) (1 + sr_{C2}C_2), \\ \Delta G_{\text{ci-o}} &= \frac{1}{L_1L_2 - M^2} \left(s^3(V_{e1}L_2 - MV_{e2}) + s^2 \frac{(r_{e3}V_{e1} - r_{e1}V_{e2})C_1 + (D'L_2 + M)I_o}{C_1} \right. \\ &\quad \left. + s \frac{(V_{e1} - V_{e2})C_1 + (D^2V_{e1} + DD'V_{e2} + (Dr_{e2} + D'r_{e3})I_o)C_2}{C_1C_2} + \frac{I_o}{C_1C_2} \right).\end{aligned}\tag{3.89}$$

Output dynamics (i.e., the bottom row of transfer functions in Eq. (3.31))

$$\begin{aligned}\Delta G_{\text{io-o}} &= \frac{1}{(L_1L_2 - M^2)C_2} \left(s^2(L_2 - M) + s(r_{e3} - r_{e2}) + \frac{D}{C_1} \right) (1 + sr_{C2}C_2), \\ \Delta Z_{\text{o-o}} &= \frac{1}{C_2} \left(s^3 + s^2 \frac{(r_{e3} - r_{C2})L_1 + (r_{e1} - r_{C2})L_2}{L_1L_2} \right. \\ &\quad \left. + s \frac{(r_{e3} - r_{C2})L_1 + (r_{e1} - r_{C2})L_2 - 2(r_{e2} - r_{C2})M}{L_1L_2 - M^2} \right. \\ &\quad \left. + \frac{D^2r_{e1} + 2DD'r_{e2} + D^2r_{e3} - r_{C2}}{(L_1L_2 - M^2)C_1} \right) (1 + sr_{C2}C_2), \\ \Delta G_{\text{co-o}} &= \left(s^2 \frac{(L_2 - M)V_{e1} + (L_1 - M)V_{e2}}{(L_1L_2 - M^2)C_2} + s \frac{E_1 + (D'(L_2 - M) - D(L_1 - M))I_o}{(L_1L_2 - M^2)C_1C_2} \right. \\ &\quad \left. + \frac{E_2}{(L_1L_2 - M^2)C_1C_2} \right) (1 + sr_{C2}C_2),\end{aligned}$$

$$\begin{aligned}E_1 &= ((r_{e3} - r_{e2})V_{e1} + (r_{e1} - r_{e2})V_{e2})C_1, \\ E_2 &= (DV_{e1} + D'V_{e2}) - (D(r_{e1} - r_{e2}) + D'(r_{e2} - r_{e3}))I_o,\end{aligned}\tag{3.90}$$

where the determinant Δ is

$$\begin{aligned}\Delta &= s^4 + s^3 \frac{r_{e1}L_2 + r_{e3}L_1 - 2Mr_{e2}}{L_1L_2 - M^2} + s^2a_2 + sa_1 + \frac{1}{(L_1L_2 - M^2)C_1C_2}, \\ a_2 &= \frac{(r_{e1}r_{e3} - r_{e2}^2)C_1C_2 + (L_1 + L_2 - 2M)C_1 + (D^2L_1 + D^2L_2 + 2DD'M)C_2}{(L_1L_2 - M^2)C_1C_2}, \\ a_1 &= \frac{(r_{e1} - 2r_{e2} + r_{e3})C_1 + (D^2r_{e1} + 2DD'r_{e2} + D^2r_{e3})C_2}{(L_1L_2 - M^2)C_1C_2}.\end{aligned}\tag{3.91}$$

The stability of the coupled-inductor converter at open loop can be studied based on the determinant coefficients as instructed in Section 2.5.3. When constructing the *Routh* array, it can be concluded that the converter is stable at open loop.

The special transfer functions can be computed based on Eqs (3.89–3.91) by applying Eq. (3.32). The resulting transfer functions, including the parasitic elements, are extremely long preventing their publication as such in this book. The solving requires the use of software packages capable of symbolic computation such as Matlab Symbolic Toolbox. The special transfer functions are given omitting the parasitic elements as follows:

$$\begin{aligned}
 Y_{\text{in-sco}} &= \frac{s^2 L_2 C_1 + D^2}{s^3 (L_1 L_2 - M^2) C_1 + s(D^2 L_1 + D'^2 L_2 + 2DD'M)}, \\
 Y_{\text{in-}\infty} &= \frac{s C_1 V_{e1} - DI_o}{s^2 (L_1 + L_2 - 2M) V_{e1} C_1 + s(D'L_2 - DL_1 + (D - D')M)I_o + V_{e1}}, \\
 T_{\text{oi-}\infty} &= \frac{s^2 (L_2 - M) C_1 V_{e1} + s(D'L_2 + DM)I_o + DV_{e1}}{s^2 (L_1 + L_2 - 2M) C_1 V_{e1} + s(D'L_2 - DL_1 + (D - D')M)I_o + V_{e1}}, \\
 Z_{\text{o-oci}}^{\text{o}} &= \frac{s^2 L_2 C_1 + D^2}{s^3 L_2 C_1 C_2 + s(C_1 + D^2 C_2)}, \\
 Z_{\text{o-}\infty} &= \frac{s^2 (L_2 - M) C_1 V_{e1} + s(D'L_2 + DM)I_o + DV_{e1}}{s^3 (L_2 - M) C_1 V_{e1} + s^2 (D'L_2 + DM)I_o + s C_2 DV_{e1} + I_o}, \\
 G_{\text{io-}\infty} &= \frac{-s C_1 V_{e1} + DI_o}{s^3 (L_2 - M) C_1 V_{e1} + s^2 (D'L_2 + DM)I_o + s C_2 DV_{e1} + I_o}.
 \end{aligned} \tag{3.92}$$

The special output impedance $Z_{\text{o-oci}}$ is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.92). In general, its value can be given by [17]

$$Z_{\text{o-oci}}^x = \frac{Z_{\text{o-x}}}{Y_{\text{in-x}}} Y_{\text{in-sco}}, \tag{3.93}$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance ($Y_{\text{in-sco}}$) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.92).

The effect of the input capacitor C_3 (i.e., if connected at the input terminal) can be taken into account in such a manner that it is actually in parallel with the impedances measured from the input terminal without the input capacitor. It has no other effects on the dynamics of the converter. As a consequence,

$$\begin{aligned}
 Y_{\text{in-x}}^{C_3} &= Y_{\text{in-x}} + \frac{s C_3}{1 + sr_{C_3} C_3}, \\
 Y_{\text{in-sco}}^{C_3} &= Y_{\text{in-sco}} + \frac{s C_3}{1 + sr_{C_3} C_3}.
 \end{aligned} \tag{3.94}$$

Input-Current Ripple Reduction

Applying the coupled inductor algorithms (cf. Section 2.4.3) to the inductor current derivatives given in Eq. (3.87), the peak-to-peak ripple values become

$$\begin{aligned}\Delta i_{L1\text{-pp}} &= \left(\frac{(L_2 - M)(V_{\text{in}} - V_o - (Dr_{L1} + r_{\text{ds}})I_o)}{L_1L_2 - M^2} + \frac{MD'(r_{C1}I_o + V_D)}{L_1L_2 - M^2} \right) DT_s, \\ \Delta i_{L2\text{-pp}} &= \left(\frac{(L_1 - M)(V_{\text{in}} - V_o - (Dr_{L1} + r_{\text{ds}})I_o)}{L_1L_2 - M^2} - \frac{L_1D'(r_{C1}I_o + V_D)}{L_1L_2 - M^2} \right) DT_s.\end{aligned}\quad (3.95)$$

According to Eq. (3.95), the close-to-zero-input ripple or $\Delta i_{L1\text{-pp}} \approx 0$ can be obtained, when $M = L_2$ or $k = \sqrt{L_2/L_1}$. These values are also the commonly defined zero input ripple conditions [20]. As a consequence, the residual peak-to-peak ripple values are

$$\begin{aligned}\Delta i_{L1\text{-pp}} &= \frac{r_{C1}I_o + V_D}{L_1 - L_2} \cdot DD'T_s, \\ \Delta i_{L2\text{-pp}} &= \frac{V_{\text{in}} - V_o - (Dr_{L1} + r_{\text{ds}})I_o}{L_2} \cdot DT_s - \frac{r_{C1}I_o + V_D}{L_1 - L_2} \cdot \frac{DD'T_sL_1}{L_2},\end{aligned}\quad (3.96)$$

which imply that L_1 should be sufficiently higher than L_2 for obtaining optimal ripple reduction.

Substituting M and k in the small-signal state space in Eq. (3.88) with the above given values yields

$$\begin{aligned}\frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1} - r_{e2}}{L_1 - L_2} \hat{i}_{L1} - \frac{r_{e2} - r_{e3}}{L_1 - L_2} \hat{i}_{L2} \\ &\quad - \frac{1}{L_1 - L_2} \hat{v}_{C1} + \frac{1}{L_1 - L_2} \hat{v}_{\text{in}} + \frac{V_{e1} - V_{e2}}{L_1 - L_2} \hat{d}, \\ \frac{d\hat{i}_{L2}}{dt} &= -\frac{L_1r_{e2} - L_2r_{e1}}{(L_1 - L_2)L_2} \hat{i}_{L1} - \frac{L_1r_{e3} - L_2r_{e2}}{(L_1 - L_2)L_2} \hat{i}_{L2} + \frac{DL_1 + D'L_2}{(L_1 - L_2)L_2} \hat{v}_{C1} - \frac{1}{L_2} \hat{v}_{C2} \\ &\quad - \frac{1}{L_1 - L_2} \hat{v}_{\text{in}} + \frac{r_{C2}}{L_2} \hat{i}_o + \frac{L_1V_{e2} - L_2V_{e1}}{(L_1 - L_2)L_2} \hat{d}, \\ \frac{d\hat{v}_{C1}}{dt} &= \frac{D'}{C_1} \hat{i}_{L1} - \frac{D}{C_1} \hat{i}_{L2} - \frac{I_o}{C_1} \hat{d}, \\ \frac{d\hat{v}_{C2}}{dt} &= \frac{1}{C_2} \hat{i}_{L1} + \frac{1}{C_2} \hat{i}_{L2} - \frac{1}{C_2} \hat{i}_o, \\ \hat{i}_{\text{in}} &= \hat{i}_{L1} \\ \hat{v}_o &= \hat{v}_{C2} + r_{C2}C_2 \frac{d\hat{v}_{C2}}{dt}.\end{aligned}\quad (3.97)$$

The corresponding set of transfer functions can be given by

Input dynamics:

$$\begin{aligned}\Delta Y_{\text{in-o}} &= \frac{s}{L_1 - L_2} \left(s^2 + s \frac{r_{e3}}{L_2} + \frac{C_1 + D^2 C_2}{L_2 C_1 C_2} \right), \\ \Delta T_{\text{oi-o}} &= \frac{1}{(L_1 - L_2) C_2} \left(s \frac{r_{e3} - r_{e2}}{L_2} + \frac{D}{L_2 C_1} \right) (1 + sr_{C_2} C_2), \\ \Delta G_{\text{ci-o}} &= \frac{1}{L_1 - L_2} (s^3 (V_e - V_{e2}) + s^2 \frac{(r_{e3} V_{e1} - r_{e2} V_{e2}) C_1 + L_2 I_o}{L_2 C_1} \\ &\quad + s \frac{(V_{e1} - V_{e2}) C_1 + (D^2 V_{e1} + DD' V_{e2} + (Dr_{e2} + D'r_{e3}) I_o) C_2}{L_2 C_1 C_2} + \frac{I_o}{L_2 C_1 C_2}).\end{aligned}\quad (3.98)$$

Output dynamics:

$$\begin{aligned}\Delta G_{\text{io-o}} &= \frac{1}{(L_1 - L_2) C_2} \left(s \frac{r_{e3} - r_{e2}}{L_2} + \frac{D}{L_2 C_1} \right) (1 + sr_{C_2} C_2), \\ \Delta Z_{\text{o-o}} &= \frac{1}{C_2} (s^3 + s^2 \frac{(r_{e3} - r_{C_2}) L_1 + (r_{e1} - 2r_{e2} + r_{C_2}) L_2}{(L_1 - L_2) L_2} \\ &\quad + s \frac{(r_{e1} r_{e3} - r_{e2}^2 - (r_{e1} - 2r_{e2} + r_{e3}) r_{C_2}) C_1 + D^2 L_1 + D'(1 + D) L_1}{(L_1 - L_2) L_2} \\ &\quad + \frac{D^2 r_{e1} + 2DD' r_{e2} + D'^2 r_{e3} - r_{C_2}}{(L_1 - L_2) L_2} (1 + sr_{C_2} C_2), \\ \Delta G_{\text{co-o}} &= \frac{V_{e2}}{L_2 C_2} (s^2 + s \frac{((r_{e3} - r_{e2}) V_{e1} + (r_{e1} - r_{e2}) V_{e2}) C_1 - D(L_1 - L_2) I_o}{V_{e2} (L_1 - L_2) C_1} \\ &\quad + \frac{DV_{e1} + D' V_{e2} + (D(r_{e2} - r_{e1}) + D'(r_{e3} - r_{e2})) I_o}{V_{e2} (L_1 - L_2) C_1} (1 + sr_{C_2} C_2),\end{aligned}\quad (3.99)$$

where the determinant (Δ) is

$$\begin{aligned}\Delta &= s^4 + s^3 \frac{r_{e3} L_1 + (r_{e1} - 2r_{e2}) L_2}{(L_1 - L_2) L_2} + s^2 a_2 + s a_1 + \frac{1}{(L_1 - L_2) L_2 C_1 C_1}, \\ a_2 &= \frac{(r_{e1} r_{e3} - r_{e2}^2) C_1 C_2 + (L_1 - L_2) C_1 + (D^2 L_1 + D'(1 + D) L_2) C_2}{(L_1 - L_2) L_2 C_1 C_2}, \\ a_1 &= \frac{(r_{e1} - 2r_{e2} + r_{e3}) C_1 + (D^2 r_{e1} + 2DD' r_{e2} + D'^2 r_{e3}) C_2}{(L_1 - L_2) L_2 C_1 C_2}.\end{aligned}\quad (3.100)$$

The special transfer functions can be computed based on Eqs. (3.98–3.100) by applying Eq. (3.32) or simply from Eq. (3.92) substituting $M = L_2$.

The special transfer functions are given omitting the parasitic elements as follows:

$$\begin{aligned}
Y_{\text{in-sco}} &= \frac{s^2 L_2 C_1 + D^2}{s^3 (L_1 - L_2) L_2 C_1 + s(D^2 L_1 + D'(1 + D)L_2)}, \\
Y_{\text{in-}\infty} &= \frac{s C_1 V_{e1} - D I_o}{s^2 (L_1 - L_2) V_{e1} C_1 + s D (L_2 - L_1) I_o + V_{e1}}, \\
T_{\text{oi-}\infty} &= \frac{s L_2 I_o + D V_{e1}}{s^2 (L_1 - L_2) C_1 V_{e1} + s D (L_2 - L_1) I_o + V_{e1}}, \\
Z_{\text{o-oci}}^{\text{o}} &= \frac{s^2 L_2 C_1 + D^2}{s^3 L_2 C_1 C_2 + s(C_1 + D^2 C_2)}, \\
Z_{\text{o-}\infty} &= \frac{s L_2 I_o + D V_{e1}}{s^2 L_2 I_o + s C_2 D V_{e1} + I_o}, \\
G_{\text{io-}\infty} &= \frac{-s C_1 V_{e1} + D I_o}{s^2 L_2 I_o + s C_2 D V_{e1} + I_o}.
\end{aligned} \tag{3.101}$$

The special output impedance $Z_{\text{o-oci}}$ is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.101). In general, its value can be given by [17]

$$Z_{\text{o-oci}}^x = \frac{Z_{\text{o-x}}}{Y_{\text{in-x}}} Y_{\text{in-sco}}, \tag{3.102}$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance ($Y_{\text{in-sco}}$) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.101).

Design Considerations

According to Eq. (3.99), the control-to-output transfer function ($G_{\text{co-o}}$) may contain two RHP zeros depending on the operating point approximately at

$$\omega_{z\text{-RHP}} \approx \sqrt{\frac{1}{(1 - k^2) L_1 C_1}} \tag{3.103}$$

or

$$\begin{aligned}
\omega_{\text{zero-RHP1}} &\approx \frac{D I_o}{V_{\text{in}} C_1}, \\
\omega_{\text{zero-RHP2}} &\approx \frac{V_{\text{in}}}{D I_o (1 - k^2) L_1},
\end{aligned} \tag{3.104}$$

when

$$(r_{e3} - r_{e2}) V_{e1} + (r_{e1} - r_{e2}) V_{e2} C_1 - D(1 - k^2) L_1 I_o < 0, \tag{3.105}$$

where k is the coupling coefficient ($\sqrt{L_2/L_1}$). The appearance of the RHP zero is most likely in the applications, where the input voltage is rather low and the output current rather high. In this case, the appearance of the RHP zeros cannot

be anymore canceled, because the coupling coefficient (k) has to be less than 1 for proper operation, and therefore, there is no possibility to choose the inductor values as in the case of uncoupled inductors in Section 3.4.4. This means that the control bandwidth shall be designed to be lower than the lowest RHP zero for stability to exist.

3.5 Fixed-Frequency Operation in DCM

The small-signal modeling of the converters operating under fixed-frequency operation in CCM can be modeled without considering the methods presented in Section 3.3, because the instantaneous inductor current is continuous within the switching cycle. Therefore, the circuit theory can be applied directly to construct the required derivatives. In DCM, the instantaneous inductor current is discontinuous, which means that the charge incorporated in the inductor current is not anymore distributed within the on- and off-times following the duty ratio and its complement. Therefore, the generalized method has to be applied.

The DCM operation is possible only if a part of the PWM switches in the power stage are implemented by using components, which can provide only unidirectional current flow such as diodes. Therefore, when the inductor current tends to go negative during the off-time, the corresponding current carrying path is effectively disconnected. As a consequence, the converters will have three different topological subcircuits during a switching cycle: one for the on-time, one for the off-time1, and one for the off-time2 (cf. Figure 3.7, Section 3.3.1). The corresponding inductor-current waveform is shown in Figure 3.15. It is natural that the time-varying averaged inductor current $\langle i_L \rangle$ is continuous regardless of the operation mode. In DCM, its value is less than half the peak value of the instantaneous inductor current.

When considering the generalized state-space equations we defined in Section 3.3, the only unknown variable is the length of the off-time1 ($t_{\text{off}1}$). The dynamics associated with $t_{\text{off}1}$ can be recovered by computing its relation to $\langle i_L \rangle$ [1] according to the waveform of Figure 3.15, which gives

$$\langle i_L \rangle = \frac{1}{T_s} \int_0^{T_s} i_L dt = \frac{1}{2T_s} \cdot m_1 t_{\text{on}} (t_{\text{on}} + t_{\text{off}1}), \quad (3.106)$$

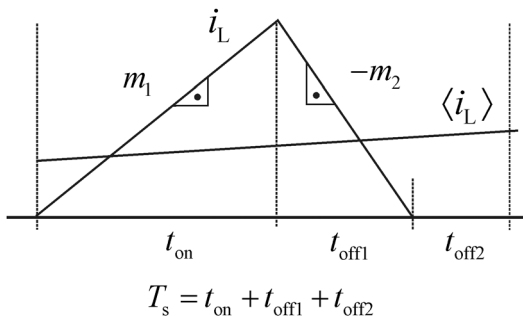


Figure 3.15 Inductor-current waveform in DCM.

and which under the fixed-frequency operation equals

$$\langle i_L \rangle = \frac{1}{2} \cdot m_1 d (d + d_1) T_s. \quad (3.107)$$

According to Eq. (3.107), we find that

$$d_1 = \frac{2\langle i_L \rangle}{dm_1 T_s} - d. \quad (3.108)$$

In order to find the fixed-frequency averaged models in DCM, $t_{\text{off}1}$ or d_1 has to be replaced with Eq. (3.108) in the generalized averaged state-space equations given in Section 3.3. We will treat in this section only the basic second-order converters. The generalized modeling method is, however, very powerful enabling the modeling of the higher order converter even in mixed conduction mode.

The DCM transfer functions are typically given in the form, where the steady-state duty ratio (D), the input (V_{in}) and output (V_{o}) voltages, and the cycle time (T_s) are embedded into the notations M (i.e., $V_{\text{o}}/V_{\text{in}}$) and K (i.e., $2L/T_s R_{\text{eq}}$), where R_{eq} corresponds to $V_{\text{o}}/I_{\text{o}}$, respectively [2]. We do not perform the modeling in detail but we give only the averaged and small-signal state spaces as well as the set of basic transfer functions.

3.5.1 Buck Converter

The power stage and the topological subcircuit structures are given in Section 3.3.1 (cf. Figures 3.6 and 3.7). The averaged state space can be derived based on Eqs (3.11–3.13), and (3.108), as already explained. This process yields

$$\begin{aligned} \frac{d\langle i_L \rangle}{dt} &= \frac{d(\langle v_{\text{in}} \rangle + (r_d - r_{\text{ds}1})\langle i_L \rangle + V_{\text{D}})}{L} \\ &\quad - \frac{2\langle i_L \rangle}{dT_s} \cdot \frac{(r_L + r_d + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_{\text{o}} \rangle + V_{\text{D}}}{\langle v_{\text{in}} \rangle - (r_L + r_{\text{ds}1} + r_C)\langle i_L \rangle - \langle v_C \rangle + r_C\langle i_{\text{o}} \rangle}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{\langle i_{\text{o}} \rangle}{C}, \\ \langle i_{\text{in}} \rangle &= \frac{d^2 T_s}{2L} (\langle v_{\text{in}} \rangle - (r_L + r_{\text{ds}1} + r_C)\langle i_L \rangle - \langle v_C \rangle + r_C\langle i_{\text{o}} \rangle), \\ \langle v_{\text{o}} \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}. \end{aligned} \quad (3.109)$$

The operation in DCM will actually remove the resonant behavior of the converter, and therefore, the parasitic loss elements of the power-stage component do not affect much on the dynamics of the converter but only on the operation point. The ESR (i.e., equivalent series resistance) of the output capacitor (r_C) is left in the state space, because it has a fundamental effect on the output dynamics in terms of load transient response and stability [1]. Therefore, the parasitic elements are usually omitted from the

state space, which yields a simplified and more convenient averaged state space as follows:

$$\begin{aligned}
 \frac{d\langle i_L \rangle}{dt} &= \frac{d\langle v_{in} \rangle}{L} - \frac{2\langle i_L \rangle \langle v_C \rangle}{dT_s(\langle v_{in} \rangle - \langle v_C \rangle)}, \\
 \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\
 \langle i_{in} \rangle &= \frac{d^2 T_s(\langle v_{in} \rangle - \langle v_C \rangle)}{2L}, \\
 \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.
 \end{aligned} \tag{3.110}$$

The operation point can be derived from Eq. (3.109) by setting the derivatives to zero. This procedure yields

$$\begin{aligned}
 I_L &= I_o, \\
 I_{in} &= \frac{((r_L + r_d)I_o + V_o + V_D)}{(V_{in} + (r_d - r_{ds1})I_o + V_D)} \cdot I_o, \\
 V_o &= V_C, \\
 D &= \sqrt{\frac{2LI_o}{T_s} \cdot \frac{V_o + V_D + (r_L + r_d)I_o}{(V_{in} - V_o - (r_L + r_{ds1})I_o)(V_{in} + V_D + (r_d - r_{ds1})I_o)}}.
 \end{aligned} \tag{3.111}$$

When omitting the parasitic loss elements in Eq. (3.111) and utilizing the denotations M , K , and R_{eq} as already defined, the operating point and the linearized state space can be given by

$$\begin{aligned}
 I_L &= I_o, \\
 I_{in} &= MI_o, \\
 V_o &= V_C, \\
 M &= \frac{2}{1 + \sqrt{1 + (4K/D^2)}}, \quad D = M\sqrt{\frac{K}{1-M}}, \quad D_1 = \sqrt{K(1-M)}.
 \end{aligned} \tag{3.112}$$

$$\begin{aligned}
 \frac{d\hat{i}_L}{dt} &= -\frac{R_{eq}}{L} \sqrt{\frac{K}{1-M}} \cdot \hat{i}_L - \frac{1}{L(1-M)} \sqrt{\frac{K}{1-M}} \cdot \hat{v}_C \\
 &\quad + \frac{(2-M)M}{L(1-M)} \sqrt{\frac{K}{1-M}} \cdot \hat{v}_{in} + \frac{2V_{in}}{L} \cdot \hat{d}, \\
 \frac{d\hat{v}_C}{dt} &= \frac{\hat{i}_L}{C} - \frac{\hat{i}_o}{C}, \\
 \hat{i}_{in} &= -\frac{M^2}{R_{eq}(1-M)} \cdot \hat{v}_C + \frac{M^2}{R_{eq}(1-M)} \cdot \hat{v}_{in} + \frac{2V_o}{R_{eq}} \sqrt{\frac{1-M}{K}} \cdot \hat{d}, \\
 \hat{v}_o &= \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt}.
 \end{aligned} \tag{3.113}$$

The set of transfer functions corresponding to Eq. (3.31) can be given by

$$\begin{aligned}
 \Delta Y_{\text{in-o}} &= \frac{M^2}{1-M} \left(s^2 \frac{1}{R_{\text{eq}}} + s \frac{1}{L} \sqrt{\frac{K}{1-M}} + \frac{1-M}{R_{\text{eq}}LC} \sqrt{\frac{K}{1-M}} \right), \\
 \Delta T_{\text{oi-o}} &= \frac{M^2}{R_{\text{eq}}C(1-M)} \cdot \left(s + \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}} \right), \\
 \Delta G_{\text{ci-o}} &= 2V_o \left(s^2 \frac{1}{R_{\text{eq}}} \sqrt{\frac{1-M}{K}} + s \frac{1}{L} + \frac{1}{R_{\text{eq}}LC} \right), \\
 \Delta G_{\text{io-o}} &= \frac{M(2-M)}{LC(1-M)} \sqrt{\frac{K}{1-M}} \cdot (1 + sr_C C), \\
 \Delta Z_{\text{o-o}} &= \frac{(sL + R_{\text{eq}} \sqrt{K/(1-M)})(1 + sr_C C)}{LC}, \\
 \Delta G_{\text{co-o}} &= \frac{2V_{\text{in}}(1 + sr_C C)}{LC},
 \end{aligned} \tag{3.114}$$

where the denominator (Δ) of the transfer functions is

$$\Delta = s^2 + s \cdot \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}} + \frac{1}{LC(1-M)} \sqrt{\frac{K}{1-M}}. \tag{3.115}$$

The special transfer functions can be computed based on Eq. (3.114) by applying Eq. (3.32) yielding

$$\begin{aligned}
 Y_{\text{in-sco}} &= \frac{M^2}{R_{\text{eq}}(1-M)}, \\
 Y_{\text{in-}\infty} &= -\frac{MI_o}{V_{\text{in}}}, \\
 T_{\text{oi-}\infty} &= \frac{M}{R_{\text{eq}}} \sqrt{\frac{1-M}{K}} \left(sL + R_{\text{eq}} \sqrt{\frac{K}{1-M}} \right), \\
 Z_{\text{o-oci}}^o &= \frac{(sL + R_{\text{eq}} \sqrt{K/(1-M)})(1 + sr_C C)}{s^2LC + sR_{\text{eq}}C \sqrt{K/(1-M)} + (1-M) \sqrt{K/(1-M)}}, \\
 Z_{\text{o-}\infty} &= \frac{sL + R_{\text{eq}} \sqrt{K/(1-M)}}{s^2LC + sR_{\text{eq}}C \sqrt{K/(1-M)} + \sqrt{K/(1-M)}}, \\
 G_{\text{io-}\infty} &= \frac{M \sqrt{K/(1-M)}(1 + sr_C C)}{s^2LC + sR_{\text{eq}}C \sqrt{K/(1-M)} + \sqrt{K/(1-M)}}.
 \end{aligned} \tag{3.116}$$

The special output impedance $Z_{\text{o-oci}}$ is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.116). In general, its value can be given by [17]

$$Z_{\text{o-oci}}^x = \frac{Z_{\text{o-x}}}{Y_{\text{in-x}}} Y_{\text{in-sco}}, \tag{3.117}$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance ($Y_{\text{in-sco}}$) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.116).

According to Eq. (3.114) (i.e., Z_{o-o}), the operation in DCM removes the resonant nature of the converter creating a lossless resistor (i.e., $R_{\text{eq}}\sqrt{K/(1-M)}$) at the output of the converter. The damping is so high that the poles of the converter are well separated and can be given by

$$\begin{aligned} s_{\text{p-low}} &\approx \frac{R_{\text{eq}}}{C(1-M)}, \\ s_{\text{p-high}} &\approx \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}}. \end{aligned} \quad (3.118)$$

3.5.2 Boost Converter

The power stage and the topological subcircuit structures are given in Section 3.3.1 (cf. Figures 3.8 and 3.9). The averaged state space can be derived based on Eqs (3.16–3.18), and (3.108) as already explained. This process yields

$$\begin{aligned} \frac{d\langle i_L \rangle}{dt} &= \frac{d((r_d + r_C - r_{\text{ds1}})\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle + V_D)}{L} \\ &\quad - \frac{2\langle i_L \rangle}{dT_s} \cdot \frac{(r_L + r_d + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C\langle i_o \rangle + V_D - \langle v_{\text{in}} \rangle}{\langle u_{\text{in}} \rangle - (r_L + r_{\text{ds1}})\langle i_L \rangle}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{d^2 T_s}{2LC} (\langle v_{\text{in}} \rangle - (r_L + r_{\text{ds1}})\langle i_L \rangle) - \frac{\langle i_o \rangle}{C}, \\ \langle i_{\text{in}} \rangle &= \langle i_L \rangle, \\ \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}. \end{aligned} \quad (3.119)$$

The operation in DCM will actually remove the resonant behavior of the converter, and therefore, the parasitic loss elements of the power-stage component do not affect much on the dynamics of the converter but only on the operation point. The ESR of the output capacitor (r_C) is left in the state space, because it has a fundamental effect on the output dynamics in terms of load transient response and stability [1]. Therefore, the parasitic elements are usually omitted from the state space, which yields a simplified and more convenient averaged state space as follows:

$$\begin{aligned} \frac{d\langle i_L \rangle}{dt} &= \frac{d\langle v_C \rangle}{L} - \frac{2\langle i_L \rangle(\langle v_C \rangle - \langle v_{\text{in}} \rangle)}{dT_s \langle u_{\text{in}} \rangle}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{d^2 T_s \langle v_{\text{in}} \rangle}{2LC} - \frac{\langle i_o \rangle}{C}, \\ \langle i_{\text{in}} \rangle &= \langle i_L \rangle, \\ \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}. \end{aligned} \quad (3.120)$$

The accurate operation point can be derived from Eq. (3.119) by setting the derivatives to zero. When omitting the parasitic loss elements in Eq. (3.119) (i.e., by using Eq. (3.120)) and utilizing the denotations M , K , and R_{eq} as defined, the operating point and the linearized state space can be given by

$$\begin{aligned} I_L &= MI_o, \\ I_{in} &= MI_o, \\ V_o &= V_C, \\ M &= \frac{1 + \sqrt{1 + (4D^2/K)}}{2}, \quad D = \sqrt{KM(M-1)}, \quad D_1 = \frac{1}{M-1}. \end{aligned} \quad (3.121)$$

$$\begin{aligned} \frac{d\hat{i}_L}{dt} &= -\frac{R_{eq}}{L} \sqrt{\frac{K(M-1)}{M}} \cdot \hat{i}_L - \frac{1}{L} \sqrt{\frac{KM}{M-1}} \cdot \hat{v}_C + \frac{M^2}{L} \sqrt{\frac{KM}{M-1}} \cdot \hat{v}_{in} + \frac{2V_o}{L} \cdot \hat{d}, \\ \frac{d\hat{v}_C}{dt} &= \frac{\hat{i}_L}{C} - \frac{M(M-1)}{R_{eq}C} \cdot \hat{v}_{in} - \frac{\hat{i}_o}{C} - \frac{2V_o}{R_{eq}C} \sqrt{\frac{M-1}{KM}} \cdot \hat{d}, \\ \hat{i}_{in} &= \hat{i}_L, \\ \hat{v}_o &= \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt}. \end{aligned} \quad (3.122)$$

The set of transfer functions corresponding to Eq. (3.31) can be given by

$$\begin{aligned} \Delta Y_{in-o} &= \frac{M^2}{L} \sqrt{\frac{KM}{M-1}} \left(s + \frac{M-1}{MR_{eq}C} \right), \\ \Delta T_{oi-o} &= \frac{1}{LC} \sqrt{\frac{KM}{M-1}}, \\ \Delta G_{ci-o} &= \frac{2V_o}{L} \left(s + \frac{1}{R_{eq}C} \right), \\ \Delta G_{io-o} &= \left(\frac{2M-1}{LC} \sqrt{\frac{KM}{M-1}} - s \cdot \frac{M(M-1)}{R_{eq}C} \right) \cdot (1 + sr_C C), \\ \Delta Z_{o-o} &= \frac{(sL + R_{eq} \sqrt{(K(M-1))/M})(1 + sr_C C)}{LC}, \\ \Delta G_{co-o} &= \frac{2V_{in}(1 - s \cdot (L/R_{eq}) \sqrt{(M(M-1))/K})(1 + sr_C C)}{LC}, \end{aligned} \quad (3.123)$$

where the denominator (Δ) of the transfer functions is

$$\Delta = s^2 + s \cdot \frac{R_{eq}}{L} \sqrt{\frac{K(M-1)}{M}} + \frac{1}{LC} \cdot \sqrt{\frac{KM}{M-1}}. \quad (3.124)$$

The special transfer functions can be computed based on Eq. (3.123) by applying Eq. (3.32) yielding

$$\begin{aligned}
 Y_{\text{in-sco}} &= \frac{M^2 \sqrt{KM/(M-1)}}{sL + R_{\text{eq}} \sqrt{K(M-1)}/M}, \\
 Y_{\text{in-}\infty} &= \frac{M \sqrt{KM/(M-1)}}{sL - R_{\text{eq}} \sqrt{K/(M(M-1))}}, \\
 T_{\text{oi-}\infty} &= \frac{R_{\text{eq}} \sqrt{KM/(M-1)}}{sL - R_{\text{eq}} \sqrt{K/(M(M-1))}}, \\
 Z_{\text{o-oci}}^{\text{o}} &= \frac{R_{\text{eq}} M (1 + sr_C C)}{sR_{\text{eq}} CM + M - 1}, \\
 Z_{\text{o-}\infty} &= \frac{R_{\text{eq}} (1 + sr_C C)}{sR_{\text{eq}} C + 1}, \\
 G_{\text{io-}\infty} &= \frac{M(1 + sr_C C)}{sR_{\text{eq}} C + 1}.
 \end{aligned} \tag{3.125}$$

The special output impedance $Z_{\text{o-oci}}$ is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.125). In general, its value can be given by [17]

$$Z_{\text{o-oci}}^x = \frac{Z_{\text{o-x}}}{Y_{\text{in-x}}} Y_{\text{in-sco}}, \tag{3.126}$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance ($Y_{\text{in-sco}}$) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.125).

According to Eq. (3.123) (i.e., $Z_{\text{o-o}}$), the operation in DCM removes the resonant nature of the converter creating a lossless resistor (i.e., $R_{\text{eq}} \sqrt{K(M-1)}/M$) at the output of the converter. The damping is so high that the poles of the converter are well separated and can be given by

$$\begin{aligned}
 s_{\text{p-low}} &\approx \frac{M}{R_{\text{eq}} C (M - 1)}, \\
 s_{\text{p-high}} &\approx \frac{R_{\text{eq}}}{L} \sqrt{\frac{K(M-1)}{M}}.
 \end{aligned} \tag{3.127}$$

According to Eq. (3.123), the output-control dynamics (i.e., $G_{\text{co-o}}$) contains an RHP zero at

$$\omega_{\text{z-RHP}} \approx \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{M(M-1)}} = \frac{2}{DT_s}, \tag{3.128}$$

which locates at much higher frequency than the corresponding zero in the converter operating in CCM. Therefore, the DCM RHP zero does not limit the control bandwidth in practice.

3.5.3 Buck–Boost Converter

The power stage and the topological subcircuit structures are given in Section 3.3.1 (cf. Figures 3.10 and 3.11). The averaged state space can be derived based on Eqs. (3.21–3.26), and (3.108) as already explained. This process yields

$$\begin{aligned}\frac{d\langle i_L \rangle}{dt} &= \frac{d((r_d + r_C - r_{ds1})\langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle + V_D + \langle v_{in} \rangle)}{L} \\ &\quad - \frac{2\langle i_L \rangle}{dT_s} \cdot \frac{(r_L + r_d + r_C)\langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle + V_D}{\langle v_{in} \rangle - (r_L + r_{ds1})\langle i_L \rangle}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{d^2 T_s}{2LC} (\langle v_{in} \rangle - (r_L + r_{ds1})\langle i_L \rangle) - \frac{\langle i_o \rangle}{C}, \\ \langle i_{in} \rangle &= \frac{d^2 T_s}{2L} (\langle v_{in} \rangle - (r_L + r_{ds1})\langle i_L \rangle), \\ \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.\end{aligned}\tag{3.129}$$

The operation in DCM will actually remove the resonant behavior of the converter, and therefore, the parasitic loss elements of the power-stage component do not affect much on the dynamics of the converter but only on the operation point. The ESR of the output capacitor (r_C) is left in the state space, because it has a fundamental effect on the output dynamics in terms of load transient response and stability [1]. Therefore, the parasitic elements are usually omitted from the state space, which yields a simplified and more convenient averaged state space as follows:

$$\begin{aligned}\frac{d\langle i_L \rangle}{dt} &= \frac{d(\langle v_C \rangle + \langle v_{in} \rangle)}{L} - \frac{2\langle i_L \rangle \langle v_C \rangle}{dT_s \langle v_{in} \rangle}, \\ \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{d^2 T_s \langle v_{in} \rangle}{2LC} - \frac{\langle i_o \rangle}{C}, \\ \langle i_{in} \rangle &= \frac{d^2 T_s \langle v_{in} \rangle}{2L}, \\ \langle v_o \rangle &= \langle v_C \rangle + r_C C \frac{d\langle v_C \rangle}{dt}.\end{aligned}\tag{3.130}$$

The accurate operation point can be derived from (3.128) by setting the derivatives to zero. When omitting the parasitic loss elements in Eq. (3.128) (i.e., by using Eq. (3.129)) and utilizing the denotations M , K , and R_{eq} as defined,

the operating point and the linearized state space can be given by

$$\begin{aligned}
 I_L &= (1 + M)I_o, \\
 I_{in} &= MI_o, \\
 V_o &= V_C, \\
 M &= \frac{D}{\sqrt{K}}, \quad D = M\sqrt{K}, \quad D_1 = \sqrt{K}.
 \end{aligned} \tag{3.131}$$

$$\begin{aligned}
 \frac{d\hat{i}_L}{dt} &= -\frac{R_{eq}\sqrt{K}}{L}\hat{i}_L - \frac{\sqrt{K}}{L}\hat{v}_C + \frac{M(M+2)\sqrt{K}}{L}\hat{v}_{in} + \frac{2(V_{in} + V_o)}{L}\hat{d}, \\
 \frac{d\hat{v}_C}{dt} &= \frac{1}{C}\hat{i}_L - \frac{M^2}{R_{eq}C}\hat{v}_{in} - \frac{1}{C}\hat{i}_o - \frac{2V_o}{R_{eq}C\sqrt{K}}\hat{d}, \\
 \hat{i}_{in} &= \frac{M^2}{R_{eq}}\hat{v}_{in} + \frac{2V_o}{R_{eq}\sqrt{K}}\hat{d}, \\
 \hat{v}_o &= \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt}.
 \end{aligned} \tag{3.132}$$

The set of transfer functions corresponding to Eq. (3.31) can be given by

$$\begin{aligned}
 \Delta Y_{in-o} &= \frac{M^2}{R_{eq}} \left(s^2 + s \frac{R_{eq}\sqrt{K}}{L} + \frac{\sqrt{K}}{LC} \right), \\
 \Delta T_{oi-o} &= 0, \\
 \Delta G_{ci-o} &= \frac{2V_o}{R_{eq}} \left(s^2 + s \frac{R_{eq}\sqrt{K}}{L} + \frac{\sqrt{K}}{LC} \right), \\
 \Delta G_{io-o} &= \frac{2M\sqrt{K}}{LC} \left(1 - s \frac{LM}{R_{eq}C\sqrt{K}} \right) (1 + sr_C C), \\
 \Delta Z_{o-o} &= \frac{(sL + R_{eq}\sqrt{K})(1 + sr_C C)}{LC}, \\
 \Delta G_{co-o} &= \frac{2V_{in} \left(1 - s \frac{ML}{R_{eq}\sqrt{K}} \right) (1 + sr_C C)}{LC},
 \end{aligned} \tag{3.133}$$

where the denominator (Δ) of the transfer functions is

$$\Delta = s^2 + s \frac{R_{eq}\sqrt{K}}{L} + \frac{\sqrt{K}}{LC}. \tag{3.134}$$

The special transfer functions can be computed based on Eq. (3.132) by applying Eq. (3.32) yielding

$$\begin{aligned}
 Y_{\text{in-sco}} &= \frac{M^2}{R_{\text{eq}}}, \\
 Y_{\text{in-}\infty} &= \frac{\sqrt{K}}{sLM - R_{\text{eq}}\sqrt{K}}, \\
 T_{\text{oi-}\infty} &= -\frac{M(sL + R_{\text{eq}}\sqrt{K})}{sLM - R_{\text{eq}}\sqrt{K}}, \\
 Z_{\text{o-oci}}^{\text{o}} &= \frac{(sL + R_{\text{eq}}\sqrt{K})(1 + sr_C C)}{s^2LC + sR_{\text{eq}}C\sqrt{K} + \sqrt{K}}, \\
 Z_{\text{o-}\infty} &= \frac{(sL + R_{\text{eq}}\sqrt{K})(1 + sr_C C)}{s^2LC + sR_{\text{eq}}C\sqrt{K} + \sqrt{K}}, \\
 G_{\text{io-}\infty} &= \frac{M\sqrt{K}(1 + sr_C C)}{s^2LC + sR_{\text{eq}}C\sqrt{K} + \sqrt{K}}.
 \end{aligned} \tag{3.135}$$

The special output impedance $Z_{\text{o-oci}}$ is dependent on the state of output voltage feedback. Its open-loop value is given in Eq. (3.135). In general, its value can be given by [17]

$$Z_{\text{o-oci}}^x = \frac{Z_{\text{o-x}}}{Y_{\text{in-x}}} Y_{\text{in-sco}}, \tag{3.136}$$

where the superscript and subscript extension x denotes either the open- “o” or closed- “c” loop transfer function. The short circuit input admittance ($Y_{\text{in-sco}}$) does not depend on the state of feedback [1]. This also applies to all the special transfer functions denoted by subscript extension ∞ in Eq. (3.135).

According to Eq. (3.133) (i.e., $Z_{\text{o-o}}$), the operation in DCM removes the resonant nature of the converter creating a lossless resistor (i.e., $R_{\text{eq}}\sqrt{K}$) at the output of the converter. The damping is so high that the poles of the converter are well separated and can be given by

$$\begin{aligned}
 \omega_{\text{p-low}} &\approx \frac{1}{R_{\text{eq}}C}, \\
 \omega_{\text{p-high}} &\approx \frac{R_{\text{eq}}\sqrt{K}}{L}.
 \end{aligned} \tag{3.137}$$

According to (3.132), the output control dynamics (i.e., $G_{\text{co-o}}$) contains an RHP zero at

$$\omega_{\text{z-RHP}} \approx \frac{R_{\text{eq}}\sqrt{K}}{LM} = \frac{2}{DT_s}, \tag{3.138}$$

which locates at much higher frequency than the corresponding zero in the converter operating in CCM. Therefore, the DCM RHP zero does not limit the control bandwidth in practice.

3.6 Source and Load Interactions

3.6.1 Source Interactions

According to the generalized source interactions given in Section 2.2.5, the source-affected set of transfer functions representing the source-impedance-induced changes in the dynamics of the voltage-fed voltage-output (VF-VO) converter (cf. Figure 3.16) can be given by

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \frac{Y_{in}}{1 + Z_S Y_{in}} & \frac{T_{oi}}{1 + Z_S Y_{in}} & \frac{G_{ci}}{1 + Z_S Y_{in}} \\ \frac{G_{io}}{1 + Z_S Y_{in}} & -\frac{1 + Z_S Y_{in-sco}}{1 + Z_S Y_{in}} Z_o & \frac{1 + Z_S Y_{in-\infty}}{1 + Z_S Y_{in}} G_{co} \end{bmatrix} \begin{bmatrix} \hat{v}_{inS} \\ \hat{v}_o \\ \hat{d} \end{bmatrix}, \quad (3.139)$$

where

$$\begin{aligned} Y_{in-sco} &= Y_{in} + \frac{G_{io} T_{oi}}{Z_o}, \\ Y_{in-\infty} &= Y_{in} - \frac{G_{io} G_{ci}}{G_{co}}. \end{aligned} \quad (3.140)$$

According to Eq. (3.139), the source impedance (Z_S) would interact with the converter via its input impedance (Z_{in}) (i.e., $1 + Z_S Y_{in}$), its short circuit input impedance (Z_{in-sco}) (i.e., $1 + Z_S Y_{in-sco}$), or its ideal input impedance ($Z_{in-\infty}$) (i.e., $1 + Z_S Y_{in-\infty}$), respectively. The interactions via the input impedance would affect all the transfer functions and would be dependent on the state of output-side feedback: When the converter operates at open loop, the usual sign of interactions is a dip in the corresponding internal transfer function. When the converter operates at closed loop, the usual sign of interactions is a peaking in the

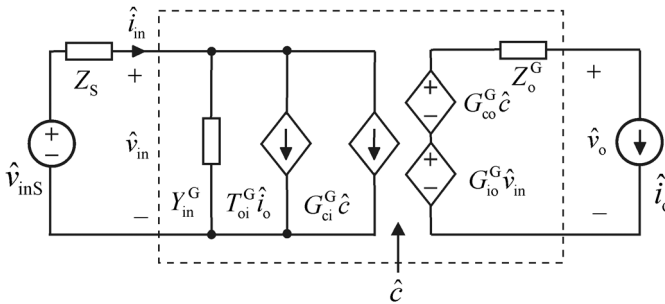


Figure 3.16 Linear network model of VF-VO converter with nonideal source.

corresponding internal transfer functions. As discussed earlier, short circuit and ideal input impedances are invariant to the state of output-side feedback. Therefore, the source interactions caused by the impedance overlap in these impedance ratios would not be removed at closed loop but they have similar effect both at open and closed loop.

The source interactions were first discussed and design rules were developed for preventing the input filter to affecting the dynamics of a converter in Refs [21,22]. In short, the design rules are such that all the above given impedance ratios should be much smaller than 1, which obviously would prevent the source to affect the converter behavior. It has turned out that the source interactions (i.e., especially the input filter-induced interactions) are most likely to take place due to the source impedance overlap with the short circuit input impedance of the converter [23,24].

3.6.2 Input Voltage Feedforward

It is possible to reduce the source interactions by applying input voltage feedforward (IVFF) control scheme, where the PWM-modulator ramp slope is made directly proportional to input voltage [25]. The effect of IVFF control scheme on the converter dynamic behavior can be found by means of the control block diagrams given in Figure 3.17, where F_m and q_{in} denote the duty-ratio gain and IVFF gain. Based on Figure 3.17, the set of transfer functions can be given by

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} - F_m q_{in} G_{ci-o} & T_{oi-o} & F_m G_{ci-o} \\ G_{io-o} - F_m q_{in} G_{co-o} & -Z_{o-o} & F_m G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{inS} \\ \hat{v}_o \\ \hat{d} \end{bmatrix}. \quad (3.141)$$

According to Eq. (3.141), the input-to-output attenuation (G_{io-o}) can be made high by designing $F_m q_{in} = G_{io-o}/G_{co-o}$. It may be obvious that in order to implement theoretically perfect IVFF-control scheme, G_{io-o} and G_{co-o} should have the same zeros. In a buck converter, this condition is valid (cf. Section 3.4.1, Eq. (3.40)) yielding the required gain product $F_m q_{in} = D/V_e \approx D/V_{in}$. If the IVFF-control scheme is implemented in a DDR buck converter, the set of transfer functions becomes

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} - \frac{G_{io-o} G_{ci-o}}{G_{co-o}} & T_{oi-o} & F_m G_{ci-o} \\ 0 & -Z_{o-o} & F_m G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{v}_{co} \end{bmatrix}. \quad (3.142)$$

Equation (3.142) shows that the converter input admittance equals the ideal input admittance. According to Eq. (3.140), we can also state that all the input admittances would equal the ideal input admittance. As a consequence, the source interactions would be greatly reduced.

The IVFF-control scheme can be implemented as shown in Figure 3.18. According to it, the duty ratio is determined when $v_{co} = kv_{in}dT_s$. According

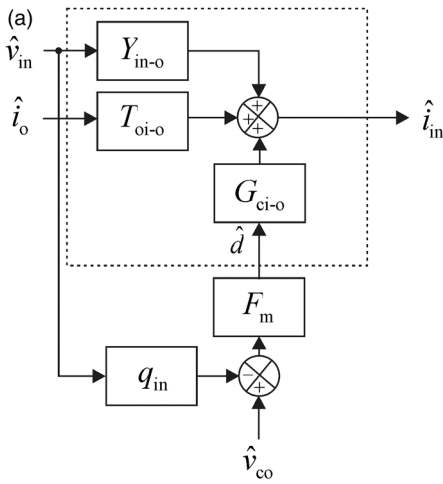


Figure 3.17 Control block diagrams for assessing the effect of IVFF-control scheme on (a) input dynamics and (b) output dynamics.

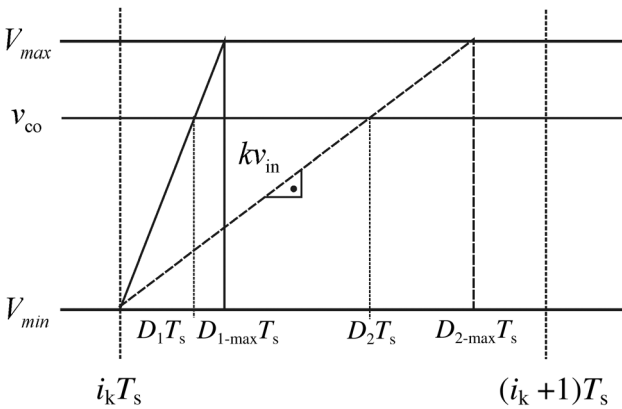
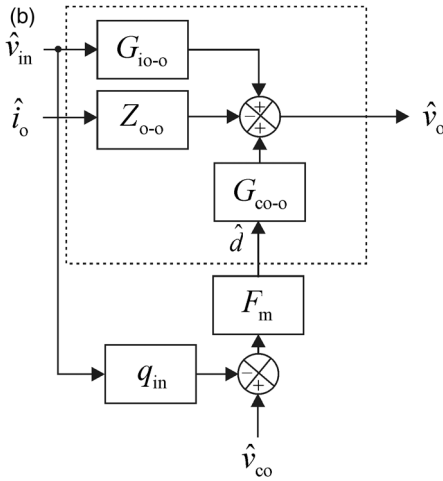


Figure 3.18 Duty-ratio generation under IVFF-control scheme.

to this relation, the small-signal duty-ratio constraints can be computed to be

$$\hat{d} = \frac{1}{kV_{in}T_s}(\hat{v}_{co} - kDT_s\hat{v}_{in}) = F_m(\hat{v}_{co} - q_{in}\hat{v}_{in}), \tag{3.143}$$

which gives $F_m q_{in} = D/V_{in}$ as required for $G_{io-o} \approx 0$.

The constant k is designed in such a manner that the duty ratio is close to 100% at a certain minimum input voltage (V_{in-min}) (cf. Figure 3.18: $D \approx D_{2-max}$). According to this assumption, $k = V_M/V_{in-min}T_s$, where $V_M = V_{max} - V_{min}$. Thus, $F_m = V_{in-min}/V_M V_{in}$ and $q_{in} = DV_M/V_{in-min}$. This means, in case of buck converter, the input and output control dynamics (i.e., G_{ci-o} and G_{co-o}) (cf. Section 3.4.1, Eq. (3.40)) are not anymore dependent on the input voltage level as in the original buck converter. The duty-ratio gain F_m can also be constructed so that it includes the normal modulator gain (G_a) and the additional part coming from the IVFF-control scheme as $F_m = G_a F'_m$, where $G_a = 1/V_M$ (cf. Section 3.2, Eq. (3.3)) and $F'_m = V_{in-min}/V_{in}$ show explicitly the effect of the scheme on the control dynamics.

3.6.3 Load Interactions

According to the generalized load interactions given in Section 2.2.5, the load-affected set of transfer functions representing the load impedance-induced changes in the dynamics of the VF-VO converter (cf. Figure 3.19) can be given by

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \frac{1 + Y_L Z_{in-oci}}{1 + Z_o Y_L} Y_{in} & \frac{T_{oi}}{1 + Z_o Y_L} & \frac{1 + Y_L Z_{o-\infty}}{1 + Z_o Y_L} G_{ci} \\ \frac{G_{io}}{1 + Z_o Y_L} & -\frac{Z_o}{1 + Z_o Y_L} & \frac{G_{co}}{1 + Z_o Y_L} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{oL} \\ \hat{d} \end{bmatrix}, \tag{3.144}$$

where

$$\begin{aligned} Z_{on-oci} &= Z_o + \frac{G_{io} T_{oi}}{Y_{in}}, \\ Z_{o-\infty} &= Z_o + \frac{T_{oi} G_{co}}{G_{ci}}. \end{aligned} \tag{3.145}$$

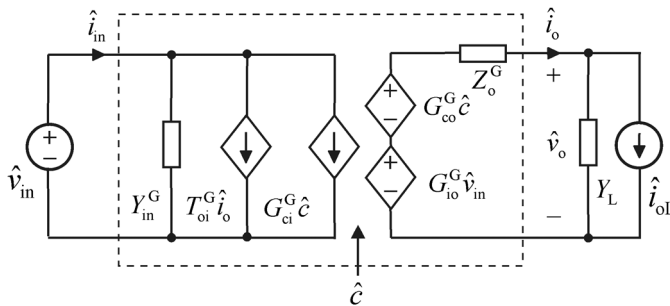


Figure 3.19 Linear network model of VF-VO converter with nonideal load.

According to Eq. (3.144), the load impedance (Z_L) would interact with the converter via its output impedance (Z_o) (i.e., $1 + Z_o Y_L$), its open-circuit output impedance (Z_{o-oci}) (i.e., $1 + Y_L Z_{o-oci}$), or its ideal output impedance ($Z_{o-\infty}$) (i.e., $1 + Y_L Z_{o-\infty}$), respectively. The interactions via the output impedance would affect all transfer functions and would be dependent on the state of feedback: When the converter operates at open loop, the usual sign of interactions is a dip in the corresponding internal transfer function. When the converter operates at closed loop, the usual sign of interactions is a peaking in the corresponding internal transfer functions. As discussed earlier, open-circuit output impedance is dependent on the state of output-side feedback.

When the IVFF-control scheme is properly implemented, the open-circuit output impedance would equal the output impedance (cf. Eq. (3.143)), which would prevent the load interactions to propagate into the input side. Without the IVFF-control scheme, the resonant load can easily change the behavior of the input impedance, and thereby, make the converter more prone to source impedance interactions [26–28].

3.6.4 Output-Current Feedforward

According to Eq. (3.144), we may conclude that the load impedance-induced interactions would be greatly reduced if the output impedance can be made to equal zero. In theory, the reduction of open-loop output impedance down to zero is possible by means of output-current feedforward (OCFF) [29]. The control-block diagrams for developing the conditions for zero output impedance are given in Figure 3.20, where R_{s2} is the output current sensing resistor and H_c the feedforward gain, respectively.

According to Figure 3.20, we can compute the set of transfer functions to be

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{oi-o} + R_{s2} H_c G_a G_{ci-o} & G_a G_{ci-o} \\ G_{io-o} & -(Z_{o-o} - R_{s2} H_c G_a G_{co-o}) & G_a G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{v}_{co} \end{bmatrix}, \quad (3.146)$$

which indicates that the OCFF-control scheme affects only the output impedance (Z_{o-o}) and the reverse transfer function (T_{oi-o}), because G_a is the required modulator gain to adapt the control voltage to the internal control variable (cf. Section 3.2, Eq. (3.3)).

The aim of the OCFF-control scheme is to produce zero open-loop output impedance. Therefore, $Z_{o-o} - R_{s2} H_c G_a G_{co-o} = 0$. As a consequence, the feedforward gain should be designed as

$$H_c = \frac{1}{R_{s2} G_a} \cdot \frac{Z_{o-o}}{G_{co-o}}. \quad (3.147)$$

It may be obvious that the required feedforward gain can be implemented only if the output dynamics is of minimum phase (i.e., G_{co-o} does not contain RHP zeros). Thus, the conventional buck converter is the only prospective

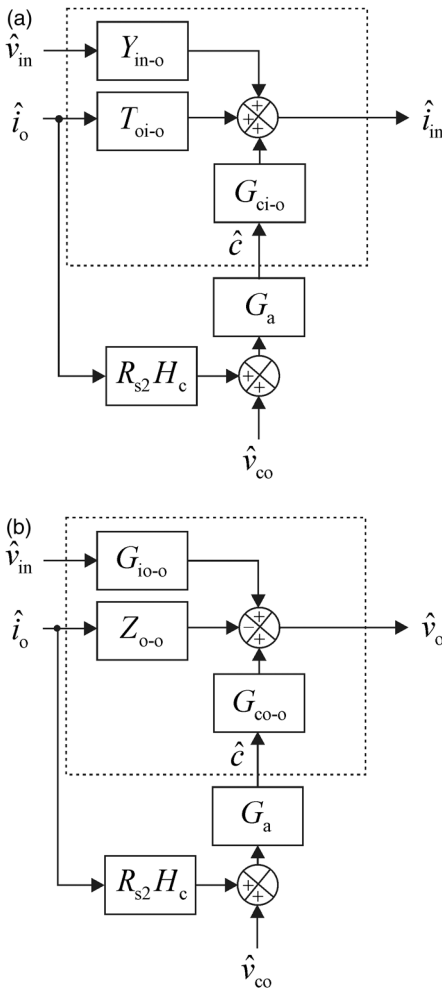


Figure 3.20 Control block diagrams for assessing the effect of OCF control scheme on (a) input dynamics and (b) output dynamics.

candidate. In case of the DDR buck converter (cf. Eq. (3.40)), the required gain becomes

$$H_c = \frac{V_M}{V_e} \cdot \frac{sL + r_e - r_C}{R_{s2}} \approx \frac{V_M}{V_{in}} \cdot \frac{sL}{R_{s2}}, \quad (3.148)$$

which is practically impossible to be implemented. The implementation will be, however, possible when the buck converter operates under PCM control [29].

If the zero-output impedance condition in Eq. (3.147) is fully implemented, the set of transfer functions in Eq. (3.146) would be

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{oi-o} + \frac{Z_{o-o} G_{ci-o}}{G_{co-o}} & G_a G_{ci-o} \\ G_{io-o} & 0 & G_a G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{v}_{co} \end{bmatrix}. \quad (3.149)$$

According to Eq. (3.149), the reverse transfer function would equal $T_{oi-\infty}$. In addition, the short circuit input admittance would be infinitely high (cf. Eq. (3.32)). This actually means that the output impedance would be always at open and closed loop as

$$Z_o = \frac{G_{io}T_{oi}}{1 + Z_s Y_{in}} Z_s, \quad (3.150)$$

because of the source effects given in Eq. (3.139). Therefore, the zero-output impedance condition would be possible only when $G_{io} = 0$.

3.7 Impedance-Based Stability Issues

The impedance-based stability analysis was originally developed for preventing the input filter to affect the dynamics of the associated converter in Refs [21,22]. The minor-loop concept has been later generalized to be applicable for an arbitrary system interface by stating that the minor-loop gain (i.e., the impedance ratio) shall be constructed in such a manner that the numerator impedance is the impedance of the voltage-type source, and the denominator impedance the impedance of the current-type source [30–33]. The boundary for the instability is naturally according to *Nyquist* stability criterion the state where the minor-loop gain passes through the point $(-1,0)$ in the complex plain. Based on this knowledge and the behavior of the input and output impedances, the sensitivity of a converter to the source and load-induced instability can be easily determined [26,27] by

$$\begin{aligned} Z_S &= |Z_{in}| \angle \varphi_{Z_{in}} + 180^\circ, \\ Z_L &= |Z_o| \angle \varphi_{Z_o} - 180^\circ, \end{aligned} \quad (3.151)$$

which are applicable for the VF-VO converters treated in this chapter.

Figure 3.22 shows the measured closed-loop input and output impedance of a conventional buck converter (cf. Figure 3.21). According to the phase behavior of

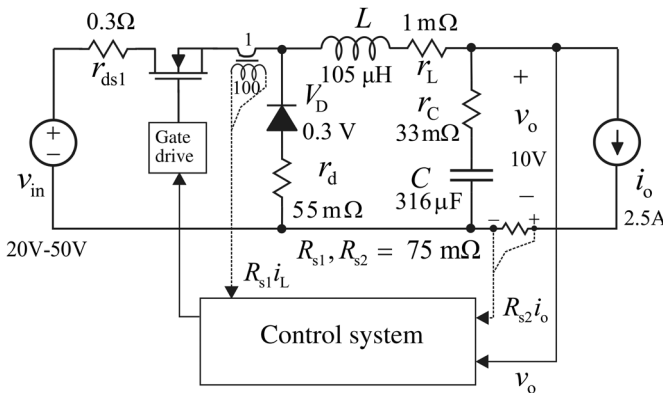


Figure 3.21 The power stage of the experimental buck converter.

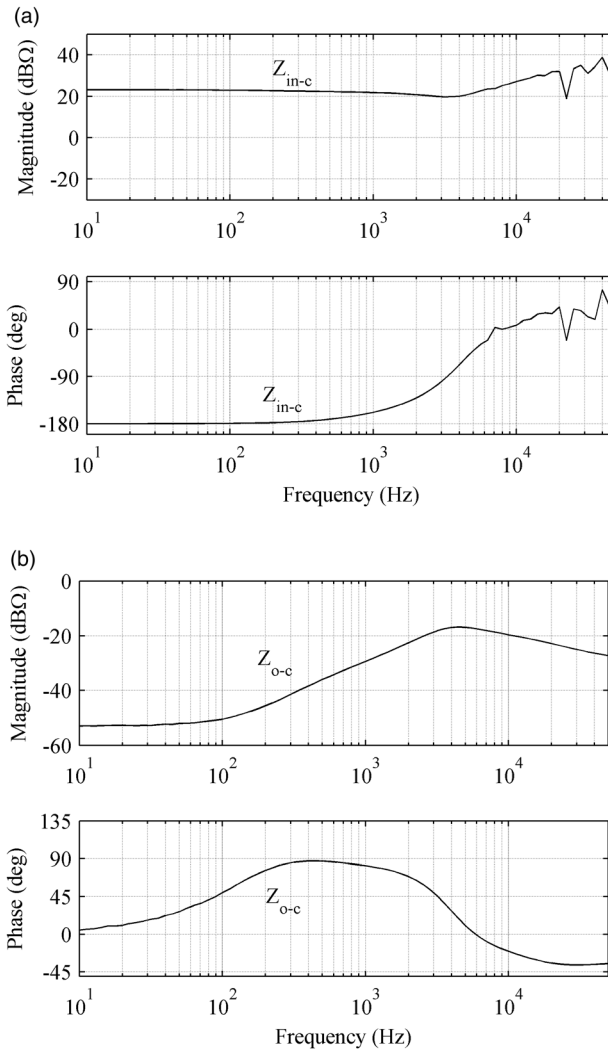


Figure 3.22 The measured closed-loop (a) input impedance and (b) output impedance of a buck converter.

the input impedance (cf. Figure 3.22a), the converter will be prone to instability when the phase of the source impedance equals 0–90°. The corresponding frequency range reaches up to 30 kHz. The appearing of instability requires the existence of parallel resonant circuit in the source side. Such a typical circuit is naturally an input EMI filter. According to the phase behavior of the output impedance (cf. Figure 3.22b), the converter is prone to instability at the frequencies from 300 to 600 Hz when capacitive load is connected at its output terminal. The instability may also take place if the converter is loaded by a regulated

converter with an input LC filter close to its resonant frequency (i.e., the series resonance of the filter). Similar conclusions can always be made when the behavior of the impedances are known.

3.8 Dynamic Review

The dynamic models derived for the DDR-controlled converters are known to be very accurate up to half the switching frequency when the modeling is correctly done and all the vital elements are taken into account, as demonstrated explicitly in Refs [1,33]. Therefore, we concentrate in this section to certain issues, which are not so well understood. The experimental buck converter applied to produce the phenomena described later is shown in Figure 3.22. The experiments are performed at the stated minimum input voltage and output power. The converter is equipped with an input filter having resonant frequency of 500 Hz and also 500 Hz resonant load for demonstrating the source and load interactions.

Figure 3.23 shows all the measured and computationally solved (Z_{in-sco}) input impedances of the converter, where Z denotes the output impedance of the input filter. According to it, there is an overlap of the source and open-loop input impedances. According to the source interactions in (3.139) and taking into account the operation at open loop, the overlap means that there will be a dip in the output voltage loop gain (i.e., G_{co-o}), which is also visible in Figure 3.24. The overlap of the source and short-circuit impedances mean that both the open and closed-loop output impedances will be affected, as explicitly shown in Figure 3.25. As a consequence, the load-transient response is also affected, as clearly visible in Figure 3.26. The decaying oscillation resembles the

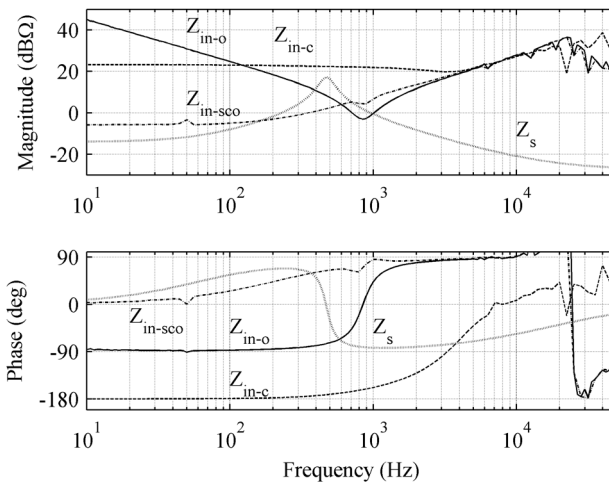


Figure 3.23 The measured input impedances.

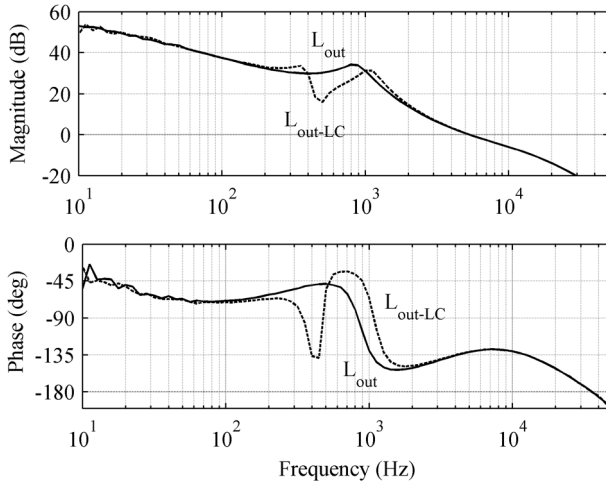


Figure 3.24 The measured output voltage loop gains.

oscillation caused by the poor phase or gain margins in the output voltage loop gain but the margins are not changed, as can be concluded from Figure 3.24. Therefore, this phenomenon cannot be removed by control design but only by providing sufficient damping to the input filter. Figure 3.23 shows that the converter is stable because there is no overlap between the source and closed-loop input impedances.

Figure 3.27 shows the measured and computationally solved (Z_{o-oci}^x) output impedances, where the resonant load is denoted by Z_L . It indicates that there are

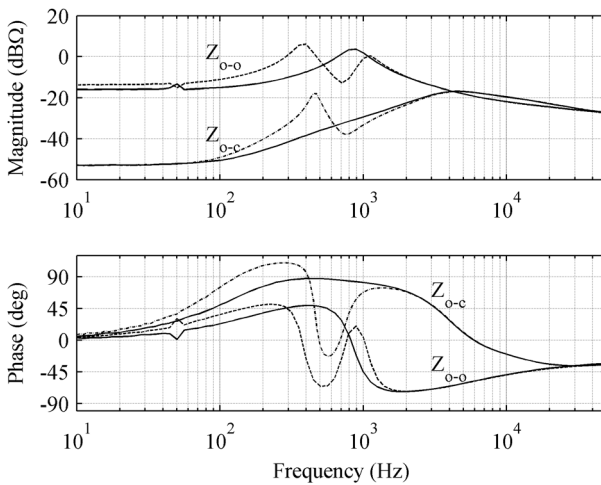


Figure 3.25 The measured open- and closed-loop output impedances.

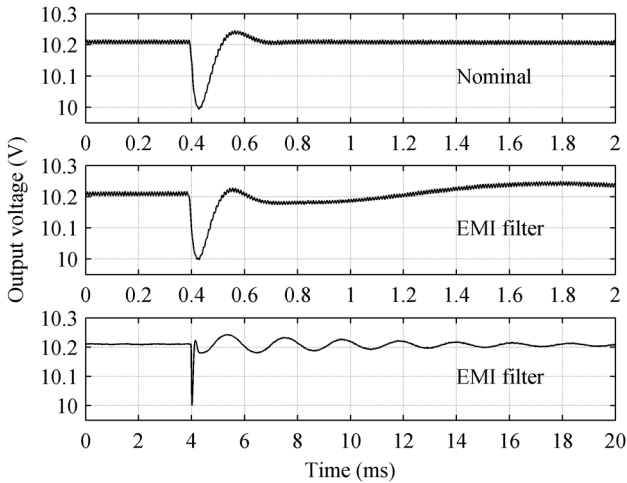


Figure 3.26 Output-voltage response to a step change in the output current without and with the input filter.

overlaps between the load and open-loop output impedances as well as the load and open-circuit output impedances. These overlaps mean (cf. Eq. (3.144)) that the output voltage loop gain and the input impedance are affected. The converter is, however, clearly stable because there is no overlap between the load and closed-loop output impedances.

Figure 3.28 shows the measured input impedances when the resonant load is connected. Because of the overlap between the load and open-circuit output impedances both the open-loop and closed-loop input impedances are affected. The figure shows that the converter is now very close to instability, because the

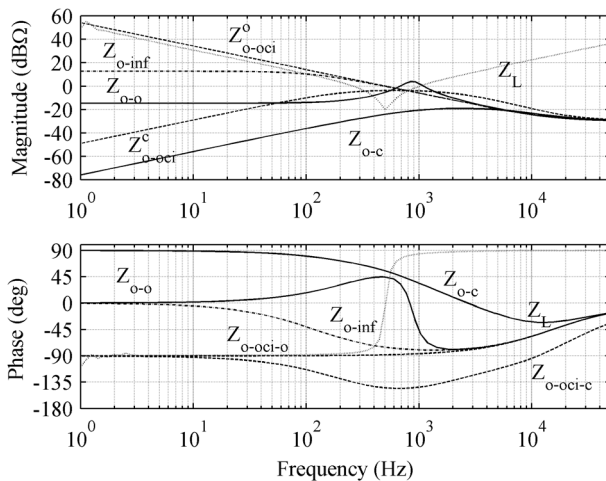


Figure 3.27 The measured and computationally solved output impedances.

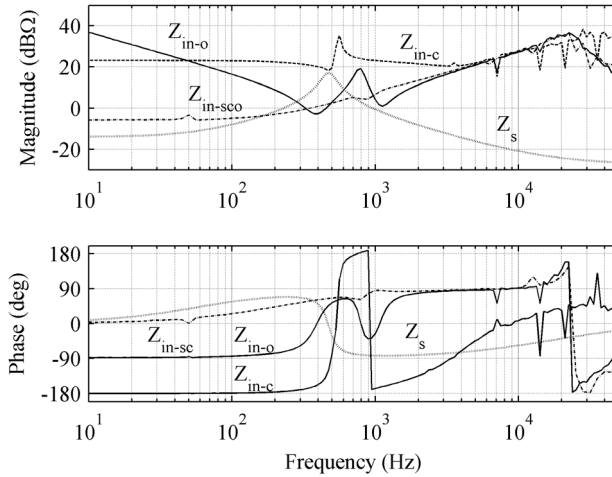


Figure 3.28 The measured input impedance when a resonant load is connected at the output of the converter.

source impedance is very close to the affected closed-loop input impedance when the input filter is connected. This is also evident when studying the output voltage loop gains in Figure 3.29 and the output voltage load responses in Figure 3.30.

Figure 3.31 shows the measured and computationally solved input impedances of the IVFF-controlled buck converter. The power stage of the converter is the same as presented in Figure 3.21. It may be obvious that the open-loop

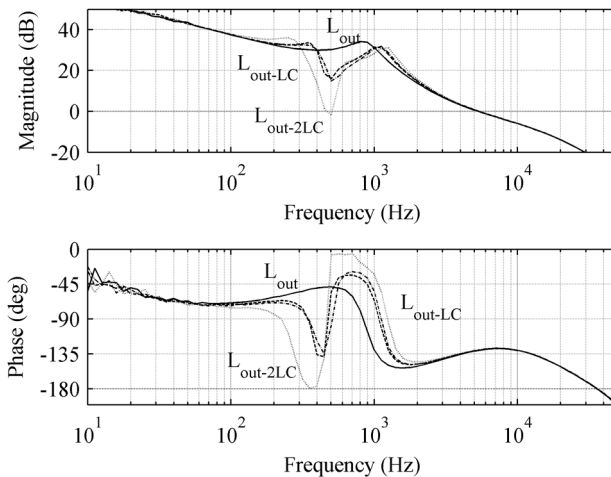


Figure 3.29 The measured output voltage loop gains when the resonant circuits are connected at the input and output terminals.

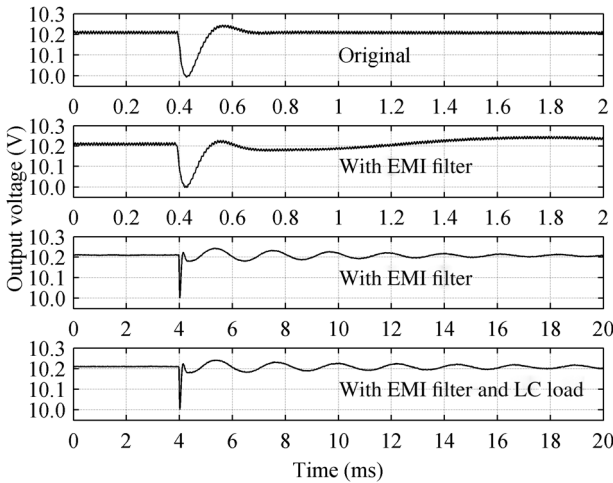


Figure 3.30 The output-voltage responses to a step change in the load current when the resonant circuits are connected at the input and output terminals.

and short circuit input impedances are changed profoundly from that of the original converter (cf. Figure 3.23), as discussed in Section 3.6.2. As a consequence, the source interactions are expected to be reduced significantly. Figures 3.32 and 3.33 confirm this clearly. It should also be observed (cf. Figure 3.31), the open- and closed-loop input impedances resemble negative incremental resistance at a wide frequency range. Therefore, the converter can also be unstable due to source interactions even at open loop, which the original converter hardly is.

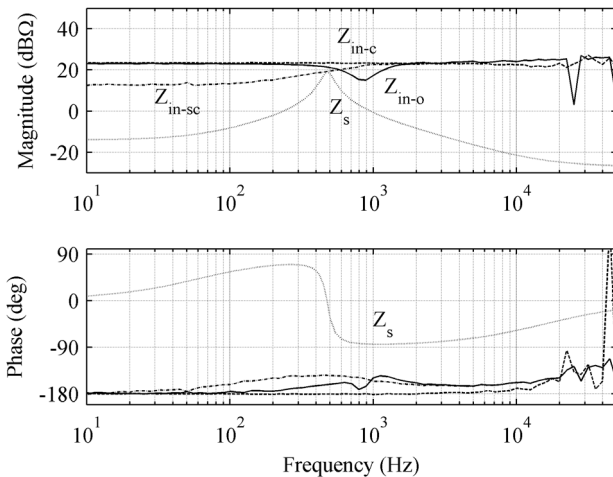


Figure 3.31 The measured and computationally solved input impedances of the IVFF converter.

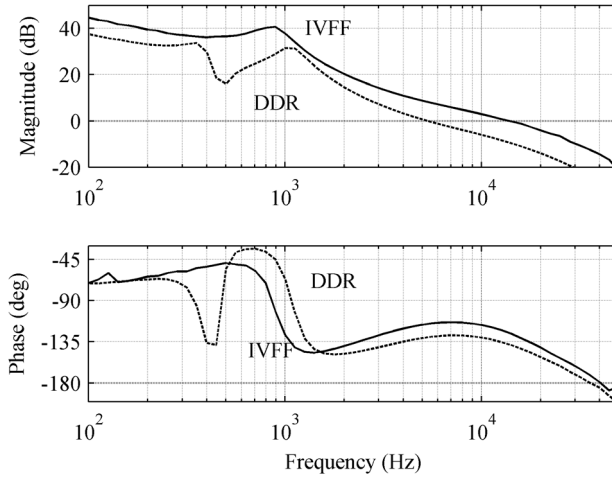


Figure 3.32 The measured output voltage loop gains of the DDR and IVFF converters.

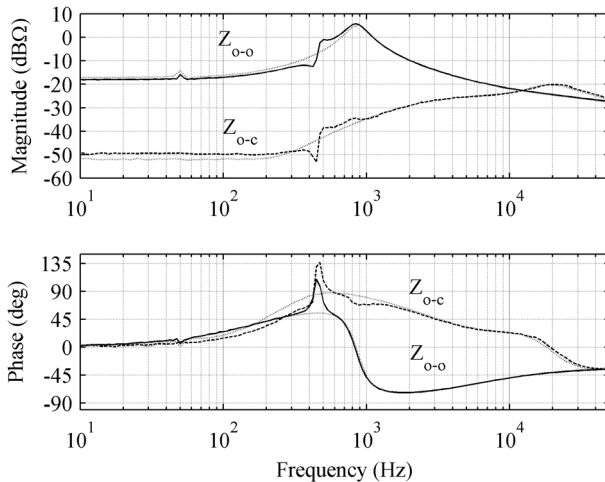


Figure 3.33 The measured output impedances of the IVFF converter.

References

- 1 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters – Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.
- 2 Erickson, R.W. and Maksimović, D. (2001) *Fundamentals of Power Electronics*, Kluwer Academic Publishers, Norwell, MA.
- 3 Wester, G.W. and Middlebrook, R.D. (1973) Low-frequency characterization of switched dc-dc converters. *IEEE Trans. Aerosp. Electron. Syst.*, **AES-9** (3), 376–385.

- 4 Middlebrook, R.D. and Čuk, S. (1977) A general unified approach to modeling switching-converter power stages. *Int. J. Electron.*, **42** (6), 521–550.
- 5 Čuk, S. and Middlebrook, R.D. (1977) A general unified approach to modelling switching DC-to-DC converters in discontinuous conduction mode, Proceeding of the IEEE PESC, pp. 36–57.
- 6 Sun, J., Mitchell, D.M., Gruel, M.F., Krein, P.T., and Bass, R.M. (2001) Average modeling of PWM converters in discontinuous modes. *IEEE Trans. Power Electron.*, **16** (4), 482–492.
- 7 Suntio, T. (2006) Unified average and small-signal modeling of direct-on-time control. *IEEE Trans. Ind. Electron.*, **53** (1), 287–295.
- 8 Tse, C.K. (2004) *Complex Behavior of Switching Power Converters*, CRC Press, Boca Raton, FL.
- 9 Banerjee, S. and Verghese, G.C. (2001) *Nonlinear Phenomena in Power Electronics*, IEEE Press, Inc., New York, NY.
- 10 Sun, J. (2002) Small-signal modeling of variable-frequency pulsewidth modulators. *IEEE Trans. Aerosp. Electron. Syst.*, **38** (3), 1104–1108.
- 11 Mitchell, D.M. (1980) Pulsewidth modulator phase shift. *IEEE Trans. Aerosp. Electron. Syst.*, **AES-16** (3), 272–278.
- 12 Karppanen, M., Sippola, M., and Suntio, T. (2008) Methods to characterize open-loop dynamics of current-mode-controlled converters, Proceeding of the IEEE PESC, pp. 636–642.
- 13 Karppanen, M., Arminen, J., Suntio, T., Savela, K., and Simola, J. (2008) Dynamical modeling and characterization of peak-current-mode-controlled superbuck converter. *IEEE Trans. Power Electron.*, **23** (3), 1370–1380.
- 14 Weaver, W.W. and Krein, P.T. (2007) Analysis and applications of a current-sourced buck converter, Proceeding of the IEEE APEC, pp. 1664–1670.
- 15 Veerachary, M. (2005) Two-loop voltage-mode control of coupled-inductor step-down buck converter. *IEE Electric Power Appl.*, **152** (6), 1516–1524.
- 16 Capel, A., Spruyt, H., Windberg, A., O’Sullivan, D., Crausaz, A., and Marpinard, J.C. (1988) A versatile zero ripple converter, Proceeding of the IEEE PESC, pp. 133–141.
- 17 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Effect of control method on impedance-based interactions in a buck converter. *IEEE Trans. Power Electron.*, **28** (11), 5311–5322.
- 18 Karppanen, M., Arminen, J., Suntio, T., Savela, K., and Simola, J. (2008) Dynamical modeling and characterization of peak-current-mode-controlled superbuck converter. *IEEE Trans. Power Electron.*, **23** (3), 1370–1380.
- 19 Huusari, J., Leppäaho, J., and Suntio, T. (2010) Dynamic properties of PCM-controlled superbuck converter – Discrete vs. coupled inductor implementation. *Eur. Power Electron. Drives J.*, **20** (2), 8–15.
- 20 Čuk, S. (1983) A new zero-ripple DC-to-DC converter and integrated magnetics. *IEEE Trans. Magn.*, **MAG-19** (2), 57–75.
- 21 Middlebrook, R.D. (1976) Input filter considerations in design and applications of switching regulators. Proceedings of the IEEE Industry Applications Society Annual Meeting, pp. 91–107.

- 22 Middlebrook, R.D. (1978) Design techniques for preventing input-filter oscillations in switched-mode regulators, Proceeding of the Power Conversion Conference, pp. A3.–A3.16.
- 23 Suntio, T. and Karppanen, M. (2009) The short-circuit input impedance as a main source of input-filter interactions in a regulated converter. *Eur. Power Electron. Drives J.*, **19** (3), 31–40.
- 24 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Effect of control method on impedance-based interactions in a buck converter. *IEEE Trans. Power Electron.*, **28** (11), 5311–5322.
- 25 Karppanen, M., Suntio, T., and Sippola, M. (2007) Dynamical characterization of input-voltage-feedforward-controlled buck converter. *IEEE Trans. Ind. Electron.*, **54** (2), 1005–1013.
- 26 Suntio, T., Hankaniemi, M., and Karppanen, M. (2006) Analysing the dynamics of regulated converters. *IEE Proc. Electric Power Appl.*, **153** (6), 905–910.
- 27 Hankaniemi, M., Karppanen, M., and Suntio, T. (2006) Load imposed instability and performance degradation in a regulated converter. *IEE Proc. Electric Power Appl.*, **153** (6), 781–786.
- 28 Hankaniemi, M., Karppanen, M., Suntio, T., Altowati, A., and Zenger, K. (2006) Source-reflected load interactions in a regulated converter, Proceeding of the IEEE IECON, pp. 2893–2898.
- 29 Karppanen, M., Hankaniemi, M., Suntio, T., and Sippola, M. (2007) Dynamical characterization of peak-current-mode-controlled buck converter with output current-feedforward. *IEEE Trans. Power Electron.*, **22** (2), 444–451.
- 30 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Impedance-based stability and transient-performance assessment applying maximum peak criteria. *IEEE Trans. Power Electron.*, **28** (5), 2099–2104.
- 31 Sun, J. (2011) Impedance-based stability criterion for grid-connected inverters. *IEEE Trans. Power Electron.*, **26** (11), 3075–3078.
- 32 Leppäaho, J., Huusari, J., Nousiainen, L., Puukko, J., and Suntio, T. (2011) Dynamic properties and stability assessment of current-fed converters in photovoltaic applications. *IEEJ Trans. Ind. Appl.*, **131** (8), 976–984.
- 33 Suntio, T., Viinamäki, J., Jokipii, J., Messo, T., and Kuperman, A. (2014) Dynamic characteristics of power electronic interfaces. *IEEE J. Emerg. Sel. Top. Power Electron.*, **2** (4), 949–961.

4

Dynamic Modeling of Current-Mode Control

4.1 Introduction

This chapter introduces the dynamic modeling of current-mode-controlled (CM) voltage-fed converters. The class of current-mode control includes peak current mode (PCM) control introduced in late 1970s [1], average current mode (ACM) control introduced in early 1990s [2], variable frequency PCM control (i.e., known also as self-oscillation control, boundary-mode control, critical-mode control, transition-mode control, etc.) [3], and hysteretic current-mode control [4,5]. Basically, the modeling of CM control requires developing proper duty ratio constraints, where the perturbed duty ratio is expressed as a function of other circuit variables being part of the duty-ratio generation [6]. The duty-ratio constraints are typically presented in the form

$$\hat{d} = F_m \left(\hat{x}_c - \sum_{i=1}^n q_i \hat{x}_i \right), \quad (4.1)$$

where F_m denotes the duty-ratio gain, x_c the new control variable, and q_i the feedback or feedforward gain related to variable x_i [6]. The modeling is simply carried out by substituting the perturbed duty ratio (\hat{d}) in the DDR small-signal state space, as stated in Eq. (4.1) [7]. The CM transfer functions will be then obtained by proceeding as instructed in Section 2.4. It should be noted that the application of CM control would also change the corresponding converter to a current-output converter. This means that the open-loop converter cannot operate at constant current load, which is required for measuring the internal transfer functions for voltage-output converters. The best option is to use resistive load and solve the required transfer functions computationally applying the load interaction formulation introduced in Section 2.2.5 [8]. If the load effect is not removed, the transfer functions do not describe the internal dynamics at all. The second option is to use a constant voltage source or a storage battery as a load, and measure the transfer functions as is proper for a VF-CO converter. The required transfer functions can be then obtained by interchanging the output and input variable at the output terminal. This topic is shortly discussed in more detail in Chapter 5. The last section of this chapter discusses the usual validation methods of the PCM control, introduces shortly Dr. Ridley's PCM models, and

verifies their accuracy for the basic second-order converters. In addition, the last section shows that the PCM models of this book can be made very accurate by means of a certain high-frequency extension as well.

4.2 Peak Current Mode Control

The first attempt to model the dynamics of PCM-controlled converter was presented in Ref. [9] quite soon after the introduction of the control method [1]. After the first attempt, it was deduced that the sampling effect would produce the phenomenon noticed in the operation of the converter, that is, the subharmonic oscillation limiting the usable duty ratio to 50% without compensation [10]. After these first attempts, a multitude of modeling methods and models have been introduced. The methods presented in Refs [11–14] would actually explain the reason for the mode limit. The most elegant of these methods is presented in Ref. [14], which is also extended to cover the higher order converters [15,16] as well as operation in DCM [17]. The methods described in this book are based on Refs [14] and [17].

The PCM control is very popular both in the nonisolated and transformer-isolated converters. The only exception where the PCM control cannot be used as such is the half-bridge-based capacitively coupled converters [18,19]. The capacitively coupled half-bridge can be, however, modified by adding an extra primary side winding, which has the same number of turns as in the main primary side winding, to balancing the midpoint voltage of the capacitive voltage divider as shown in Figure 4.1.

4.2.1 PCM Control Principles

Under PCM control, the on-time (t_{on}) or duty ratio is generated by comparing the on-time inductor current and the control current (i_{co}) (i.e., $i_{co} = v_{co}/R_s$ in Figure 4.2, where R_s is the equivalent inductor current sensing resistor). In order to extend the duty ratio (d) beyond the mode limit of 50%, the control current has to be compensated by using an artificial ramp (M_c). In practice, the compensation ramp is added to the inductor current signal, but the analysis would be more convenient considering the compensation ramp to be subtracted from the control current, as depicted in Figure 4.2. The duty ratio (d) is established when the inductor current signal reaches the compensated control current (cf. Figure 4.2b).

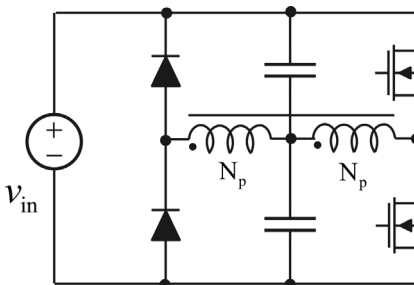


Figure 4.1 Adding a balancing primary side winding for a capacitively coupled half-bridge converter.

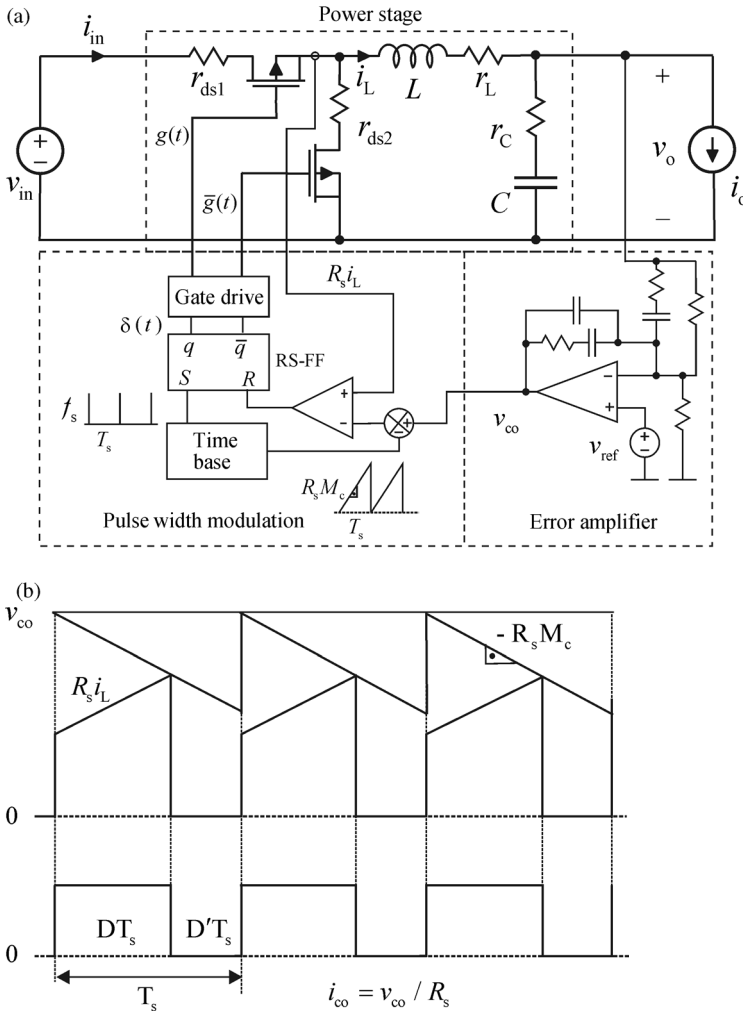


Figure 4.2 PCM control principles. (a) Circuit schematics with a buck converter. (b) Duty-ratio generation.

The state variables and contributors to the dynamic behavior of a converter are the time varying inductor currents, as discussed in Chapter 3. When the inductor currents are used to generate the duty ratio (cf. Figure 4.3), the desired feedback signals would be $\langle i_{Li} \rangle$ but the real duty-ratio generation takes place as illustrated in Figure 4.2. According to Figure 4.3b, we can compute that at $t = (k + d)T_s$, the following holds:

$$\langle i_{co} \rangle - m_c d T_s = \sum_{i=1}^n \langle i_{Li} \rangle + \Delta i_L, \quad (4.2)$$

where Δi_L denotes the difference between the peak inductor current feedback signal and its time-averaged value at $t = (k + d)T_s$. Equation (4.2) is known as

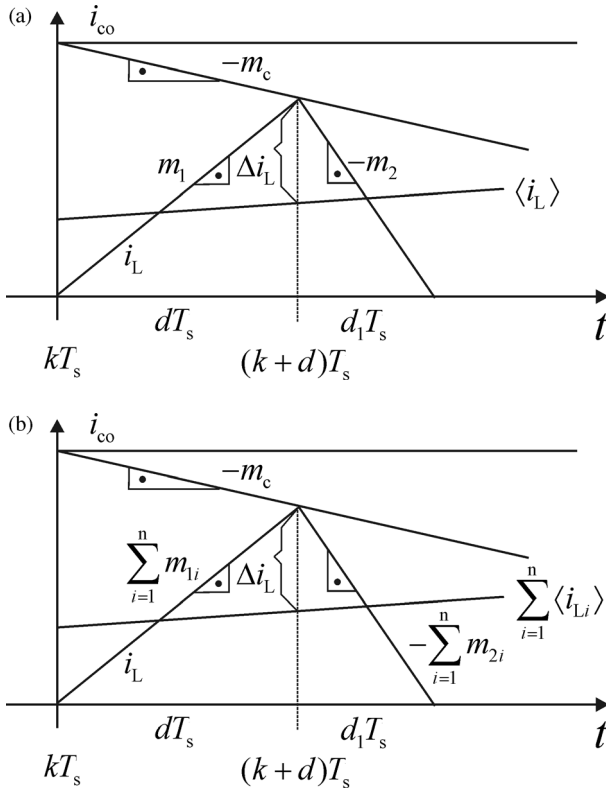


Figure 4.3 Duty-ratio generation under PCM control with (a) single inductor current and (b) multiple inductor currents.

comparator equation due to its physical realization, as shown in Figure 4.2a. This means that the duty-ratio constraints can be determined if Δi_L can be found. It would be obvious that Δi_L would be affected by the operation mode of the converter (i.e., CCM or DCM).

4.2.2 Development of Duty-Ratio Constraints in CCM

In CCM, the time-averaged inductor current $\langle i_L \rangle$ lies exactly in the inductor-current ripple band. Its derivative can be approximated by means of the up and down slopes of the instantaneous inductor current, as given in Chapter 3. Therefore, we can express $\langle i_L \rangle$ by

$$\langle i_L \rangle = (dm_1 - d'm_2)t + \frac{dd'T_s}{2}(m_1 + m_2) + i_L(kT_s), \quad (4.3)$$

where $i_L(kT_s)$ is the value of the time varying averaged inductor current in the beginning of the cycle (cf. Figure 4.3a). More detailed derivation of Eq. (4.3) can be found from Ref. [14]. The on-time instantaneous inductor current i_{L-on}

(cf. Figure 4.3a) can be approximated by

$$i_{L\text{-on}} = m_1 t + i_L(kT_s). \quad (4.4)$$

According to Figure 4.3a, Δi_L can be given by

$$\Delta i_L = i_{L\text{-on}}((k+d)T_s) - \langle i_L((k+d)T_s) \rangle, \quad (4.5)$$

yielding

$$\Delta i_L = \frac{dd'T_s}{2}(m_1 + m_2), \quad (4.6)$$

and the comparator equation as

$$\langle i_{co} \rangle - M_c d T_s = \langle i_L \rangle + \frac{dd'T_s}{2}(m_1 + m_2), \quad (4.7)$$

when the compensation ramp is assumed to be constant. The corresponding duty-ratio constraints in Eq. (4.1) can be developed from Eq. (4.7) by substituting the up and down slopes with the topology-dependent values and linearizing the resulting comparator equation at the defined operating point.

If several inductor currents constitute the feedback signal, the overall $\Delta i_{L\Sigma}$ can be given by

$$\Delta i_{L\Sigma} = \frac{dd'T_s}{2} \sum_{i=1}^n (m_{1i} + m_{2i}), \quad (4.8)$$

and the corresponding comparator equation by

$$\langle i_{co} \rangle - M_c d T_s = \sum_{i=1}^n \left(\langle i_{Li} \rangle + \frac{dd'T_s}{2} (m_{1i} + m_{2i}) \right). \quad (4.9)$$

The comparator equation in Eq. (4.9) facilitates the modeling of the higher order converters, as will be demonstrated later in this chapter by presenting the modeling of the superbuck converter under PCM control based on the DDR state space given in Section 3.3.4.

PCM control is also applied to control the transformer-isolated converters, where the inductor current feedback is usually taken from the primary side containing the secondary side reflected inductor current (i'_L) and the transformer magnetizing inductor current (i_{L_M}), as depicted in Figure 4.4 in case of an active reset *forward converter*. Similar conditions also apply to the other transformer-isolated converters, but the shape of magnetizing current can vary, and consequently, its effect on the duty ratio constraints may be different. It may be obvious that the magnetizing current would have similar effect as the artificial compensation ramp has. As a consequence, the comparator equation may be given by

$$\langle i_{co} \rangle - m_c d T_s - \frac{kdT_s v'_{in}}{L'_M} = \langle i_L \rangle + \Delta i_L, \quad (4.10)$$

where v'_{in} and L'_M denote the corresponding values given at the secondary side, and k is the coefficient taking into account the shape of the magnetizing current (i.e., conventional *forward converter*: $k = 1$, *active reset forward*, *full* and *half-bridge*,

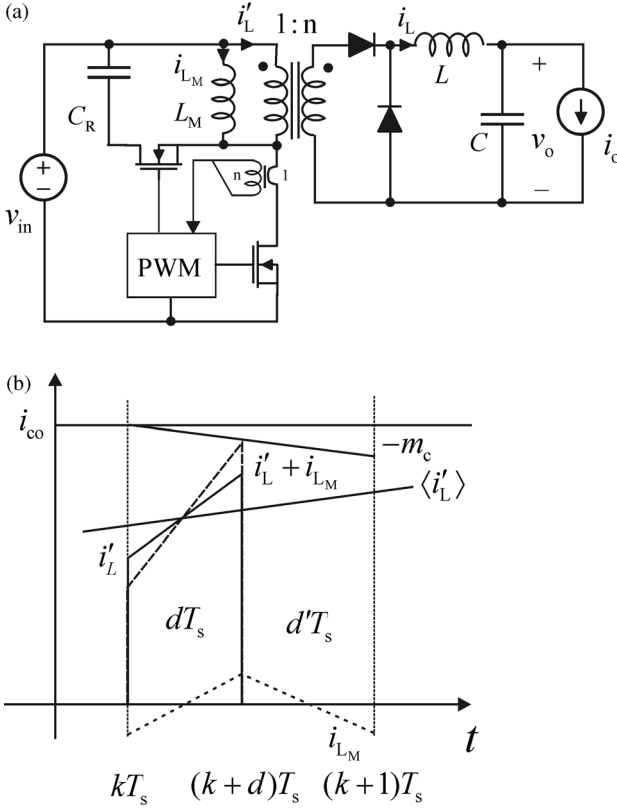


Figure 4.4 Active reset forward converter. (a) Schematics. (b) MOSFET current during the on-time (dT_s).

push-pull converters: $k = 1/2$). This means that the duty-ratio gain (F_m) and the input voltage feedforward gain (q_{in}) would be changed compared to the corresponding basic converters.

By linearizing the comparator equation in Eq. (4.9), we can compute the generalized duty-ratio gain to be

$$F_m = \frac{1}{T_s \left(M_c + (D' - D) \left(\sum_{i=1}^n (M_{1i} + M_{2i}) / 2 \right) \right)}. \quad (4.11)$$

It may be obvious that the duty ratio gain would become infinite when the duty ratio reaches the value:

$$D_{ML} = \frac{1}{2} + \frac{M_c}{\sum_{i=1}^n (M_{1i} + M_{2i})}, \quad (4.12)$$

which defines the generalized mode limit (ML) for the PCM-controlled converter in CCM. It is obvious that the mode limit is 0.5 if the compensation is set to zero

(i.e., $M_c = 0$), as also has been observed in practice. Equation (4.12) also implies that the compensation ramp should be chosen according to

$$M_c \geq \left(D_{ML} - \frac{1}{2} \right) \sum_{i=1}^n (M_{1i} + M_{2i}), \quad (4.13)$$

for guaranteeing proper operation up to the chosen duty ratio (D_{ML}).

4.2.3 Development of Duty-Ratio Constraints in DCM

The modeling of PCM control in DCM is the similar process as in CCM. The same comparator equation (4.2) applies, and the main task is to find a proper definition for $\langle i_L \rangle$. According to Figure 4.5, we can compute that at $t = (k + d)T_s$

$$\Delta i_L = m_1 d T_s - \frac{m_1 d (d + d_1) T_s}{2}, \quad (4.14)$$

where the first term corresponds to the peak inductor current and the last term to the average inductor current. The unknown duty ratio (d_1) can be solved from the equality $d m_1 = d_1 m_2$, which yields

$$d_1 = \frac{m_1}{m_2} \cdot d. \quad (4.15)$$

Substituting d_1 in Eqs (4.11) with (4.12) yields

$$\Delta i_L = m_1 d T_s - \frac{m_1 (m_1 + m_2) d^2 T_s}{2 m_2}, \quad (4.16)$$

and consequently, the comparator equation in Eq. (4.2) becomes as

$$\langle i_{co} \rangle - m_c d T_s = \langle i_L \rangle + m_1 d T_s - \frac{m_1 (m_1 + m_2) d^2 T_s}{2 m_2}. \quad (4.17)$$

The coefficients of the duty-ratio constraints in Eq. (4.1) can be solved from Eq. (4.14) by substituting the inductor-current slopes (i.e., m_1 and m_2) with their

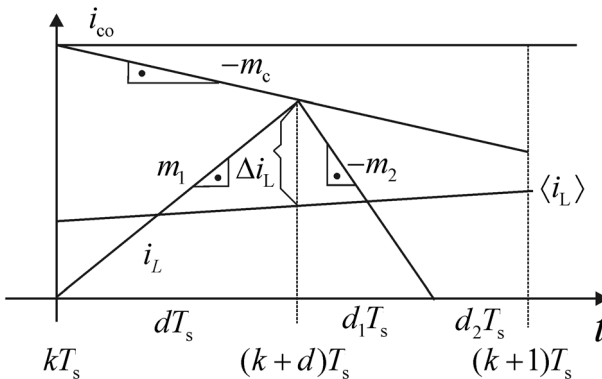


Figure 4.5 Inductor-current waveforms in DCM.

topology-based values and linearizing the resulting comparator equation at the specific operating point.

By linearizing the comparator equation in Eq. (4.17), we can compute the generalized duty-ratio gain of a second-order converter to be

$$F_m = [1] / \left[T_s \left(M_c + \frac{M_1(M_2 - (M_1 + M_2)D)}{M_2} \right) \right]. \quad (4.18)$$

It may be obvious that the duty ratio gain would become infinite, similarly as in CCM when the duty ratio reaches the value

$$D_{ML} = \frac{M_2}{M_1 + M_2} + \frac{M_2 M_c}{M_1(M_1 + M_2)}. \quad (4.19)$$

The first term in Eq. (4.19) defines actually the value of the duty ratio, where the converter enters into CCM mode of operation [6].

4.2.4 Origin and Consequences of Mode Limits in CCM and DCM

When the converter operates in CCM, we can compute according to the averaged comparator equation in Eq. (4.7) at steady state that the difference between the control current (I_{co}) and the averaged inductor current (I_L) in terms of duty ratio (D) can be given by

$$I_{co} - I_L = -\frac{(M_1 + M_2)T_s}{2} \cdot D^2 + \left(M_c + \frac{M_1 + M_2}{2} \right) T_s \cdot D, \quad (4.20)$$

which has a minima according to

$$|I_{co} - I_L|_{\min} = \frac{M_c T_s}{2} \left(1 + \frac{M_c}{M_1 + M_2} \right) + \frac{(M_1 + M_2)T_s}{8}, \quad (4.21)$$

at the duty ratio (D)

$$D = \frac{1}{2} + \frac{M_c}{M_1 + M_2}. \quad (4.22)$$

The duty ratio in Eq. (4.22), where the minima takes place, is the same as obtained for the mode limit in Eq. (4.12). The parabola shape of Eq. (4.20) dictates that the difference would decrease along the increase in duty ratio until the mode limit in Eq. (4.22) is reached. After that the difference should start increasing again, but it is physically impossible within a single cycle, because the difference should keep on decreasing along the increasing duty ratio. As a consequence, the converter is forced to enter into the second-harmonic mode of operation, where the difference naturally increases and a stable operating point would be found, as shown in Figure 4.6. The possible sub-harmonic operation modes may exist at $f_s/2^n$, where f_s is the switching frequency and $n = 1, 2, 3, \dots$, until the converter enters into chaotic operation mode [14].

Equation (4.20) may also be developed in terms of D as

$$D^2 - \left(1 + \frac{2M_c}{M_1 + M_2} \right) D + \frac{2(I_{co} - I_L)}{T_s(M_1 + M_2)} = 0, \quad (4.23)$$

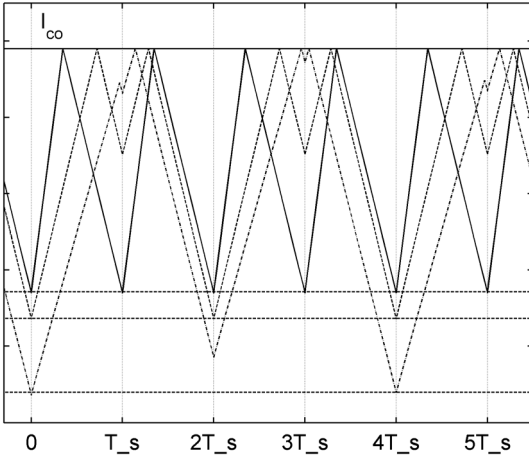


Figure 4.6 Simulated inductor current waveforms in normal (solid line) and subharmonic modes (second-harmonic: dashed line, fourth-harmonic: dash-dotted line) based on an uncompensated buck converter.

having roots at

$$D_{1,2} = \frac{1}{2} + \frac{M_c}{M_1 + M_2} \pm \sqrt{\left(\frac{1}{2} + \frac{M_c}{M_1 + M_2}\right)^2 - \frac{2(I_{co} - I_L)}{T_s(M_1 + M_2)}}. \quad (4.24)$$

If the difference in Eq. (4.24) is substituted with $|I_{co} - I_L|_{\min}$ in Eq. (4.21), the quadratic equation in Eq. (4.23) would have a double root coinciding with Eq. (4.22), which means that the real-valued solution exists only up to the mode limit. Therefore, it is obvious that the averaged comparator equation in Eq. (4.9) and the small-signal duty ratio gain (F_m) in Eq. (4.11) correctly predict the existence as well as the value of duty ratio where it will take place.

It is observed in practice that the inductor-current up (M_1) and down (M_2) slopes maintain certain relation in subharmonic mode, which is clearly visible in Figure 4.7 as well. The formula mathematically defining the relation can be derived as follows: The small-signal inductor current loop has infinite duty ratio gain (i.e., $F_m = \infty$) at the mode limit. As a consequence, the perturbation in the inductor current would follow exactly the perturbation in the control current, which is zero at open loop. This means that the derivative of the time-averaged inductor current ($\langle i_L \rangle$) has to be zero, that is,

$$d_{ML}m_1 - d'_{ML}m_2 = 0, \quad (4.25)$$

where d_{ML} equals Eq. (4.22). If substituting d_{ML} in Eq. (4.25) with Eq. (4.22), we get

$$M_2 = M_1 + 2M_c, \quad (4.26)$$

which shows that the absolute values of the slopes are equal in an uncompensated (i.e., $M_c = 0$) converter, as Figure 4.7a also clearly shows. From Figure 4.7b, we

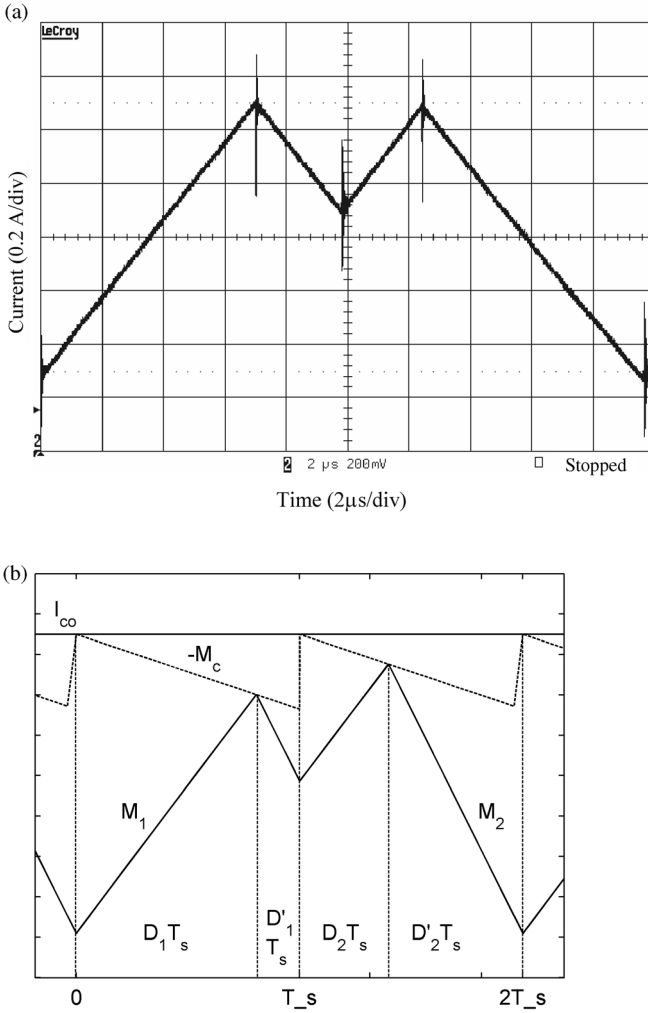


Figure 4.7 Inductor-current waveforms in second-harmonic mode. (a) Measured inductor current without compensation. (b) Simulated inductor current with certain amount of compensation.

may compute that

$$\begin{aligned} (M_1 + M_c)D_1 &= M_2D'_2 + M_cD_2, \\ (M_1 + M_c)D_2 &= M_2D'_1 + M_cD_1, \end{aligned} \quad (4.27)$$

which yields the average duty ratio (D_{av}) as

$$D_{av} = \frac{D_1 + D_2}{2} = \frac{M_2}{M_1 + M_2}. \quad (4.28)$$

If we denote $M = V_o/V_{in}$ and consider the ideal basic converts, then by applying Eq. (4.28) we will get $M = D_{av}$ for a buck converter, $M = 1/D'_{av}$ for a

boost converter, and $M = D_{av}/D'_{av}$ for a buck–boost converter, which are similar to the ideal modulus (i.e., $M(D)$) defined for the converters in Ref. [20]. The average duty ratio in Eq. (4.28) can be shown to equal the mode-limit duty ratio in Eq. (4.12) by substituting M_2 in Eq. (4.28) with Eq. (4.26) and applying some mathematical manipulation. This means, in practice, that the converter is not anymore controllable, because the average duty ratio cannot be changed.

When the converter operates in DCM, the comparator equation in Eq. (4.17) may also be presented at steady, when the compensation is set to zero, by

$$I_{co} - I_L = -\frac{M_1(M_1 + M_2)T_s}{2M_2}D^2 + M_1T_sD. \quad (4.29)$$

Equation (4.29) is a similar quadratic equation as in CCM (i.e., Eq. (4.20)), which dictates that the difference ($I_{co} - I_L$) shall decrease along the increase in the duty ratio until the minimum value

$$|I_{co} - I_L|_{\min} = \frac{M_1M_2T_s}{2(M_1 + M_2)}, \quad (4.30)$$

is reached. The corresponding mode-limit duty ratio (D_{ML}) is

$$D_{ML} = \frac{M_2}{M_1 + M_2}, \quad (4.31)$$

which is known to define the mode limit between DCM and CCM operation as already discussed. The averaged comparator equation can also be developed in terms of duty ratio as

$$D^2 - \frac{2M_2}{M_1 + M_2}D - \frac{2M_2(I_{co} - I_L)}{T_sM_1(M_1 + M_2)} = 0. \quad (4.32)$$

It may be obvious that Eq. (4.32) has a real-valued solution only up to the duty ratio corresponding to Eq. (4.31).

The steady-state comparator equation in Eq. (4.17) can also be developed in terms of the input-to-output relation (M), when taking into account that $D = M\sqrt{KM/1 - M}$ for a buck converter, $D = \sqrt{KM(M - 1)}$ for a boost converter, and $D = M\sqrt{K}$ for a buck–boost converter. This procedure yields for a buck converter

$$M^3 - M^2 + K\left(\frac{I_{co}R_{Leq}}{V_{in}}\right)^2 = 0, \quad (4.33)$$

for a boost converter

$$M^2 - M - \frac{K}{V_{in}}\left(\frac{I_{co}R_{Leq}}{2}\right)^2 = 0, \quad (4.34)$$

and for a buck–boost converter

$$M = \frac{\sqrt{K} \cdot I_{co}}{2V_{in}}, \quad (4.35)$$

where $R_{Leq} = V_o/I_o$.

Equation (4.33) can be developed further yielding

$$\left(M - \frac{2}{3}\right)^2 \left(M - \left(\frac{3I_{co}R_{Leq}}{4V_{in}}\right)^2\right) = 0, \quad (4.36)$$

which shows that there exist a double root at $M = 2/3$, which means that there are no real-valued solutions for M after $M = 2/3$ at open loop, as also discussed in Ref. [18]. It can be, however, proved theoretically that the mode limit $M = 2/3$ exists only at open loop: According to the inductor current waveforms (cf. Figure 4.5, $M_c = 0$), we can compute substituting D with $M\sqrt{K/(1-M)}$ and D_1 with $\sqrt{K(1-M)}$ that a real-valued solution for the control current can always be found as

$$I_{co} = \frac{2V_o}{R_{Leq}} \sqrt{\frac{1 - (V_o/V_{in})}{K}}, \quad (4.37)$$

when the feedback loop is closed. This proves that the corresponding mode limit does not exist under feedback control.

Figure 4.8 shows the simulated inductor current waveforms of an uncompensated buck converter having $K = 0.45$ (i.e., $L = 9 \mu\text{H}$, $R_{eq} = 4 \Omega$, $f_s = 100 \text{ kHz}$); the subharmonic operation would also take place in DCM. The possible subharmonic frequencies are all the even and odd harmonics of switching frequency. It is obvious that there is not such a need in DCM as in CCM to compensate the inductor current loop, because the design of the converter would be such that the mode limit does not exist in the targeted operation range of the converter.

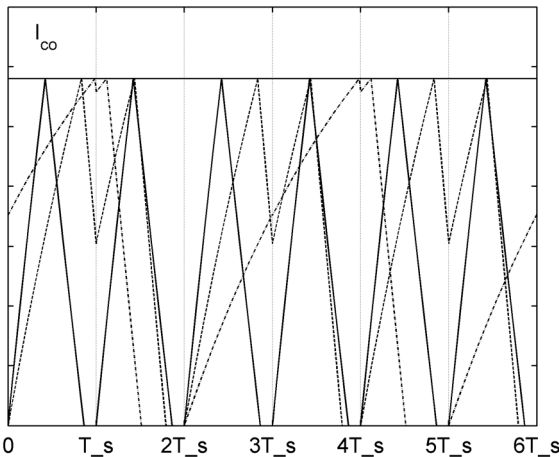


Figure 4.8 Simulated inductor-current waveforms in subharmonic modes in a DCM buck converter (basic switching frequency: solid line, second-harmonic: dashed line, third-harmonic: dash-dotted line).

4.2.5 Duty-Ratio Constraints in CCM

The duty-ratio constraints in Eq. (4.1) can be given for the second-order converters in the form of

$$\hat{d} = F_m(\hat{i}_{co} - q_L \hat{i}_L - q_C \hat{v}_C - q_{in} \hat{v}_{in} - q_{io} \hat{i}_o), \quad (4.38)$$

by means of which the perturbed duty ratio in the corresponding DDR state space will be replaced, and the corresponding PCM transfer functions can be solved from the PCM state space. The transfer functions can also be found by utilizing the open-loop control engineering block diagrams [6]. For that purpose, the duty-ratio constraints would be presented in the form of

$$\hat{d} = F_m(\hat{i}_{co} - q_L \hat{i}_L - q_{in} \hat{v}_{in} - q_o \hat{v}_o). \quad (4.39)$$

For the fourth-order converters, the duty-ratio constraints for the state-space application can be given as

$$\hat{d} = F_m(\hat{i}_{co} - q_{L1} \hat{i}_{L1} - q_{L2} \hat{i}_{L2} - q_{C1} \hat{v}_{C1} - q_{C2} \hat{v}_{C2} - q_{in} \hat{v}_{in} - q_{io} \hat{i}_o), \quad (4.40)$$

and for the control engineering block diagram application as

$$\hat{d} = F_m(\hat{i}_{co} - q_{L1} \hat{i}_{L1} - q_{L2} \hat{i}_{L2} - q_{in} \hat{v}_{in} - q_o \hat{v}_o). \quad (4.41)$$

4.2.5.1 Buck Converter

The power stage of the buck converter is given in Figure 3.6. The locally averaged inductor-current slopes are given in Eqs (3.12–3.14). Applying the given information, the comparator equation in (4.7) can be given by

$$\begin{aligned} \langle i_{co} \rangle - M_c d T_s &= \langle i_L \rangle + \frac{dd' T_s}{2L} (\langle v_{in} \rangle + (r_{ds2} - r_{ds1}) \langle i_L \rangle), \\ \langle i_{co} \rangle - M_c d T_s &= \langle i_L \rangle + \frac{dd' T_s}{2L} (\langle v_{in} \rangle + V_D + (r_d - r_{ds1}) \langle i_L \rangle). \end{aligned} \quad (4.42)$$

The duty-ratio constraints in Eqs (4.38) and (4.39) can be equally obtained from Eq. (4.42) by linearizing the given equations at a certain operating point, which yields

$$\begin{aligned} F_m &= 1 / \left(T_s \left(M_c + \frac{(D' - D) V_e}{2L} \right) \right), \\ q_L &= 1 + \frac{DD' T_s}{2L} (r_{ds2} - r_{ds1}), \text{ or } 1 + \frac{DD' T_s}{2L} (r_d - r_{ds1}), \\ q_C &= 0, \\ q_{in} &= \frac{DD' T_s}{2L}, \\ q_{io} &= 0, \end{aligned} \quad (4.43)$$

where V_e is defined in Section 3.4.1.

4.2.5.2 Boost Converter

The power stage of the buck converter is given in Figure 3.8. The locally averaged inductor-current slopes are given in Eqs. (3.17–3.19). Applying the given

information, the comparator equation in Eq. (4.7) can be given for the state-space application by

$$\begin{aligned}\langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd' T_s}{2L} (\langle v_C \rangle + (r_{ds2} + r_C - r_{ds1}) \langle i_L \rangle - r_C \langle i_o \rangle), \\ \langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd' T_s}{2L} (\langle v_C \rangle + V_D + (r_d + r_C - r_{ds1}) \langle i_L \rangle - r_C \langle i_o \rangle),\end{aligned}\quad (4.44)$$

and for the control block diagram application by

$$\begin{aligned}\langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd' T_s}{2L} (\langle v_o \rangle + (r_{ds2} - r_{ds1}) \langle i_L \rangle), \\ \langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd' T_s}{2L} (\langle v_o \rangle + V_D + (r_d - r_{ds1}) \langle i_L \rangle).\end{aligned}\quad (4.45)$$

The duty-ratio constraints in Eq. (4.38) can be obtained from Eq. (4.44) by linearizing the given equations at a certain operating point, which yields

$$\begin{aligned}F_m &= 1 / \left(T_s (M_c + \frac{(D' - D)V_e}{2L}) \right), \\ q_L &= 1 + \frac{DD' T_s}{2L} (r_{ds2} + r_C - r_{ds1}) \text{ or } 1 + \frac{DD' T_s}{2L} (r_d + r_C - r_{ds1}), \\ q_C &= \frac{DD' T_s}{2L}, \\ q_{in} &= 0, \\ q_{io} &= -\frac{DD' T_s}{2L} r_C,\end{aligned}\quad (4.46)$$

where V_e is defined in Section 3.4.2.

The duty-ratio constraints in Eq. (4.39) can be obtained from Eq. (4.45) by linearizing the given equations at a certain operating point, which yields

$$\begin{aligned}F_m &= 1 / \left(T_s (M_c + \frac{(D' - D)(V_o + (r_{ds2} - r_{ds1})I_L)}{2L}) \right) \\ \text{or} \\ F_m &= 1 / \left(T_s (M_c + \frac{(D' - D)(V_o + V_D + (r_d - r_{ds1})I_L)}{2L}) \right), \\ q_L &= 1 + \frac{DD' T_s}{2L} (r_{ds2} - r_{ds1}) \text{ or } 1 + \frac{DD' T_s}{2L} (r_d - r_{ds1}), \\ q_{in} &= 0, \\ q_{io} &= \frac{DD' T_s}{2L}.\end{aligned}\quad (4.47)$$

4.2.5.3 Buck-Boost Converter

The power stage of the buck converter is given in Figure 3.10. The locally averaged inductor-current slopes are given in Eqs. (3.22–3.26). Applying the given

information, the comparator equation in Eq. (4.7) can be given for the state-space application by

$$\begin{aligned}\langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd'T_s}{2L} (\langle v_{in} \rangle + \langle v_C \rangle + (r_{ds2} + r_C - r_{ds1}) \langle i_L \rangle - r_C \langle i_o \rangle), \\ \langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd'T_s}{2L} (\langle v_{in} \rangle + \langle v_C \rangle + V_D + (r_d + r_C - r_{ds1}) \langle i_L \rangle - r_C \langle i_o \rangle),\end{aligned}\quad (4.48)$$

and for the control block diagram application by

$$\begin{aligned}\langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd'T_s}{2L} (\langle v_{in} \rangle + \langle v_o \rangle + (r_{ds2} - r_{ds1}) \langle i_L \rangle), \\ \langle i_{co} \rangle - M_c dT_s &= \langle i_L \rangle + \frac{dd'T_s}{2L} (\langle v_{in} \rangle + \langle v_o \rangle + V_D + (r_d - r_{ds1}) \langle i_L \rangle).\end{aligned}\quad (4.49)$$

The duty-ratio constraints in Eq. (4.38) can be obtained from Eq. (4.48) by linearizing the given equations at a certain operating point, which yields

$$\begin{aligned}F_m &= 1 / \left(T_s \left(M_c + \frac{(D' - D)V_e}{2L} \right) \right), \\ q_L &= 1 + \frac{DD'T_s}{2L} (r_{ds2} + r_C - r_{ds1}) \text{ or } 1 + \frac{DD'T_s}{2L} (r_d + r_C - r_{ds1}), \\ q_C &= \frac{DD'T_s}{2L}, \\ q_{in} &= \frac{DD'T_s}{2L}, \\ q_{io} &= -\frac{DD'T_s}{2L} r_C,\end{aligned}\quad (4.50)$$

where V_e is defined in Section 3.4.3.

The duty-ratio constraints in Eq. (4.39) can be obtained from Eq. (4.49) by linearizing the given equations at a certain operating point, which yields

$$\begin{aligned}F_m &= 1 / \left[T_s \left(M_c + \frac{(D' - D)(V_{in} + V_o + (r_{ds2} - r_{ds1})I_L)}{2L} \right) \right] \\ \text{or} \\ F_m &= 1 / \left[T_s \left(M_c + \frac{(D' - D)(V_{in} + V_o + V_D + (r_d - r_{ds1})I_L)}{2L} \right) \right], \\ q_L &= 1 + \frac{DD'T_s}{2L} (r_{ds2} - r_{ds1}) \text{ or } 1 + \frac{DD'T_s}{2L} (r_d - r_{ds1}), \\ q_{in} &= \frac{DD'T_s}{2L}, \\ q_{io} &= \frac{DD'T_s}{2L}.\end{aligned}\quad (4.51)$$

4.2.5.4 Superbuck Converter

The power stage of the buck converter is given in Fig. 3.13. The locally averaged inductor-current slopes are given in Eqs (3.29) and (3.30). Applying the given information, the comparator equation in Eq. (4.9) can be given for the state-space application by

$$\langle i_{co} \rangle - M_c dT_s = \langle i_{L1} \rangle + \langle i_{L2} \rangle + \frac{dd'T_s}{2} \left(\frac{\langle v_1 \rangle}{L_1} + \frac{\langle v_2 \rangle}{L_2} \right), \quad (4.52)$$

where $\langle v_1 \rangle$ and $\langle v_2 \rangle$ are defined as

$$\begin{aligned} \langle v_1 \rangle &= \langle v_{C1} \rangle + V_D + (r_{C1} + r_d - r_{ds})\langle i_{L1} \rangle + (r_d - r_{ds})\langle i_{L2} \rangle, \\ \langle v_2 \rangle &= \langle v_{C1} \rangle + V_D + (r_d - r_{ds})\langle i_{L1} \rangle + (r_d - r_{C1} - r_{ds})\langle i_{L2} \rangle. \end{aligned} \quad (4.53)$$

The duty-ratio constraints in Eq. (4.40) can be obtained from Eq. (4.52) by linearizing the given equations at a certain operating point, which yields

$$\begin{aligned} F_m &= 1 / \left[T_s \left(M_c + \frac{D' - D}{2} \left(\frac{V_1}{L_1} + \frac{V_2}{L_2} \right) \right) \right], \\ q_{L1} &= 1 + \frac{DD'T_s}{2} \left(\frac{r_{C1} + r_d - r_{ds}}{L_1} + \frac{r_d - r_{ds}}{L_2} \right), \\ q_{L2} &= 1 + \frac{DD'T_s}{2} \left(\frac{r_d - r_{ds}}{L_1} + \frac{r_d - r_{C1} - r_{ds}}{L_2} \right), \\ q_{C1} &= \frac{DD'T_s}{2} \cdot \frac{L_1 L_2}{L_1 + L_2}, \\ q_{C2} &= 0, \\ q_{in} &= 0, \\ q_{io} &= 0, \\ V_1 &= V_{in} + V_D + (r_d - r_{ds} + Dr_{C1} - Dr_{L1} + D'r_{L2})I_o, \\ V_2 &= V_1 - r_{C1}I_o. \end{aligned} \quad (4.54)$$

The formula of the duty-ratio gain (F_m) in Eq. (4.54) indicates that F_m would become infinite when the mode-limit duty ratio (D_{ML}) is reached

$$D_{ML} = \frac{1}{2} + M_c L_1 L_2 / (L_2 V_1 + L_1 V_2). \quad (4.55)$$

When the duty ratio exceeds the mode limit value, the converter will enter into the second-harmonic mode of operation, similar to the conventional buck converter. In order to ensure proper operation of the converter up to the desired mode limit, the compensation shall be designed as

$$M_c \geq \left(D_{ML} - \frac{1}{2} \right) \left(\frac{V_1}{L_1} + \frac{V_2}{L_2} \right). \quad (4.56)$$

4.2.5.5 Coupled-Inductor Superbuck Converter

We assume that the coupling of the inductors are carried out by minimizing the input current ripple, as described in Section 3.4.5 (i.e., $M = L_2$ and $k = \sqrt{L_2/L_1}$). The coupling of the inductors naturally affects the up (m_{1i}) and down (m_{2i}) slopes of the inductor currents. By applying the algorithm presented in Section 2.4.3 (Eq. (2.85)), Δi_L can be given by

$$\Delta i_L = \frac{dd'T_s}{2} \left(\frac{r_d - r_{ds}}{L_2} \langle i_{L1} \rangle + \frac{r_{L2} + r_d - r_{ds}}{L_2} \langle i_{L2} \rangle + \frac{\langle v_{C1} \rangle + V_D}{L_2} \right). \quad (4.57)$$

The duty-ratio constraints can be found by linearizing the comparator equation

$$\langle i_{co} \rangle - M_c d T_s = \langle i_{L1} \rangle + \langle i_{L2} \rangle + \Delta i_L, \quad (4.58)$$

which yields

$$\begin{aligned} F_m &= 1 / \left[T_s \left(M_c + \frac{D' - D}{2L_2} (V_{in} + V_D + (r_d - r_{ds} - Dr_{L1} + 2D'r_{L2})I_o) \right) \right], \\ q_{L1} &= 1 + \frac{DD'T_s}{2L_2} (r_d - r_{ds}), \\ q_{L2} &= 1 + \frac{DD'T_s}{2L_2} (r_d - r_{ds} + r_{L2}), \\ q_{C1} &= \frac{DD'T_s}{2L_2}, \\ q_{C2} &= 0, \\ q_{in} &= 0, \\ q_{io} &= 0. \end{aligned} \quad (4.59)$$

The coupling also affects the duty ratio at the mode limit, where the converter would enter into the second-harmonic mode of operation, and its compensation as

$$\begin{aligned} D_{ML} &= \frac{1}{2} + \frac{L_2 M_c}{V_{in} + V_D + (r_d - r_{ds} - Dr_{L1} + 2D'r_{L2})I_o}, \\ M_c &\geq \left(D_{ML} - \frac{1}{2} \right) \frac{V_{in} + V_D + (r_d - r_{ds} - Dr_{L1} + 2D'r_{L2})I_o}{L_2}. \end{aligned} \quad (4.60)$$

4.2.6 Duty-Ratio Constraints in DCM

The DCM duty-ratio constraints are given only for the buck, boost, and buck-boost converters.

4.2.6.1 Buck Converter

The inductor-current up slope is $m_1 = (\langle v_{in} \rangle - \langle v_o \rangle)/L$ and the down slope $m_2 = \langle v_o \rangle/L$. As a consequence, the averaged comparator equation can be

given by

$$\langle i_{co} \rangle - M_c dT_s = \langle i_L \rangle + \frac{(\langle v_{in} \rangle - \langle v_o \rangle) dT_s}{L} - \frac{(\langle v_{in} \rangle - \langle v_o \rangle) \langle v_{in} \rangle d^2 T_s}{2L \langle v_o \rangle}, \quad (4.61)$$

and the corresponding small-signal duty-ratio-constraints coefficients by

$$\begin{aligned} F_m &= 1 / \left[T_s \left(M_c + \frac{V_{in}(1-M)(M-D)}{LM} \right) \right], \\ q_L &= 1, \\ q_C &= \frac{DT_s}{L} \left(\frac{D}{2M^2} - 1 \right), \\ q_{in} &= \frac{DT_s}{L} \left(1 - \frac{(2-M)D}{2M} \right), \end{aligned} \quad (4.62)$$

where $M = V_o/V_{in}$.

4.2.6.2 Boost Converter

The inductor-current up slope is $m_1 = \langle v_{in} \rangle / L$ and the down slope $m_2 = (\langle v_o \rangle - \langle v_{in} \rangle) / L$. As a consequence, the averaged comparator equation can be given by

$$\langle i_{co} \rangle - M_c dT_s = \langle i_L \rangle + \frac{\langle v_{in} \rangle dT_s}{L} - \frac{\langle v_{in} \rangle \langle v_o \rangle d^2 T_s}{2L(\langle v_o \rangle - \langle V_{in} \rangle)}, \quad (4.63)$$

and the corresponding small-signal duty-ratio-constraints coefficients by

$$\begin{aligned} F_m &= 1 / \left[T_s \left(M_c + \frac{V_{in}(D'M - 1)}{L(M - 1)} \right) \right], \\ q_L &= 1, \\ q_C &= \left(\frac{D^2 T_s}{2L(M - 1)^2} \right), \\ q_{in} &= \frac{DT_s}{L} \left(1 - \frac{DM^2}{2(M - 1)} \right), \end{aligned} \quad (4.64)$$

where $M = V_o/V_{in}$.

4.2.6.3 Buck-Boost Converter

The inductor-current up slope is $m_1 = \langle v_{in} \rangle / L$ and the down slope $m_2 = \langle v_o \rangle / L$. As a consequence, the averaged comparator equation can be given by

$$\langle i_{co} \rangle - M_c dT_s = \langle i_L \rangle + \frac{\langle v_{in} \rangle dT_s}{L} - \frac{\langle v_{in} \rangle (\langle v_{in} \rangle + \langle v_o \rangle) d^2 T_s}{2L \langle v_o \rangle}, \quad (4.65)$$

and the corresponding small-signal duty-ratio-constraints coefficients by

$$\begin{aligned}
 F_m &= 1/\left[T_s\left(M_c + \frac{V_{in}(D'M - D)}{LM}\right)\right], \\
 q_L &= 1, \\
 q_C &= \frac{D^2 T_s}{2LM^2}, \\
 q_{in} &= \frac{DT_s}{L}\left(1 - \frac{D(2+M)}{2M}\right),
 \end{aligned} \tag{4.66}$$

where $M = V_o/V_{in}$.

4.2.7 General PCM Transfer Functions in CCM

The general PCM transfer functions, which are valid for a buck, boost, and buck–boost converters in CCM, can be derived based on the duty-ratio-constraints coefficients corresponding to Eq. (4.39), the coefficients A and B (i.e., buck: $A = 1$, $B = 0$; boost and buck–boost: $A = D'$, $B = I_L$), the corresponding DDR transfer functions, and the block diagrams given in Figure 4.9. As a consequence, the general transfer functions can be given by

$$\begin{aligned}
 Y_{in-o} &= Y_{in-o}^{DDR} - \frac{F_m\left((q_o + (q_L/AZ_C))G_{io-o}^{DDR} + q_{in}\right)G_{ci-o}^{DDR}}{1 + L_c + L_v}, \\
 T_{oi-o} &= T_{oi-o}^{DDR} + \frac{F_m\left((q_o + (q_L/AZ_C))Z_{o-o}^{DDR} - (q_L/A)\right)G_{ci-o}^{DDR}}{1 + L_c + L_v}, \\
 G_{ci-o} &= \frac{F_m G_{ci-o}^{DDR}}{1 + L_c + L_v}, \\
 G_{io-o} &= \frac{\left(1 + (BF_m q_L/A)\right)G_{io-o}^{DDR} - F_m q_{in} G_{co-o}^{DDR}}{1 + L_c + L_v}, \\
 Z_{o-o} &= \frac{\left(1 + (BF_m q_L/A)\right)Z_{o-o}^{DDR} + (F_m q_L/A)G_{co-o}^{DDR}}{1 + L_c + L_v}, \\
 G_{co-o} &= \frac{F_m G_{co-o}^{DDR}}{1 + L_c + L_v},
 \end{aligned} \tag{4.67}$$

where Z_C denotes the impedance of the output capacitor and L_c and L_v denotes the internal inductor-current-loop gain and output-voltage-loop gain, respectively:

$$\begin{aligned}
 L_c &= F_m q_L G_{cl-o}^{DDR}, \\
 L_v &= F_m q_o G_{co-o}^{DDR}.
 \end{aligned} \tag{4.68}$$

G_{cl-o}^{DDR} in (4.68) denotes the control-to-inductor-current transfer function of the corresponding DDR-controlled converter.

The general transfer functions are actually very useful for the following reasons:

- 1) If the DDR control-to-output or control-to-input transfer function (G_{co-o}^{DDR} or G_{ci-o}^{DDR}) contains an RHP zero, then the same zero also exists in the PCM converter with the same control bandwidth limitations.

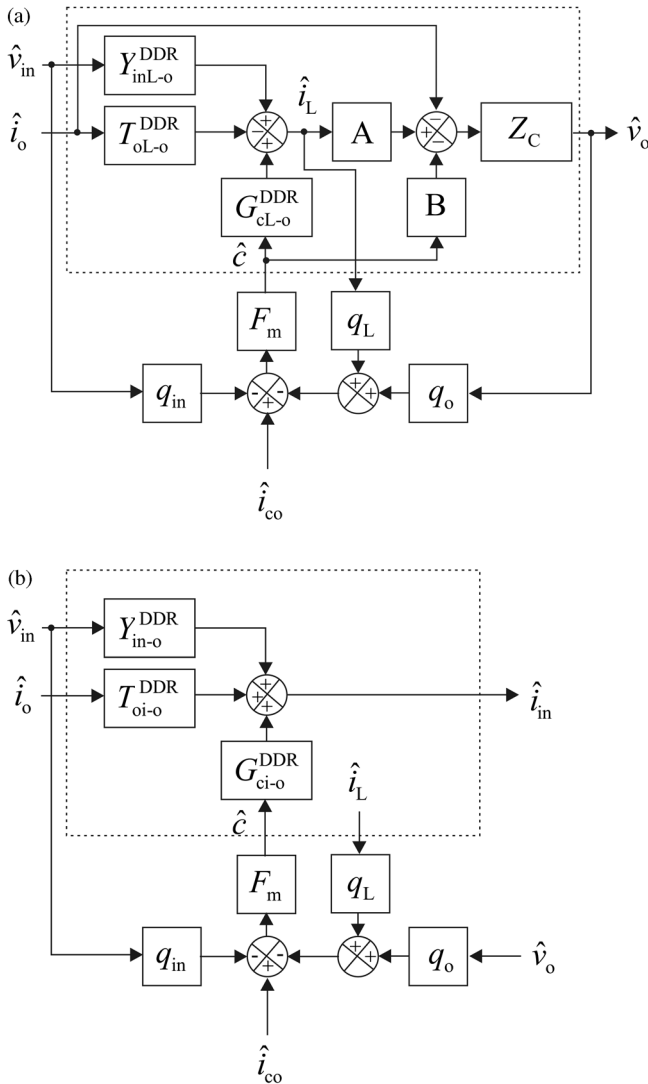


Figure 4.9 Block diagrams for computing the generalized PCM transfer functions for the basic converters. (a) Input dynamics. (b) Output dynamics.

- 2) If $q_{in} = 0$, then the input-to-output transfer function (G_{io-o}) cannot be nullified by means of the artificial inductor-current compensation.
- 3) If G_{io-o} can be nullified, then $Y_{in-o} = Y_{in-c} = Y_{in-sco} = Y_{in-\infty} = Y_{in-o}^{DDR} - \frac{G_{io-o}^{DDR} G_{ci-o}^{DDR}}{G_{co-o}^{DDR}}$.
- 4) We can also verify that the set of special ideal transfer functions derived for the DDR-controlled converters is also valid for the corresponding PCM-controlled converters:

$$\begin{aligned}
Y_{in-\infty}^{PCM} &= Y_{in-o}^{DDR} - \frac{G_{io-o}^{DDR} G_{ci-o}^{DDR}}{G_{co-o}^{DDR}}, \\
Z_{o-\infty}^{PCM} &= Z_{o-o}^{DDR} + \frac{T_{oi-o}^{DDR} G_{co-o}^{DDR}}{G_{ci-o}^{DDR}}, \\
T_{oi-\infty}^{PCM} &= T_{oi-o}^{DDR} + \frac{Z_{o-o}^{DDR} G_{ci-o}^{DDR}}{G_{co-o}^{DDR}}, \\
G_{io-\infty}^{PCM} &= G_{io-o}^{DDR} - \frac{Y_{in-o}^{DDR} G_{co-o}^{DDR}}{G_{ci-o}^{DDR}}.
\end{aligned} \tag{4.69}$$

4.2.8 PCM State Spaces and Transfer Functions in CCM

As stated in the beginning of the chapter, the PCM state spaces can be obtained from the corresponding DDR state spaces derived in Chapter 3 by substituting the perturbed duty ratio (\hat{d}) in them with the defined duty ratio constraints given in Section 4.2.5 (i.e., the state-space application-specific constraints).

4.2.8.1 Buck Converter

The linearized state space of the DDR-controlled converter is given in Section 3.4.1 (Eq. (3.37)). Substituting the perturbed duty ratio (\hat{d}) with the derived duty-ratio constraints

$$\begin{aligned}
\hat{d} &= F_m(\hat{i}_{co} - q_L \hat{i}_L - q_{in} \hat{v}_{in}), \\
F_m &= 1 / \left[T_s \left(M_c + \frac{(D' - D)V_e}{2L} \right) \right], \\
q_L &= 1 + \frac{DD'T_s}{2L} (r_{ds2} - r_{ds1}) \text{ or } 1 + \frac{DD'T_s}{2L} (r_d - r_{ds1}), \\
q_{in} &= \frac{DD'T_s}{2L},
\end{aligned} \tag{4.70}$$

yields the PCM small-signal state space as

$$\begin{aligned}
\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \begin{bmatrix} -\frac{r_e + F_m V_e q_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{D - F_m V_e q_{in}}{L} & \frac{r_C}{L} & \frac{F_m V_e}{L} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}, \\
\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} =D - F_m I_L q_L & 0 \\ 0 & 1 + r_C C \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} -F_m I_L q_{in} & 0 & F_m I_L \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix},
\end{aligned} \tag{4.71}$$

where r_e and V_e are defined in Section 3.4.1 (Eqs (3.38) and (3.39)). Applying *Laplace* transformation and matrix algebra to Eq. (4.71), the input dynamics can be given by

$$\begin{aligned}
Y_{\text{in-o}} &= \frac{((D - F_m V_e q_{\text{in}})(D - F_m I_L q_L)s)/L}{\Delta} - F_m q_{\text{in}} I_L, \\
\Delta T_{\text{oi-o}} &= \frac{(D - F_m I_L q_L)(1 + sr_C C)}{LC}, \\
G_{\text{ci-o}} &= \frac{(F_m V_e (D - F_m I_L q_L)s)/L}{\Delta} + F_m I_L,
\end{aligned} \tag{4.72}$$

and the output dynamics by

$$\begin{aligned}
\Delta G_{\text{io-o}} &= \frac{(D - F_m V_e q_{\text{in}})(1 + sr_C C)}{LC}, \\
\Delta Z_{\text{o-o}} &= \frac{(r_e - r_C + F_m V_e q_L + sL)(1 + sr_C C)}{LC}, \\
\Delta G_{\text{co-o}} &= \frac{F_m V_e (1 + sr_C C)}{LC},
\end{aligned} \tag{4.73}$$

where the denominator (Δ) is defined by

$$\Delta = s^2 + s \cdot \frac{r_e + F_m V_e q_L}{L} + \frac{1}{LC}. \tag{4.74}$$

As stated earlier, the ideal special transfer functions equal the corresponding DDR transfer functions defined in Section 3.4.1 (Eq. (3.41)). The input admittance at short-circuited output ($Y_{\text{in-sco}}$), and the output impedance at open-circuit input ($Z_{\text{o-oci}}$) can be given by

$$\begin{aligned}
Y_{\text{in-sco}} &= \frac{(D - F_m V_e q_{\text{in}})(D - F_m I_o q_L)}{sL + F_m V_e q_L + r_e - r_C} - F_m I_o q_{\text{in}}, \\
Z_{\text{o-oci}}^{\text{o}} &= \frac{1}{C} \cdot \left\{ \frac{\left[\left(s + \frac{D(F_m q_L I_o - D) + F_m q_{\text{in}}(DV_e + (r_e - r_C)I_o)}{LF_m q_{\text{in}} I_L} \right) (1 + sr_C C) \right]}{\left[s^2 + s \frac{D(F_m q_L I_o - D) + F_m q_{\text{in}}(DV_e + r_e I_o)}{LF_m q_{\text{in}} I_L} + \frac{1}{LC} \right]} \right\}, \\
Z_{\text{o-oci}}^{\text{c}} &= \frac{Z_{\text{o-c}}}{Y_{\text{in-c}}} Y_{\text{in-sco}}.
\end{aligned} \tag{4.75}$$

The optimal compensation of a PCM-controlled buck converter [20] is usually such that the input-to-output transfer function ($G_{\text{io-o}}$) is nullified. According to Eq. (4.73), this means that $D - F_m V_e q_{\text{in}} = 0$. According to this condition, the optimal compensation ($M_{\text{c-opt}}$) would be

$$M_{\text{c-opt}} = \frac{DV_e}{2L} \approx \frac{V_o}{2L}. \tag{4.76}$$

The optimal compensation does not necessarily ensure the operation of the converter up to the duty ratio of 100% in transient conditions, where dV_e does not

equal V_o . In order to avoid the converter to enter into the second-harmonic mode, the compensation should be designed by

$$M_{c-100\%} = \frac{V_e}{2L} \approx \frac{V_{in}}{2L}, \quad (4.77)$$

but such a fixed compensation is not easy to provide due to the varying input voltage. The entering into the second-harmonic mode will just limit the dynamics of the converter but is not otherwise harmful to the converter operation.

When the optimal compensation is applied in a buck converter, the input admittance (Y_{in-o}) and the short-circuit input admittance (Y_{in-sco}) would equal $-DI_o/V_e$ (i.e., $Y_{in-\infty}$) as well as the DC gain of the control-to-output transfer function (G_{co-o}) would equal $2L/T_s/D'$ (i.e., will increase when the input voltage decreases), as can be deduced based on Eqs. (4.72–4.73) and (4.75).

It is well known [6] that the poles of the PCM-controlled converter are well separated due to high damping, which can be theoretically addressed to the lossless resistor ($F_m V_e q_L$) connected in series with the inductor (cf. Z_{o-o} in Eq. (4.73)). Therefore, the low- (ω_{p-low}) and high-frequency (ω_{p-high}) poles can be approximated by

$$\begin{aligned} \omega_{p-low} &\approx \frac{1}{F_m V_{in} C} \approx \frac{T_s D'}{2LC}, \\ \omega_{p-high} &\approx \frac{F_m V_{in}}{L} \approx \frac{2}{T_s D'}. \end{aligned} \quad (4.78)$$

The last terms in Eq. (4.78) correspond to the optimally compensated converter. The behavior of the low-frequency pole means that the output-voltage-loop crossover frequency does not change when the input voltage changes, which is quite different to what takes place in a DDR-controlled buck converter.

If the converter control-to-output transfer function (G_{co-o}) is measured by using a resistive load, its dynamic behavior would be highly dominated by the load resistor as

$$G_{co-o} \approx \frac{F_m V_{in}(1 + sr_C C)}{s^2 LC + sF_m V_{in} C + \frac{F_m V_{in}}{R_L}}. \quad (4.79)$$

According to Eq. (4.79), we can conclude that the low-frequency pole $\omega_{p-low} \approx 1/R_L C$, the low-frequency gain $G_{co-o}(DC) \approx R_L$, and only the high-frequency pole is not affected (i.e., $\omega_{p-high} \approx F_m V_{in}/L$). Therefore, it is extremely important to remove the load effect when using the transfer functions for control design and other purposes.

4.2.8.2 Boost Converter

The linearized state space of the DDR-controlled converter is given in Section 3.4.2 (Eq. (3.47)). Substituting the perturbed duty ratio (\hat{d}) with the derived duty-ratio constraints

$$\begin{aligned}
\hat{d} &= F_m(\hat{i}_{co} - q_L \hat{i}_L - q_C \hat{v}_C - q_{io} \hat{i}_o), \\
F_m &= 1 / \left[T_s \left(M_c + \frac{(D' - D)V_e}{2L} \right) \right], \\
q_L &= 1 + \frac{DD'T_s}{2L} (r_{ds2} + r_C - r_{ds1}) \text{ or } 1 + \frac{DD'T_s}{2L} (r_d + r_C - r_{ds1}), \\
q_C &= \frac{DD'T_s}{2L}, \\
q_{in} &= 0, \\
q_{io} &= -\frac{DD'T_s}{2L} r_C,
\end{aligned} \tag{4.80}$$

yields the PCM small-signal state space as

$$\begin{aligned}
\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \begin{bmatrix} -\frac{r_e + F_m V_e q_L}{L} & -\frac{D' + F_m V_e q_C}{L} \\ \frac{D' + F_m I_L q_L}{C} & \frac{F_m I_L q_C}{C} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \\
&+ \begin{bmatrix} \frac{1}{L} & \frac{D'r_C - F_m V_e q_{io}}{L} & \frac{F_m V_e}{L} \\ 0 & -\frac{1 - F_m I_L q_{io}}{C} & -\frac{F_m I_L}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}, \\
\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 + r_C C \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix},
\end{aligned} \tag{4.81}$$

where r_e and V_e are defined in Section 3.4.2 (Eqs. (3.50) and (3.51)). Applying *Laplace* transformation and matrix algebra to Eq. (4.81), the input dynamics can be given by

$$\begin{aligned}
\Delta Y_{in-o} &= \frac{1}{L} \left(s - \frac{F_m I_L q_C}{C} \right), \\
\Delta T_{oi-o} &= \frac{D'r_C - F_m V_e q_{io}}{L} \left(s + \frac{(D' + F_m V_e q_C)L}{(D'r_C - F_m V_e q_{io})C} \right), \\
\Delta G_{ci-o} &= \frac{F_m V_e}{L} \left(s + \frac{D'I_L}{CV_e} \right),
\end{aligned} \tag{4.82}$$

and the output dynamics by

$$\begin{aligned}
\Delta G_{io-o} &= \frac{(D' + F_m I_L q_L)}{LC} (1 + sr_C C), \\
\Delta Z_{o-o} &= \frac{(1 - F_m I_L q_{io})}{LC} \left(\frac{r_e - D'^2 r_C + F_m V_e (q_L + D' q_{io}) - F_m I_L (q_{io} r_e + q_L D' r_C)}{1 - F_m I_L q_{io}} + sL \right) \\
&\quad (1 + sr_C C), \\
\Delta G_{co-o} &= \frac{F_m (D' V_e - I_L r_e)}{LC} \left(1 - s \frac{L I_L}{D V_e - I_L r_e} \right) (1 + sr_C C),
\end{aligned} \tag{4.83}$$

where the denominator (Δ) is defined by

$$\Delta = s^2 + s \cdot \left(\frac{r_e + F_m V_e q_L}{L} - \frac{F_m I_L q_C}{C} \right) + \frac{D^2 + D' F_m (V_e q_C + I_L q_L) - F_m I_L q_C r_e}{LC}. \quad (4.84)$$

As stated earlier, the ideal special transfer functions equal the corresponding DDR transfer functions defined in Section 3.4.2 (Eq. (3.53)). The input admittance at short-circuited output ($Y_{\text{in-sco}}$) and the output impedance at open-circuit input ($Z_{\text{o-oci}}$) can be given by

$$\begin{aligned} Y_{\text{in-sco}} &= 1 / \left[sL + \frac{r_e - D'^2 r_C + F_m V_e (q_L + D' q_{\text{io}}) - F_m I_L (q_{\text{io}} r_e + q_L D' r_C)}{1 - F_m I_L q_{\text{io}}} \right], \\ Z_{\text{o-oci}}^{\text{o}} &= \frac{(1 - F_m q_{\text{in}} I_L)(1 + s r_C C)}{sC - F_m q_{\text{in}} I_L}, \\ Z_{\text{o-oci}}^{\text{c}} &= \frac{Z_{\text{o-c}}}{Y_{\text{in-c}}}. \end{aligned} \quad (4.85)$$

In a PCM-controlled boost converter, similar optimal compensation scheme as in the buck converter does not exist. The compensation should be carried out by providing the duty ratio range of 100% by designing $M_{\text{c-100\%}}$ as

$$M_{\text{c-100\%}} = \frac{V_e}{2L} \approx \frac{V_o}{2L}. \quad (4.86)$$

The same RHP zero in the control-to-output transfer function ($G_{\text{co-o}}$) as in the DDR-controlled boost converter clearly exists according to Eq. (4.83). Its low-frequency gain $G_{\text{co-o}}(DC) \approx L/T_s/D'^2$ is highly dependent on the duty ratio, when the compensation in Eq. (4.86) is applied. The poles of the transfer functions are also highly separated for the similar reason as in a buck converter (i.e., lossless resistor $F_m V_e q_L$), and can be approximated by

$$\begin{aligned} \omega_{\text{p-low}} &\approx \frac{D^2}{F_m V_o C} \approx \frac{T_s D^3}{LC}, \\ \omega_{\text{p-high}} &\approx \frac{F_m V_o}{L} \approx \frac{1}{T_s D}, \end{aligned} \quad (4.87)$$

where the last terms correspond to the compensated converter (i.e., Eq. (4.86)). Similarly as in the buck converter, the use of resistive load for characterizing the converter dynamics would yield highly load-dominated transfer functions, which do not characterize the converter dynamics at all.

4.2.8.3 Buck-Boost Converter

The linearized state space of the DDR-controlled converter is given in Section 3.4.3 (Eq. (3.60)). Substituting the perturbed duty ratio (\hat{d}) with the derived

duty-ratio constraints

$$\begin{aligned}
 \hat{d} &= F_m(\hat{i}_{co} - q_L \hat{i}_L - q_C \hat{v}_C - q_{in} \hat{v}_{in} - q_{io} \hat{i}_o), \\
 F_m &= 1 / \left[T_s \left(M_c + \frac{(D' - D)V_e}{2L} \right) \right], \\
 q_L &= 1 + \frac{DD'T_s}{2L}(r_{ds2} + r_C - r_{ds1}) \text{ or } 1 + \frac{DD'T_s}{2L}(r_d + r_C - r_{ds1}), \\
 q_C &= \frac{DD'T_s}{2L}, \\
 q_{in} &= \frac{DD'T_s}{2L}, \\
 q_{io} &= -\frac{DD'T_s}{2L}r_C,
 \end{aligned} \tag{4.88}$$

yields the PCM small-signal state space as

$$\begin{aligned}
 \begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \begin{bmatrix} -\frac{r_e + F_m V_e q_L}{L} & -\frac{D' + F_m V_e q_C}{L} \\ \frac{D' + F_m I_L q_L}{C} & \frac{F_m I_L q_C}{C} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \\
 &+ \begin{bmatrix} \frac{D - F_m V_e q_{in}}{L} & \left(\frac{D' r_C - F_m V_e q_{io}}{L} \right) / L & \frac{F_m V_e}{L} \\ \frac{F_m I_L q_{in}}{C} & -\frac{1 - F_m I_L q_{io}}{C} & -\frac{F_m I_L}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}, \\
 \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} D - F_m I_L q_L & -F_m I_L q_C \\ 0 & 1 + r_C C \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \\
 &+ \begin{bmatrix} -F_m I_L q_{in} & -F_m I_L q_{io} & F_m I_L \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix},
 \end{aligned} \tag{4.89}$$

where r_e and V_e are defined in Section 3.4.3 (Eqs. (3.65–3.67)). Applying *Laplace* transformation and matrix algebra to Eq. (4.89), the output dynamics can be given by

$$\begin{aligned}
 \Delta G_{io-o} &= \frac{F_m I_L q_{in}}{C} \left(s + \frac{D(D' + F_m I_L q_L) + F_m q_{in}(r_e I_L - D' V_e)}{L F_m I_L q_{in}} \right) (1 + s r_C C), \\
 \Delta Z_{o-o} &= \frac{(1 - F_m I_L q_{io})}{LC} \left(\frac{r_e - D'^2 r_C + F_m V_e q_L + F_m(q_{io}(D' V_e - r_e I_L) - q_L I_L D' r_C)}{1 - F_m^{sp} I_L q_{io}^{sp}} + sL \right) \\
 &\quad (1 + s r_C C), \\
 \Delta G_{co-o} &= \left[F_m(D' V_e - r_e I_L) \left(1 - s \cdot \frac{L I_L}{D' V_e - r_e I_L} \right) (1 + s r_C C) \right] / LC,
 \end{aligned} \tag{4.90}$$

where the denominator (Δ) is defined by

$$\Delta = s^2 + s \left(\frac{r_e + F_m V_e q_L}{L} - \frac{F_m I_L q_C}{C} \right) + \frac{D'^2 + D' F_m (V_e q_C + I_L q_L) - F_m I_L q_C r_e}{LC}. \quad (4.91)$$

The transfer functions corresponding to the input dynamics are extremely long and complicated. Therefore, they are not given explicitly here but they can be solved from the given state space in Eq. (4.87).

The ideal special transfer functions equal the corresponding transfer functions of the DDR-controlled converter given in Section 3.4.3 (Eq. (3.69)). The short-circuit input admittance (Y_{in-sco}) and the open-circuit output impedance (Z_{o-oci}) can be computed based on the transfer functions given in Eqs (4.89) and (4.90) applying their definitions given explicitly in Section 3.4 (Eq. (3.32)), but the resulting symbolic transfer functions are extremely long and, therefore, they are not given here.

In a PCM-controlled buck–boost converter, similar optimal compensation scheme as in the buck converter does not exist. The compensation should be carried out by providing the duty ratio range of 100% by designing $M_{c-100\%}$ as

$$M_{c-100\%} = \frac{V_e}{2L} \approx \frac{V_{in} + V_o}{2L}, \quad (4.92)$$

which is difficult to implement perfectly because of its dependence on the varying input voltage.

The same RHP zero in the control-to-output transfer function (G_{co-o}) as in the DDR-controlled boost converter clearly exists according to Eq. (4.90). The poles of the transfer functions are also highly separated for the similar reason as in a buck converter (i.e., lossless resistor $F_m V_e q_L$), and can be approximated by

$$\begin{aligned} \omega_{p-low} &\approx \frac{D'^2}{F_m (V_{in} + V_o) C}, \\ \omega_{p-high} &\approx \frac{F_m (V_{in} + V_o)}{L}. \end{aligned} \quad (4.93)$$

Similarly as in the buck converter, the use of resistive load for characterizing the converter dynamics would yield highly load-dominated transfer functions, which do not characterize the converter dynamics at all.

4.2.8.4 Superbuck Converter

The linearized state space of the DDR-controlled converter is given in Section 3.4.4 (Eq. (3.76)). Substituting the perturbed duty ratio (\hat{d}) with the derived duty-ratio constraints

$$\begin{aligned}
\hat{d} &= F_m(\hat{i}_{co} - q_{L1}\hat{i}_{L1} - q_{L2}\hat{i}_{L2} - q_{C1}\hat{v}_{C1}), \\
F_m &= 1/\left[T_s\left(M_c + \frac{D' - D}{2}\left(\frac{V_1}{L_1} + \frac{V_2}{L_2}\right)\right)\right], \\
q_{L1} &= 1 + \frac{DD'T_s}{2}\left(\frac{r_{C1} + r_d - r_{ds}}{L_1} + \frac{r_d - r_{ds}}{L_2}\right), \\
q_{L2} &= 1 + \frac{DD'T_s}{2}\left(\frac{r_d - r_{ds}}{L_1} + \frac{r_d - r_{C1} - r_{ds}}{L_2}\right), \\
q_{C1} &= \frac{DD'T_s}{2}\left(\frac{1}{L_1} + \frac{1}{L_2}\right), \\
q_{C2} &= 0, \\
q_{in} &= 0, \\
q_{io} &= 0, \\
V_1 &= V_{in} + V_D + (r_d - r_{ds} + Dr_{C1} - Dr_{L1} + D'r_{L2})I_o, \\
V_2 &= V_1 - r_{C1}I_o,
\end{aligned} \tag{4.94}$$

yields the PCM small-signal state space as

$$\begin{aligned}
\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{v}_{C1}}{dt} \\ \frac{d\hat{v}_{C2}}{dt} \end{bmatrix} &= \begin{bmatrix} \frac{r_{e1} + F_m q_{L1} V_{e1}}{L_1} & \frac{r_{e2} + F_m q_{L2} V_{e1}}{L_1} & \frac{D' + F_m q_{C1} V_{e1}}{L_1} & -\frac{1}{L_1} \\ \frac{r_{e2} + F_m q_{L1} V_{e2}}{L_2} & \frac{r_{e3} + F_m q_{L2} V_{e2}}{L_2} & \frac{D - F_m q_{C1} V_{e2}}{L_2} & -\frac{1}{L_2} \\ \frac{D' + F_m q_{L1} I_o}{C_1} & \frac{D - F_m q_{L2} I_o}{C_1} & \frac{F_m q_{C1} I_o}{C_1} & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} \\
&+ \begin{bmatrix} \frac{1}{L_1} & \frac{r_{C2}}{L_1} & \frac{F_m V_{e1}}{L_1} \\ 0 & \frac{r_{C2}}{L_2} & \frac{F_m V_{e2}}{L_2} \\ 0 & 0 & -\frac{F_m I_o}{C_1} \\ 0 & -\frac{1}{C_2} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}, \\
\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 + r_{C2} C_2 \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix},
\end{aligned} \tag{4.95}$$

where r_{e1} and V_{e1} are defined in Section 3.4.4 (Eq. (3.77)). Applying *Laplace* transformation and matrix algebra to Eq. (4.95), the input dynamics can be

given by

$$\begin{aligned}\Delta Y_{\text{in-o}} &= \frac{1}{L_1} \left(s^3 + s^2 \frac{F_m(V_{e2}C_1 + I_o q_{C1}L_2)}{L_2C_1} + s \frac{C_1 + D(D - F_m(V_{e2}q_{C1} + I_o))C_2}{L_2C_1} - \frac{F_m I_o q_{C1}}{L_2C_1C_2} \right), \\ \Delta T_{\text{oi-o}} &= \frac{1}{L_1C_2} \left(s^2 + s \frac{F_m((V_{e2} - V_{e1})C_1 + I_o q_{C1}L_2)}{L_2C_1} + \frac{D + F_m((V_{e1} - V_{e2})q_{C1} - I_o)}{L_2C_1} \right), \\ \Delta G_{\text{ci-o}} &= \frac{F_m V_{e1}}{L_1} \left(s^3 + s^2 \frac{D'I_o}{V_{e1}C_1} + s \frac{(V_{e1} - V_{e2})C_1 + (D^2V_{e1} + DD'V_{e2})C_2}{V_{e1}L_2C_1C_2} + \frac{I_o}{V_{e1}L_2C_1C_2} \right),\end{aligned}\quad (4.96)$$

and the output dynamics by

$$\begin{aligned}\Delta G_{\text{io-o}} &= \frac{1}{L_1C_2} \left(s^2 - s \frac{F_m I_o q_{C1}}{C_1} + \frac{D - F_m V_{e2} q_{C1}}{L_2C_1} \right), \\ \Delta Z_{\text{o-o}} &= \frac{1}{C_2} \left(s^3 + s^2 \frac{F_m((V_{e2}L_1 + V_{e1}L_2)C_1 - I_o q_{C1}L_1L_2)}{L_1L_2C_1} \right. \\ &\quad \left. + s \frac{D^2L_1 + D^2L_2 + F_m(q_{C1}(V_{e1}D'L_2 - V_{e2}DL_1) + I_o(D'L_2 - DL_1))}{L_1L_2C_1} \right. \\ &\quad \left. + \frac{F_m(DV_{e1} + D'V_{e2})}{L_1L_2C_1} \right), \\ \Delta G_{\text{co-o}} &= \frac{F_m(V_{e1}L_2 + V_{e2}L_1)}{L_1L_2C_2} \left(s^2 + s \frac{(D'L_2 - DL_1)I_o}{(V_{e1}L_2 + V_{e2}L_1)C_1} + \frac{DV_{e1} + D'V_{e2}}{(V_{e1}L_2 + V_{e2}L_1)C_1} \right),\end{aligned}\quad (4.97)$$

where the denominator (Δ) is defined by

$$\begin{aligned}\Delta &= s^4 + s^3 \frac{F_m((V_{e1}L_2 + V_{e2}L_1)C_1 - I_o q_{C1}L_1L_2)}{L_1L_2C_1} \\ &\quad + s^2 \frac{(L_1 + L_2)(C_1 + D^2C_2) + F_m(q_{C1}(V_{e1}D'L_2 - V_{e2}DL_1) + I_o(D'L_2 - DL_1))C_2}{L_1L_2C_1C_2} \\ &\quad + s \frac{F_m((DV_{e1} + D'V_{e2})C_2 - I_o q_{C1}(L_1 + L_2))}{L_1L_2C_1C_2} + \frac{1 + F_m q_{C1}(V_{e1} - V_{e2})}{L_1L_2C_1C_2}.\end{aligned}\quad (4.98)$$

The parasitic elements are neglected in Eqs (4.96)–(4.98) for reducing the complexity and boosting their information content. The state space in Eq. (4.95) contains, however, all the parasitic elements, and by means of it the corresponding transfer functions, including all the parasitic elements can be solved by applying a proper software package such as Matlab™ Symbolic Toolbox.

The ideal special transfer functions equal the corresponding transfer functions of the DDR-controlled converter given in Section 3.4.4 (Eq. (3.84)). The short-circuit input admittance ($Y_{\text{in-sco}}$) and the open-circuit output impedance ($Z_{\text{o-oci}}$) can be computed based on the transfer functions given in Eqs (4.96) and (4.97) applying their definitions given explicitly in Section 3.4 (Eq. (3.32)), but the resulting symbolic transfer functions are extremely long and, therefore, they are not given here.

Similarly as in the DDR-controlled superbuck converter, the control-to-output transfer functions ($G_{\text{co-o}}$) can contain an RHP-zero (cf. Eq. (4.97)). Therefore, the inductors should be designed in such a manner that $L_2 \geq (D_{\text{max}}/D'_{\text{max}})L_1$, where D_{max} denotes the maximum duty ratio within the desired input voltage range.

The low-frequency input noise attenuation in a PCM-controlled superbuck converter (cf. G_{i_o-o} in Eq. (4.97)) can also be maximized by designing the inductor current signal compensation by

$$M_{c-opt} \approx \frac{V_o}{2L_p}, \quad L_p = \frac{L_1 L_2}{L_1 + L_2}, \quad (4.99)$$

which means that $D - F_m V_{e2} q_{C1} \approx 0$.

The complexity of the fourth-order denominator in Eq. (4.98) is such that its roots cannot be anymore approximated similarly as in case of the DDR-controlled superbuck converter. Therefore, the Routh–Hurwitz method should be utilized to estimate the existence of RHP poles, that is, the stability of the converter at open loop. According to the denominator in Eq. (4.98), the polynomial coefficients can be given by

$$\begin{aligned} a_4 &= 1, \\ a_3 &= \left[F_m \left(V_{in} - \frac{DD'T_s I_o}{2C_1} \right) \right] / L_p, \\ a_2 &= \frac{(L_1 + L_2)(C_1 + D^2 C_2) + F_m ((DD'T_s/2L_p) + I_o)(D'L_2 - DL_1)C_2}{L_1 L_2 C_1 C_2}, \\ a_1 &= F_m \left(V_{in} - \frac{DD'T_s I_o L_1 L_2}{2L_p^2 C_2} \right) \frac{1}{L_1 L_2 C_1}, \\ a_0 &= \frac{1}{L_1 L_2 C_1 C_2}. \end{aligned} \quad (4.100)$$

The lowest- and highest-order coefficients are positive. Therefore, all the other polynomial coefficients in Eq. (4.100) and in the leftmost column of Routh's array have to be positive as well. The positive signs of a_1 , a_2 , and a_3 would require that $C_1 > DD'T_s I_o / 2V_{in} = C_{1-min}$, $L_2/L_1 \geq D/D'$, and $C_2 > (L_1 L_2 / L_p^2) \cdot C_{1-min}$, respectively. If the converter satisfies these conditions, then the array element b_1 can be given by

$$b_1 = \frac{1}{L_p} \left(\frac{1}{C_2} + D'_{max}(D'_{max} - D_{max}) \frac{1}{C_1} \right), \quad (4.101)$$

which is a positive number if $C_1/C_2 > D'_{max}(D'_{max} - D_{max})$, where D_{max} is the maximum duty ratio applied for designing L_1 and L_2 . This requirement will be surely fulfilled, because the last term is usually negative in practical design. Similarly, the array element c_1 can be given by

$$c_1 = \frac{F_m V_{in}}{L_1 L_2 C_1} \left(1 - \frac{1}{1 + D'_{max}(D'_{max} - D_{max}) \cdot (C_2/C_1)} \right), \quad (4.102)$$

when $D_{max} > 0.5$ then $D'_{max}(D'_{max} - D_{max}) < 0$ and c_1 would also become negative according to Eq. (4.102) and consequently, the converter would be unstable. The sign of the elements b_2 and d_1 is always positive because of equaling the zeroth-order polynomial coefficient. In practice, the effect of the parasitic elements would maintain the stability of the converter, but it is highly recommended to perform more accurate analysis than presented here.

4.2.8.5 Coupled-Inductor Superbuck Converter

The linearized state space of the DDR-controlled converter is given in Section 3.4.5 (Eq. (3.88)). Substituting the perturbed duty ratio (\hat{d}) with the derived duty-ratio constraints

$$\begin{aligned}
 \hat{d} &= F_m(\hat{i}_{co} - q_{L1}\hat{i}_{L1} - q_{L2}\hat{i}_{L2} - q_{C1}\hat{v}_{C1}), \\
 F_m &= 1 / \left[T_s \left(M_c + \frac{D' - D}{2L_2} (V_{in} + V_D + (r_d - r_{ds} - Dr_{L1} + 2D'r_{L2})I_o) \right) \right], \\
 q_{L1} &= 1 + \frac{DD'T_s}{2L_2} (r_d - r_{ds}), \\
 q_{L2} &= 1 + \frac{DD'T_s}{2L_2} (r_d - r_{ds} + r_{L2}), \\
 q_{C1} &= \frac{DD'T_s}{2L_2}, \\
 q_{C2} &= 0, \\
 q_{in} &= 0, \\
 q_{io} &= 0,
 \end{aligned} \tag{4.103}$$

yields the PCM small-signal state space as

$$\begin{aligned}
 \begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{v}_{C1}}{dt} \\ \frac{d\hat{v}_{C2}}{dt} \end{bmatrix} &= \begin{bmatrix} \frac{\Delta r_{e1} + F_m q_{L1} \Delta V_{e1}}{\Delta L_{12}} & \frac{\Delta r_{e2} + F_m q_{L2} \Delta V_{e1}}{\Delta L_{12}} & \frac{-1 + F_m q_{C1} \Delta V_{e1}}{\Delta L_{12}} & 0 \\ \frac{\Delta r_{e3} + F_m q_{L1} \Delta V_{e2}}{\Delta L_{12}} & \frac{\Delta r_{e4} + F_m q_{L2} \Delta V_{e2}}{\Delta L_{12}} & \frac{D(L_1/L_2) + D' - F_m q_{C1} \Delta V_{e2}}{\Delta L_{12}} & -\frac{1}{L_2} \\ \frac{D' + F_m q_{L1} I_o}{C_1} & \frac{-D - F_m q_{L2} I_o}{C_1} & \frac{F_m q_{C1} I_o}{C_1} & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} \\
 &+ \begin{bmatrix} \frac{1}{\Delta L_{12}} & 0 & \frac{F_m \Delta V_{e1}}{\Delta L_{12}} \\ \frac{1}{\Delta L_{12}} & \frac{r_{C2}}{L_2} & \frac{F_m \Delta V_{e2}}{\Delta L_{12}} \\ 0 & 0 & -\frac{F_m I_o}{C_1} \\ 0 & -\frac{1}{C_2} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}, \\
 \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 + r_{C2} C_2 \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix},
 \end{aligned} \tag{4.104}$$

where Δr_{e1} , ΔL_{12} , and ΔV_{e1} are as follows:

$$\begin{aligned}\Delta r_{e1} &= r_{e1} - r_{e2}, & \Delta r_{e2} &= r_{e2} - r_{e3}, \\ \Delta r_{e3} &= \frac{L_1}{L_2} r_{e2} - r_{e1}, & \Delta r_{e4} &= \frac{L_1}{L_2} r_{e3} - r_{e2}, \\ \Delta L_{12} &= L_1 - L_2, \\ \Delta V_{e1} &= V_{e1} - V_{e2}, & \Delta V_{e2} &= \frac{L_1}{L_2} V_{e2} - V_{e1},\end{aligned}\tag{4.105}$$

and r_{e1} and V_{e1} are as defined in Section 3.4.4 (Eq. (3.77)). Applying *Laplace* transformation and matrix algebra to Eq. (4.104), the input dynamics can be given by

$$\begin{aligned}\Delta Y_{in-o} &= \frac{1}{L_1 - L_2} \left(s^3 + s^2 \frac{F_m(V_{in}C_1 - q_{C1}I_oL_2)}{L_2C_1} + s \frac{C_1 + (D^2 - DF_m(q_{C1}U_{in} + I_o))C_2}{L_2C_1C_2} - \frac{F_mq_{C1}I_o}{L_2C_1C_2} \right), \\ \Delta T_{oi-o} &= \frac{D - F_mI_o}{(L_1 - L_2)L_2C_1C_2}, \\ \Delta G_{ci-o} &= \frac{F_mI_o}{(L_1 - L_2)C_1} \left(s^2 + s \frac{DV_{in}}{I_oL_2} + \frac{1}{L_2C_2} \right),\end{aligned}\tag{4.106}$$

and the output dynamics by

$$\begin{aligned}\Delta G_{io-o} &= \frac{D - F_mq_{C1}V_{in}}{(L_1 - L_2)L_2C_1C_2}, \\ \Delta Z_{o-o} &= \frac{1}{C_2} \left(s^3 + s^2 \frac{F_m(V_{in}C_1 - q_{C1}I_oL_2)}{L_2C_1} \right. \\ &\quad \left. + s \frac{D^2L_1 + D'(1 + D)L_2 - DF_m(q_{C1}V_{in} + I_o)(L_1 - L_2)}{(L_1 - L_2)L_2C_1} + \frac{F_mV_{in}}{(L_1 - L_2)L_2C_1} \right), \\ \Delta G_{co-o} &= \frac{F_mV_{in}}{L_2C_2} \left(s^2 - s \frac{DI_o}{V_{in}C_1} + \frac{1}{(L_1 - L_2)C_1} \right),\end{aligned}\tag{4.107}$$

where the denominator (Δ) is defined by

$$\begin{aligned}\Delta &= s^4 + s^3 \frac{F_m(V_{in}C_1 - q_{C1}I_oL_2)}{L_2C_1} + s^2 \frac{(C_1 + (D^2 - DF_m(q_{C1}V_{in} + I_o))C_2)(L_1 - L_2) + L_2C_2}{(L_1 - L_2)L_2C_1C_2} \\ &\quad + s \frac{F_m(V_{in}C_2 - q_{C1}I_o(L_1 - L_2))}{(L_1 - L_2)L_2C_1C_2} + \frac{1}{(L_1 - L_2)L_2C_1C_2}.\end{aligned}\tag{4.108}$$

The parasitic elements are neglected in Eqs. (4.106)–(4.108) for reducing the complexity and boosting their information content. The state space in Eq. (4.104) contains, however, all the parasitic elements, and by means of it the corresponding transfer functions, including all the parasitic elements can be solved by applying a proper software package such as Matlab Symbolic Toolbox.

The ideal special transfer functions equal the corresponding transfer functions of the DDR-controlled converter given in Section 3.4.5 (Eq. (3.92)). The short-circuit input admittance (Y_{in-sco}) and the open-circuit output impedance (Z_{o-oci}) can be computed based on the transfer functions given in Eqs. (4.106) and (4.107) applying their definitions given explicitly in Section 3.4 (Eq. (3.32)), but the resulting symbolic transfer functions are extremely long and, therefore, they are not given here.

The input-to-output transfer function (G_{io-o}) in Eq. (4.107) indicates that the optimal compensation ($M_{c-opt} \approx V_o/2L_p$) defined in Eq. (4.99) will also nullify G_{io-o} of the coupled inductor PCM-controlled converter. When this optimal compensation is applied, the input dynamics can be given by

$$\begin{aligned} Y_{in-o} &= \frac{1}{L_1 - L_2} \cdot \left[\left(s - \frac{DI_o}{V_{in}C_1} \right) / \left(s^2 - s \frac{DI_o}{V_{in}C_1} + \frac{1}{(L_1 - L_2)C_1} \right) \right], \\ \Delta T_{oi-o} &= \frac{D(1 - (2L_2I_o/T_s D' U_o))}{(L_1 - L_2)L_2C_1C_2}, \\ \Delta G_{ci-o} &= \frac{2L_2I_o}{T_s D' V_o(L_1 - L_2)C_1} \left(s^2 + s \frac{DV_{in}}{I_o L_2} + \frac{1}{L_2C_2} \right), \end{aligned} \quad (4.109)$$

and the output dynamics by

$$\begin{aligned} \Delta G_{io-o} &= 0, \\ \Delta Z_{o-o} &= \frac{1}{C_2} (s^3 + s^2 \frac{2V_{in}C_1 - DD'T_s I_o}{D'V_{in}T_s C_1} \\ &\quad + s \frac{D^2L_1 + D'(1+D)L_2 - (2L_2DI_o/T_s D'V_{in})(L_1 - L_2)}{(L_1 - L_2)L_2C_1} + \frac{2}{D'T_s(L_1 - L_2)C_1}), \\ \Delta G_{co-o} &= \frac{2}{T_s D' C_2} \left(s^2 - s \frac{DI_o}{V_{in}C_1} + \frac{1}{(L_1 - L_2)C_1} \right), \end{aligned} \quad (4.110)$$

where the denominator (Δ) is defined by

$$\Delta = \left(s^2 + s \frac{2}{D'T_s} + \frac{1}{L_2C_2} \right) \left(s^2 - s \cdot \frac{DI_o}{V_{in}C_1} + \frac{1}{(L_1 - L_2)C_1} \right). \quad (4.111)$$

The denominator in Eq. (4.111) shows that there exists two complex poles approximately at $1/\sqrt{L_2C_2}$ and also possibly one or two RHP poles depending on the effect of the parasitic elements. The control-to-output transfer function (G_{co-o}) contains one or two RHP poles approximately at the same frequencies as the RHP poles exist. Even if the zeros and poles are at the frequencies close to each other, we cannot state that they cancel each other. So the application of the coupled inductor technique and designing the input current ripple to be minimized, leads to the situation where the existence of the RHP zero cannot be removed, and the converter may become unstable at open loop.

4.2.9 PCM State Spaces in DCM

The state spaces induced by the PCM control in DCM are given only for the buck, boost, and buck–boost converters. The corresponding transfer functions are not solved explicitly but left for the reader. The solving of the transfer functions is instructed in Section 2.4.1.

4.2.9.1 Buck Converter

The linearized state space of the DDR-controlled converter is given in Section 3.5.1 (Eq. (3.113)). Substituting the perturbed duty ratio (\hat{d}) with the derived duty-ratio constraints

$$\begin{aligned}\hat{d} &= F_m(\hat{i}_{co} - \hat{i}_{L1} - q_o \hat{v}_C - q_{in} \hat{v}_{in}), \\ F_m &= 1 / \left[T_s \left(M_c + \frac{V_{in}(1-M)(M-D)}{LM} \right) \right], \\ q_L &= 1, \\ q_C &= \frac{DT_s}{L} \left(\frac{D}{2M^2} - 1 \right), \\ q_{in} &= \frac{DT_s}{L} \left(1 - \frac{(2-M)D}{2M} \right),\end{aligned}\tag{4.112}$$

yields the PCM small-signal state space as

$$\begin{aligned}\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \begin{bmatrix} -\left(\frac{R_{eq}}{L} \sqrt{\frac{K}{1-M}} + \frac{2F_m V_{in}}{L} \right) & -\left(\frac{1}{L(1-M)} \sqrt{\frac{K}{1-M}} + \frac{2F_m V_{in} q_C}{L} \right) \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \\ &+ \begin{bmatrix} \left(\frac{(2-M)M}{L(1-M)} \sqrt{\frac{K}{1-M}} - \frac{2F_m V_{in} q_{in}}{L} \right) & 0 & \frac{2F_m V_{in}}{L} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}, \\ \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} -\frac{2F_m V_o}{R_{eq}} \sqrt{\frac{1-M}{K}} & -\left(\frac{M^2}{R_{eq}(1-M)} + \frac{2F_m V_o q_C}{R_{eq}} \sqrt{\frac{1-M}{K}} \right) \\ 0 & 1 + r_C C \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \\ &+ \begin{bmatrix} \left(\frac{M^2}{R_{eq}(1-M)} - \frac{2F_m V_o}{R_{eq}} \sqrt{\frac{1-M}{K}} \right) & 0 & \frac{2F_m V_o}{R_{eq}} \sqrt{\frac{1-M}{K}} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}.\end{aligned}\tag{4.113}$$

4.2.9.2 Boost Converter

The linearized state space of the DDR-controlled converter is given in Section 3.5.2 (Eq. (3.122)). Substituting the perturbed duty ratio (\hat{d}) with the derived duty-ratio constraints

$$\begin{aligned}
\hat{d} &= F_m(\hat{i}_{co} - \hat{i}_L - q_o \hat{v}_C - q_{in} \hat{v}_{in}), \\
F_m &= 1 / \left[T_s \left(M_c + \frac{V_{in}(DM-1)}{L(M-1)} \right) \right], \\
q_L &= 1, \\
q_C &= \frac{D^2 T_s}{2L(M-1)^2}, \\
q_{in} &= \frac{DT_s}{L} \left(1 - \frac{DM^2}{2(M-1)} \right),
\end{aligned} \tag{4.114}$$

yields the PCM small-signal state space as

$$\begin{aligned}
\begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \begin{bmatrix} -\left(\frac{R_{eq}}{L} \sqrt{\frac{KM(M-1)}{M}} + \frac{2F_m V_o}{L} \right) & -\left(\frac{1}{L} \sqrt{\frac{KM}{M-1}} + \frac{2F_m V_o q_C}{L} \right) \\ \left(1 + \frac{2F_m V_o}{R_{eq}} \sqrt{\frac{M-1}{KM}} \right) \frac{1}{C} & \frac{2F_m V_o q_C}{R_{eq} C} \sqrt{\frac{M-1}{KM}} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \\
&+ \begin{bmatrix} \left(\frac{M^2}{L} \sqrt{\frac{KM}{M-1}} - \frac{2F_m V_o q_{in}}{L} \right) & 0 & \frac{2F_m V_o}{L} \\ \frac{1}{R_{eq} C} \left(M(M-1) - 2F_m V_o q_C \sqrt{\frac{M-1}{KM}} \right) & -\frac{1}{C} & -\frac{2F_m V_o}{R_{eq} C} \sqrt{\frac{M-1}{KM}} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}, \\
\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 + r_C C \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}.
\end{aligned} \tag{4.115}$$

4.2.9.3 Buck-Boost Converter

The linearized state space of the DDR-controlled converter is given in Section 3.5.3 (Eq. (3.132)). Substituting the perturbed duty ratio (\hat{d}) with the derived duty-ratio constraints

$$\begin{aligned}
\hat{d} &= F_m(\hat{i}_{co} - \hat{i}_L - q_o \hat{v}_C - q_{in} \hat{v}_{in}), \\
F_m &= 1 / \left[T_s \left(M_c + \frac{V_{in}(DM-D)}{LM} \right) \right], \\
q_L &= 1, \\
q_C &= \frac{D^2 T_s}{2LM^2}, \\
q_{in} &= \frac{DT_s}{L} \left(1 - \frac{D(2+M)}{2M} \right),
\end{aligned} \tag{4.116}$$

yields the PCM small-signal state space as

$$\begin{aligned}
 \begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \end{bmatrix} &= \begin{bmatrix} -\left(\frac{R_{eq}\sqrt{K}}{L} + \frac{2F_m(V_{in} + V_o)}{L}\right) & -\left(\frac{\sqrt{K}}{L} + \frac{2F_m(V_{in} + V_o)q_C}{L}\right) \\ \left(1 + \frac{2F_m V_o}{R_{eq}\sqrt{K}}\right) \cdot \frac{1}{C} & \frac{2F_m V_o q_C}{R_{eq} C \sqrt{K}} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \\
 &+ \begin{bmatrix} \frac{M(M+2)\sqrt{K}}{L} - \frac{2F_m(V_{in} + V_o)q_{in}}{L} & 0 & \frac{2F_m(V_{in} + V_o)}{L} \\ -\frac{1}{R_{eq}C} \left(M^2 - \frac{2F_m V_o q_{in}}{\sqrt{K}}\right) & -\frac{1}{C} & -\frac{2F_m V_o}{R_{eq}C\sqrt{K}} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}, \\
 \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} &= \begin{bmatrix} -\frac{2F_m V_o}{R_{eq}\sqrt{K}} & -\frac{2F_m V_o}{R_{eq}\sqrt{K}} \\ 0 & 1 + r_C C \frac{d}{dt} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{M^2}{R_{eq}} - \frac{2F_m V_o q_{in}}{R_{eq}\sqrt{K}} & 0 & \frac{2F_m V_o}{R_{eq}\sqrt{K}} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{i}_{co} \end{bmatrix}.
 \end{aligned} \tag{4.117}$$

4.3 Average Current-Mode Control

4.3.1 Introduction

It is widely assumed that average current-mode control was first time proposed in Ref. [2] but actually the topic was discussed already in late 1970s [21] and its digital implementation was patented in early 1980 [22]. ACM control is widely used in power-factor-correction applications to control the input or inductor current of a boost converter [23]. Photovoltaic generator interfacing is another application area, where the ACM control would provide beneficial contributions as well [24].

Dynamic modeling of ACM control has not attracted similar amount of interest as the PCM control. The first modeling attempts can be traced back to late 1990s [25] and early 2000s [26,27]. The models in Ref. [25] omits the inductor current ripple effects and are, therefore, well suited to be used in digital control applications, where the sampling of the inductor current can be arranged in such a manner that the feedback signal is exactly the time varying average inductor current (i.e., the sampling is timed to half the on-time). As a consequence of this, there are no ripple effects. It was concluded in Refs [28,29] that ACM and PCM controls have similarities depending on how large the residual inductor current ripple in the duty ratio generation is. It was shown that the amount of residual ripple dictates whether the converter dynamics resemble the dynamics under DDR or PCM control. The ACM control affects naturally the low-frequency behavior of the converter despite the amount of inductor current ripple in duty ratio generation.

We introduce only the modeling of ACM control when the inductor current ripple will fully affect the duty-ratio-generation process in CCM operation mode. The ACM models are given as a set of generalized transfer functions similarly as in PCM control (Section 4.2.7).

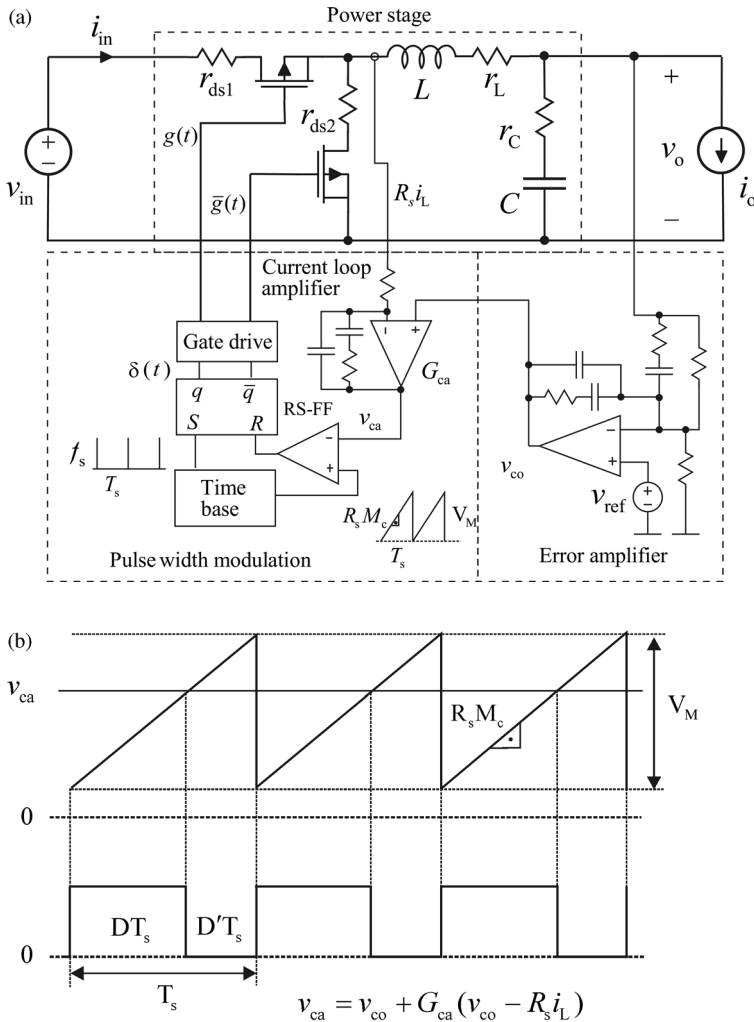


Figure 4.10 ACM control principles. (a) Circuit schematics with a buck converter. (b) Duty ratio generation.

4.3.2 ACM Control Principle

Under analog ACM control, the duty ratio is generated comparing the output signal (v_{ca}) of the current loop amplifier and the constant ramp signal ($R_s M_c$) provided by the PWM modulator shown in Figure 4.10, where R_s denotes the inductor current sensing resistor and M_c the slope of the PWM ramp in current domain. The duty ratio is established when the output signal (v_{ca}) of the current amplifier reaches the PWM ramp signal. The output signal (v_{ca}) can be given by

$$v_{ca} = v_{co} + G_{ca}(v_{co} - R_s i_L), \quad (4.118)$$

where v_{co} denotes the output signal of the voltage loop error amplifier and G_{ca} the transfer function of the current-loop amplifier (cf. Figure 4.10). The

instantaneous inductor current (i_L) can be given as a sum of its time varying average value ($\langle i_L \rangle$) and the triangle-shaped ripple current ($i_{L\text{-ripple}}$). Therefore, the current-loop-amplifier output signal can be given according to Refs [26,27] by

$$v_{ca} = v_{co} + G_{ca}(v_{co} - R_s \langle i_L \rangle) - G_{ca} R_s i_{L\text{-ripple}}. \quad (4.119)$$

The current-loop amplifier is typically a PI-type controller with an extra high-frequency pole, as depicted in Figure 4.10a. The transfer function of a PI controller is actually similar to an averaging filter and, therefore, the control method is known as ACM control. It is obvious according to Eq. (4.119) that the inductor-current ripple may affect the duty-ratio generation, if the extra high-frequency pole or the switching-frequency gain of the current-loop amplifier does not remove the ripple. The models presented in Ref. [25] are based on the assumption that the ripple term in Eq. (4.119) is zero. If the ripple term is not zero, then we can assume that the dynamics of the converter would change from that of zero-ripple condition. In practice, the ACM models exist only in case of zero-ripple [25] or full-ripple [26,27] conditions. The full ripple condition would be valid when the high-frequency zero is placed beyond the switching frequency.

4.3.3 Modeling with Full Ripple Inductor Current Feedback

As discussed in the beginning of this chapter, the fundamental issue is to find the proper duty-ratio constraints in the form of Eq. (4.1). The inductor current loop is provided by an averaging filter or PI controller (cf. Figure 4.10a), which is shown in Figure 4.11a in current domain, that is, the voltage signals are replaced with the corresponding current signals to facilitate the development of the duty ratio constraints. Its transfer function (G_{ca}) can be given by

$$G_{ca} = \frac{1 + sR_f C_f}{sR_{in}(C_f + C_p) \left(1 + sR_f \frac{C_f C_p}{C_f + C_p} \right)}, \quad (4.120)$$

and the corresponding frequency response is given conceptually in Figure 4.11b, where the effect of the location of the extra high-frequency pole (f_p) is explicitly shown. When performing the modeling, we assume that f_p is much higher than the switching frequency (f_s) of the converter. This means that the gain of the current loop amplifier at the switching frequency is $K_f \approx R_f/R_{in}$ (cf. Figure 4.11b), and consequently, the inductor-current switching ripple would be weighted by K_f without any additional phase shift. Therefore, the amplifier output signal in Eq. (4.119) can be given in current domain by

$$i_{ca} = (1 + G_{ca}) \langle i_{co} \rangle - G_{ca} \langle i_L \rangle - K_f i_{L\text{-ripple}}. \quad (4.121)$$

The corresponding duty-ratio-generation process, when taking into account Eq. (4.121), is shown in Figure 4.12, where $\langle i_{ca} \rangle = (1 + G_{ca}) \langle i_{co} \rangle - G_{ca} \langle i_L \rangle$, m_1 , and m_2 are the corresponding inductor-current up and down slopes (Note: m_2 is the absolute value of the instantaneous down slope) and K_f the gain of the current loop amplifier at switching frequency (cf. Figure 4.11b).

According to the already presented duty-ratio-generation process, it may be obvious that Δi_L is the same value as defined in the conjunction with the PCM

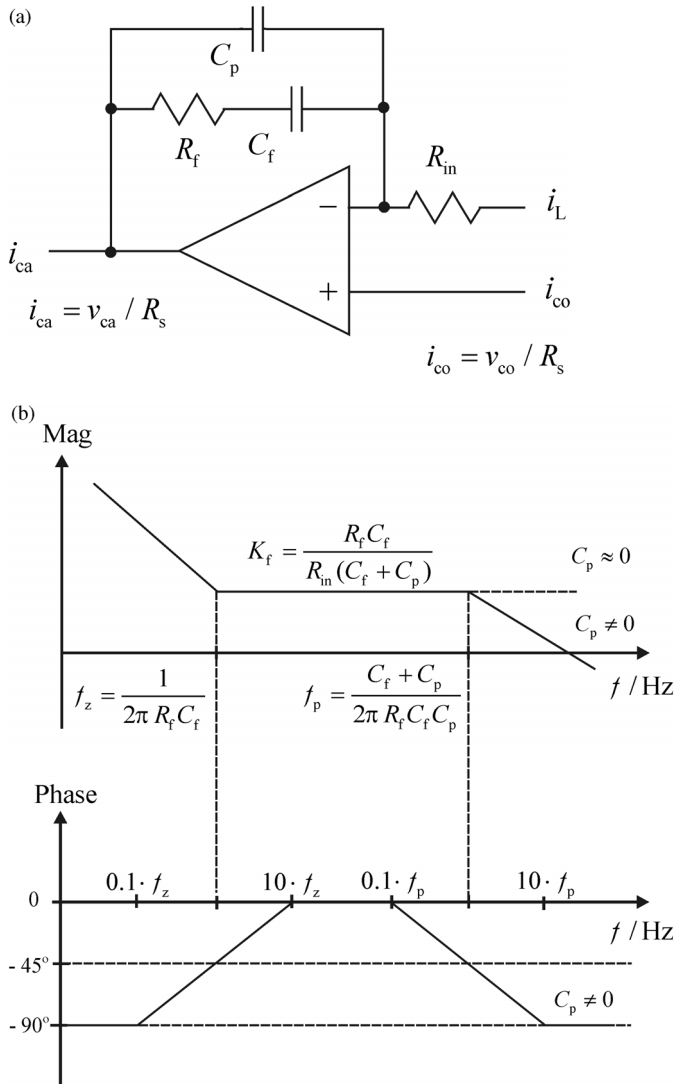


Figure 4.11 Current-loop PI controller. (a) Physical amplifier. (b) Its frequency response.

modeling, that is, $\Delta i_L = dd' T_s (m_1 + m_2) / 2$. This means that the duty-ratio constraints can be given by

$$\hat{d} = \left(1 / \left[T_s \left(M_c + \frac{K_f (D' - D) V_e}{2L} \right) \right] \right) \left((1 + G_{ca}) \hat{i}_{co} - G_{ca} \hat{i}_L - K_f q_{in} \hat{v}_{in} - K_f q_o \hat{v}_o \right), \quad (4.122)$$

by applying the duty-ratio constraints developed for the PCM control in Section 4.2.5 for the buck, boost, and buck–boost converters.

According to Eq. (4.122), it may be obvious that the current-loop-amplifier gain at the switching frequency would have a fundamental influence on the

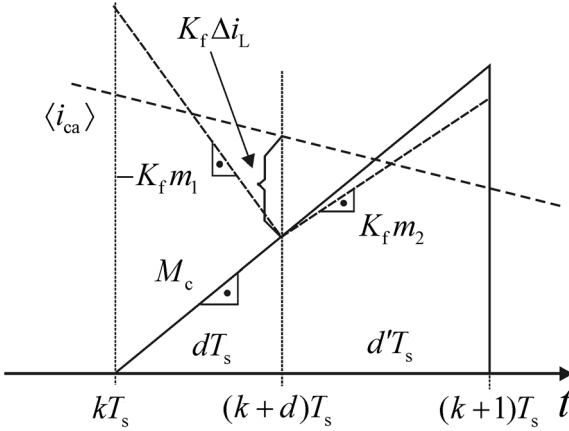


Figure 4.12 The duty-ratio-generation process in current domain.

inductor-current-ripple effects. It may also be obvious that the similar mode limit as in the PCM control does not easily exist, because the inductor-current loop is automatically compensated by means of M_c (i.e., the PWM ramp). Reference [28] provides excessive data on determining the value of F_m for an ACM-controlled buck converter, and coming up to the conclusion that $F_m = 1/R_s T_s M_c = 1/V_M$, where V_M is the peak-to-peak voltage of the PWM ramp. The tests were carried out close to $D = 0.5$, and K_f was also very small. According to Eq. (4.122), the conclusion is evident and correct, because $M_c = V_M/R_s T_s$.

The ACM transfer functions can be most conveniently derived for the basic converters by applying the same technique as in conjunction with the PCM control for deriving the generalized transfer functions in Section 4.2.7. Figure 4.13 shows the required block diagrams, where the coefficients A and B for the basic converters are as follows: buck $A = 1$ and $B = 0$; boost and buck–boost $A = D'$ and $B = I_L$, and q_{in} and q_o as defined in Section 4.2.5 for the corresponding converters.

From Figure 4.13a, we can compute the generalized transfer functions representing input dynamics as a function of the corresponding DDR transfer functions to be as follows:

$$\begin{aligned}
 Y_{in-o} &= Y_{in-o}^{DDR} - \left[\left(F_m \left(q_o + \frac{G_{ca}}{AZ_C} \right) G_{io-o}^{DDR} + q_{in} \right) G_{ci-o}^{DDR} \right] / (1 + L_c + L_v), \\
 T_{oi-o} &= T_{oi-o}^{DDR} + \left\{ \left[F_m \left(\left(q_o + \frac{G_{ca}}{AZ_C} \right) Z_{o-o}^{DDR} - \frac{G_{ca}}{A} \right) G_{ci-o}^{DDR} \right] / [1 + L_c + L_v] \right\}, \\
 G_{ci-o} &= \frac{(1 + G_{ca}) F_m G_{ci-o}^{DDR}}{1 + L_c + L_v}.
 \end{aligned}
 \tag{4.123}$$

From Figure 4.13b, we can compute the generalized transfer functions representing output dynamics as a function of the corresponding DDR transfer functions to be as follows:

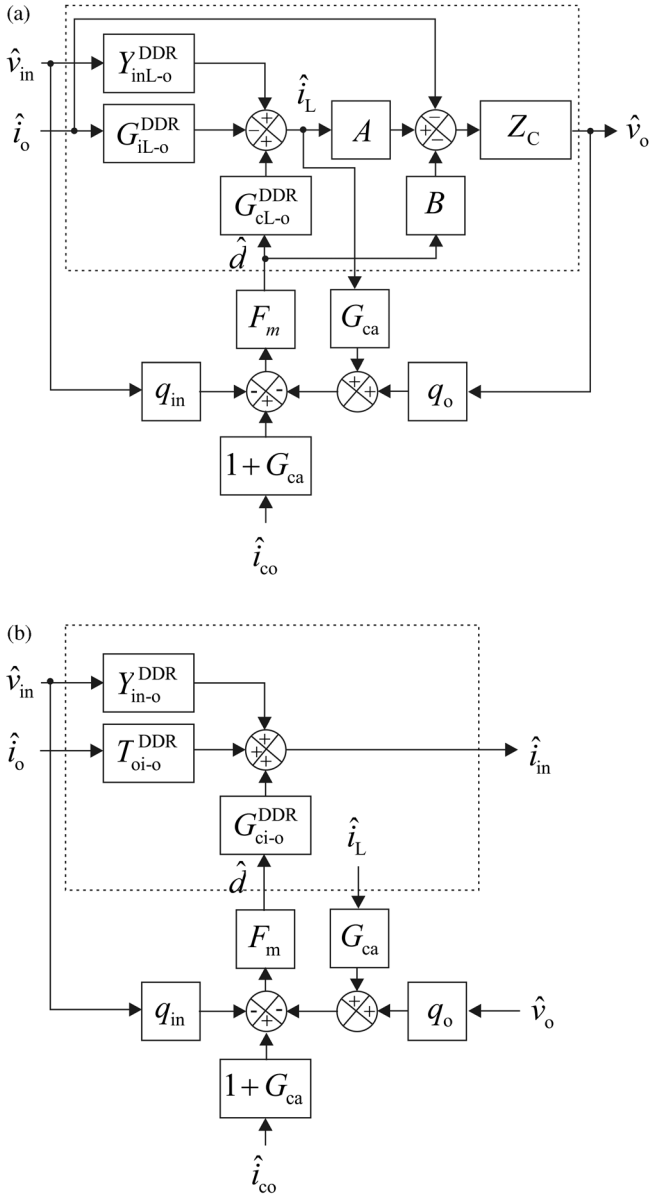


Figure 4.13 Block diagrams for ACM control in CCM. (a) Input dynamics. (b) Output dynamics.

$$\begin{aligned}
G_{io-o} &= \left[\left(1 + \frac{BF_m G_{ca}}{A} \right) G_{io-o}^{DDR} - F_m q_{in} G_{co-o}^{DDR} \right] / [1 + L_c + L_v], \\
Z_{o-o} &= \left[\left(1 + \frac{BF_m G_{ca}}{A} \right) Z_{o-o}^{DDR} + \frac{F_m G_{ca}}{A} G_{co-o}^{DDR} \right] / [1 + L_c + L_v], \\
G_{co-o} &= \frac{(1 + G_{ca}) F_m G_{co-o}^{DDR}}{1 + L_c + L_v},
\end{aligned} \tag{4.124}$$

where the inductor current (L_c) and output voltage (L_v) loops are defined by

$$\begin{aligned}
L_c &= G_{ca} F_m G_{L-o}^{DDR}, \\
L_v &= F_m q_o G_{co-o}^{DDR}.
\end{aligned} \tag{4.125}$$

According to Eqs (4.123) and (4.124), we may conclude the following:

- 1) The control-to-output transfer function (G_{co-o}) incorporates the same RHP zeros as in the corresponding DDR-controlled converter, if any.
- 2) The buck converter may have high input noise attenuation similar to the corresponding PCM-controlled converter depending on the level of ripple effects.
- 3) If K_f is small, then the transfer functions will have features resembling the DDR control. Under digital ACM control $K_f = 0$.
- 4) If K_f is high, then the transfer functions will have features resembling the PCM control.
- 5) We can also verify that the set of special ideal transfer functions derived for the DDR-controlled converters is also valid for the corresponding ACM-controlled converters:

$$\begin{aligned}
Y_{in-\infty}^{ACM} &= Y_{in-o}^{DDR} - \frac{G_{io-o}^{DDR} G_{ci-o}^{DDR}}{G_{co-o}^{DDR}}, \\
Z_{o-\infty}^{ACM} &= Z_{o-o}^{DDR} + \frac{T_{oi-o}^{DDR} G_{co-o}^{DDR}}{G_{ci-o}^{DDR}}, \\
T_{oi-\infty}^{ACM} &= T_{oi-o}^{DDR} + \frac{Z_{o-o}^{DDR} G_{ci-o}^{DDR}}{G_{co-o}^{DDR}}, \\
G_{io-\infty}^{ACM} &= G_{io-o}^{DDR} - \frac{Y_{in-o}^{DDR} G_{co-o}^{DDR}}{G_{ci-o}^{DDR}}.
\end{aligned} \tag{4.126}$$

4.4 Variable-Frequency Control

4.4.1 Introduction

Variable-frequency operation would take places when the termination of the switching cycle is based either on the behavior of inductor current [29] or capacitor voltage [30]. The inductor current-based control belongs naturally to a class of current-mode controls, and the capacitor-voltage-based control to a

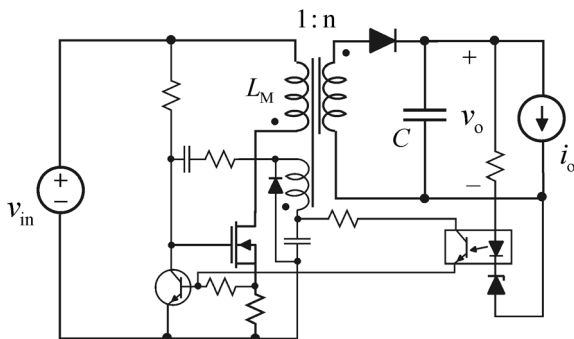


Figure 4.14 A simple self-oscillating flyback converter.

class of voltage-mode controls. Self-oscillation control [3,31–36] – also known as boundary, critical, and transition-mode control – is a mode of peak current mode control, which is typically used in the applications requiring low-EMI or low-cost solutions, such as power factor correction [23] as well as mobile phone and notebook charging [35]. Boost and flyback converters [3,23,35] are the most common converter topologies applied under self-oscillation control. Under self-oscillation control, the cycle is initiated when the inductor current reaches the zero level or after a determined delay of the zero crossing [36]. The on-time is terminated when the inductor reaches the control current. A simple self-oscillating flyback converter used in mobile phone charging application is shown in Figure 4.14 illustrating the implementation of the control principle in its simplest form [3].

The variable-frequency control-mode, where the cycle is initiated, when the inductor current reaches a certain minimum current and the on-time is determined when the inductor current reaches the control current is known as hysteretic current control [37–39]. The hysteretic current-mode control can be implemented either by using constant hysteresis value or by using two different control currents separately for the upper and lower limits.

It has been usually assumed that the dynamics associated with the variable-frequency control is similar to the fixed-frequency DDR control [31,35]. The PCM control and variable switching frequency would, however, change the dynamics requiring special modeling methods to capture it [3,26,27,36]. It has also been noticed that the phase shift of the variable-frequency converters are usually lower than the average models would predict, as is clearly visible in Ref. [39]. Reference [40] provides an extra modulator gain, which would remove the inaccuracy of the average models.

4.4.2 Self-Oscillation Modeling – DOT and PCM Control

The self-oscillating control is a derivative of PCM control, in which the resulting inductor current waveforms are shown in Figure 4.15, when a determined switching delay (T_D) is applied. Similarly to PCM control, we have to find the proper duty-ratio constraints under variable switching frequency. However, the

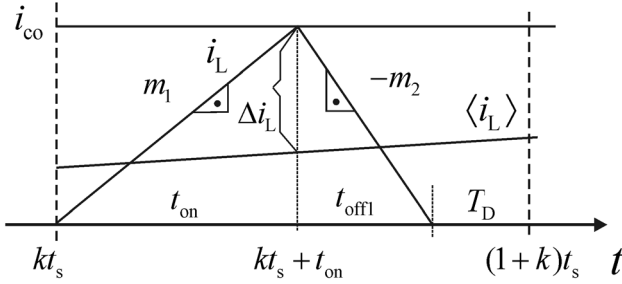


Figure 4.15 Inductor-current waveforms under self-oscillation control.

small-signal state space under DOT control has to be solved before we can proceed with the PCM modeling. The DOT control is not a physical control mode but a fictive mode serving only the purposes of the modeling.

According to Section 3.3, the derivative of the time-averaged inductor current $\langle i_L \rangle$ can be given in general by

$$\frac{d\langle i_L \rangle}{dt} = \frac{t_{on}}{t_s} \cdot m_1 - \frac{t_{off1}}{t_s} \cdot m_2. \quad (4.127)$$

From the inductor current waveforms in Figure 4.15, we can solve t_{off1} by means of $\langle i_L \rangle$ yielding

$$t_{off1} = \frac{2\langle i_L \rangle}{m_2(1 - (T_D/t_s))}. \quad (4.128)$$

Substituting t_{off1} in Eqs (4.127) with (4.128) yields

$$\frac{d\langle i_L \rangle}{dt} = \frac{t_{on}}{t_s} \cdot m_1 - \frac{2}{t_s - T_D}. \quad (4.129)$$

The derivative of the average capacitor voltage ($\langle v_C \rangle$) can be generally given by

$$\frac{d\langle v_C \rangle}{dt} = q_1 \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \quad (4.130)$$

where the coefficient q_1 is as follows: buck $q_1 = 1$, boost and buck–boost $q_1 = 1 - t_{on}/(t_s - T_D)$. The average output voltage ($\langle v_o \rangle$) can be given by

$$\langle v_o \rangle = \langle v_C \rangle + r_C \frac{d\langle v_C \rangle}{dt}, \quad (4.131)$$

and the average input current ($\langle i_{in} \rangle$) by

$$\langle i_{in} \rangle = q_2 \langle i_L \rangle, \quad (4.132)$$

where the coefficient q_2 is as follows: buck and buck–boost $q_2 = t_{on}/(t_s - T_D)$, boost $q_2 = 1$.

As a summary, the general averaged state space under DOT control can be given by

$$\begin{aligned}\frac{d\langle i_L \rangle}{dt} &= \frac{t_{\text{on}}}{t_s} \cdot m_1 - \frac{2}{t_s - T_D}, \\ \frac{d\langle v_C \rangle}{dt} &= q_1 \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\ \langle i_{\text{in}} \rangle &= q_2 \langle i_L \rangle, \\ \langle v_o \rangle &= \langle v_C \rangle + r_C \frac{d\langle v_C \rangle}{dt},\end{aligned}\tag{4.133}$$

where q_1 and q_2 are as already defined.

The steady-state operating point of the converter can be naturally solved from Eq. (4.133) by setting the derivatives to zero and substituting the inductor-current up-slope (m_1) with its topology-based values given in Section 3.3. The operating point can also be given as an equivalent circuit shown in Figure 4.16, where the coefficients of the equivalent circuit and the other operating point variables can be defined for the basic converters as follows:

Buck:

$$\begin{aligned}M\left(D, \frac{T_D}{T_s}\right) &= \frac{D}{1 - (T_D/T_s)}, \\ V_E &= \frac{D' - (T_D/T_s)}{1 - (T_D/T_s)} \cdot V_D, \\ r_E &= r_L + \frac{D}{1 - (T_D/T_s)} \cdot r_{\text{ds1}} + \frac{D' - (T_D/T_s)}{1 - (T_D/T_s)} \cdot r_d, \\ I_L &= I_o, \\ I_{\text{in}} &= \frac{D}{1 - (T_D/T_s)} \cdot I_o.\end{aligned}\tag{4.134}$$

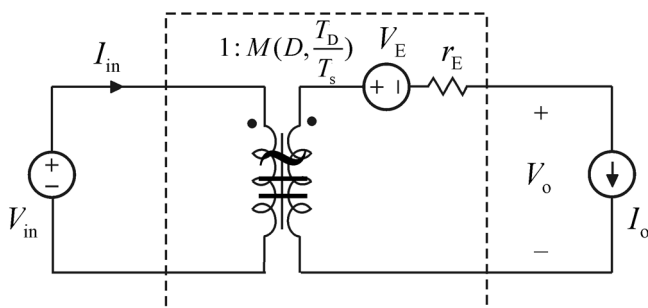


Figure 4.16 The steady-state equivalent circuit for the self-oscillating converter.

Boost:

$$\begin{aligned}
 M\left(D, \frac{T_D}{T_s}\right) &= \frac{1 - (T_D/T_s)}{D' - (T_D/T_s)}, \\
 V_E &= V_D, \\
 r_E &= \frac{(1 - (T_D/T_s))^2}{(D' - (T_D/T_s))^2} \cdot r_L + \frac{D(1 - (T_D/T_s))}{(D' - (T_D/T_s))^2} \cdot r_{ds1} \\
 &\quad + \frac{1 - (T_D/T_s)}{D' - (T_D/T_s)} \cdot r_d + \frac{D}{D' - (T_D/T_s)} \cdot r_C, \\
 I_L &= \frac{1 - (T_D/T_s)}{D' - (T_D/T_s)} \cdot I_o, \\
 I_{in} &= \frac{1 - (T_D/T_s)}{D' - (T_D/T_s)} \cdot I_o.
 \end{aligned} \tag{4.135}$$

Buck–Boost:

$$\begin{aligned}
 M\left(D, \frac{T_D}{T_s}\right) &= \frac{D}{D' - (T_D/T_s)}, \\
 V_E &= V_D, \\
 r_E &= \frac{(1 - (T_D/T_s))^2}{(D' - (T_D/T_s))^2} \cdot r_L + \frac{D(1 - (T_D/T_s))}{(D' - (T_D/T_s))^2} \cdot r_{ds1} \\
 &\quad + \frac{1 - (T_D/T_s)}{D' - (T_D/T_s)} \cdot r_d + \frac{D}{D' - (T_D/T_s)} \cdot r_C, \\
 I_L &= \frac{1 - (T_D/T_s)}{D' - (T_D/T_s)} \cdot I_o, \\
 I_{in} &= \frac{D}{D' - (T_D/T_s)} \cdot I_o.
 \end{aligned} \tag{4.136}$$

The steady-state cycle time (T_s) can be solved from the inductor current waveforms in Figure 4.15 in a general form yielding

$$T_s^2 - \left(2T_D + \frac{2I_1(M_1 + M_2)}{M_1M_2}\right) \cdot T_s + T_D^2 = 0, \tag{4.137}$$

and substituting the topology-based up and down slopes of the inductor current with the values defined in Section 3.3.

The small-signal state space can be derived from the averaged state space in Eq. (4.133) by developing the proper partial derivatives. Under self-oscillation control or generally in the variable-frequency operation, the cycle time (t_s) is also variable. Therefore, we have to also develop proper dynamic constraints (i.e., cycle-time constraints) for the varying cycle time in order to introduce its effect on the dynamics of the converter.

The cycle-time constraints can be obtained from the definition of the cycle time $t_s = t_{on} + t_{off1} + T_D$ by substituting t_{off1} with Eq. (4.128) yielding

$$t_s = t_{on} + \frac{2\langle i_L \rangle}{m_2(1 - (T_D/t_s))} + T_D, \tag{4.138}$$

Table 4.1 Cycle-time constraints.

Converter	F_m^c	q_L^c	q_C^c	q_{in}^c	q_{io}^c
Buck ^{a)}	$1/\left[1 + \frac{2L I_L T_D}{V_o(T_s - T_D)^2}\right]$	$\frac{2L T_s}{V_o(T_s - T_D)}$	$\frac{-2L I_L T_s}{V_o^2(T_s - T_D)}$	0	0
Boost	$1/\left[1 + \frac{2L I_L T_D}{(V_o - V_{in})(T_s - T_D)^2}\right]$	$\frac{2L T_s}{(V_o - V_{in})(T_s - T_D)}$	$\frac{-2L I_L T_s}{(V_o - V_{in})^2(T_s - T_D)}$	$\frac{2L I_L T_s}{(V_o - V_{in})^2(T_s - T_D)}$	0

a) Applies also for the buck–boost converter.

and developing the proper partial derivatives, and formulating the results as

$$\hat{t}_s = F_m^c(\hat{t}_{on} + q_L^c \hat{v}_L + q_C^c \hat{v}_C + q_{in}^c \hat{v}_{in} + q_{io}^c \hat{i}_o). \quad (4.139)$$

The final small-signal state space results when the perturbed cycle time (\hat{t}_s) is substituted with Eq. (4.139) in the linearized form of Eq. (4.113). The cycle-time constraints are presented in Table 4.1, when the power-stage losses are neglected. The losses can be naturally taken into account by considering m_2 accordingly in Eq. (4.138).

The steady-state values of I_L and T_s can naturally be solved from the corresponding operating points given in Eqs (4.134)–(4.136) and the quadratic cycle time equation in Eq. (4.137). We do not give the explicit DOT state spaces but we will leave that for the reader.

In order to obtain the PCM small-signal state space, we have to develop the on-time constraints relating the perturbed on-time (\hat{t}_{on}) to the control current (\hat{i}_{co}) and the other circuit variables and elements similarly as in the fixed-frequency PCM control described in Section 4.2. The comparator equation defining the length of on-time at $t = kt_s + t_{on}$ can be given based on Figure 4.15 by

$$i_{co} = \langle i_L \rangle + \Delta i_L. \quad (4.140)$$

The difference (Δi_L) between the peak inductor current and its time varying average value can be computed to be

$$\Delta i_L = \frac{t_{on} m_1}{2} \left(1 + \frac{T_D}{t_s}\right). \quad (4.141)$$

Therefore, the comparator equation in Eq. (4.140) becomes

$$i_{co} = \langle i_L \rangle + \frac{t_{on} m_1}{2} \left(1 + \frac{T_D}{t_s}\right), \quad (4.142)$$

from which the on-time constraints can be solved by developing the proper partial derivatives and applying the cycle time constraints in Eq. (4.139) yielding

$$\hat{t}_{on} = F_m^o(\hat{i}_{co} - q_L^o \hat{v}_L - q_C^o \hat{v}_C - q_{in}^o \hat{v}_{in} - q_{io}^o \hat{i}_o). \quad (4.143)$$

The generalized perturbed form of (4.142) can be given by

$$\hat{i}_{co} = \hat{i}_L + \frac{M_1}{2} \left(1 + \frac{T_D}{T_s}\right) \hat{t}_{on} + \frac{T_{on}}{2} \left(1 + \frac{T_D}{T_s}\right) \hat{m}_1 - \frac{DM_1 T_D}{2T_s} \hat{t}_s, \quad (4.144)$$

where M_1 is the steady-state up-slope of the inductor current (cf. Section 3.3), and \hat{m}_1 the linearized form of the up-slope. By further processing Eq. (4.144), the on-time constraints can be found. We do not give them here explicitly but will leave the development for the reader. Usually, the dynamic effect of the power-stage losses and the delay (T_D) are insignificant because of heavily damped dynamics of the converters. As a consequence, we give explicitly the state spaces as well as the normal and special transfer functions for the basic converters, where the losses and delay are omitted:

Buck:

$$\begin{aligned}\frac{d\hat{i}_L}{dt} &= -\frac{4}{T_s}\hat{i}_L + \frac{2}{T_s}\hat{i}_{co}, \\ \frac{d\hat{v}_C}{dt} &= \frac{1}{C}\hat{i}_L - \frac{1}{C}\hat{i}_o,\end{aligned}\quad (4.145)$$

$$\hat{i}_{in} = D(2D-1)\hat{i}_L + \frac{DD'T_s}{2L}\hat{v}_C - \frac{D^2D'T_s}{2L}\hat{v}_{in} + DD'\hat{i}_{co},$$

$$\hat{v}_o = \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt}.$$

$$\begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci-o} \\ G_{io-o} & Z_{o-o} & G_{co-o} \end{bmatrix} = \begin{bmatrix} -\frac{D^2D'T_s}{2L} & -\frac{DD'T_s}{s2LC} & \frac{DD'(s^2 + s(2/D'T_s) + (1/LC))}{s(s + (4/T_s))} \\ 0 & \frac{1 + sr_C C}{sC} & \frac{2(1 + sr_C C)}{sT_s C(s + (4/T_s))} \end{bmatrix}\quad (4.146)$$

or

$$\begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci-o} \\ G_{io-o} & Z_{o-o} & G_{co-o} \end{bmatrix} = \begin{bmatrix} -\frac{DI_o}{V_{in}} & -\frac{DI_o}{sCV_o} & \frac{DD'(s^2 + s(V_o/LI_o) + (1/LC))}{s(s + (2D'V_o/LI_o))} \\ 0 & \frac{1 + sr_C C}{sC} & \frac{2(1 + sr_C C)}{sT_s C(s + (2D'V_o/LI_o))} \end{bmatrix},\quad (4.147)$$

where we have applied the identity $T_s = 2LI_L/D'V_o$ (cf. Eq. (4.137)).

The special transfer functions can be computed based on Eq. (4.146) and applying Eq. (3.32) in Chapter 3, which yields

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ Z_{o-oci} & Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} -\frac{D^2D'T_s}{2L} & -\frac{D^2D'T_s}{2L} & \frac{DD'}{2}\left(s + \frac{2}{D'T_s}\right) \\ \frac{1 + sr_C C}{sC} & \frac{(s + (2/D'T_s))(1 + sr_C C)}{C(s^2 + s(2/D'T_s) + (1/LC))} & \frac{D(1 + sr_C C)}{LC(s^2 + s(2/D'T_s) + (1/LC))} \end{bmatrix}\quad (4.148)$$

or

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ Z_{o-oci} & Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} -\frac{DI_o}{V_{in}} & -\frac{DI_o}{V_{in}} & \frac{DD'}{2}\left(s + \frac{V_o}{LI_o}\right) \\ \frac{1 + sr_C C}{sC} & \frac{(s + (V_o/LI_o))(1 + sr_C C)}{C(s^2 + s(V_o/LI_o) + (1/LC))} & \frac{D(1 + sr_C C)}{LC(s^2 + s(V_o/LI_o) + (1/LC))} \end{bmatrix},\quad (4.149)$$

where we have applied the same identity as in developing Eq. (4.147).

In BCM, the average inductor current equals half the peak current, which is defined by the control current. Therefore, it is obvious that $G_{i_{o-o}} = 0$ and $Z_{o-o} = (1 + sr_C C)/sC$ (i.e., the impedance of the output capacitor), because $I_L = I_o = I_{co}/2$, as well as the input admittance and the short-circuit input admittance equal the ideal input admittance ($Y_{in-\infty} \approx -DI_L/V_{in}$). The transfer functions are mainly of first order except the control-related transfer functions.

Boost:

$$\begin{aligned}\frac{d\hat{i}_L}{dt} &= -\frac{4}{T_s}\hat{i}_L + \frac{2}{T_s}\hat{i}_{co}, \\ \frac{d\hat{v}_C}{dt} &= \frac{D'(2D+1)}{C}\hat{i}_L - \frac{DD^2T_s}{2LC}\hat{v}_C + \frac{DD'T_s}{2LC}\hat{v}_{in} - \frac{1}{C}\hat{i}_o - \frac{DD'}{C}\hat{i}_{co}, \\ \hat{i}_{in} &= \hat{i}_L, \\ \hat{v}_o &= \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt}.\end{aligned}\quad (4.150)$$

$$\begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci-o} \\ G_{io-o} & Z_{o-o} & G_{co-o} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{2}{T_s(s+(4/T_s))} \\ \frac{DD'T_s(1+sr_C C)}{2LC(s+(DD^2T_s/2LC))} & \frac{1+sr_C C}{C(s+(DD^2T_s/2LC))} & \frac{2D(1-s(DT_s/2))(1+sr_C C)}{T_s C(s+(DD^2T_s/2LC))(s+(4/T_s))} \end{bmatrix}\quad (4.151)$$

or

$$\begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci-o} \\ G_{io-o} & Z_{o-o} & G_{co-o} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{DV_o}{LI_o(s+(2DV_o/LI_o))} \\ \frac{I_o(1+sr_C C)}{CD'V_o(s+(I_o/CV_o))} & \frac{1+sr_C C}{C(s+(I_o/CV_o))} & \frac{DD'V_o(1-s(LI_o/V_o))(1+sr_C C)}{LCI_o(s+(I_o/CV_o))(s+(2DV_o/LI_o))} \end{bmatrix},\quad (4.152)$$

where we have applied the identity $T_s = 2LI_L/DV_{in}$ (cf. Eq. (4.137)).

The special transfer functions can be computed based on Eq. (4.151) and applying Eq. (3.32) in Chapter 3, which yields

$$\begin{bmatrix} Y_{in-sco} & Y_{in-\infty} & T_{oi-\infty} \\ Z_{o-oci} & Z_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L(s-(2/DT_s))} & \frac{-2}{DD'T_s(s-(2/DT_s))} \\ 0 & \frac{1+sr_C C}{C(s+(DD^2T_s/2LC))} & \frac{DD'T_s(1+sr_C C)}{2LC(s+(DD^2T_s/2LC))} \end{bmatrix}\quad (4.153)$$

or

$$\begin{bmatrix} Y_{\text{in-sco}} & Y_{\text{in-}\infty} & T_{\text{oi-}\infty} \\ Z_{\text{o-oci}} & Z_{\text{o-}\infty} & G_{\text{io-}\infty} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L(s - (V_{\text{in}}/LI_L))} & \frac{-V_{\text{in}}}{D'LI_L(s - (V_{\text{in}}/LI_L))} \\ 0 & \frac{1 + sr_C C}{C(s + (I_o/CV_o))} & \frac{I_o(1 + sr_C C)}{CV_{\text{in}}(s + (I_o/CV_o))} \end{bmatrix}, \quad (4.154)$$

where we have applied the same identity as in developing Eq. (4.152).

In case of a boost converter, the input current does not change due to changes in the input variable, because the input current equals the inductor current, which is totally controlled by the control current. Therefore, $Y_{\text{in-o}}$ and $T_{\text{oi-o}}$ as well as $Y_{\text{in-sco}}$ and $Z_{\text{o-oci}}$ equal naturally zero as also indicated in Eqs (4.151)–(4.154). The converter contains an RHP zero in its output dynamics at $\omega_{z\text{-RHP}} = 2/D'T_s$, which is same as in the DCM boost converter (cf. Section 3.5.2). We may also conclude based on $G_{\text{co-o}}$ in Eq. (4.151) that the maximum control bandwidth would be limited by the size of ESR of the output capacitor because of the requirement of high enough GM.

Buck–Boost:

$$\begin{aligned} \frac{d\hat{i}_L}{dt} &= -\frac{4}{T_s}\hat{i}_L + \frac{2}{T_s}\hat{i}_{\text{co}}, \\ \frac{d\hat{v}_C}{dt} &= \frac{D'(2D+1)}{C}\hat{i}_L - \frac{DD^2T_s}{2LC}\hat{v}_C + \frac{D^2D'T_s}{2LC}\hat{v}_{\text{in}} - \frac{1}{C}\hat{i}_o - \frac{DD'}{C}\hat{i}_{\text{co}}, \end{aligned} \quad (4.155)$$

$$\hat{i}_{\text{in}} = D(D-D')\hat{i}_L + \frac{DD^2T_s}{2L}\hat{v}_C - \frac{D^2D'T_s}{2L}\hat{v}_{\text{in}} + DD'\hat{i}_{\text{co}},$$

$$\hat{v}_o = \hat{v}_C + r_C C \frac{d\hat{v}_C}{dt}.$$

$$\begin{bmatrix} Y_{\text{in-o}} & T_{\text{oi-o}} & G_{\text{ci-o}} \\ G_{\text{io-o}} & Z_{\text{o-o}} & G_{\text{co-o}} \end{bmatrix} = \begin{bmatrix} -\frac{D^2D'T_s s}{2L(s + (DD^2T_s/2LC))} & -\frac{DD^2T_s s}{2LC(s + (DD^2T_s/2LC))} & \frac{DD'(s^2 + s(2/D'T_s) + (D'/LC))}{(s + (DD^2T_s/2LC))(s + (4/T_s))} \\ \frac{D^2D'T_s(1 + sr_C C)}{2LC(s + (DD^2T_s/2LC))} & \frac{1 + sr_C C}{C(s + (DD^2T_s/2LC))} & \frac{2D'(1 - s(DT_s/2))(1 + sr_C C)}{T_s C(s + (DD^2T_s/2LC))(s + (4/T_s))} \end{bmatrix} \quad (4.156)$$

or

$$\begin{bmatrix} Y_{\text{in-o}} & T_{\text{oi-o}} & G_{\text{ci-o}} \\ G_{\text{io-o}} & Z_{\text{o-o}} & G_{\text{co-o}} \end{bmatrix} = \begin{bmatrix} -\frac{D^2I_L s}{V_o(s + (D'I_o/CV_{\text{in}}))} & -\frac{D'I_o s}{CV_{\text{in}}(s + (D'I_o/CV_{\text{in}}))} & \frac{DD'(s^2 + s(V_o/LI_L) + (D'/LC))}{(s + (D'I_o/CV_{\text{in}}))(s + (2D'V_o/LI_L))} \\ \frac{D^2I_L(1 + sr_C C)}{CV_o(s + (D'I_o/CV_{\text{in}}))} & \frac{1 + sr_C C}{C(s + (D'I_o/CV_{\text{in}}))} & \frac{D^2V_o(1 - s(LI_L/V_{\text{in}}))(1 + sr_C C)}{I_L(s + (D'I_o/CV_{\text{in}}))(s + (2D'V_o/LI_L))} \end{bmatrix}, \quad (4.157)$$

where we have applied the identity $T_s = 2LI_L/DV_{\text{in}}$ (cf. Eq. (4.137)).

The special transfer functions can be computed based on Eq. (4.156) and applying Eq. (3.32) in Chapter 3, which yields

$$\begin{bmatrix} Y_{\text{in-sco}} & Y_{\text{in-}\infty} & T_{\text{oi-}\infty} \\ Z_{\text{o-oci}} & Z_{\text{o-}\infty} & G_{\text{io-}\infty} \end{bmatrix} = \begin{bmatrix} -\frac{DD^2T_s}{2L} & \frac{D}{L(s-(2/DT_s))} & \frac{-(s+(2/D'T_s))}{(s-(2/DT_s))} \\ \frac{1+sr_C C}{sC} & \frac{(s+(2/D'T_s))(1+sr_C C)}{C(s^2+s(2/D'T_s)+(D'/LC))} & \frac{D(1+sr_C C)}{LC(s^2+s(2/D'T_s)+(D'/LC))} \end{bmatrix} \quad (4.158)$$

or

$$\begin{bmatrix} Y_{\text{in-sco}} & Y_{\text{in-}\infty} & T_{\text{oi-}\infty} \\ Z_{\text{o-oci}} & Z_{\text{o-}\infty} & G_{\text{io-}\infty} \end{bmatrix} = \begin{bmatrix} -\frac{D'I_o}{CV_{\text{in}}} & \frac{D}{L(s-(V_{\text{in}}/LI_L))} & \frac{-(s+(V_o/LI_L))}{(s-(V_{\text{in}}/LI_L))} \\ \frac{1+sr_C C}{sC} & \frac{(s+(V_o/LI_L))(1+sr_C C)}{C(s^2+s(V_o/LI_L)+(D'/LC))} & \frac{D(1+sr_C C)}{LC(s^2+s(V_o/LI_L)+(D'/LC))} \end{bmatrix}, \quad (4.159)$$

where we have applied the same identity as in developing Eq. (4.157).

The converter contains an RHP zero in its output dynamics at $\omega_{z\text{-RHP}} = 2/DT_s$, which equals the RHP zero in the DCM buck–boost converter (cf. Section 3.5.3). We may also conclude based on $G_{\text{co-o}}$ in Eq. (4.156) that the maximum control bandwidth would be limited by the size of ESR of the output capacitor because of the requirement of high enough GM.

In general, the averaging technique applied here would not yield very accurate high-frequency phase responses but the phase shift is slightly less than the practical measurements would yield. This inaccuracy can be corrected by applying the information given in Ref. [40], where the correction factor for the phase is given by $e^{sT_{\text{off}}/2}$. This will increase the phase by $\omega T_{\text{off}}/2$.

4.5 Source and Load Interactions

The basic formulations solving the source and load interaction in case of voltage-fed voltage-output (VF/VO) converters are explicitly presented in Section 3.6. Under different current-mode controls, the input-to-output noise attenuation at open loop (i.e., $G_{\text{io-o}}$) can be very high (i.e., $G_{\text{io-o}} \approx 0$). In addition, the current-output nature of the converters means that their output impedance ($Z_{\text{o-o}}$) is usually rather high, especially at the low frequencies. These two properties yield positive contributions especially to the source and load dynamics of a buck converter in terms of increased insensitivity to external impedance interactions [41]. In order to better understand the origin of these improvements, the source (cf. Eq. (4.160)) and load (cf. Eq. (4.162)) interaction formulations are given in Eqs (4.160–4.163), including also the formulation for the closed-loop

input admittance under output voltage control (Y_{in-c}) from Section 2.2.3.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \frac{Y_{in}}{1 + Z_S Y_{in}} & \frac{T_{oi}}{1 + Z_S Y_{in}} & \frac{G_{ci}}{1 + Z_S Y_{in}} \\ \frac{G_{io}}{1 + Z_S Y_{in}} & -\frac{1 + Z_S Y_{in-sco}}{1 + Z_S Y_{in}} Z_o & \frac{1 + Z_S Y_{in-\infty}}{1 + Z_S Y_{in}} G_{co} \end{bmatrix} \begin{bmatrix} \hat{v}_{inS} \\ \hat{v}_o \\ \hat{d} \end{bmatrix}, \quad (4.160)$$

where

$$\begin{aligned} Y_{in-sco} &= Y_{in} + \frac{G_{io} T_{oi}}{Z_o}, \\ Y_{in-\infty} &= Y_{in} - \frac{G_{io} G_{ci}}{G_{co}}, \end{aligned} \quad (4.161)$$

$$Y_{in-c} = \frac{Y_{in-o}}{1 + L_{out}} + \frac{L_{out}}{1 + L_{out}} Y_{in-\infty}.$$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \frac{1 + Y_L Z_{in-ocin}}{1 + Z_o Y_L} Y_{in} & \frac{T_{oi}}{1 + Z_o Y_L} & \frac{1 + Y_L Z_{o-\infty}}{1 + Z_o Y_L} G_{ci} \\ \frac{G_{io}}{1 + Z_o Y_L} & -\frac{Z_o}{1 + Z_o Y_L} & \frac{G_{co}}{1 + Z_o Y_L} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{oL} \\ \hat{d} \end{bmatrix}. \quad (4.162)$$

$$\begin{aligned} Z_{on-oci} &= Z_o + \frac{G_{io} T_{oi}}{Y_{in}} = \frac{Z_o}{Y_{in}} Y_{in-sco}, \\ Z_{o-\infty} &= Z_o + \frac{T_{oi} G_{co}}{G_{ci}}. \end{aligned} \quad (4.163)$$

According to Eq. (4.161), $Y_{in-o} \approx Y_{in-c} \approx Y_{in-sco} \approx Y_{in-\infty}$ if $G_{io-o} \approx 0$. It is also well known that the ideal input impedance of the buck converter equals approximately $-V_{in}/I_{in}$. As a consequence, the output impedance (Z_o) and output voltage loop gain ($L_{out} \approx G_{co-o}$) will stay intact, because the numerator and denominator terms in the corresponding formulas are equal and effectively would cancel each other. When the input impedance equals the ideal input impedance at open and closed loop, which is independent of frequency, the converter may become unstable both at open and closed loop at any frequencies due to the source impedance interactions. Therefore, it is extremely important that there is no overlap with the input impedance of the converter and the source impedance as well as that the GM of the corresponding impedance ratios would be high enough for preventing the excess peaking to affect the converter dynamics.

According to Eq. (4.163), $Z_{o-o} \approx Z_{o-oci}^o$ and $Z_{o-c} \approx Z_{o-oci}^c$ if $G_{io-o} \approx 0$. As a consequence, the load impedance does not affect the input impedance of the converter, because the numerator and denominator terms are equal, thus canceling effectively each other.

4.5.1 Output Current Feedforward

According to Eq. (4.162), we may conclude that the load impedance does not affect the converter dynamics if the output impedance (Z_o) can be made zero, as

discussed in Section 3.6.4 including the relevant formulation for obtaining the goal by means of output current feedforward control [42–44]. It was also explicitly stated that in case of DDR-controlled converter that the goal is difficult to fulfill. In case of different CM controls, the zero-impedance condition is not anymore impossible to be fulfilled in a buck converter.

According to Eq. (3.147), the feedforward gain should be

$$H_c = \frac{R_{s1}}{R_{s2}} \cdot \frac{Z_{o-o}}{G_{co-o}}, \quad (4.164)$$

for obtaining the zero-output impedance in case of CM control, where R_{s1} and R_{s2} denote the inductor-current and output-current sensing resistors, respectively. According to this, the required feedforward gain of a PCM-controlled buck converter would be approximately

$$H_c \approx \frac{R_{s1}}{R_{s2}} \left(1 + s \frac{D'T_s}{2} \right) \approx \frac{R_{s1}}{R_{s2}}, \quad (4.165)$$

when the optimal inductor current loop compensation ($M_c = V_o/2L$) is utilized. Eq. (4.165) indicates that basically the unity feedforward gain would yield highly reduced open-loop output impedance, as discussed and also demonstrated in Refs [43,44]. When applying the unity feedforward gain (cf. Eq. (4.165)), the affected transfer functions of the PCM-controlled buck converter (i.e., Z_{o-o} and T_{oi-o}) (cf. Eq. (3.146)) can be given by

$$\begin{aligned} Z_{o-o} &= \left[(r_e - r_C + (q_L - \frac{R_{s2}}{R_{s1}})F_m V_e + sL)(1 + sr_C C) \right] / \left[LC \left(s^2 + s \frac{r_e + F_m V_e q_L}{L} + \frac{1}{LC} \right) \right], \\ T_{oi-o} &= \left\{ \frac{\left[(D - F_m I_o q_L) \left(1 + s \left(r_C + \frac{R_{s2}}{R_{s1}} F_m V_e \right) C \right) \right]}{\left[LC \left(s^2 + s \frac{r_e + F_m V_e q_L}{L} + \frac{1}{LC} \right) \right]} \right\} + \frac{R_{s2}}{R_{s1}} F_m I_o. \end{aligned} \quad (4.166)$$

Equation (4.166) indicates that the zeros of the open-loop output impedance would equal the zeros of the DDR-controlled buck converter, and the poles would equal the poles of the PCM-controlled buck converter, when the current sensing resistors are equal. This means that the magnitude of the output impedance would be rather small (cf. Figure 4.17). If the sensing resistors are not equal, the magnitude would increase along the increase in the mismatch (cf. Figure 4.17). In addition, the phase of the output impedance would start at low frequencies at -180 degrees, if $R_{s2} > R_{s1}$, which would also affect slightly the transient response (i.e., causing an extra overshoot) (cf. Figure 4.17) [44].

The application of the output current feedforward would also change the short-circuit input admittance (Y_{in-sco}), and the open-circuit output impedance (Z_{o-oci}). Y_{in-sco} can be given as follows:

$$Y_{in-sco} = \frac{(D - F_m V_e q_{in})(D - F_m I_o (q_L - (R_{s2}/R_{s1})))}{sL + r_e - r_C + F_m V_e (q_L - (R_{s2}/R_{s1}))} - F_m q_{in} I_o, \quad (4.167)$$

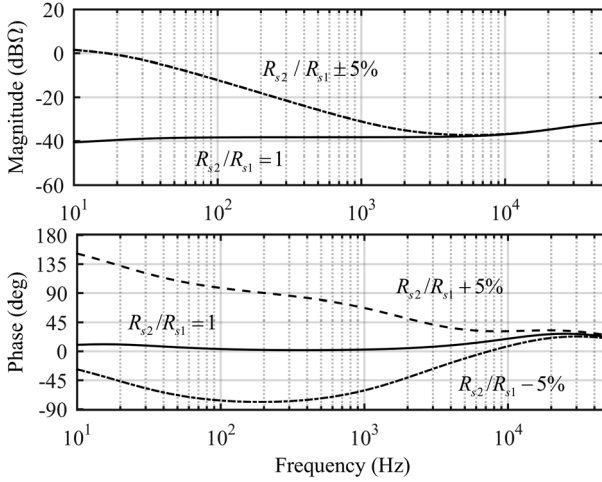


Figure 4.17 The open loop output impedance of PCM-OCF-controlled buck converter when the inductor current loop is compensated by using the optimal compensation (i.e., $M_c = V_o/2L$) and the current sensing resistor ratio is varying.

and Z_{o-oci}^x can be computed based on

$$Z_{o-oci}^x = \frac{Z_{o-x}}{Y_{in-x}} Y_{in-sco}, \quad (4.168)$$

where the superscript and subscript extension x denotes open (“o”) or closed (“c”) loop, respectively. All the other special parameters are the same as given for a buck converter in Section 3.4.

Eq. (4.167) indicates that Y_{in-sco} would equal the ideal input admittance ($Y_{in-\infty} = -F_m q_{in} I_o \approx -I_{in}/V_{in}$) if the inductor current loop compensation (M_c) is designed in such a manner that $G_{io-o} = 0$ (i.e., $M_c = DV_e/2L$). Usually the required compensation cannot be fulfilled, and Y_{in-sco} would deviate from the ideal input admittance depending on the value of the sensing resistor ratio (R_{s2}/R_{s1}).

Figure 4.18 illustrates the effects of the inductor current loop compensation and the current sensing resistor ratio on the short-circuit input impedance. The optimal compensation ($M_c = V_o/2L$) does not actually nullify G_{io-o} , and therefore, Z_{in-sco} is lower than the ideal impedance, when the resistor ratio is unity, as seen in Figure 4.18. When the resistor ratio deviates from unity, Z_{in-sco} approaches the ideal input impedance, as seen in Figure 4.18.

Figure 4.19 illustrates the effect of the inductor-current-loop compensation on the short-circuit input impedance, which clearly indicate that the over compensation decreases the magnitude making the converter more sensitive to the input-source interactions via the short-circuit input impedance compared to the original PCM-controlled buck converter.

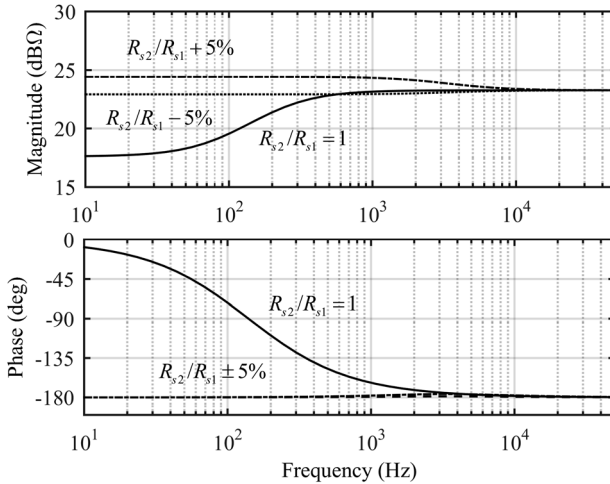


Figure 4.18 The behavior of the short-circuit input impedance (Z_{in-sco}) when the optimal compensation is utilized and the current sensing resistor ratio is varying.

4.6 Impedance-Based Stability Issues

Similarly as in Chapter 3, we can state the stability boundary for the source (Z_S) and load (Z_L) impedances based on

$$\begin{aligned} Z_S &= |Z_{in}| \angle \varphi_{Z_{in}} + 180^\circ, \\ Z_L &= |Z_o| \angle \varphi_{Z_o} - 180^\circ, \end{aligned} \tag{4.169}$$

and the behavior of the closed-loop input and output impedances. Figures 4.21a and 4.21b show the closed-loop input and output impedances of the PCM-controlled

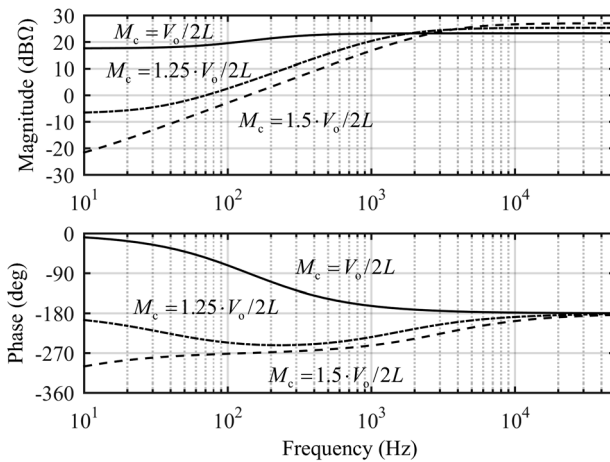


Figure 4.19 The behavior of the short-circuit input impedance (Z_{in-sco}) when the inductor current loop optimal compensation is varied compared to the optimal compensation and the current sensing resistor ratio is kept at unity.

buck converter (cf. Figure 4.20). Figure 4.21c shows the closed-loop output impedance of the PCM-OCF-controlled buck converter. Its closed-loop input impedance is the same as shown in Figure 4.21a.

Based on the given information, we can state that the PCM and PCM-OCF-controlled buck converters are very sensitive to resonant-type (i.e., input LC filter) at very wide frequency range on the contrast to the DDR-controlled buck converter discussed Section 3.6.5. The closed-loop output impedances indicate that the converters are not sensitive to any kind of passive loads. The only type of load, which has theoretical possibility to make the converter unstable is another converter equipped with an input LC filter and exhibiting negative incremental resistance behavior. The low magnitude of the output impedance would imply that it is not very likely at all.

4.7 Dynamic Review

The dynamic models derived for the CCM-converters are known to be quite accurate in the frequency range of interest [6]. The only exception is the phase behavior of the PCM-controlled converters where the control-related models given in this chapter predict slightly less phase shift than the experimental frequency responses indicate. Therefore, we concentrate in this section to the issues which are not so well known and understood. The experimental buck converter is given in Figure 4.20 and the measurements are performed at the input voltage of 20 V and in the output conditions described in Figure 4.20. The input LC filter and output resonant load are the same as applied also in Chapter 3 having resonant frequency close to 500 Hz.

Figure 4.22 shows all the input impedances of the PCM-controlled buck converter and the output impedance of the input LC filter. All the input impedance are effectively the same, and therefore, all the source interactions are canceled, because the numerator and denominator terms are the same, and thus canceling each other (cf. Eq. (4.160)).

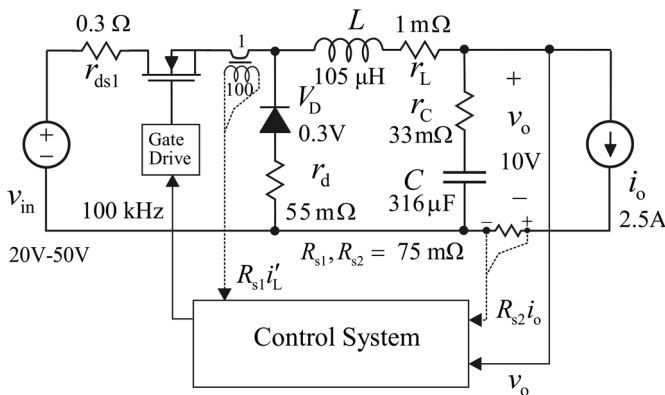


Figure 4.20 The power stage of the experimental buck converter.

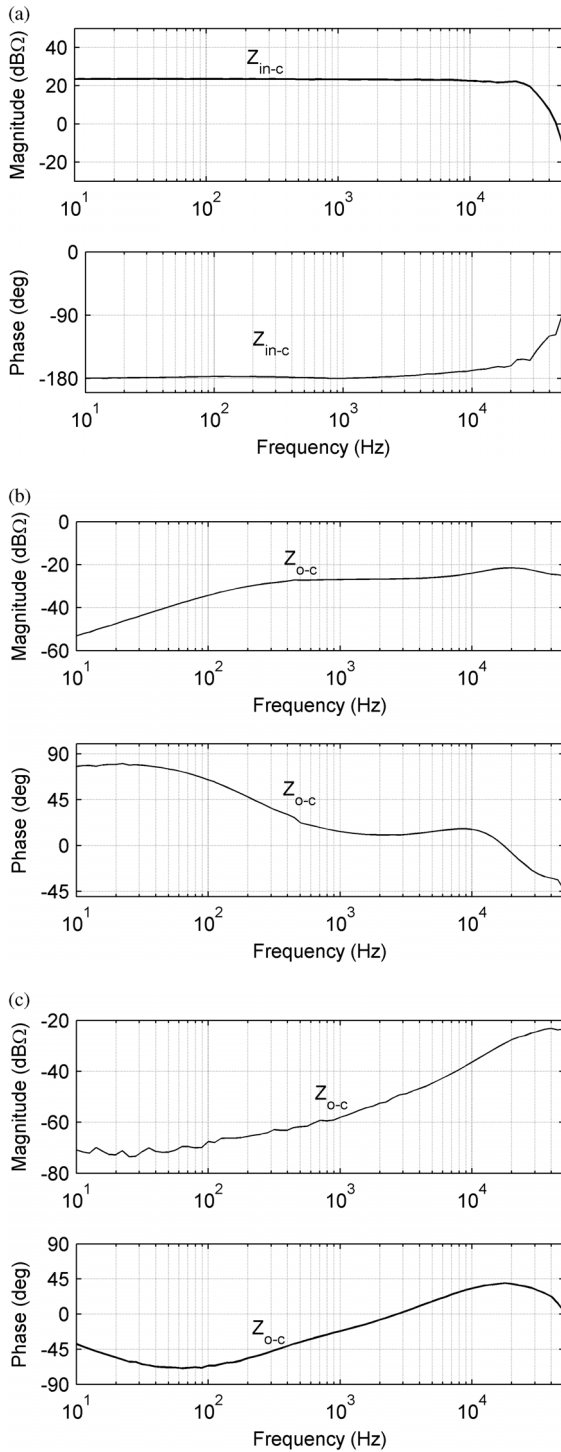


Figure 4.21 The measured closed-loop (a) input impedance, (b) the closed-loop output impedance of the PCM-controlled buck converter, and (c) the closed-loop output impedance of the PCM-OCF-controlled buck converter.

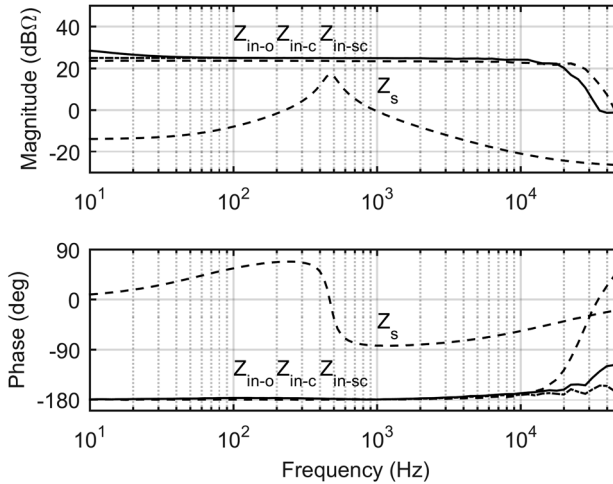


Figure 4.22 The measured input impedances of the experimental PCM-controlled buck converter and the output impedance of the input LC filter.

Figure 4.23 shows all the input impedances of the PCM-OCF-controlled buck converter and the output impedance of the input LC filter. As discussed earlier, the magnitude of the short-circuit input impedance (Z_{in-sc}) is slightly reduced and overlap takes place between the short-circuit and input-filter output impedance. This implies that the open- and closed-loop output impedances would be equally slightly affected as Figure 4.24 clearly shows (Note: The short-circuit input impedance contributes equally to the open- and closed-loop output impedances because it is the same regardless of the state of output-side feedback). The changes in the output impedance are very small and do not affect the load transient response.

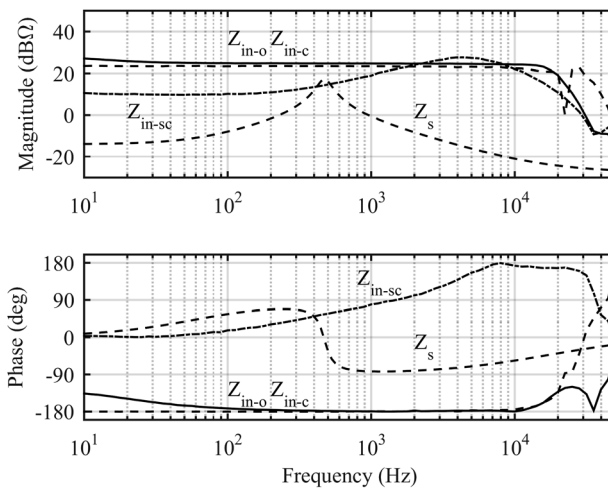


Figure 4.23 The measured input impedances of the experimental PCM-OCF-controlled buck converter and the output impedance of the input LC filter.

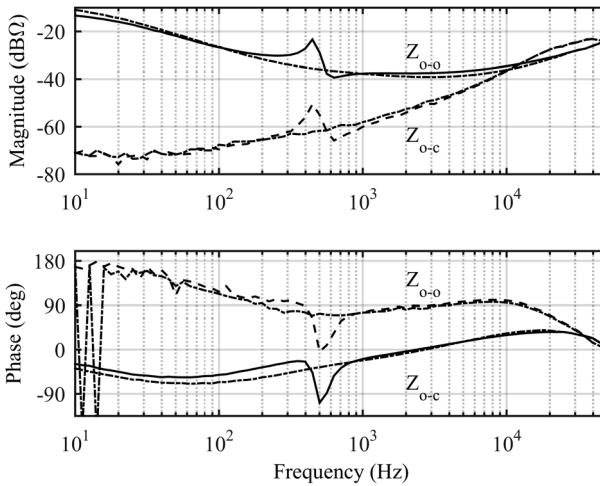


Figure 4.24 The measured open and closed-loop output impedances of the experimental PCM-OCF-controlled buck converter.

Figure 4.25 shows the load-transient responses of the PCM and PCM-OCF-controlled buck converters to a step change in the output current. The figure shows that the settling time of the PCM-OCF-controlled buck converter is very fast compared to the PCM-controlled buck converter. In the load transient of the PCM-OCF-controlled converter, a small overshoot in output voltage is visible. Figure 4.26 shows the measured output voltage loop gains, which are identical for both of the converters as expected based on the theoretical models. Figure 4.27 shows the measured closed-loop output impedances of the converters. According to Figure 4.27, the phase of the PCM-OCF-controlled buck converter starts from 180 degrees at the low frequencies, which causes the small overshoot in the

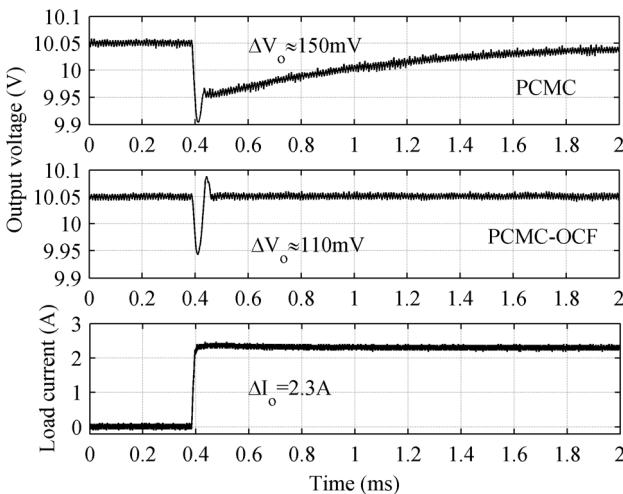


Figure 4.25 The load-transient responses of the PCM and PCM-OCF-controlled buck converter.

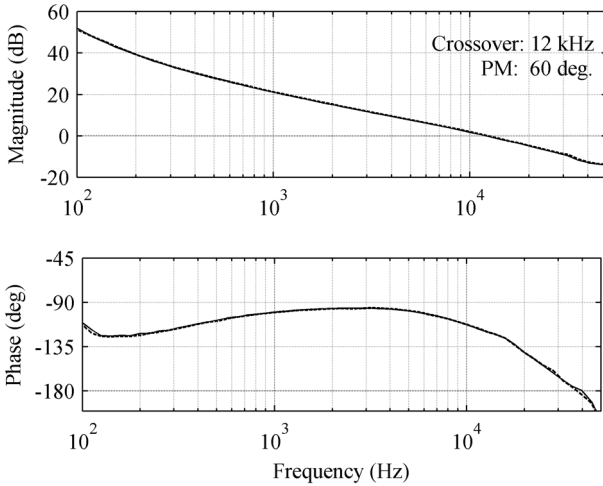


Figure 4.26 The measured output voltage loop gains of the PCM and PCM-OCF-controlled buck converters.

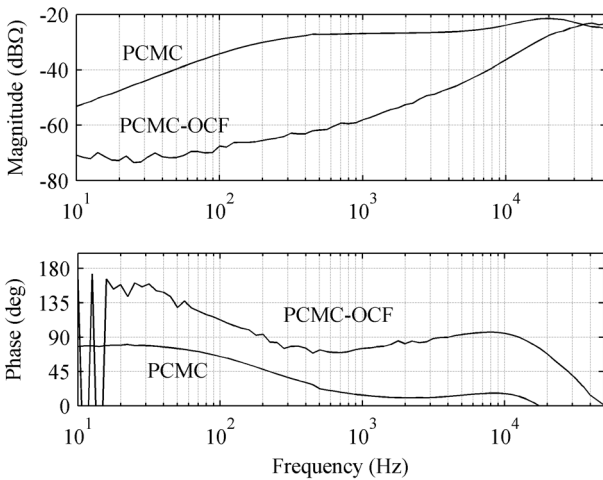


Figure 4.27 The measured closed-loop output impedances of the PCM and PCM-OCF-controlled buck converters.

transient response (cf. Figure 4.25) as discussed earlier. The magnitudes of the output impedances at the output-voltage-loop crossover frequency (i.e., at 12 kHz) are 73 m Ω (PCM) and 22 m Ω (PCM-OCF). The voltage dip of the PCM-controlled buck converter corresponds well to the magnitude of the output impedance at the voltage loop crossover frequency and the applied step change in the output current. The voltage dip of the PCM-OCF-controlled converter is a little bit higher than the magnitude of the output impedance and step change in the output current would yield.

4.8 Critical Discussions on PCM Models and Their Validation

As we have stated explicitly earlier, the inductor current feedback in a current-mode-controlled converter will change the converter as a current source [1], which can operate at open loop either loaded by a resistor or a constant voltage-type load. The converters are, however, operated usually as output voltage feedback-controlled voltage sources. Therefore, the transfer functions have to correspond also to the same mode of output terminal operation. Neither of the named loads would allow to measure directly the required transfer functions. If a resistor is used as the load, then the corresponding transfer functions are resistive load affected and do not suffice for validating the modeling methods. If the constant voltage-type terminal source is used as the load, then the transfer functions will correspond to the current-output mode of operation (i.e., the Y -parameters). The most usual case is to use a resistor as a load, as in Refs [9–12,45,46], which will hide the real low-frequency behavior of the corresponding transfer functions as well. The validation of the PCM models by means of the practical measurements is also very difficult, because even small parasitic components will easily dominate especially the high-frequency measurements, as is clearly visible, for example, in Ref. [45]. Actually, the only feasible method to validate the models is to use deterministic simulation models from which the frequency responses can be usually accurately measured. In this section, we will validate the accuracy of the PCM models of the buck converter presented in Section 4.2 and the models derived by Dr. Raymond Ridley in Ref. [10]. We will also provide a feasible method to compute the frequency responses based on Ridley's method. In addition, we will show that the PCM models of the book can be made very accurate as well. The frequency responses presented in this section are measured by using the pseudorandom binary sequence method introduced in Refs [47,48].

4.8.1 Ridley's Models

The frequency responses based on Ridley's models can be computed based on the general transfer functions given in Eqs (4.170) and (4.171), which are modified from Eqs (4.67) and (4.68) (cf. Figure 4.28). The parameters k_f , k_r , F_m , Q_s , and ω_s are defined in Table 4.2. The transfer functions with the superscript "DDR" are defined in Table 4.2.

Table 4.2 Ridley's model parameters for buck, boost and buck–boost converters.

Converter	F_m	F_c	k_f	k_r	Q_s	ω_s
Buck	$\frac{1}{T_s(M_1 + M_c)}$	$\frac{1}{R_s}$	$-\frac{DT_s}{L} \left(1 - \frac{D}{2}\right)$	$\frac{T_s}{2L}$	$-\frac{2}{\pi}$	$\frac{\pi}{T_s}$
Boost	$\frac{1}{T_s(M_1 + M_c)}$	$\frac{1}{R_s}$	$-\frac{T_s}{2L}$	$\frac{D^2 T_s}{2L}$	$-\frac{2}{\pi}$	$\frac{\pi}{T_s}$
Buck–Boost	$\frac{1}{T_s(M_1 + M_c)}$	$\frac{1}{R_s}$	$-\frac{DT_s}{L} \left(1 - \frac{D}{2}\right)$	$\frac{D^2 T_s}{2L}$	$-\frac{2}{\pi}$	$\frac{\pi}{T_s}$

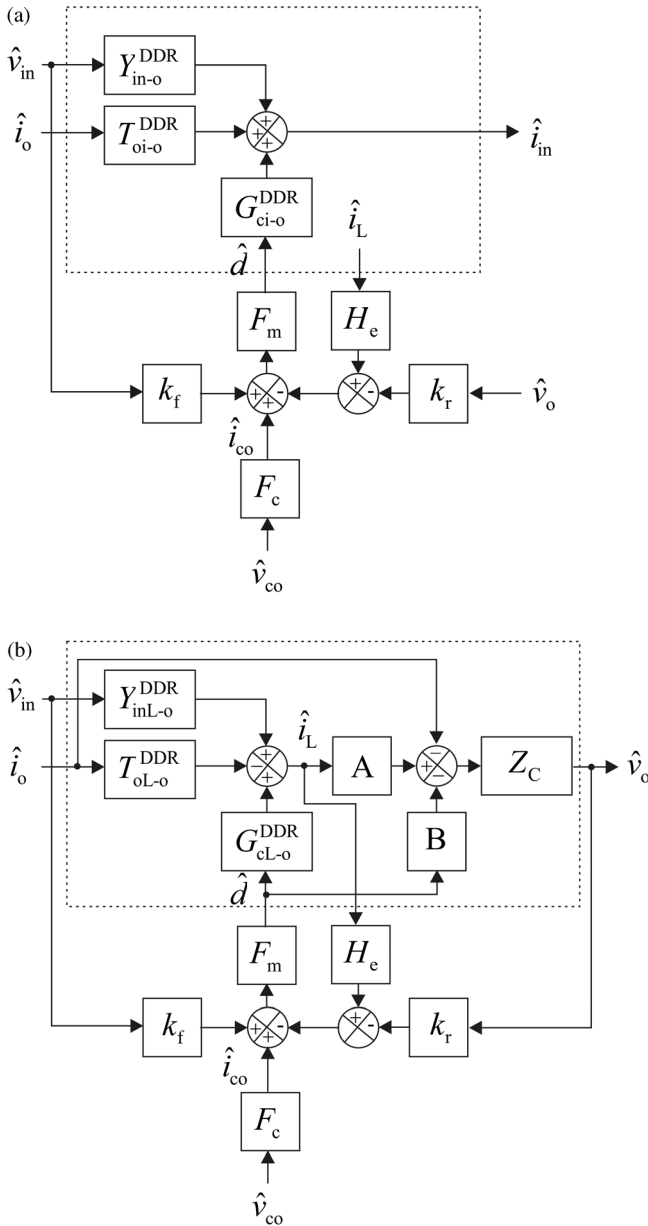


Figure 4.28 Control engineering block diagrams for solving Ridley's PCM transfer functions. (a) Input dynamics. (b) Output dynamics.

denote the open-loop transfer functions of the corresponding DDR-controlled converters given in Chapter 3. The parameters A and B are as follows: buck: $A = 1$ and $B = 0$, boost and buck–boost: $A = D'$ and $B = I_L$. Note that the resistive load effect is removed from all the parameters and transfer functions given further. All the items in Ridley's original material in Ref. [10] include the effect of load resistor

and the inductor current equivalent sensing resistor, which is also removed.

$$\begin{aligned}
 Y_{in-o} &= Y_{in-o}^{DDR} - \frac{F_m((-k_r + (H_e(s)/AZ_C))G_{io-o}^{DDR} - k_f)G_{ci-o}^{DDR}}{1 + L_c - L_v}, \\
 T_{oi-o} &= T_{oi-o}^{DDR} + \frac{F_m((-k_r + (H_e(s)/AZ_C))Z_{o-o}^{DDR} - (H_e(s)/A))G_{ci-o}^{DDR}}{1 + L_c - L_v}, \\
 G_{ci-o} &= \frac{F_m G_{ci-o}^{DDR}}{1 + L_c - L_v}, \\
 G_{io-o} &= \left[\left(1 + \frac{BF_m H_e(s)}{A} \right) G_{io-o}^{DDR} + F_m k_f G_{co-o}^{DDR} \right] / [1 + L_c - L_v], \\
 Z_{o-o} &= \left[\left(1 + \frac{BF_m H_e(s)}{A} \right) Z_{o-o}^{DDR} + \frac{F_m H_e(s)}{A} G_{co-o}^{DDR} \right] / [1 + L_c - L_v], \\
 G_{co-o} &= \frac{F_m G_{co-o}^{DDR}}{1 + L_c - L_v},
 \end{aligned} \tag{4.170}$$

where

$$\begin{aligned}
 L_c &= F_m H_e(s) G_{cl-o}^{DDR}, \\
 L_v &= F_m k_r G_{co-o}^{DDR}, \\
 H_e(s) &= 1 + s/Q_s \omega_s + s^2/\omega_s^2, \\
 G_{cl-o}^{DDR} &= \frac{V_e s C}{s^2 LC + s r_e C + 1}.
 \end{aligned} \tag{4.171}$$

M_1 and M_c denote the steady-state up slope of the inductor current and its compensation ramp.

The approximate transfer functions of a buck converter given by Ridley in Ref. [10] are as follows:

$$\begin{aligned}
 G_{co-o}^{Buck} &= \frac{L}{T_s(M_R D' - 0.5)} F_p(s) F_h(s), \\
 G_{io-o}^{Buck} &= \frac{D(M_R D' - 1 + (D/2))}{M_R D' - 0.5} F_p(s) F_h(s), \\
 Z_{o-o}^{Buck} &= \frac{F_p(s)}{M_R D' - 0.5},
 \end{aligned} \tag{4.172}$$

where

$$\begin{aligned}
 M_R &= 1 + \frac{M_c}{M_1}, \\
 F_p(s) &= \frac{1 + s r_c C}{1 + s/\omega_p}, \quad \omega_p = \frac{T_s(M_R D' - 0.5)}{LC}, \\
 F_h(s) &= 1 / \left[1 + \frac{s}{Q\omega_n} + \frac{s^2}{\omega_n^2} \right], \quad Q = \frac{1}{\pi(M_R D' - 0.5)}, \quad \omega_n = \frac{\pi}{T_s}.
 \end{aligned} \tag{4.173}$$

4.8.2 The Book PCM Model in CCM

It has turned out that the PCM models presented for the second-order converters in Section 4.2 can be improved to model accurately also the high frequency behavior of the transfer functions by adding an ideal high-frequency resonant series element in the inductor current feedback loop similarly as Ridley has done in Ref. [10]. The series resonant filter, however, differs from Ridley’s filter. The transfer function of the high-frequency series resonant element can be given by

$$H_{sr}(s) = 1 + \frac{s^2}{\omega_{sr}^2}, \tag{4.174}$$

$$\omega_{sr} = \frac{\pi}{T_s},$$

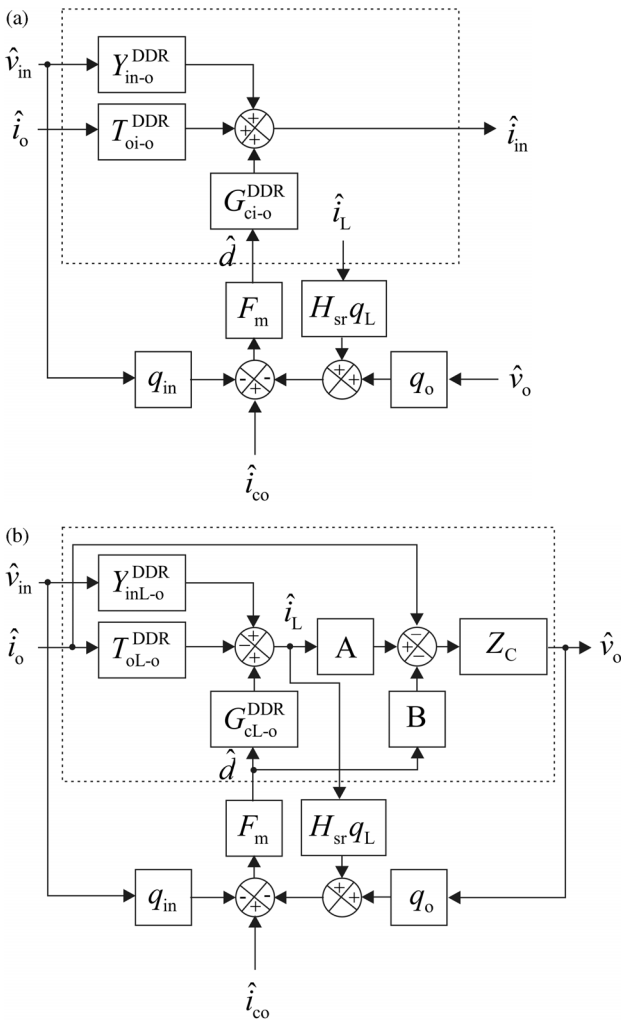


Figure 4.29 Control engineering block diagrams for solving the modified PCM transfer functions of the book. (a) Input dynamics. (b) Output dynamics.

and the corresponding general transfer functions for the basic converters can be given by (cf. Figure 4.29)

$$\begin{aligned}
 Y_{in-o} &= Y_{in-o}^{DDR} - \frac{F_m \left((q_o + (H_{sr}(s)q_L/AZ_C)) G_{io-o}^{DDR} + q_{in} \right) G_{ci-o}^{DDR}}{1 + L_c + L_v}, \\
 T_{oi-o} &= T_{oi-o}^{DDR} + \frac{F_m \left((q_o + (H_{sr}(s)q_L/AZ_C)) Z_{o-o}^{DDR} - (H_{sr}(s)q_L/A) \right) G_{ci-o}^{DDR}}{1 + L_c + L_v}, \\
 G_{ci-o} &= \frac{F_m G_{ci-o}^{DDR}}{1 + L_c + L_v}, \\
 G_{io-o} &= \left[\left(1 + \frac{BF_m H_{sr}(s)q_L}{A} \right) G_{io-o}^{DDR} - F_m q_{in} G_{co-o}^{DDR} \right] / [1 + L_c + L_v], \\
 Z_{o-o} &= \left[\left(1 + \frac{BF_m H_{sr}(s)q_L}{A} \right) Z_{o-o}^{DDR} + \frac{F_m H_{sr}(s)q_L}{A} G_{co-o}^{DDR} \right] / [1 + L_c + L_v], \\
 G_{co-o} &= \frac{F_m G_{co-o}^{DDR}}{1 + L_c + L_v},
 \end{aligned} \tag{4.175}$$

where

$$\begin{aligned}
 L_c &= F_m H_{sr}(s)q_L G_{cl-o}^{DDR}, \\
 L_v &= F_m q_o G_{co-o}^{DDR}.
 \end{aligned} \tag{4.176}$$

4.8.3 Evaluation of PCM-Controlled Buck in CCM

The used Simulink-based switching models are explicitly given in Chapter 6 and the buck converter is specified in Figure 4.20. The converter is loaded with a 4-Ω resistor. Figure 4.30 shows the switching model-based measured (dots and

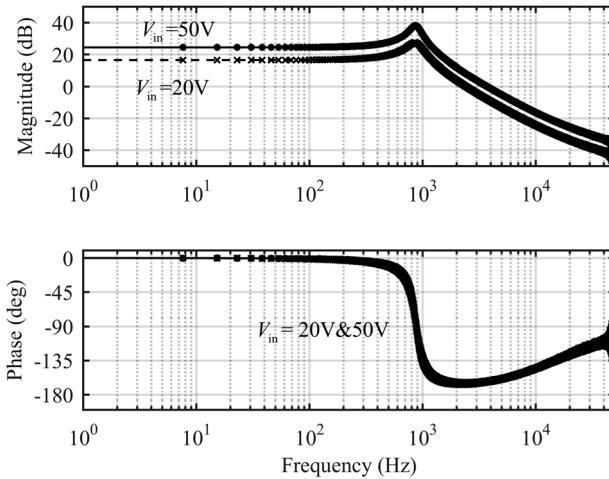


Figure 4.30 The control-to-output-voltage transfer functions of DDR-controlled buck converter measured at the input voltage of 20 and 50 V. The solid and dashed lines denote the predicted transfer functions, the dot and cross-marked lines the measured transfer functions.

crosses) and predicted (solid and dashed lines) control-to-output-voltage transfer functions of a DDR-controlled buck converter, where the power stage corresponds to Figure 4.20. The model-based predictions and the measured transfer functions have a perfect match. It should also be noted that the high-frequency phase does not have any extra deviations when approaching half the switching frequency (i.e., the maximum x -axis frequency in the figure), as discussed in Ref. [49]. This means that the basic SSA modeling method [50] will really yield perfect predictions for the converter internal dynamics.

Figure 4.31a shows the predicted and measured control-to-output-voltage transfer functions as resistive load-affected (G_{co-o}^{RL}) and as unterminated where the load effect is removed. The inductor-current loop is compensated by using the optimal compensation (i.e., $M_c = V_o/2L$). The load effect is clearly visible at the low frequencies, where the magnitude stays constant at 34.54 dB despite the changes in the input voltage. The dB value corresponds directly to R_L/R_s . The low-frequency magnitude of the internal transfer function increases only slightly when the input voltage drops to 20 V. This is the effect of the optimal compensation.

Figure 4.31b shows the high-frequency part of the transfer functions (i.e., from 8 to 50 kHz). The solid and dashed lines represent the predicted responses by the basic PCM model of the book. The excess phase shift at the high frequencies is also clearly visible. The basic PCM models of the book will accurately predict the phase behavior up to 1/10th of the switching frequency. Ridley's model also predicts accurately the high-frequency behavior.

Figure 4.31c shows the internal responses of Ridley's model (solid lines) and the modified model of the book (dashed lines) when the high-frequency resonant element is added according to Section 4.8.2. Both of the responses are virtually the same.

Figure 4.32 shows the measured and predicted inductor current loop gains, which are load resistance affected according to Eq. (4.177), where G_{cl-o}^{DDR} , G_{co-o}^{DDR} , Z_{o-o}^{DDR} , and T_{ol-o}^{DDR} denote the open-loop control-to-inductor-current transfer function, control-to-output-voltage transfer function, output impedance, and output current-to-inductor-current transfer function of the DDR-controlled buck converter, respectively, as given in Eq. (4.178). The low-frequency part of the loop gain equals $F_m q_L V_e/R_L$ in Figure 4.32, which is exactly predicted by the model of this book. The high-frequency extension is not added in the prediction. The high-frequency phase behavior of the measured inductor current loop implies the existence of series resonant RHP circuit in the loop, as discussed by Ridley, but it does not work with the model of the book as discussed earlier. Dr. Ridley gives also the measured frequency response in Ref. [10], but according to his comments the low-frequency part does not match with the predictions. He has not actually taken into account that the feedback from output voltage (i.e., k_r) affects also the inductor-current-loop gain (cf. Eq. (4.170)), which would correct the predictions.

$$L_{ind-cur}^{Z_L} = F_m q_L \left(G_{cl-o}^{DDR} + \frac{T_{ol-o}^{DDR}}{Z_L} \cdot \frac{G_{co-o}^{DDR}}{1 + (Z_{o-o}^{DDR}/Z_L)} \right). \quad (4.177)$$

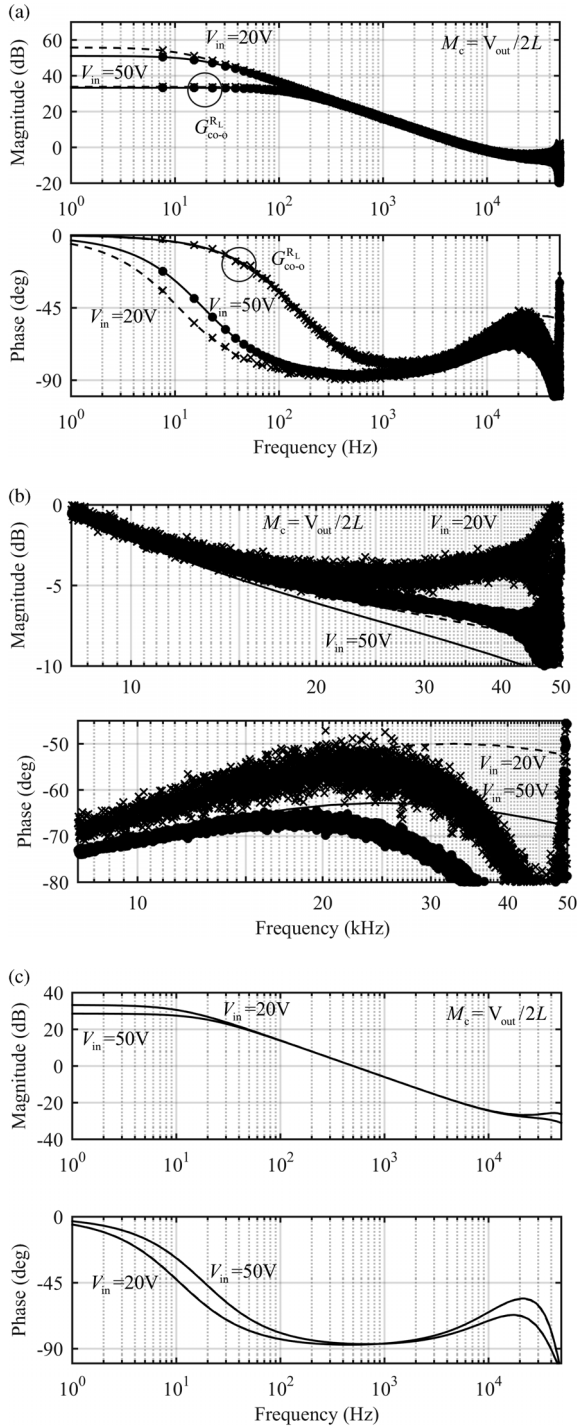


Figure 4.31 The control-to-output-voltage transfer functions. (a) The measured and predicted load affected as well as load effect removed. (b) The high-frequency part of the transfer functions (i.e., 8–50 kHz). (c) The comparison of Ridley's model (solid lines) versus the modified book model (dashed lines).

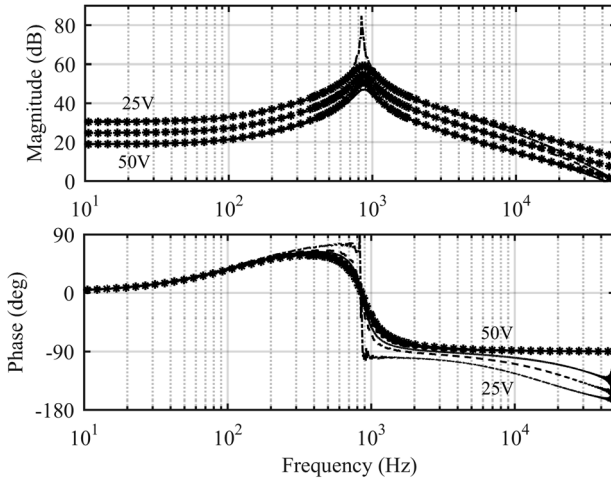


Figure 4.32 The measured and predicted load-affected ($R_L = 4 \Omega$) inductor current loop gain at the input voltage of 50, 30, and 25 V. The predictions are marked with an asterisk.

$$\begin{aligned}
 G_{cL-o}^{DDR} &= \frac{V_e s C}{s^2 LC + sr_e C + 1}, \\
 G_{co-o}^{DDR} &= \frac{V_e(1 + sr_e C)}{s^2 LC + sr_e C + 1}, \\
 Z_{o-o}^{DDR} &= \frac{(r_e - r_c + sL)(1 + sr_e C)}{s^2 LC + sr_e C + 1}, \\
 T_{oL-o}^{DDR} &= \frac{1 + sr_e C}{s^2 LC + sr_e C + 1}.
 \end{aligned} \tag{4.178}$$

Figure 4.33 shows the same set of output impedances as in Figure 4.31a. The effect of load on the transfer functions ($Z_{o-o}^{R_L}$) is obvious (i.e., the low-frequency

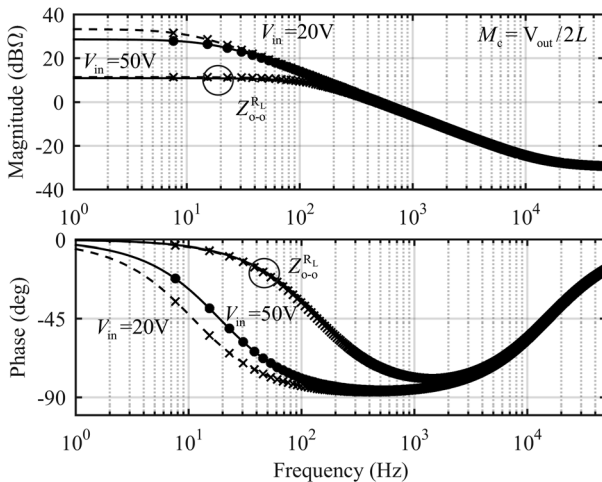


Figure 4.33 The set of output impedances as in Figure 4.31a.

magnitude is 12 dB). In practice, the internal output impedances can be measured directly. The high-frequency phase does not exhibit any extra phase shift. As a consequence of this, the basic PCM model of the book gives exact prediction as well. Ridley’s model as well as the modified book model will give exactly the same responses. It is sometimes argued that Ridley has left the high-frequency extension (F_h) out of the model to make the model more accurate, but it is not actually true.

Figure 4.34a shows all the input-to-output transfer functions (G_{i-o}) similarly as in Figure 4.31a. The resistive load clearly increases the attenuation due

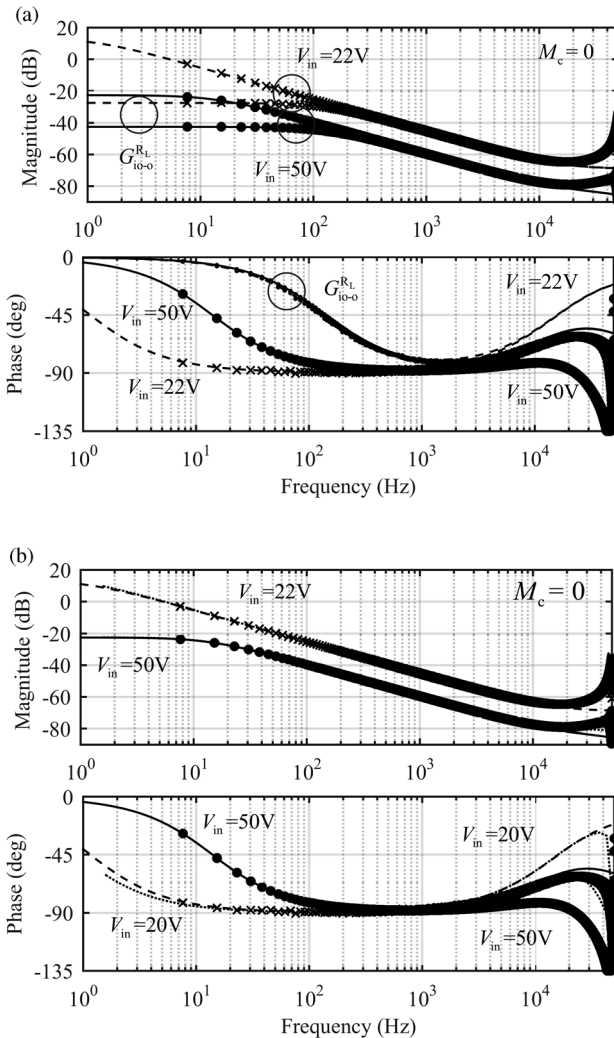


Figure 4.34 The set of input-to-output transfer functions similarly as in Figure 4.31a. (a) All the transfer functions. (b) The internal transfer functions (Ridley: dotted line, Book basic model: solid and dashed lines). The inductor current loop compensation is set to zero.

to the voltage divider action. The high-frequency attenuation of the magnitude is so high that even Matlab-based frequency response analysis is subject of resolution problems, which causes the high-frequency phase to have more phase shift than it has in reality. Figure 4.34b shows the comparison of Ridley's model responses (dotted lines) and the basic model of the book. The modified model of the book gives exactly the same responses as Ridley's responses are. They can be considered to show the correct high-frequency phase behavior as well.

4.8.4 Evaluation of PCM-Controlled Boost in CCM

The power stage of the boost converter, which is used in the evaluation, is given in Figure 4.35 with the defined operating points and components. The actual load of the converter is a $50\ \Omega$ resistor when it is operated at open loop under PCM control. The control-to-output-voltage transfer function (G_{co-o}) and output impedance (Z_{o-o}) are measured from the corresponding Simulink model and predicted by using Ridley's models as well as the book model with the high-frequency extension H_{sr} defined in Eq. (4.174). As discussed earlier, the internal output impedance can be measured as such but all the other transfer functions are load affected and, therefore, the corresponding unterminated transfer functions have to be solved computationally. In this case, we do not give the load-affected transfer functions. The inductor-current loop is compensated by using $M_c = V_o/2L$, which will guarantee the operation of the converter without the second-harmonic mode in all conditions.

The measured (diamonds (20 V) and squares (50 V)) and predicted (solid and dashed lines) frequency responses of the control-to-output-voltage transfer functions are given in Figure 4.36. The excess high-frequency phase shift, which is typical to the PCM control, is clearly visible. Both of the PCM models will describe perfectly the control-related dynamics.

The measured (diamonds (20 V) and squares (50 V)) and predicted (solid and dashed lines) frequency responses of the output impedances are given in Figure 4.37. The excess high-frequency phase shift does not affect the output impedance. Both of the models predict perfectly the behavior of the output impedance as well.

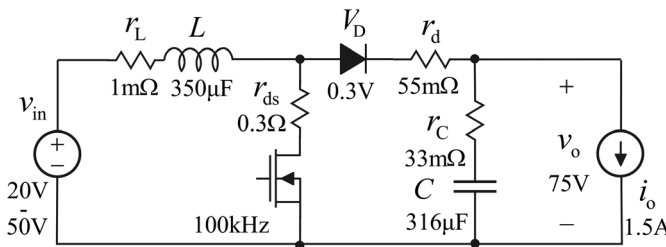


Figure 4.35 Boost converter with operating point and component definitions.

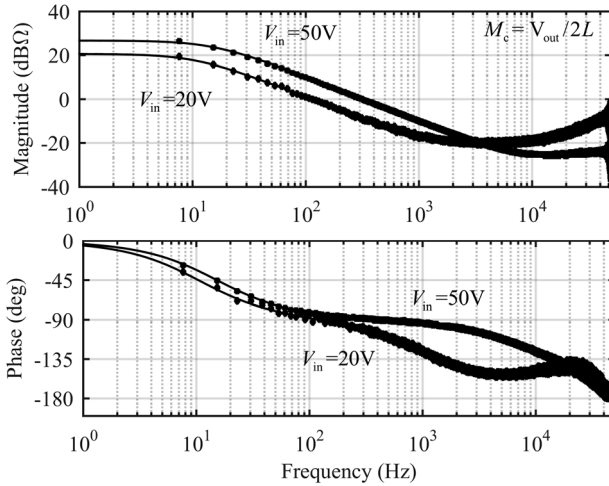


Figure 4.36 The set of frequency responses of the control-to-output-voltage transfer functions at the input voltage of 20 and 50 V.

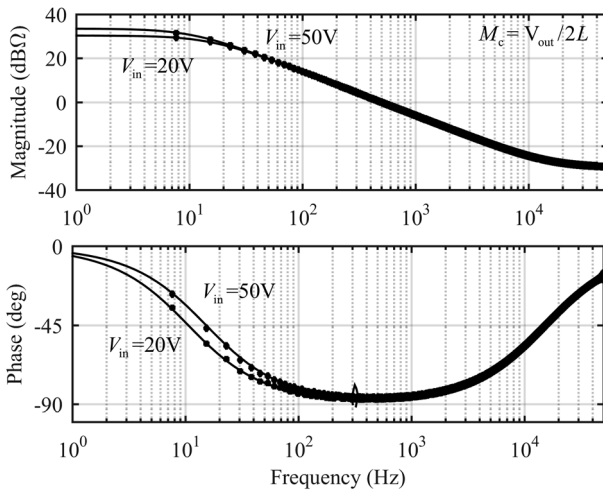


Figure 4.37 The set of frequency responses of the output impedances at the input voltage of 20 and 50 V.

4.8.5 Concluding Remarks

The accurate modeling of PCM control has been subject of intensive research and debate for years. Multitude of models have been developed, of which most are based on the assumption of sampling effect causing the peculiar phenomena observed in the dynamic behavior of the PCM-controlled converters. This theme is also evident in Dr. Ridley's modeling, which can be easily noticed when reading his Ph.D. dissertation [51] and different publications. His dissertation, however,

reveals that the modeling is not based on sampling effect by no means but it follows quite much the same procedures as introduced in this book. By computing the real low-frequency duty-ratio gain in Dr. Ridley's buck converter models (cf. Eq. (4.179)) by means of G_{co-o} in Eq. (4.170), it is exactly the same as the duty-ratio gain of this book. Dr. Ridley's modeling approach is more intuitive, including also assumptions which are not actually true, compared to the modeling method of this book. This is now quite obvious, when the high-frequency extension was also added to the models of the book yielding perfect accuracy in predictions and coinciding perfectly with measurements. The modeling method of this book is consistent, because all the steps taken are explicitly justified. It is also very easy to apply to different converter topologies as demonstrated in this book.

$$F_{m-DC}^{\text{Ridley}} = 1 / \left[T_s \left(M_c + \frac{(D' - D)V_{in}}{2L} \right) \right]. \quad (4.179)$$

References

- 1 Deisch, C.W. (1978) Simple switching control method changes power converter into a current source. Proceeding of the IEEE PESC, pp. 300–306.
- 2 Dixon, L.H. (1990) Average current mode control of switching power supplies. Proceeding of the Power Supply Design Seminar SEM 700, Unitrode Corporation, pp. 5.1–5.14.
- 3 Lempinen, J. and Suntio, T. (2001) Small-signal modeling for design of robust variable-frequency flyback battery chargers for portable device applications. Proceeding of the IEEE IECON, pp. 548–554.
- 4 Redl, R. and Sokal, N.O. (1985) Current-mode control, five different types, used with the three basic classes of power converters: small-signal AC and large-signal DC characterization, stability requirements, and implementation of practical circuits. Proceeding of the IEEE PESC, pp. 771–785.
- 5 Redl, R. and Sokal, N.O. (1985) What a design engineer should know about current-mode control. Proceeding of the Power Electronics Design Conference, pp. 18–33.
- 6 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters – Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.
- 7 Suntio, T. (2006) Unified average and small-signal modeling of direct-on-time control. *IEEE Trans. Ind. Electron.*, **53** (1), 287–295.
- 8 Suntio, T., Karppanen, M., and Sippola, M. (2008) Methods to characterize open-loop dynamics of current-mode-controlled converters. Proceeding of the IEEE PESC, pp. 636–642.
- 9 Hsu, S.-P., Brown, A., Rensink, L., and Middlebrook, R.D. (1979) Modelling and analysis of switching DC-to-DC converters in constant-frequency current-programmed mode. Proceeding of the IEEE PESC, pp. 284–301.
- 10 Ridley, R.B. (1991) A new, continuous-time model for current-mode control. *IEEE Trans. Power Electron.*, **6** (2), 271–280.
- 11 Schultz, C.P. (1993) A unified model of constant frequency switching regulators using multiloop feedback control. Proceeding of the Power Conversion Conference, pp. 319–329.

- 12 Tan, F.D. and Middlebrook, R.D. (1995) A unified model for current-programmed converters. *IEEE Trans. Power Electron.*, **10** (4), 397–408.
- 13 Sun, J. and Bass, R.M. (1997) A new approach to average modeling of PWM converters with current-mode control. Proceeding of the IEEE IECON, pp. 599–604.
- 14 Suntio, T., Hankaniemi, M., and Roinila, T. (2007) Dynamical modelling of peak-current-mode-controlled converter in continuous conduction mode. *J. Simul. Model. Pract. Theory*, **15** (10), 1320–1337.
- 15 Karppanen, M., Arminen, J., Suntio, T., Savela, K., and Simola, J. (2008) Dynamical modeling and characterization of peak-current-mode-controlled superbuck converter. *IEEE Trans. Power Electron.*, **23** (3), 1370–1380.
- 16 Sarmaljärvi, T., Lakhdari, F., Karppanen, M., and Suntio, T. (2008) Modelling and dynamic characterisation of peak-current-mode-controlled superboost converter. *IET Power Electr.*, **1** (4), 527–536.
- 17 Suntio, T. (2001) Analysis and modeling of peak-current-mode controlled buck converter in DICM. *IEEE Trans. Ind. Electron.*, **48** (1), 127–135.
- 18 Redl, R. and Sokal, N.O. (1987) How to use current-mode control with capacitively coupled half-bridge converters. Proceeding of the IEEE APEC, pp. 257–265.
- 19 Andreyckak, W. (1985) Practical considerations in current mode power supplies. Proceeding of the Unitrode Power Supply Design Seminar SEM 500, Unitrode Corporation, pp. 1.1–1.17.
- 20 Erickson, R.W. and Maksimović, D. (2001) *Fundamentals of Power Electronics*, Kluwer Academic Publishers, Norwell, MA.
- 21 Papatomas, T.V. and Giapocelli, J.N. (1979) Digital implementation and simulation of an average current controlled switching regulator. Proceeding of the IEEE PESC, pp. 155–161.
- 22 Papatomas, T.V. (1983) Average current controlled switching regulator – stability and feedforward analysis and simulation. Proceeding of the IEEE PESC, pp. 61–69.
- 23 Redl, R. (1994) Power-factor correction in single-phase switching power supplies – an overview. *Int. J. Electron.*, **77** (5), 555–582.
- 24 Urtasun, A., Sanchis, P., and Marroyo, L. (2013) Adaptive control of the DC/DC boost stage in PV converters with small input capacitor. *IEEE Trans. Power Electron.*, **28** (11), 5038–5048.
- 25 Sun, J. and Bass, R.M. (1999) Modeling and practical design issues for average current control. Proceeding of the IEEE APEC, pp. 980–986.
- 26 Suntio, T., Lempinen, J., Gadoura, I., and Zenger, K. (2001) Dynamic effects of inductor current ripple in average current mode control. Proceeding of the IEEE PESC, pp. 1259–1264.
- 27 Suntio, T., Rahkala, M., Gadoura, I., and Zenger, K. (2001) Dynamic effects of inductor ripple in peak-current and average-current-mode control. Proceeding of the IEEE IECON, pp. 1072–1077.
- 28 Cook, P. (2000) Modeling average current mode control. Proceeding of the IEEE APEC, pp. 256–262.
- 29 Ridley, R.B. (1990) A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM. Proceeding of the IEEE PESC, pp. 382–389.

- 30 Redl, R. and Sun, J. (2009) Ripple-based control of switching regulators – an overview. *IEEE Trans. Power Electron.*, **24** (12), 2669–2680.
- 31 Spiazzi, G., Tagliavia, D., and Spampinato, S. (2000) DC–DC flyback converters in critical conduction mode: a reexamination. Proceeding of the IEEE IECON, pp. 2426–2432.
- 32 Irving, B. and Jovanovic, M. (2002) Analysis and design of self-oscillating flyback converter. Proceeding of the IEEE APEC, pp. 897–903.
- 33 Chen, J., Erickson, R., and Maksimovic, D. (2001) Averaged switch-modeling of boundary conduction mode DC-to-DC converters. Proceeding of the IEEE IECON, pp. 844–849.
- 34 Lempinen, J. and Suntio, T. (2001) Modeling and analysis of a self-oscillating peak-current controlled flyback converter. Proceeding of the IEEE IECON, pp. 960–965.
- 35 Irving, B., Panov, Y., and Jovanovic, M. (2003) Small-signal model of variable-frequency flyback converter. Proceeding of the IEEE APEC, pp. 997–982.
- 36 Suntio, T. (2006) Average and small-signal modelling of self-oscillating flyback converter with applied switching delay. *IEEE Trans. Power Electron.*, **21** (2), 479–486.
- 37 Redl, R. (1991) Small-signal high-frequency analysis of the free-running current-mode-controlled converter. Proceeding of the IEEE PESC, pp. 898–906.
- 38 Liu, Y.-F. and Sen, P.C. (1996) Large-signal modeling of hysteretic current-programmed converters. *IEEE Trans. Power Electron.*, **11** (3), 423–430.
- 39 Park, J.H. and Cho, B.H. (2006) Small-signal modeling of hysteretic current mode control using the PWM switch model. Proceeding of the IEEE COMPEL, pp. 225–230.
- 40 Sun, J. (2002) Small-signal modeling of variable-frequency pulsewidth modulators. *IEEE Trans. Aerosp. Electron. Syst.*, **38** (3), 1104–1108.
- 41 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Effect of control method on impedance-based interactions in a buck converter. *IEEE Trans. Power Electron.*, **28** (11), 5311–5322.
- 42 Vargas, L. and Losic, N. (1992) Synthesis of zero-impedance converter. *IEEE Trans. Power Electron.*, **7** (1), 152–170.
- 43 Redl, R. and Sokal, N.O. (1989) Near-optimum dynamic regulation of DC–DC converters using feed-forward of output current and input voltage with current-mode control. *IEEE Trans. Power Electron.*, **PE-1** (3), 181–191.
- 44 Karppanen, M., Hankaniemi, M., Suntio, T., and Sippola, M. (2007) Dynamical characterization of peak-current-mode-controlled buck converter with output-current feedforward. *IEEE Trans. Power Electron.*, **22** (2), 444–451.
- 45 Smithson, S.C. and Williamson, S.S. (2015) A unified state-space model of constant-frequency current-mode-controlled power converters in continuous conduction mode. *IEEE Trans. Ind. Electron.*, **62** (7), 4514–4524.
- 46 Herbst, G. (2016) Comment on A unified state-space model of constant-frequency current-mode-controlled power converters in continuous conduction mode. *IEEE Trans. Ind. Electron.*, **63** (5), 3198–3200.
- 47 Roinila, T., Helen, T., Vilkkko, M., and Suntio, T. (2009) Circular correlation based identification of switching power converter with uncertainty analysis using fuzzy density approach. *J. Simul. Model. Pract. Theory*, **17** (6), 1043–1058.

- 48 Roinila, T., Vilkkö, M., and Suntio, T. (2009) Fast loop gain measurement of switched-mode converter using binary signal with specified amplitude spectrum. *IEEE Trans. Power Electron.*, **24** (12), 2746–2755.
- 49 Mitchell, D.M. (1980) Pulsewidth modulator phase shift. *IEEE Trans. Aerosp. Electron. Syst.*, **AES-16** (3), 272–278.
- 50 Middlebrook, R.D. and Ćuk, S. (1977) A general unified approach to modeling switching-converter power stages. *Int. J. Electron.*, **42** (6), 521–550.
- 51 Ridley, R.B. (1991) A new small-signal model to current-mode control. PhD dissertation, Virginia Polytechnic Institute and State University.

5

Dynamic Modeling of Current-Output Converters

5.1 Introduction

The use of energy storage either to ensure uninterrupted operation (cf. Figure 5.1) [1] as a primary energy source [2] or assisting the operation of the system [3–6] is growing rapidly due to the increasing use of different battery-powered devices as well as due to increased utilization of renewable energy sources incorporating intermittent nature in energy production. In such applications, the power electronic converters have to be able to operate in two different operational modes, as shown in Figure 5.1b: When the storage battery is fully charged, the power electronic converter will maintain the charge operating at constant voltage-output mode (cf. Figures 5.1b and 5.2a). After the discharging of the storage battery, its recharging will take place at current-limiting mode for protecting the converter from damage due to the short circuit nature of storage battery (i.e., extremely low internal impedance). As a consequence, the dynamics of the converter would vary between the voltage and current-output modes, which are profoundly different from each other and require different control design considerations [7,8]. The typical problem involved in the change of feedback arrangement is the profound change of control bandwidth, which easily leads to instability either due to the source impedance interactions as reported in Ref. [9] or due to extending the current-loop crossover frequency beyond the switching frequency [10–12].

A voltage-fed DDR-controlled converter (cf. Chapter 3) is a voltage-output converter at open loop. Therefore, the current-output transfer functions representing the dynamics of the converter cannot be measured by using a constant voltage sink as a load as the theory requires because of violation of Kirchhoff's laws. Therefore, a resistor is to be used as a load, but as a consequence, the transfer functions are load affected and the effect of the load resistor has to be removed computationally by applying proper load-interaction formulation.

A CM-controlled converter (cf. Chapter 4) is a current-output converter at open loop, which can be easily characterized by connecting a constant voltage sink at its output terminals. The dynamics of a CM-controlled converter cannot be measured at open loop by using a constant current sink as a load because of violating Kirchhoff's laws [13]. Therefore, the measurements have to be carried

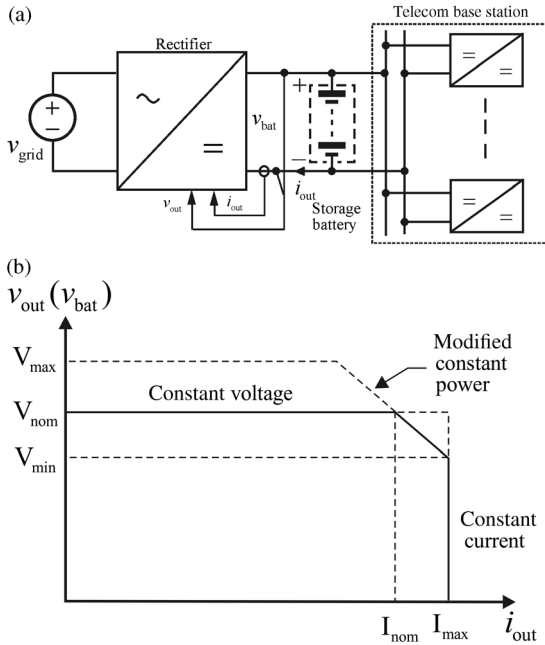


Figure 5.1 Typical DC UPS (a) system structure and (b) the required output terminal behavior.

out by using a resistor as a load, and the load effect has to be removed computationally by applying proper load-interaction formulation.

The dynamic models of the current-output converter can also be developed directly from the known corresponding voltage-output mode transfer functions by interchanging the input and output variables at the output terminal (i.e., $v_o \leftrightarrow i_o$) [10–12].

The dynamic modeling and impedance-based interaction analysis of a voltage-fed current-output converter will be introduced in detail in the subsequent sections. A DDR- and PCM-controlled buck converter is used as an example for demonstrating the dynamical changes the output mode will induce.

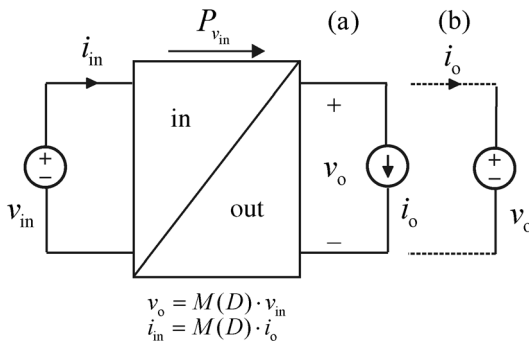


Figure 5.2 VF converter at (a) VO and (b) CO mode.

5.2 Dynamic Modeling

The dynamic modeling of the voltage-fed current-output converter can be performed by using the same methods as introduced for the DDR-controlled converters in Chapter 3 and for the CM-controlled converters in Chapter 4. The only difference is that the voltage at the output terminal has to be considered as an input variable, and the current as an output variable, respectively, as illustrated in Figure 5.3. The set of transfer functions describing the dynamics of voltage-fed current-output converter is known as Y parameters [8], and given in Eq. (5.1), where \hat{c} denotes the general control variable. The set of special transfer functions can be given based on Eq. (5.1) and their generalized definition in Sections 2.2.3 and 2.2.5 according to Eq. (5.2). The methods for modeling the dynamics of voltage-output converters are well described in Chapters 3 and 4. Therefore, in this chapter we introduce the modeling method applying the known dynamic models of the voltage-output converters. This technique has to be utilized anyway when the converter is subjected to the change of output mode.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y_{in}^Y & T_{oi}^Y & G_{ci}^Y \\ G_{io}^Y & -Y_o^Y & G_{co}^Y \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_o \\ \hat{c} \end{bmatrix}. \tag{5.1}$$

$$\begin{bmatrix} Y_{in-oco}^Y & Y_{in-\infty}^Y & T_{oi-\infty}^Y \\ Y_{o-oci}^{Y-x} & Y_{o-\infty}^Y & G_{io-\infty}^Y \end{bmatrix} = \begin{bmatrix} Y_{in-o}^Y + \frac{G_{io-o}^Y T_{oi-o}^Y}{Y_{o-o}^Y} & Y_{in-o}^Y - \frac{G_{io-o}^Y G_{ci-o}^Y}{G_{co-o}^Y} & T_{oi-o}^Y + \frac{Y_{o-o}^Y G_{ci-o}^Y}{G_{co-o}^Y} \\ Y_{o-x}^Y + \frac{G_{io-x}^Y T_{oi-x}^Y}{Y_{in-x}^Y} & Y_{o-o}^Y + \frac{T_{oi-o}^Y G_{co-o}^Y}{G_{ci-o}^Y} & G_{io-o}^Y - \frac{Y_{in-o}^Y G_{co-o}^Y}{G_{ci-o}^Y} \end{bmatrix}, \tag{5.2}$$

where the open-circuit output admittance can also be given by

$$Y_{o-oci}^{Y-x} = \frac{Y_{o-x}^Y}{Y_{in-x}^Y} Y_{in-oco}^Y. \tag{5.3}$$

The superscript and subscript extension x in Eq. (5.3) denotes that the open-circuit output admittance is dependent on the state of output-side feedback.

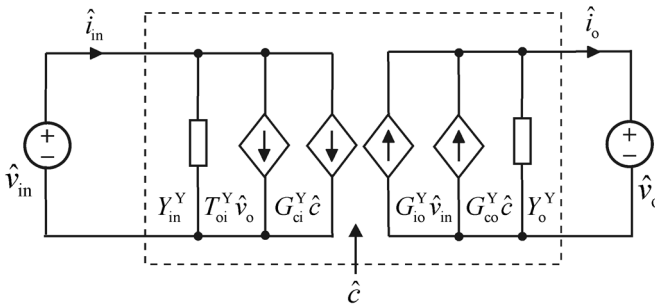


Figure 5.3 A linear circuit representing the internal dynamics of the voltage-fed current-output converter.

As already discussed, the difference between the voltage and current-output modes is that the output terminal voltage and current denote different input and output variables depending on the mode of output. The method to obtain the dynamic models of the current-output converter from the dynamic models of the voltage-output converter is to changing the output and input variables at the output terminal as follows (Note: the superscript G denotes the transfer functions of the voltage-fed voltage-output converter and the superscript Y the transfer functions of the voltage-fed current-output converter):

$$\begin{cases} \hat{i}_{in} = Y_{in}^G \hat{v}_{in} + T_{oi}^G \hat{i}_o + G_{ci}^G \hat{c}, \\ \hat{v}_o = G_{io}^G \hat{v}_{in} - Z_o^G \hat{i}_o + G_{co}^G \hat{c}. \end{cases} \quad (5.4)$$

$$\begin{cases} \hat{i}_{in} = \left(Y_{in}^G + \frac{G_{io}^G T_{oi}^G}{Z_o^G} \right) \hat{v}_{in} - \frac{T_{oi}^G}{Z_o^G} \hat{v}_o + \left(G_{ci}^G + \frac{T_{oi}^G G_{co}^G}{Z_o^G} \right) \hat{c}, \\ \hat{i}_o = \frac{G_{io}^G}{Z_o^G} \hat{v}_{in} - \frac{1}{Z_o^G} \hat{v}_o + \frac{G_{co}^G}{Z_o^G} \hat{c}. \end{cases} \quad (5.5)$$

Based on Eq. (5.5), we may state that

$$\begin{bmatrix} Y_{in}^Y & T_{oi}^Y & G_{ci}^Y \\ G_{io}^Y & Y_o^Y & G_{co}^Y \end{bmatrix} = \begin{bmatrix} Y_{in}^G + \frac{G_{io}^G T_{oi}^G}{Z_o^G} & -\frac{T_{oi}^G}{Z_o^G} & G_{ci}^G + \frac{T_{oi}^G G_{co}^G}{Z_o^G} \\ \frac{G_{io}^G}{Z_o^G} & \frac{1}{Z_o^G} & \frac{G_{co}^G}{Z_o^G} \end{bmatrix}, \quad (5.6)$$

or

$$\begin{bmatrix} Y_{in}^Y & T_{oi}^Y & G_{ci}^Y \\ G_{io}^Y & Y_o^Y & G_{co}^Y \end{bmatrix} = \begin{bmatrix} Y_{in-sco}^G & -\frac{T_{oi}^G}{Z_o^G} & \frac{G_{co}^G}{Z_o^G} T_{oi-\infty}^G \\ \frac{G_{io}^G}{Z_o^G} & \frac{1}{Z_o^G} & \frac{G_{co}^G}{Z_o^G} \end{bmatrix}. \quad (5.7)$$

It may be understandable, when looking at Eq. (5.6), that the dynamics of the current-output converter would be profoundly different compared to the dynamics of the corresponding voltage-output converter. The only transfer function, which is the same, is the output impedances (Z_o^G).

The special transfer functions in Eq. (5.2) can also be given by means of the transfer functions of the voltage-fed voltage-output converter as follows:

$$\begin{bmatrix} Y_{in-oco}^Y & Y_{in-\infty}^Y & T_{oi-\infty}^Y \\ Y_{o-oci}^{Y-x} & Y_{o-\infty}^Y & G_{io-\infty}^Y \end{bmatrix} = \begin{bmatrix} Y_{in-o}^G & Y_{in-\infty}^G & \frac{G_{ci-o}^G}{G_{co-o}^G} \\ \frac{Y_{in-x}^G}{Z_{o-x}^G Y_{in-sco}^G} & \frac{G_{ci-o}^G}{G_{co-o}^G T_{oi-\infty}^G} & -\frac{Y_{in-\infty}^G}{T_{oi-\infty}^G} \end{bmatrix}. \quad (5.8)$$

Equation (5.8) indicates that the ideal admittance ($Y_{in-\infty}$) and the open-circuit output admittance ($Y_{o-oci} = 1/Z_{o-oci}$) will stay intact. It is also quite obvious that the open-circuit input admittance (Y_{in-oco}) equals the open-loop input

admittance (Y_{in-o}^G) of the voltage-output converter (i.e., the internal impedance of the constant current sink is infinite).

When applying the information given in Eq. (5.6) and the dynamic models derived for the DRR-controlled buck converter in Section 3.4.1, the set of current-output transfer functions for a buck converter can be given by

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} D^2 & -D & DV_e + I_o(sL + r_e - r_C) \\ D & -s^2LC + sr_eC + 1/(1 + sr_C C) & V_e \end{bmatrix} / (sL + r_e - r_C) \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_o \\ \hat{d} \end{bmatrix}, \quad (5.9)$$

where V_e and r_e are explicitly defined in Section 3.4.1.

When applying the information given in Eq. (5.4) and the dynamic models derived for the PCM-controlled buck converter in Section 4.2.8, the set of current-output transfer functions for a buck converter can be given for the input dynamics by

$$\begin{aligned} Y_{in-o} &= \frac{(D - F_m V_e q_{in})(D - F_m I_o q_L)}{\Delta} - F_m q_{in} I_o, \\ \Delta T_{oi-o} &= -(D - F_m I_L q_L), \\ \Delta G_{ci-o} &= DF_m V_e + F_m I_o (sL + r_e - r_C), \end{aligned} \quad (5.10)$$

and for the output dynamics by

$$\begin{aligned} \Delta G_{io-o} &= D - F_m V_e q_{in}, \\ \Delta Z_{o-o} &= \frac{s^2LC + s(r_e + F_m V_e q_L)C + 1}{1 + sr_C C}, \\ \Delta G_{co-o} &= F_m V_e, \end{aligned} \quad (5.11)$$

where the denominator (Δ) is defined by

$$\Delta = sL + F_m V_e q_L + r_e - r_C. \quad (5.12)$$

5.3 Source and Load Interactions

The effect of nonideal source and load on the voltage-fed current-output converter can be solved by means of the linear circuit in Figure 5.4 by computing the input voltage (v_{in}) and output voltage (v_o) and substituting them into the unterminated equations given in Eq. (5.1). The detailed derivations are presented in the subsequent sections.

5.3.1 Source Interactions

We assume that the output load is ideal when computing the required equations for the source interactions. According to the already described process, the input voltage present at the direct input terminal would be

$$\hat{v}_{in} = \hat{v}_{inS} - Z_S \hat{i}_{in}. \quad (5.13)$$

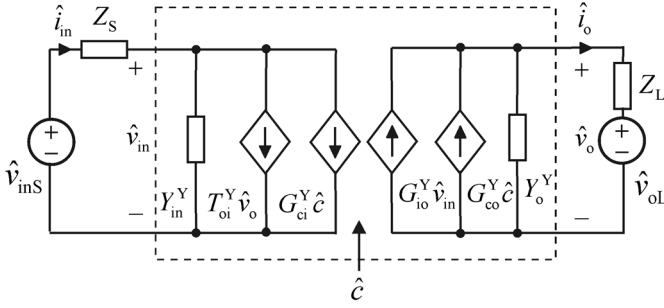


Figure 5.4 A linear circuit representing the internal dynamics of the voltage-fed current-output converter terminated with a nonideal source and load.

When the input voltage (\hat{v}_{in}) defined in Eq. (5.13) is substituted into the unterminated dynamic representation in Eq. (5.14), the source-affected representation will yield as given in Eq. (5.15).

$$\begin{cases} \hat{i}_{in} = Y_{in}^Y \hat{v}_{in} + T_{oi}^Y \hat{v}_o + G_{ci}^Y \hat{c}, \\ \hat{i}_o = G_{io}^Y \hat{v}_{in} - Y_o^Y \hat{v}_o + G_{co}^Y \hat{c}. \end{cases} \quad (5.14)$$

$$\begin{cases} \hat{i}_{in} = \frac{Y_{in}^Y}{1 + Z_S Y_{in}^Y} \hat{v}_{inS} + \frac{T_{oi}^Y}{1 + Z_S Y_{in}^Y} \hat{v}_o + \frac{G_{ci}^Y}{1 + Z_S Y_{in}^Y} \hat{c}, \\ \hat{i}_o = \frac{G_{io}^Y}{1 + Z_S Y_{in}^Y} \hat{v}_{inS} - \frac{1 + Z_S (Y_{in}^Y + (G_{io}^Y T_{oi}^Y / Y_o^Y))}{1 + Z_S Y_{in}^Y} Y_o^Y \hat{v}_o + \frac{1 + Z_S (Y_{in}^Y - (G_{io}^Y G_{ci}^Y / G_{co}^Y))}{1 + Z_S Y_{in}^Y} G_{co}^Y \hat{c}, \end{cases} \quad (5.15)$$

which can be also given according to Eq. (5.2) by

$$\begin{cases} \hat{i}_{in} = \frac{Y_{in}^Y}{1 + Z_S Y_{in}^Y} \hat{v}_{inS} + \frac{T_{oi}^Y}{1 + Z_S Y_{in}^Y} \hat{v}_o + \frac{G_{ci}^Y}{1 + Z_S Y_{in}^Y} \hat{c}, \\ \hat{i}_o = \frac{G_{io}^Y}{1 + Z_S Y_{in}^Y} \hat{v}_{inS} - \frac{1 + Z_S Y_{in-oco}^Y}{1 + Z_S Y_{in}^Y} Y_o^Y \cdot \hat{v}_o + \frac{1 + Z_S Y_{in-\infty}^Y}{1 + Z_S Y_{in}^Y} G_{co}^Y \cdot \hat{c}. \end{cases} \quad (5.16)$$

As stated in Eq. (5.8), Y_{in-oco}^Y equals the open-circuit input admittance of the corresponding voltage-output converter, which is known to have resonant behavior in the DDR-controlled converter. Therefore, the converter output admittance may be more sensitive to the source-impedance interactions than the output impedance of the corresponding voltage-output converter. For the CM-controlled converters, the source sensitivity does not change when the output mode is changed.

5.3.2 Load Interactions

We assume that the input source is ideal when computing the required equations for the load interactions. According to the already described process, the output

voltage present at the direct input terminal would be

$$\hat{v}_o = \frac{Z_L G_{io}^Y}{1 + Z_L Y_o^Y} \hat{v}_{in} + \frac{1}{1 + Z_L Y_o^Y} \hat{v}_{oL} + \frac{Z_L G_{co}^Y}{1 + Z_L Y_o^Y} \hat{c}. \quad (5.17)$$

When the output voltage (\hat{v}_o) defined in Eq. (5.17) is substituted into the unterminated dynamic representation in Eq. (5.14), the load-affected representation will yield as given in Eq. (5.18).

$$\begin{cases} \hat{i}_{in} = \frac{1 + Z_L (Y_o^Y + (G_{io}^Y T_{oi}^Y / Y_o^Y))}{1 + Z_L Y_o^Y} Y_{in}^Y \hat{v}_{in} + \frac{T_{oi}^Y}{1 + Z_L Y_o^Y} \hat{v}_o + \frac{1 + Z_L (Y_o^Y + (T_{oi}^Y G_{co}^Y / G_{ci}^Y))}{1 + Z_L Y_o^Y} G_{ci}^Y \hat{c}, \\ \hat{i}_o = \frac{G_{io}^Y}{1 + Z_L Y_o^Y} \hat{v}_{in} - \frac{Y_o^Y}{1 + Z_L Y_o^Y} \hat{v}_{oL} + \frac{G_{co}^Y}{1 + Z_L Y_o^Y} \hat{c}, \end{cases} \quad (5.18)$$

which can be also given according to (5.2) by

$$\begin{cases} \hat{i}_{in} = \frac{1 + Z_L Y_{o-oci}^Y}{1 + Z_L Y_o^Y} Y_{in}^Y \hat{v}_{in} + \frac{T_{oi}^Y}{1 + Z_L Y_o^Y} \hat{v}_o + \frac{1 + Z_L Y_{o-\infty}^Y}{1 + Z_L Y_o^Y} G_{ci}^Y \hat{c}, \\ \hat{i}_o = \frac{G_{io}^Y}{1 + Z_L Y_o^Y} \hat{v}_{in} - \frac{Y_o^Y}{1 + Z_L Y_o^Y} \hat{v}_{oL} + \frac{G_{co}^Y}{1 + Z_L Y_o^Y} \hat{c}. \end{cases} \quad (5.19)$$

As stated in Eq. (5.8), $Y_{o-oci}^Y = 1/Z_{o-oci}^G$, which means that the load-impedance interaction to the input impedance does not change due to the change of output mode. If the controller of the current-output converter is designed and validated by using a resistive load, then its application in the intended usage would actually recover the internal dynamics. As a consequence of this, the control bandwidth would increase substantially. If $Z_L Y_o^Y \gg 1$, then it would be obvious that the load-affected control-to-output transfer function would be

$$G_{co}^{Y-L} = \frac{G_{co}^G}{Z_L}, \quad (5.20)$$

which means that the output-current loop gain will have the dynamic properties of the voltage-output converter. In case of DDR-controlled converters, this would mean that the designer has to consider the use of PID controller even if PI controller would suffice. This kind of situation may be valid in the cases where the storage-battery internal impedance is increasing due to a reason or another (i.e., aging, low temperature, etc.).

5.4 Impedance-Based Stability Issues

The change of output mode would also affect how the minor-loop gain has to be defined at the output terminal for having correct stability information when applying *Nyquist* stability criterion: Actually the correct minor-loop gain is also

visible in the derived source and load-interaction formulations in Eqs (5.16) and (5.19), that is, the impedance ratio shall be Z_L/Z_o^Y . The input-side minor-loop gain does not naturally change although the input impedance of the converter has experienced some changes, as discussed in Section 5.2.

5.5 Dynamic Review

A buck converter (cf. Figure 5.5) is used as an example. The converter is operated both under DDR and PCM controls in order to demonstrate the differences imposed by the different control methods. The load of the converters is a parallel connection of a 4-Ω resistor and a 5-mF capacitor mimicking the dynamic short circuit. The pure resistive load is naturally the 4-Ω resistor.

As already discussed, the resistive load would affect significantly the current-output converter dynamics as shown in Figure 5.6 in case of DDR-controlled buck

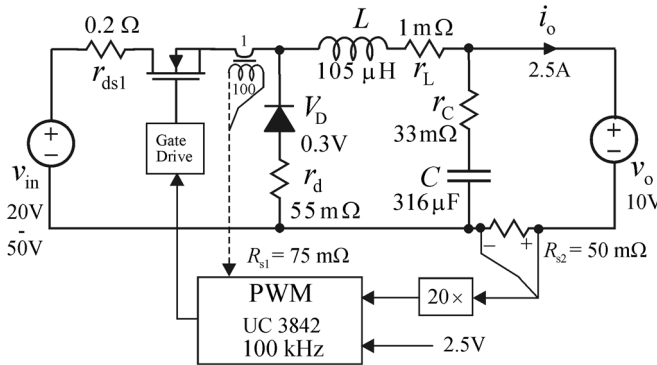


Figure 5.5 Experimental DDR/PCM-controlled buck converter at current-output mode.

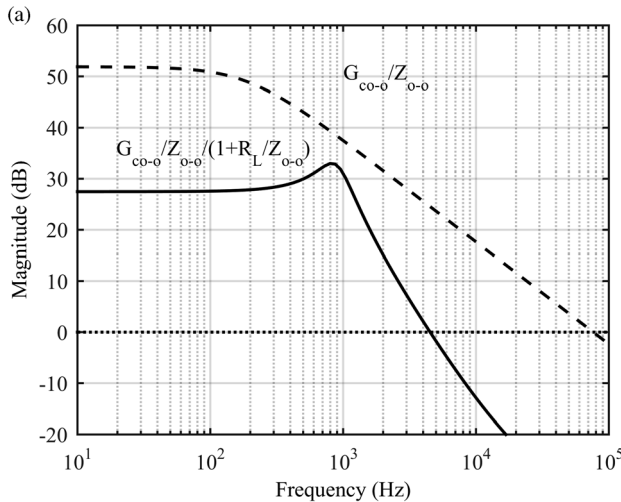


Figure 5.6 The predicted (a) and (b) measured effect of restive load on the control-to-output transfer function of the DDR-controlled buck converter.

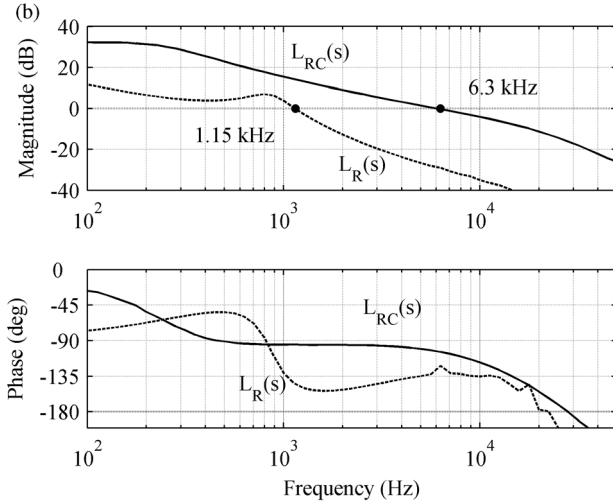


Figure 5.6 (Continued)

converter, and in Figure 5.7 in case of PCM-controlled converter: Figure 5.6a predicts that the magnitude of the control-to-output transfer function (G_{co-o}^Y) decreases significantly when the resistive load is applied, which implies that the current-loop crossover frequency can change by one decade depending on the type of load as the measured current-loop gains clearly indicated in Figure 5.6b. In addition, the resistive-load-affected loop gain shows the resonant nature of the voltage-output converter. Figure 5.7a shows the same predicted load effect on the control-to-output transfer function of the PCM-controlled converter, which implies that the current-loop crossover frequency can change even by two decades depending on the load applied, as Figure 5.7b clearly confirms.

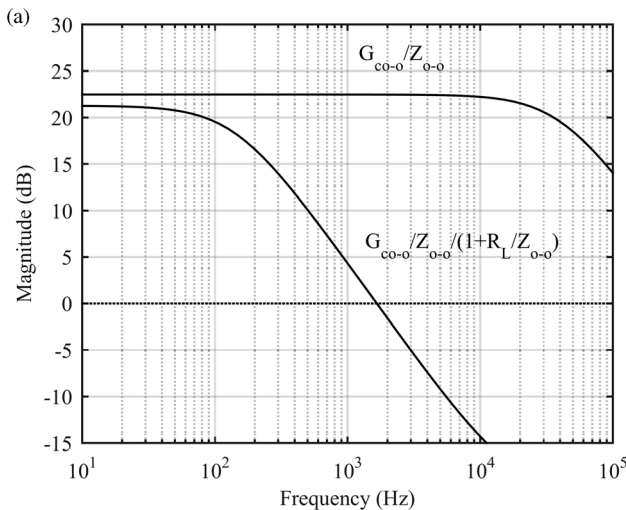


Figure 5.7 The predicted (a) and (b) measured effect of resistive load on the control-to-output transfer function of the PCM-controlled buck converter.

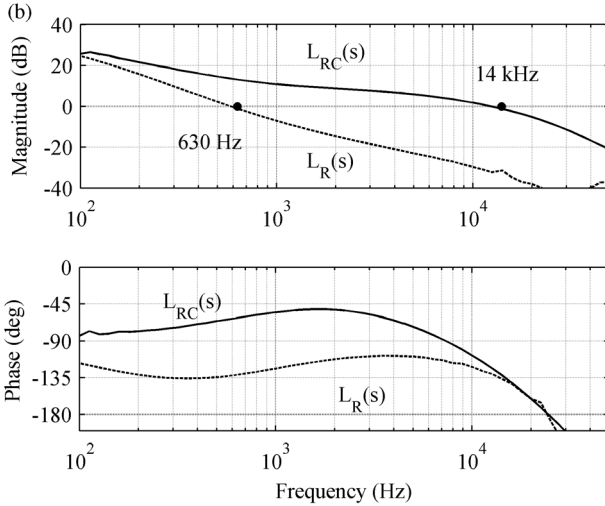


Figure 5.7 (Continued)

The design validation of the power electronic converters is very often performed by using electronic loads. The fact is, however, that usually only the constant current load behaves as expected. Figure 5.8a shows the measured open-loop output impedances of the DDR and PCM-controlled buck converter as well as the internal impedance of an electronic load configured to operate as a constant voltage load. According to the figure, the electronic load internal impedance overlaps with the open-loop output impedance of the PCM-controlled converter. This implies that the current-loop gain would be affected, as is clearly shown in Figure 5.8b: The converter is clearly close to instability, and if the design of the current-loop gain is corrected in order to meet the requirements, the outcome would be an unstable converter in normal usage.

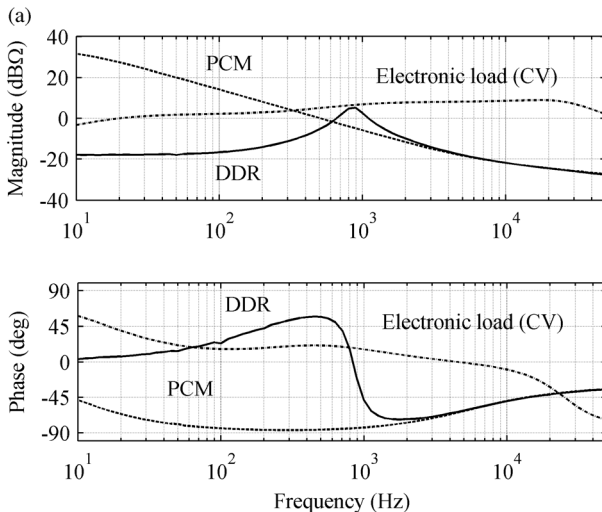


Figure 5.8 (a) The measured open-loop output impedances of the DDR and PCM-controlled buck converter as well as the internal impedance of an electronic load. (b) The measured current-loop gains of the original PCM-controlled converter and the electronic-load-affected converter.

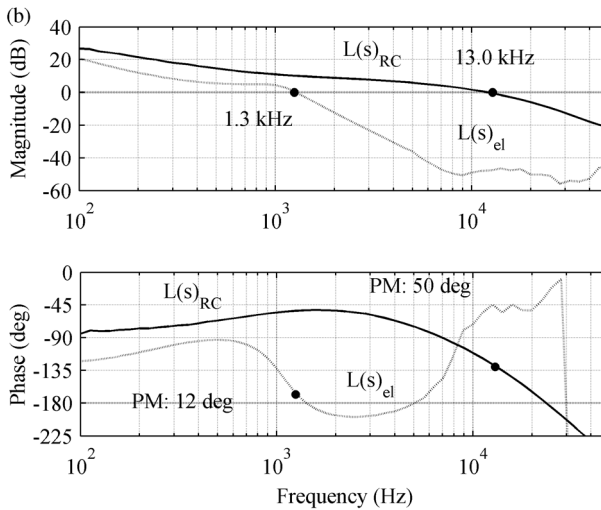


Figure 5.8 (Continued)

References

- 1 Suntio, T., Glad, A., and Waltari, P. (1996) Constant-current vs. constant-power protected rectifier as a DC UPS building block. *Proceedings of the IEEE INTELEC*, pp. 227–233.
- 2 Suntio, T., Gadoura, I., Lempinen, J., and Zenger, K. (2000) Practical design issues of multi-loop controller for a telecom rectifier. *Proceedings of the IEEE TESC*, pp. 197–201.
- 3 Lempinen, J. and Suntio, T. (2001) Small-signal modeling for design of robust variable frequency flyback battery chargers for portable device applications. *Proceedings of the IEEE APEC*, pp. 548–554.
- 4 Vazquez, S., Lukic, S.M., Galvan, E., Franguelo, L.G., and Carrasco, J.M. (2010) Energy storage systems for transport and grid applications. *IEEE Trans. Ind. Electron.*, **57** (12), 3881–3895.
- 5 Hill, C.A., Such, C., Chen, D., Gonzalez, J., and Grady, W.M. (2012) Battery energy storage for enabling integration of distributed solar power generation. *IEEE Trans. Smart Grid*, **3** (4), 850–857.
- 6 Wang, G., Ciobotaru, M., and Agelidis, V.G. (2014) Power smoothing of large solar PV plant using hybrid energy storage. *IEEE Trans. Sustain. Energy*, **5** (3), 834–842.
- 7 Suntio, T., Viinamäki, J., Jokipii, J., Messo, T., and Kuperman, A. (2014) Dynamic characteristics of power electronic interfaces. *IEEE J. Emerg. Sel. Top. Power*, **2** (4), 949–961.
- 8 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters – Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.
- 9 Sun, J. (2008) AC power electronic systems: stability and power quality. *Proceedings of the IEEE COMPEL*, pp. 1–10.

- 10 Hankaniemi, M. and Suntio, T. (2006) Small-signal models for constant-current regulated converters. Proceedings of the IEEE IECON, pp. 2037–2348.
- 11 Hankaniemi, M., Suntio, T., and Sippola, M. (2006) Analysis of the load interactions in constant-current-controlled buck converter. Proceedings of the IEEE INTELEC, pp. 343–348.
- 12 Hankaniemi, M. and Suntio, T. (2007) Dynamic modeling and control of current-output converters. *Int. Rev. Electr. Eng.*, **2** (5), 671–680.
- 13 Suntio, T., Karppanen, M., and Sippola, M. (2008) Methods to characterize open-loop dynamics of current-mode-controlled converters, Proceedings of the IEEE PESC, pp. 636–642.

6

Control Design Issues in Voltage-Fed DC–DC Converters

6.1 Introduction

The voltage-fed switched-mode converters are usually applied to supply power for different electronics loads, where the transient performance requirements can be very stringent due to low supply voltages and rapidly changing load currents as in powering microcomputers and digital signal processors [1–3]. Such applications are usually based on the use of intermediate bus architectures (IBA) shown in Figure 6.1a [4], where the converters operate as voltage-output converters. Although the load transient requirements are generally stringent, a part of the converters (i.e., the bus converter) may operate even without feedback from the output voltage for reducing the costs of implementation.

In some applications, the system may incorporate elements, which would require the use of output current limiting to protect the converters from damage, as in Telecom uninterruptible power supply (UPS) systems shown in Figure 6.2a [5]. In such a system, the converter providing the recharging of the storage batteries have to be able to operate both as a voltage-output and current-output converter requiring the use of multiloop control arrangement, as depicted in Figure 6.2b [6]. The cascaded nature of the control as well as the varying dynamic features of the voltage-output and current-output operation modes would further complicate the design of the required controllers, as shortly discussed in Section 2.3.4.

Basically, it is always question of maintaining robust stability and achieving adequate transient dynamics [7–26] within the certain constraints stipulated by the application. In practice, the internal dynamical profile of the converter would determine what the real transient dynamics would be in the operational environment [27–31]. Of course, the fact is that a poor control design would yield also poor transient performance and compromise the stability of the converter. There are also several other factors that may affect the closed-loop dynamics, such as remote sensing [32–34], and lead to unsatisfactory dynamic behavior even if the original control design would be excellent. The reader is recommended to study carefully the material provided in Chapter 2 (cf. Section 2.5) for avoiding the typical problems in control design and understanding the frequency domain behavior of different controllers. Chapters 3–5 provide in addition to the dynamic

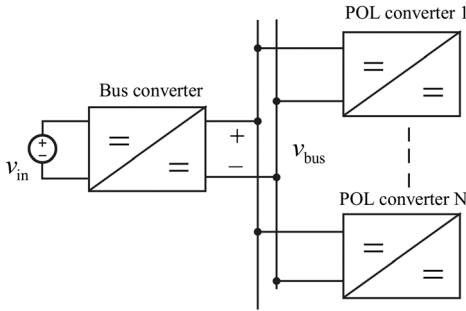


Figure 6.1 Intermediate bus architecture-based DC–DC power system.

models of the converters also detailed discussions on the control design anomalies involved in the different converters under the named internal control methods. We do not repeat those topics anymore in this chapter if not deemed absolutely necessary.

The feedback amplifier design in voltage-fed converters is most often based on the use of proportional integral derivative (PID) or proportional integral (PI) controllers [15,22–26]. In the control applications, where the control-related transfer functions exhibit resonant-like behavior, the use of PID controller is required for having capability to boost enough the phase for obtaining proper phase margin. The lack of resonant behavior may allow the use of PI controllers but the designer should carefully consider the other possible effects arising from the application of the converter (cf. e.g., current-output converters in Chapter 5).

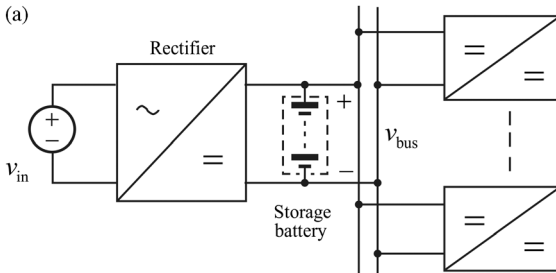
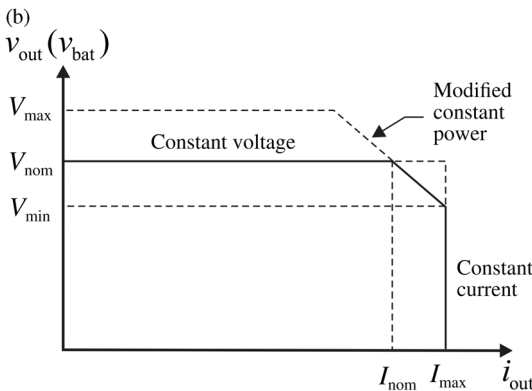


Figure 6.2 DC UPS. (a) System principle. (b) The output characteristics of the battery charger.



Very simple cost-effective control systems are often based on the use of TL431-type shunt regulators [35,36]. The dynamics and nature of the shunt regulator is usually not very well understood. Reference [23] provides detailed information on the problems associated with the application of these devices.

The rest of the chapter is organized as follows: We introduce first the method to construct the switching and averaged converter models for being able to verify the designs by simulation in MatlabTM Simulink environment. Simulink toolbox is very handy tool for these purposes. Next, we introduce the factors affecting the load transient response for being able to design the converter power stage and controller to proving fast response. The next section discusses on the problems induced by the application of output voltage remote sensing. The last section provides examples on the simple controller design method.

6.2 Developing Switching and Average Models

The switching model of the power stage can be easily constructed based on the development of the averaged state spaces for the DDR-controlled converters in Chapter 3. The basic idea in constructing the Simulink model is to integrate the derivatives of the state variables to obtain the instantaneous state variables (i.e., inductor currents and capacitor voltages) separately for on-time and off-time, respectively. The operation mode is simply selected in such a manner that the state variable value is limited to zero for DCM operation similarly as the diode works in the actual circuit. If the value of the state variable is not limited, then the converter operates in CCM all the time as if all the switches are MOSFETs allowing bipolar flow of currents. The given power-stage switching models can be used to construct the switching models for the other control modes by modifying the method to generate the duty ratio.

The averaged model is simply constructed based on the average state space of the converter following otherwise the same principles, as already discussed. This method works extremely well for the DDR-controlled converters, and yields exactly the same dynamic responses in time and frequency domains as the switching model. We will also introduce a method to construct an averaged simulation model for a PCM-controlled converter but there are some minor things that would reduce its accuracy a little bit compared to the averaged models of DDR-controlled converter.

6.2.1 Switching Models

The method to construct the switching models is illustrated by using a buck converter as an example (cf. Figure 6.3). The detailed example of the development of the averaged state space of an ideal synchronous buck converter (i.e., CCM operation only possible) is given in Section 2.4.2.

As discussed extensively in Chapter 3, the topological structures of the converter (cf. Figure 6.4) during the on-time and off-time shall be first identified for obtaining the required derivatives of the state variables (i.e., inductor current and capacitor voltage) and the dependence of the output variables (i.e., input

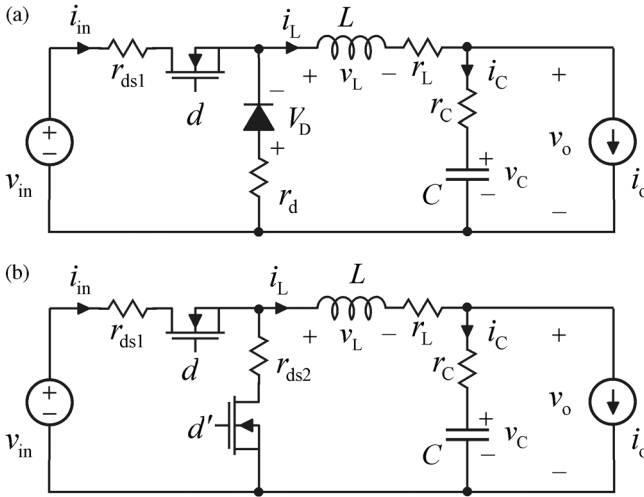


Figure 6.3 Buck converter power stage. (a) Operating both in CCM and DCM depending on the level of load current. (b) Operating only in CCM regardless of the level of load current.

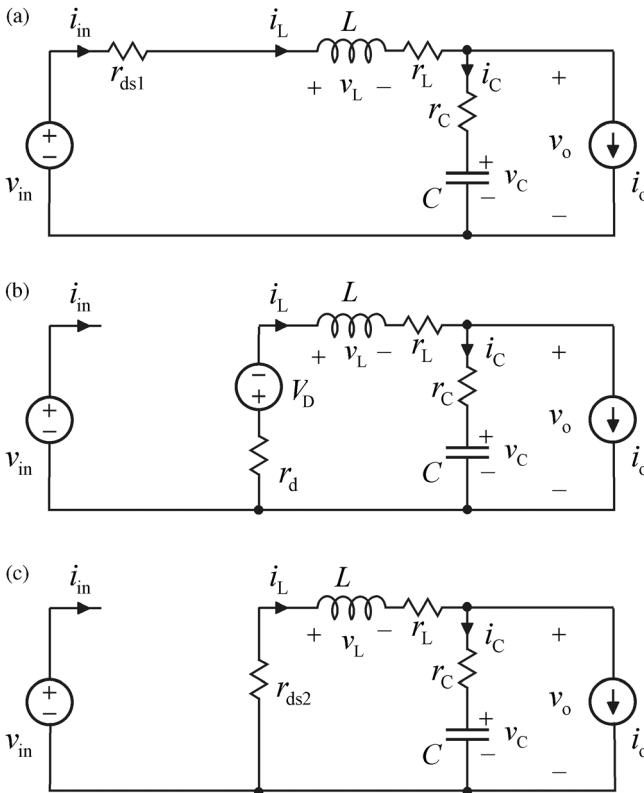


Figure 6.4 The topological sub circuit structures during (a) the on-time of both of the converters, (b) the off-time of the diode-switched converter (cf. Figure 6.3b), and (c) the off-time of the synchronous-switching converter (cf. Figure 6.3c).

current and output voltage) on the circuit variables and elements by applying Kirchhoff's laws.

Applying Kirchhoff's voltage and current laws, we can compute that during the on-time (cf. Figure 6.4a)

$$\begin{cases} v_L = v_{in} - (r_L + r_{ds1})i_L - v_o, \\ i_C = i_L - i_o, \\ i_{in} = i_L, \\ v_o = v_C + r_C i_C = v_C + r_C i_L - r_C i_o, \end{cases} \quad (6.1)$$

and during the off-time (cf. Figure 6.4b)

$$\begin{cases} v_L = -(r_L + r_d)i_L - v_o - V_D, \\ i_C = i_L - i_o, \\ i_{in} = 0, \\ v_o = v_C + r_C i_C = v_C + r_C i_L - r_C i_o, \end{cases} \quad (6.2)$$

or (cf. Figure 6.4c)

$$\begin{cases} v_L = -(r_L + r_{ds2})i_L - v_o, \\ i_C = i_L - i_o, \\ i_{in} = 0, \\ v_o = v_C + r_C i_C = v_C + r_C i_L - r_C i_o. \end{cases} \quad (6.3)$$

According to the basic electrical engineering principles, $di_L/dt = v_L/L$ and $dv_C/dt = i_C/C$. Therefore, Eqs (6.1)–(6.3) can be given by

$$\begin{cases} \frac{di_L}{dt} = \frac{v_{in}}{L} - \frac{(r_L + r_{ds1})i_L}{L} - \frac{v_o}{L}, \\ \frac{dv_C}{dt} = \frac{i_L}{C} - \frac{i_o}{C}, \\ i_{in} = i_L, \\ v_o = v_C + r_C i_L - r_C i_o. \end{cases} \quad (6.4)$$

$$\begin{cases} \frac{di_L}{dt} = -\frac{(r_L + r_d)i_L}{L} - \frac{v_o}{L} - \frac{V_D}{L}, \\ \frac{dv_C}{dt} = \frac{i_L}{C} - \frac{i_o}{C}, \\ i_{in} = 0, \\ v_o = v_C + r_C i_L - r_C i_o. \end{cases} \quad (6.5)$$

$$\begin{cases} \frac{di_L}{dt} = -\frac{(r_L + r_{ds2})i_L}{L} - \frac{v_o}{L}, \\ \frac{dv_C}{dt} = \frac{i_L}{C} - \frac{i_o}{C}, \\ i_{in} = 0, \\ v_o = v_C + r_C i_L - r_C i_o. \end{cases} \quad (6.6)$$

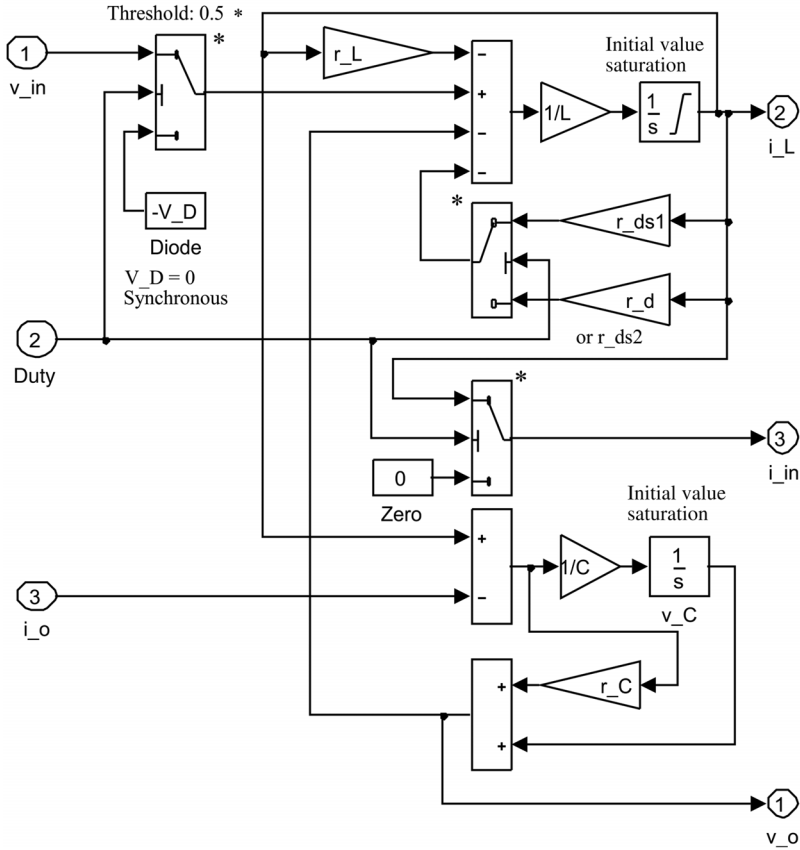


Figure 6.5 The power-stage Simulink model.

The power-stage Simulink model of the diode-switched buck converter can be given as shown in synchronous-switched buck converter shown in Figure 6.5, where the duty signal equals 1 for on-time and 0 for off-time. Therefore, the threshold for the selector switches marked with “*” shall be set to 0.5 for proper operation. The state of the selector switches are shown in the figures when the duty signal is higher than the threshold value. The switch will change its state to the lower position when the duty is less than the threshold. The initial values and saturation levels of the integrators can be set to desired values. The setting of initial values to the steady-state values may accelerate the settling processes and is, therefore, recommended to be used. If the power stage is to work also in DCM, then the lower limit of the saturation of the inductor current shall be set to zero. If the operation is to be only in CCM, then the saturation levels shall not be defined. It should be noted that the output voltage can be directly used when computing the inductor current, which is not allowed in the dynamic modeling. The differences between the two topologies are related to the value of V_D and r_d/r_{ds2} .

Figure 6.6 shows the power-stage model as an open-loop subsystem, including some necessary items connected to its input (i.e., left side) and output (i.e., right

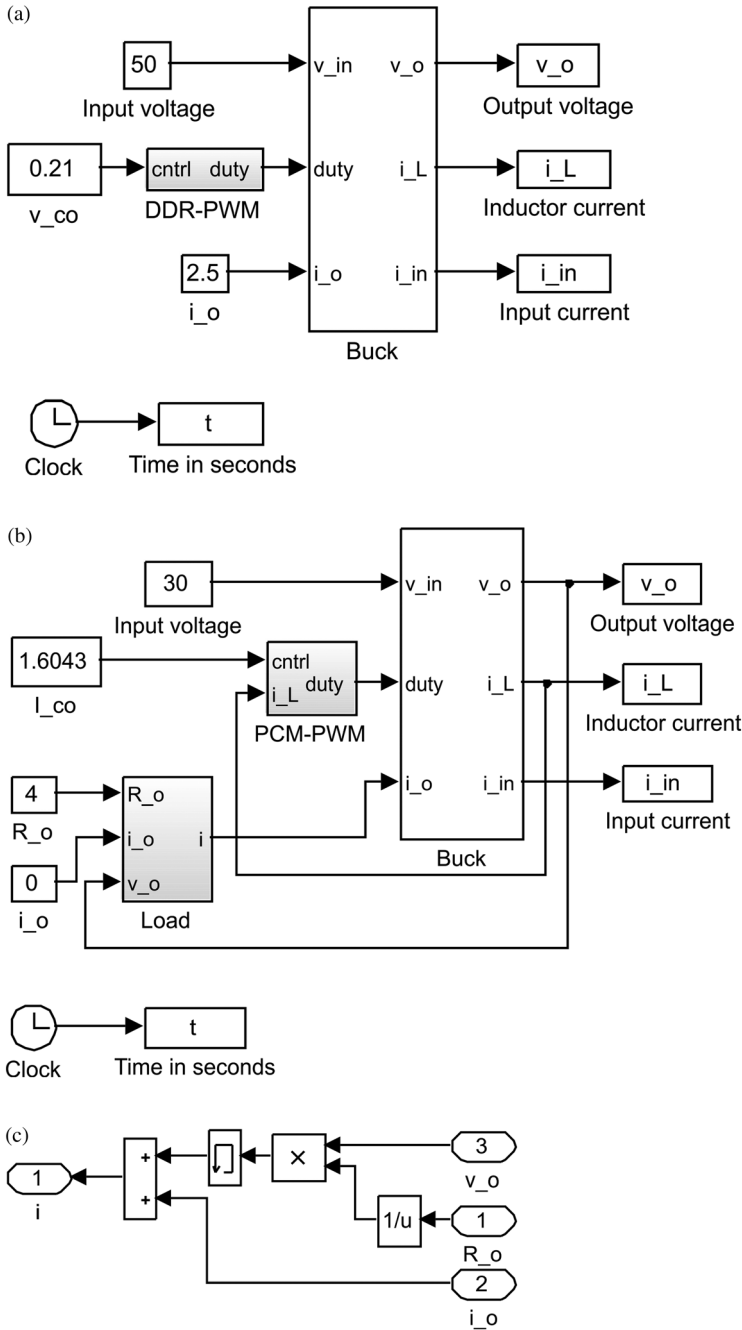


Figure 6.6 The open-loop power-stage Simulink model as a subsystem for (a) DDR-controlled second-order converters, (b) PCM-controlled second-order converters, and (c) the resistive load application.

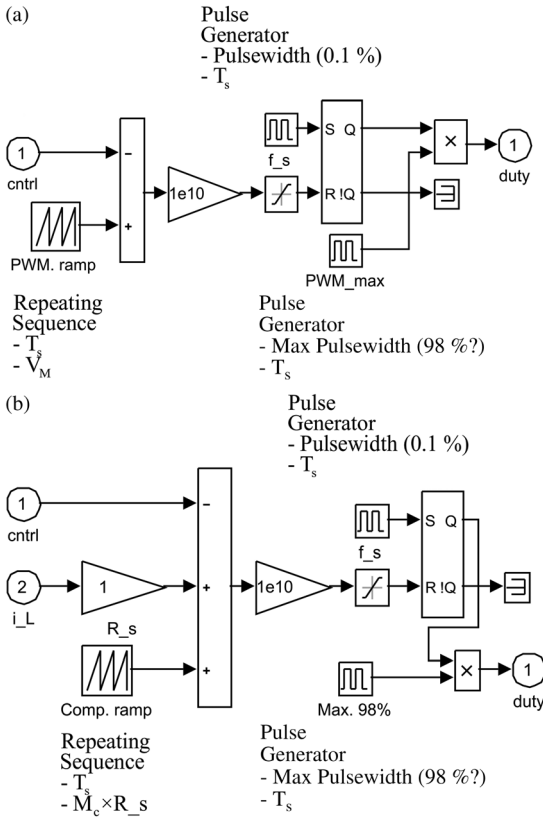


Figure 6.7 PWM modulators for (a) DDR control and (b) PCM control.

side) terminals for controlling it, recording the results for documentation, and providing timing of the events. The presented model in Figure 6.6a is applicable for DDR-controlled converters and in Figure 6.6b for PCM-controlled converters. It should be noticed that a PCM-controlled converter cannot work at constant current load but a resistive load has to be used instead (cf. Figure 6.6b). The Simulink model for the resistive load is given in Figure 6.6c.

Figure 6.7 shows the implementation of the DDR-PWM and PCM-PWM blocks to generate the duty ratio signal to control the power stage of the corresponding converters. In Figure 6.7a, the PWM ramp signal is generated by using a repeating sequence, where the cycle time ($T_s = 1/f_s$) and the minimum and maximum values (i.e., $\text{max} - \text{min} = V_M$) of the ramp have to be specified. Two pulse generators are used to generate the pace signal (i.e., switching frequency) for setting the flip-flop (i.e., initiating the cycle) and for limiting to maximum pulse width to a desired value depending on the delays in the control of the active switches, and so on. The pulse width of the pace signal shall be set to 0.1%, and the pulse width of the maximum duty ratio shall be set to the desired value. The time setting of both of the pulse generators must be equal to the inverse of the switching frequency (f_s).

In Figure 6.7b, the repeating sequence is used to compensate the inductor current loop, where the time has to be set to the inverse of the switching

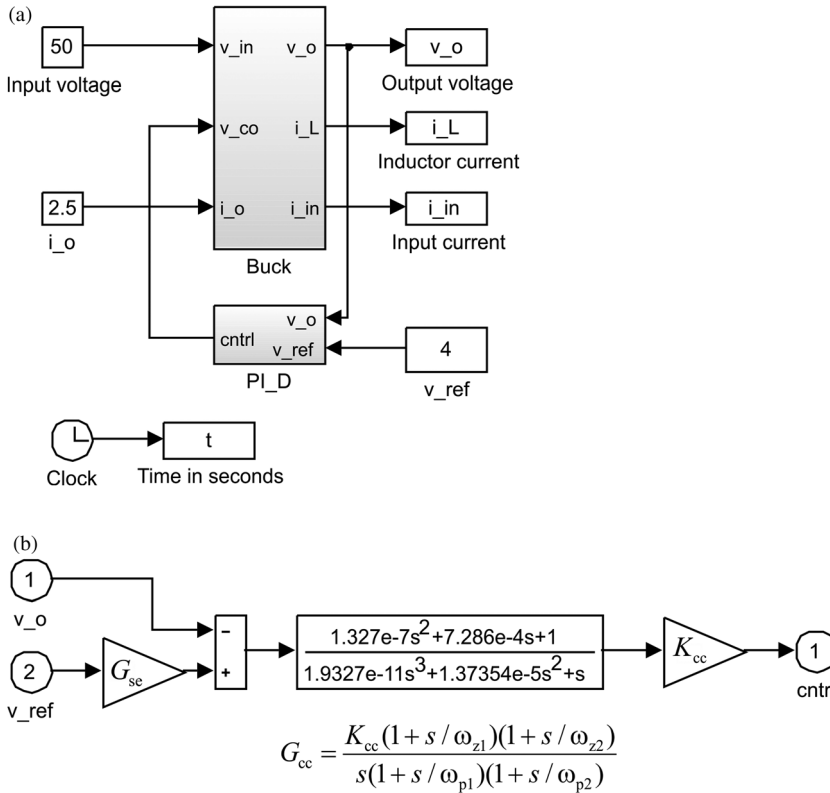


Figure 6.8 Closed-loop converter model. (a) The connection of controller to the power stage. (b) The controller implementation.

frequency, the minimum value of the ramp to zero, and the maximum value to $R_s M_c T_s$. R_s denotes the equivalent sensing resistor (Ω) of the inductor current, M_c the compensation ramp (A/s) (commonly for buck converter $V_o/2L$), and T_s the cycle time (s).

Figure 6.8 shows the closed-loop converter model, including the implementation of the control system. The controller is shown by using PID implementation as an example but the other controller types can be equally implemented based on their transfer function given in Section 2.5.6.

Figure 6.9a shows the connection of a single-section LC (SS-LC) filter at the input of the converter and Figure 6.9b the corresponding Simulink model. Figure 6.9c shows the Simulink model of the LC input filter, where L_f and C_f denote the inductor and capacitor values, respectively, and r_{Lf} and r_{Cf} their equivalent series resistances (ESR), respectively. Figure 6.9a provides the key for understanding the principles for constructing the Simulink models.

Figure 6.10a shows the connection of a single-section LC (SS-LC) filter at the output of the converter, and Figure 6.10b shows the corresponding Simulink model. Figure 6.10c shows the Simulink model of the LC-type resonant load, where L_f and C_f denote the inductor and capacitor values and r_{Lf} and r_{Cf} their

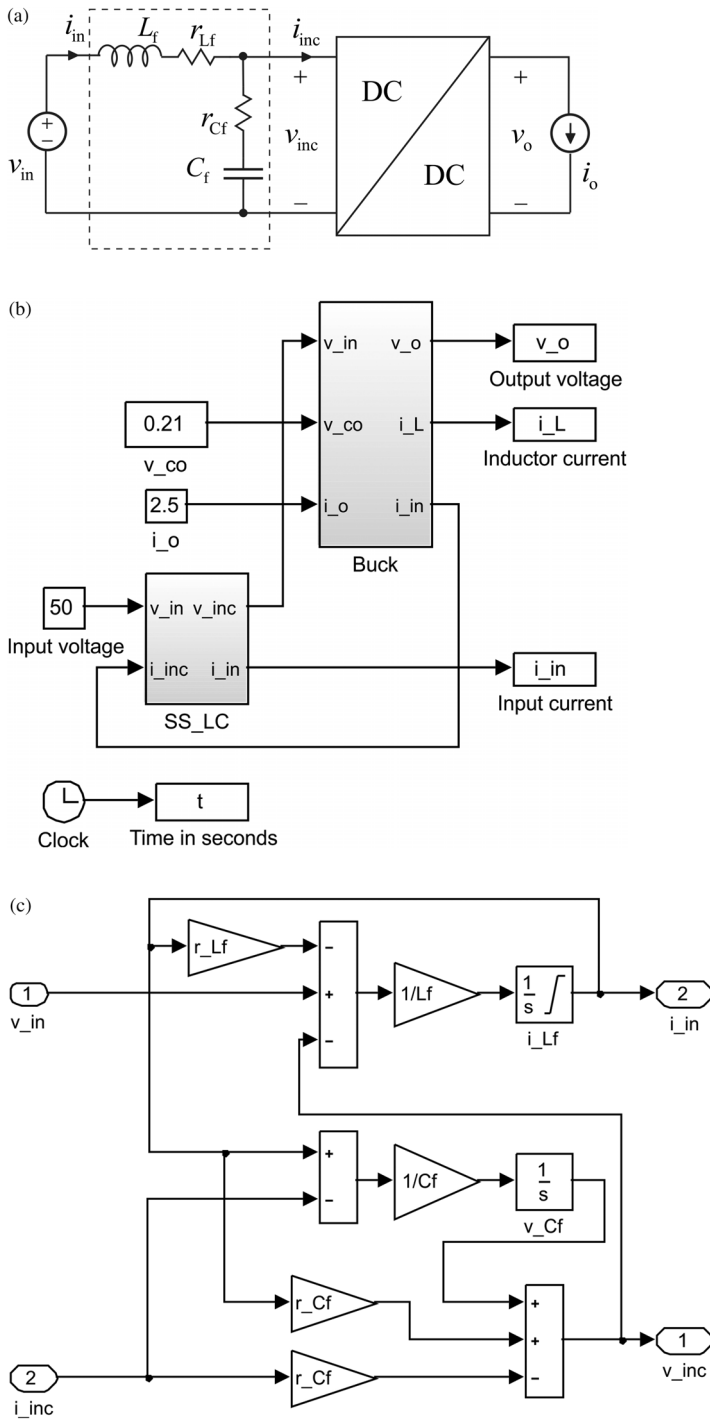


Figure 6.9 Single-section LC input filter. (a) Connection to the converter input terminal. (b) The Simulink model of the cascaded connection of the input filter and the converter. (c) The Simulink model of the LC input filter.

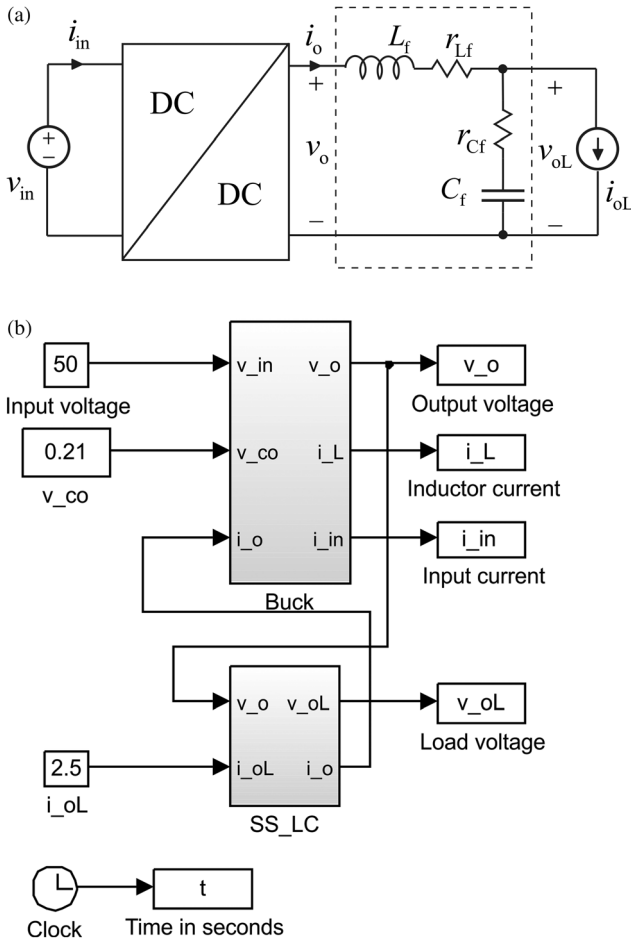


Figure 6.10 Single-section LC load filter. (a) Connection to the converter output terminal. (b) The overall Simulink model. (c) The Simulink model of the LV filter. (d) The model for combined constant current restive loads.

ESR, respectively. Figure 6.10a provides the key for understanding the principles for constructing the Simulink models.

6.2.2 Averaged Models

The averaged model of the converter is the corresponding averaged state space given in Chapter 3 for a number of converters. As an example, the Simulink model for a buck converter is given in this section, which is valid for CCM operation. It is obvious that the CCM and DCM models are different because the dynamic behaviors are different. The method to construct the Simulink models is basically the same as applied to constructing the switched models in Section 6.2.1. The main difference is that the duty ratio-controlled switch cannot be naturally used anymore. Therefore, the duty ratio and its complement have to be used directly to implement the required multiplications in the averaged state space.

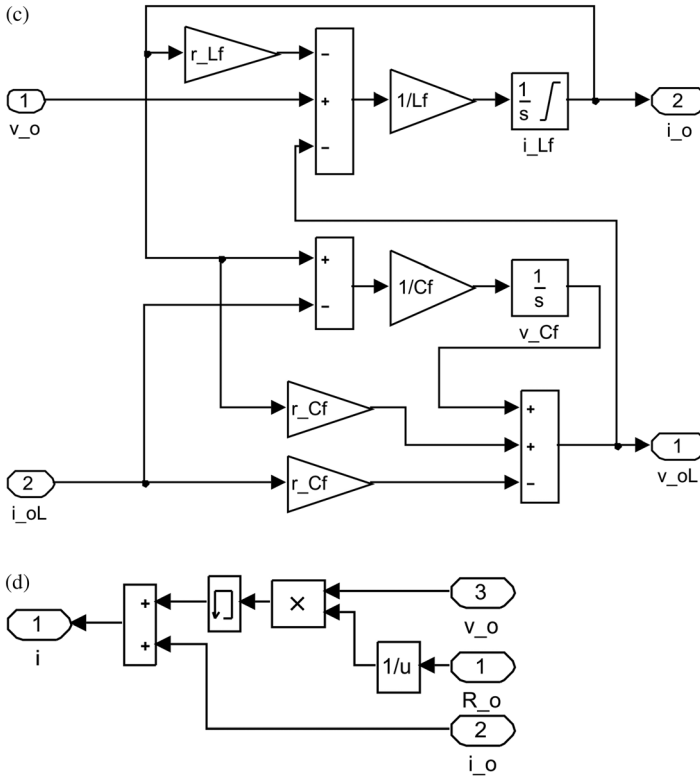


Figure 6.10 (Continued)

The averaged state space of the synchronous buck converter is given in Section 3.4.1 by

$$\begin{aligned}
 \frac{d\langle i_L \rangle}{dt} &= -\frac{r_L + dr_{ds1} + d'r_{ds2} + r_C}{L} \langle i_L \rangle - \frac{1}{L} \langle v_C \rangle + \frac{d}{L} \langle v_{in} \rangle + \frac{r_C}{L} \langle i_o \rangle, \\
 \frac{d\langle v_C \rangle}{dt} &= \frac{\langle i_L \rangle}{C} - \frac{\langle i_o \rangle}{C}, \\
 \langle i_{in} \rangle &= d \langle i_L \rangle, \\
 \langle v_o \rangle &= r_C \langle i_L \rangle + \langle v_C \rangle - r_C \langle i_o \rangle.
 \end{aligned}
 \tag{6.7}$$

Figure 6.11a shows the closed-loop Simulink model for the DDR-controlled buck converter. The power-stage model is given in Figure 6.11b and the DDR modulator model in Figure 6.11c, where V_m denotes the modulator gain and the saturation block limits the duty ratio to the range of 0–1.

The Simulink model for the PCM control is based on the same power-stage model as given in Figure 6.11b but the PWM modulator is modified to correspond to the PCM control, where the inductor current is used to provide the duty ratio, as discussed in detail in Chapter 4. The closed-loop Simulink model for the PCM-controlled converter is shown in Figure 6.12a.

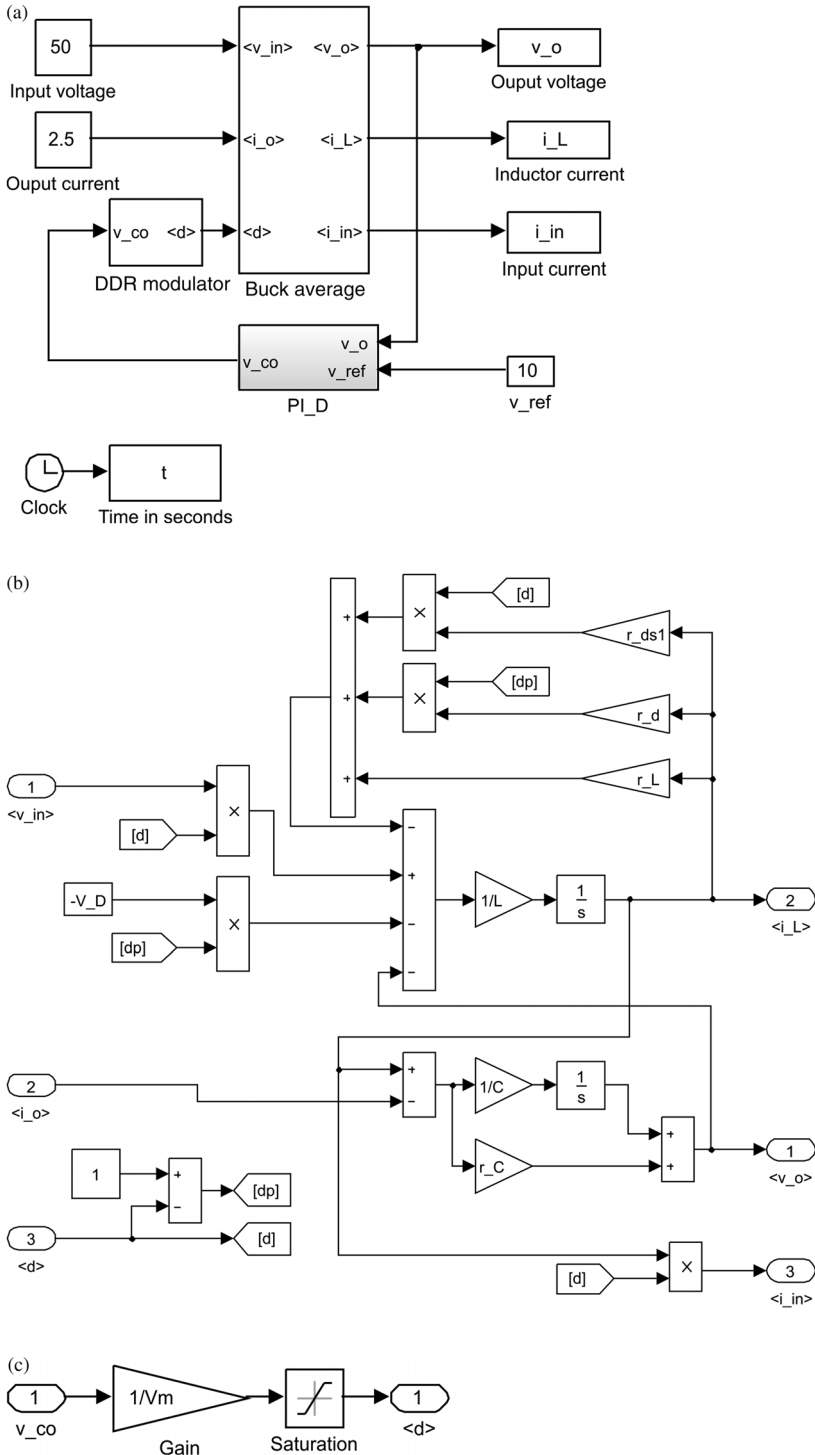


Figure 6.11 Buck converter average models for (a) closed-loop system, (b) power stage, and (c) DDR PWM modulator.

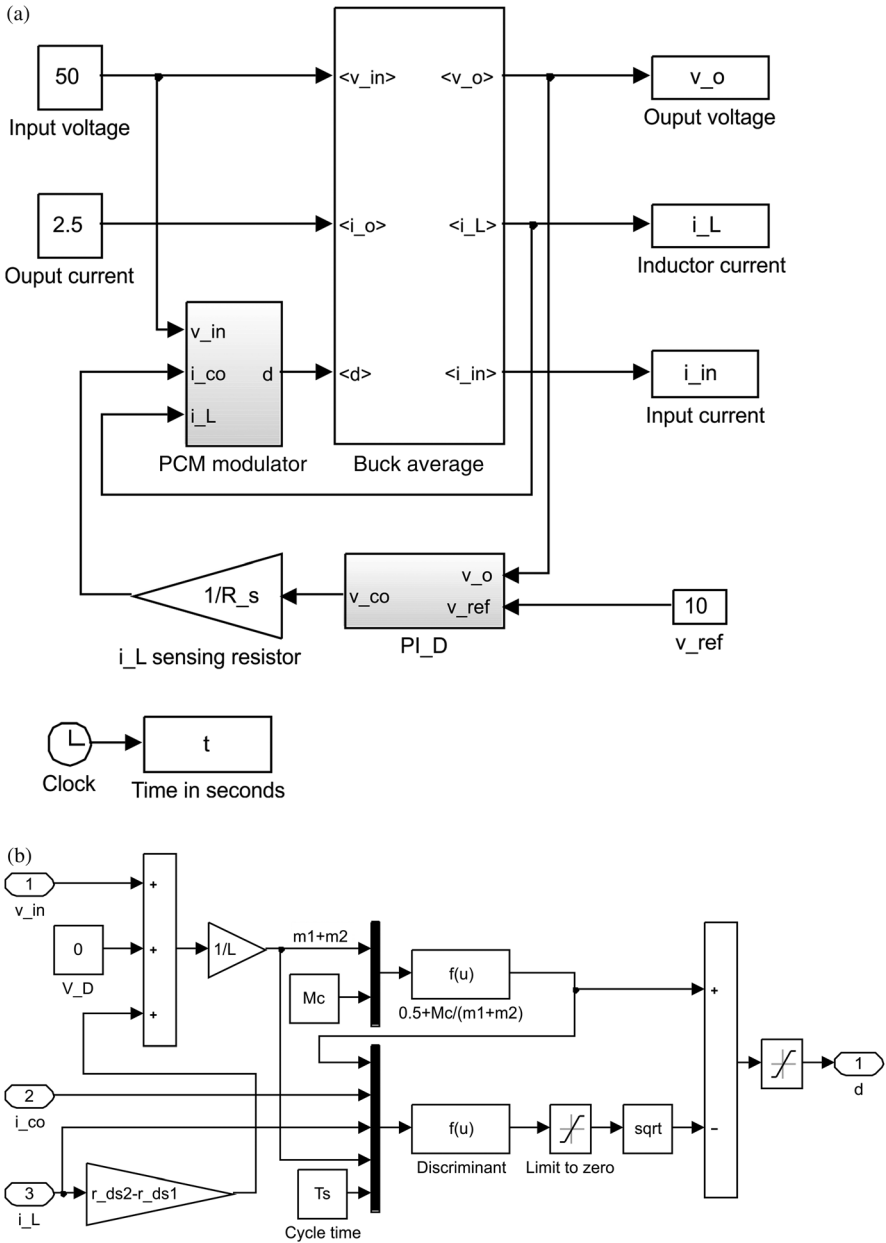


Figure 6.12 Averaged models for PCM-controlled converter in CCM. (a) Closed-loop system. (b) PCM modulator.

The general averaged comparator equation for the single-inductor converters (cf. Section 4.2.2), by means of which the duty ratio can be solved, can be given by

$$\langle i_{co} \rangle - M_c d T_s = \langle i_L \rangle + \frac{dd' T_s}{2} (m_1 + m_2), \tag{6.8}$$

where m_1 and m_2 denotes the absolute value of the inductor current up and down slopes, respectively. The comparator equation is a quadratic equation in terms of duty ratio, which can be given by

$$d^2 - \left(1 + \frac{2M_c}{m_1 + m_2}\right)d + \frac{2(\langle i_{co} \rangle - \langle i_L \rangle)}{(m_1 + m_2)T_s} = 0, \quad (6.9)$$

from which the duty ratio can be solved as follows

$$d = \frac{1}{2} + \frac{M_c}{m_1 + m_2} - \sqrt{\left(\frac{1}{2} + \frac{M_c}{m_1 + m_2}\right)^2 - \frac{2(\langle i_{co} \rangle - \langle i_L \rangle)}{(m_1 + m_2)T_s}}. \quad (6.10)$$

Equation (6.10) defines the structure of the PCM modulator to generate the duty ratio. The implementation of (6.10) in Simulink for the synchronous buck converter is shown in Figure 6.12b.

As discussed in Chapter 4, the averaged duty ratio of a PCM-controlled converter cannot be higher than the value of duty ratio at the mode limit (i.e., the operation at mode limit and second or higher harmonic modes). In the PCM modulator, this limitation is implemented by forcing the discriminator of the square root operator to be always higher or at least zero. This means that the duty ratio cannot be unity within a cycle during the dynamic operation similarly as in a practical converter. This would cause some inaccuracy in the dynamic behavior if the transient response is very fast and the steady-state duty ratio is quite close to the mode limit value (i.e., the input voltage is at its defined minimum).

Even if we have presented the development of the switching and averaged Simulink models for a buck converter, the models for other converters can be naturally developed applying the described methods as well.

6.3 Factors Affecting Transient Response

The most important and strictly specified transient response is usually the load transient response, which can be affected by means of the power-stage component and control designs. Neither of these alone would give an optimized transient response. If the control-related transfer functions of the converter incorporate RHP zeros (i.e., nonminimum phase system), then the most important control design goal is to ensure stability. The transient response would be anyway quite poor. As we have discussed in Chapter 3, the RHP zero could be sometimes removed by a proper selection of the power-stage component affecting the appearance of the zero. The use of coupled inductor technique would sometimes reduce the degree of freedom to select the components as required. From the design point of view, this kind of knowledge is quite essential.

There are several other factors, which will significantly affect the transient response as discussed in Refs [20,37–41]. The selection of the output capacitor

of a converter is sometimes implied to be performed based on the voltage ripple caused by the charge/discharge processes of the output capacitor, as in Ref. [22]. In practice, there are several other factors, which may determine the required capacitor characteristics rather than the charge/discharge-induced voltage ripple, because the capacitor has a significant role in the load transient response [20,42,43].

6.3.1 Output Voltage Undershoot

Figure 6.13 shows the simulated output voltage response to a step change of 1.5 A in the output current of the DDR-controlled buck converter shown in Figure 6.14. Figure 6.13 has been produced applying the given switched and averaged models in Section 6.2. The response is naturally similar to the response given in Ref. [20] except that the effect of series inductance is missing. In practice, the pure capacitor voltage cannot be measured, because the capacitor ESR is embedded in the capacitor.

As stated in Chapter 3, the averaged derivative of the inductor current can be given in CCM by

$$\frac{d\langle i_L \rangle}{dt} = dm_1 - d'm_2, \tag{6.11}$$

where m_1 and m_2 are the up and down slope of the inductor current, respectively, as absolute values and d and d' the duty ratio and its complement, respectively. The slopes are dependent on the voltage across the inductor and its inductance value, respectively. As Figure 6.13 indicates, the output capacitor discharges until the averaged inductor current reaches the value of the load current, causing a dip in the output voltage. It may be obvious that the larger the value of inductance and the lower the input voltage are, the larger the dip would be. The third factor is naturally the maximum value of the duty ratio, which is dependent on the ability of the controller (cf. Figure 6.14b) to react to the changes in the output voltage.

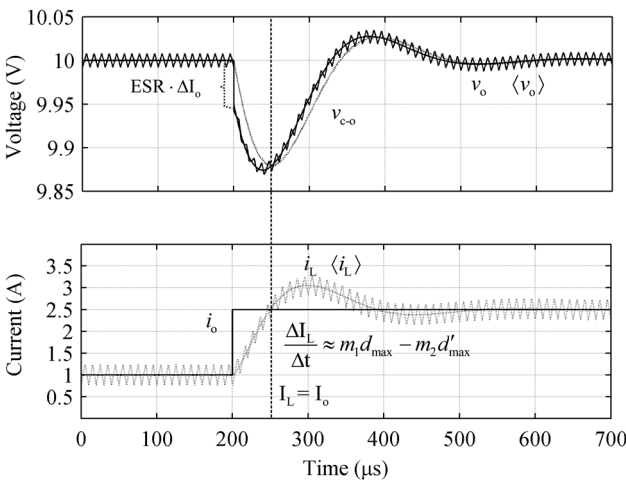


Figure 6.13 An output-voltage response to a step change in output current in a buck converter.

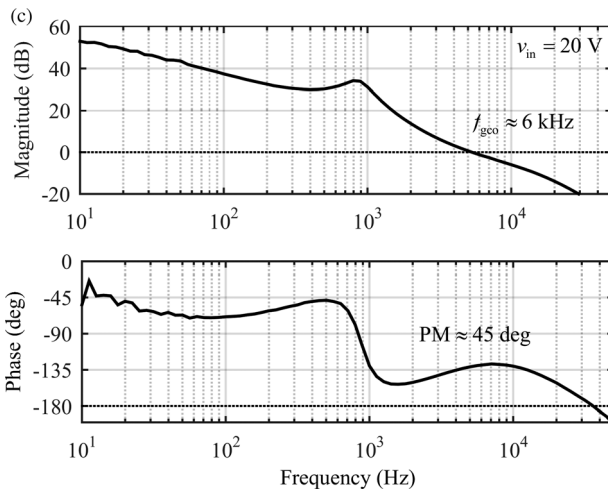
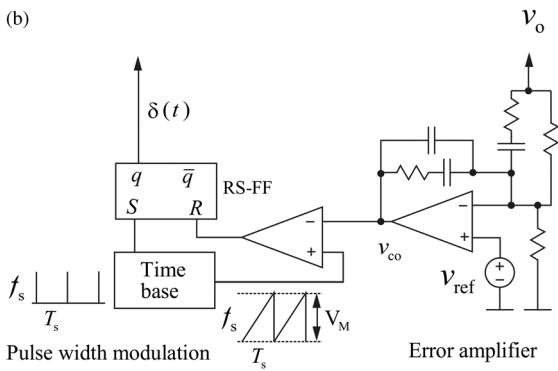
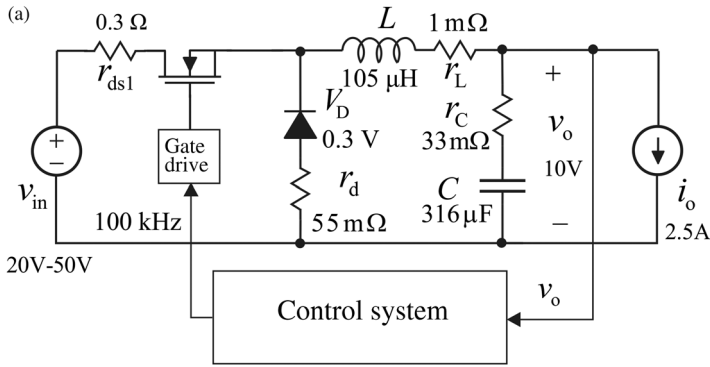


Figure 6.14 A DDR-controlled buck converter. (a) The power stage. (b) The control system. (c) The output voltage loop gain.

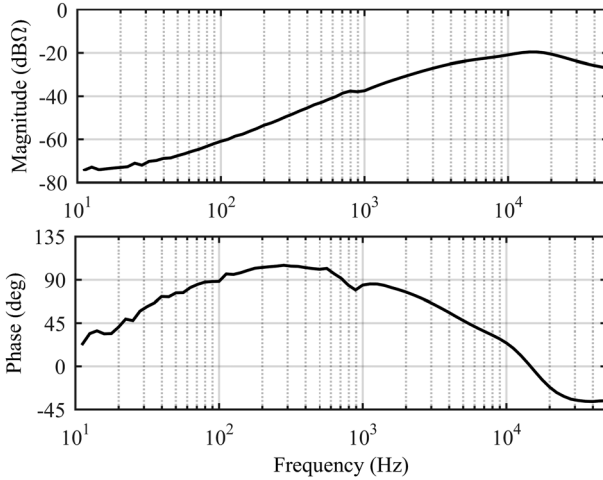


Figure 6.15 The closed-loop output impedance of the DDR-controlled buck converter.

Based on Figure 6.13 and Eq. (6.11), we can compute the value of the capacitance (C_{out}) for satisfying the requirement for a certain dip in the output voltage as follows:

$$C_{\text{out}} \geq \frac{(\Delta i_o)^2}{2\Delta v_o(d_{\text{max}}m_1 - d'_{\text{max}}m_2)}. \quad (6.12)$$

As discussed in Chapter 2, the value of the voltage dip corresponds closely to the value of the small-signal closed-loop output impedance at the voltage loop crossover frequency. According to Figure 6.15, the value of the output impedance is approximately 90 mΩ, which yields a voltage dip of 135 mV for the step change of 1.5 A in the output current. According to Figure 6.13, the voltage dip is approximately 130 mV.

The minimum voltage dip would naturally correspond to $\Delta i_o \cdot r_C$ if the control is arranged accordingly or other methods, such as the load current feedforward scheme, are applied. Applying just the output voltage feedback, the voltage dip is always higher than the absolute minimum.

6.3.2 Settling Time

According to Refs [24,25], the output voltage settling time is dependent on the location of the controller zeros, because the zeros form the time constants of the exponential functions determine the envelope behavior of the response. This can be easily understood by looking the frequency domain equation governing the output voltage transient in case of a step change in the output current, which can be given by

$$\begin{aligned} \Delta v_o(s) &= \frac{Z_{o-o}}{1 + L(s)} \cdot \Delta i_o(s), \\ L(s) &= G_{\text{se-out}} G_a G_{\text{cc}} G_{\text{co-o}}, \end{aligned} \quad (6.13)$$

where Z_{o-o} denotes open-loop output impedance, $L(s)$ output voltage feedback loop gain, G_{se-out} out voltage sensing gain, G_a modulator gain, G_{cc} controller transfer function, and G_{co-o} control-to-output-voltage transfer function. At the low frequencies, where $L(s) \gg 1$, the output voltage response in Eq. (6.13) can be given by

$$\begin{aligned} \Delta v_o(s) &\approx \frac{Z_{o-o-num}}{G_{se-out} G_a G_{cc} G_{co-o-num}} \cdot \Delta i_o(s), \\ G_{cc}(PID) &= \frac{K(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s(1 + s/\omega_{p1})(1 + s/\omega_{p2})}, \\ G_{cc}(PI) &= \frac{K(1 + s/\omega_{z1})}{s(1 + s/\omega_{p1})}. \end{aligned} \quad (6.14)$$

According to Eq. (6.14), it is obvious that the zeros of G_{cc} would form the poles of $\Delta v_o(s)$, and thereby, their inverses are the time constants of the corresponding exponential time functions. This actually means that the higher the frequency of the zeros, the faster the settling process.

Physically, the settling process is quite dependent on the behavior of the low-frequency gain of the feedback loop, which is reflected as the ability of the error amplifier (cf. Figure 6.14b) to keep the control voltage and thereby, the duty ratio to be higher than its steady-state value [37]. As a consequence, we can state that all the measures that would increase the low-frequency gain of the feedback loop would make the settling process faster. These actually include the level of modulator gain (i.e., V_M), the feedback loop crossover frequency (f_{gco}), and the phase margin (PM) as well [37]. For fast response, PM should be approximately 50 deg.

Figures 6.16 and 6.17 show the effect of the PID-controller zeros (i.e., placed at $0.25 \cdot f_{res}$, $0.5 \cdot f_{res}$, and f_{res}) and the varying input voltage on the dynamics of the

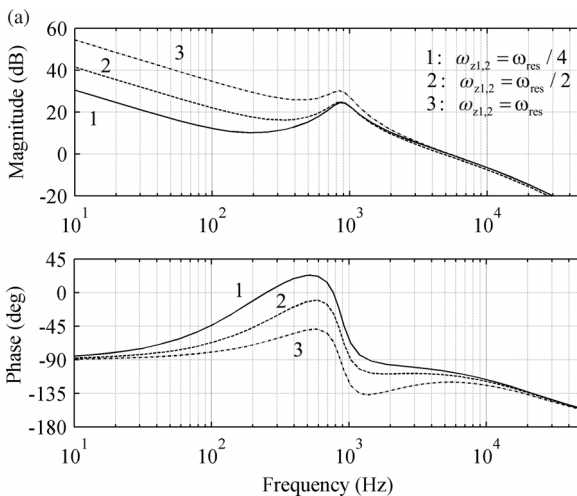


Figure 6.16 The effect of controller zeros at the input voltage of 20 V on (a) voltage feedback loop and (b) the transient response.

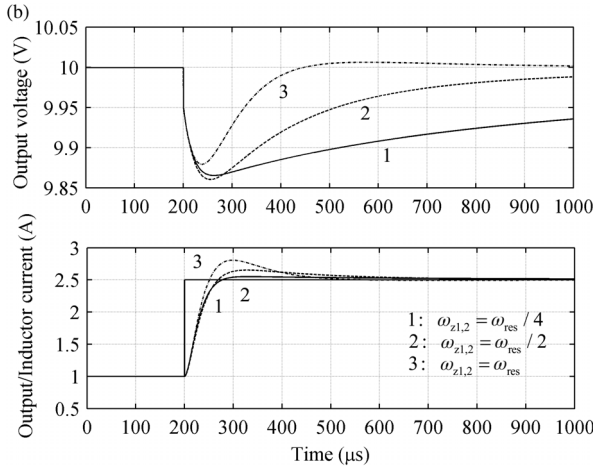


Figure 6.16 (Continued)

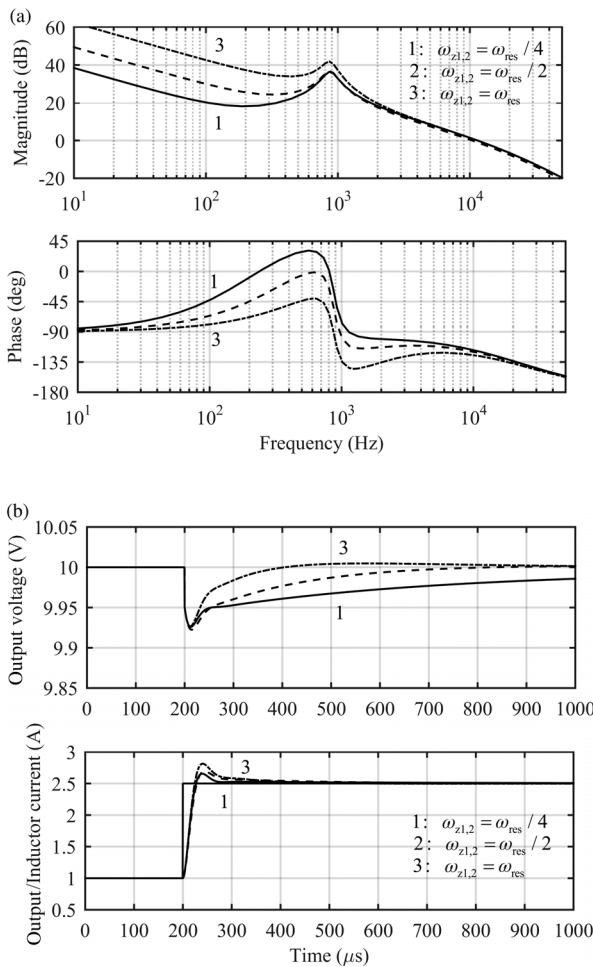


Figure 6.17 The effect of controller zeros at the input voltage of 50V on (a) voltage feedback loop and (b) the transient response.

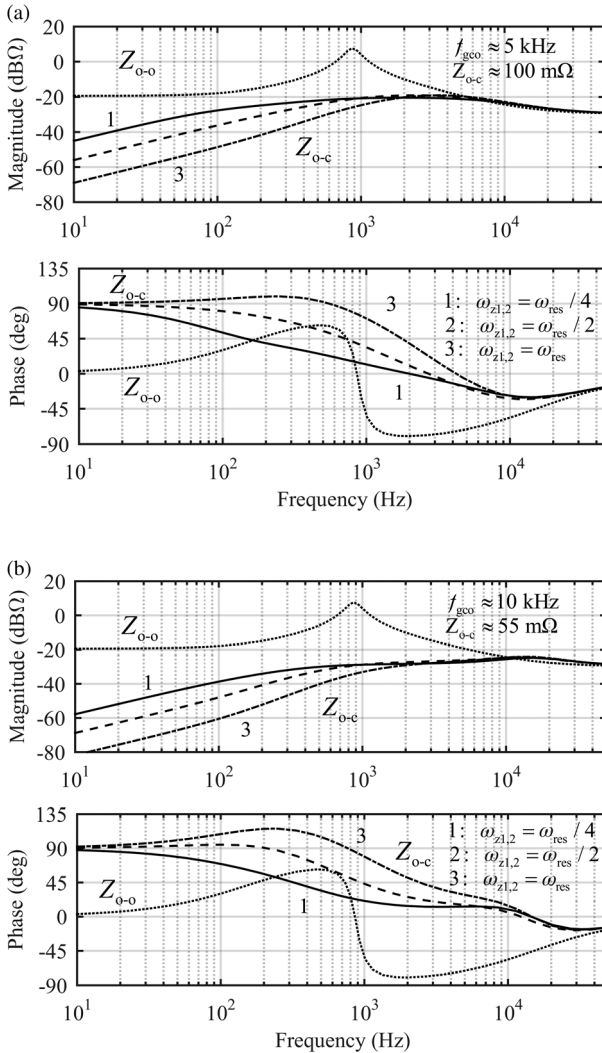


Figure 6.18 The behavior of the closed-loop output impedances due to the changes in the controller zeros and the input voltage. (a) 20 V. (b) 50 V.

DDR-controlled converter. The effect of the input voltage on the feedback loop behavior is quite clearly visible (i.e., the crossover frequency ($5 \text{ kHz}(20\text{V}) \rightarrow 10 \text{ kHz}(50\text{V})$) and the low-frequency gain (+10 dB)). The phase margin is also slightly reduced when the input voltage is increased providing slightly accelerated response. Figures 6.16b and 6.17b show the effect of the zeros and the input voltage on the output voltage transient response (i.e., the voltage dip and settling time). The reduction of the voltage dip can be actually related to the level of the output impedance at the voltage feedback loop crossover frequency (cf. Figure 6.18).

Figure 6.18 shows the effect of the controller zeros and the input voltage on the closed-loop output impedance of the DDR-controlled converter, including the

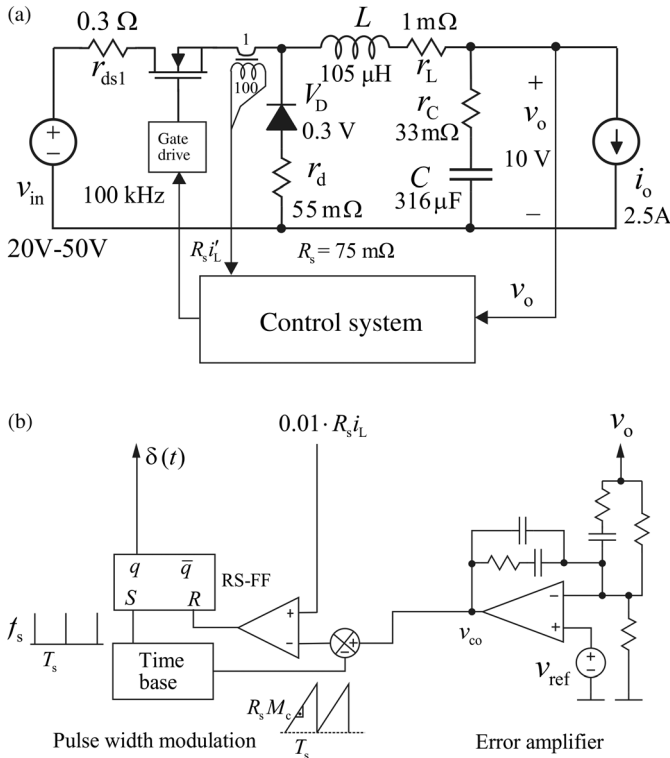


Figure 6.19 PCM-controlled buck converter. (a) The power stage. (b) The control system.

value of the output impedance at the voltage-feedback-loop crossover frequency. According to Figure 8.18a, the voltage dip would be 150 mV, and according to Figure 6.18b, the voltage dip would be 83 mV. The predicted voltage dips correspond quite well to the voltage dips readable from Figures 6.16b and 6.17b.

Figure 6.19 shows the power stage and the control-system arrangement of the PCM-controlled buck converter, which is used for analyzing the effect of the placement of the controller zeros as well as the input voltage on its output-voltage-feedback loop and load transient response. The power stage is exactly the same as in case of the DDR-controlled buck converter. As discussed in Chapter 4, the resonant-free nature of the PCM-controlled converters allows the use of PI-type feedback controller (cf. Eq. 6.14) containing only a single zero placed at $0.25 \cdot f_{res}$, $0.5 \cdot f_{res}$, and f_{res} . Even if the PCM-controlled converter does not have resonant behavior, the same inductor and output capacitor as in the DDR-controlled converter are still a part of the power stage. Therefore, the imaginary resonant frequency can be defined (i.e., $\omega_{res} = 1/\sqrt{LC}$) and applied in the control design as well.

Figure 6.20a shows the effect of the placement of the controller zero on the output voltage feedback loop at the input voltage of 20 and 50 V. As discussed in Chapter 4, the varying input voltage does not have practical effect on the loop gain at all. It should be noticed (cf. Figure 6.20a) that the phase margin is quite large,

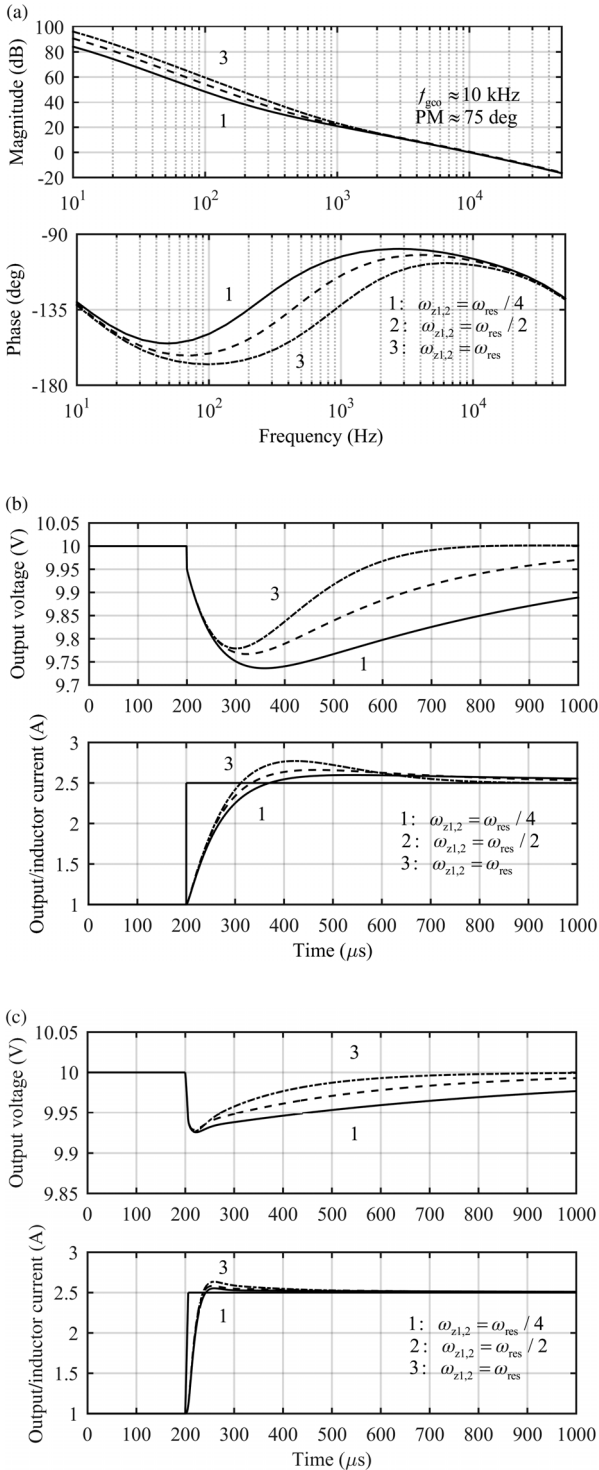


Figure 6.20 The effect of controller zeros and the varying input voltage on (a) the voltage feedback loop, (b) the transient response at the input voltage of 20 V, and (c) the transient response at the input voltage of 50 V.

which actually would make the transient response quite sluggish, as shown in Figure 6.20b ($v_{in} = 20$ V) and Figure 6.20c ($v_{in} = 50$ V). The input voltage clearly has a significant effect on the response, which would be quite expected. The responses are, however, much more sluggish than the responses of the DDR-controlled converter in Figures 6.16b and 6.17b.

The control system is modified by placing the high-frequency pole in such a manner that the phase margin would correspond to the phase margin of the DDR-controlled buck converter. The modified output voltage feedback loop gain is given in Figure 6.21a and the corresponding load transient response at the input voltage of 50 V in Figure 6.21b. The phase margin has a clear effect on the transient response. It should be understood that a too low phase

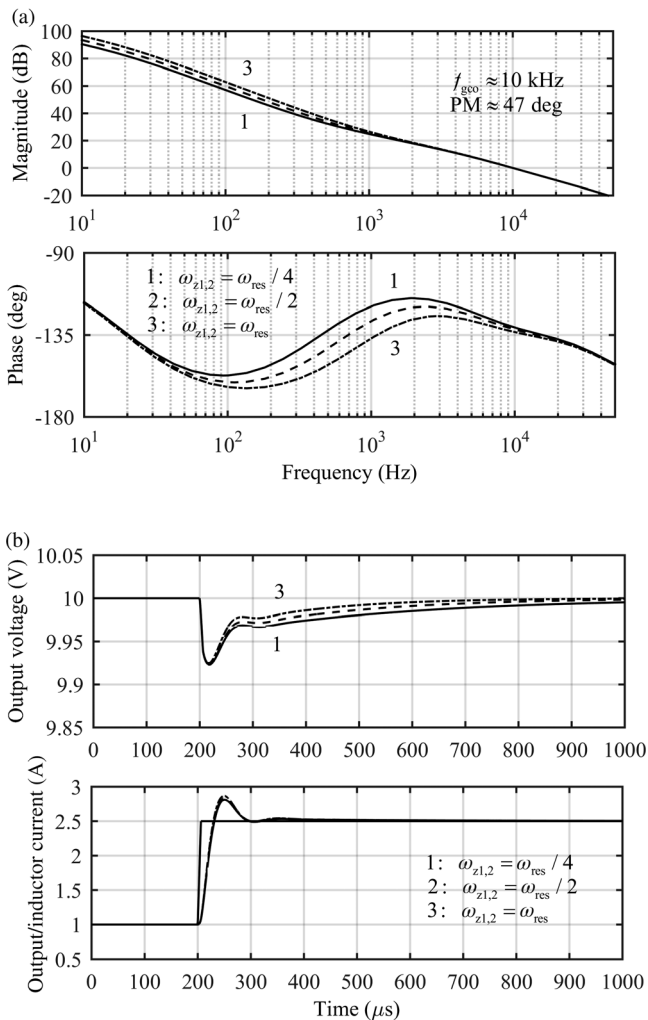


Figure 6.21 The effect of the controller zero on (a) the voltage loop gain and (b) the transient response, when the phase margin is reduced. The input voltage is 50 V.

margin could significantly deteriorate the response by causing oscillation and increasing the voltage dip by affecting the output impedance (cf. Section 2.5).

The output voltage dip corresponds usually well to the product $\Delta i_o \cdot Z_{o-c}(\omega = \omega_{gco})$, where the output impedance is defined at the output voltage loop crossover frequency as demonstrated in case of the DDR-controlled converter. The behavior of the output impedance of the PCM-controlled buck converter at the input voltage of 20 (cf. Figure 6.22a) and 50 V (cf. Figure 6.22b) are given in Figure 6.22. The output impedance of Figure 6.22a corresponds to the conditions given in Figure 6.20, and the output impedance of Figure 6.22b corresponds to the conditions given in Figure 6.21.

According to Figure 6.20b, the voltage dip is approximately 250 mV, and the predicted voltage dip is 77 mV. According to Figure 6.21b, the voltage dip is

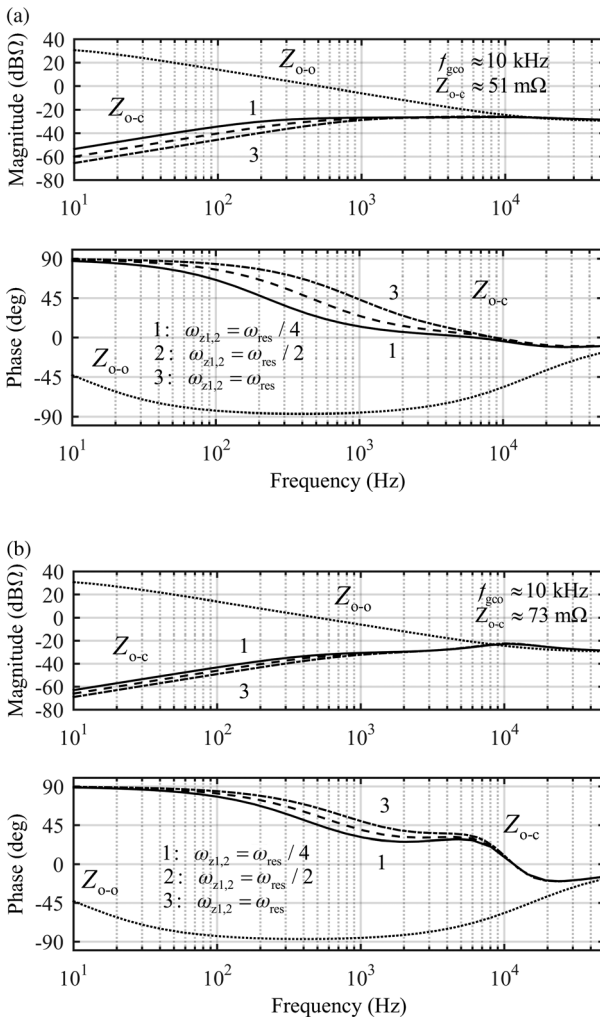


Figure 6.22 The predicted output impedances of the PCM-controlled buck converter at the input voltage of (a) 20 V and (b) 50 V.

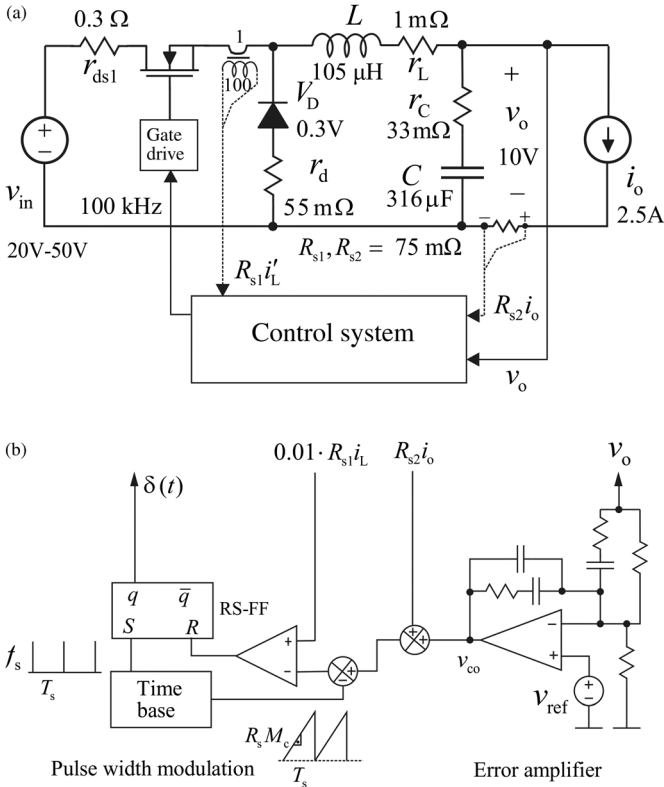


Figure 6.23 The buck converter. (a) The power stage and connections to the control system. (b) The PCM-OCF control system.

approximately 75 mV, and the predicted voltage dip is 110 mV. The accuracy of the predictions based on the small-signal behavior of the PCM-controlled converter is not very high at all, but it gives only a good estimate.

Figure 6.23 shows the power stage of a practical buck converter including the required connections for control system as DRR, PCM, and PCM-OCF converter (Figure 6.23a) as well as the control system of PCM-OCF mode (Figure 6.23b). The other control system principles are given in Figures 6.14b (DDR) and 6.19b (PCM), respectively. More detailed information on the PCM-OCF control implementation can be found from Ref. [44]. In practice, a large input capacitor has to be connected at the input terminal of the converter in order to avoid damage due to the rapidly changing input current and cabling inductance.

The output-voltage load-transient responses of the converters, when a step change of 2 A in the output current is applied, are given in Figure 6.24a. Figure 6.24b and c show the measured output-voltage-loop gains and the corresponding closed-loop output impedances.

Figure 6.24b indicates that the crossover frequency of the control loop in the DDR-controlled converter is approximately 5 kHz and PM approximately 49°. The same values for the PCM-controlled converters are 12 kHz and 64°,

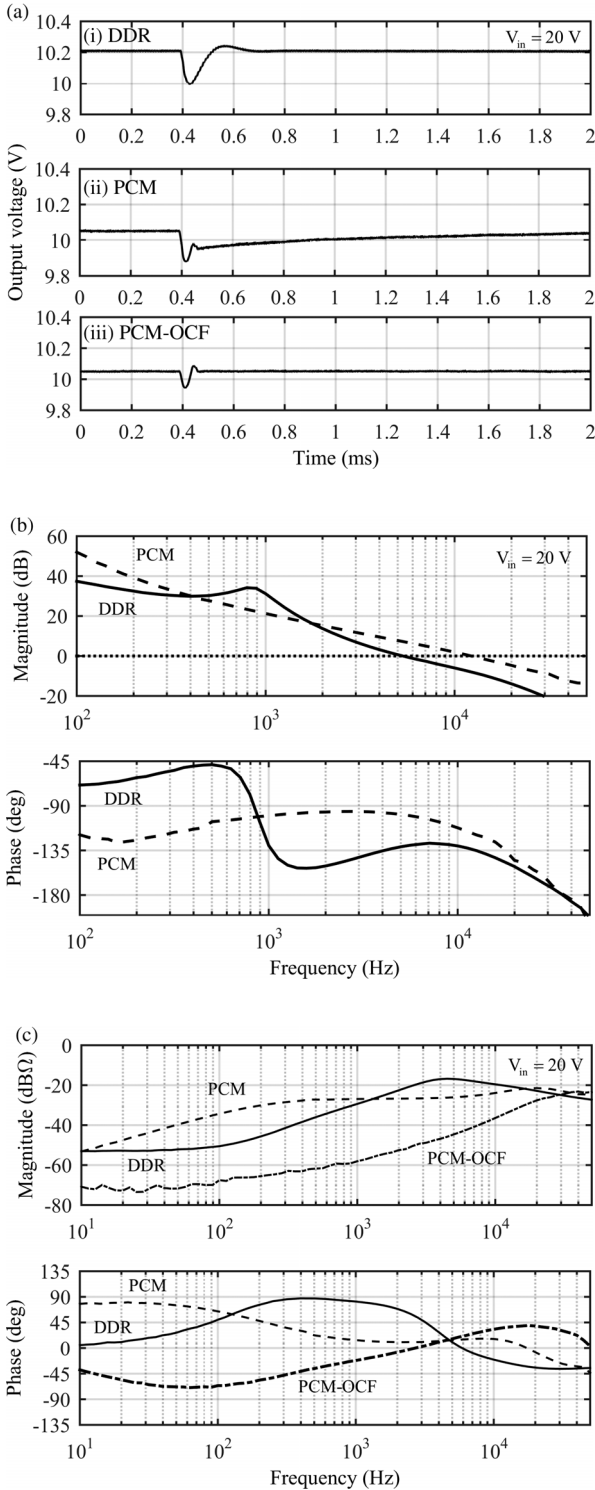


Figure 6.24 The measured (a) output voltage load transients, (b) output voltage loop gains, and (c) closed-loop output impedances.

respectively. The control systems are designed in such a manner that the controller zeros are placed at $0.5 \cdot \omega_{\text{res}}$. As discussed earlier, the output voltage responses would be slightly better if the zeros were placed closer to the resonant frequency and the phase margin of the PCM-controlled converter were decreased close to the phase margin of DDR-controlled converter.

According to Figure 6.24c, the closed-loop output impedances at the output-voltage-loop crossover frequency are as follows: DDR: 143 m Ω , PCM: 73 m Ω , and PCM-OCF: 18 m Ω . In these cases, the small-signal output impedances predict quite well the measured voltage dips except for the PCM-OCF converter: DDR: 216 mV versus 286 mV; PCM: 180 mV versus 145 mV, and PCM-OCF: 106 mV versus 36 mV. Basically, the minimum dip should be approximately 66 mV due to the ESR of the output capacitor as all the measured voltage dips definitively are.

6.4 Remote Sensing

6.4.1 Introduction

Usually the commercially available DC–DC converter modules are equipped with two extra pins, which are intended for remote sensing the voltage at the exact input terminals of the load powered by the DC–DC converter (cf. Figure 6.25). It is not very well known, however, that the application of the remote sensing can deteriorate the dynamics of the power module, and thereby, also the well-being of the load system due to the extra impedances between the converter and the load [32–34]. The effect of the external input and output impedance on the converter dynamic behavior is well known, as already discussed in Chapters 3, 4, and 5. Actually, similar methods as used in the source, and load interaction analyses can be equally utilized also to analyze the effect of the remote sensing-related impedances denoted in Figure 6.25 by Z_{remote} .

6.4.2 Remote Sensing Dynamic Effect Analysis Method

Similarly as developing the general load-affected dynamic models of a converter in Section 2.2.5, the same methods can also be applied to a more complex load than just a single impedance, as used in Chapter 2. The only difference is that the load subsystem contains four elements instead of one.

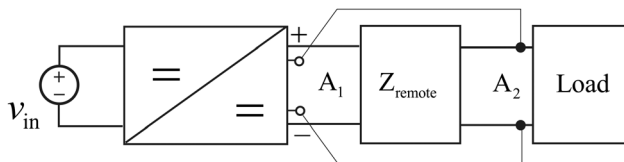


Figure 6.25 Typical application of output voltage remote sensing.

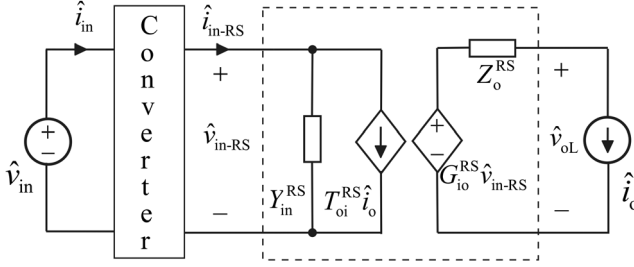


Figure 6.26 A cascaded system consisting of the converter and the remote sensing impedance block.

Based on Figure 6.26 and the G -parameters of the converter at open loop, the subsystems can be given by

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{in-RS} \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{oi-o} & G_{ci-o} \\ G_{io-o} & -Z_{o-o} & G_{co-o} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{in-RS} \\ \hat{c} \end{bmatrix}, \quad (6.15)$$

$$\begin{bmatrix} \hat{i}_{in-RS} \\ \hat{v}_{oL} \end{bmatrix} = \begin{bmatrix} Y_{in}^{RS} & T_{oi}^{RS} \\ G_{io}^{RS} & -Z_o^{RS} \end{bmatrix} \begin{bmatrix} \hat{v}_{in-RS} \\ \hat{i}_o \end{bmatrix},$$

and the remote sensing impedance-affected dynamic description of the converter can be given by

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{oL} \end{bmatrix} = \begin{bmatrix} Y_{in-o} + \frac{Y_{in}^{RS} G_{io-o} T_{oi-o}}{1 + Z_{o-o} Y_{in}^{RS}} & \frac{T_{oi}^{RS} T_{oi-o}}{1 + Z_{o-o} Y_{in}^{RS}} & G_{ci-o} + \frac{Y_{in}^{RS} G_{co-o} T_{oi-o}}{1 + Z_{o-o} Y_{in}^{RS}} \\ \frac{G_{io}^{RS} G_{io-o}}{1 + Z_{o-o} Y_{in}^{RS}} & -\frac{1 + Z_{o-o} Y_{in-sco}^{RS}}{1 + Z_{o-o} Y_{in}^{RS}} Z_o^{RS} & \frac{G_{io}^{RS} G_{co-o}}{1 + Z_{o-o} Y_{in}^{RS}} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix}, \quad (6.16)$$

where Y_{in-sco}^{RS} denotes the short-circuit input admittance of the remote sensing impedance block and can be defined by

$$Y_{in-sco}^{RS} = Y_{in}^{RS} + \frac{G_{io}^{RS} T_{oi}^{RS}}{Z_o^{RS}}. \quad (6.17)$$

According to Eq. (6.16), it may be obvious that the dynamic behavior may change significantly compared to the situation where the remote sensing is not used. We will show later that even small inductances and capacitances can have a significant effect and make the converter sensitive even to instability.

Based on Figure 6.26, the basic understanding of the formation of the special impedance/admittance parameters of the converter is as follows:

- The ideal input admittance ($Y_{in-\infty}$) would stay intact, because the output side current is zero in small-signal sense, when the ideal input admittance is determined,
- The short-circuit input admittance (Y_{in-sco}) would change, because the impedance block generates an impedance in the output current path. The overall

short-circuit input impedance can be easily defined by inspecting the circuitry given in Figure 6.26 as an impedance by

$$Z_{\text{in-sco}}^M = Z_{\text{in-sco}} + \frac{Z_{\text{in-sco}}^{\text{RS}}}{M(D)^2}, \tag{6.18}$$

where the superscript M denotes the overall short-circuit input impedance and $M(D)$ the ideal input-to-output modulo of the original converter. This means that the converter sensitivity to source interactions would be changed.

- The other special parameters can be naturally easily computed based on Eq. (6.16) and the definition of the parameters, for example in Section 3.4, which are valid for the voltage-fed voltage-output converters. In a generalized form, the definitions can be found from Section 2.2.

6.4.3 Remote Sensing Impedance Block Examples

The typical remote sensing impedance blocks are the cable or circuit board trace connection shown in Figure 6.27a and the T-type LCL circuit shown in Figure 6.27b.

The impedance blocks in Figure 6.27 can be represented by means of their G -parameter sets as follows (cf. Eq. (6.15)):

$$\begin{bmatrix} 0 & 1 \\ 1 & -(sL_{\text{RS}} + r_{\text{L-RS}}) \end{bmatrix} \left[\begin{array}{c} \frac{sC_{\text{RS}}}{s^2L_{\text{RS1}}C_{\text{RS}} + s(r_{\text{L-RS1}} + r_{\text{C-RS}})C_{\text{RS}} + 1} \quad \frac{1 + sr_{\text{C-RS}}C_{\text{RS}}}{s^2L_{\text{RS1}}C_{\text{RS}} + s(r_{\text{L-RS1}} + r_{\text{C-RS}})C_{\text{RS}} + 1} \\ \frac{1 + sr_{\text{C-RS}}C_{\text{RS}}}{s^2L_{\text{RS1}}C_{\text{RS}} + s(r_{\text{L-RS1}} + r_{\text{C-RS}})C_{\text{RS}} + 1} - \left(sL_{\text{RS2}} + r_{\text{L-RS2}} + \frac{(r_{\text{L-RS1}} + sL_{\text{RS1}})(1 + sr_{\text{C-RS}}C_{\text{RS}})}{s^2L_{\text{RS1}}C_{\text{RS}} + s(r_{\text{L-RS1}} + r_{\text{C-RS}})C_{\text{RS}} + 1} \right) \end{array} \right]. \tag{6.19}$$

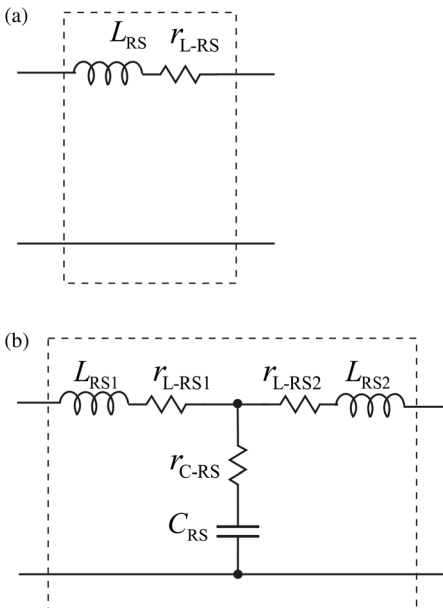


Figure 6.27 Remote sense impedance blocks. (a) Cable connection. (b) T-type LCL circuit.

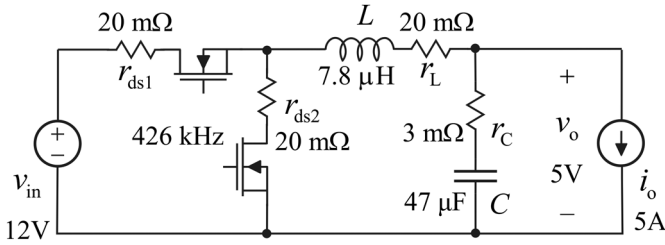


Figure 6.28 The power stage of the experimental synchronous buck converter.

6.4.4 Experimental Evidence

The experimental analyses of the effect of output-voltage remote sensing on the converter dynamics are performed by using the DDR-controlled buck converter given in Figure 6.14a and the DDR-controlled synchronous buck converter given in Figure 6.28. The component values of the used remote sensing impedance blocks are defined in Figure 6.29. The selection of the capacitor in the T-type impedance block in Figure 6.29b has to be performed in such a manner that its ESR is high enough for maintaining the stability of the converter.

The remote sensing effect of the 100 kHz DDR-controlled buck converter (cf. Figure 6.14a) was tested by connecting the connection cable between the converter output and the load. Figure 6.30a shows that the output impedance of the converter will become inductive at the high frequencies. The inductive nature of the output impedance would make the converter sensitive, especially, to capacitive load. Figure 6.30b shows the measured internal (1) and cable

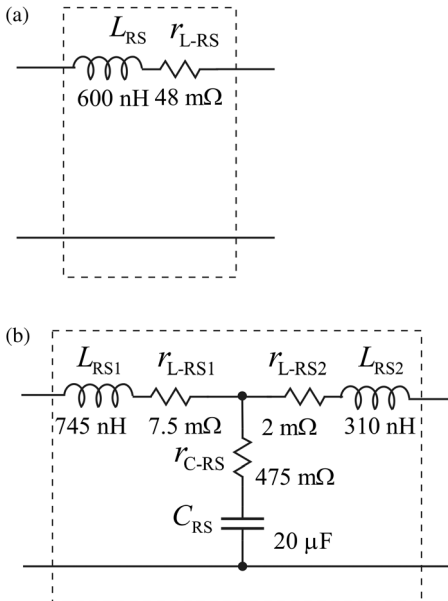


Figure 6.29 The component definitions of the remote sensing impedance blocks. (a) Connection cable. (b) T-type LCL circuit.

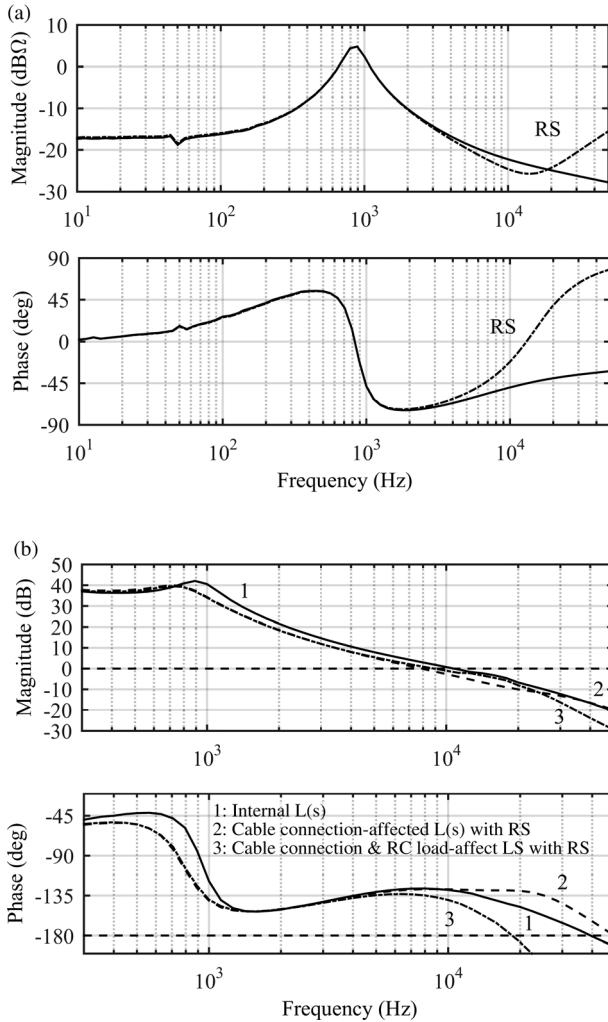


Figure 6.30 The effect of a connection cable on (a) the open-loop output impedance and (b) the effect of an additional RC loading on the converter loop gain.

connection-affected (2) output-voltage loop gains, where the effect of the inductive loading is visible as an increase in the loop phase only. An RC circuit was connected at the input terminal of the load, where the capacitance value is $110\ \mu\text{F}$ and the resistance value $4\ \Omega$. The effect of the combination of the cable connection and the RC load on the output voltage loop gain is shown in Figure 6.30b as the curve (3). It is obvious that the converter would be close to instability, which clearly confirms the existence of the sensitivity to capacitive load as already discussed.

The effect of the T-type LCL block on the converter dynamics was tested by using the synchronous buck converter (cf. Figure 6.28). The LCL load-affected (cf. Figure 6.29b) open-loop output impedance of the converter is shown in

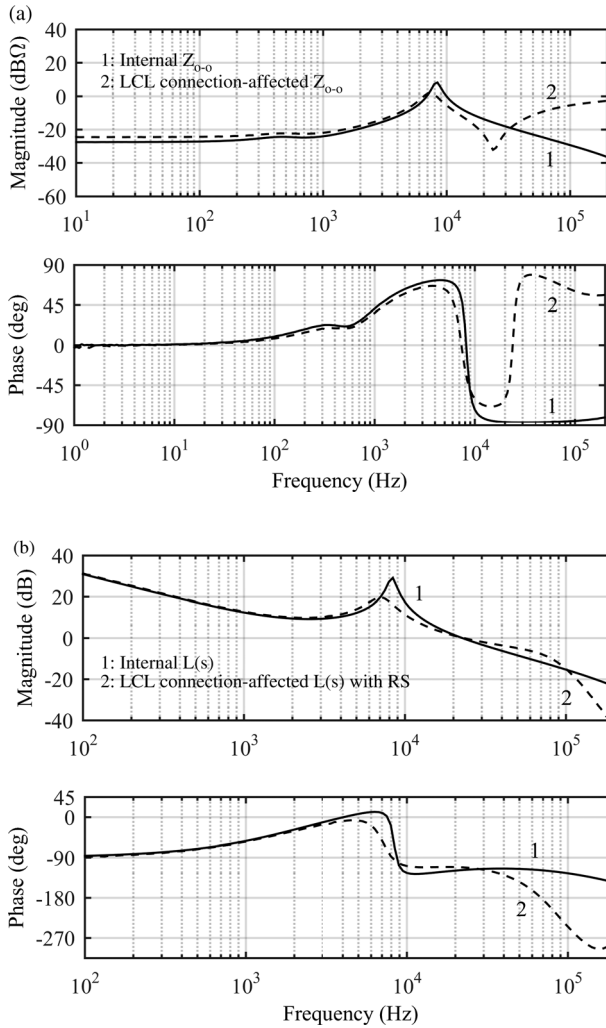


Figure 6.31 The remote sensing effect of T-type LCL impedance block on (a) the open-loop output impedance and (b) the output voltage loop gain.

Figure 6.31a containing the resonant behavior characteristic to resonant circuit. Figure 6.31b shows the LCL load-affected output-voltage loop gain, where the robustness of the performance is clearly deteriorated. Figures 6.32 and 6.33 show the corresponding time domain output-voltage responses (a) without LCL impedance connection, (b) with the LCL impedance but without remote sensing, and (c) with the remote sensing confirming the reduction in the performance robustness.

It may be obvious that the application of the remote sensing option in the DC–DC converter modules requires careful considerations, identification of the additional impedances, and analyzing their effect on the system performance before activating the connection. The sufficient techniques to do the required measures are already well presented.

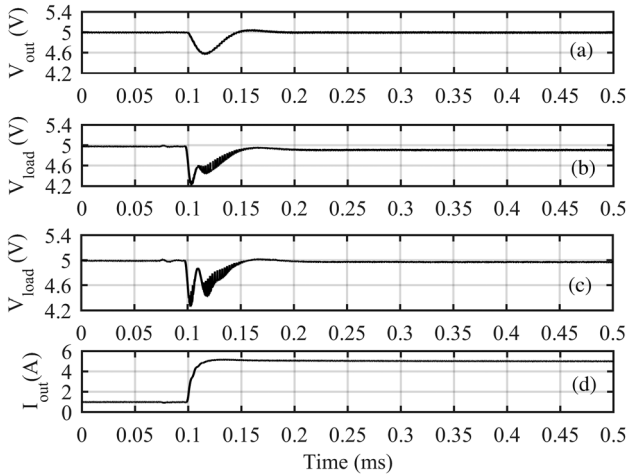


Figure 6.32 The time domain behavior of (a) the output voltage of the original converter, (b) the load–voltage response without remote sensing, (c) with the remote sensing, and (d) when a step change in the load current from 1 to 5 A is applied.

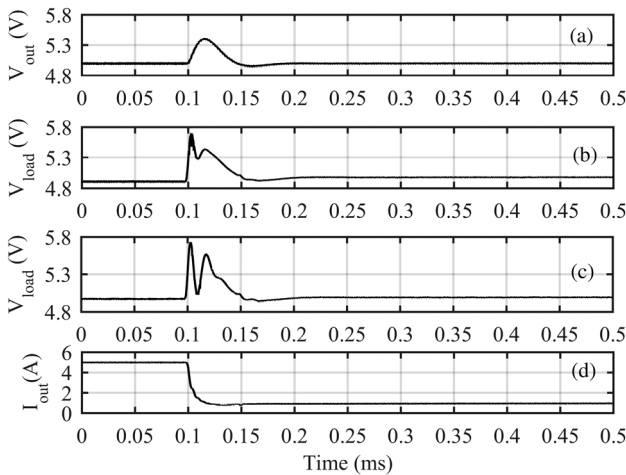


Figure 6.33 The time domain behavior of (a) the output voltage of the original converter, (b) the load–voltage response without remote sensing, (c) with the remote sensing, and (d) when a step change in the load current from 5 to 1 A is applied.

6.5 Simple Control Design Method

There are available very sophisticated methods for performing the control loop design in the contemporary control design textbooks such as Refs [45–49]. The use of robust control design methods yields usually very high-order controllers, which cannot be easily realized in practice, and therefore, the controller-order-reduction methods have to be utilized to get practically realizable controller. Usually, the method known as loop shaping yields quite satisfactory results and is

easy to apply. The use of software packages such as Matlab makes the design iterations and computing of different closed-loop transfer functions fast and easy. It is highly recommended to use authentic measured transfer functions of the converter as the dynamics description of the converter. The different algorithms and formulas we have given in Chapter 2 are equally valid when using the measured transfer functions or the predicted transfer functions given in Chapters 3–5 or their combination. When using measured and predicted (i.e., analytic) transfer functions at the same time, both of them have to be transferred into the same domain (i.e., complex numbers).

In order to succeed in the design, we have to first identify the true feedback loop gain, that is, all the elements affecting the dynamic behavior of the converter. In the nonisolated converters, this task is usually pretty easy but it should be, however, understood that the used PWM modulator may also contain different scaling factors, poles, and so on, which have to be taken into account. Therefore, the data sheet information shall be carefully studied, and the information transferred as elements in the loop if necessary. When using digital control, the sampling of the signals will necessitate adding a delay in the control loops, which usually corresponds to the sampling frequency (T_{SF}) as $e^{-sT_{SF}}$. The delay can be approximated by using the first-order *Padé* approximation in *Laplace* domain as

$$e^{-sT_{SF}} \approx \frac{1 - s(T_{SF}/2)}{1 + s(T_{SF}/2)}. \quad (6.20)$$

It should also be understood as Eq. (6.20) also indicates that the delay affects only the phase by decreasing it as $-\omega T_{SF}$ (cf. Section 2.5.8 for further information).

In case of transformer-isolated converters, the control loop usually also contains isolation by means of an optocoupler or some other medium. The optocoupler contains many dynamic elements such as current transfer ratio (CTR), a single pole, and delay, which shall be identified based on the data sheet provided by the manufacturer. Chapter 2 Section 2.5.7 provides more details on this topic.

If the control-related transfer function of the loop gain contains an RHP zero, then the control loop crossover frequency has to be less than the frequency of the zero. Usually, the practical limitation will materialize as proving sufficient gain margin in the control loop. If the control-related transfer function contains an RHP pole (i.e., the system is unstable at open loop), then the control loop crossover frequency has to be higher than the frequency of the pole. The location of poles has to be carefully considered when the operating point of converter varies for identifying the worst case operating point, where design has to be performed.

In the next sections, we will provide control design examples for a buck and boost converters under DDR and PCM controls in CCM. If the control design is performed in CCM and the converter enters into DCM, there will be no problems in its dynamic behavior. If the converter is designed to be operated only in DCM and the control design is performed accordingly, the unintentional operation of the converter in CCM would lead to instability. This means that the selection of the inductor for guaranteeing DCM operation has to be carried out with care.

6.5.1 DDR-Controlled Buck Converter

The relevant transfer functions and the operating point values for the DDR-controlled buck converter are given in Section 3.4.1. The corresponding power stage and the control system are given in Figure 6.14. The switching frequency is assumed to be 100 kHz and the peak-to-peak voltage (V_M) of the modulator ramp signal is assumed to be 3 V. The goal of the design is to produce a feedback loop gain having maximum crossover frequency of 20 kHz, PM of 50°, and GM of at least 6 dB. As stated earlier, the resonant nature of the converter necessitates to using PID-type controller in order to provide enough phase boost at the resonant frequency for the stable operation.

The output-voltage feedback loop gain can be given generally by

$$L(s) = G_a \cdot G_{cc} \cdot G_{co-o}, \quad (6.21)$$

where G_a denotes the modulator gain (i.e., $1/V_M$), G_{cc} the controller transfer function, and G_{co-o} the control-to-output-voltage transfer function. It is obvious that V_M and G_{co-o} are known and we have to choose the zeros, poles, and the gain of the transfer function such that the goals are met. We also target to minimize the settling time as discussed earlier in this chapter. Therefore, the loop gain can be given by

$$L(s) = \frac{1}{3} \cdot \frac{K_{cc}(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \cdot \frac{(V_{in} + V_D + (r_d - r_{ds1})I_o)(1 + sr_C C)}{s^2 LC + s(r_L + Dr_{ds1} + D'r_d + r_C)C + 1}. \quad (6.22)$$

According to G_{co-o} , its highest gain takes place at the highest input voltage. Therefore, we plot first the known part of the loop gain at the input voltage of 50 V, and design the controller in such a manner that the phase behavior yields PM of 50°. In order to achieve good transient settling behavior, the zeros of the controller are located at the resonant frequency. It is recommended in Ref. [24] that the first controller pole should be placed at the frequency of the zero caused by the output capacitor and its ESR (i.e., $\omega_{p1} = 1/r_C C$), and the second pole at the proximity of the switching frequency (i.e., $\omega_{p2} = (0.5 - 0.8) \cdot \omega_s$). In this case, the ESR zero locates at 15.3 kHz, and we have placed the first pole at $20 \cdot \omega_{z1}$, which is close to the ESR zero as recommended in Ref. [24]. In many applications, the output capacitor is of ceramic multilayer type having very small ESR, and therefore, the ESR-related zero can locate at too high frequency. Therefore, we have here adopted a little bit different approach for being able to meet the target PM. The second pole is placed at $\omega_s/4$, in order to achieve PM of 50° at 20 kHz. According to these principles, the Bode plots of $G_{co-o}/3$ and G_{cc} with $K_{cc} = 1$ can be given by as shown in Figure 6.34.

Figure 6.35 shows the Bode plot of the output voltage loop gain (i.e., dashed line) when the controller gain is unity (i.e., $K_{cc} = 1$). According to it, we need approximately 80 dB (i.e., $K_{cc} = 9660$) gain boost for achieving the crossover frequency of 20 kHz. The final loop gain is presented in Figure 6.35 as a solid line. The phase behavior shows that the phase margin is approximately 50°, which fulfills the goal. Figure 6.36 shows the effect of the varying input voltage on the loop gain: The reduction of the crossover frequency from 20 to 10 kHz when the

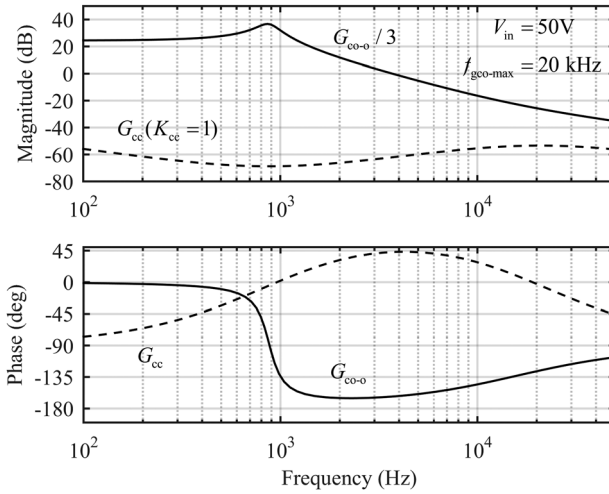


Figure 6.34 Bode plots of the control-to-output-voltage and controller transfer functions at the input voltage of 50 V.

input voltage is reduced from 50 to 20 V is expected due to the reduction of the gain of G_{co-o} from 40 to 26 dB at the low frequencies. The PM is also slightly improved from 50° to 63° that may slightly affect the settling process of the transient response.

Figure 6.37 shows the behavior of the closed-loop output impedance at the input voltage of 50 (solid line) and 20 V (dashed line). The corresponding closed-loop output impedance values at crossover frequencies are 48 and 58 m Ω . This means that the voltage dip of the load transient response at the input voltage of 20 V would be slightly higher than at 50 V.

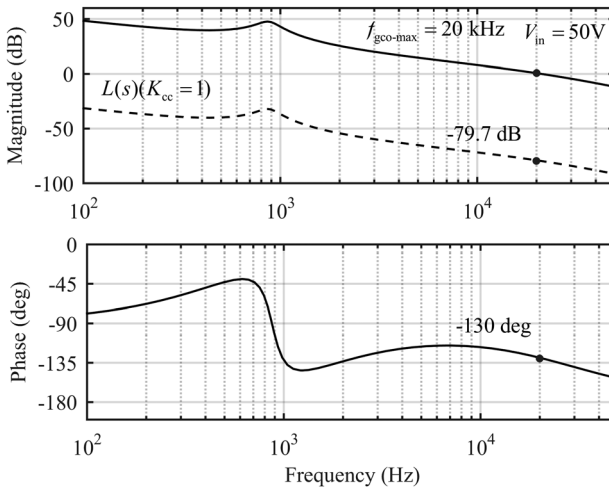


Figure 6.35 The output-voltage loop gains with $K = 1$ (dashed line) and $K_{cc} = 9660$ (solid line).

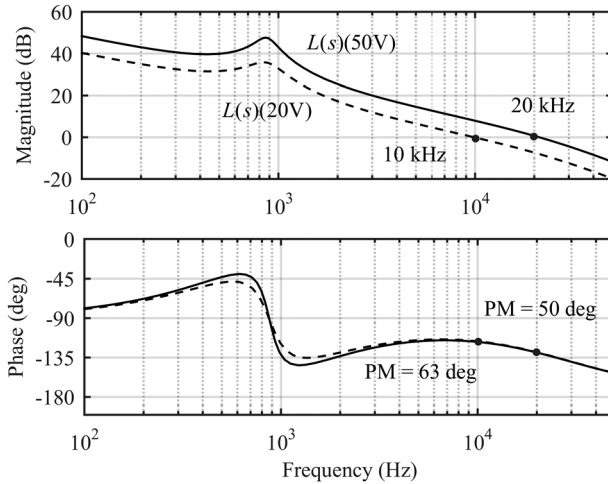


Figure 6.36 The output-voltage loop gains at the input voltage of 50 V (solid line) and 20 V (dashed line).

Figure 6.38 shows the output-voltage responses to the step change in the output current from 1 to 2.5 A at the input voltage of 50 and 20 V. According to the impedance values given in Figure 6.37, the predicted voltage dips would be 72 and 87 mV, respectively. According to the simulations, the corresponding values are 57 and 76 mV, which are reasonably close to each other but not exactly the same. The settling time of the converter at 50 V is slightly faster than at 20 V, as already discussed.

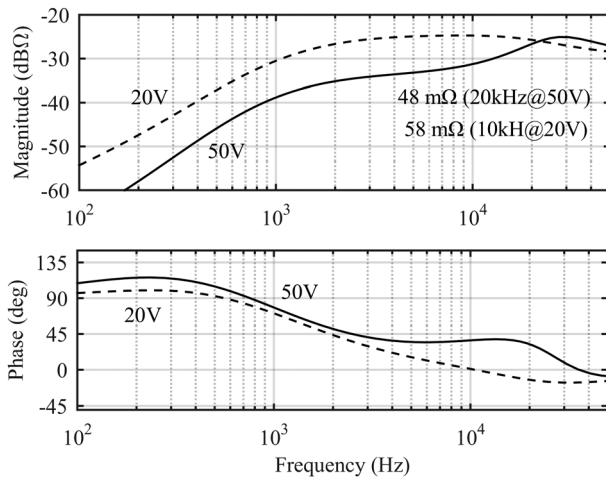


Figure 6.37 The closed-loop output impedances at the input voltage of 50 V (solid line) and 20 V (dashed line).

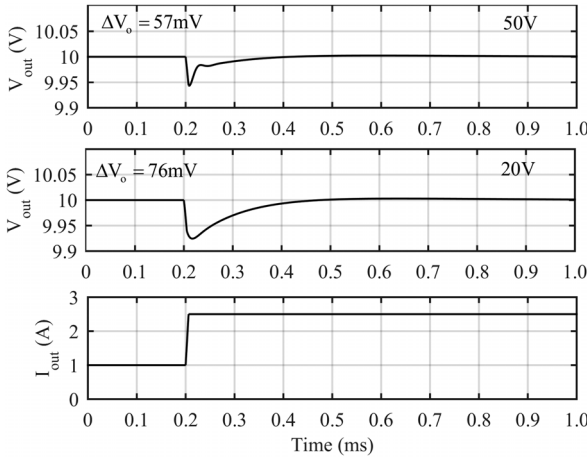


Figure 6.38 The output-voltage responses to a step change in the output current from 1 to 2.5 A with a slew rate of 0.25 A/ μ s.

6.5.2 PCM-Controlled Buck Converter

The relevant transfer functions and the operating point values for the PCM-controlled buck converter are given in Sections 4.2.8.1 and 3.4.1, respectively. The corresponding power stage and the control system are given in Figure 6.19. The switching frequency is assumed to be 100 kHz and the inductor current loop optimally compensated ($M_c = V_o/2L$). The goal of the design is to produce a feedback loop gain having maximum crossover frequency of 20 kHz, PM of 50°, and GM of at least 6 dB. As stated earlier, the resonant-free nature of the converter allows using PI-type controller.

The output-voltage feedback loop gain can be given generally by

$$L(s) = G_a \cdot G_{cc} \cdot G_{co-o}, \quad (6.23)$$

where G_a denotes the modulator gain, which usually equals $1/R_s$ but the PWM modulator may also include an additional scaling factor [23], G_{cc} the controller transfer function, and G_{co-o} the control-to-output-voltage transfer function. It is obvious that R_s and G_{co-o} are known and we have to choose the zero, pole, and the gain of the transfer function such that the goals are met. We also target to minimize the settling time as discussed earlier in this chapter. Therefore, the loop gain can be given by

$$L(s) = \frac{1}{75 \times 10^{-3}} \cdot \frac{K_{cc}(1 + s/\omega_{z1})}{s(1 + s/\omega_{p1})} \cdot \frac{F_m V_e (1 + sr_c C)}{s^2 LC + s(r_e + F_m V_e q_L)C + 1}, \quad (6.24)$$

where

$$\begin{aligned} r_e &= r_L + D r_{ds} + D' r_d + r_C, \\ V_e &= V_{in} + V_D + (r_d - r_{ds1}) I_o, \\ F_m &= 1 / \left[T_s \left(M_c + \frac{(D' - D) V_e}{2L} \right) \right], \\ q_L &= 1 + \frac{DD' T_s}{2L} (r_d - r_{ds1}). \end{aligned} \quad (6.25)$$

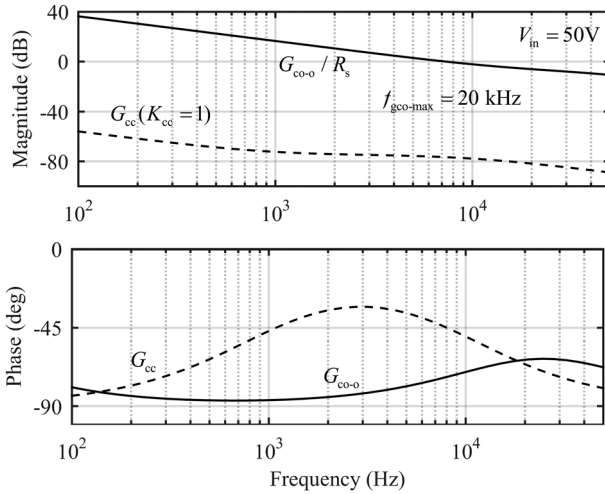


Figure 6.39 Bode plots of the control-to-output-voltage and controller transfer functions at the input voltage of 50 V.

According to G_{co-o} , its highest gain takes place at the highest input voltage. Therefore, we plot first the known part of the loop gain at the input voltage of 50 V, and design the controller in such a manner that the phase behavior yields PM of 50°. In order to achieve good transient settling behavior, the zero of the controller is located at the virtual resonant frequency. In case of PI control, the location of the controller pole is to be iterated in order to achieve PM of 50° at 20 kHz. We have placed the pole at $\omega_s/10$. According to these principles, the Bode plots of G_{co-o}/R_s and G_{cc} with $K_{cc} = 1$ can be given by as shown in Figure 6.39.

Figure 6.40 shows the Bode plot of the output voltage loop gain (i.e., dashed line) when the controller gain is unity (i.e., $K_{cc} = 1$). According to it, we need

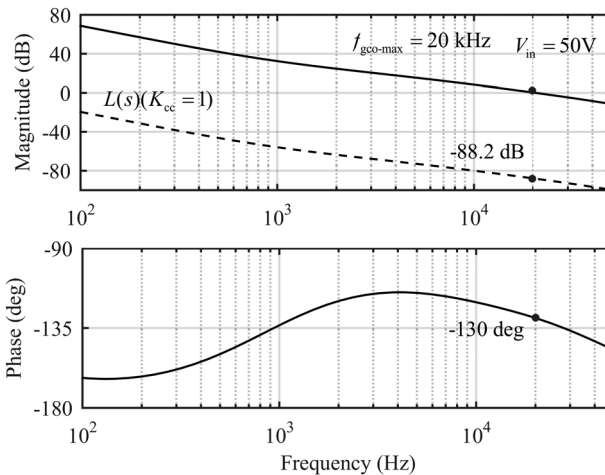


Figure 6.40 The output-voltage loop gains with $K_{cc} = 1$ (dashed line) and $K_{cc} = 25763$ (solid line).

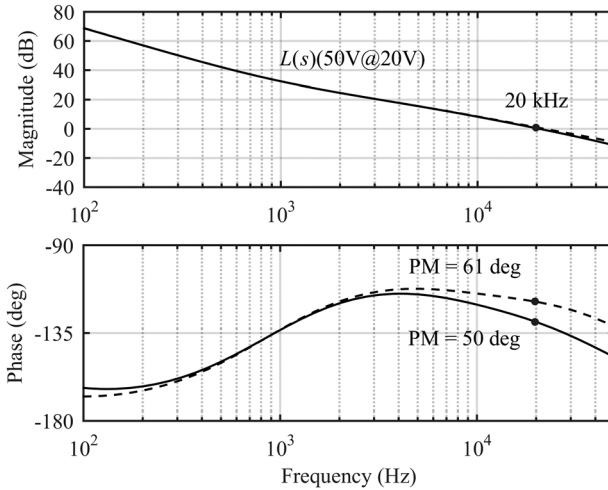


Figure 6.41 The output-voltage loop gains at the input voltage of 50 V (solid line) and 20 V (dashed line).

approximately 88 dB (i.e., $K_{cc} = 25763$) gain boost for achieving the crossover frequency of 20 kHz. The final loop gain is presented in Figure 6.40 as a solid line. The phase behavior shows that the phase margin is approximately 50° , which fulfills the goal. Figure 6.41 shows the effect of the varying input voltage on the loop gain: The crossover frequency will stay essentially intact at 20 kHz when the input voltage is reduced from 50 to 20 V. This kind of behavior is characteristic to PCM control, as discussed in Chapter 4. The PM is, however, slightly increased from 50° to 61° , which may slightly affect the settling process of the transient response.

Figure 6.42 shows the behavior of the closed-loop output impedance at the input voltage of 50 (solid line) and 20 V (dashed line). The corresponding

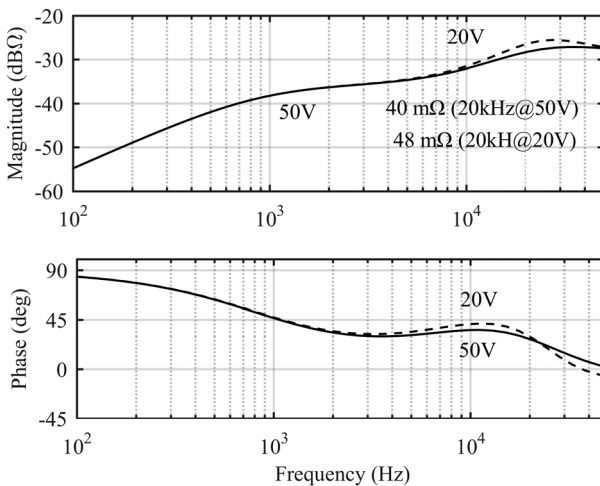


Figure 6.42 The closed-loop output impedances at the input voltage of 50 V (solid line) and 20 V (dashed line).

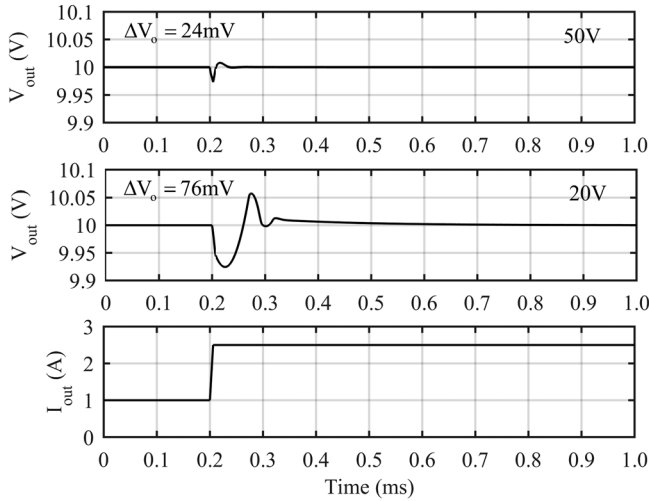


Figure 6.43 The output voltage responses to a step change in the output current from 1 to 2.5 A with a slew rate of $0.25 \text{ A}/\mu\text{s}$ by using the average model.

closed-loop output impedance values at crossover frequencies are 40 and 48 $\text{m}\Omega$. This means that the voltage dip of the load-transient response at the input voltage of 20 V would be slightly higher than at 50 V.

Figure 6.43 shows the output voltage responses to the step change in the output current from 1 to 2.5 A at the input voltage of 50 and 20 V, when the simulation is based on the average model. Figure 6.44 shows the same output-voltage responses, when the simulation is based on the switching mode. The averaged model-based responses show small overshoot in the responses, which does not exist in the switching model-based responses. The overshoot is the consequence

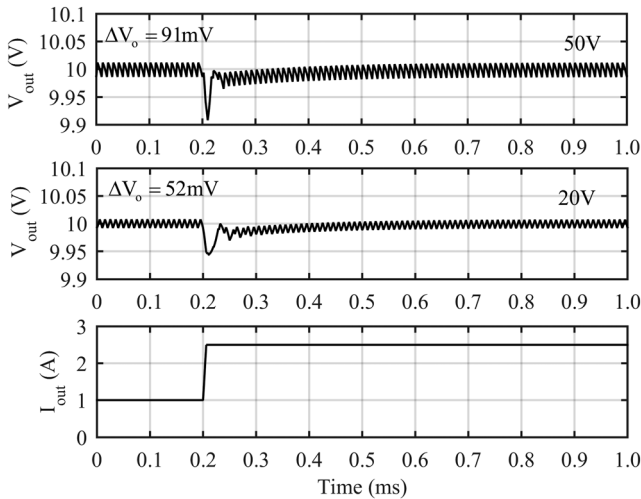


Figure 6.44 The output-voltage responses to a step change in the output current from 1 to 2.5 A with a slew rate of $0.25 \text{ A}/\mu\text{s}$ by using the switching model.

of the saturation of the averaged duty ratio to the mode limit value, which does not exist in the real converter in the beginning of the transient. According to the impedance values given in Figure 6.42, the predicted voltage dips would be 60 and 87 mV. According to the simulations, the corresponding values are 24 and 76 mV with average model and 91 and 52 mV with the switching model. The small-signal output impedance-based predictions are not very accurate at all. The settling time of the converter at 50 V is slightly faster than at 20 V, as already discussed.

Figure 6.45 shows the behavior of the inductor current and the duty ratio during 10 switching cycles in the beginning of the transient. It may be obvious that the converter enters into the subharmonic mode at the input voltage of 20 and 50 V but recovers to the normal operation. This phenomenon was discussed earlier in Chapter 4 and named as dynamic mode limit in contrast to the static mode limit. The inductor current was compensated by using the optimal compensation (i.e., $M_c = V_o/2L$), which ensures steady-state operation up to $D = 1$ but dynamically only to $0.5 \cdot (1 + V_o/V_{in})$. Figure 6.46 shows the behavior of the averaged inductor current based on the averaged model. The averaged inductor current behavior reflects quite closely the behavior of the average inductor current at the input voltage of 50 V (cf. Figure 6.45) but the average model fails to produce the correct inductor current behavior at the input voltage of 20 V due to the long-lasting second-harmonic mode operation. The averaged dynamic mode limit duty ratios are given in Figure 6.46, which explains the differences between the switched and average model responses very well. The real behavior of the PCM-controlled converter is difficult to be captured by using average model-based simulations.

Figure 6.47 shows the inductor current instantaneous and average behaviors when the inductor current loop is compensated by $M_c = V_{in}/2L$, which ensures second-harmonic-free operation of the converter up to 100% of duty ratio, as

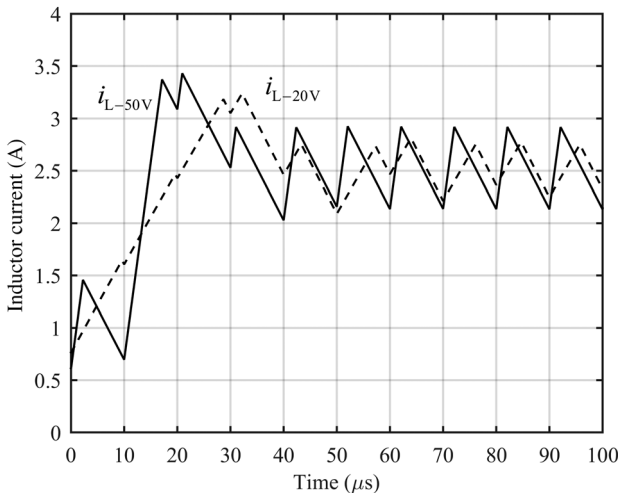


Figure 6.45 The behavior of the instantaneous inductor current during 10 switching cycles in the beginning of the transient based on the switching model.

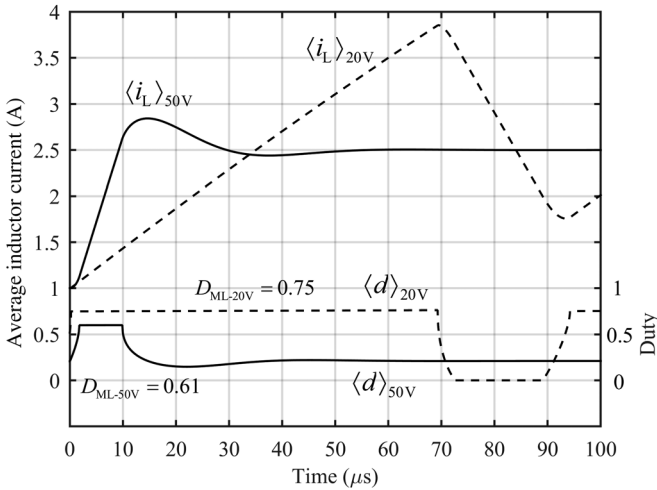


Figure 6.46 The behavior of the averaged inductor current during 10 switching cycles in the beginning of the transient based on the average model.

discussed in Section 4.2.8.1. Figure 6.47 clearly indicates that the compensation works, as we have claimed. Figure 6.47 also indicates that the average model predicts quite accurately the behavior of average inductor current due to lack of second-harmonic operation. In practice, the used compensation scheme does not work if it cannot follow the changes in the input voltage.

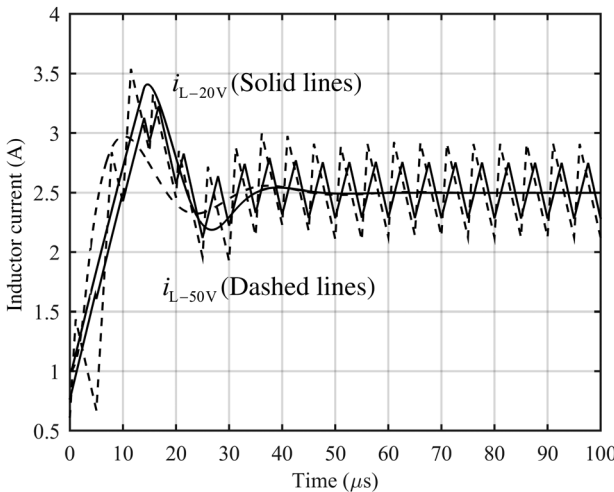


Figure 6.47 The behavior of the instantaneous and average inductor current during the 10 switching cycles in the beginning of the transient based on the switching and average models, when the inductor current loop is compensated based on $M_c = V_{in}/2L$.

6.5.3 DDR-Controlled Boost Converter

The relevant transfer functions and the operating point values for the DDR-controlled boost converter are given in Section 3.4.2. The corresponding power stage and the control system are given in Figure 6.48. The switching frequency is assumed to be 100 kHz and the peak-to-peak voltage (V_M) of the modulator ramp signal is assumed to be 3 V. It is well known that the boost converter incorporates an RHP zero in its output side control dynamics, which would limit the output voltage loop crossover frequency to the frequency of the RHP zero or even to lower frequency. Therefore, the goal of the design is to produce a feedback loop gain having as high as possible crossover frequency with an acceptable PM and GM of at least 6 dB. As stated earlier, the resonant nature of the converter necessitates to using PID-type controller in order to provide enough phase boost at the resonant frequency for the stable operation.

The output-voltage feedback loop gain can be given generally by

$$L(s) = G_a \cdot G_{cc} \cdot G_{co-o}, \tag{6.26}$$

where G_a denotes the modulator gain (i.e., $1/V_M$), G_{cc} the controller transfer function, and G_{co-o} the control-to-output-voltage transfer function. It is obvious that V_M and G_{co-o} are known and we have to choose the zeros, poles, and the gain of the transfer function such that the goals are met. We also target to minimize the settling time as discussed earlier in this chapter. Therefore, the loop gain can be given by

$$L(s) = \frac{1}{3} \cdot \frac{K_{cc}(1+s/\omega_{z1})(1+s/\omega_{z2})}{s(1+s/\omega_{p1})(1+s/\omega_{p2})} \cdot \frac{D'(V_o + V_D) + (r_L + r_{ds1} + D^2 r_C)I_L - sLI_L)(1 + sr_C C)}{s^2 LC + s(r_L + Dr_{ds1} + D'(r_d + r_C))C + D^2}. \tag{6.27}$$

According to the explicit form of G_{co-o} in Eq. (6.27), the RHP zero (i.e., $\omega_{z-RHP} \approx V_{in}/LI_L$) locates closest to the origin when the input voltage is at its

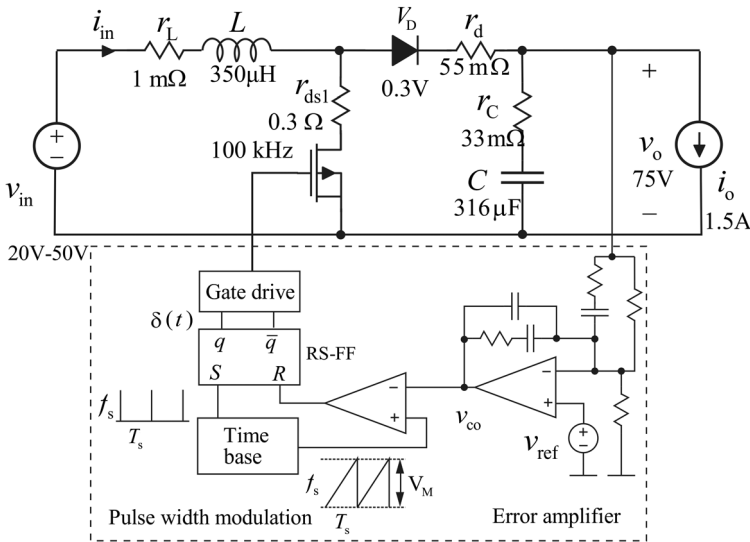


Figure 6.48 DDR-controlled boost converter and the corresponding control system.

minimum value, and the output load is at its highest value. In this case, the RHP zero locates at 1.37 kHz, which would be the absolute maximum output voltage loop crossover frequency. Therefore, the control design has to be performed at this operating point to ensure stable operation within the specified operation range. It should also be noticed that the resonant frequency would vary along the changes in the input voltage. Therefore, we plot first the known part of the loop gain at the input voltage of 20 V, and design the controller in such a manner that the loop gain behavior yields GM of at least 6 dB and an acceptable PM. It may be obvious that the load transient behavior would be quite poor whatever we do in the control design.

We have placed the controller zeros ($\omega_{z1,2}$) at the resonant frequency (i.e., 358 Hz) at the input voltage of 20 V. It is recommended in Ref. [24] that the first controller pole should be placed at the frequency of the zero caused by the output capacitor and its ESR (i.e., $\omega_{p1} = 1/r_C C$), and the second pole at the proximity of the switching frequency (i.e., $\omega_{p2} = (0.5 - 0.8) \cdot \omega_s$). In this case, the ESR zero locates at 15.3 kHz, and we have placed the first pole at $30 \cdot \omega_{z1}$ (i.e., 11 kHz), which is close to the ESR zero as recommended in Ref. [24]. The second pole is placed at $\omega_s/8$, in order to achieve PM of 50° at 20 kHz. According to these principles, the Bode plots of $G_{co-o}/3$ and G_{cc} with $K_{cc} = 1$ can be given by as shown in Figure 6.49.

Figure 6.50 shows the Bode plot of the output-voltage loop gain (i.e., dashed line) when the controller gain is unity (i.e., $K_{cc} = 1$). According to it, we need approximately 28 dB (i.e., $K_{cc} = 24.55$) gain boost for achieving the crossover frequency of 421 Hz, which ensures PM of 50° and GM of 8 dB as can be confirmed based on the final loop gain (solid line).

Figure 6.51 shows the effect of the varying input voltage on the loop gain: The change of resonant frequency along the changes in the input voltage is clearly visible. In addition, the damping of the resonant frequency is very high at the

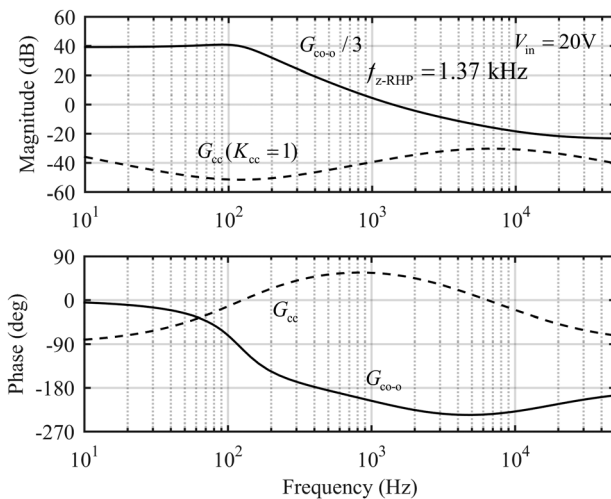


Figure 6.49 Bode plots of the control-to-output-voltage and controller transfer functions at the input voltage of 20 V.

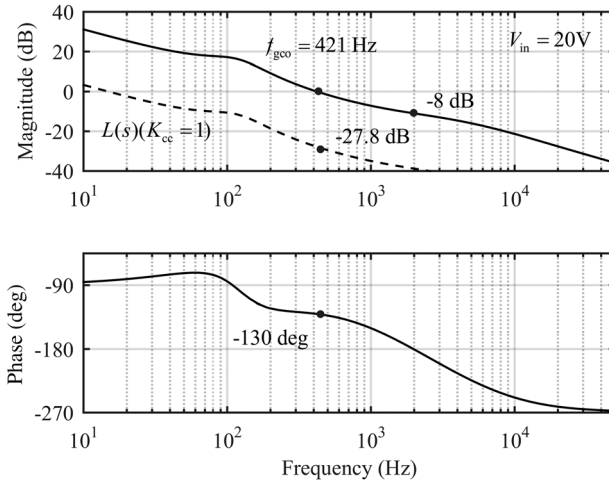


Figure 6.50 The output-voltage loop gains with $K_{cc} = 1$ (dashed line) and $K_{cc} = 24.55$ (solid line).

input voltage of 20 V and decreases clearly when the input voltage increases. The increase in the crossover frequency is clearly visible when the input voltage increases.

Figure 6.52 shows the behavior of the closed-loop output impedance at the input voltage of 20 V (solid line) and 50 V (dashed line). The corresponding closed-loop output impedance values at crossover frequencies are 1.54 and 0.53 Ω . These impedance values would imply that the expected load transient-induced dips would be rather high as shown in Figure 6.53.

Figure 6.53 shows the output voltage responses to the step change in the output current from 0.2 to 1.5 A at the input voltage of 50 and 20 V, when the simulation

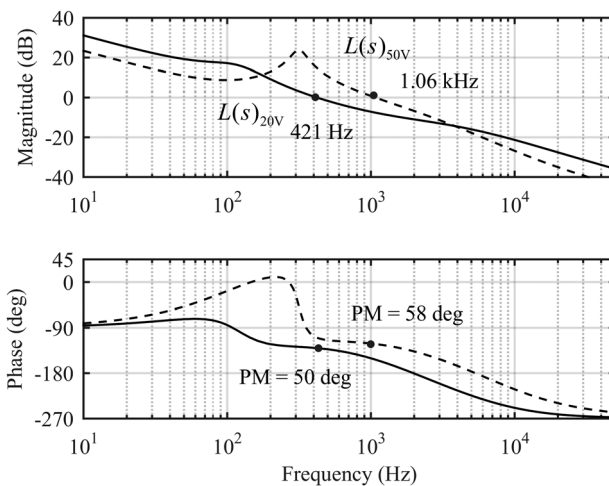


Figure 6.51 The output-voltage loop gains at the input voltage of 50 V (solid line) and 20 V (dashed line).

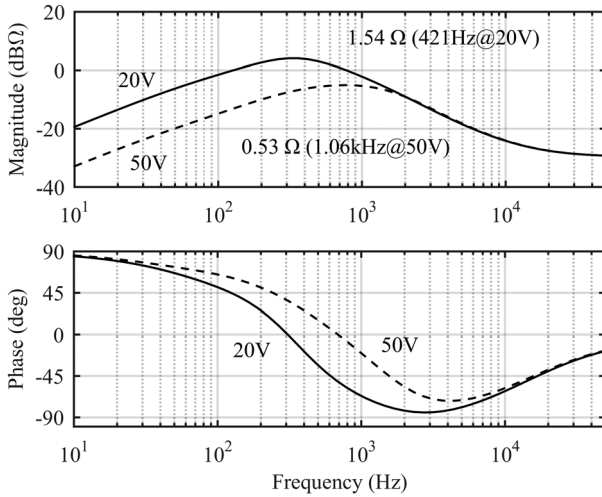


Figure 6.52 The closed-loop output impedances at the input voltage of 20 V (solid line) and 50 V (dashed line).

is based on the average model. According to the impedance values given in Figure 6.51, the predicted voltage dips would be 0.69 and 2.0 V. According to the simulations, the corresponding values are 0.56 and 1.37 V. The small-signal output impedance-based predictions are not very accurate. The output-voltage transients in Figure 6.53 clearly shows that it is not possible to achieve fast settling transient behavior and low voltage dips when the control system contains an RHP zero, which locates at rather low frequencies. Therefore, the nonminimum phase converters are usually designed to operate in DCM, where the RHP zero locates at much higher frequencies, as discussed in Chapter 3.

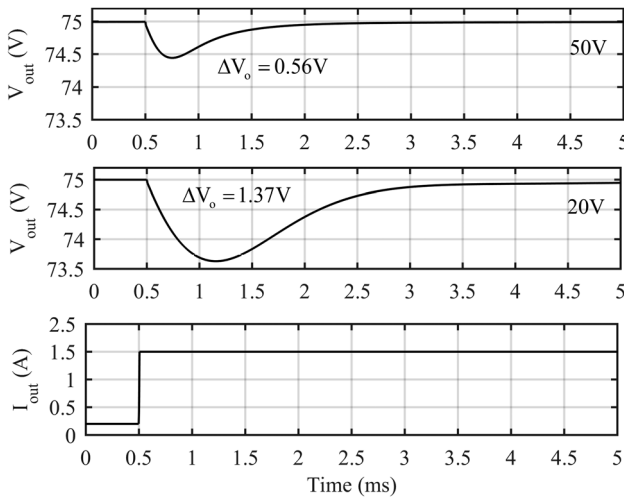


Figure 6.53 The output-voltage responses to a step change in the output current from 0.2 to 1.5 A with a slew rate of 0.25 A/ μ s by using the average model.

6.5.4 PCM-Controlled Boost Converter

The relevant transfer functions and the operating point values for the PCM-controlled boost converter are given in Sections 4.2.8.2 and 3.4.2. The corresponding power stage and the control system are given in Figure 6.54. The switching frequency is assumed to be 100 kHz and the inductor current loop compensated ($M_c = V_o/2L$) for ensuring the duty ratio range of 100% both for static and dynamic operations. It is well known that the boost converter incorporates an RHP zero in its output side control dynamics, which would limit the output voltage loop crossover frequency to the frequency of the RHP zero or even to lower frequency. The PCM control does not remove the effect of the RHP zero even if claimed, for example, in Ref. [50]. Under PCM control, the limiting factor would be the high-frequency behavior of the loop magnitude (i.e., to obtain adequate gain margin). Therefore, the goal of the design is to produce a feedback loop having as high as possible crossover frequency with an acceptable PM and GM of at least 6 dB. As stated earlier, the resonant-free nature of the converter allows using PI-type controller.

The output-voltage feedback loop gain can be given generally by

$$L(s) = G_a \cdot G_{cc} \cdot G_{co-o}, \quad (6.28)$$

where G_a denotes the modulator gain, which usually equals $1/R_s$ but the PWM modulator may also include an additional scaling factor [23], G_{cc} the controller transfer function, and G_{co-o} the control-to-output-voltage transfer function. It is obvious that R_s and G_{co-o} are known and we have to choose the zero, pole, and the gain of the transfer function such that the goals are met. We also target to minimize the settling time as discussed earlier in this chapter. Therefore, the loop

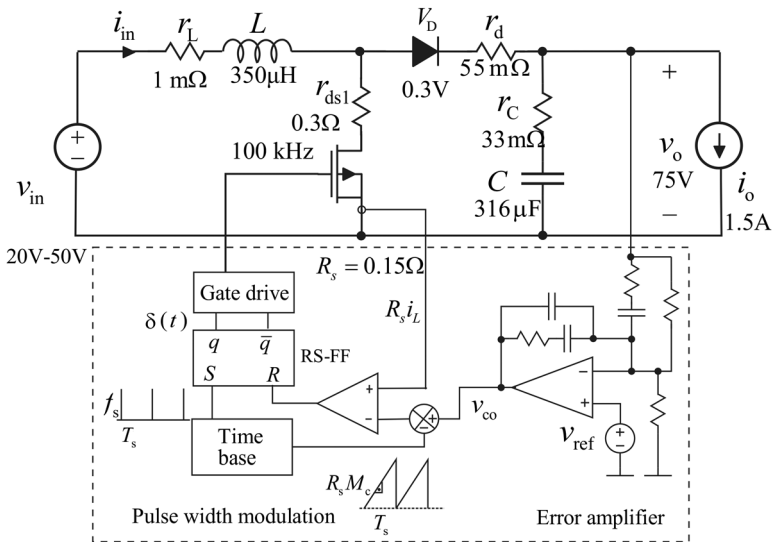


Figure 6.54 PCM-controlled boost converter and the corresponding control system.

gain can be given by

$$L(s) = \frac{1}{0.15} \cdot \frac{K_{cc}(1+s/\omega_{z1})}{s(1+s/\omega_{p1})} \cdot \left[\left(\frac{F_m(DV_e - I_L r_e)}{LC} \left(1 - s \frac{LI_L}{DV_e - I_L r_e} \right) (1 + s r_C C) \right) / \Delta \right], \quad (6.29)$$

where

$$\begin{aligned} \Delta &= s^2 + s \cdot \left(\frac{r_e + F_m V_e q_L}{L} - \frac{F_m I_L q_C}{C} \right) + \frac{D'^2 + D' F_m (V_e q_C + I_L q_L) - F_m I_L q_C r_e}{LC}, \\ r_e &= r_L + D r_{ds1} + D' r_d + D' r_C, \\ V_e &= V_o + V_D + (r_d - r_{ds1} + D r_C) \frac{I_o}{D}, \\ F_m &= 1 / \left[T_s \left(M_c + \frac{(D' - D) V_e}{2L} \right) \right], \\ q_L &= 1 + \frac{DD' T_s}{2L} (r_d + r_C - r_{ds1}), \\ q_C &= \frac{DD' T_s}{2L}. \end{aligned} \quad (6.30)$$

According to the explicit form of G_{co-o} in Eq. (6.29), the RHP zero (i.e., $\omega_{z-RHP} \approx V_{in}/LI_L$) locates closest to the origin, when the input voltage is at its minimum value, and the output load is at its maximum value. In this case, the RHP zero locates at 1.37 kHz, which would be the absolute maximum output voltage loop crossover frequency. Therefore, the control design has to be performed at this operating point to ensure stable operation within the specified operation range. Therefore, we plot first the known part of the loop gain at the input voltage of 20 V, and design the controller in such a manner that the loop gain behavior yields GM of at least 6 dB and an acceptable PM. It may be obvious that the load transient behavior would be quite poor whatever we do in the control design.

We have placed the controller zero (ω_{z1}) at 2/3 of the imaginary resonant frequency (i.e., $\omega_{res} = D'/\sqrt{LC}$, that is, 87 Hz) at the input voltage of 20 V. The controller pole is placed at $\omega_s/8$ (i.e., 12.5 kHz) to obtain PM of 50° at 671 Hz. According to these principles, the Bode plots of G_{co-o}/R_s and G_{cc} with $K_{cc} = 1$ can be given by as shown in Figure 6.55. The controller zero can also be placed at the imaginary resonant frequency but the PM would be then slightly reduced.

Figure 6.56 shows the Bode plot of the output voltage loop gain (i.e., dashed line) when the controller gain is unity (i.e., $K_{cc} = 1$). According to it, we need approximately 58 dB (i.e., $K_{cc} = 750$) gain boost for achieving the crossover frequency of 671 Hz, which ensures PM of 50° and GM of 7 dB as can be confirmed based on the final loop gain (solid line). As can be seen in Figure 6.55, the high-frequency magnitude behavior of the loop gain actually limits the crossover frequency to approximately half the RHP zero frequency. The obtained crossover frequency is only slightly higher than the corresponding crossover frequency of the DDR-controlled converter (cf. Figure 6.49).

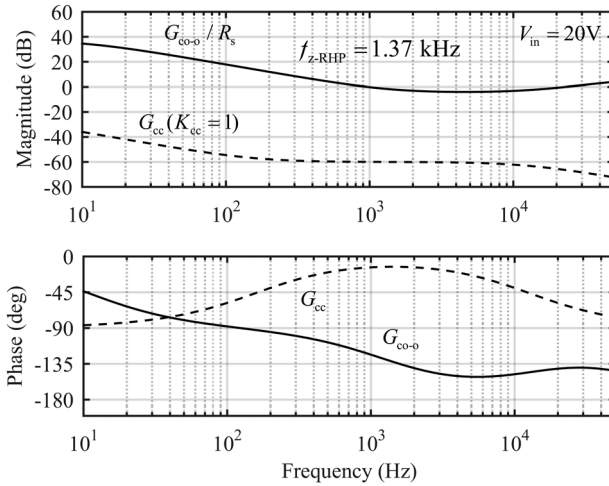


Figure 6.55 Bode plots of the control-to-output-voltage and controller transfer functions at the input voltage of 20 V.

Figure 6.57 shows the effect of the varying input voltage on the loop gain: The output-voltage loop gain does not stay constant as in the PCM-controlled buck converter (cf. Figure 6.41), but behaves similarly as the DDR-controlled boost converter having an increase in the loop crossover frequency and PM (cf. Figure 6.51). The varying input voltage affects the phase margin much more than in the DDR-controlled converter.

Figure 6.58 shows the behavior of the closed-loop output impedance at the input voltage of 20 (solid line) and 50 V (dashed line). The corresponding closed-loop output impedance values at crossover frequencies are 0.9 and 0.26 Ω , which

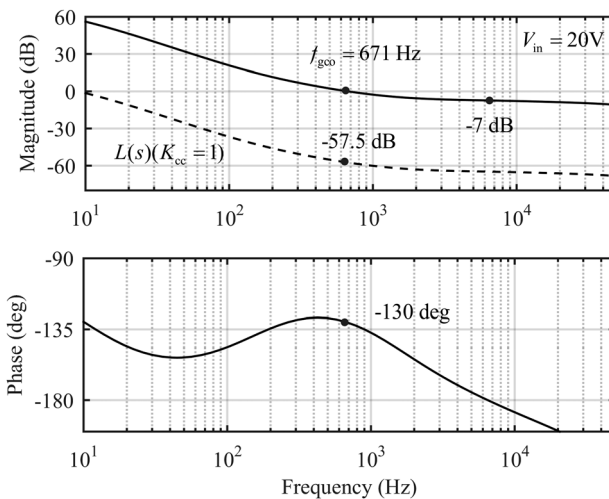


Figure 6.56 The output-voltage loop gains with $K_{cc} = 1$ (dashed line) and $K_{cc} = 750$ (solid line).

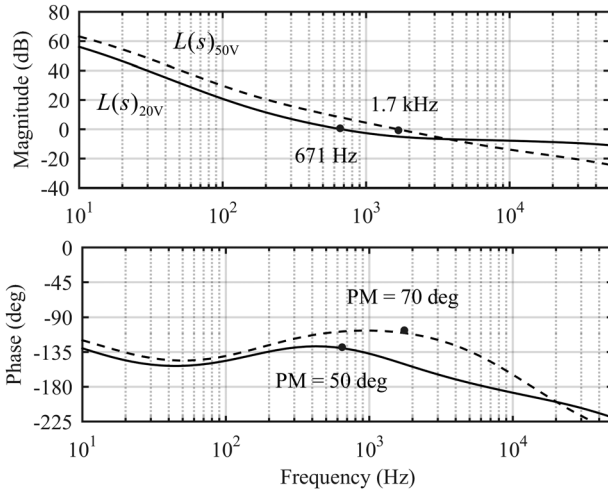


Figure 6.57 The output-voltage loop gains at the input voltage of 50 V (solid line) and 20 V (dashed line).

are much smaller than the values of the DDR-controlled converter (cf. Figure 6.51). These impedance values would imply that the expected load transient-induced dips would be lower than the output voltage dips in the DDR-controlled converter (cf. Figure 6.53).

Figure 6.59 shows the output-voltage responses to the step change in the output current from 0.2 to 1.5 A at the input voltage of 50 and 20 V, when the simulation is based on the average model. According to the impedance values given in Figure 6.58, the predicted voltage dips would be 0.34 and 1.2 V.

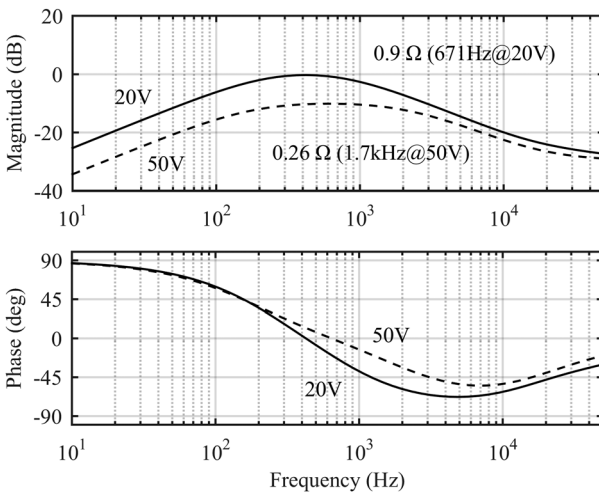


Figure 6.58 The closed-loop output impedances at the input voltage of 20 V (solid line) and 50 V (dashed line).

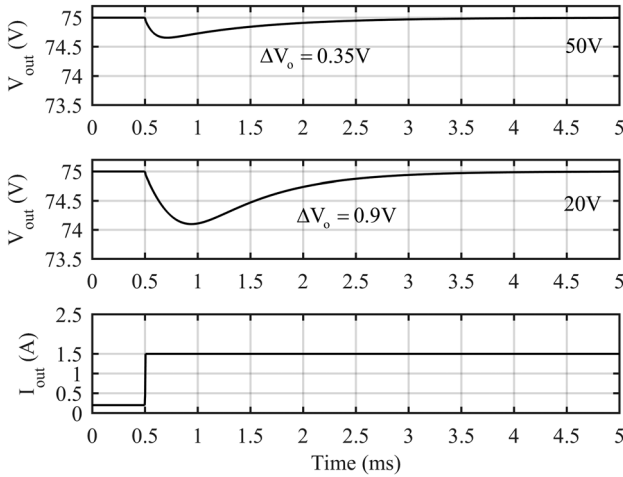


Figure 6.59 The output-voltage responses to a step change in the output current from 0.2 to 1.5 A with a slew rate of 0.25 A/ μ s by using the average model.

According to the simulations, the corresponding values are 0.35 and 0.9 V, respectively, which match quite well to each other. The settling times of the transients are quite similar to the settling times of the DDR-controlled converter. The output voltage transients in Figure 6.58 clearly shows that it is not possible to achieve fast settling transient behavior and low-voltage dips when the control system contains an RHP zero, which locates at rather low frequencies.

Figure 6.60 shows the behavior of instantaneous inductor current (i.e., based on switching model) and the average inductor current (i.e., based on the average model) during the 21st switching cycle in the beginning of the transient. The

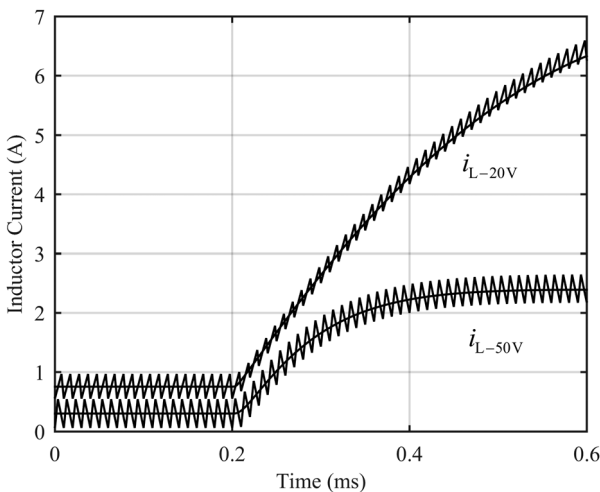


Figure 6.60 The behavior of the instantaneous inductor current during the 20 switching cycles in the beginning of the transient based on the switching and average models.

figure shows that the converter does not enter into the second-harmonic mode as the PCM-controlled buck converter with the optimal compensation will do in the beginning of the transient (cf. Figure 6.45). The reason for this kind of behavior is that the used compensation (i.e., $M_c = V_o/2L$) ensures static and dynamic second-harmonic-free operation up to the 100% of duty ratio, as discussed in Section 4.2.8.2. Figure 6.60 also shows (cf. the ripple-free lines in the response) that the average model will describe the average dynamics of the converter quite well. There is visible light in accuracy in the 20 V response only, which can be noticed when the average response does not follow exactly the midline of the peak-to-peak inductor current, as it does in the 50 V response.

6.6 PCM-Controlled Superbuck Converter: Experimental Examples

6.6.1 Introduction

The dynamic models of the PCM-controlled superbuck converter without [51] and with coupled inductors [52] are given in Section 4.2.8.4. The experimental power stages are given in Figures 6.61 and 6.62 with the relevant component definitions and the operating range. As discussed in Section 3.4.4, the superbuck

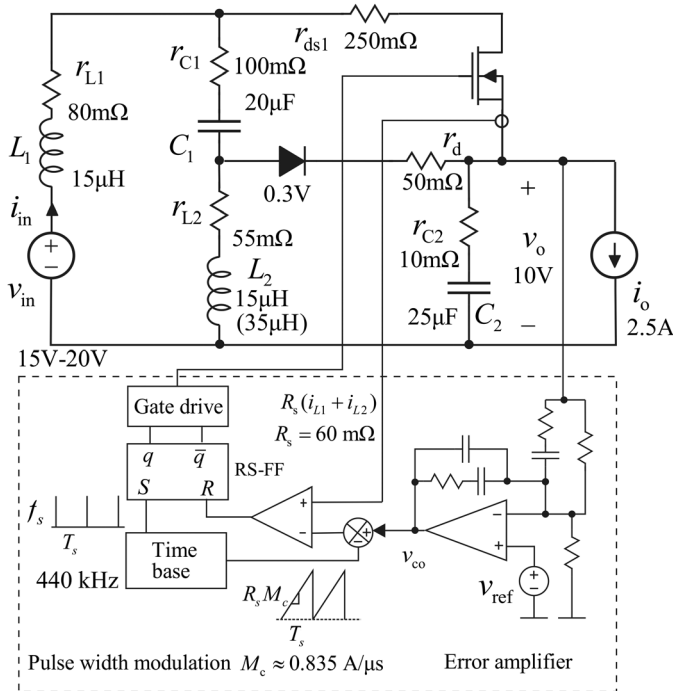


Figure 6.61 The power stage and component values of the PCM-controlled discrete-inductor superbuck converter.

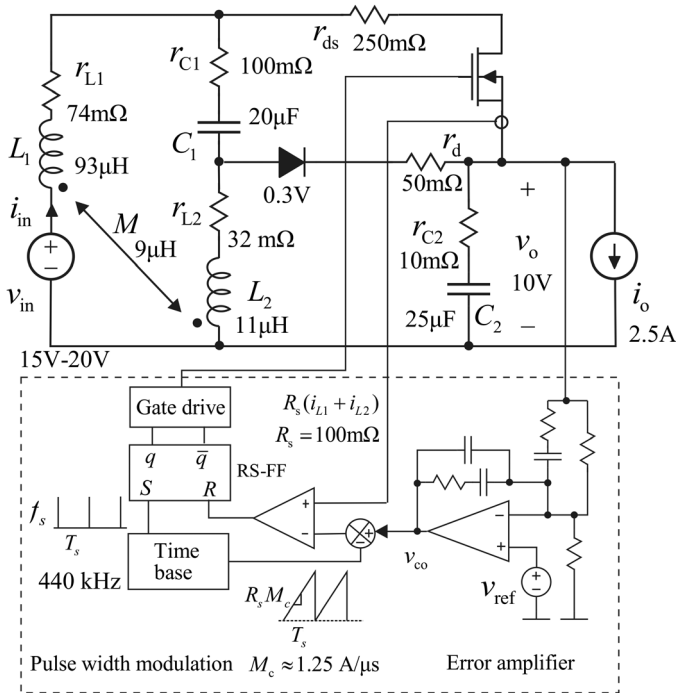


Figure 6.62 The power stage and component values of the PCM-controlled coupled-inductor superbuck converter.

converter incorporates an RHP zero in its output dynamics but it can be effectively removed by designing the ratio of the inductors properly. The value of the inductor L_2 given in parenthesis corresponds to the theoretical value, which can be obtained by means of the design algorithm $L_2 D'_{\max} - L_1 D_{\max} \approx 0$ without considering the losses for $D_{\max} = 0.7$. The effect of the losses was, in this case, such that equal inductance values could be used without the RHP zero.

If extremely low ripple of one of the inductor currents is desirable, then it can be implemented by coupling the inductors in a certain manner as discussed in detail in Chapter 3. In this particular case, the ripple of input current of the converter is minimized by designing the coupling of the inductors accordingly. The design outcome is that the values of the inductors cannot be anymore designed to remove the appearance of the RHP zero, but actually the design would boost the appearing. As a consequence, the converter transient dynamics would be extremely poor even if the switching frequency were rather high.

6.6.2 Discrete-Inductor Superbuck

Figure 6.63 shows the measured output-voltage loop gains at the input voltage of 15 and 20 V, which are effectively identical having crossover frequency approximately at 58 kHz and PM of 68° . This kind of phenomenon is typical to the PCM-

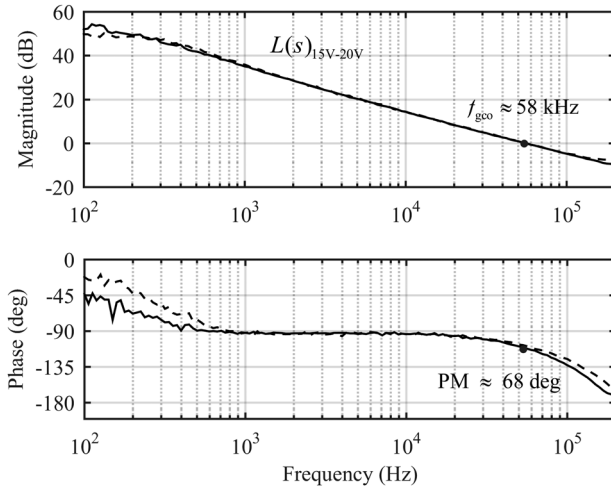


Figure 6.63 The measured output-voltage loop gains at the input voltage of 15 and 20 V.

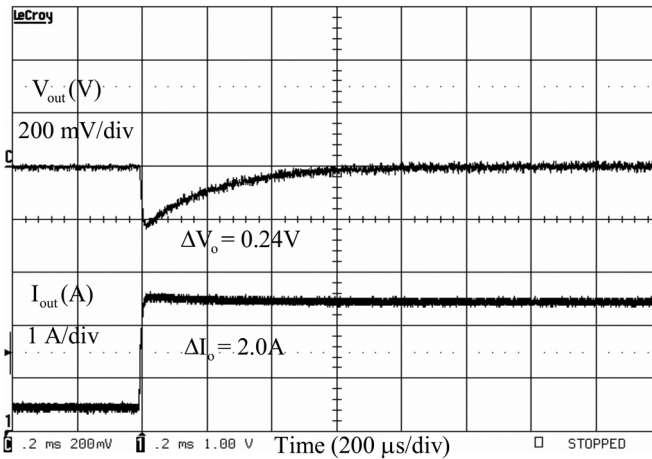


Figure 6.64 The output-voltage response to a step change in the output current from 0.5 to 2.5 A.

controlled buck-type converters, as clearly demonstrated earlier in Figure 6.41. The figure also shows that the RHP zero does not appear into the control dynamics within the specified operational range. Figure 6.64 shows the output-voltage response to a step change in the output current from 0.5 to 2.5 A.

6.6.3 Coupled-Inductor Superbuck

Figure 6.65 shows the measured output voltage loop gains at the input voltage of 15 and 20 V. The output-voltage loop magnitudes are effectively identical but the

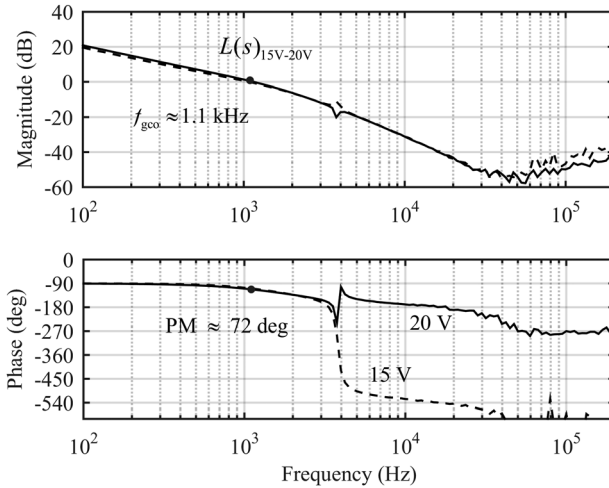


Figure 6.65 The measured output-voltage loop gains at the input voltage of 15 and 20V.

phase behavior indicates that the RHP zero appears into the control dynamics when the input voltage decreases. As a consequence, the loop crossover frequency has been designed to be approximately 1.1 kHz with PM of 72° . Figure 6.66 shows the output-voltage response to a step change in the output current from 1.0 to 2.4 A. The transient behavior is rather poor as could be expected when the RHP zero locates at the low frequencies (i.e., 4 kHz). Figure 6.67 shows the measured inductor currents, which clearly indicates that the coupled-inductor technique can be used to minimize one of the inductor currents but the penalty, in this case, is the extremely poor transient performance.

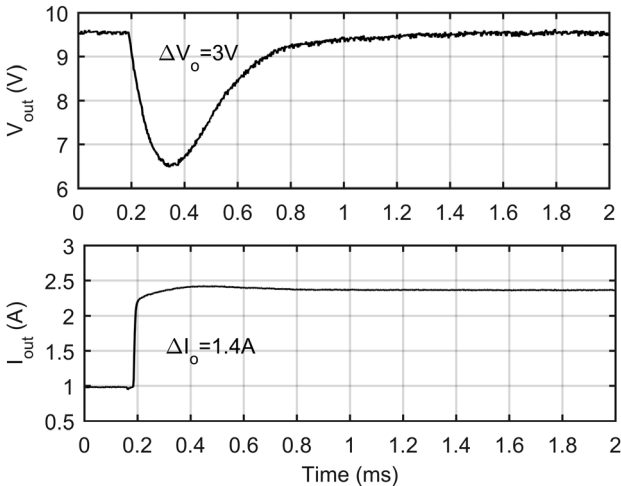


Figure 6.66 The output-voltage response to a step change in the output current from 1 to 2.4 A.

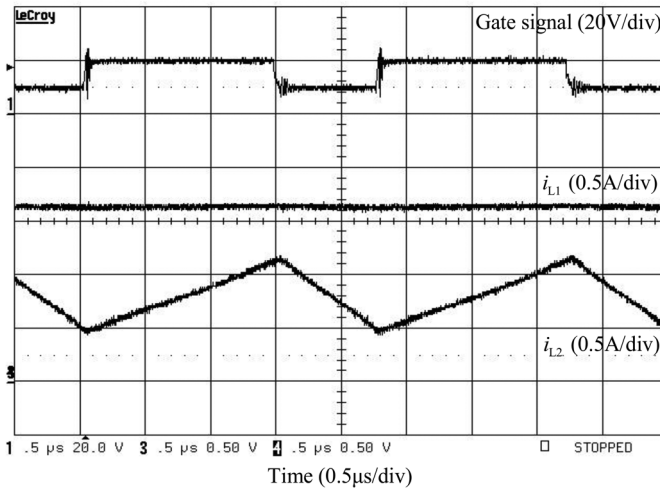


Figure 6.67 The measured inductor currents.

6.7 Concluding Remarks

Chapter 10 of the book gives more information on the effect of feedback loop crossover frequency and phase margin on the dynamics of the converters. It will show that the undamped natural frequency (ω_n) and the damping factor (ζ) can be explicitly computed based on the crossover frequency and phase margin (PM). As a summary, it can be stated that the system time constant $\tau \approx 1/\omega_n \zeta$. The large PM is reflected as high damping, which will make the transient responses more sluggish compared to the low PM.

References

- 1 Lidow, A., Kinzinger, D., Sheridan, G., and Tam, D. (2001) The semiconductor roadmap for power management in the new millennium. *Proc. IEEE*, **89** (6), 803–812.
- 2 Lidow, A. and Sheridan, G. (2003) Defining future for microprocessor power delivery. Proceedings of the APEC, pp. 3–9.
- 3 Miftakhutdinov, R. (2001) An analytical comparison of alternative control techniques for powering next generation microprocessors. Proceedings of the Power Supply Design Seminar (SEM 1400), Texas Instruments, Dallas, TX, USA, pp. 1-1–1-39.
- 4 Huang, H. (2005) Coordination of design issues in the intermediate bus architecture. Proceedings of the IEEE APEC, pp. 169–175.
- 5 Suntio, T. and Glad, A. (1990) The batteries as principal component in DC UPS systems. Proceedings of the IEEE INTELEC, pp. 400–411.

- 6 Suntio, T., Gadoura, I., Lempinen, J., and Zenger, K. (2000) Practical design issues of multiloop controller for a telecom rectifier. Proceedings of the IEEE INTELEC, pp. 197–201.
- 7 Venable, D. (1997) Testing power supply for stability. Technical report 1, Venable Industries, Inc., Austin, TX, USA (available at www.venable.biz).
- 8 Venable, D. (1997) Optimum feedback amplifier design for control systems. Technical report 3, Venable Industries, Inc., Austin, TX, USA (available at www.venable.biz).
- 9 Jacobs, M.E. (2006) Optimal feedback control of switch-mode power converters. Proceedings of the IEEE INTELEC, pp. 508–517.
- 10 Dixon, L. (1994) Switching power supply control loop design. Proceedings of the Power Supply Design Seminar (SEM-1000), Unitrode Corp., Merrimack, NH, USA, pp. C1-1–C1-10.
- 11 Dixon, L. (1996) Control loop cookbook. Proceedings of the Power Supply Design Seminar (SEM-1100), Unitrode Corp., Merrimack, NH, USA, pp. 5-1–5-26.
- 12 Mitchell, D. and Mammano, R. (2001) Designing stable control loops. Proceedings of the Power Supply Design Seminar (SEM-1400), Texas Instruments, Dallas, TX, USA, pp. 5-1–5-30.
- 13 Sun, J. (2003) Control design considerations for voltage regulator modules. Proceedings of the IEEE INTELEC, pp. 84–91.
- 14 Tuttle, W.H. (1984) Relating converter transient response characteristics to feedback loop control design. Proceedings of the 11th National Power Conversion Conference, pp. 10-1–10-12.
- 15 Basio, J.C. and Matos, S.R. (2002) Design of PI and PID controllers with transient performance specifications. *IEEE Trans. Edu.*, **45** (4), 364–370.
- 16 Meyer, E., Zhang, Z., and Liu, Y.-F. (2008) An optimal control method for a buck converters using a practical capacitor charge balance. *IEEE Trans. Power Electron.*, **23** (4), 1802–1812.
- 17 De Nardo, A., Femia, N., Petrone, G., and Spagnuolo, G. (2010) Optimal buck converter output filter design for point-of-load applications. *IEEE Trans. Ind. Electron.*, **57** (4), 1330–1341.
- 18 Cantillo, A., De Nardo, A., Femia, N., and Zamboni, W. (2011) A unified practical design method for capacitors of switching converters. *IEEE Trans. Ind. Electron.*, **58** (8), 3521–3536.
- 19 Di Lorenzo del Casale, M., Femia, N., Lamberti, P., and Mainardi, V. (2004) Selection of optimal closed-loop controllers for DC–DC voltage regulators based on nominal and tolerance design. *IEEE Trans. Ind. Electron.*, **51** (4), 840–849.
- 20 Redl, R., Erisman, B.P., and Zansky, Z. (1998) Optimizing the load transient response of the buck converter. Proceedings of the IEEE APEC, pp. 170–176.
- 21 Choi, B. (1997) Step load response of a current-mode-controlled DC-to-DC converter. *IEEE Trans. Aerosp. Electron. Syst.*, **33** (4), 1115–1121.
- 22 Erickson, R.W. and Maksimovic, D. (2001) *Fundamentals of Power Electronics*, 2nd edn, Kluwer Academic Publishers, Norwell, MA.
- 23 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters – Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.

- 24 Choi, B. (2013) *Pulsewidth Modulated DC-to-DC Power Conversion – Circuits, Dynamics, and Control*, IEEE Press John Wiley & Sons, Inc., Hoboken, NJ, USA.
- 25 Kazimierczuk, M.K. (2008) *Pulse-width Modulated DC–DC Power Converters*, John Wiley & Sons, Ltd., Chichester, UK.
- 26 Krein, P.T. (2015) *Elements of Power Electronics*, 2nd edn, Oxford University Press, Oxford, NY.
- 27 Roinila, T., Hankaniemi, M., Suntio, T., Sippola, M., and Vilkkö, M. (2007) Dynamical profile of a switched-mode converter – reality or imagination. *Proceedings of the IEEE INTELEC*, pp. 420–427.
- 28 Vesti, S., Suntio, T., Oliver, J.A., Prieto, R., and Cobos, J.A. (2013) Effect of control method on impedance-based interactions in a buck converter. *IEEE Trans. Power Electron.*, **28** (11), 5311–5322.
- 29 Suntio, T., Hankaniemi, M., and Karppanen, M. (2006) Analysing the dynamics of regulated converters. *IEE Proc. Electric Power Appl.*, **153** (6), 905–910.
- 30 Hankaniemi, M., Karppanen, M., and Suntio, T. (2006) Load imposed instability and performance degradation in a regulated converter. *IEE Proc. Electric Power Appl.*, **153** (6), 781–786.
- 31 Suntio, T. and Karppanen, M. (2009) The short-circuit input impedance as a main source of input-filter interactions in a regulated converter. *Eur. Power Electron. Drives J.*, **19** (3), 31–40.
- 32 Karppanen, M., Sippola, M., and Suntio, T. (2007) Impact of remote sensing on converter stability and performance. *Proceedings of the EPE*, pp. 1–10.
- 33 Karppanen, M., Suntio, T., and Sippola, M. (2007) Impact of output-voltage remote sensing on converter dynamics. *Int. Rev. Electr. Eng.*, **2** (2), 196–202.
- 34 Liang, X., Wong, H., Uan-Zo-li, A., and Zhou, X. (2015) Evaluation of a new remote sensing method for onboard voltage regulator in computing system. *IEEE Trans. Power Electron.*, **30** (6), 3057–3067.
- 35 Tepsa, T. and Suntio, T. (2003) Adjustable shunt regulator based control. *IEEE Power Electron. Lett.*, **1** (4), 93–96.
- 36 Irving, B.T. and Jovanovic, M.M. (2002) Analysis and design of self-oscillating flyback converter. *Proceedings of the IEEE APEC*, pp. 897–903.
- 37 Suntio, T. and Kivimäki, J. (2014) Physical insight into the factors affecting the load transient response of a buck converter. *Proceedings of the EPE-ECCE*, pp. 1–10.
- 38 Yao, K., Ren, Y., and Lee, F.C. (2004) Critical bandwidth for the load transient response of voltage regulator modules. *IEEE Trans. Power Electron.*, **19** (6), 1454–1461.
- 39 Wong, P.-L., Lee, F.C., Xu, P., and Yao, K. (2002) Critical inductance in voltage regulator modules. *IEEE Trans. Power Electron.*, **17** (4), 485–492.
- 40 Yao, K., Meng, Y., and Lee, F.C. (2002) Control bandwidth and transient response of buck converters. *Proceedings of the IEEE PESC*, pp. 137–142.
- 41 Chang, J.-S., Oh, H.-S., Jun, Y.-H., and Kong, B.-S. (2013) Fast output voltage-regulated PWM buck converter with an adaptive ramp amplitude control. *IEEE Trans. Circuits Syst. II Express Briefs*, **60** (10), 712–716.
- 42 Ridley, R. (2001) Custom vs. standard – adding capacitors to your power supply. *Switching Power Mag.*, **2**, 22–26.

- 43 Cantillo, A., De Nardo, A., Femia, N., and Zamboni, W. (2011) A unified practical design method for capacitors of switching converters. *IEEE Trans. Ind. Electron.*, **58** (8), 3521–3536.
- 44 Karppanen, M., Hankaniemi, M., Suntio, T., and Sippola, M. (2007) Dynamical characterization of peak-current-mode-controlled buck converter with output-current feedforward. *IEEE Trans. Power Electron.*, **22** (2), 444–451.
- 45 Ogata, K. (1997) *Modern Control Engineering*, Prentice-Hall, Upper Saddle River, NJ.
- 46 Dorf, R. and Bishop, R. (1998) *Modern Control Systems*, Addison-Wesley, Menlo Park, CA.
- 47 Goodwin, G., Graebe, S., and Salgado, M. (2001) *Control System Design*, Prentice Hall, Upper Saddle River, NJ.
- 48 Zhou, K. (1998) *Essentials of Robust Control*, Prentice Hall, Upper Saddle River, NJ.
- 49 Zhou, K., Doyle, J., and Glover, K. (1996) *Robust and Optimal Control*, Prentice Hall, Upper Saddle River, NJ.
- 50 Mitchell, D.M. (2001) Tricks of the trade: understanding the right-half-plane zero in small-signal DC-DC converter models. *IEEE Power Electron. Soc. News Letter*, 5–6.
- 51 Karppanen, M., Arminen, J., Suntio, T., Savela, K., and Simola, J. (2008) Dynamical modeling and characterization of peak-current-mode-controlled superbuck converter. *IEEE Trans. Power Electron.*, **23** (3), 1370–1380.
- 52 Huusari, J., Leppäaho, J., and Suntio, T. (2010) Dynamic properties of PCM-controlled superbuck converter – discrete vs. coupled inductor implementation. *Eur. Power Electron. Drives J.*, **20** (2), 8–15.

Part Three

Current-Fed Converters

7

Introduction to Current-Fed Converters

7.1 Introduction

Majority of the converter power stages developed by far are devoted to the voltage-fed applications due to the dominance of voltage as the main property of the energy sources [1,2]. There are, however, also energy sources having current as their main property such as photovoltaic generators [3–5] and superconductive magnetic energy storage (SMES) devices [6,7]. As a consequence, there also have to be power electronic converters, which can accept a current source as their main input source [2]. Even the concept of duality in circuit theory would imply their existence due to the dual nature of voltage and current [8].

The current-fed converters can be implemented from the corresponding voltage-fed converters by applying the duality transformation methods [9–14] or adding a capacitor at their input terminals for satisfying the terminal constraints stipulated by the source [15,16]. It is also natural that the current-fed converters can be implemented applying the capacitive switching cells (i.e., capacitive energy transfer) [17] similarly as the inductive switching cells (i.e., inductive energy transfer) applied for designing the voltage-fed converters [1].

The rest of this chapter is dedicated to implementing current-fed converters from the known voltage-fed converters by applying duality transformation methods. A short introduction to the steady-state properties of the current-fed converters implemented by adding a capacitor at their input terminals is also provided. The dynamic issues related to these converters are introduced in the subsequent chapters in detail.

7.2 Duality Transformation Basics

Duality transformation changes the power-stage components into their duals in the new power stage, as depicted in Figure 7.1. The usual problem in the transformation process is forgetting the changing of the conducting mode of the power-stage switching components to their corresponding duals, that is, when the switching component is turned on during the on-time in the original

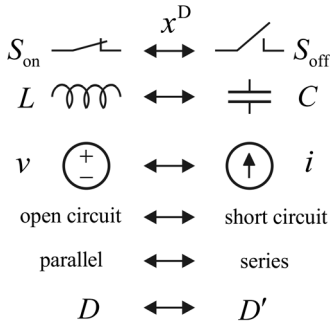


Figure 7.1 The duality-transformation pairs.
 Source: Leppäaho 2010. Reproduced with permission of IEEE.

power stage, it will be turned on during the off-time in the new power stage. This problem is clearly visible, for example, in Ref. [7].

A highly theoretical method to perform the duality transformation is to use graph technique as introduced in Refs [8,11], but this method would sometimes fail to produce the dual of the converter as in the case of the voltage-fed superbuck (cf. Chapter 3) [12]. The method introduced in Ref. [9] would yield easily the desired result when applied as follows:

A dot is placed in the center of every mesh of the power stage and one outside it serving as a common ground. The adjacent dots are connected together once over a certain branch. In the transformed power stage, the dots provide the connection points for the duality-transformed component in the branch over which the connection line goes between two adjacent dots. The branch components are transformed into their duals following the principles laid down in Figure 7.1. The input and output terminals contain usually a source and a series or parallel-connected component, which necessitates applying double conversion (i.e., the components and their connection method (series/parallel)). It is recommended that the parasitic elements associated with the converters are considered as embedded elements in the component, that is, the power stage shall be the ideal power stage of the converter. Sometimes the transformation of the switching components may not be clear enough. In such cases, it is highly recommended to transform the on-time and off-time subcircuits of the voltage-fed converter separately for studying how the subcircuits of the current-fed converter would look like in order to place correctly the switching components. It shall be remembered that the on-time subcircuit of the voltage-fed converter would yield the off-time subcircuit of the corresponding current-fed converter and the off-time subcircuit of the voltage-fed converter would yield the on-time subcircuit of the current-fed converter.

As an example of the application of the duality-transformation process, the voltage-fed superbuck (Figure 7.2) converter is transformed into its dual, that is, the current-fed superbuck converter (Figure 7.3). The duality transformation retains the basic static and dynamic properties of the original converter also in the transformed converter.

In the original converter (cf. Figure 7.2), the MOSFET switch (S_F) is turned on during the on-time, and the diode switch (S_D) conducts during the off-time. Figure 7.3 depicts the duality-transformation process according to the principles

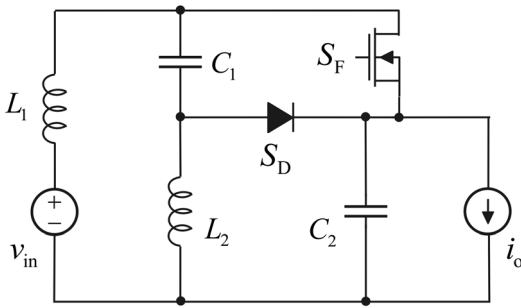


Figure 7.2 The voltage-fed superbuck converter. *Source:* Leppäaho 2010. Reproduced with permission of IEEE.

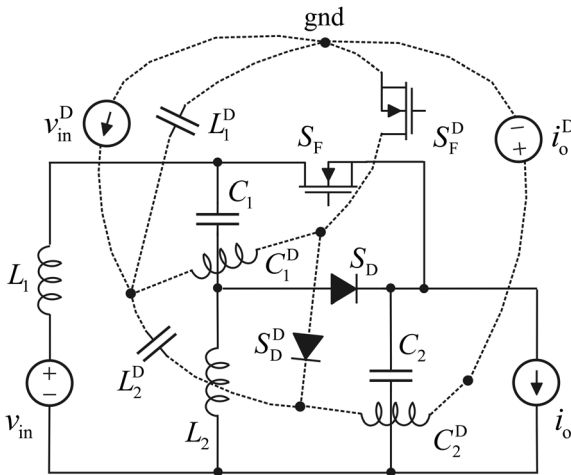


Figure 7.3 The original superbuck power stage and the transformation process flow. *Source:* Leppäaho 2010. Reproduced with permission of IEEE.

laid down above. Figure 7.4 shows the power stage of the current-fed superbuck, where the MOSFET will be turned on during the off-time. This means that the gate signal used in the voltage-fed converter has to be inverted for correct operation.

Figure 7.5 shows the subcircuits of the power stage during the on-time and off-time. According to circuit theory, by applying Kirchhoff's laws we can compute the voltages over the inductors and the currents flowing through the capacitors during the on-time and off-time as well as their averages as follows:

$$\begin{cases} v_{L1}^{\text{on}} = -v_{C2} \\ v_{L2}^{\text{on}} = v_{C1} + v_{C2} - v_o \\ i_{C1}^{\text{on}} = i_{\text{in}} - i_{L2} \\ i_{C2}^{\text{on}} = i_{L1} - i_{L2} \end{cases} \quad (7.1)$$

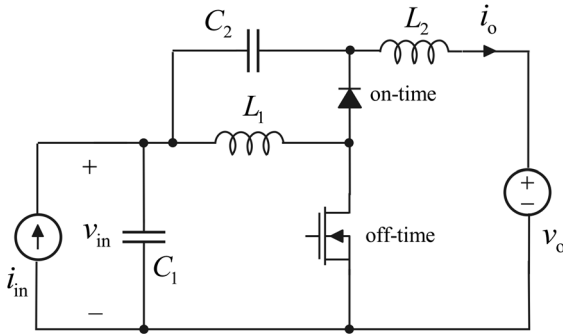


Figure 7.4 The power stage of the current-fed superbuck. *Source:* Leppäaho 2010. Reproduced with permission of IEEE.

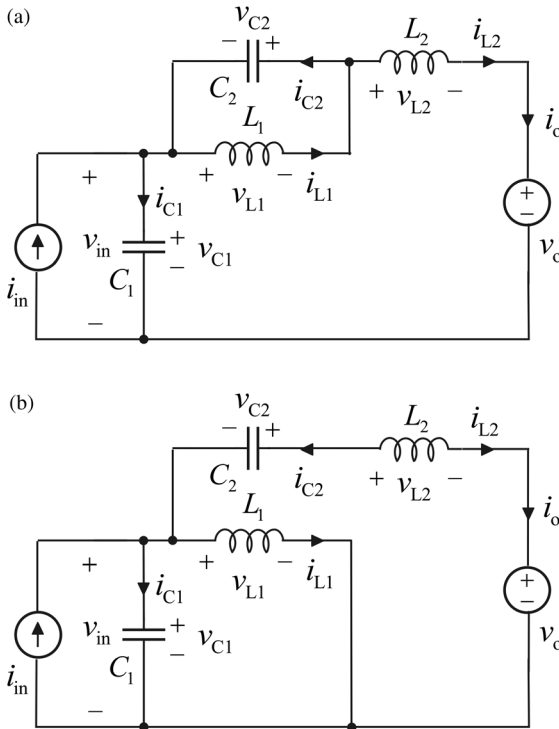


Figure 7.5 The subcircuits of the power stage during the (a) on-time, and (b) off-time. *Source:* Leppäaho 2010. Reproduced with permission of IEEE.

$$\begin{cases} v_{L1}^{\text{off}} = v_{C1} \\ v_{L2}^{\text{off}} = v_{C1} + v_{C2} - v_o \\ i_{C1}^{\text{off}} = i_{\text{in}} - i_{L1} - i_{L2} \\ i_{C2}^{\text{off}} = -i_{L2} \end{cases} \quad (7.2)$$

$$\begin{cases} \langle v_{L1} \rangle = d' \langle v_{C1} \rangle - d \langle v_{C2} \rangle \\ \langle v_{L2} \rangle = \langle v_{C1} \rangle + \langle v_{C2} \rangle - \langle v_o \rangle \\ \langle i_{C1} \rangle = \langle i_{in} \rangle - d' \langle i_{L1} \rangle - \langle i_{L2} \rangle \\ \langle i_{C2} \rangle = d \langle i_{L1} \rangle - \langle i_{L2} \rangle \end{cases} \quad (7.3)$$

Applying Vs and As balances (i.e., the averaged values have to be zero), we can obtain the operating point as follows:

$$\begin{aligned} V_{C1} &= DV_o \\ V_{C2} &= D'V_o \\ V_{in} &= V_{C1} \\ I_{L1} &= I_{in} \\ I_{L2} &= DI_{in} \\ I_o &= I_{L2} \end{aligned} \quad (7.4)$$

The operating point in Eq. (7.4) shows that $I_o = DI_{in}$ and $V_{in} = DV_o$, which indicate that the converter has the characteristic properties of buck converter (i.e., the input and output variables at the input and output terminals, respectively, are related by $M(D) = D$). We shall notice that the input and output variables are interchanged when considering the original voltage-fed converter and current-fed converter. If we are studying the levels of voltages and currents at the input and output terminals by not taking into account the change of input and output variables, we will observe that the transformed converter looks like a boost converter if the original converter looked like a buck converter or vice versa. Actually, it is true that the power stages of the voltage-fed buck and boost converters are dual of each other.

7.3 Duality-Transformed Converters

We provide here a collection of duality-transformed current-fed converters and their counterparts in the voltage-fed domain. Only the noninverting converters are treated. It shall be remembered that the transformation will interchange the input and output variables at both of the terminals, which means that the input-to-output modulo ($M(D)$) is related to the ratio of output- and input-terminal voltages (i.e., $M(D) = V_o/V_{in}$) in the voltage-fed converter and to the ratio of output- and input-terminal currents (i.e., $M(D) = I_o/I_{in}$) in the current-fed converter, respectively (Figures 7.6–7.11).

Figure 7.12 shows the voltage-fed and duality-transformed current-fed full-bridge converters equipped with an input LC filter. The corresponding gate-driven signals of the converters are shown in Figure 7.12c, where VF denotes the voltage-fed converter and CF the current-fed converter. It is also well known that the DDR-controlled full-bridge converter needs a capacitor connected in series with the primary side of the main transformer for ensuring proper transformer reset. In the current-fed converter, the proper transformer reset can be ensured by using the voltage-doubler circuit at the secondary side of the converter, as shown in Figure 7.12b.

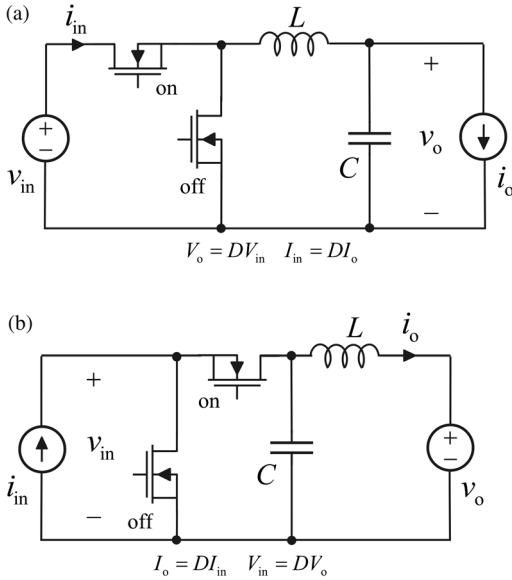


Figure 7.6 Buck converters. (a) Voltage-fed buck. (b) Current-fed buck. *Source:* Leppäaho 2010. Reproduced with permission of IEEE.

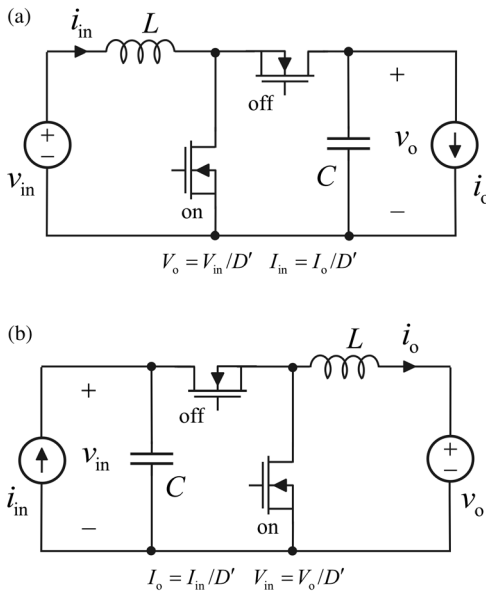


Figure 7.7 Boost converters. (a) Voltage-fed boost. (b) Current-fed boost.

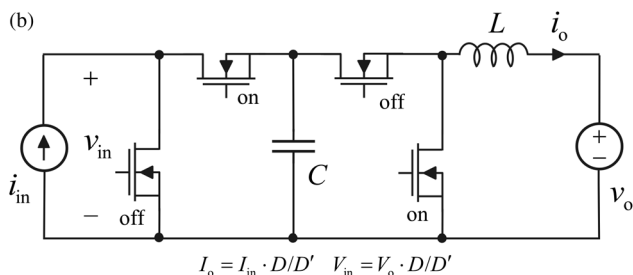
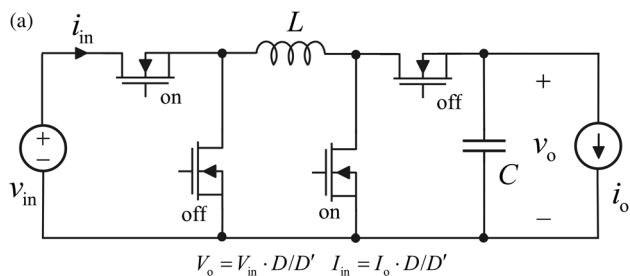


Figure 7.8 Buck-boost converters. (a) Voltage-fed noninverting buck-boost converter. (b) Current-fed noninverting buck-boost converter.

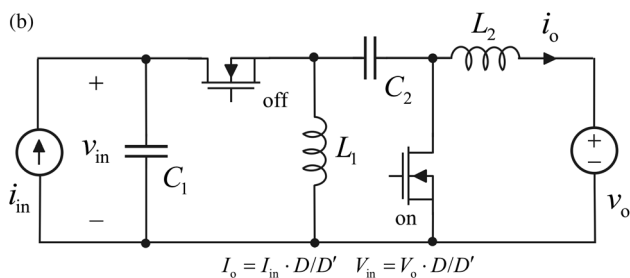
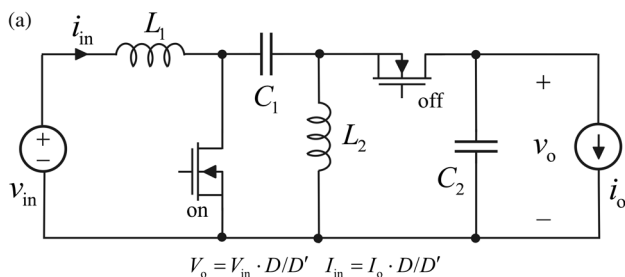


Figure 7.9 SEPIC converters. (a) Voltage-fed SEPIC. (b) Current-fed SEPIC.

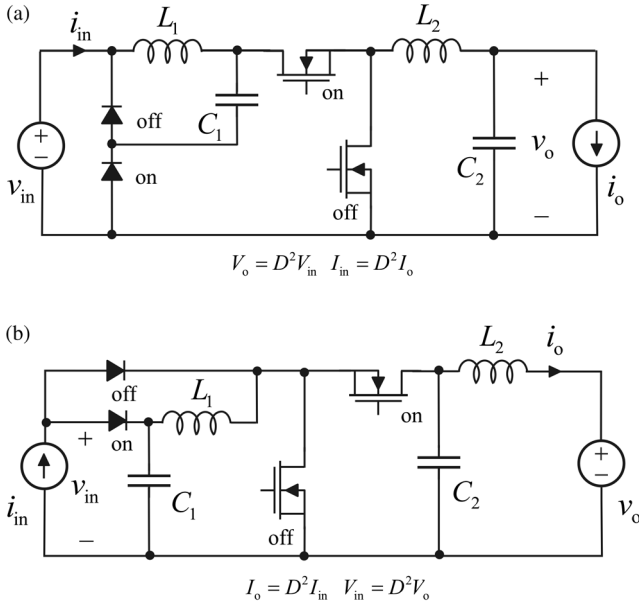


Figure 7.10 Quadratic buck converters. (a) Voltage-fed quadratic buck. (b) Current-fed quadratic buck.

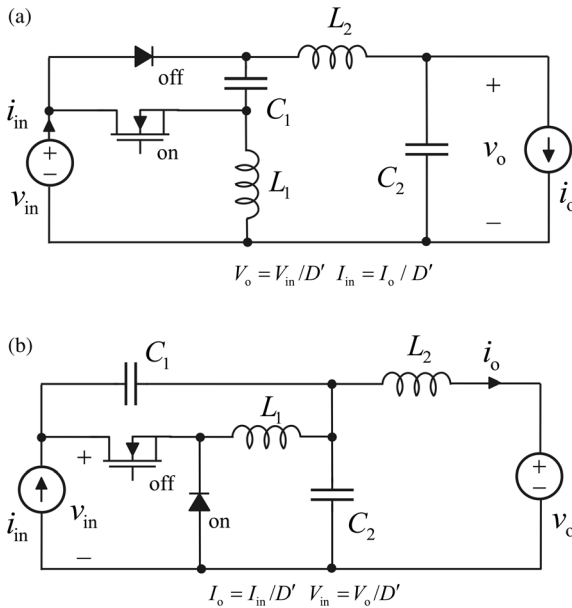


Figure 7.11 Superboost converters. (a) Voltage-fed superboost. (b) Current-fed superboost.

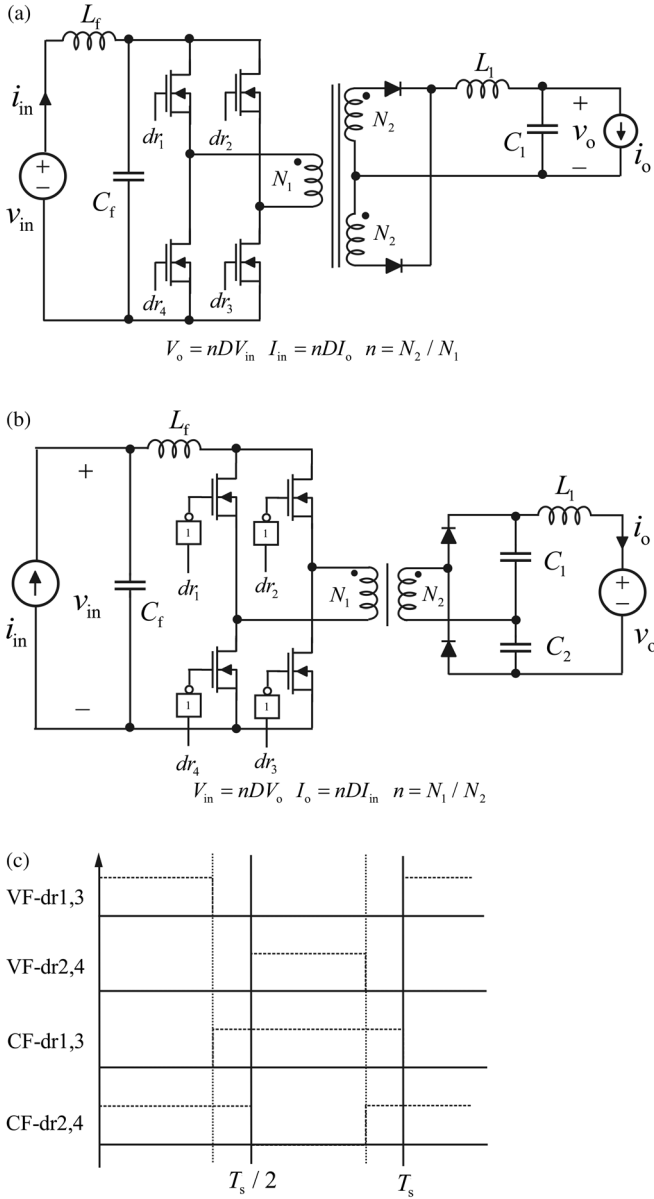


Figure 7.12 Full-bridge converters with input LC filters. (a) Voltage-fed full-bridge. (b) Current-fed full-bridge. (c) The corresponding gate control schemes.

Figure 7.13 shows the voltage-fed and duality-transformed current-fed half-bridge converters equipped with the input LC filters. It should be noticed that a part of the power-stage components at the primary side works also as the filter elements. The switch-control schemes of the converters are depicted in

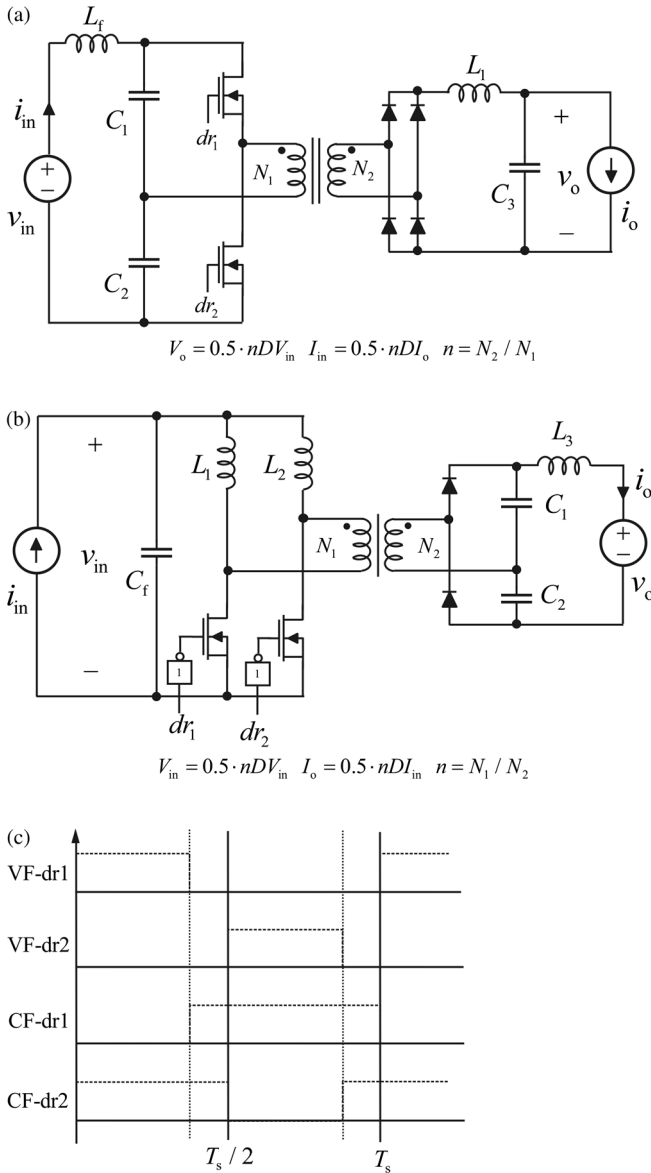


Figure 7.13 Half-bridge converters. (a) Voltage-fed full-bridge scheme. (b) Current-fed full-bridge scheme. (c) The corresponding gate control scheme.

Figure 7.13c. Proper transformer reset is automatically ensured in the voltage-fed converter due to the input-side capacitors. In the current-fed converter, the proper transformer reset can be ensured by using the voltage-doubler circuit at the secondary side of the converter, as shown in Figure 7.13b.

7.4 Input Capacitor-Based Converters

The most common way of providing the interface between the current-based sources such as photovoltaic generator is to use the well-known voltage-fed converters equipped with an input capacitor [5,18–21]. It has been clearly noticed that the controlling of the converter requires decreasing the duty ratio for increasing the output variables when the switch control signals are maintained as they are in the original voltage-fed converter [15,18,19]. Many other dynamic anomalies will appear in addition to the necessity to decrement the duty ratio instead of incrementing it for increasing the output variables. We will discuss more in detail on those dynamic issues in Chapters 8 and 9.

Figures 7.14–7.16 show the basic power stages applied in the current-fed applications and their input-to-output relations in current and voltage levels. The physical terminal voltage and current levels are maintained the same as they are in the voltage-fed application. If looking at the input-to-output modulus in the figures, it is obvious that the duty ratio has to be decreased for increasing the corresponding output variables.

The current-fed buck power-stage converter (cf. Figure 7.14) is usually applied in interfacing the storage batteries and photovoltaic generators [22]. The power stage resembles closely the current-fed boost converter shown in Figure 7.7b. The current-fed boost converter properties can be fully recovered by inverting the gate signals of the switch components [15].

The current-fed boost power stage converter (cf. Figure 7.15) is usually applied as a front-end converter between the photovoltaic generator and the grid-connected inverter for enabling the use of wider operation range in the photovoltaic generator [23,24]. The power stage resembles the current-fed buck

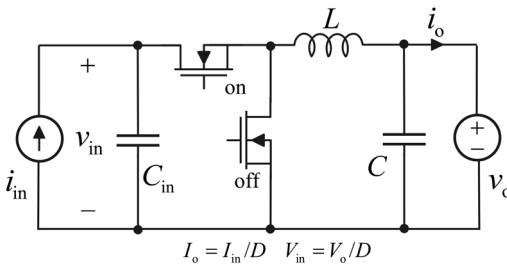


Figure 7.14 Current-fed buck power-stage converter.

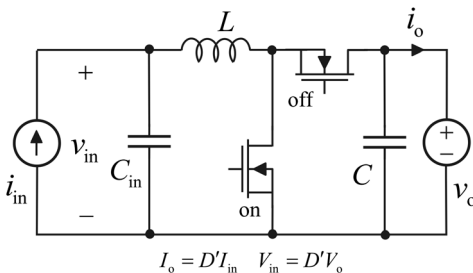


Figure 7.15 Current-fed boost power-stage converter.

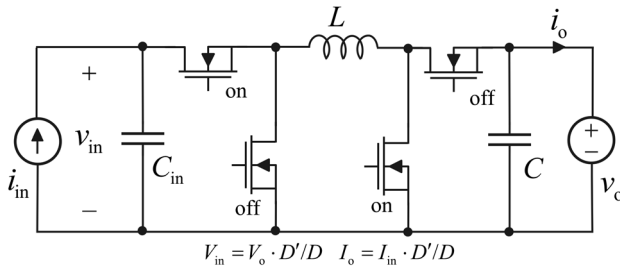


Figure 7.16 Current-fed buck–boost power-stage converter.

converter in Figure 7.6b when a LC input filter is added at its input terminal. The missing of the output inductor means that the output current is pulsating. When inverting the gate signals of the switches, the input-to-output relation also becomes that of the buck converter.

The current-fed buck–boost power-stage converter (cf. Figure 7.16) is usually applied in series-connected distributed photovoltaic applications, where the level of the converter output voltage can be higher or lower than the corresponding input voltage [25]. When all the switches of the converter are based on controlled switches, the converter can be operated either in buck, boost, or buck–boost mode. Similar manner as above, the buck–boost input-to-output relation can be recovered by inverting the gate signals.

References

- 1 Tymerski, R. and Vorpérian, V. (1988) Generation and classification of PWM DC-to-DC converters. *IEEE Trans. Aerosp. Electron. Syst.*, **24** (6), 743–754.
- 2 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters – Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.
- 3 Lyi, S. and Dougal, R.A. (2002) Dynamic multiphysics model for solar array. *IEEE Trans. Energy Convers.*, **17** (2), 285–294.
- 4 Nousiainen, L., Puuko, J., Mäki, A., Messo, T., Huusari, J., Jokipii, J., Viinamäki, J., Torres Lobera, D., Valkealahti, S., and Suntio, T. (2013) Photovoltaic generator as an input source for power electronic converters. *IEEE Trans. Power Electron.*, **28** (6), 3028–3038.
- 5 Capel, A., Marpinar, J.C., Jalade, J., and Valentin, M. (1983) Current fed and voltage fed switching dc/dc converters – steady state and dynamic models, their application in space technology. Proceedings of the INTELEC, pp. 421–430.
- 6 Ali, M.H., Wu, B., and Dougal, R.A. (2010) An overview of SMES applications in power and energy systems. *IEEE Trans. Sustain. Energy*, **1** (1), 38–45.
- 7 Shmilovitz, D. and Singer, S. (2002) A switched mode converter suitable for superconductive magnetic energy storage (SMES) systems. Proceedings of the IEEE APEC, pp. 630–634.
- 8 Desoer, C.A. and Kuh, E.S. (1969) *Basic Circuit Theory*, McGraw-Hill Kogakusha, Tokyo, Japan.

- 9 Cuk, S. (1979) General topological properties of switching structures. Proceedings of the IEEE PESC'79, pp. 109–130.
- 10 Wolfs, P.J. (1993) A current-sourced DC–DC converter derived via duality principle from half-bridge converter. *IEEE Trans. Ind. Electron.*, **40** (1), 139–144.
- 11 Shmilovitz, D. (2005) Application of duality for derivation of current converter topologies. *HIT J. Sci. Eng. B*, **2** (3–4), 529–557.
- 12 Leppäaho, J. and Suntio, T. (2011) Dynamic characteristics of current-fed superbuck converter. *IEEE Trans. Power Electron.*, **26** (1), 200–209.
- 13 Huusari, J. and Suntio, T. (2012) Dynamic properties of current-fed quadratic full-bridge buck converter for distributed photovoltaic MPP-tracking systems. *IEEE Trans. Power Electron.*, **27** (11), 4681–4689.
- 14 Williams, B.W. (2014) Generation and analysis of canonical switching cell DC-to-DC converters. *IEEE Trans. Ind. Electron.*, **61** (1), 329–346.
- 15 Leppäaho, J., Nousiainen, L., Puukko, J., Huusari, J., and Suntio, T. (2010) Implementing current-fed converters by adding an input capacitor at the input of voltage-fed converter for interfacing solar generator. Proceedings of the EPE-PEMC, pp. 81–88.
- 16 Huusari, J. and Suntio, T. (2012) Interfacing constraints of distributed maximum power point tracking converters in photovoltaic applications. Proceedings of the EPE-PEMC, pp. DS3d.1–1-DS3d1-7.
- 17 Shmilovitz, D. (2006) Gyrator realization based on a capacitive switched cell. *IEEE Trans. Circuits Syst., Exp. Briefs*, **53** (12), 1418–1422.
- 18 Ziao, W., Dunford, W.G., Palmer, P.R., and Capel, A. (2007) Regulation of photovoltaic voltage. *IEEE Trans. Ind. Electron.*, **54** (3), 1365–1374.
- 19 Xiao, W., Ozog, N., and Dunford, W.G. (2007) Topology study of photovoltaic interface for maximum power point tracking. *IEEE Trans. Ind. Electron.*, **54** (3), 1696–1704.
- 20 Dehbonei, H., Lee, S.R., and Nehrir, H. (2009) Direct energy transfer for high efficiency photovoltaic energy systems – Part I: concepts and hypothesis. *IEEE Trans. Aerosp. Electron. Syst.*, **45** (1), 31–45.
- 21 Dehbonei, H., Lee, S.R., and Ko, S.H. (2009) Direct energy transfer for high efficiency photovoltaic energy systems – Part II: experimental evaluation. *IEEE Trans. Aerosp. Electron. Syst.*, **45** (1), 46–57.
- 22 Gadelovits, S., Sitbon, M., Suntio, T., and Kuperman, A. (2015) Single-source multibattery solar charger: case study and implementation issues. *Prog. Photovolt. Res. Appl.*, **23** (12), 1916–1928.
- 23 Yang, Y., Wang, H., Blaabjerg, F., and Kerekes, T. (2014) A hybrid power control concept for PV inverters with reduced thermal loading. *IEEE Trans. Power Electron.*, **29** (12), 6271–6275.
- 24 Viinamäki, J., Jokipii, J., Messo, T., Suntio, T., Sitbon, M., and Kuperman, A. (2015) Comprehensive dynamic analysis of PV-generator-interfacing DC–DC boost power stage. *IET Renew. Power Gener.*, **9** (4), 306–314.
- 25 Huusari, J. and Suntio, T. (2013) Origin of cross-coupling effects in distributed DC–DC converters in photovoltaic applications. *IEEE Trans. Power Electron.*, **28** (10), 5311–5322.

8

Dynamic Modeling of DDR-Controlled CF Converters

8.1 Introduction

In principle, the methods applied to model the dynamics of DDR-controlled voltage-fed converters introduced in Chapter 3 [1–7] will apply equally also to model the dynamics of the current-fed converters. The main problem encountered, in practice, is the inability to recognize the correct input and output variables, which are naturally interchanged compared to the voltage-fed converters [8]. When the converter is fed by a current source, the internal mode of operation is classified based on the behavior of capacitor voltage similarly as in case of the voltage-fed converters based on the behavior of inductor current [9]: The operation mode is continuous if the corresponding state variable has two different derivatives, and the operation is discontinuous if the corresponding state variable will stay at zero level during a part of the cycle (cf. Chapter 3 and Figure 2.37). Earlier, the discontinuous capacitor-voltage-mode operation has been utilized in shaping the input current of the power factor correction converters to emulate the shape of the input voltage [10,11].

In the renewable applications, where the current-fed converters are most often used, the discontinuous mode of operation is not relevant. This means that we will concentrate in this book on modeling the dynamic behavior of the relevant converters in the continuous mode of operation only applying the basic state space averaging method introduced in Ref. [4]. The renewable energy converters will be operating most often as current-output converters (cf. Figure 8.1a) but the output mode can be changed to voltage-output mode (cf. Figure 8.1b), for example, to prevent the DC-link voltage to researching too high level in case of the grid-connected inverter failure. The parameter set in Figure 8.1a represents H -parameters, and in Figure 8.1b Z -parameters. We will actually provide dynamic models only to the current-fed current-output CF-CO converter, and the dynamic models for the current-fed voltage-output (CF-VO) converter can be developed by interchanging the input-terminal input and output variables similarly as obtaining the dynamic models for the VF-CO converters from the corresponding dynamic models of the VF-VO converter introduced in Chapter 5.

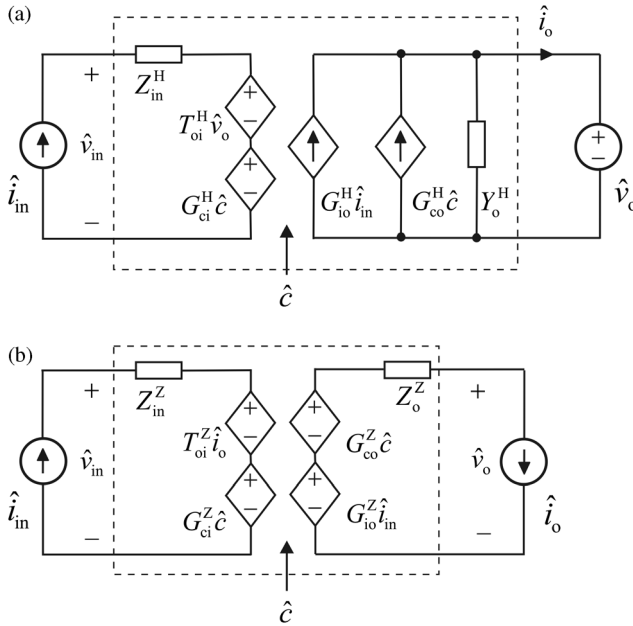


Figure 8.1 The dynamic equivalent circuits of (a) a current-fed current-output converter and (b) a current-fed voltage-output converter.

8.2 Dynamic Models

As already stated, we will model the relevant converters in CCM only, where all the state variables are continuous and the associated ripple components do not contribute to the dynamic behavior of the converter. In practice, this means that pure circuit theory can be applied for computing the required derivatives of the state variables and the formulations for the output variables as instructed in Chapter 2. In addition to the basic transfer functions, we will also give the set of special transfer functions. The set of basic transfer functions forms the H -parameter representation of the CF-CO converter (cf. Figure 8.1a), where the input variables are the input current (i_{in}) and output voltage (v_o), the output variables are the input voltage (v_{in}) and output current (i_o), the state variables are the inductor currents (i_{Li}) and capacitor voltages (v_{Ci}), and the control variable is the duty ratio (d). The corresponding set of the basic transfer functions can be given by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in} & T_{oi} & G_{ci} \\ G_{io} & -Y_o & G_{co} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \\ \hat{d} \end{bmatrix}, \quad (8.1)$$

and the set of special transfer functions by

$$\begin{bmatrix} Z_{in-oco} & Z_{in-\infty} & T_{oi-\infty} \\ Y_{o-sci} & Y_{o-\infty} & G_{io-\infty} \end{bmatrix} = \begin{bmatrix} Z_{in} + \frac{G_{io}T_{oi}}{Y_o} & Z_{in} - \frac{G_{io}G_{ci}}{G_{co}} & T_{oi} + \frac{Y_oG_{ci}}{G_{co}} \\ Y_o + \frac{G_{io}T_{oi}}{Z_{in}} & Y_o + \frac{T_{oi}G_{co}}{G_{ci}} & G_{io} - \frac{Z_{in}G_{co}}{G_{ci}} \end{bmatrix}. \quad (8.2)$$

The CF converters in the renewable energy applications are usually operated at closed loop under input-voltage feedback control. Therefore, Z_{in-oco} (i.e., input impedance at open-circuit output) will be affected by the state of input-voltage feedback. Y_{o-sci} (i.e., output admittance at short-circuited input) is not affected by the state of input-voltage feedback. Thus Z_{in-oco}^x can be given in general by

$$Z_{in-oco}^x = Z_{in-x} + \frac{G_{io-x} T_{oi-x}}{Y_{o-x}} = \frac{Z_{in-x}}{Y_{o-x}} \cdot Y_{o-sci}, \quad (8.3)$$

where the superscript and subscript extension x denotes the state of input-voltage feedback (i.e., $x = o$ at open loop and $x = c$ at closed loop). If the feedback is taken from the output current only, then Z_{in-oco} will be invariant to the state of feedback. All the other special parameters in Eq. (8.2) are invariant to the state of input-voltage or output-current feedback.

If the CF converter is used in the output-voltage mode, the corresponding transfer functions (i.e., the Z -parameter set) can be found by changing the input and output variables at the output terminal in Eq. (8.1), which yields

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Z_{in}^Z & T_{oi}^Z & G_{ci}^Z \\ G_{io}^Z & -Z_o^Z & G_{co}^Z \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}, \quad (8.4)$$

where

$$\begin{bmatrix} Z_{in}^Z & T_{oi}^Z & G_{ci}^Z \\ G_{io}^Z & Z_o^Z & G_{co}^Z \end{bmatrix} = \begin{bmatrix} Z_{in} + \frac{G_{io} T_{oi}}{Y_o} & -\frac{T_{oi}}{Y_o} & G_{ci} + \frac{T_{oi} G_{co}}{Y_o} \\ \frac{G_{io}}{Y_o} & \frac{1}{Y_o} & \frac{G_{co}}{Y_o} \end{bmatrix}. \quad (8.5)$$

The corresponding set of ideal parameters can be given by

$$\begin{bmatrix} Z_{in-oco}^Z & Z_{in-\infty}^Z & T_{oi-\infty}^Z \\ Z_{o-sci}^Z & Z_{o-\infty}^Z & G_{io-\infty}^Z \end{bmatrix} = \begin{bmatrix} Z_{in}^Z + \frac{G_{io}^Z T_{oi}^Z}{Z_o^Z} & Z_{in}^Z - \frac{G_{io}^Z G_{ci}^Z}{G_{co}^Z} & T_{oi}^Z + \frac{Z_o^Z G_{ci}^Z}{G_{co}^Z} \\ Z_o^Z + \frac{G_{io}^Z T_{oi}^Z}{Z_{in}^Z} & Z_o^Z + \frac{T_{oi}^Z G_{co}^Z}{G_{ci}^Z} & G_{io}^Z - \frac{Z_{in}^Z G_{co}^Z}{G_{ci}^Z} \end{bmatrix}, \quad (8.6)$$

or

$$\begin{bmatrix} Z_{in-oco}^Z & Z_{in-\infty}^Z & T_{oi-\infty}^Z \\ Z_{o-sci}^Z & Z_{o-\infty}^Z & G_{io-\infty}^Z \end{bmatrix} = \begin{bmatrix} Z_{in} & Z_{in-\infty} & \frac{G_{ci}}{G_{co}} \\ \frac{1}{Y_{o-sci}} & \frac{1}{Y_{o-\infty}} & \frac{G_{io-\infty}}{Y_{o-\infty}} \end{bmatrix}. \quad (8.7)$$

We do not give explicitly the Z -parameter-based transfer functions, which can be developed easily by means of the H -parameter-based transfer functions given in Eqs (8.5) and (8.7) by applying a proper software package such as Matlab™ and its Symbolic Toolbox.

8.2.1 Duality Transformed Converters

As stated in Chapter 7, the duality transformed converters retain the similar steady-state and dynamic properties as their original voltage-fed converters have, that is, the input-to-output modulo, the basic dynamical features, and the increase in the duty ratio yields an increase in the corresponding output variables accordingly.

8.2.1.1 Buck Converter

The power stage of the CF buck converter is given in Figure 8.2a with all the relevant parasitic elements. In practice, the CF buck converter cannot be used as such but an input filter has to be connected at its input terminal as depicted in Figure 8.2b because of the output capacitor of the practical input current sources [12]. If comparing the input filter of a VF converter and CF converter, the input and output terminals are interchanged. The input filter will affect the dynamics of the converter by means of its output impedance, which is a parallel resonant circuit in case of VF converter and a series resonant circuit in case of CF converter. This change of resonant circuit type also complies well with the duality transformation principle.

The power stage of the CF buck converter in Figure 8.2a can be given during the on-time as shown in Figure 8.3a, and during the off-time as shown in Figure 8.3b. Applying Kirchhoff's voltage and current laws, the set of state-space equations related to the on-time can be given by

$$\begin{aligned}
 \frac{di_{L1}}{dt} &= -\frac{r_{L1} + r_{C1}}{L_1} i_{L1} + \frac{1}{L_1} v_{C1} + \frac{r_{C1}}{L_1} i_{in} - \frac{1}{L_1} v_o, \\
 \frac{dv_{C1}}{dt} &= -\frac{1}{C_1} i_{L1} + \frac{1}{C_1} i_{in}, \\
 v_{in} &= -r_{C1} i_{L1} + v_{C1} + (r_{C1} + r_{ds1}) i_{in}, \\
 i_o &= i_{L1},
 \end{aligned} \tag{8.8}$$

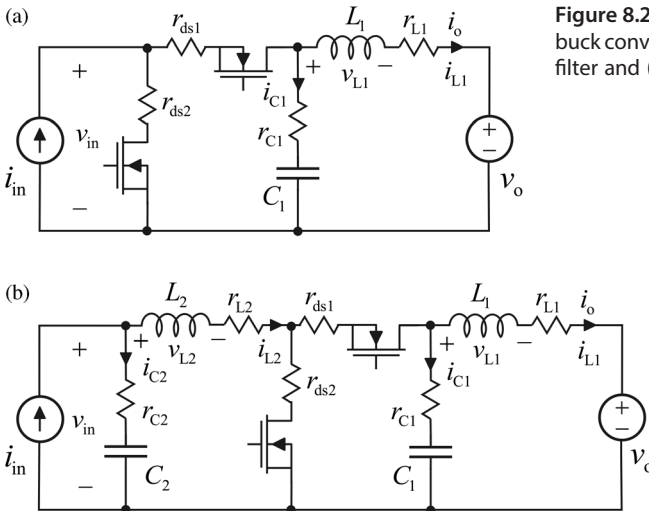


Figure 8.2 The power stage of a CF buck converter (a) without the input filter and (b) with the input filter.

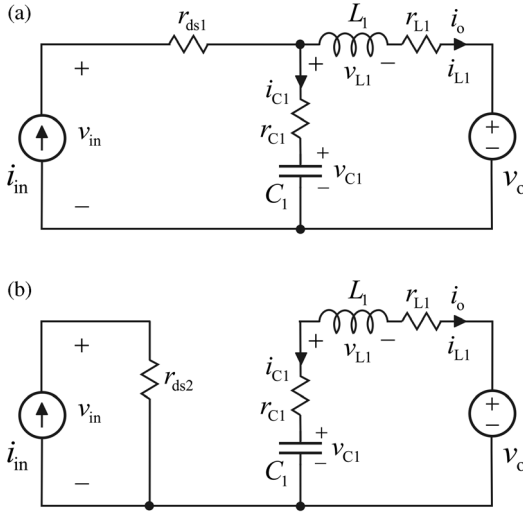


Figure 8.3 CF buck power-stage structures. (a) During the on-time. (b) During the off-time.

and related to the off-time by

$$\begin{aligned} \frac{di_{L1}}{dt} &= -\frac{r_{L1} + r_{C1}}{L_1} i_{L1} + \frac{1}{L_1} v_{C1} - \frac{1}{L_1} v_o, \\ \frac{dv_{C1}}{dt} &= -\frac{1}{C_1} i_{L1}, \\ v_{in} &= r_{ds2} i_{in}, \\ i_o &= i_{L1}. \end{aligned} \quad (8.9)$$

The averaged state-space equations and the operating point can be given by

$$\begin{aligned} \frac{d\langle i_{L1} \rangle}{dt} &= -\frac{r_{L1} + r_{C1}}{L_1} \langle i_{L1} \rangle + \frac{1}{L_1} \langle v_{C1} \rangle + \frac{dr_{C1}}{L_1} \langle i_{in} \rangle - \frac{1}{L_1} \langle v_o \rangle, \\ \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{C_1} \langle i_{L1} \rangle + \frac{d}{C_1} \langle i_{in} \rangle, \\ \langle v_{in} \rangle &= -dr_{C1} \langle i_{L1} \rangle + d \langle v_{C1} \rangle + (d(r_{C1} + r_{ds1}) + d' r_{ds2}) \langle i_{in} \rangle, \\ \langle i_o \rangle &= \langle i_{L1} \rangle. \\ V_{C1} &= V_o + Dr_{L1} I_{in}, \\ V_{in} &= DV_o + (D^2 r_{L1} + DD' r_{C1} + Dr_{ds1} + D' r_{ds2}) I_{in}, \\ I_o &= I_{L1} = DI_{in}. \end{aligned} \quad (8.10)$$

According to the operating point values in Eq. (8.11), the input modulo ($M(D)$) equals clearly the steady-state duty ratio (D), which means that the converter is a buck-type converter.

The linearized state space can be given by

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1}\hat{i}_{L1} + \frac{1}{L_1}\hat{v}_{C1} + \frac{Dr_{C1}}{L_1}\hat{i}_{in} - \frac{1}{L_1}\hat{v}_o + \frac{r_{C1}I_{in}}{L_1}\hat{d}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{C_1}\hat{i}_{L1} + \frac{D}{C_1}\hat{i}_{in} + \frac{I_{in}}{C_1}\hat{d}, \\
 \hat{v}_{in} &= -Dr_{C1}\hat{i}_{L1} + D\hat{v}_{C1} + r_{e2}\hat{i}_{in} + V_{e1}\hat{d}, \\
 \hat{i}_o &= \hat{i}_{L1},
 \end{aligned} \tag{8.12}$$

where

$$\begin{aligned}
 r_{e1} &= r_{L1} + r_{C1}, \\
 r_{e2} &= Dr_{C1} + Dr_{ds1} + D'r_{ds2}, \\
 V_{e1} &= V_o + (Dr_{L1} + D'r_{C1} + r_{ds1} - r_{ds2})I_{in}.
 \end{aligned} \tag{8.13}$$

The set of transfer function representing the dynamic behavior of the converter can be solved from the linearized state space in Eq. (8.12), as instructed in Chapter 2. Thus the input dynamics can be given by

$$\begin{aligned}
 \Delta Z_{in-o} &= s^2 r_{e2} + sD^2 \frac{(L_1 + (r_{e1}r_{e2} - r_{C1}^2)C_1)}{L_1 C_1} + \frac{r_{e2} + D^2(r_{e1} - r_{C1})}{L_1 C_1}, \\
 \Delta T_{oi-o} &= \frac{D(1 + sr_{C1}C_1)}{L_1 C_1}, \\
 \Delta G_{ci-o} &= s^2 V_{e1} + s \frac{(r_{e1}V_{e1}C_1 + D(L_1 - r_{C1}^2 C_1)I_{in})}{L_1 C_1} + \frac{V_{e1} + D(r_{e1} - 2r_{C1})I_{in}}{L_1 C_1},
 \end{aligned} \tag{8.14}$$

and the output dynamics by

$$\begin{aligned}
 \Delta Y_{o-o} &= \frac{s}{L_1}, \\
 \Delta G_{io-o} &= \frac{D(1 + sr_{C1}C_1)}{L_1 C_1}, \\
 \Delta G_{co-o} &= \frac{I_{in}(1 + sr_{C1}C_1)}{L_1 C_1}.
 \end{aligned} \tag{8.15}$$

Δ in Eqs (8.14) and (8.15) denotes the determinant of the system and can be given by

$$\Delta = s^2 + s \frac{r_{e1}}{L_1} + \frac{1}{L_1 C_1}. \tag{8.16}$$

The set of special parameters can be given as follows:

$$\begin{aligned}
 Z_{\text{in-oco}}^o &= \frac{D^2 + sr_{e2}C_1}{sC_1}, \\
 Y_{\text{o-sci}} &= (D^2 + sr_{e2}C_1)/(L_1C_1r_{e2}(s^2 + s\left(\frac{D^2}{r_{e2}C_1} + \frac{r_{e1}r_{e2} - D^2r_{C1}}{L_1}\right) + \frac{r_{e2} + D^2(r_{e1} - 2r_{C1})}{L_1C_1}), \\
 Z_{\text{in-}\infty} &= r_{e2} - \frac{DV_{e1}}{I_{\text{in}}}, \\
 T_{\text{oi-}\infty} &= \frac{D(1 + s(V_{e1}C_1/DI_{\text{in}}))}{1 + sr_{C1}C_1}, \\
 Y_{\text{o-}\infty} &= \frac{DI_{\text{in}}(1 + s(V_{e1}C_1/DI_{\text{in}}))}{LCV_{e1}(s^2 + s((DI_{\text{in}}/V_{e1}C_1) + (r_{e1} - (DI_{\text{in}}/V_{e1})r_{C1}^2)/L_1) + (1 + D(r_{e1} - 2r_{C1})(I_{\text{in}}/V_{e1})/L_1C_1))}. \\
 G_{\text{io-}\infty} &= ((DV_{e1} - r_{e2}I_{\text{in}})(1 + sr_{C1}C_1))/\left(LCV_{e1}(s^2 + s\left(\frac{DI_{\text{in}}}{V_{e1}C_1} + \frac{r_{e1} - (DI_{\text{in}}/V_{e1})r_{C1}^2}{L_1}\right) + \frac{1 + D(r_{e1} - 2r_{C1})(I_{\text{in}}/V_{e1})}{L_1C_1}\right), \quad (8.17)
 \end{aligned}$$

When comparing the dynamic representations of the VF buck converter given in Chapter 3 and the CF buck converter given in Eqs (8.14)–(8.17), they resemble very closely to each other, that is, $G_{\text{io-o}}$ and $T_{\text{oi-o}}$ are symbolically the same, the resonant frequency is not dependent on the duty ratio, the control-related transfer functions do not contain RHP zeros, the ideal input impedance corresponds to a negative incremental resistance (i.e., $Z_{\text{in-}\infty} \approx -(V_{\text{in}}/I_{\text{in}})$), and so on. It is obvious that the duality transformation retains both steady-state and dynamic properties quite intact.

The on-time and off-time power stages of the CF buck converter with the input filter are shown in Figure 8.4, respectively. Applying Kirchhoff's voltage and current laws, the state space during the on-time can be given by

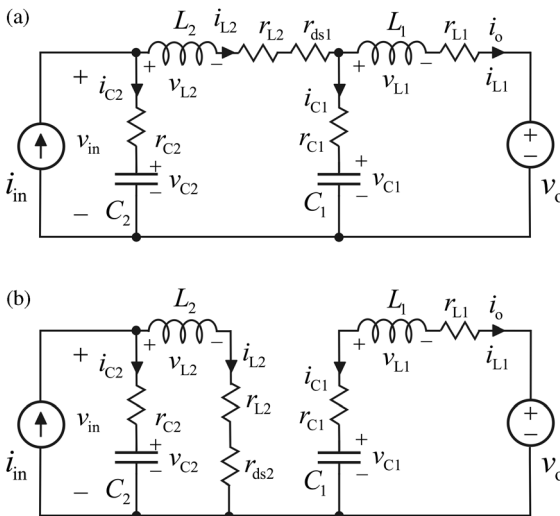


Figure 8.4 CF buck power-stage structures with the input filter. (a) During the on-time. (b) During the off-time.

$$\begin{aligned}
\frac{di_{L1}}{dt} &= -\frac{r_{L1} + r_{C1}}{L_1} i_{L1} + \frac{r_{C1}}{L_1} i_{L2} + \frac{1}{L_1} v_{C1} - \frac{1}{L_1} v_o, \\
\frac{di_{L2}}{dt} &= \frac{r_{C1}}{L_2} i_{L1} - \frac{r_{L2} + r_{ds1} + r_{C1} + r_{C2}}{L_2} i_{L2} - \frac{1}{L_2} v_{C1} + \frac{1}{L_2} v_{C2} + \frac{r_{C2}}{L_2} i_{in}, \\
\frac{dv_{C1}}{dt} &= -\frac{1}{C_1} i_{L1} + \frac{1}{C_1} i_{L2}, \\
\frac{dv_{C2}}{dt} &= -\frac{1}{C_2} i_{L2} + \frac{1}{C_2} i_{in}, \\
v_{in} &= -r_{C2} i_{L2} + v_{C2} + r_{C2} i_{in}, \\
i_o &= i_{L1},
\end{aligned} \tag{8.18}$$

and during the off-time by

$$\begin{aligned}
\frac{di_{L1}}{dt} &= -\frac{r_{L1} + r_{C1}}{L_1} i_{L1} + \frac{1}{L_1} v_{C1} - \frac{1}{L_1} v_o, \\
\frac{di_{L2}}{dt} &= -\frac{r_{L2} + r_{ds2} + r_{C2}}{L_2} i_{L2} + \frac{1}{L_2} v_{C2} + \frac{r_{C2}}{L_2} i_{in}, \\
\frac{dv_{C1}}{dt} &= -\frac{1}{C_1} i_{L1}, \\
\frac{dv_{C2}}{dt} &= -\frac{1}{C_2} i_{L2} + \frac{1}{C_2} i_{in}, \\
v_{in} &= -r_{C2} i_{L2} + v_{C2} + r_{C2} i_{in}, \\
i_o &= i_{L1}.
\end{aligned} \tag{8.19}$$

The averaged state space and the operating point values can be computed from Eqs (8.18) and (8.19) and given by

$$\begin{aligned}
\frac{d\langle i_{L1} \rangle}{dt} &= -\frac{r_{L1} + r_{C1}}{L_1} \langle i_{L1} \rangle + \frac{dr_{C1}}{L_1} \langle i_{L2} \rangle + \frac{1}{L_1} \langle v_{C1} \rangle - \frac{1}{L_1} \langle v_o \rangle, \\
\frac{d\langle i_{L2} \rangle}{dt} &= \frac{dr_{C1}}{L_2} \langle i_{L1} \rangle - \frac{r_{L2} + r_{C2} + dr_{C1} + dr_{ds1} + d'r_{ds2}}{L_2} \langle i_{L2} \rangle - \frac{d}{L_2} \langle v_{C1} \rangle \\
&\quad + \frac{1}{L_2} \langle v_{C2} \rangle + \frac{r_{C2}}{L_2} \langle i_{in} \rangle, \\
\frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{C_1} \langle i_{L1} \rangle + \frac{d}{C_1} \langle i_{L2} \rangle, \\
\frac{d\langle v_{C2} \rangle}{dt} &= -\frac{1}{C_2} \langle i_{L2} \rangle + \frac{1}{C_2} \langle i_{in} \rangle, \\
\langle v_{in} \rangle &= -r_{C2} \langle i_{L2} \rangle + \langle v_{C2} \rangle + r_{C2} \langle i_{in} \rangle, \\
\langle i_o \rangle &= \langle i_{L1} \rangle.
\end{aligned} \tag{8.20}$$

$$\begin{aligned}
V_{C1} &= V_o + Dr_{L1}I_{in}, \\
V_{in} &= V_{C2} = DV_o + (D^2r_{L1} + r_{L2} + DD'r_{C1} + Dr_{ds1} + D'r_{ds2})I_{in}, \\
I_{L1} &= DI_{in}, \\
I_{L2} &= I_{in}, \\
I_o &= DI_{in}.
\end{aligned} \tag{8.21}$$

The linearized state space can be computed from the averaged state space in Eq. (8.20) applying the methods presented in Chapter 2. This process yields

$$\begin{aligned}
\frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1}\hat{i}_{L1} + \frac{Dr_{C1}}{L_1}\hat{i}_{L2} + \frac{1}{L_1}\hat{v}_{C1} - \frac{1}{L_1}\hat{v}_o + \frac{r_{C1}I_{in}}{L_1}\hat{d}, \\
\frac{d\hat{i}_{L2}}{dt} &= \frac{Dr_{C1}}{L_2}\hat{i}_{L1} - \frac{r_{e2}}{L_2}\hat{i}_{L2} - \frac{D}{L_2}\hat{v}_{C1} + \frac{1}{L_2}\hat{v}_{C2} + \frac{r_{C2}}{L_2}\hat{i}_{in} - \frac{V_{e1}}{L_2}\hat{d}, \\
\frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{C_1}\hat{i}_{L1} + \frac{D}{C_1}\hat{i}_{L2} + \frac{I_{in}}{C_1}\hat{d}, \\
\frac{d\hat{v}_{C2}}{dt} &= -\frac{1}{C_2}\hat{i}_{L2} + \frac{1}{C_2}\hat{i}_{in}, \\
\hat{v}_{in} &= -r_{C2}\hat{i}_{L2} + \hat{v}_{C2} + r_{C2}\hat{i}_{in} = \hat{v}_{C2} + r_{C2}C_2\frac{d\hat{v}_{C2}}{dt}, \\
\hat{i}_o &= \hat{i}_{L1},
\end{aligned} \tag{8.22}$$

where

$$\begin{aligned}
r_{e1} &= r_{L1} + r_{C1}, \\
r_{e2} &= r_{L2} + r_{C2} + Dr_{C1} + Dr_{ds1} + D'r_{ds2}, \\
V_{e1} &= V_o + (Dr_{L1} + r_{C1} + r_{ds1} - r_{ds2})I_{in}.
\end{aligned} \tag{8.23}$$

We present here only the set of transfer functions without the parasitic elements in order to verify whether the adding of the input filter would produce such anomalies, which would affect the control design or stability of the converter. The input dynamics of the ideal converter can be given by

$$\begin{aligned}
\Delta Z_{in-o} &= \left[s \left(s^2 + \frac{D^2L_1 + L_2}{L_1L_2C_1} \right) \right] / (C_2), \\
\Delta T_{oi-o} &= \frac{D}{L_1L_2C_1C_2}, \\
\Delta G_{ci-o} &= \frac{V_o}{L_2C_2} \left(s^2 + s \frac{DI_{in}}{V_oC_1} + \frac{1}{L_1C_1} \right),
\end{aligned} \tag{8.24}$$

and the output dynamics by

$$\begin{aligned}\Delta Y_{o-o} &= \frac{s}{L_1} \left(s^2 + \frac{C_1 + D^2 C_2}{L_2 C_1 C_2} \right), \\ \Delta G_{io-o} &= \frac{D}{L_1 L_2 C_1 C_2}, \\ \Delta G_{co-o} &= \frac{I_{in}}{L_1 C_1} \left(s^2 - s \frac{D V_o}{I_{in} L_2} + \frac{1}{L_2 C_2} \right).\end{aligned}\quad (8.25)$$

Δ in Eqs (8.24) and (8.25) denotes the determinant of the system and can be given by

$$\Delta = s^4 + s^2 \left(\frac{1}{L_1 C_1} + \frac{1}{L_2 C_2} + \frac{D^2}{L_2 C_1} \right) + \frac{1}{L_1 L_2 C_1 C_2}.\quad (8.26)$$

The adding of input filter changes naturally the converter to a fourth-order converter (cf. Eq. (8.26)) but the control-to-output-current transfer function (G_{co-o}) in Eq. (8.25) will also contain an RHP zero, which will limit the maximum control bandwidth to the frequency of the zero. The control-to-input-voltage transfer function (G_{ci-o}) in Eq. (8.24) does not contain any RHP zeros. This is a very good example of the necessity to perform the dynamic analysis fully without assuming anything based on the original converter.

The dynamic effect of the input filter on the converter dynamic behavior can also be solved by applying the technique of source interactions, which is described in detail in Chapter 2. The cascaded connection of the input filter (i.e., the source) and CF converter is shown in Figure 8.5. In this technique, we can apply directly the knowledge of the known transfer functions of the cascaded elements. As depicted in Figure 8.5, the variables at the interface of the converters (i.e., \hat{i}_s and \hat{v}_s) serve two different purposes depending on which of the cascaded elements are in question. The H -parameter sets of the cascaded elements are given in Eqs (8.26) and (8.27), which will clarify the above statement. The transfer functions in Eq. (8.27) are explicitly given in Eqs (8.14)–(8.16).

$$\begin{aligned}\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_s \end{bmatrix} &= \begin{bmatrix} Z_{in}^{LC} & T_{oi}^{LC} \\ G_{io}^{LC} & -Y_o^{LC} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_s \end{bmatrix}, \\ \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_s \end{bmatrix} &= \frac{\begin{bmatrix} (r_{L2} + sL_2)(1 + sr_{C2}C_2) & 1 + sr_{C2}C_2 \\ 1 + sr_{C2}C_2 & -sC_2 \end{bmatrix}}{s^2 L_2 C_2 + s(r_{L2} + r_{C2})C_2 + 1} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_s \end{bmatrix}.\end{aligned}\quad (8.27)$$

$$\begin{bmatrix} \hat{v}_s \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Z_{in-o}^{CF} & T_{oi-o}^{CF} & G_{ci-o}^{CF} \\ G_{io-o}^{CF} & -Y_{o-o}^{CF} & G_{co-o}^{CF} \end{bmatrix} \begin{bmatrix} \hat{i}_s \\ \hat{v}_o \\ \hat{d} \end{bmatrix}.\quad (8.28)$$

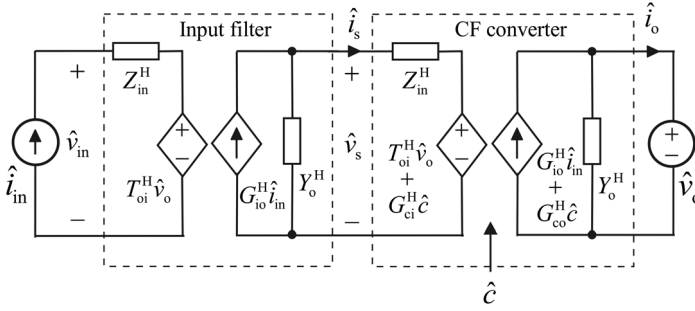


Figure 8.5 The cascaded connection of the input filter and the CF converter.

The set of the input-to-output transfer functions of the cascaded system can be given by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \frac{1 + Z_{in-o}^{CF} Y_{o-sci}^{LC} Z_{in}^{LC}}{1 + Y_o^{LC} Z_{in-o}^{CF}} Z_{in}^{LC} & \frac{T_{oi}^{LC}}{1 + Y_o^{LC} Z_{in-o}^{CF}} T_{oi-o}^{CF} & \frac{T_{oi}^{LC}}{1 + Y_o^{LC} Z_{in-o}^{CF}} G_{ci-o}^{CF} \\ \frac{G_{io-o}^{CF}}{1 + Y_o^{LC} Z_{in-o}^{CF}} G_{io}^{LC} & -\frac{1 + Y_o^{LC} Z_{in-oco}^{CF}}{1 + Y_o^{LC} Z_{in-o}^{CF}} Y_{o-o}^{CF} & \frac{1 + Y_o^{LC} Z_{in-\infty}^{CF}}{1 + Y_o^{LC} Z_{in-o}^{CF}} G_{co-o}^{CF} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \\ \hat{d} \end{bmatrix} \quad (8.29)$$

The set of cascaded transfer functions in Eq. (8.29) reveals that the original filter and converter transfer functions are affected through the output and input impedances of the cascaded elements as well as through their special impedance-like parameters defined as H -parameters in Eq. (8.2). The special parameters of the CF buck converter are given explicitly in Eq. (8.17). The special parameters for the input filter can be given by

$$\begin{aligned} Z_{in-oco}^{LC} &= \frac{1 + sr_{C2}C_2}{sC_2}, \\ Y_{o-sci}^{LC} &= \frac{1}{sL_2 + r_{L2}}. \end{aligned} \quad (8.30)$$

The appearing of the RHP zero in the output-current dynamics is the consequence of the interaction of the source output admittance (i.e., Y_o^{LC} in Eq. (8.27)) with the ideal input impedance of the converter (i.e., $Z_{in-\infty}^{CF}$ in Eq. (8.25)).

The practical analysis of the cascaded system in Figure 8.5 will be usually performed by means of the individual transfer functions of the subsystems and the set of transfer functions in (8.30) by utilizing a proper software package such as Matlab and its toolboxes.

8.2.1.2 Boost Converter

The power stage of the CF boost converter with the relevant components is given in Figure 8.6a. Its on-time and off-time power-stage structures are given in Figure 8.6b and c, respectively.

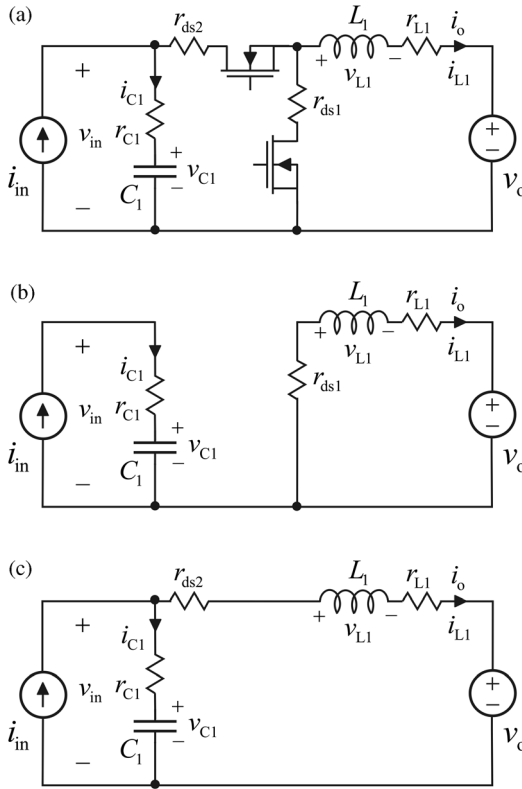


Figure 8.6 CF boost converter. (a) Basic power stage. (b) On-time power-stage structure. (c) Off-time power-stage structure.

According to Figure 8.6b, we can compute the on-time state-space equations to be

$$\begin{aligned}
 \frac{di_{L1}}{dt} &= -\frac{(r_{L1} + r_{ds1})}{L_1} i_{L1} - \frac{1}{L_1} v_o, \\
 \frac{dv_{C1}}{dt} &= \frac{1}{C_1} i_{in}, \\
 v_{in} &= v_{C1} + r_{C1} i_{in}, \\
 i_o &= i_{L1},
 \end{aligned} \tag{8.31}$$

and according to Figure 8.6c, we can compute the off-time state-space equations to be

$$\begin{aligned}
 \frac{di_{L1}}{dt} &= -\frac{(r_{L1} + r_{C1} + r_{ds2})}{L_1} i_{L1} + \frac{1}{L_1} v_{C1} + \frac{r_{C1}}{L_1} i_{in} - \frac{1}{L_1} v_o, \\
 \frac{dv_{C1}}{dt} &= -\frac{1}{C_1} i_{L1} + \frac{1}{C_1} i_{in}, \\
 v_{in} &= -r_{C1} i_{L1} + v_{C1} + r_{C1} i_{in}, \\
 i_o &= i_{L1}.
 \end{aligned} \tag{8.32}$$

The averaged state space can be computed based on Eqs (8.31) and (8.32) as discussed in Chapter 2. The averaging process yields the averaged state space

$$\begin{aligned}\frac{d\langle i_{L1} \rangle}{dt} &= -\frac{(r_{L1} + d'r_{C1} + dr_{ds1} + d'r_{ds2})}{L_1} \langle i_{L1} \rangle + \frac{d'}{L_1} \langle v_{C1} \rangle + \frac{d'r_{C1}}{L_1} \langle i_{in} \rangle - \frac{1}{L_1} \langle v_o \rangle, \\ \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{d'}{C_1} \langle i_{L1} \rangle + \frac{1}{C_1} \langle i_{in} \rangle, \\ \langle v_{in} \rangle &= -d'r_{C1} \langle i_{L1} \rangle + \langle v_{C1} \rangle + r_{C1} \langle i_{in} \rangle = \langle v_{C1} \rangle + r_{C1} C_1 \frac{d\langle v_{C1} \rangle}{dt}, \\ \langle i_o \rangle &= \langle i_{L1} \rangle,\end{aligned}\tag{8.33}$$

and the steady-state operating point

$$\begin{aligned}I_o &= I_{L1} = \frac{I_{in}}{D'}, \\ V_{in} &= V_{C1} = \frac{V_o}{D'} + \frac{r_{L1} + DD'r_{C1} + Dr_{ds1} + D'r_{ds2}}{D'^2} I_{in}.\end{aligned}\tag{8.34}$$

The linearized state space can be computed from Eq. (8.33) by applying the methods described in Chapter 2. This process yields

$$\begin{aligned}\frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1} \hat{i}_{L1} + \frac{D'}{L_1} \hat{v}_{C1} + \frac{D'r_{C1}}{L_1} \hat{i}_{in} - \frac{1}{L_1} \hat{v}_o - \frac{V_{e1}}{L_1} \hat{d}, \\ \frac{d\hat{v}_{C1}}{dt} &= -\frac{D'}{C_1} \hat{i}_{L1} + \frac{1}{C_1} \hat{i}_{in} + \frac{I_{in}}{D'C_1} \hat{d}, \\ \hat{v}_{in} &= \hat{v}_{C1} + r_{C1} C_1 \frac{d\hat{v}_{C1}}{dt}, \\ \hat{i}_o &= \hat{i}_{L1},\end{aligned}\tag{8.35}$$

where

$$\begin{aligned}r_{e1} &= r_{L1} + D'r_{C1} + Dr_{ds1} + D'r_{ds2}, \\ V_{e1} &= \frac{V_o}{D'} + \frac{r_{L1} + (D - D')r_{C1} + r_{ds1}}{D'^2} I_{in}.\end{aligned}\tag{8.36}$$

The set of transfer functions representing the input dynamics can be given by

$$\begin{aligned}\Delta Z_{in-o} &= \frac{1}{C_1} \left(s + \frac{r_{e1} - D'^2 r_{C1}}{L_1} \right) (1 + sr_{C1}C), \\ \Delta T_{oi-o} &= \frac{D'}{L_1 C_1} (1 + sr_{C1}C), \\ \Delta G_{ci-o} &= \frac{I_{in}}{D'C_1} \left(s + r_{e1} + \frac{D'^2 V_{e1}}{I_{in}} \right) (1 + sr_{C1}C),\end{aligned}\tag{8.37}$$

and the set of transfer functions representing the output dynamics by

$$\begin{aligned}\Delta Y_{o-o} &= \frac{s}{L_1}, \\ \Delta G_{io-o} &= \frac{D'}{L_1 C_1} (1 + sr_{C1} C_1), \\ \Delta G_{co-o} &= \frac{I_{in}}{L_1 C_1} \left(1 - s \frac{V_{e1} C_1}{I_{in}} \right).\end{aligned}\quad (8.38)$$

Δ in Eqs (8.37) and (8.38) denotes the determinant of the system and can be given by

$$\Delta = s^2 + s \frac{r_{e1}}{L_1} + \frac{D'^2}{L_1 C_1}. \quad (8.39)$$

The corresponding set of ideal impedance-like parameters can be given by

$$\begin{aligned}Z_{in-oco}^o &= \frac{1 + sr_{C1} C_1}{s C_1}, \\ Y_{o-sci} &= \frac{1}{s L_1 + r_{e1} - D'^2 r_{C1}}, \\ Z_{in-\infty} &= \frac{(V_{e1} + r_{C1} I_{in})(1 + sr_{C1} C_1)}{V_{e1} C_1 (s - (I_{in}/V_{e1} C_1))}, \\ T_{oi-\infty} &= -\frac{I_{in}}{D' V_{e1} C_1 (s - (I_{in}/V_{e1} C_1))}, \\ Y_{o-\infty} &= \frac{1}{s L_1 + (D'^2 V_{e1}/I_{in}) + r_{e1}}, \\ G_{io-\infty} &= \left[D' \left(r_{C1} + \frac{V_{e1}}{I_{in}} \right) \right] / \left(s L_1 + \frac{D'^2 V_{e1}}{I_{in}} + r_{e1} \right).\end{aligned}\quad (8.40)$$

The operating point given in Eq. (8.34) indicates that the converter has the steady-state property of a boost converter when the input–output modulo is considered in terms of input and output currents. The dynamic properties given in Eqs (8.38)–(8.40) are quite similar to the properties of the VF boost converter introduced in Chapter 3, that is, the resonant frequency is dependent on the complement of the duty ratio, the control-to-output-current transfer function (G_{co-o}) contains an RHP zero, and so on.

8.2.1.3 Noninverting Buck–Boost Converter

The power stage of the CF buck–boost converter with the relevant components is given in Figure 8.7a. Its on-time and off-time power-stage structures are given in Figure 8.7b and c, respectively.

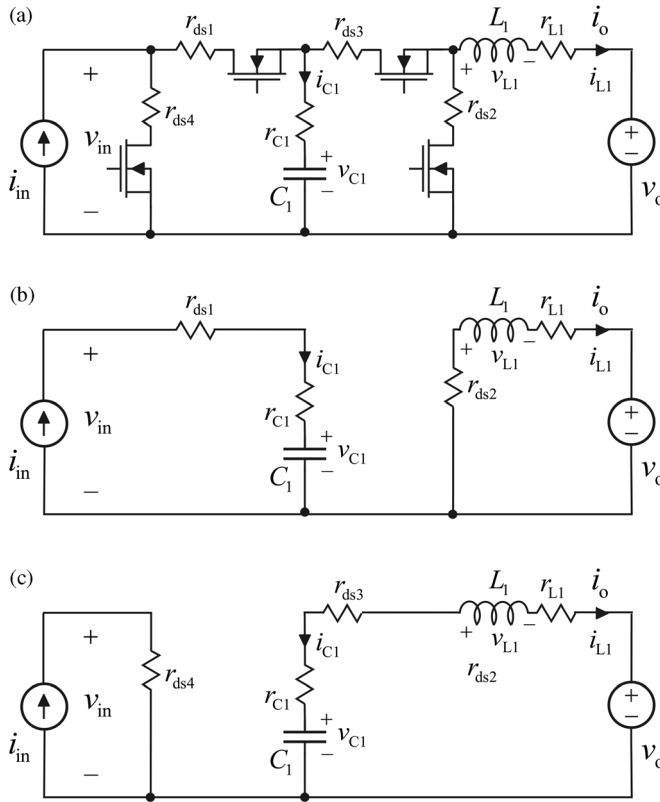


Figure 8.7 CF buck-boost converter. (a) Basic power stage. (b) On-time power stage-structure. (c) Off-time power stage structure.

According to Figure 8.7b, we can compute the on-time state-space equations to be

$$\begin{aligned}\frac{di_{L1}}{dt} &= -\frac{(r_{L1} + r_{ds2})}{L_1} i_{L1} - \frac{1}{L_1} v_o, \\ \frac{dv_{C1}}{dt} &= \frac{1}{C_1} i_{in}, \\ v_{in} &= v_{C1} + (r_{C1} + r_{ds1}) i_{in}, \\ i_o &= i_{L1},\end{aligned}\tag{8.41}$$

and according to Figure 8.7c, we can compute the on-time state-space equations to be

$$\begin{aligned}\frac{di_{L1}}{dt} &= -\frac{(r_{L1} + r_{C1} + r_{ds3})}{L_1} i_{L1} + \frac{1}{L_1} v_{C1} - \frac{1}{L_1} v_o, \\ \frac{dv_{C1}}{dt} &= -\frac{1}{C_1} i_{L1}, \\ v_{in} &= r_{ds4} i_{in}, \\ i_o &= i_{L1}.\end{aligned}\tag{8.42}$$

Based on Eqs. (8.41) and (8.42), the averaged state space can be given by

$$\begin{aligned}
 \frac{d\langle i_{L1} \rangle}{dt} &= -\left(\frac{r_{L1} + dr_{ds2} + d'r_{C1} + d'r_{ds3}}{L_1} \right) \langle i_{L1} \rangle + \frac{d'}{L_1} \langle v_{C1} \rangle - \frac{1}{L_1} \langle v_o \rangle, \\
 \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{d'}{C_1} \langle i_{L1} \rangle + \frac{d}{C_1} \langle i_{in} \rangle, \\
 \langle v_{in} \rangle &= d\langle v_{C1} \rangle + (dr_{C1} + dr_{ds1} + d'r_{ds4}) \langle i_{in} \rangle, \\
 \langle i_o \rangle &= \langle i_{L1} \rangle,
 \end{aligned} \tag{8.43}$$

and the corresponding operation point values by

$$\begin{aligned}
 I_o &= I_{L1} = \frac{D}{D'} I_{in}, \\
 V_{C1} &= \frac{V_o}{D'} + \frac{D}{D'^2} (r_{L1} + Dr_{ds2} + D'r_{C1} + D'r_{ds3}) I_{in}, \\
 V_{in} &= \frac{D}{D'} V_o + \frac{D^2}{D^2} \left(r_{L1} + \frac{D^2}{D} r_{ds1} + Dr_{ds2} + D'r_{ds3} + \frac{D'}{D^2} r_{ds4} + \frac{D'}{D} r_{C1} \right) I_{in}.
 \end{aligned} \tag{8.44}$$

The corresponding linearized state space can be given by

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1} \hat{i}_{L1} + \frac{D'}{L_1} \hat{v}_{C1} - \frac{1}{L_1} \hat{v}_o - \frac{V_{e1}}{L_1} \hat{d}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{D'}{C_1} \hat{i}_{L1} + \frac{D}{C_1} \hat{i}_{in} + \frac{I_{in}}{D'C_1} \hat{d}, \\
 \hat{v}_{in} &= D\hat{v}_{C1} + r_{e2} \hat{i}_{in} + V_{e2} \hat{d}, \\
 \hat{i}_o &= \hat{i}_{L1},
 \end{aligned} \tag{8.45}$$

where

$$\begin{aligned}
 r_{e1} &= r_{L1} + Dr_{ds2} + D'r_{C1} + D'r_{ds3}, \\
 r_{e2} &= Dr_{C1} + Dr_{ds1} + D'r_{ds4}, \\
 V_{e1} &= V_{C1} + \frac{D}{D'} (r_{ds2} - r_{ds3} - r_{C1}) I_{in}, \\
 V_{e2} &= V_{C1} + (r_{ds1} - r_{ds4} + r_{C1}) I_{in}.
 \end{aligned} \tag{8.46}$$

The set of transfer functions representing the input dynamics can be given by

$$\begin{aligned}\Delta Z_{\text{in-o}} &= s^2 + s\left(\frac{D^2}{r_{e2}C_1} + \frac{r_{e1}}{L_1}\right) + \frac{D^2r_{e2} + D^2r_{e1}}{r_{e2}L_1C_1}, \\ \Delta T_{\text{oi-o}} &= \frac{DD'}{L_1C_1}, \\ \Delta G_{\text{ci-o}} &= V_{e2}\left(s^2 + s\left(\frac{DI_{\text{in}}}{D'V_{e2}C_1} + \frac{r_{e1}}{L_1}\right) + \frac{D^2(D'V_{e2} + DV_{e1}) + Dr_{e1}I_{\text{in}}}{D'V_{e2}L_1C_1}\right),\end{aligned}\quad (8.47)$$

and the set of transfer functions representing the output dynamics by

$$\begin{aligned}\Delta Y_{\text{o-o}} &= \frac{s}{L_1}, \\ \Delta G_{\text{io-o}} &= \frac{DD'}{L_1C_1}, \\ \Delta G_{\text{co-o}} &= \frac{I_{\text{in}}}{L_1C_1}\left(1 - s\frac{V_{e1}C_1}{I_{\text{in}}}\right).\end{aligned}\quad (8.48)$$

Δ in Eqs (8.47) and (8.48) denotes the determinant of the system and can be given by

$$\Delta = s^2 + s\frac{r_{e1}}{L_1} + \frac{D^2}{L_1C_1}.\quad (8.49)$$

The corresponding set of ideal impedance-like parameters can be given by

$$\begin{aligned}Z_{\text{in-oco}}^{\text{o}} &= \frac{D^2 + sr_{e2}C_1}{sC_1}, \\ Y_{\text{o-sci}} &= (D^2 + sr_{e2}C_1)/r_{e2}L_1C_1s^2 + \left(s\left(\frac{D^2}{r_{e2}C_1} + \frac{r_{e1}}{L_1}\right) + \frac{D^2r_{e1} + D^2r_{e2}}{r_{e2}L_1C_1}\right), \\ Z_{\text{in-}\infty} &= \left[r_{e2}\left(s + \frac{D^2V_{e1} + DD'V_{e2} - r_{e2}I_{\text{in}}}{r_{e2}V_{e1}C_1}\right)\right] / \left[s - \frac{I_{\text{in}}}{V_{e1}C_1}\right], \\ T_{\text{oi-}\infty} &= -\left(\left[V_{e2}\left(s + \frac{DI_{\text{in}}}{D'V_{e2}C_1}\right)\right] / \left[V_{e1}\left(s - \frac{I_{\text{in}}}{V_{e1}C_1}\right)\right]\right), \\ Y_{\text{o-}\infty} &= \left(s + \frac{DI_{\text{in}}}{D'V_{e2}C_1}\right) / \\ &\quad \left(L_1\left(s^2 + s\left(\frac{DI_{\text{in}}}{D'V_{e2}C_1} + \frac{r_{e1}}{L_1}\right) + \frac{D^2(D'V_{e2} + DV_{e1}) + Dr_{e1}I_{\text{in}}}{D'V_{e2}L_1C_1}\right)\right), \\ G_{\text{io-}\infty} &= \left[r_{e2}\left(s + \frac{D(DV_{e1} + D'V_{e2}) - r_{e2}I_{\text{in}}}{r_{e2}V_{e1}C_1}\right)\right] / \\ &\quad \left[L_1\left(s^2 + s\left(\frac{DI_{\text{in}}}{D'V_{e2}C_1} + \frac{r_{e1}}{L_1}\right) + \frac{D^2(D'V_{e2} + DV_{e1}) + Dr_{e1}I_{\text{in}}}{D'V_{e2}L_1C_1}\right)\right].\end{aligned}\quad (8.50)$$

The operating point given in Eq. (8.46) indicates that the converter has the steady-state property of a buck–boost converter when the input–output modulo is considered in terms of input and output currents. The dynamic properties given in Eqs (8.47)–(8.50) are quite similar to the properties of the VF buck–boost converter introduced in Chapter 3, that is, the resonant frequency is dependent on the complement of the duty ratio, the control-to-output-current transfer function ($G_{c_{o-o}}$) contains an RHP zero, and so on.

Similarly as the CF buck converter, the CF buck–boost converter cannot be used without the input filter in practical applications due to the output capacitor of the practical current sources such as the photovoltaic generator [12]. We do not, however, perform the analysis in this book, because the topology is not relevant from the practical point of view.

8.2.1.4 CF Superbuck Converter

The power stage of the CF superbuck–boost converter with the relevant components is given in Figure 8.8a. Its on-time and off-time power-stage structures are given in Figure 8.8b and c, respectively. The dynamic modeling of the CF superbuck converter also is presented in Ref. [13], including the verification of the dynamic models and the operation in practical application in interfacing photovoltaic generator. We do not present here anymore all the details included in the modeling, which can be easily performed by means of Figure 8.8 and the instructions given in Chapter 2 and the examples in the previous sections.

The averaged state space of the CF superbuck converter can be given by

$$\begin{aligned}
 \frac{d\langle i_{L1} \rangle}{dt} &= -\frac{d(r_{C2} + r_d) + d'(r_{C1} + r_{ds1}) + r_{L1}}{L_1} \langle i_{L1} \rangle - \frac{d'r_{C1} - dr_{C2}}{L_1} \langle i_{L2} \rangle \\
 &\quad + \frac{d'}{L_1} \langle v_{C1} \rangle - \frac{d}{L_1} \langle v_{C2} \rangle + \frac{d'r_{C1}}{L_1} \langle i_{in} \rangle - \frac{dV_D}{L_1}, \\
 \frac{d\langle i_{L2} \rangle}{dt} &= -\frac{d'r_{C1} - dr_{C2}}{L_2} \langle i_{L1} \rangle - \frac{r_{C1} + r_{C2} + r_{L2}}{L_2} \langle i_{L2} \rangle + \frac{1}{L_2} \langle v_{C1} \rangle \\
 &\quad + \frac{1}{L_2} \langle v_{C2} \rangle + \frac{r_{C1}}{L_2} \langle i_{in} \rangle - \frac{1}{L_2} \langle v_o \rangle, \\
 \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{d'}{C_1} \langle i_{L1} \rangle - \frac{1}{C_1} \langle i_{L2} \rangle + \frac{1}{C_1} \langle i_{in} \rangle, \\
 \frac{d\langle v_{C2} \rangle}{dt} &= \frac{d}{C_2} \langle i_{L1} \rangle - \frac{1}{C_2} \langle i_{L2} \rangle, \\
 \langle v_{in} \rangle &= -d'r_{C1} \langle i_{L1} \rangle - r_{C1} \langle i_{L2} \rangle + \langle v_{C1} \rangle + r_{C1} \langle i_{in} \rangle, \\
 \langle i_o \rangle &= \langle i_{L2} \rangle,
 \end{aligned} \tag{8.51}$$

the operating point parameter values by

$$\begin{aligned}
 I_{L1} &= I_{in}, \\
 I_o &= I_{L2} = DI_{in}, \\
 V_{in} &= V_{C1} = D(V_o + V_D) + (DD'r_{C2} - D^2r_{C1} + Dr_d + D'r_{ds1} + r_{L1} + D^2r_{L2})I_{in}, \\
 V_{C2} &= D'V_o - DV_D - (DD'r_{C2} - D^2r_{C1} + Dr_d + D'r_{ds1} + r_{L1} - DD'r_{L2})I_{in},
 \end{aligned} \tag{8.52}$$

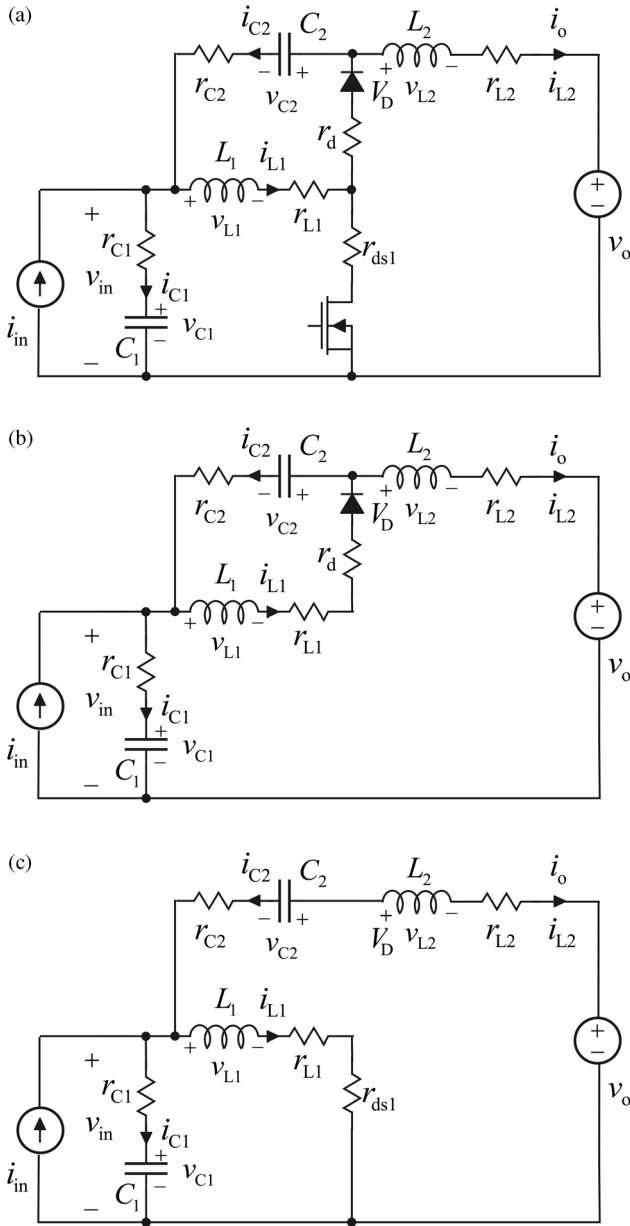


Figure 8.8 CF super-buck converter. (a) Basic power stage. (b) On-time power stage structure. (c) Off-time power stage structure. *Source:* Leppäaho 2011. Reproduced with permission of IEEE.

and the corresponding linearized state space by

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1}\hat{i}_{L1} - \frac{e_{e2}}{L_1}\hat{i}_{L2} + \frac{D'}{L_1}\hat{v}_{C1} - \frac{D}{L_1}\hat{v}_{C2} + \frac{D'r_{C1}}{L_1}\hat{i}_{in} - \frac{V_{e1}}{L_1}\hat{d}, \\
 \frac{d\hat{i}_{L2}}{dt} &= -\frac{r_{e2}}{L_2}\hat{i}_{L1} - \frac{r_{e3}}{L_2}\hat{i}_{L2} + \frac{1}{L_2}\hat{v}_{C1} + \frac{1}{L_2}\hat{v}_{C2} + \frac{r_{C1}}{L_2}\hat{i}_{in} - \frac{\hat{v}_o}{L_2} + \frac{V_{e2}}{L_2}\hat{d}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{D'}{C_1}\hat{i}_{L1} - \frac{1}{C_1}\hat{i}_{L2} + \frac{1}{C_1}\hat{i}_{in} + \frac{I_{in}}{C_1}\hat{d}, \\
 \frac{d\hat{v}_{C2}}{dt} &= \frac{D}{C_2}\hat{i}_{L1} - \frac{1}{C_2}\hat{i}_{L2} + \frac{I_{in}}{C_2}\hat{d}, \\
 \hat{v}_{in} &= \hat{v}_{C1} + r_{C1}C_1\frac{d\hat{v}_{C1}}{dt}, \\
 \hat{i}_o &= \hat{i}_{L2},
 \end{aligned} \tag{8.53}$$

where

$$\begin{aligned}
 r_{e1} &= D'(r_{C1} + r_{ds1}) + D(r_{C2} + r_d) + r_{L1}, \\
 r_{e2} &= D'r_{C1} - Dr_{C2}, \\
 r_{e3} &= r_{C1} + r_{C2} + r_{L2}, \\
 V_{e1} &= V_o + V_D + (Dr_{L2} + D'r_{C2} - Dr_{C1} + r_d - r_{ds1})I_{in}, \\
 V_{e2} &= (r_{C1} + r_{C2})I_{in}.
 \end{aligned} \tag{8.54}$$

The set of transfer functions representing the output dynamics can be given by

$$\begin{aligned}
 \Delta Z_{in-o} &= \frac{1}{C_1}(s^3 + s^2 \frac{L_1(r_{e3} - r_{C1}) + L_2(r_{e1} - D^2r_{C1})}{L_1L_2} + \\
 &\quad s \frac{L_1 + D^2L_2 + (r_{e1}(r_{e3} - r_{C1}) - D^2r_{e3}r_{C1} - r_{e2}^2 + 2D'r_{e2}r_{C1})C_2}{L_1L_2C_2} \\
 &\quad + \frac{r_{e1} + 2Dr_{e2} + D^2r_{e3} - r_{C1}}{L_1L_2C_2})(1 + sr_{C1}C_1), \\
 \Delta T_{oi-o} &= \frac{1}{L_2C_1} \left(s^2 + s \frac{r_{e1} - D'r_{e2}}{L_1} + \frac{D}{L_1C_2} \right) (1 + sr_{C1}C_1), \\
 \Delta G_{ci-o} &= (s^3 \frac{I_{in}}{C_1} + s^2 \frac{L_1(I_{in}r_{e3} - V_{e2}) + L_2(I_{in}r_{e1} + D'V_{e1})}{L_1L_2C_1} + \\
 &\quad s \frac{L_2DI_{in} + C_2(V_{e1}(D'r_{e3} - r_{e2}) + V_{e2}(D'r_{e2} - r_{e1}) + I_{in}(r_{e1}r_{e2} - r_{e2}^2))}{L_1L_2C_1C_2} \\
 &\quad + \frac{V_{e1} - DV_{e2} + I_{in}(r_{e2} + Dr_{e3})}{L_1L_2C_1C_2})(1 + sr_{C1}C_1),
 \end{aligned} \tag{8.55}$$

and the set of the transfer functions representing the output dynamics by

$$\begin{aligned}\Delta Y_{o-o} &= \frac{s}{L_2} \left(s^2 + s \frac{r_{e1}}{L_1} + \frac{D^2 C_1 + D^2 C_2}{L_1 C_1 C_2} \right), \\ \Delta G_{i_{o-o}} &= \frac{1}{L_2 C_1} \left(s^2 + s \frac{r_{e1} - D r_{e2}}{L_1} + \frac{D}{L_1 C_2} \right) (1 + s r_{C1} C_1), \\ \Delta G_{c_{o-o}} &= s^3 \frac{V_{e2}}{L_2} + s^2 \frac{(V_{e1} r_{e2} + V_{e2} r_{e1}) C_1 C_2 + I_{in} L_1 (C_1 + C_2)}{L_1 L_2 C_1 C_2} + \\ &\quad \frac{(D(DV_{e2} - V_{e1}) + I_{in}(r_{e1} + D r_{e2})) C_1}{s \frac{(D(V_{e1} + D' V_{e2}) + I_{in}(r_{e1} - D' r_{e2})) C_2}{L_1 L_2 C_1 C_2}} + \frac{I_{in}}{L_1 L_2 C_1 C_2}.\end{aligned}\tag{8.56}$$

Δ in Eqs (8.55) and (8.56) denotes the determinant of the system and can be given by

$$\begin{aligned}\Delta &= s^4 + s^3 \frac{L_1 r_{e3} + L_2 r_{e1}}{L_1 L_2} + s^2 \frac{L_1 (C_1 + C_2) + L_2 (D^2 C_1 + D^2 C_2) + C_1 C_2 (r_{e1} r_{e3} - r_{e2}^2)}{L_1 L_2 C_1 C_2} + \\ &\quad s \frac{(r_{e1} + 2D r_{e2} + D^2 r_{e3}) C_1 + (r_{e1} - 2D' r_{e2} + D'^2 r_{e3}) C_2}{L_1 L_2 C_1 C_2} + \frac{1}{L_1 L_2 C_1 C_2}.\end{aligned}\tag{8.57}$$

The complex conjugate roots of the determinant can be approximated by neglecting the parasitic elements to be

$$f_{p1} \approx \frac{1}{2\pi} \sqrt{\frac{1}{L_1 (C_1 + C_2)}}, \quad f_{p2} \approx \frac{1}{2\pi} \sqrt{\frac{C_1 + C_2}{L_2 C_1 C_2}}.\tag{8.58}$$

The neglecting of the parasitic elements in the numerator of the control-to-output transfer functions ($G_{c_{o-o}}$) in Eq. (8.56) reveals that the output control dynamics can contain a complex conjugate RHP zero pair approximately at $1/(2\pi\sqrt{L_1(C_1 + C_2)})$ (cf. Eq. (8.60)), which is quite close to the LHP pole pair (f_{p1}) in Eq. (8.58). The appearance of the RHP zero can be, however, eliminated by selecting the sizes of the capacitors in such a way that $D'_{\max} C_2 - D_{\max} C_1 > 0$, where D_{\max} denotes the maximum value of the duty ratio within the practical operating range. This is quite the same phenomenon as encountered in the VF superbuck converter but in terms of inductor values (cf. Chapter 3).

$$G_{c_{o-o}}^{\text{Num}} \approx s^2 + s \frac{V_o (D' C_2 - D C_1)}{I_{in} L_1 (C_1 + C_2)} + \frac{1}{L_1 (C_1 + C_2)}.\tag{8.59}$$

The neglecting of the parasitic elements in the numerator of the control-to-input transfer function ($G_{c_{i-o}}$) yields

$$G_{c_{i-o}}^{\text{Num}} = \frac{I_{in}}{C_1} \left(s^3 + s^2 \frac{D' V_o}{I_{in} L_1} + s \frac{D}{L_1 C_2} + \frac{V_o}{I_{in} L_1 L_2 C_2} \right).\tag{8.60}$$

By applying Routh–Hurwitz test to the third-order polynomial in Eq. (8.60), we find out that there can be at least one RHP root because of the change of sign in the first row of Routh's array. In reality, the parasitic elements may prevent the

RHP zero to appear, but it is highly recommended to verify the real situation due to its effect on the control design. The feedback control of the input voltage is the most often utilized control method in the renewable energy applications.

The corresponding set of ideal impedance-like parameters neglecting the parasitic elements can be given by

$$\begin{aligned}
 Z_{in-oco}^o &= \left(s^2 + \frac{D^2}{L_1 C_2} \right) / \left(C_1 s \left(s^2 + \frac{D^2 C_1 + D^2 C_2}{L_1 C_1 C_2} \right) \right), \\
 Y_{o-sci} &= \left(s^2 + \frac{D^2}{L_1 C_2} \right) / \left(L_2 s \left(s^2 + \frac{L_1 + D^2 L_2}{L_1 L_2 C_2} \right) \right), \\
 Z_{in-\infty} &= \frac{1}{C_1 + C_2} \cdot \left[\left(s - \frac{D V_o}{I_{in} L_1} \right) / \left(s^2 + s \frac{V_o (D' C_2 - D C_1)}{I_{in} L_1 (C_1 + C_2)} + \frac{1}{L_1 (C_1 + C_2)} \right) \right], \\
 T_{oi-\infty} &= \frac{C_2}{C_1 + C_2} \cdot \left[\left(s^2 + s \frac{D' V_o}{I_{in} L_1 C_2} + \frac{D}{L_1 C_2} \right) / \left(s^2 + s \frac{(D' C_2 - D C_1) V_o}{I_{in} L_1 (C_1 + C_2)} + \frac{1}{L_1 (C_1 + C_2)} \right) \right], \\
 Y_{o-\infty} &= \frac{1}{L_2} \cdot \left[\left(s^2 + s \frac{D' V_o}{L_1 I_{in}} + \frac{D D'}{L_1 C_2} \right) / \left(s^3 + s^2 \frac{D' V_o}{I_{in} L_1} + s \frac{D}{L_1 C_2} + \frac{V_o}{I_{in} L_1 L_2 C_2} \right) \right], \\
 G_{io-\infty} &= -\frac{1}{L_2 C_2} \cdot \left[\left(s - \frac{D V_o}{I_{in} L_1} \right) / \left(s^3 + s^2 \frac{D' V_o}{I_{in} L_1} + s \frac{D}{L_1 C_2} + \frac{V_o}{I_{in} L_1 L_2 C_2} \right) \right].
 \end{aligned} \tag{8.61}$$

$$\begin{aligned}
 Z_{in-\infty}^c &= \frac{1}{C_1 + C_2} \cdot \left[\left(s - \frac{D U_o}{I_{in} L_1} \right) / \left(s^2 + s \frac{U_o (D' C_2 - D C_1)}{I_{in} L_1 (C_1 + C_2)} + \frac{1}{L_1 (C_1 + C_2)} \right) \right], \\
 T_{oi-\infty}^c &= \frac{C_2}{C_1 + C_2} \cdot \left[\left(s^2 + s \frac{D' U_o}{L_1 C_2 I_{in}} + \frac{D}{L_1 C_2} \right) / \left(s^2 + s \frac{(D' C_2 - D C_1) U_o}{I_{in} L_1 (C_1 + C_2)} + \frac{1}{L_1 (C_1 + C_2)} \right) \right], \\
 Y_{o-\infty}^c &= \frac{1}{L_2} \cdot \left[\left(s^2 + s \frac{D' U_o}{L_1 I_{in}} + \frac{D D'}{L_1 C_2} \right) / \left(s^3 + s^2 \frac{D' U_o}{L_1 I_{in}} + s \frac{D}{L_1 C_2} + \frac{U_o}{L_1 L_2 C_2 I_{in}} \right) \right], \\
 G_{io-\infty}^c &= -\frac{1}{L_2 C_2} \cdot \left[\left(s - \frac{D U_o}{L_1 I_{in}} \right) / \left(s^3 + s^2 \frac{D' U_o}{L_1 I_{in}} + s \frac{D}{L_1 C_2} + \frac{U_o}{L_1 L_2 C_2 I_{in}} \right) \right].
 \end{aligned} \tag{8.62}$$

The operating point variables in Eq. (8.52) show that the modulo of the converter is D . Therefore, the converter is a buck-type converter. The existence of RHP zeros in the higher order converters is quite common as demonstrated in Chapter 3. Therefore, the performing of the full-scale dynamic analysis is actually quite mandatory for guaranteeing the product quality.

8.2.2 Input Capacitor-Based Converters

As discussed in Chapter 7, the other method to produce CF converters is to use the well-known VF power stages and add a capacitor at the input terminal of the converter for satisfying the terminal constraints stipulated by a current source as

an input source [14,15]. Applying duality transformation will produce a CF converter having similar steady-state and dynamic properties as the original VF converter has, as explicitly demonstrated in Section 8.2.1. The input capacitor-based CF converters will actually have the steady-state and dynamic properties as the dual of the VF converters [15]. In addition, if the gate signals of the active switches are maintained as they are in the corresponding VF converter, then the duty ratio has to be decremented for increasing the output variables of the CF converter [15,16]. We will provide the dynamic models for the buck-, boost-, and noninverted buck–boost-type power stages in the subsequent sections. We will name those converters based on what their power stages are known in voltage domain.

8.2.2.1 Buck Power-Stage Converter

The power stage of the CF buck power-stage converter with the relevant components is given in Figure 8.9a. Its on-time and off-time power-stage structures are given in Figure 8.9b and c, respectively. (Note: The switch control scheme is maintained as it is in the VF buck converter). The dynamic modeling of the buck power-stage converter is also presented in Refs [8,15], including the verification of the dynamic models and the operation in practical application in interfacing photovoltaic generator. We do not present here anymore all the

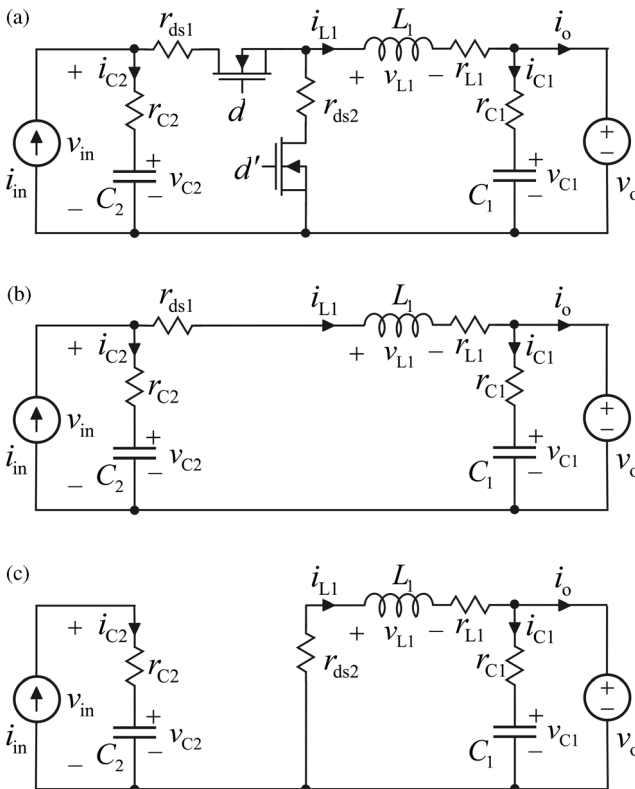


Figure 8.9 CF buck power-stage converter. (a) Basic power stage. (b) On-time power-stage structure. (c) Off-time power-stage structure.

details included in the modeling, which can be easily performed by means of Figure 8.9, the instructions given in Chapter 2, and the examples in the previous sections.

The average state space and the operating point can be given by

$$\begin{aligned}
 \frac{d\langle i_{L1} \rangle}{dt} &= -\frac{r_{L1} + dr_{ds1} + d'r_{ds2} + dr_{C2}}{L_1} \langle i_{L1} \rangle + \frac{d}{L_1} \langle v_{C2} \rangle + \frac{dr_{C2}}{L_1} \langle i_{in} \rangle - \frac{1}{L_1} \langle v_o \rangle, \\
 \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_o \rangle, \\
 \frac{d\langle v_{C2} \rangle}{dt} &= -\frac{d}{C_2} \langle i_{L1} \rangle + \frac{1}{C_2} \langle i_{in} \rangle, \\
 \langle v_{in} \rangle &= -d\langle i_{L1} \rangle + \langle v_{C2} \rangle + r_{C2} \langle i_{in} \rangle = \langle v_{C2} \rangle + r_{C2}C_2 \frac{d\langle v_{C2} \rangle}{dt}, \\
 \langle i_o \rangle &= \langle i_{L1} \rangle + \frac{1}{r_{C2}} \langle v_{C2} \rangle - \frac{1}{r_{C2}} \langle v_o \rangle,
 \end{aligned} \tag{8.63}$$

and

$$\begin{aligned}
 V_{in} = V_{C2} &= \frac{V_o}{D} + \frac{r_{L1} + Dr_{ds1} + D'r_{ds2} + DD'r_{C2}}{D^2} I_{in}, \\
 I_o &= I_{L1} = \frac{I_{in}}{D}.
 \end{aligned} \tag{8.64}$$

The corresponding linearized state space can be given by

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1} \hat{i}_{L1} + \frac{D}{L_1} \hat{v}_{C2} + \frac{dr_{C2}}{L_1} \hat{i}_{in} - \frac{1}{L_1} \hat{v}_o + \frac{V_{e1}}{L_1} \hat{d}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{r_{C1}C_1} \hat{v}_{C1} + \frac{1}{r_{C1}C_1} \hat{v}_o, \\
 \frac{d\hat{v}_{C2}}{dt} &= -\frac{D}{C_2} \hat{i}_{L1} + \frac{1}{C_2} \hat{i}_{in} - \frac{I_{in}}{DC_2} \hat{d}, \\
 \hat{v}_{in} &= \hat{v}_{C2} + r_{C2}C_2 \frac{d\hat{v}_{C2}}{dt}, \\
 \hat{i}_o &= \hat{i}_{L1} + \frac{1}{r_{C1}} \hat{v}_{C1} - \frac{1}{r_{C1}} \hat{v}_o,
 \end{aligned} \tag{8.65}$$

where

$$\begin{aligned}
 r_{e1} &= r_{L1} + Dr_{ds1} + D'r_{ds2} + Dr_{C2}, \\
 V_{e1} &= \frac{V_o}{D} + \frac{r_{L1} + r_{ds2}}{D^2} I_{in}.
 \end{aligned} \tag{8.66}$$

The set of transfer functions representing the input dynamics of the converter can be given by

$$\begin{aligned}\Delta Z_{\text{in-o}} &= \left(s + \frac{r_{e1} - D^2 r_{C2}}{L_1 C_2} \right) (1 + sr_{C2} C_2), \\ \Delta T_{\text{oi-o}} &= \frac{D}{L_1 C_2} (1 + sr_{C2} C_2), \\ \Delta G_{\text{ci-o}} &= -\frac{I_{\text{in}}}{DC_2} \left(s + \frac{D^2 V_{e1} + r_{e1} I_{\text{in}}}{I_{\text{in}} L_1} \right) (1 + sr_{C2} C_2),\end{aligned}\quad (8.67)$$

and the set of transfer functions representing the output dynamics by

$$\begin{aligned}Y_{\text{o-o}} &= \frac{s}{L_1 (s^2 + s(r_{e1}/L_1) + (D^2/L_1 C_2))} + \frac{1 + sr_{C1} C_1}{s C_1}, \\ \Delta G_{\text{io-o}} &= \frac{D}{L_1 C_2} (1 + sr_{C2} C_2), \\ \Delta G_{\text{co-o}} &= \frac{V_{e1}}{L_1} \left(s - \frac{I_{\text{in}}}{V_{e1} C_2} \right).\end{aligned}\quad (8.68)$$

Δ in Eqs (8.67) and (8.68) denotes the determinant of the system and can be given by

$$\Delta = s^2 + s \frac{r_{e1}}{L_1} + \frac{D^2}{L_1 C_2}. \quad (8.69)$$

The special parameters can be given by

$$\begin{aligned}Z_{\text{in-oco}}^{\text{o}} &= \left[\left(s^2 + s \frac{r_{e1} + r_{C1} - D^2 r_{C2}}{L_1} + \frac{1}{L_1 C_1} \right) (1 + sr_{C2} C_2) \right] / \\ &\quad \left[s C_2 \left(s^2 + s \frac{r_{e1} + r_{C1}}{L_1} + \frac{C_2 + D^2 C_1}{L_1 C_1 C_2} \right) \right], \\ Y_{\text{o-sci}} &= \frac{1}{sL_1 + r_{e1} - D^2 r_{C2}} + \frac{sC_1}{1 + sr_{C1} C_1}, \\ Z_{\text{in-}\infty} &= \frac{(V_{e1} + r_{C2} I_{\text{in}})(1 + sr_{C2} C_2)}{sV_{e1} C_2 - I_{\text{in}}}, \\ T_{\text{oi-}\infty} &= -\frac{C_1 (s^2 L_1 I_{\text{in}} + s(D^2 V_{e1} + (r_{e1} + r_{C1}) I_{\text{in}}) + I_{\text{in}})(1 + sr_{C2} C_2)}{s^2 D V_{e1} r_{C1} C_1 C_2 + sD(V_{e1} C_2 - r_{C2} I_{\text{in}} C_1) - D I_{\text{in}}}, \\ Y_{\text{o-}\infty} &= \frac{1}{sL_1 + r_{e1} + (D^2 V_{e1}/I_{\text{in}})} + \frac{sC_1}{1 + sr_{C1} C_1}, \\ G_{\text{io-}\infty} &= \left[D \left(r_{C2} + \frac{V_{e1}}{I_{\text{in}}} \right) \right] / \left[sL_1 + r_{e1} + \frac{D^2 V_{e1}}{I_{\text{in}}} \right].\end{aligned}\quad (8.70)$$

According to the operating point, it may be obvious that the duty ratio has to be decreased for increasing the output variables. The negative low-frequency sign of the control-related transfer functions in Eqs. (8.67) and (8.68) indicates that the

corresponding feedback signal and its reference have to be interchanged for ensuring stable operation. In addition, the control-to-output-current transfer function (G_{co-o}) contains an RHP zero approximately at $I_{in}/V_{in}C_1$, which has to be taken into consideration when designing the controller. The appearing of the RHP zero was already detected in late 1970s [17] when the buck power-stage converter was applied in PV applications. The RHP zero locates at very low frequency, and therefore, the control bandwidth of the output-side feedback controller would be also very low, and usually not satisfying any control performance requirements. In the renewable energy applications, the input-side feedback control would anyway dominate, and the control-to-input transfer function (G_{ci-o}) does not contain RHP zeros.

The inverting of the gate drive signals in Figure 8.9 (i.e., the on-time and off-time subcircuits are interchanged) would yield the averaged state space, operating point, and linearized state space as follows:

$$\begin{aligned}
 \frac{d\langle i_{L1} \rangle}{dt} &= -\frac{r_{L1} + d'r_{ds1} + dr_{ds2} + d'r_{C2}}{L_1} \langle i_{L1} \rangle + \frac{d'}{L_1} \langle v_{C2} \rangle + \frac{d'r_{C2}}{L_1} \langle i_{in} \rangle - \frac{1}{L_1} \langle v_o \rangle, \\
 \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_o \rangle, \\
 \frac{d\langle v_{C2} \rangle}{dt} &= -\frac{d'}{C_2} \langle i_{L1} \rangle + \frac{1}{C_2} \langle i_{in} \rangle, \\
 \langle v_{in} \rangle &= -d' \langle i_{L1} \rangle + \langle v_{C2} \rangle + r_{C2} \langle i_{in} \rangle = \langle v_{C2} \rangle + r_{C2}C_2 \frac{d\langle v_{C2} \rangle}{dt}, \\
 \langle i_o \rangle &= \langle i_{L1} \rangle + \frac{1}{r_{C1}} \langle v_{C1} \rangle - \frac{1}{r_{C1}} \langle v_o \rangle.
 \end{aligned} \tag{8.71}$$

$$V_{in} = V_{C2} = \frac{V_o}{D'} + \frac{r_{L1} + D'r_{ds1} + Dr_{ds2} + DD'r_{C2}}{D'^2} I_{in}, \tag{8.72}$$

$$I_o = I_{L1} = \frac{I_{in}}{D'},$$

and

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1} \hat{i}_{L1} + \frac{D'}{L_1} \hat{v}_{C2} + \frac{d'r_{C1}}{L_1} \hat{i}_{in} - \frac{1}{L_1} \hat{v}_o - \frac{V_{e1}}{L_1} \hat{d}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{D'}{C_1} \hat{i}_{L1} + \frac{1}{C_1} \hat{i}_{in} + \frac{I_{in}}{D'C_1} \hat{d}, \\
 \frac{d\hat{v}_{C2}}{dt} &= -\frac{1}{r_{C2}C_2} \hat{v}_{C2} + \frac{1}{r_{C2}C_2} \hat{v}_o, \\
 \hat{v}_{in} &= \hat{v}_{C1} + r_{C1}C_1 \frac{d\hat{v}_{C1}}{dt}, \\
 \hat{i}_o &= \hat{i}_{L1} + \frac{1}{r_{C2}} \hat{v}_{C2} - \frac{1}{r_{C2}} \hat{v}_o,
 \end{aligned} \tag{8.73}$$

where

$$\begin{aligned} r_{e1} &= r_{L1} + D'r_{ds1} + Dr_{ds2} + D'r_{C2}, \\ V_{e1} &= \frac{V_o}{D} + \frac{r_{L1} + r_{ds2}}{D^2} I_{in}. \end{aligned} \quad (8.74)$$

The set of transfer function representing the input dynamics can also be given by

$$\begin{aligned} \Delta Z_{in-o} &= \frac{1}{C_2} \left(s + \frac{r_{e1} - D^2 r_{C2}}{L_1} \right) (1 + sr_{C2}C_2), \\ \Delta T_{oi-o} &= \frac{D'}{L_1 C_2} (1 + sr_{C2}C_2), \\ \Delta G_{ci-o} &= \frac{I_{in}}{D' C_2} \left(s + \frac{D^2 V_{e1} + r_{e1} I_{in}}{I_{in} L_1} \right) (1 + sr_{C2}C_2), \end{aligned} \quad (8.75)$$

and the set of transfer functions representing the output dynamics by

$$\begin{aligned} Y_{o-o} &= \frac{s}{L_1 (s^2 + s(r_{e1}/L_1) + (D^2/L_1 C_2))} + \frac{1 + sr_{C1}C_1}{sC_1}, \\ \Delta G_{io-o} &= \frac{D'}{L_1 C_2} (1 + sr_{C2}C_2), \\ \Delta G_{co-o} &= -\frac{V_{e1}}{L_1} \left(s - \frac{I_{in}}{V_{e1} C_2} \right), \end{aligned} \quad (8.76)$$

where Δ denotes the denominator of the transfer functions and can be given by

$$\Delta = s^2 + s \frac{r_{e1}}{L_1} + \frac{D^2}{L_1 C_2}. \quad (8.77)$$

The set of special parameters can be given by

$$\begin{aligned} Z_{in-oco}^o &= \left[(s^2 + s \frac{r_{e1} + r_{C1} - D^2 r_{C2}}{L_1} + \frac{1}{L_1 C_1}) (1 + sr_{C2}C_2) \right] / \\ &\quad \left[sC_2 \left(s^2 + s \frac{r_{e1} + r_{C1}}{L_1} + \frac{C_2 + D^2 C_1}{L_1 C_1 C_2} \right) \right], \\ Y_{o-sci} &= \frac{1}{sL_1 + r_{e1} - D^2 r_{C2}} + \frac{sC_1}{1 + sr_{C1}C_1}, \\ Z_{in-\infty} &= \frac{(V_{e1} + r_{C2} I_{in}) (1 + sr_{C2}C_2)}{sV_{e1} C_2 - I_{in}}, \\ T_{oi-\infty} &= -\frac{C_1 (s^2 L_1 I_{in} + s(D^2 V_{e1} + (r_{e1} + r_{C1}) I_{in}) + I_{in}) (1 + sr_{C2}C_2)}{D' (s^2 V_{e1} r_{C1} C_1 C_2 + s(V_{e1} C_2 - r_{C1} I_{in} C_2) - I_{in})}, \\ Y_{o-\infty} &= \frac{1}{sL_1 + r_{e1} + (D^2 V_{e1}/I_{in})} + \frac{sC_1}{1 + sr_{C1}C_1}, \\ G_{io-\infty} &= \left[D' \left(r_{C2} + \frac{V_{e1}}{I_{in}} \right) \right] / \left[sL_1 + r_{e1} + \frac{D^2 V_{e1}}{I_{in}} \right]. \end{aligned} \quad (8.78)$$

When the gate signals of the active switches are inverted, the operating point in Eq. (8.72) indicates that the converter is a boost-type converter. In addition, the control-related transfer functions do not anymore have negative low-frequency sign, which means that the conventional feedback arrangement works. Actually, the sets given in Eqs (8.72)–(8.78) can be derived from the corresponding sets of the original buck power-stage converter by substituting duty ratio by its complement or vice versa, and changing the sign of the control-related transfer functions. It should also be noted that the signs of the perturbed duty ratio in Eq. (8.73) have been changed (i.e., multiplied by -1) compared to Eq. (8.65).

The output capacitor (C_1) in Figure 8.9 may not be used, and therefore, we also present the same sets excluding the operating point as above in case of non-inverted gate signals when the output capacitor is omitted:

$$\begin{aligned}\frac{d\langle i_{L1} \rangle}{dt} &= -\frac{r_{L1} + dr_{ds1} + d'r_{ds2} + dr_{C2}}{L_1} \langle i_{L1} \rangle + \frac{d}{L_1} \langle v_{C2} \rangle + \frac{dr_{C2}}{L_1} \langle i_{in} \rangle - \frac{1}{L_1} \langle v_o \rangle, \\ \frac{d\langle v_{C2} \rangle}{dt} &= -\frac{d}{C_2} \langle i_{L1} \rangle + \frac{1}{C_2} \langle i_{in} \rangle, \\ \langle v_{in} \rangle &= -dr_{C2} \langle i_{L1} \rangle + \langle v_{C2} \rangle + r_{C2} \langle i_{in} \rangle = \langle v_{C2} \rangle + r_{C2} C_2 \frac{d\langle v_{C2} \rangle}{dt}, \\ \langle i_o \rangle &= \langle i_{L1} \rangle.\end{aligned}\tag{8.79}$$

$$\begin{aligned}\frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1} \hat{i}_{L1} + \frac{D}{L_1} \hat{v}_{C2} + \frac{dr_{C2}}{L_1} \hat{i}_{in} - \frac{1}{L_1} \hat{v}_o + \frac{V_{e1}}{L_1} \hat{d}, \\ \frac{d\hat{v}_{C2}}{dt} &= -\frac{D}{C_2} \hat{i}_{L1} + \frac{1}{C_2} \hat{i}_{in} - \frac{I_{in}}{DC_2} \hat{d}, \\ \hat{v}_{in} &= \hat{v}_{C2} + r_{C2} C_2 \frac{d\hat{v}_{C2}}{dt}, \\ \hat{i}_o &= \hat{i}_{L1},\end{aligned}\tag{8.80}$$

where

$$\begin{aligned}r_{e1} &= r_{L1} + Dr_{ds1} + D'r_{ds2} + Dr_{C2}, \\ V_{e1} &= \frac{V_o}{D} + \frac{r_{L1} + r_{ds2}}{D^2} I_{in}.\end{aligned}\tag{8.81}$$

$$\begin{aligned}\Delta Z_{in-o} &= \left(s + \frac{r_{e1} - D^2 r_{C2}}{L_1 C_2} \right) (1 + sr_{C1} C_2), \\ \Delta T_{oi-o} &= \frac{D}{L_1 C_2} (1 + sr_{C2} C_2),\end{aligned}\tag{8.82}$$

$$\Delta G_{ci-o} = -\frac{I_{in}}{DC_2} \left(s + \frac{D^2 V_{e1} + r_{e1} I_{in}}{I_{in} L_1} \right) (1 + sr_{C2} C_2).$$

$$\Delta Y_{o-o} = \frac{s}{L_1},$$

$$\Delta G_{io-o} = \frac{D}{L_1 C_2} (1 + sr_{C2} C_2), \quad (8.83)$$

$$\Delta G_{co-o} = \frac{V_{e1}}{L_1} \left(s - \frac{I_{in}}{V_{e1} C_2} \right).$$

$$\Delta = s^2 + s \frac{r_{e1}}{L_1} + \frac{D^2}{L_1 C_2}. \quad (8.84)$$

$$Z_{in-oco}^o = \frac{1 + sr_{C2} C_2}{s C_2},$$

$$Y_{o-sci} = \frac{1}{sL_1 + r_{e1} - D^2 r_{C2}},$$

$$Z_{in-\infty} = \frac{(V_{e1} + r_{C2} I_{in})(1 + sr_{C2} C_2)}{sV_{e1} C_2 - I_{in}}, \quad (8.85)$$

$$T_{oi-\infty} = -\frac{I_{in}(1 + sr_{C2} C_2)}{D(sV_{e1} C_2 - I_{in})},$$

$$Y_{o-\infty} = \frac{1}{sL_1 + r_{e1} + (D^2 V_{e1} / I_{in})},$$

$$G_{io-\infty} = \left(D(r_{C2} + \frac{V_{e1}}{I_{in}}) \right) / \left(sL_1 + r_{e1} + \frac{D^2 V_{e1}}{I_{in}} \right).$$

8.2.2.2 Boost Power-Stage Converter

The power stage of the CF boost power-stage converter with the relevant components is given in Figure 8.10a. Its on-time and off-time power-stage structures are given in Figure 8.10b and c, respectively. (Note: The switch control scheme is maintained as it is in the VF boost converter). The dynamic modeling of the boost power-stage converter is also presented in Ref. [18] including the verification of the dynamic models and the operation in practical application in interfacing photovoltaic generator. We do not present here anymore all the

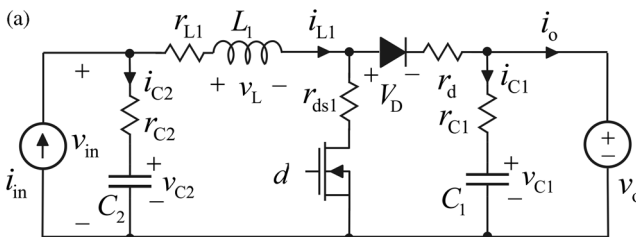


Figure 8.10 CF boost power-stage converter. (a) Basic power stage. (b) On-time power-stage structure. (c) Off-time power-stage structure.

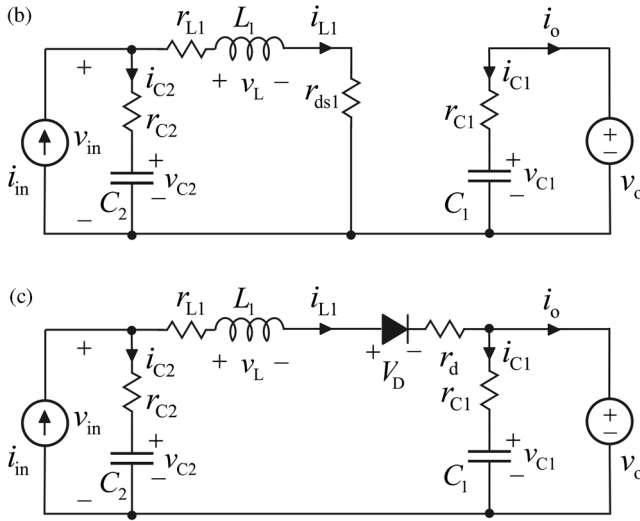


Figure 8.10 (Continued)

details included in the modeling, which can be easily performed by means of Figure 8.10, the instructions given in Chapter 2, and the examples in the previous sections.

The average state space can be given by

$$\frac{d\langle i_{L1} \rangle}{dt} = -\frac{r_{L1} + dr_{ds1} + d'r_d + r_{C2}}{L_1} \langle i_{L1} \rangle + \frac{1}{L_1} \langle v_{C2} \rangle + \frac{r_{C2}}{L_1} \langle i_{in} \rangle - \frac{d'}{L_1} \langle v_o \rangle - \frac{d'}{L_1} V_D,$$

$$\frac{d\langle v_{C1} \rangle}{dt} = -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_o \rangle,$$

$$\frac{d\langle v_{C2} \rangle}{dt} = -\frac{1}{C_2} \langle i_{L1} \rangle + \frac{1}{C_2} \langle i_{in} \rangle,$$

$$\langle v_{in} \rangle = -r_{C2} \langle i_{L1} \rangle + \langle v_{C2} \rangle + r_{C2} \langle i_{in} \rangle = \langle v_{C2} \rangle + r_{C2} C_2 \frac{d\langle v_{C2} \rangle}{dt},$$

$$\langle i_o \rangle = d' \langle i_{L1} \rangle + \frac{1}{r_{C1}} \langle v_{C1} \rangle - \frac{1}{r_{C1}} \langle v_o \rangle,$$

(8.86)

the operating point by

$$V_{in} = V_{C2} = D'(V_o + V_D) + (r_{L1} + Dr_{ds1} + D'r_d)I_{in},$$

$$V_{C1} = V_o,$$

$$I_{L1} = I_{in},$$

$$I_o = D'I_{in},$$

(8.87)

and the linearized state space by

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1}\hat{i}_{L1} + \frac{1}{L_1}\hat{v}_{C2} + \frac{r_{C2}}{L_1}\hat{i}_{in} - \frac{D'}{L_1}\hat{v}_o + \frac{V_{e1}}{L_1}\hat{d}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{r_{C1}C_1}\hat{v}_{C1} + \frac{1}{r_{C1}C_1}\hat{v}_o, \\
 \frac{d\hat{v}_{C2}}{dt} &= -\frac{1}{C_2}\hat{i}_{L1} + \frac{1}{C_2}\hat{i}_{in}, \\
 \hat{v}_{in} &= \hat{v}_{C2} + r_{C2}C_2\frac{d\hat{v}_{C2}}{dt}, \\
 \hat{i}_o &= D\hat{i}_{L1} + \frac{1}{r_{C1}}\hat{v}_{C1} - \frac{1}{r_{C1}}\hat{v}_o - I_{in}\hat{d},
 \end{aligned} \tag{8.88}$$

where

$$\begin{aligned}
 r_{e1} &= r_{L1} + Dr_{ds1} + D'r_d + r_{C2}, \\
 V_{e1} &= V_o + V_D + (r_d - r_{ds1})I_{in}.
 \end{aligned} \tag{8.89}$$

The set of transfer functions representing the input dynamics can be given by

$$\begin{aligned}
 \Delta Z_{in-o} &= \frac{(sL_1 + r_{e1} - r_{C2})}{L_1C_2}(1 + sr_{C2}C_2), \\
 \Delta T_{oi-o} &= \frac{D'}{L_1C_2}(1 + sr_{C2}C_2), \\
 \Delta G_{ci-o} &= -\frac{V_{e1}}{L_1C_2}(1 + sr_{C2}C_2),
 \end{aligned} \tag{8.90}$$

and the set of transfer functions representing output dynamics by

$$\begin{aligned}
 \Delta Y_{o-o} &= \frac{D'^2s}{L_1} + \frac{sC_1}{\Delta(1 + sr_{C1}C_1)}, \\
 \Delta G_{io-o} &= \frac{D'}{L_1C_2}(1 + sr_{C2}C_2), \\
 \Delta G_{co-o} &= -I_{in}\left(s^2 - s\left(\frac{D'V_{e1}}{L_1I_{in}} - \frac{r_{e1}}{L_1}\right) + \frac{1}{L_1C_2}\right),
 \end{aligned} \tag{8.91}$$

where Δ denotes the denominator of the transfer functions and can be given by

$$\Delta = s^2 + s\frac{r_{e1}}{L_1} + \frac{1}{L_1C_2}. \tag{8.92}$$

The set of related special transfer functions can be given as follows:

$$\begin{aligned}
 Z_{\text{in-oco}}^{\circ} &= \left[\left(s^2 + s \frac{r_{e1} + D^2 r_{C1} - r_{C2}}{L_1} + \frac{D^2}{L_1 C_1} \right) (1 + sr_{C2} C_2) \right] / \\
 &\quad \left[C_2 s \left(s^2 + s \frac{r_{e1} + D^2 r_{C1}}{L_1} + \frac{C_1 + D^2 C_2}{L_1 C_1 C_2} \right) \right], \\
 Y_{\text{o-sci}} &= \frac{D^2}{sL_1 + r_{e1} - r_{C2}} + \frac{sC_1}{1 + sr_{C1} C_1}, \\
 Z_{\text{in-}\infty} &= \left[\left(s - \frac{D' V_{e1} + (r_{C2} - r_{e1}) I_{\text{in}}}{L_1 I_{\text{in}}} \right) (1 + sr_{C2} C_2) \right] / \\
 &\quad \left[C_2 \left(s^2 - s \frac{D' V_{e1} - r_{e1} I_{\text{in}}}{L_1 I_{\text{in}}} + \frac{1}{L_1 C_2} \right) \right], \\
 T_{\text{oi-}\infty} &= \frac{(sC_1(V_{e1} + D' r_{C1} I_{\text{in}}) + D' I_{\text{in}})(1 + sr_{C2} C_2)}{s^3 L_1 C_1 C_2 r_{C1} I_{\text{in}} - s^2 (C_1 C_2 (D' r_{C1} V_{e1} - r_{C1} r_{e1} I_{\text{in}}) - L_1 C_2 I_{\text{in}}) - s(C_2 (D' V_{e1} - r_{e1} I_{\text{in}}) - C_1 r_{C1} I_{\text{in}}) + I_{\text{in}}}, \\
 Y_{\text{o-}\infty} &= \frac{D' I_{\text{in}}}{V_{e1}} + \frac{sC_1}{1 + sr_{C1} C_1}, \\
 G_{\text{io-}\infty} &= -\frac{I_{\text{in}} L_1}{V_{e1}} \left(s - \frac{D' V_{e1} + (r_{C2} - r_{e1}) I_{\text{in}}}{L_1 I_{\text{in}}} \right).
 \end{aligned} \tag{8.93}$$

The operating point in Eq. (8.87) reveals that the duty ratio has to be decreased for increasing the corresponding output variables. The negative low-frequency signs of the control-related transfer functions in Eqs (8.90) and (8.91) indicate that the feedback and its reference signals have to be interchanged for ensuring stability. These behaviors are similar as in the buck power-stage converter introduced in Section 8.2.2.1.

The conventional feedback arrangement and duty ratio control can be restored by inverting the gate drive signals of the active switches. The corresponding transfer functions can be obtained from Eqs (8.89)–(8.93) by replacing D with D' and D' with D as well as multiplying the control-related transfer functions in Eqs (8.90) and (8.91) by -1 . According to these procedures, the operating point will become

$$\begin{aligned}
 V_{\text{in}} &= V_{C2} = D(V_{\text{o}} + V_{\text{D}}) + (r_{L1} + D' r_{\text{ds1}} + D r_{\text{d}}) I_{\text{in}}, \\
 I_{L1} &= I_{\text{in}}, \\
 I_{\text{o}} &= D I_{\text{in}},
 \end{aligned} \tag{8.94}$$

which implies that the converter is a buck-type converter (i.e., $M(D) = D$) but its control-to-output current transfer function ($G_{\text{co-o}}$) will contain two different RHP zeros approximately at

$$\omega_{\text{low-freq}} \approx \frac{I_{\text{in}}}{V_{\text{in}} C_2}, \tag{8.95}$$

and at

$$\omega_{\text{medium-freq}} \approx \frac{V_{\text{in}}}{L_1 I_{\text{in}}} \quad (8.96)$$

The first RHP zero corresponds to the RHP zero of the buck power-stage converter in Eq. (8.68) and the second RHP zero to the RHP zero of the VF boost converter defined in Chapter 3.

8.2.2.3 Noninverting Buck–Boost Power-Stage Converter

The power stage of the CF buck–boost power-stage converter with the relevant components is given in Figure 8.11a. Its on-time and off-time power-stage structures are given in Figure 8.11b and c, respectively. (Note: The switch control scheme is maintained as it is in the VF buck–boost converter, which is indicated by d and d' .) The dynamic modeling of the buck–boost power-stage converter is also presented in Ref. [19], including the verification of the dynamic models and the operation in practical application in interfacing photovoltaic generator. We do not present here anymore all the details included in the modeling, which can be easily performed by means of Figure 8.11, the instructions given in Chapter 2, and the examples in the previous sections.

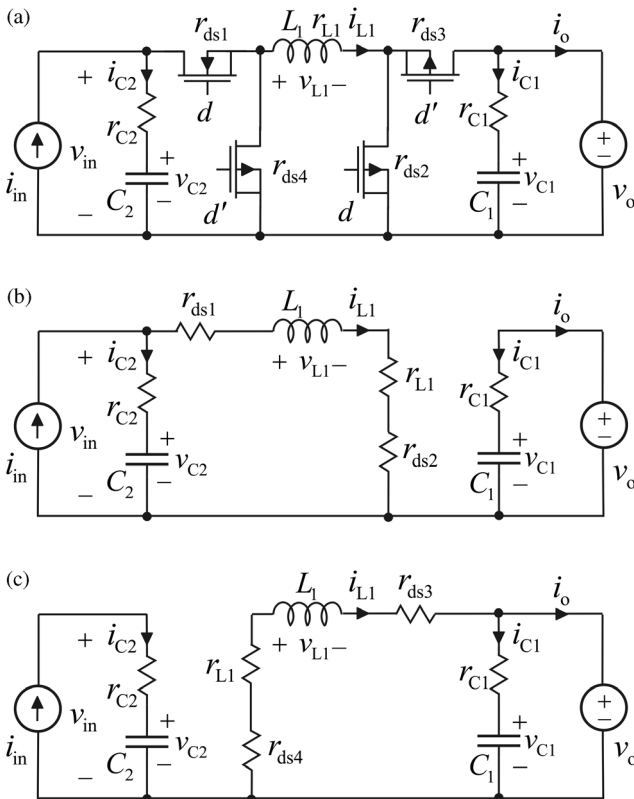


Figure 8.11 Noninverting CF buck–boost power-stage converter. (a) Basic power stage. (b) On-time power-stage structure. (c) Off-time power-stage structure.

The average state space can be given by

$$\begin{aligned}
 \frac{d\langle i_{L1} \rangle}{dt} &= -\frac{r_{L1} + d(r_{ds1} + r_{ds2}) + d'(r_{ds3} + r_{ds4}) + dr_{C2}}{L_1} \langle i_{L1} \rangle \\
 &\quad + \frac{d}{L_1} \langle v_{C2} \rangle + \frac{dr_{C2}}{L_1} \langle i_{in} \rangle - \frac{d'}{L_1} \langle v_o \rangle, \\
 \frac{d\langle v_{C1} \rangle}{dt} &= -\frac{1}{r_{C1}C_1} \langle v_{C1} \rangle + \frac{1}{r_{C1}C_1} \langle v_o \rangle, \\
 \frac{d\langle v_{C2} \rangle}{dt} &= -\frac{d}{C_2} \langle i_{L1} \rangle + \frac{1}{C_2} \langle i_{in} \rangle, \\
 \langle v_{in} \rangle &= \langle v_{C2} \rangle + r_{C2}C_2 \frac{d\langle v_{C2} \rangle}{dt}, \\
 \langle i_o \rangle &= d' \langle i_{L1} \rangle + \frac{1}{r_{C1}} \langle v_{C1} \rangle - \frac{1}{r_{C1}} \langle v_o \rangle,
 \end{aligned} \tag{8.97}$$

the operating point by

$$\begin{aligned}
 V_{in} &= V_{C2} = \frac{D'}{D} V_o + (r_{L1} + D(r_{ds1} + r_{ds2}) + D'(r_{ds3} + r_{ds4}) + DD'r_{C2}) \frac{I_{in}}{D^2}, \\
 V_{C1} &= V_o, \\
 I_{L1} &= \frac{I_{in}}{D}, \\
 I_o &= D'I_{L1} = \frac{D'}{D} I_{in},
 \end{aligned} \tag{8.98}$$

and the linearized state space by

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1}}{L_1} \hat{i}_{L1} + \frac{D}{L_1} \hat{v}_{C2} + \frac{Dr_{C2}}{L_1} \hat{i}_{in} - \frac{D'}{L_1} \hat{v}_o + \frac{V_{e1}}{L_1} \hat{d}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{r_{C1}C_1} \hat{v}_{C1} + \frac{1}{r_{C1}C_1} \hat{v}_o, \\
 \frac{d\hat{v}_{C2}}{dt} &= -\frac{D}{C_2} \hat{i}_{L1} + \frac{1}{C_2} \hat{i}_{in} - \frac{I_{in}}{DC_2} \hat{d}, \\
 \hat{v}_{in} &= \hat{v}_{C2} + r_{C2}C_2 \frac{d\hat{v}_{C2}}{dt}, \\
 \hat{i}_o &= D'\hat{i}_{L1} + \frac{1}{r_{C1}} \hat{v}_{C1} - \frac{1}{r_{C1}} \hat{v}_o - \frac{I_{in}}{D} \hat{d},
 \end{aligned} \tag{8.99}$$

where

$$\begin{aligned}
 r_{e1} &= r_{L1} + D(r_{ds1} + r_{ds2}) + D'(r_{ds3} + r_{ds4}) + Dr_{C2}, \\
 V_{e1} &= \frac{V_o}{D} + \frac{(r_{L1} + D^2(r_{ds1} + r_{ds2}) + D'(1+D)(r_{ds3} + r_{ds4}) + D^2r_{C2})}{D^2} I_{in}.
 \end{aligned} \tag{8.100}$$

The set of transfer functions representing the input dynamics can be given by

$$\begin{aligned}\Delta Z_{\text{in-o}} &= \frac{(sL_1 + r_{e1} - D^2r_{C2})}{L_1C_2}(1 + sr_{C2}C_2), \\ \Delta T_{\text{oi-o}} &= \frac{DD'}{L_1C_2}(1 + sr_{C2}C_2), \\ \Delta G_{\text{ci-o}} &= -\frac{sL_1I_{\text{in}} + D^2V_{e1} + r_{e1}I_{\text{in}}}{DL_1C_2}(1 + sr_{C2}C_2),\end{aligned}\quad (8.101)$$

and the set of transfer functions representing output dynamics by

$$\begin{aligned}\Delta Y_{\text{o-o}} &= \frac{D^2s}{L_1} + \frac{sC_1}{\Delta(1 + sr_{C1}C_1)}, \\ \Delta G_{\text{io-o}} &= \frac{DD'}{L_1C_2}(1 + sr_{C2}C_2), \\ \Delta G_{\text{co-o}} &= -\frac{I_{\text{in}}}{D}\left(s^2 - s\left(\frac{DD'V_{e1}}{L_1I_{\text{in}}} - \frac{r_{e1}}{L_1}\right) + \frac{D}{L_1C_2}\right),\end{aligned}\quad (8.102)$$

where Δ denotes the denominator of the transfer functions and can be given by

$$\Delta = s^2 + s\frac{r_{e1}}{L_1} + \frac{D^2}{L_1C_2}. \quad (8.103)$$

The set of related special transfer functions can be given as follows:

$$\begin{aligned}Z_{\text{in-oco}}^{\text{o}} &= \left[\left(s^2 + s\frac{r_{e1} + D^2r_{C1} - D^2r_{C2}}{L_1} + \frac{D^2}{L_1C_1} \right) (1 + sr_{C2}C_2) \right] / \\ &\quad \left[C_2s \left(s^2 + s\frac{r_{e1} + D^2r_{C1}}{L_1} + \frac{D^2C_1 + D^2C_2}{L_1C_1C_2} \right) \right], \\ Y_{\text{o-sci}} &= \frac{D^2}{sL_1 + r_{e1} - D^2r_{C2}} + \frac{sC_1}{1 + sr_{C1}C_1}, \\ Z_{\text{in-}\infty} &= \left[\left(s - \frac{DD'V_{e1} + (Dr_{C2} - r_{e1})I_{\text{in}}}{L_1I_{\text{in}}} \right) (1 + sr_{C2}C_2) \right] / \\ &\quad \left[C_2 \left(s^2 - s\frac{DD'V_{e1} - r_{e1}I_{\text{in}}}{L_1I_{\text{in}}} + \frac{D}{L_1C_2} \right) \right], \\ T_{\text{oi-}\infty} &= \frac{(s^2L_1C_1I_{\text{in}} + sC_1(D^2V_{e1} + (r_{e1} + Dr_{C1})I_{\text{in}} + D'I_{\text{in}}))(1 + sr_{C2}C_2)}{s^3L_1C_1C_2r_{C1}I_{\text{in}} - s^2(C_1C_2(DD'r_{C1}V_{e1} - r_{C1}r_{e1}I_{\text{in}}) - L_1C_2I_{\text{in}}) - s(C_2(DD'V_{e1} - r_{e1}I_{\text{in}}) - C_1Dr_{C1}I_{\text{in}}) + DI_{\text{in}}}, \\ Y_{\text{o-}\infty} &= \frac{D'}{sL_1 + (D^2V_{e1}/I_{\text{in}}) + r_{e1}} + \frac{sC_1}{1 + sr_{C1}C_1}, \\ G_{\text{io-}\infty} &= -\left[\left(s - \frac{DD'V_{e1} + (Dr_{C2} - r_{e1})I_{\text{in}}}{L_1I_{\text{in}}} \right) / \left(s + \frac{D^2V_{e1} + r_{e1}I_{\text{in}}}{L_1I_{\text{in}}} \right) \right].\end{aligned}\quad (8.104)$$

The operating point in Eq. (8.98) reveals that the duty ratio has to be decreased for increasing the corresponding output variables. The negative low-frequency signs of the control-related transfer functions in Eqs (8.101) and (8.102) indicate that the feedback and its reference signals have to be interchanged for ensuring stability. These behaviors are similar as in the buck and boost power-stage converters introduced in Sections 8.2.2.1 and 8.2.2.2.

The conventional feedback arrangement and duty ratio control can be restored by inverting the gate drive signals of the active switches. The corresponding transfer functions can be obtained from Eqs (8.101)–(8.104) by replacing D with D' and D' with D as well as multiplying the control-related transfer functions in Eqs (8.101) and (8.102) by -1 . According to these procedures, the operating point will become

$$\begin{aligned} V_{\text{in}} &= V_{C2} = \frac{D}{D'} V_o + (r_{L1} + D'(r_{\text{ds}1} + r_{\text{ds}2}) + D(r_{\text{ds}3} + r_{\text{ds}4}) + DD'r_{C2}) \frac{I_{\text{in}}}{D'^2}, \\ V_{C1} &= V_o, \\ I_{L1} &= \frac{I_{\text{in}}}{D'}, \\ I_o &= DI_{L1} = \frac{D}{D'} I_{\text{in}}, \end{aligned} \tag{8.105}$$

which implies that the converter is a buck–boost-type converter (i.e., $M(D) = D/D'$) but its control-to-output current transfer function ($G_{\text{co-o}}$) will contain two different RHP zeros approximately at

$$\omega_{\text{low-freq}} \approx \frac{I_{\text{in}}}{V_{\text{in}} C_2}, \tag{8.106}$$

and at

$$\omega_{\text{medium-freq}} \approx \frac{V_{\text{in}}}{L_1 I_{\text{in}}}. \tag{8.107}$$

The first RHP zero corresponds to the RHP zero of the buck power-stage converter in Eq. (8.68) and the second RHP zero to the RHP zero of the VF buck–boost converter defined in Chapter 3.

8.3 Source and Load Interactions

The general formulations for the source and load interactions are presented in Chapter 2. In this section, we present the specific formulations for the CF-CO and CF-VO converters.

8.3.1 CF-CO Converters

8.3.1.1 Source Interactions

According to the generalized source interactions given in Section 2.2.5, the source-affected set of transfer functions representing the source impedance-

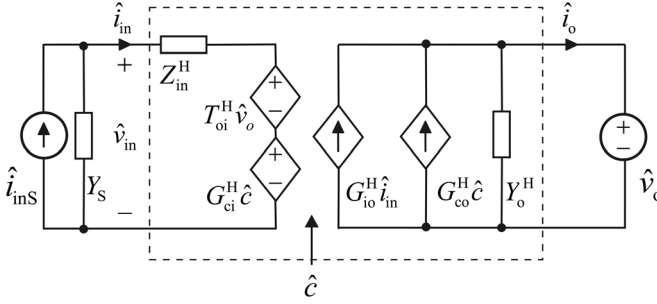


Figure 8.12 Linear network model of CF-CO converter with nonideal source.

induced changes in the dynamics of the CF-CO converter (cf. Figure 8.12) can be given by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \frac{Z_{in}^H}{1 + Y_S Z_{in}^H} & \frac{T_{oi}^H}{1 + Y_S Z_{in}^H} & \frac{G_{ci}^H}{1 + Y_S Z_{in}^H} \\ \frac{G_{io}^H}{1 + Y_S Z_{in}^H} & -\frac{1 + Y_S Z_{in-oco}^{H-x}}{1 + Y_S Z_{in-x}^H} Y_{o-x}^H & \frac{1 + Y_S Z_{in-\infty}^H}{1 + Y_S Z_{in}^H} G_{co}^H \end{bmatrix} \begin{bmatrix} \hat{i}_{inS} \\ \hat{v}_o \\ \hat{d} \end{bmatrix}, \quad (8.108)$$

where

$$\begin{aligned} Z_{in-oco}^{H-x} &= Z_{in-x}^H + \frac{G_{io-x}^H T_{oi-x}^H}{Y_{o-x}^H}, \\ Z_{in-\infty}^H &= Z_{in}^H - \frac{G_{io}^H G_{ci}^H}{G_{co}^H}, \end{aligned} \quad (8.109)$$

and the superscript x denotes that the open-circuit input impedance is dependent on the state of input-side feedback, as discussed in Section 8.2.

According to Eq. (8.108), the source admittance (Y_S) would interact with the converter via its input impedance (Z_{in}) (i.e., $1 + Y_S Z_{in}^H$), its open-circuit input impedance (Z_{in-oco}^{H-x}) (i.e., $1 + Y_S Z_{in-oco}^{H-x}$), or its ideal input impedance ($Z_{in-\infty}^H$) (i.e., $1 + Y_S Z_{in-\infty}^H$). The interactions would take place when the source impedance ($1/Y_S$) is smaller than the named impedances. The series resonant-type source impedance behavior would be the dominating origin of source interactions. In the voltage-fed converters, the dominating origin of source interactions is the parallel-resonant source behavior, as discussed in Chapter 3.

8.3.1.2 Load Interactions

According to the generalized load interactions given in Section 2.2.5, the load-affected set of transfer functions representing the load impedance-induced

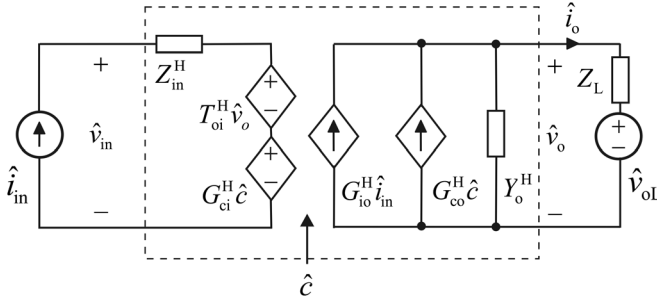


Figure 8.13 Linear network model of CF-CO converter with nonideal load.

changes in the dynamics of the CF-CO converter (cf. Figure 8.13) can be given by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \frac{1 + Z_L Y_{o-sci}^H}{1 + Z_L Y_o^H} Z_{in}^H & \frac{T_{oi}^H}{1 + Z_L Y_o^H} & \frac{1 + Z_L Y_{o-\infty}^H}{1 + Z_L Y_o^H} G_{ci}^H \\ \frac{G_{io}^H}{1 + Z_L Y_o^H} & -\frac{Y_o^H}{1 + Z_L Y_o^H} & \frac{G_{co}^H}{1 + Z_L Y_o^H} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{oL} \\ \hat{d} \end{bmatrix}, \quad (8.110)$$

where

$$Y_{in-sci}^H = Y_o^H + \frac{G_{io}^H T_{oi}^H}{Y_o^H}, \quad (8.111)$$

$$Y_{o-\infty}^H = Y_o^H + \frac{T_{oi}^H G_{co}^H}{G_{ci}^H}.$$

According to Eq. (8.110), the load impedance (Z_L) would interact with the converter via its output admittance (Y_o) (i.e., $1 + Z_L Y_o^H$), its short-circuit output admittance (Y_{o-sci}^H) (i.e., $1 + Z_L Y_{o-sci}^H$), or its ideal output admittance ($Y_{o-\infty}^H$) (i.e., $1 + Z_L Y_{o-\infty}^H$). The interactions would take place when the load admittance ($1/Z_L$) is smaller than the named admittances. The dominant origin of the load interactions would be the parallel resonant-type load impedances.

8.3.2 CF-VO Converters

8.3.2.1 Source Interactions

According to the generalized source interactions given in Section 2.2.5, the source-affected set of transfer functions representing the source impedance-induced changes in the dynamics of the CF-VO converter (cf. Figure 8.14) can be given by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \frac{Z_{in}^Z}{1 + Y_S Z_{in}^Z} & \frac{T_{oi}^Z}{1 + Y_S Z_{in}^Z} & \frac{G_{ci}^Z}{1 + Y_S Z_{in}^Z} \\ \frac{G_{io}^Z}{1 + Y_S Z_{in}^Z} & -\frac{1 + Y_S Z_{in-sco}^Z}{1 + Y_S Z_{in}^Z} Z_o^Z & \frac{1 + Y_S Z_{in-\infty}^Z}{1 + Y_S Z_{in}^Z} G_{co}^Z \end{bmatrix} \begin{bmatrix} \hat{i}_{inS} \\ \hat{i}_o \\ \hat{d} \end{bmatrix}, \quad (8.112)$$

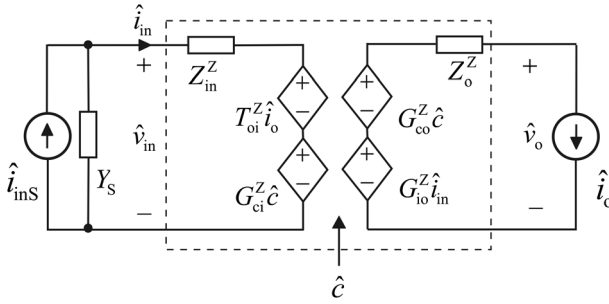


Figure 8.14 Linear network model of CF-VO converter with nonideal source.

where

$$Z_{in-sco}^Z = Z_{in}^Z + \frac{G_{io}^Z T_{oi}^Z}{Z_o^Z}, \tag{8.113}$$

$$Z_{in-\infty}^Z = Z_{in}^Z - \frac{G_{io}^Z G_{ci}^Z}{G_{co}^Z}.$$

Both of the special parameters in Eq. (8.113) are invariant to the state of output-side feedback.

In a similar manner as in case of the CF-CO converter, the source interactions will take place via the source admittance through the input impedance and its special impedances. The interactions would take place when the source impedance ($1/Y_S$) is smaller than the named input-side impedances. Only the ideal input impedance is same as the corresponding impedance of the CF-CO converter. Hence, the interactions taken place in the CF-CO converter cannot be used to estimate the interactions that would take place in the CF-VO converter.

8.3.2.2 Load Interactions

According to the generalized load interactions given in Section 2.2.5, the load-affected set of transfer functions representing the load impedance-induced changes in the dynamics of the CF-VO converter (cf. Figure 8.15) can be given

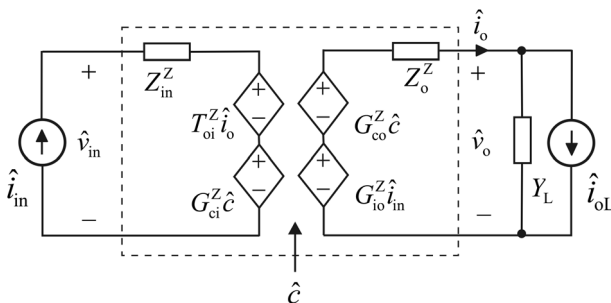


Figure 8.15 Linear network model of CF-VO converter with nonideal load.

by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \frac{1 + Y_L Z_{o-sci}^{Z-x}}{1 + Y_L Z_o^Z} & \frac{T_{oi}^Z}{1 + Y_L Z_o^Z} & \frac{1 + Y_L Z_{o-\infty}^Z}{1 + Y_L Z_o^Z} \\ \frac{G_{io}^Z}{1 + Y_L Z_o^Z} & -\frac{Z_o^Z}{1 + Y_L Z_o^Z} & \frac{G_{co}^Z}{1 + Y_L Z_o^Z} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ \hat{i}_{oL} \\ \hat{d} \end{bmatrix}, \quad (8.114)$$

where

$$\begin{aligned} Z_{o-sci}^{Z-x} &= Z_{o-x}^Z + \frac{G_{io-x}^Z T_{oi-x}^Z}{Z_{in-x}^Z}, \\ Z_{o-\infty}^Z &= Z_o^Z + \frac{T_{oi}^Z G_{co}^Z}{G_{ci}^Z}. \end{aligned} \quad (8.115)$$

The superscript x in the short-circuit output impedance denotes its dependence on the state of output-side feedback.

According to Eq. (8.114), the load impedance ($1/Y_L$) would interact with the converter via its output impedance (Z_o) (i.e., $1 + Y_L Z_o^Z$), its short-circuit output impedance (Z_{o-sci}^Z) (i.e., $1 + Y_L Z_{o-sci}^Z$), or its ideal output impedance ($Z_{o-\infty}^Z$) (i.e., $1 + Y_L Z_{o-\infty}^Z$). The interactions would take place when the load impedance ($1/Y_L$) is smaller than the named impedances. The dominant origin of the load interactions would be the series resonant-type load impedances.

8.4 Impedance-Based Stability Assessment

As stated in Section 2.2.5, the impedance ratio known as minor-loop gain would be composed in such a way that the numerator impedance is the internal impedance of the voltage-type subsystem and the denominator impedance is the internal impedance of the current-type subsystem. Hence, in the CF converters, the impedance ratio has to be taken as $Z_{in}^{H,Z}/Z_S$ as also visible in the source-affected sets of transfer functions in Eqs (8.108) and (8.112), respectively. At the output terminal of the CF-CO converter, the impedance ratio shall be taken as Z_L/Z_o^Z , which is also clearly visible in (8.110). At the output terminal of the CF-VO converter, the impedance ratio shall be taken as Z_o^Z/Z_L , which is also clearly visible in Eq. (8.114). The boundary condition for the instability is the ratio equals -1 . The existence of stability requires that the impedance ratio satisfies the Nyquist stability criterion discussed in Chapter 2.

8.5 Output-Voltage Feedforward

The renewable energy systems compose usually of two stages, where the first stage is a DC–DC converter implementing the PV-generator interfacing and the second stage is a DC–AC converter implementing the grid interfacing. In the single-phase applications, the pulsating nature of the grid power at twice the grid

frequency is reflected into the DC side of the DC–AC converter causing the DC-link voltage to fluctuate at twice the grid frequency [20,21]. If this voltage fluctuation passes through the DC–DC stage into the PV generator, it would decrease the energy taken from the generator or disturb the tracking of the maximum power point of the generator [20]. The DC-link voltage fluctuation can be reduced by increasing the size of the capacitor. The same also applies to the PV generator output side. The large capacitors are usually of electrolyte type, which are known to have limited life time at elevated temperatures and at high ripple currents.

According to the basic dynamic features of a CF-CO converter, we know that the ripple at the output terminal voltage is reflected to the input terminal voltage as $\hat{v}_{in} = T_{oi-o}^H \hat{v}_o$. At open loop, the magnitude of T_{oi-o}^H at low frequencies corresponds to $M(D)$, which does not provide usually sufficient attenuation at twice the grid frequency. The only way to improve the attenuation is to design the converter power stage such that its resonant frequency would locate approximately at one tenth of twice the grid frequency, which is not usually feasible. At closed loop, the input voltage feedback can improve attenuation significantly, which may satisfy the stated requirements.

We would investigate, in this section, the method to improve the attenuation of T_{oi-o}^H by applying output-voltage feedforward (OVFF) technique. The input and output dynamics of the CF-CO converter with the application of the OVFF technique are given in Figure 8.16.

According to Figure 8.16a, we can compute that the input dynamics can be given by

$$\hat{v}_{in} = Z_{in-o}^H \hat{i}_{in} + (T_{oi-o}^H + G_{ovff} G_a G_{ci-o}^H) \hat{v}_o + G_a G_{ci-o}^H \hat{v}_{co}, \quad (8.116)$$

and according to Figure 8.16b, we can compute that the output dynamics can be given by

$$\hat{i}_o = G_{io-o}^H \hat{i}_{in} - (Y_{o-o}^H - G_{ovff} G_a G_{co-o}^H) \hat{v}_o + G_a G_{co-o}^H \hat{v}_{co}. \quad (8.117)$$

According to Eq. (8.117), we can conclude that the output admittance can be, in theory, nullified by selecting the OVFF gain by

$$G_{ovff} = \frac{Y_{o-o}^H}{G_a G_{co-o}^H}. \quad (8.118)$$

This is quite in-line with what would take place in a VF-VO converter, when applying the output current feedforward technique [22]. When computing the effect of the OVFF on T_{oi-o}^{H-OVFF} by means of Eq. (8.116) with the OVFF gain in Eq. (8.118), we will come up to the conclusion that

$$T_{oi-o}^{H-OVFF} = T_{oi-o}^H + \frac{Y_{o-o}^H G_{ci-o}^H}{G_a G_{co-o}^H} = T_{oi-\infty}^H, \quad (8.119)$$

which has the same low-frequency behavior as T_{oi-o}^H (i.e., $M(D)$).

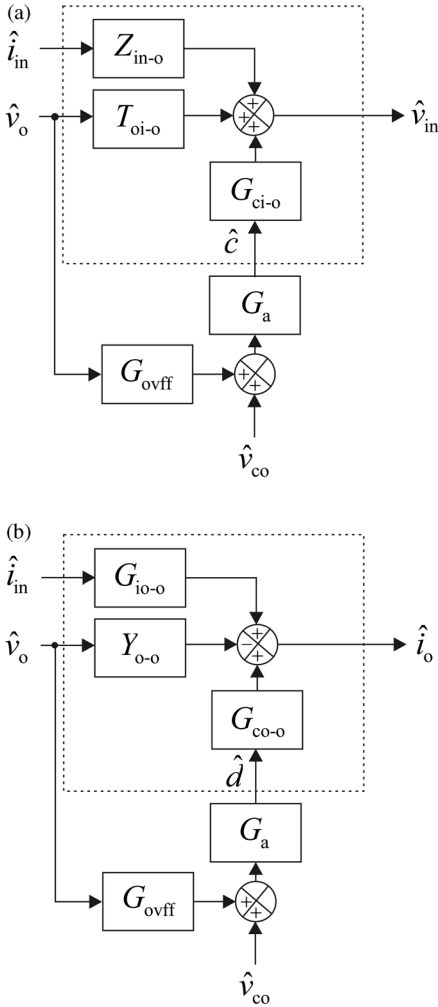


Figure 8.16 Application of OVFF (a) at the input side and (b) at output side.

In order to nullify T_{oi-o}^{H-OVFF} , the OVFF gain shall be (cf. Eq. (8.116))

$$G_{ovff} = -\frac{T_{oi-o}^H}{G_a G_{ci-o}^H}, \tag{8.120}$$

which yields that

$$\begin{aligned} T_{oi-o}^{H-OVFF} &= 0, \\ Y_{o-o}^{H-OVFF} &= Y_{o-o}^H + \frac{T_{oi-o}^H G_{co-o}^H}{G_{ci-o}^H} = Y_{o-\infty}^H. \end{aligned} \tag{8.121}$$

According to Eq. (8.121), we can conclude that the application of OVFF with negative sign makes the converter to resemble a constant power source similarly as under input voltage feedback control (i.e., $Y_{o-c}^H = (Y_{o-o}^H/1 + L_{in})+$

$(L_{in}/1 + L_{in})Y_{0-\infty}^H$). The required sign of G_{ovff} is dependent on the gate drive scheme of the converter: If the output variables will increase along the increase in duty ratio, then the sign of G_{ovff} will be as already presented. If the output variables will decrease along the increase in duty ratio, then the sign of G_{ovff} shall be interchanged compared to what has been already presented.

We will take as an example of the boost power-stage converter modeled in Section 8.2.2.2. According to Eq. (8.120) and the corresponding transfer functions in Eq. (8.90), we will come up to the conclusion that the OVFF gain should be

$$G_{ovff} = D' \frac{V_M}{V_{e1}} \approx D' \frac{V_M}{V_o}, \quad (8.122)$$

where V_M is the inverse of the modulator gain (i.e., $1/G_a$). All the other variables in Eq. (8.122) are quite constant except the complement of the duty ratio. According to the operation point definition in Eq. (8.87), we can rewrite Eq. (8.122) as

$$G_{ovff} \approx \frac{V_{in}}{V_o^2} V_M. \quad (8.123)$$

The OVFF gain in Eq. (8.123) can be easily implemented when digital control is applied but the use of measured input and output voltage would provide additional feedback/feedforward loops, which have to be carefully analyzed and considered.

8.6 Dynamic Review

The predicted frequency responses of the control-to-output current (G_{co-o}) and control-to-input voltage (G_{ci-o}) transfer functions of a buck (cf. Figure 8.17) and boost power-stage (cf. Figure 8.18) converters are compared to the experimental measurements and presented in Figures 8.19 (Buck) and 8.20 (Boost), respectively. The operating point and the relevant component values are given in the corresponding power stage figures. The corresponding predicted transfer functions in symbolic form are given in Eqs (8.67)–(8.69) for the buck converter, and in Eqs (8.90)–(8.92) for the boost converter. The switch control scheme of the converters is as it is in their VF counter parts.

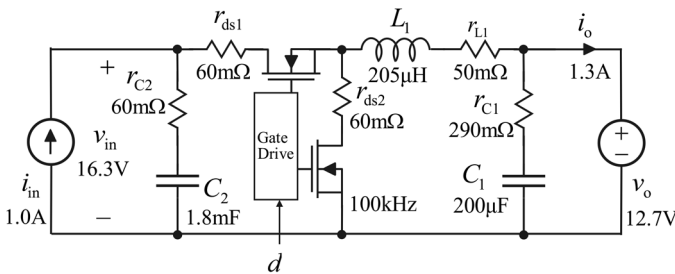


Figure 8.17 The power stage of the experimental buck power-stage converter.

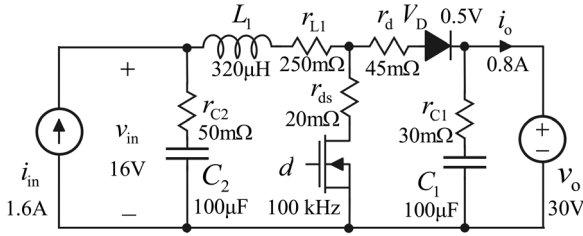


Figure 8.18 The power stage of the experimental boost power-stage converter.

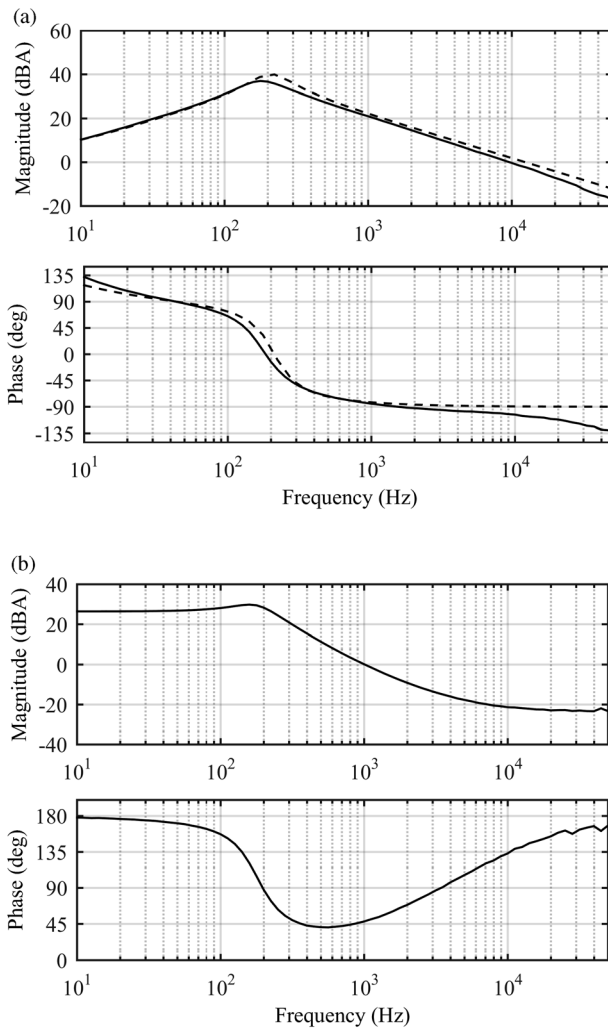


Figure 8.19 The control-related transfer functions of the buck power-stage converter. (a) G_{co-o} and (b) G_{ci-o} (Solid line denotes the measured transfer functions and dashed line the predicted transfer functions).

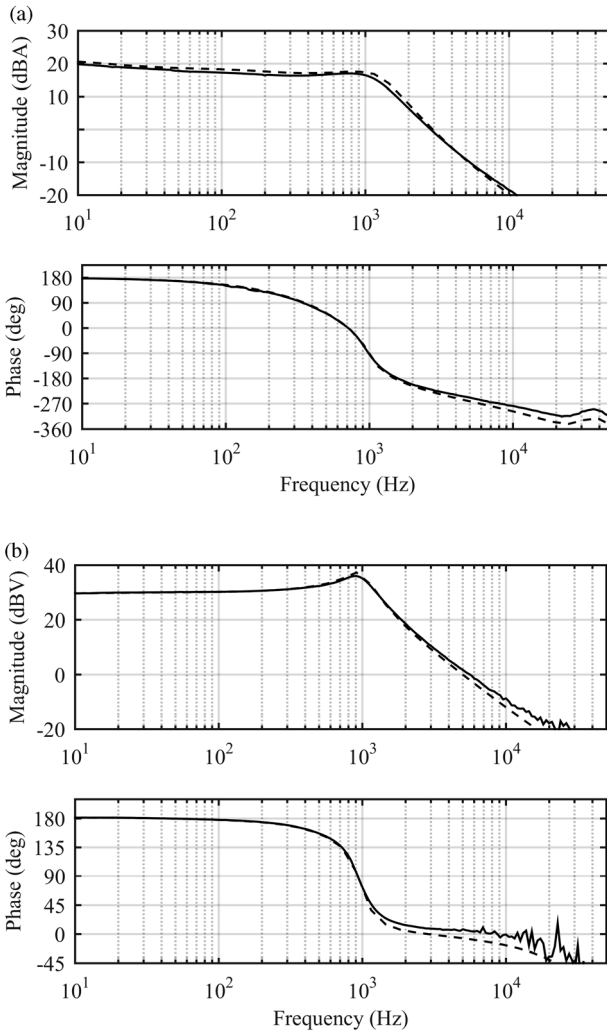


Figure 8.20 The control-related transfer functions of the boost power-stage converter. (a) G_{co-o} and (b) G_{ci-o} (Solid line denotes the measured transfer functions and dashed line the predicted transfer functions).

The measured control-related transfer functions (i.e., G_{co-o} and G_{ci-o}) of the buck power-stage converter in Figure 8.19 indicates that the phase of the transfer functions will start at 180 degrees as the developed analytical models predict. The control-to-output current transfer function (G_{co-o}) in Figure 8.19a shows that the predicted RHP zero locates at quite low frequency (i.e., ≈ 5 Hz) making the magnitude resemble inductive behavior, but the phase behavior reveals that the origin of behavior is the RHP zero. Figure 8.19b proves that the control-to-input voltage transfer function (G_{ci-o}) does not contain RHP zeros. The dashed line in Figure 8.19a denotes the predicted behavior of the transfer function that matches very well with the measured response.

The measured control-related transfer functions (i.e., G_{co-o} and G_{ci-o}) of the boost power-stage converter in Figure 8.20 indicates that the phase of the transfer

functions will start at 180 degrees as the developed analytical models predict. The behavior of the control-to-output current transfer function (G_{co-o}) in Figure 8.20a shows that there are two RHP zeros in the output dynamics as the developed model correctly predicts. Figure 8.20b proves that the control-to-input voltage transfer function (G_{ci-o}) does not contain RHP zeros. The dashed lines in Figure 8.20 denote the predicted behavior of the transfer functions, which match very well with the measured response.

References

- 1 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters – Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim, Germany.
- 2 Erickson, R.W. and Maksimović, D. (2001) *Fundamentals of Power Electronics*, Kluwer Academic Publishers, Norwell, MA.
- 3 Wester, G.W. and Middlebrook, R.D. (1973) Low-frequency characterization of switched dc–dc converters. *IEEE Trans. Aerosp. Electron. Syst.*, **AES-9** (3), 376–385.
- 4 Middlebrook, R.D. and Čuk, S. (1977) A general unified approach to modeling switching-converter power stages. *Int. J. Electron.*, **42** (6), 521–550.
- 5 Čuk, S. and Middlebrook, R.D. (1977) A general unified approach to modelling switching DC-to-DC converters in discontinuous conduction mode. Proceedings of the IEEE PESC, pp. 36–57.
- 6 Sun, J., Mitchell, D.M., Gruel, M.F., Krein, P.T., and Bass, R.M. (2001) Average modeling of PWM converters in discontinuous modes. *IEEE Trans. Power Electron.*, **16** (4), 482–492.
- 7 Suntio, T. (2006) Unified average and small-signal modeling of direct-on-time control. *IEEE Trans. Ind. Electron.*, **53** (1), 287–295.
- 8 Suntio, T., Viinamäki, J., Jokipii, J., Messo, T., and Kuperman, A. (2014) Dynamic characteristics of power electronic interfaces. *IEEE J. Emerg. Sel. Top. Power*, **2** (4), 949–961.
- 9 Maksimović, D. and Čuk, S. (1991) A unified analysis of PWM converters in discontinuous modes. *IEEE Trans. Power Electron.*, **6** (4), 476–490.
- 10 Grigore, V. and Kyyrä, J. (1999) High power factor rectifier based on buck converter operating in discontinuous capacitor voltage mode. Proceedings of the IEEE APEC, pp. 612–619.
- 11 Tse, C.K. and Chow, M.H.I. (1997) New single-stage power-factor-corrected regulators operating in discontinuous capacitor voltage mode. Proceedings of the IEEE PESC, pp. 371–377.
- 12 Kumar, R.A., Suresh, M.S., and Nagaraju, J. (2006) Effect of solar array capacitance on the performance of switching shunt voltage regulator. *IEEE Trans. Power Electron.*, **21** (2), 543–548.
- 13 Leppäaho, J. and Suntio, T. (2011) Dynamic characteristics of current-fed superbuck converter. *IEEE Trans. Power Electron.*, **26** (1), 200–209.
- 14 Huusari, J. and Suntio, T. (2012) Interfacing constraints of distributed maximum power point tracking converters in photovoltaic applications. Proceedings of the EPE-PEMC, pp. DS3d.1-1–DS3d1-7.

- 15 Leppäaho, J., Nousiainen, L., Puukko, J., Huusari, J., and Suntio, T. (2010) Implementing current-fed converters by adding an input capacitor at the input of voltage-fed converter for interfacing solar generator. Proceedings of the EPE-PEMC, pp. 81–88.
- 16 Ziao, W., Dunford, W.G., Palmer, P.R., and Capel, A. (2007) Regulation of the photovoltaic voltage. *IEEE Trans. Ind. Electron.*, **54** (3), 1365–1374.
- 17 Glass, M.C. (1977) Advancements in the design of solar array to battery charge current regulators. Proceedings of the IEEE PESC, pp. 346–350.
- 18 Viinamäki, J., Jokipii, J., Messo, T., Suntio, T., Sitbon, M., and Kuperman, A. (2015) Comprehensive dynamic analysis of photovoltaic generator interfacing DC–DC boost converter. *IET Renew. Power Gener.*, **9** (4), 306–314.
- 19 Huusari, J. and Suntio, T. (2013) Origin of cross-coupling effects in distributed DC–DC converters in photovoltaic applications. *IEEE Trans. Power Electron.*, **28** (10), 4625–4635.
- 20 Hu, H., Harb, S., Kutkut, N., Batarseh, I., and Zhen, Z.J. (2013) A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems. *IEEE Trans. Power Electron.*, **28** (6), 2711–2726.
- 21 Su, M., Pan, P., Long, X., Sun, Y., and Yang, J. (2014) An active power-decoupling method for single-phase AC–DC converters. *IEEE Trans. Industr. Inform.*, **10** (1), 461–468.
- 22 Karppanen, M., Hankaniemi, M., Suntio, T., and Sippola, M. (2007) Dynamical characterization of peak-current-mode-controlled buck converter with output-current feedforward. *IEEE Trans. Power Electron.*, **22** (2), 444–451.

9

Dynamic Modeling of PCM/PVM-Controlled CF Converters

9.1 Introduction

As discussed in Chapter 4, the peak current-mode (PCM) control would provide highly desirable features, especially in the voltage-fed buck-type converters [1,2]. The PCM-controlled converters have also been applied in interfacing the photovoltaic (PV) generators into the rest of the system [3,4]. It was noticed earlier that the application of PCM-controlled buck converter in PV applications could lead to system instability. The origin of the instability was later addressed to the cascaded nature of the control under PCM control in Ref. [5]. The dynamic modeling of the converter under PCM control can be performed by applying exactly the same methods as have been introduced earlier in Chapter 4. The resulting dynamic models are, however, quite different compared with the dynamic models of the corresponding voltage-fed converters. We model only the buck and boost power-stage converters in this chapter.

The peak voltage mode (PVM) is not introduced anywhere, but it seems to be a quite natural control method when the duality is in question: It is the dual of PCM control. The voltage ripple-based control is discussed in Ref. [6] but not in the same sense as we will do in this chapter. We apply the modeling only to the CF buck and CF superbuck converters introduced in Chapter 7. The main problem with the PVM control is the measuring of the high-frequency capacitor voltage ripple in such a way that it can be used for generating the duty ratio as depicted in Figure 9.1, where the measured capacitor-voltage ripples of the CF superbuck converter introduced in Chapters 7 and 8 are shown. The ripple component may also be very small compared to the average capacitor voltage making its accurate measurement a challenging task. The development of the PVM-controlled models actually indicates that the PVM control is not practical in renewable energy applications, as explained in more detail in Section 9.2.1. In the applications where the output current is controlled constant, the PVM control will provide similar features as the PCM control in VF converters. The dominating applications are, however, in the future, the renewable energy applications, and in those applications the PCM control would give the desired advantageous features, as discussed in Chapter 4.

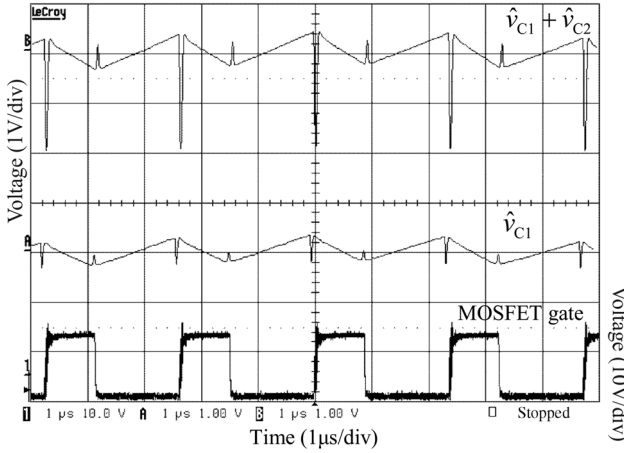


Figure 9.1 The measured capacitor voltage ripples in the CF superbuck converter [7]. Source: Leppäaho 2011. Reproduced with permission of IEEE.

9.2 Duty-Ratio Constraints and Dynamic Models under PCM Control

The averaged comparator equation can be given, in general form, based on the inductor current feedback arrangement in Figure 9.2 by

$$\langle i_{co} \rangle - M_c dT_s = \sum_{i=1}^n \left(\langle i_{Li} \rangle + \frac{dd'T_s}{2} (m_{1i} + m_{2i}) \right). \quad (9.1)$$

Therefore, the main task is to develop the formulations to the up (m_{1i}) and down (m_{2i}) slopes of the associated inductor current to finalize the averaged duty-ratio constraints for the specific converters. As already said, we will treat in this chapter only the PCM-controlled current-fed buck (Figure 9.3) and boost (Figure 9.4) power-stage converters.

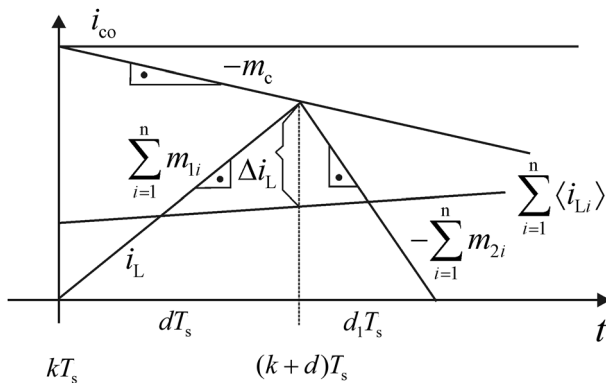


Figure 9.2 Duty-ratio generation under PCM control with multiple inductor currents.

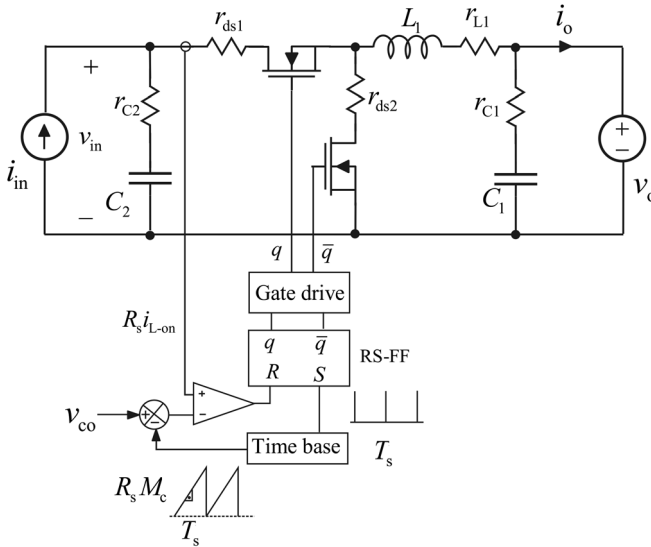


Figure 9.3 The power stage of PCM-controlled current-fed buck power-stage converter.

9.2.1 Buck Power-Stage Converter

The power stage of the PCM-controlled buck power-stage converter is given in Figure 9.3, where the control scheme of the MOSFETs is the same as in the corresponding voltage-fed converter. The converter is a second-order converter, and therefore, the averaged comparator equation can be given by

$$\langle i_{co} \rangle - M_c dT_s = \langle i_{L1} \rangle + \frac{dd'T_s}{2} (m_1 + m_2). \tag{9.2}$$

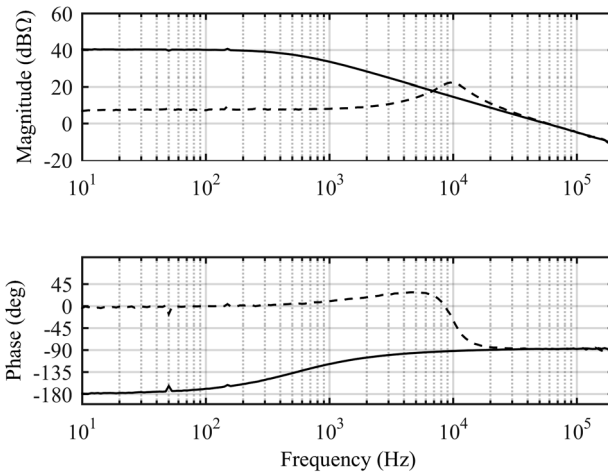


Figure 9.4 The behavior of converter input impedance, when $M_c = 0$ (solid line) and when $M_c \approx 10 \times M_{c-opt}$ (dashed line) (i.e., Eq. (9.14)).

The inductor-current slopes as positive values (i.e., as required in Eq. (9.2) (cf. Chapter 4)) can be computed to be

$$m_1 = \frac{v_{C2} - (r_{L1} + r_{ds1} + r_{C2})\dot{i}_{L1} + r_{C2}\dot{i}_{in} - v_o}{L_1} \quad (9.3)$$

and

$$m_2 = \frac{v_o + (r_{L1} + r_{ds2})\dot{i}_{L1}}{L_1}. \quad (9.4)$$

Substituting m_1 and m_2 in Eq. (9.2) by Eqs (9.3) and (9.4) yields the averaged comparator equation to be

$$\langle \dot{i}_{co} \rangle - M_c d T_s = \left(1 - \frac{dd' T_s}{2L_1} (r_{C2} + r_{ds1} - r_{ds2}) \right) \langle \dot{i}_{L1} \rangle + \frac{dd' T_s}{2L_1} \langle v_{C2} \rangle + \frac{dd' T_s r_{C2}}{2L_1} \langle \dot{i}_{in} \rangle. \quad (9.5)$$

By linearizing Eq. (9.5), we will get the required gains of the linearized duty-ratio constraints in the form of

$$\hat{d} = F_m^H \hat{i}_{co} - q_{L1}^H \hat{i}_{L1} - q_{C2}^H \hat{v}_{C2} - q_{in}^H \hat{i}_{in}, \quad (9.6)$$

where

$$\begin{aligned} F_m^H &= 1 / \left[T_s \left(M_c + \frac{(D' - D)(DV_o + (r_{L1} + r_{ds2})I_{in})}{2L_1 D^2} \right) \right], \\ q_{L1}^H &= 1 - \frac{DD' T_s}{2L} (r_{C2} + r_{ds1} - r_{ds2}), \\ q_{C2}^H &= \frac{DD' T_s}{2L}, \\ q_{in}^H &= \frac{DD' T_s}{2L} r_{C2}. \end{aligned} \quad (9.7)$$

The coefficients of the duty-ratio constraints resemble the duty-ratio constraints of the corresponding voltage-fed converter (cf. Chapter 4). The duty-ratio gain (F_m^H) will become infinite without compensation when the duty ratio equals 50%. This means that the converter will enter into the second-harmonic mode when the instantaneous duty ratio is further increased beyond 0.5. The required value of compensation (M_c) can be selected similarly as in case of the voltage-fed converter to keep the converter operating without second-harmonic mode, that is,

$$M_c + \frac{(D' - D)(DV_o + (r_{L1} + r_{ds2})I_{in})}{2L_1 D^2} > 0. \quad (9.8)$$

The linearized state space representing the dynamics of the PCM-controlled current-fed buck power-stage converter can be obtained from the linearized state space of the DDR-controlled current-fed buck power-stage converter

(cf. Eq. (8.65)) [8] by substituting the perturbed duty ratio with Eq. (9.6). This procedure will yield

$$\begin{aligned}
 \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1} + F_m^H q_{L1}^H V_{e1}}{L_1} \hat{i}_{L1} + \frac{D - F_m^H q_{C2}^H V_{e1}}{L_1} \hat{v}_{C2} + \frac{Dr_{C2} - F_m^H q_{in}^H V_{e1}}{L_1} \hat{i}_{in} \\
 &\quad - \frac{1}{L_1} \hat{v}_o + \frac{F_m^H V_{e1}}{L_1} \hat{i}_{co}, \\
 \frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{r_{C1} C_1} \hat{v}_{C1} + \frac{1}{r_{C1} C_1} \hat{v}_o, \\
 \frac{d\hat{v}_{C2}}{dt} &= -\frac{D^2 - F_m^H q_{L1}^H I_{in}}{DC_2} \hat{i}_{L1} + \frac{F_m^H q_{C2}^H I_{in}}{DC_2} \hat{v}_{C2} + \frac{D + F_m^H q_{in}^H I_{in}}{DC_2} \hat{i}_{in} - \frac{F_m^H I_{in}}{DC_2} \hat{i}_{co}, \\
 \hat{v}_{in} &= \hat{v}_{C2} + r_{C2} C_2 \frac{d\hat{v}_{C2}}{dt}, \\
 \hat{i}_o &= \hat{i}_{L1} + \frac{1}{r_{C1}} \hat{v}_{C1} - \frac{1}{r_{C1}} \hat{v}_o,
 \end{aligned} \tag{9.9}$$

where

$$\begin{aligned}
 r_{e1} &= r_{L1} + Dr_{ds1} + D'r_{ds2} + Dr_{C2}, \\
 V_{e1} &= \frac{V_o}{D} + \frac{r_{L1} + r_{ds2}}{D^2} I_{in}.
 \end{aligned} \tag{9.10}$$

The set of transfer functions representing the input dynamics of the converter can be given by

$$\begin{aligned}
 \Delta Z_{in-o} &= \frac{D + F_m^H q_{C2}^H I_{in} r_{C2}}{DC_2} \\
 &\quad \left(s + \frac{r_{e1} + F_m^H q_{L1}^H V_{e1}}{L_1} - \frac{(D^2 - F_m^H q_{L1}^H I_{in})(D - F_m^H q_{C2}^H V_{e1}) r_{C2}}{L_1(D + F_m^H q_{C2}^H I_{in} r_{C2})} \right) \\
 &\quad (1 + sr_{C2} C_2),
 \end{aligned} \tag{9.11}$$

$$\Delta T_{oi-o} = \frac{D^2 - F_m^H q_{L1}^H I_{in}}{DL_1 C_2} (1 + sr_{C2} C_2),$$

$$\Delta G_{ci-o} = -\frac{F_m^H I_{in}}{DC_2} \left(s + \frac{D^2 V_{e1} + r_{e1} I_{in}}{L_1 I_{in}} \right) (1 + sr_{C2} C_2),$$

and the transfer functions representing the output dynamics by

$$\begin{aligned}\Delta Y_{o-o} &= \frac{s - F_m^H q_{C2}^H I_{in}}{D} + \frac{sC_1}{\Delta(1 + sr_{C1}C_1)}, \\ \Delta G_{io-o} &= \frac{(D - F_m^H q_{C2}^H V_{e1})}{L_1 C_2} (1 + sr_{C2}C_2), \\ \Delta G_{co-o} &= -\frac{F_m^H V_e}{L_1} \left(-s + \frac{I_{in}}{V_{e1}C_2} \right),\end{aligned}\tag{9.12}$$

where the denominator (Δ) of the transfer functions can be given by

$$\Delta = s^2 + s \left(\frac{r_{e1} + F_m^H q_{L1}^H V_{e1}}{L_1} - \frac{F_m^H q_{C2}^H I_{in}}{DC_2} \right) + \frac{D^3 - F_m^H (D^2 q_{C2}^H V_{e1} + (Dq_{L1}^H + r_{e1} q_{C2}^H) I_{in})}{DL_1 C_2}.\tag{9.13}$$

The special parameters can be given by

$$\begin{aligned}Z_{in-oco}^o &= \frac{Z_{in-o}}{Y_{o-o}}, \\ Y_{o-sci} &= \frac{D + F_m^H q_{in}^H I_{in}}{sL_1(D + F_m^H q_{in}^H I_{in}) + D(r_{e1} - D^2 r_{C2} + F_m^H (V_{e1}(Dq_{in}^H + q_{L1}^H) + I_{in}(q_{in}^H r_{e1} + q_{L1}^H r_{C2})))} \\ &\quad + \frac{sC_1}{1 + sr_{C1}C_1}, \\ Z_{in-\infty} &= \frac{(V_{e1} + r_{C2}I_{in})(1 + sr_{C2}C_2)}{sV_{e1}C_2 - I_{in}}, \\ T_{oi-\infty} &= -\frac{C_1(s^2 L_1 I_{in} + s(D^2 V_{e1} + (r_{e1} + r_{C1})I_{in}) + I_{in})(1 + sr_{C2}C_2)}{s^2 D V_{e1} r_{C1} C_1 C_2 + sD(V_{e1}C_2 - r_{C2}I_{in}C_1) - DI_{in}}, \\ Y_{o-\infty} &= \frac{1}{sL_1 + r_{e1} + (D^2 V_{e1}/I_{in})} + \frac{sC_1}{1 + sr_{C1}C_1}, \\ G_{io-\infty} &= \left[D \left(r_{C2} + \frac{V_{e1}}{I_{in}} \right) \right] / \left[sL_1 + r_{e1} + \frac{D^2 V_{e1}}{I_{in}} \right],\end{aligned}\tag{9.14}$$

where the parameters denoted by the subscript “ ∞ ” are exactly the same as in the DDR-controlled converter. The only special parameters, which are changed by the application of the PCM control, are the open-circuit input impedance (Z_{in-oco}^x) and the short-circuit output admittance (Y_{o-sci}). The formula of Z_{in-oco}^o is not explicitly given, because it is very long but it is easily computed by using a proper software package.

According to Eq. (9.12), the input noise attenuation can be made very high by designing $D - F_m^H q_{C2}^H V_{e1} = 0$ by means of the compensation M_c . If neglecting the

parasitic elements, the required value of compensation will be

$$M_c \approx \frac{V_o}{2L_1}, \quad (9.15)$$

which is the same value as in the corresponding PCM-controlled voltage-fed converter and known as an optimal value. The value of compensation in Eq. (9.15) does not, however, guarantee that the converter will operate without entering into the second-harmonic mode at all the operation points of the converter (cf. Chapter 4 discussing PCM-controlled buck converter).

If neglecting the parasitic elements and replacing M_c in Eq. (9.13) with Eq. (9.15), then the characteristic polynomial in Eq. (9.13) becomes

$$\Delta \approx s^2 + s \left(\frac{2}{T_s D'} - \frac{I_{in}}{V_{in} C_2} \right) - \frac{2I_{in}}{T_s D' V_{in} C_2}, \quad (9.16)$$

which indicates that the open-loop converter will be unstable when operating as a current-fed converter. When the roots of the polynomial in Eq. (9.16) are well separated then they can be approximated as

$$\omega_{p\text{-LHP}} = \frac{I_{in}}{V_{in} C_2} - \frac{2}{T_s D'} \quad (9.17)$$

and

$$\omega_{p\text{-RHP}} = 1 / \left[\frac{V_{in}}{I_{in}} C_2 - \frac{D' T_s}{2} \right] \quad (9.18)$$

The converter can be stabilized by means of input voltage feedback control by designing its crossover frequency to be always higher than the frequency of the RHP pole in Eq. (9.18). It may be obvious that the RHP pole will locate the closer to the origin the larger the size of the input capacitor. This may explain why the problem is not noticed or reported, for example, in Refs [4,9]. The open-loop converter can also be stabilized [5] by providing excess inductor current loop compensation according to

$$M_c > \frac{V_o}{2L_1} + \frac{I_{in}}{D^2 T_s}. \quad (9.19)$$

The origin of the open-loop instability can also be traced in such a way that we construct a similar engineering block diagram as for the PCM control in Chapter 4 from which we can conclude that the denominator of the transfer functions (Δ) would be of the form

$$\Delta = 1 + F_m^H q_{L1}^H G_{cL1-o}, \quad (9.20)$$

where G_{cL1-o} denotes the control-to-inductor-current transfer function of the DDR-controlled converter, which can be given by

$$G_{cL1-o} = \left[V_{e1} \left(s - \frac{I_{in}}{V_{e1} C_2} \right) \right] / \left[L_1 \left(s^2 + s \frac{r_{e1}}{L_1} + \frac{1}{L_1 C_2} \right) \right]. \quad (9.21)$$

According to Eq. (9.21), G_{cl1} contains the same RHP zero as in the control-to-output-current transfer function (G_{co-o}). Typically the magnitude of the inductor current loop (i.e., $F_m^H q_{L1}^H G_{cl1-o}$) is high especially at the low frequencies, and therefore, the zeros of G_{cl1} will become the poles of the corresponding transfer functions with slight modification (cf. Eq. (9.18)).

The stabilizing effect of the excess inductor current loop compensation in Eq. (9.19) will arise from the change of the phase behavior of the converter input impedance, as shown in Figure 9.4: The low-frequency phase will start from zero (Figure 9.4: dashed line) as the consequence of excess compensation instead of 180° (Figure 9.4: solid line) without compensation.

9.2.2 Boost Power-Stage Converter

The power stage of the PCM-controlled boost power-stage converter is given in Figure 9.5, where the control scheme of the MOSFETs is the same as in the corresponding voltage-fed converter. The converter is a second-order converter, and therefore, the averaged duty-ratio constraints can be given by means of Eq. (9.2).

The inductor current slopes as positive values (i.e., as required in Eq. (9.2) (cf. Chapter 4)) can be computed to be

$$m_1 = \frac{v_{C2} - (r_{L1} + r_{ds1} + r_{C2})i_{L1} + r_{C2}i_{in}}{L_1} \tag{9.22}$$

and

$$m_2 = \frac{-v_{C2} + (r_{L1} + r_d + r_{C2})i_{L1} - r_{C2}i_{in} + v_o + V_D}{L_1}. \tag{9.23}$$

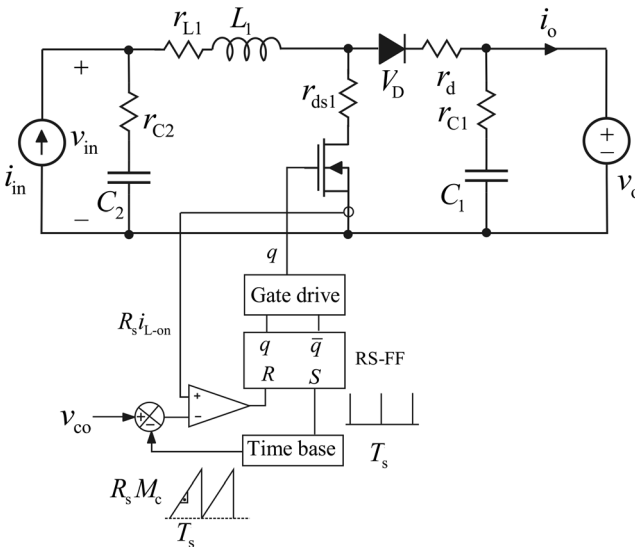


Figure 9.5 The power stage of PCM-controlled current-fed boost power-stage converter.

Substituting m_1 and m_2 in Eq. (9.2) by Eqs (9.21) and (9.22) yields the averaged comparator equation to be

$$\langle i_{co} \rangle - M_c d T_s = \left(1 + \frac{dd' T_s}{2L_1} (r_d - r_{ds1}) \right) \langle i_{L1} \rangle + \frac{dd' T_s}{2L_1} (\langle v_o \rangle + V_D). \quad (9.24)$$

By linearizing Eq. (9.23), we will get the required gains of the linearized duty-ratio constraints in the form of

$$\hat{d} = F_m^H (\hat{i}_{co} - q_{L1}^H \hat{i}_{L1} - q_o^H \hat{v}_o), \quad (9.25)$$

where

$$\begin{aligned} F_m^H &= 1 / \left[T_s \left(M_c + \frac{(D' - D)(V_o + V_D + (r_d - r_{ds1})I_{in})}{2L_1} \right) \right], \\ q_{L1}^H &= 1 + \frac{DD' T_s}{2L} (r_d - r_{ds1}) I_{in}, \\ q_o^H &= \frac{DD' T_s}{2L}. \end{aligned} \quad (9.26)$$

The coefficients of the duty-ratio constraints resemble the duty-ratio constraints of the corresponding voltage-fed converter (cf. Chapter 4). The duty-ratio gain (F_m^H) will become infinite without compensation when the duty ratio equals 50%. This means that the converter will enter into the second-harmonic mode when the instantaneous duty ratio is further increased beyond 0.5. The required value of compensation (M_c) can be selected similarly as in case of the voltage-fed converter to keep the converter operating without second-harmonic mode, that is,

$$M_c + \frac{(D' - D)(V_o + V_D + (r_d - r_{ds1})I_{in})}{2L_1} > 0. \quad (9.27)$$

The linearized state space representing the dynamics of the PCM-controlled current-fed boost power-stage converter can be obtained from the linearized state space of the DDR-controlled current-fed boost power-stage converter (Eq. (8.88)) by substituting the perturbed duty ratio with Eq. (9.24) (See also Ref. [10]). This procedure will yield

$$\begin{aligned} \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1} + F_m^H q_{L1}^H V_{e1}}{L_1} \hat{i}_{L1} + \frac{1}{L_1} \hat{v}_{C2} + \frac{r_{C2}}{L_1} \hat{i}_{in} - \frac{D' + F_m^H q_o^H V_{e1}}{L_1} \hat{v}_o + \frac{F_m^H V_{e1}}{L_1} \hat{i}_{co}, \\ \frac{d\hat{v}_{C1}}{dt} &= -\frac{1}{r_{C1} C_1} \hat{v}_{C1} + \frac{1}{r_{C1} C_1} \hat{v}_o, \\ \frac{d\hat{v}_{C2}}{dt} &= -\frac{1}{C_2} \hat{i}_{L1} + \frac{1}{C_2} \hat{i}_{in}, \\ \hat{v}_{in} &= \hat{v}_{C2} + r_{C2} C_2 \frac{d\hat{v}_{C2}}{dt}, \\ \hat{i}_o &= (D' + F_m^H q_{L1}^H I_{in}) \hat{i}_{L1} + \frac{1}{r_{C1}} \hat{v}_{C1} - \left(\frac{1}{r_{C1}} - F_m^H q_o^H I_{in} \right) \hat{v}_o - F_m^H I_{in} \hat{i}_{co}, \end{aligned} \quad (9.28)$$

where

$$\begin{aligned} r_{e1} &= r_{L1} + Dr_{ds1} + D'r_d + r_{C2}, \\ V_{e1} &= V_o + V_D + (r_d - r_{ds1})I_{in}. \end{aligned} \quad (9.29)$$

The set of transfer functions representing the input dynamics of the converter can be given by

$$\begin{aligned} \Delta Z_{in-o} &= \frac{sL_1 + r_{e1} - r_{C2} + F_m^H q_{L1}^H V_{e1}}{L_1 C_2} (1 + sr_{C2} C_2), \\ \Delta T_{oi-o} &= \frac{D' + F_m^H q_o^H V_{e1}}{L_1 C_2} (1 + sr_{C2} C_2), \\ \Delta G_{ci-o} &= -\frac{F_m^H V_{e1}}{L_1 C_2} (1 + sr_{C2} C_2), \end{aligned} \quad (9.30)$$

and the transfer functions representing the output dynamics by

$$\begin{aligned} \Delta Y_{o-o} &= -F_m^H q_o^H I_{in} \left(s^2 - s \frac{D'^2 + F_m^H (D' (q_o^H V_{e1} + q_{L1}^H I_{in}) - q_o^H I_{in} r_{e1})}{L_1 F_m^H q_o^H I_{in}} + \frac{1}{L_1 C_2} \right) \\ &\quad + \frac{sC_1}{\Delta(1 + sr_{C1} C_1)}, \\ \Delta G_{io-o} &= \frac{(D' + F_m^H q_{L1}^H I_{in})}{L_1 C_2} (1 + sr_{C2} C_2), \\ \Delta G_{co-o} &= -\frac{F_m^H I_{in}}{L_1} \left(s^2 - s \left(\frac{D' V_{e1}}{L_1 I_{in}} - \frac{r_{e1}}{L_1} \right) + \frac{1}{L_1 C_2} \right), \end{aligned} \quad (9.31)$$

where the denominator (Δ) of the transfer functions can be given by

$$\Delta = s^2 + s \frac{r_{e1} + F_m^H q_{L1}^H V_{e1}}{L_1} + \frac{1}{L_1 C_2}. \quad (9.32)$$

The special parameters can be given by

$$\begin{aligned} Z_{in-oco}^o &= \frac{Z_{in-o}}{Y_{o-o}}, \\ Y_{o-sci} &= \frac{-sL_1 F_m^H q_o^H I_{in} + D'^2 + D' F_m^H (q_o^H V_{e1} + q_{L1}^H I_{in}) + F_m^H q_o^H I_{in} (r_{C2} - r_{e1}) + sC_1}{sL_1 + r_{e1} - r_{C2} + F_m^H q_{L1}^H V_{e1}} + \frac{sC_1}{1 + sr_{C1} C_1}, \\ Z_{in-\infty} &= \left[\left(s - \frac{D' V_{e1} + (r_{C2} - r_{e1}) I_{in}}{L_1 I_{in}} \right) (1 + sr_{C2} C_2) \right] / \left[C_2 \left(s^2 - s \frac{D' V_{e1} - r_{e1} I_{in}}{L_1 I_{in}} + \frac{1}{L_1 C_2} \right) \right], \\ T_{oi-\infty} &= \frac{(sC_1 (V_{e1} + D' r_{C1} I_{in}) + D' I_{in}) (1 + sr_{C2} C_2)}{s^3 L_1 C_1 C_2 r_{C1} I_{in} - s^2 (C_1 C_2 (D' r_{C1} V_{e1} - r_{C1} r_{e1} I_{in}) - L_1 C_2 I_{in}) - s (C_2 (D' V_{e1} - r_{e1} I_{in}) - C_1 r_{C1} I_{in}) + I_{in}}, \\ Y_{o-\infty} &= \frac{D' I_{in}}{V_{e1}} + \frac{sC_1}{1 + sr_{C1} C_1}, \\ G_{io-\infty} &= -\frac{I_{in} L_1}{V_{e1}} \left(s - \frac{D' V_{e1} + (r_{C2} - r_{e1}) I_{in}}{L_1 I_{in}} \right), \end{aligned} \quad (9.33)$$

where the parameters denoted by the subscript “∞” are exactly the same as in the DDR-controlled converter. The only special parameters, which are changed by the application of the PCM control, are the open-circuit input impedance (Z_{in-oco}^x) and the short-circuit output admittance (Y_{o-sci}). The formula of Z_{in-oco}^o is not explicitly given, because it is very long but it is easily computed by using a proper software package.

The formulas of T_{oi-o} and G_{io-o} in Eqs (9.30) and (9.31) indicate that the PCM control would reduce the attenuation of the output and input side noise in contrast to the PCM-controlled buck power-stage converter introduced in Section 9.2.1. The control-to-output transfer function (G_{co-o}) contains the same zeros as the corresponding DDR-controlled converter (i.e., one RHP zero and one LHP zero). The denominator in Eq. (9.32) indicates that the PCM-controlled boost power-stage converter will not be unstable at open loop, because all the coefficients in Eq. (9.32) are always positive.

9.3 Duty-Ratio Constraints and Dynamic Models under PVM Control

In a similar manner as in case of PCM control, the dynamics of the converter under PVM control can be developed by constructing the dependence of the duty ratio on the other variables and circuit elements. The duty-ratio-generation process in case of PVM control is illustrated in Figure 9.6, when the associated currents are assumed to be constant similarly as the voltages under the PCM control. The equivalent series resistances (ESRs; r_{Ci}) of the capacitors are embedded into them and, therefore, the pure capacitor voltages can be never measured. The real capacitor voltage is denoted in the figure by dashed line. In a manner similar to PCM control, the averaged comparator equation can be given

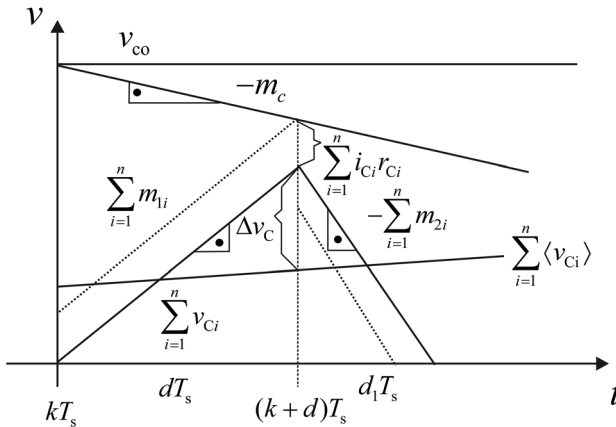


Figure 9.6 The duty-ratio generation under PVM control based on the series-connected capacitor voltage waveforms.

in general form by

$$\langle v_{co} \rangle - M_c dT_s = \sum_{i=1}^n \left(\langle v_{Ci} \rangle + \frac{dd'T_s}{2} (m_{1i} + m_i) + i_{Ci-on} r_{Ci} \right). \quad (9.34)$$

Thus the main task is to develop the formulations for the up (m_{1i}) and down (m_{2i}) slopes of the associated capacitor voltages as well as the corresponding on-time capacitor currents for computing the ohmic loss ($\sum_{i=1}^n i_{Ci-on} r_{Ci}$).

9.3.1 CF Buck Converter

The power stage of the CF buck converter with the PVM control system is given in Figure 9.7, where G_{sf} denotes the capacitor voltage scaling factor. The converter is a second-order converter, and therefore, the averaged comparator equation is of the form

$$\langle v_{co} \rangle - M_c dT_s = \langle v_{C1} \rangle + \frac{dd'T_s}{2} (m_{11} + m_{12}) + i_{C1-on} r_{C1}. \quad (9.35)$$

The slopes of the capacitor voltage and the on-time capacitor current can be given by

$$\begin{aligned} m_{11} &= -\frac{i_{L1}}{C_1} + \frac{i_{in}}{C_1}, \\ m_{12} &= \frac{i_{L1}}{C_1}, \\ i_{C1-on} &= -i_{L1} + i_{in}. \end{aligned} \quad (9.36)$$

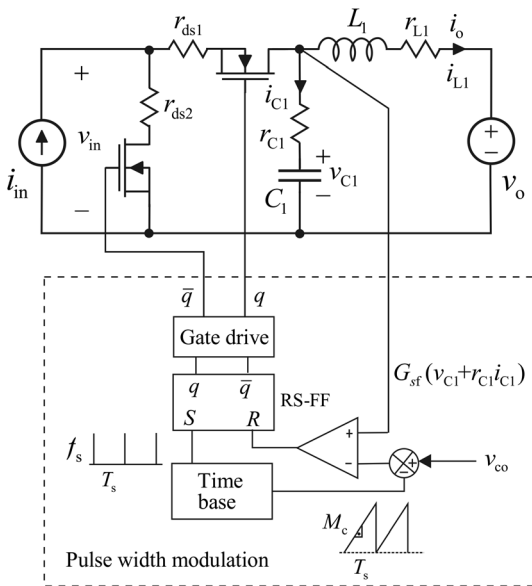


Figure 9.7 The power stage of the PVM-controlled CF buck converter.

Thus, the averaged comparator equation in Eq. (9.35) can be given by

$$\langle v_{co} \rangle - M_c d T_s = \langle v_{C1} \rangle + \left(r_{C1} + \frac{dd' T_s}{2C_1} \right) \langle i_{in} \rangle - r_{C1} \langle i_{L1} \rangle, \quad (9.37)$$

and the duty-ratio constraints will be of the form

$$\hat{d} = F_m^H (\hat{v}_{co} - q_{L1}^H \hat{i}_{L1} - q_{C1}^H \hat{v}_{C1} - q_{in}^H \hat{i}_{in}), \quad (9.38)$$

where

$$\begin{aligned} F_m^H &= 1 / \left[T_s \left(M_c + \frac{(D' - D) I_{in}}{2C_1} \right) \right], \\ q_{L1}^H &= -r_{C1}, \\ q_{C1}^H &= 1, \\ q_{in}^H &= r_{C1} + \frac{DD' T_s}{2C_1}. \end{aligned} \quad (9.39)$$

The duty-ratio gain (F_m^H) in Eq. (9.39) indicates that the converter will enter into the second-harmonic mode if $M_c = 0$ and $D > 0.5$, similarly as the PCM-controlled converter. The second-harmonic mode can be avoided by designing M_c such that $M_c + \frac{(D' - D) I_{in}}{2C_1} > 0$.

The corresponding linearized state space can be computed by substituting \hat{d} in the DDR-controlled state space (Eq. (8.12)) with Eq. (9.38). This process yields

$$\begin{aligned} \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1} + F_m^H q_{L1}^H r_{C1} I_{in}}{L_1} \hat{i}_{L1} + \frac{1 - F_m^H q_{C1}^H r_{C1} I_{in}}{L_1} \hat{v}_{C1} + \frac{(D - F_m^H q_{in}^H I_{in}) r_{C1}}{L_1} \hat{i}_{in} \\ &\quad - \frac{1}{L_1} \hat{v}_o + \frac{F_m^H r_{C1} I_{in}}{L_1} \hat{d}, \\ \frac{d\hat{v}_{C1}}{dt} &= -\frac{1 + F_m^H q_{L1}^H I_{in}}{C_1} \hat{i}_{L1} - \frac{F_m^H q_{C1}^H I_{in}}{C_1} \hat{v}_{C1} + \frac{D - F_m^H q_{in}^H I_{in}}{C_1} \hat{i}_{in} + \frac{F_m^H I_{in}}{C_1} \hat{d}, \\ \hat{v}_{in} &= -(Dr_{C1} + F_m^H q_{L1}^H V_{e1}) \hat{i}_{L1} + (D - F_m^H q_{C1}^H V_{e1}) \hat{v}_{C1} \\ &\quad + (r_{e2} - F_m^H q_{in}^H V_{e1}) \hat{i}_{in} + F_m^H V_{e1} \hat{d}, \\ \hat{i}_o &= \hat{i}_{L1}, \end{aligned} \quad (9.40)$$

where

$$\begin{aligned}
 r_{e1} &= r_{L1} + r_{C1}, \\
 r_{e2} &= Dr_{C1} + Dr_{ds1} + D'r_{ds2}, \\
 V_{e1} &= V_o + (Dr_{L1} + D'r_{C1} + r_{ds1} - r_{ds2})I_{in}.
 \end{aligned} \tag{9.41}$$

The set of transfer functions representing the input dynamics can be given by

$$\begin{aligned}
 \Delta Z_{in-o} &= s^2(r_{e2} - F_m^H q_{in}^H V_{e1}) + s \frac{A_1}{L_1 C_1} + \frac{A_0}{L_1 C_1}, \\
 A_1 &= r_{e1} r_{e2} - D^2 r_{C1}^2 - F_m^H ((q_{in}^H + D q_{L1}^H r_{C1}) V_{e1} - (D q_{in}^H r_{C1} + q_{L1}^H r_{e2}) r_{C1} I_{in}), \\
 A_0 &= r_{e2} + D^2 (r_{e1} - 2r_{C1}) - F_m^H V_{e1} (q_{in}^H + D q_{L1}^H + q_{C1}^H (r_{e1} - r_{C1})) \\
 &\quad + F_m^H I_{in} ((q_{L1}^H + q_{C1}^H (r_{e1} - r_{C1})) r_{e2} - D q_{in}^H (r_{e1} - 2r_{C1})), \\
 \Delta T_{oi-o} &= s \frac{F_m^H q_{L1}^H V_{e1} + D r_{C1}}{L_1} + \frac{D - F_m^H q_{C1}^H V_{e1} + D F_m^H I_{in} (q_{L1}^H + q_{C1}^H r_{C1})}{L_1 C_1}, \\
 \Delta G_{ci-o} &= F_m^H \left(s^2 V_{e1} + s \frac{(r_{e1} V_{e1} C_1 + D(L_1 - r_{C1}^2) I_{in})}{L_1 C_1} + \frac{V_{e1} + D(r_{e1} - 2r_{C1}) I_{in}}{L_1 C_1} \right),
 \end{aligned} \tag{9.42}$$

and the set of transfer functions representing the output dynamics by

$$\begin{aligned}
 \Delta Y_{o-o} &= \frac{s C_1 + F_m^H q_{C1}^H I_{in}}{L_1 C_1}, \\
 \Delta G_{io-o} &= \frac{(D - F_m^H q_{in}^H I_{in})(1 + s r_{C1} C_1)}{L_1 C_1}, \\
 \Delta G_{co-o} &= F_m^H \left(\frac{I_{in}(1 + s r_{C1} C_1)}{L_1 C_1} \right),
 \end{aligned} \tag{9.43}$$

where the denominator of the transfer functions (Δ) can be given by

$$s^2 + s \left(\frac{r_{e1} + F_m^H q_{L1}^H I_{in} r_{C1}}{L_1} + \frac{F_m^H q_{C1}^H I_{in}}{C_1} \right) + \frac{1 + F_m^H I_{in} (q_{L1}^H + (r_{e1} - r_{C1}) q_{C1}^H)}{L_1 C_1}. \tag{9.44}$$

The set of special parameters can be given as follows:

$$\begin{aligned}
 Z_{\text{in-oco}}^o &= \frac{sC_1(r_{e2} - F_m^H q_{\text{in}}^H V_{e1}) + F_m^H ((q_{C1}^H r_{e2} - Dq_{\text{in}}^H)I_{\text{in}} - Dq_{C1}^H V_{e1})}{sC_1 + F_m^H q_{C1}^H I_{\text{in}}}, \\
 Y_{\text{o-sci}} &= \frac{Y_{\text{o-o}}}{Z_{\text{in-o}}^o} Z_{\text{in-oco}}^o, \\
 Z_{\text{in-}\infty} &= r_{e2} - \frac{DV_{e1}}{I_{\text{in}}}, \\
 T_{\text{oi-}\infty} &= \left[D \left(1 + s \frac{V_{e1}C_1}{DI_{\text{in}}} \right) \right] / [1 + sr_{C1}C_1], \\
 Y_{\text{o-}\infty} &= \left[DI_{\text{in}} \left(1 + s \frac{V_{e1}C_1}{DI_{\text{in}}} \right) \right] / \\
 &\quad \left[LCV_{e1}(s^2 + s \left(\frac{DI_{\text{in}}}{V_{e1}C_1} + \frac{r_{e1} - (DI_{\text{in}}/V_{e1})r_{C1}^2}{L_1} \right)) + \frac{1 + D(r_{e1} - 2r_{C1})(I_{\text{in}}/V_{e1})}{L_1C_1} \right], \\
 G_{\text{io-}\infty} &= [(DV_{e1} - r_{e2}I_{\text{in}})(1 + sr_{C1}C_1)] / \\
 &\quad \left[LCV_{e1}(s^2 + s \left(\frac{DI_{\text{in}}}{V_{e1}C_1} + \frac{r_{e1} - (DI_{\text{in}}/V_{e1})r_{C1}^2}{L_1} \right)) + \frac{1 + D(r_{e1} - 2r_{C1})(I_{\text{in}}/V_{e1})}{L_1C_1} \right], \tag{9.45}
 \end{aligned}$$

where $Y_{\text{o-osi}}$ is not explicitly given due to its very long formula. It shall be also noticed that all the ideal transfer functions are exactly the same as in the DDR-controlled CF buck converter.

The input-to-output transfer function ($G_{\text{io-o}}$) in Eq. (9.43) indicates that the input-to-output attenuation can be made high by designing the capacitor voltage loop compensation (M_c) such that

$D - F_m^H q_{\text{in}}^H I_{\text{in}} = 0$. This means that M_c shall be

$$M_c \approx \frac{DI_{\text{in}}}{2C_1} = \frac{I_o}{2C_1} \tag{9.46}$$

This requirement can be met if the converter output current is controlled constant. In practice, the CF converters are usually applied in such a manner that the input voltage is controlled constant and therefore, the output current varies along the changes in the input current (i.e., $I_o = (V_{\text{in}}/V_o)I_{\text{in}}$). This means that the nullifying of the input–output gain is impossible. In order to guarantee the operation of the converter without entering into the second-harmonic mode, the compensation should be done by

$$M_c \approx \frac{I_{\text{in}}}{2C_1}. \tag{9.47}$$

From the practical point of view, the PVM control is not feasible in a CF buck converter. The set of transfer functions show that there are many similarities between the PCM-controlled VF buck converter and the PVM-controlled CF buck converter such as resonant-free operation, no RHP zero, the theoretical possibility to nullify the input-to-output gain, and so on. The duality, however,

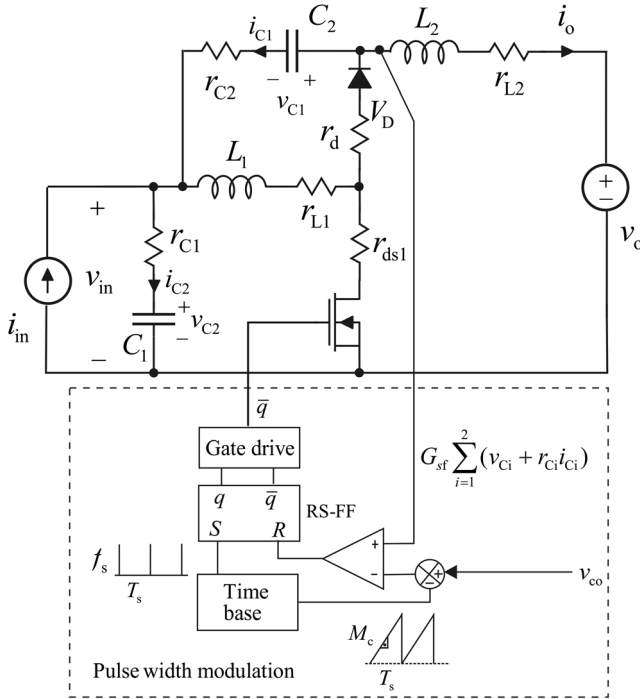


Figure 9.8 The power stage of the PVM-controlled CF superbuck converter.

dictates that the capacitor voltage loop shall be compensated in respect to output current, which is not usually controlled constant in the practical renewable energy applications. Therefore, the PVM control will not be practical in these applications.

9.3.2 CF Superbuck Converter

The power stage of the CF superbuck converter is given in Figure 9.8 with the associated components as well as the control system principle. We will develop only the duty ratio constraints and the PVM state space without solving the transfer functions due to the reasons discussed in the introduction.

In case of CF superbuck converter, the averaged comparator equation is of the form

$$\begin{aligned} \langle v_{co} \rangle - M_c dT_s = \langle v_{C1} \rangle + \langle v_{C2} \rangle + \frac{dd'T_s}{2} (m_{11} + m_{12} + m_{21} + m_{22}) \\ + i_{C1-on} r_{C1} + i_{C2-on} r_{C2}, \end{aligned} \quad (9.48)$$

where the up slopes (m_{1i}) of the capacitor voltages can be given by

$$\begin{aligned} m_{11} &= -\frac{i_{L2}}{C_1} + \frac{i_{in}}{C_1}, \\ m_{21} &= \frac{i_{L1}}{C_2} - \frac{i_{L2}}{C_2}, \end{aligned} \quad (9.49)$$

and the on-time capacitor currents by

$$\begin{aligned} i_{C1\text{-on}} &= -i_{L2} + i_{\text{in}}, \\ i_{C2\text{-on}} &= i_{L1} - i_{L2}, \end{aligned} \quad (9.50)$$

as well as the down slopes (m_{2i}) of the capacitor voltages by

$$\begin{aligned} m_{12} &= \frac{i_{L1}}{C_1} + \frac{i_{L2}}{C_1} - \frac{i_{\text{in}}}{C_1} \\ m_{22} &= \frac{i_{L2}}{C_2} \end{aligned} \quad (9.51)$$

By replacing the variables in Eq. (9.35) as defined in Eqs (9.36)–(9.38), the averaged comparator equation becomes

$$\langle v_{\text{co}} \rangle - M_c dT_s = \langle v_{C1} \rangle + \langle v_{C2} \rangle + \left(\frac{dd' T_s C_1 + C_2}{2 C_1 C_2} + r_{C2} \right) \langle i_{L1} \rangle - (r_{C1} + r_{C2}) \langle i_{L2} \rangle + r_{C1} \langle i_{\text{in}} \rangle, \quad (9.52)$$

and the duty-ratio constraints will be of the form

$$\hat{d} = F_m^H (\hat{v}_{\text{co}} - q_{L1}^H \hat{i}_{L1} - q_{L2}^H \hat{i}_{L2} - q_{C1}^H \hat{v}_{C1} - q_{C2}^H \hat{v}_{C2} - q_{\text{in}}^H \hat{i}_{\text{in}}), \quad (9.53)$$

where

$$\begin{aligned} F_m^H &= 1 / \left[T_s \left(M_c + \frac{(D' - D) D I_{\text{in}} (C_1 + C_2)}{2 C_1 C_2} \right) \right], \\ q_{L1}^H &= r_{C2} + \frac{DD' T_s (C_1 + C_2)}{2 C_1 C_2}, \\ q_{L2}^H &= -(r_{C1} + r_{C2}), \\ q_{C1}^H &= q_{C2}^H = 1, \\ q_{\text{in}}^H &= r_{C1}, \end{aligned} \quad (9.54)$$

The corresponding linearized state space can be computed by substituting \hat{d} in the DDR state space (Eq. (8.53)) with Eq. (9.53). This process yields

$$\begin{aligned} \frac{d\hat{i}_{L1}}{dt} &= -\frac{r_{e1} - F_m^H q_{L1}^H V_{e1}}{L_1} \hat{i}_{L1} - \frac{e_{e2} - F_m^H q_{L2}^H V_{e1}}{L_1} \hat{i}_{L2} + \frac{D' + F_m^H q_{C1}^H V_{e1}}{L_1} \hat{v}_{C1} \\ &\quad - \frac{D - F_m^H q_{C2}^H V_{e1}}{L_1} \hat{v}_{C2} + \frac{D r_{C1} + -F_m^H q_{\text{in}}^H V_{e1}}{L_1} \hat{i}_{\text{in}} - \frac{F_m^H V_{e1}}{L_1} \hat{v}_{\text{co}}, \\ \frac{d\hat{i}_{L2}}{dt} &= -\frac{r_{e2} + F_m^H q_{L1}^H V_{e2}}{L_2} \hat{i}_{L1} - \frac{r_{e3} + F_m^H q_{L2}^H V_{e2}}{L_2} \hat{i}_{L2} + \frac{1 - F_m^H q_{C1}^H V_{e2}}{L_2} \hat{v}_{C1} \\ &\quad + \frac{1 - F_m^H q_{C2}^H V_{e2}}{L_2} \hat{v}_{C2} + \frac{r_{C1} - F_m^H q_{\text{in}}^H V_{e2}}{L_2} \hat{i}_{\text{in}} - \frac{\hat{v}_o}{L_2} + \frac{F_m^H V_{e2}}{L_2} \hat{v}_{\text{co}}, \end{aligned}$$

$$\begin{aligned}
\frac{d\hat{v}_{C1}}{dt} &= -\frac{D' + F_m^H q_{L1}^H I_{in} \hat{i}_{L1}}{C_1} \hat{i}_{L1} - \frac{1 + F_m^H q_{L2}^H I_{in} \hat{i}_{L2}}{C_1} \hat{i}_{L2} - \frac{F_m^H q_{C1}^H I_{in}}{C_1} \hat{v}_{C1} - \frac{F_m^H q_{C2}^H I_{in}}{C_1} \hat{v}_{C2} \\
&\quad + \frac{1 - F_m^H q_{in}^H I_{in} \hat{i}_{in}}{C_1} \hat{i}_{in} + \frac{F_m^H I_{in}}{C_1} \hat{v}_{co}, \\
\frac{d\hat{v}_{C2}}{dt} &= \frac{D - F_m^H q_{L1}^H I_{in} \hat{i}_{L1}}{C_2} \hat{i}_{L1} - \frac{1 + F_m^H q_{L2}^H I_{in} \hat{i}_{L2}}{C_2} \hat{i}_{L2} - \frac{F_m^H q_{C1}^H I_{in}}{C_2} \hat{v}_{C1} - \frac{F_m^H q_{C2}^H I_{in}}{C_2} \hat{v}_{C2} \\
&\quad - \frac{F_m^H q_{in}^H I_{in} \hat{i}_{in}}{C_2} \hat{i}_{in} + \frac{F_m^H I_{in}}{C_2} \hat{v}_{co}, \\
\hat{v}_{in} &= \hat{v}_{C1} + r_{C1} C_1 \frac{d\hat{v}_{C1}}{dt}, \\
\hat{i}_o &= \hat{i}_{L2},
\end{aligned} \tag{9.55}$$

where

$$\begin{aligned}
r_{e1} &= D'(r_{C1} + r_{ds1}) + D(r_{C2} + r_d) + r_{L1}, \\
r_{e2} &= D'r_{C1} - Dr_{C2}, \\
r_{e3} &= r_{C1} + r_{C2} + r_{L2}, \\
V_{e1} &= V_o + V_D + (Dr_{L2} + D'r_{C2} - Dr_{C1} + r_d - r_{ds1})I_{in}, \\
V_{e2} &= (r_{C1} + r_{C2})I_{in}.
\end{aligned} \tag{9.56}$$

9.4 Concluding Remarks

It was once again proved that the full dynamic analysis has to be performed before concluding the applicability of the proposed control method or a power-stage topology in the practical applications: It could be thought that the PVM control is naturally the best control method in these converters because of duality of the CF and VF converters, but as explicitly shown that may not be true but only under certain conditions. The feedback control of output current and voltage are duals of each other but when the feedback is taken from the input side, the duality does not anymore exist. The PCM control works, because the output or DC-link voltage is usually controlled constant by the downstream converter, and thus, the inductor-current-loop compensation can be performed in a consistent manner.

References

- 1 Deisch, C.W. (1978) Simple switching control method changes power converter into a current source. Proceedings of the IEEE PESC, pp. 300–306.

- 2 Suntio, T. (2009) *Dynamic Profile of Switched-Mode Converters – Modeling, Analysis and Control*, Wiley-VCH Verlag GmbH, Weinheim Germany.
- 3 Park, S.H., Bae, H.S., Lee, J.H., and Cho, B.H. (2006) Design of peak and charge current mode control for parallel module solar array regulator system. *Proceedings of the IEEE PESC*, pp. 1–5.
- 4 Park, S.-J., Kang, T.-S., Cho, S.E., Moon, C.-J., Nam, H.-K., and Ise, T. (2006) New parallel driving strategy based on modified converters and peak current mode control for photovoltaic power generation. *Solar Energy*, **80** (5), 524–534.
- 5 Leppäaho, J. and Suntio, T. (2014) Characterizing the dynamics of the peak-current-mode-controlled buck-power-stage converter in photovoltaic applications. *IEEE Trans. Power Electron.*, **29** (7), 3840–3847.
- 6 Redl, R. and Sun, J. (2009) Ripple-based control of switching regulators – an overview. *IEEE Trans. Power Electron.*, **24** (12), 2669–2680.
- 7 Leppäaho, J. and Suntio, T. (2011) Dynamic characteristics of current-fed superbuck converter. *IEEE Trans. Power Electron.*, **26** (1), 200–209.
- 8 Suntio, T., Viinamäki, J., Jokipii, J., Messo, T., and Kuperman, A. (2014) Dynamic characterization of power electronic interfaces. *IEEE J. Emerg. Sel. Top. Power Electron.*, **2** (4), 949–961.
- 9 Siri, K. (2000) Study of system instability in solar-array-based power systems. *IEEE Trans. Aerosp. Electron. Syst.*, **36** (3), 957–964.
- 10 Viinamäki, J., Jokipii, J., Messo, T., Suntio, T., Sitbon, M., and Kuperman, A. (2015) Comprehensive dynamic analysis of photovoltaic generator interfacing DC–DC boost converter. *IET Renew. Power Gener.*, **9** (4), 306–314.

10

Introduction to Photovoltaic Generator

10.1 Introduction

In this chapter, we will introduce the properties of the photovoltaic (PV) generator from the power electronics point of view, that is, we will concentrate on the topics that are relevant for understanding the phenomena in the power electronic converters interfacing the PV generator to the rest of the power system. More detailed information on the semiconductor-related issues can be found, for example, from Ref. [1]. The maximum power point (MPP) tracking is one of the very essential topics in PV field. We will treat the topic only briefly in this chapter but the detailed information can be found, for example, from Refs [2–6] or other similar sources. Reference [2] also presents the methods to model the PV generators as well as to obtain the parameters governing the behavior of the generator.

The operation of solar cell is based on the phenomenon known as *photo-voltaic effect*, where the photons with sufficient energy emitted by the Sun will create electron hole pairs in a proper semiconductor material, and thus electric current when the circuit is closed. The spectral content of the sunlight at the Earth's surface also contains a diffuse (indirect) component in addition to the direct component coming from the Sun. The diffused component is created by scattering and reflections in the atmosphere and surrounding landscape and can account up to 20% of the total light incident on a solar cell [1]. The nominal value of the direct and diffused irradiations at the Earth's surface is considered to be 1 kW/m^2 , but it is naturally varied depending on the atmospheric conditions and the angle of incidence of the irradiation over the location of the cell, as depicted in Figure 10.1. Figure 10.1a represents a clear sky condition, where the angle of incident is reduced due to the season of year. Figure 10.1b represents a typical condition, where the clouds are moving over the solar cells removing temporarily the direct irradiation from the spectrum of the light on the surface of the cells (i.e., the residual irradiation corresponds to the diffused radiation only).

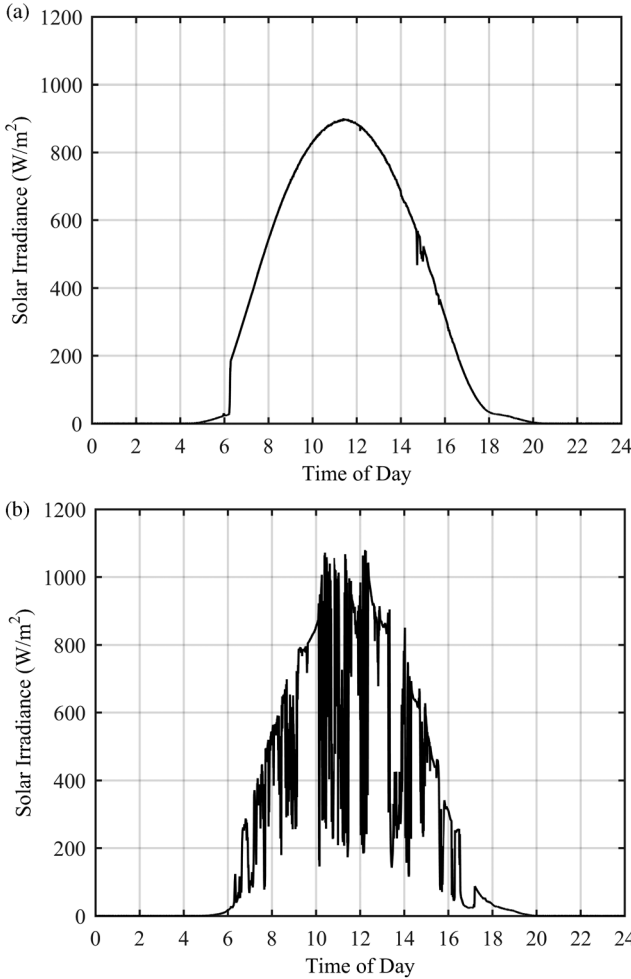


Figure 10.1 Measured irradiance behavior over a day. (a) Clear sky condition. (b) Cloud passing condition.

10.2 Solar Cell Properties

In principle, a solar cell can be represented by an equivalent circuit composed of a current source in parallel with two diodes, as depicted in Figure 10.2 [1,2,7]. The current–voltage (I – V) characteristics of a cell can be given by

$$i_{pv} = i_{ph} - I_{s1}(\exp(qv_{pv}/kT_K) - 1) - I_{s2}(\exp(qv_{pv}/2kT_K) - 1), \quad (10.1)$$

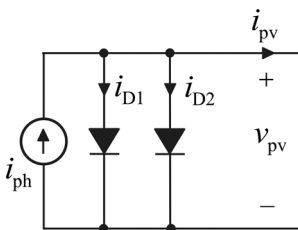


Figure 10.2 Simplified two-diode model of a photovoltaic or solar cell.

where $q = 1.60217646 \times 10^{-19}$ C (i.e., the electron charge), $k = 1.3806503 \times 10^{-23}$ J/K (i.e., the Boltzmann constant), T_K denotes the temperature in Kelvin degrees, and I_{s1} and I_{s2} denote the saturation currents of the diodes, respectively. The two-diode equivalent circuit is most often simplified to a single diode model, where the contributions of the two diodes are combined as follows [2,7]:

$$i_{pv} = i_{ph} - I_s(\exp(qv_{pv}/\eta k T_K) - 1), \quad (10.2)$$

where I_s denotes the combined diode saturation current and η the diode ideality factor.

The photoinduced current (i_{ph}) is dependent on the characteristics of the semiconductor material used for the cell and is linearly dependent on the cell area, irradiation level, and temperature. Its dependence on the irradiation level (G) and temperature in Celsius degrees (T_C) in respect to their values in standard test conditions (STC) can be given by [2]

$$I_{ph} = I_{ph-STC} \frac{G}{G_{STC}} [1 + \alpha_i(T_C - T_{STC})], \quad (10.3)$$

where STC is defined by $G_{STC} = 1$ kW/m² and $T_{STC} = 25^\circ\text{C}$ as well as α_i denotes the temperature coefficient of the photocurrent in STC.

Figure 10.3 shows the practical I–V characteristics of a solar cell, where the current and voltage are normalized in respect to their values at the MPP. The MPP is actually created by the behavior of the diodes when they start conducting current along the increase in the cell terminal voltage. As depicted in the figure, the cell current stays relatively constant in the region where the terminal voltage is less than the MPP voltage. Therefore, this region is commonly known as constant current region (CCR). The region defined by the cell terminal voltage higher than

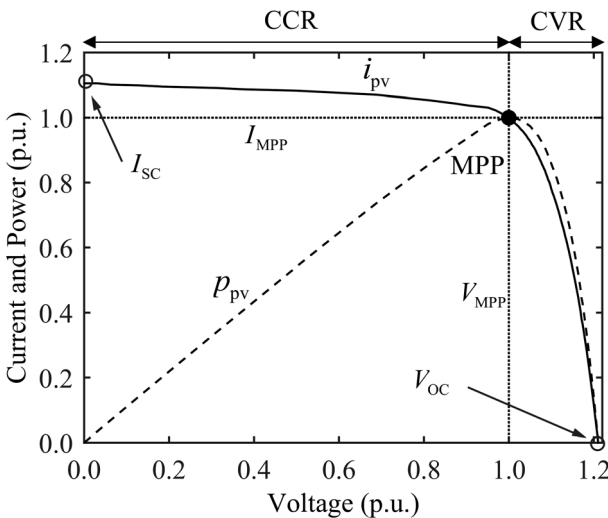


Figure 10.3 The normalized I–V characteristics of a solar cell.

the MPP voltage is commonly known as constant voltage region (CVR), because the cell terminal voltage stays relatively constant when the cell terminal current changes. The maximum terminal current and voltage are commonly known as short-circuit current (I_{SC}) and open-circuit voltage (V_{OC}). I_{SC} clearly equals I_{ph} , as depicted in Figure 10.3.

The open-circuit voltage (V_{OC}) can be given by

$$V_{OC} \approx \frac{kT_K}{q} \ln \left(\frac{I_{SC}}{I_s} \right), \quad (10.4)$$

where $I_{SC} \gg I_s$ [1]. As a consequence, the open-circuit voltage stays relatively constant when the irradiation level varies during a day. The open-circuit voltage is known, however, to be negatively dependent on the cell temperature (i.e., its temperature coefficient is negative). The temperature coefficient for silicon corresponds to about -2.5 mV/ $^{\circ}$ C at 25 $^{\circ}$ C. This means that the open-circuit cell voltage decreases approximately by 2.5 mV when the temperature increases by 1 $^{\circ}$ C. The temperature dependence of the open-circuit voltage can also be given by [2]

$$V_{OC} = V_{OC-STC} \left[1 + \alpha_v(T_C - T_{C-STC}) + a \ln \left(\frac{G}{G_{STC}} \right) \right], \quad (10.5)$$

where α_v denotes the temperature coefficient of the voltage and $a = 0.06$ according to IEC 60891. The temperature coefficients α_i (Eq. (10.3)) and α_v (Eq. (10.5)) are typically given by the manufacturer of the solar cells (i.e., included in the PV panel data sheet).

In practice, the cell also contains series (r_s) and parallel (r_p) resistances (cf. Figure 10.4a), which actually affect the I–V characteristics as well: The effect is visible as an increase in the slopes of the I–V curve. When the resistive losses are taken into account, the I–V characteristics can be given by [2]

$$i_{pv} = i_{ph} - I_s \left(\exp(q(v_{pv} + r_s i_{pv}) / \eta k T_K) - 1 \right) - \frac{v_{pv} + r_s i_{pv}}{r_p}. \quad (10.6)$$

It is well known that the amount of current flowing through a silicon diode is reflected as diode dynamic resistance (r_d) and also as dynamic capacitance (c_d), which is naturally dependent on the operating point of the cell and are connected in parallel with r_p . From the power electronics point of view, the solar cell can be seen in small-signal sense as an operating point-dependent constant current source with an impedance structure, as depicted in Figure 10.4b [8]. Therefore, the small-signal source impedance can be given by

$$Z_{pv} = r_s + \frac{r_p \parallel r_d}{1 + s(r_p \parallel r_d)c_d} \approx r_s + \frac{r_d}{1 + sr_d c_d} \approx \frac{r_d}{1 + sr_d c_d}. \quad (10.7)$$

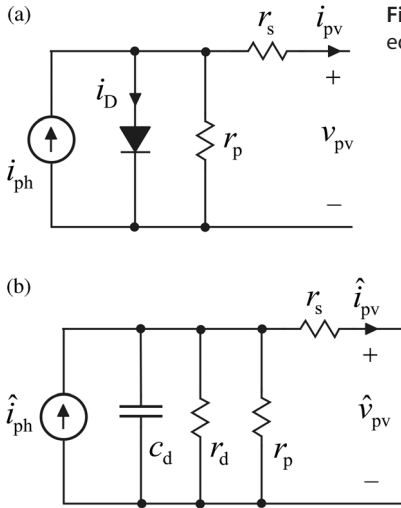


Figure 10.4 Solar cell equivalent circuits. (a) Practical equivalent circuit. (b) Its small-signal equivalent.

Figure 10.5 shows the behavior of the cell output resistance ($r_{pv} \approx r_s + r_d$) and output capacitance ($c_{pv} \approx c_d$) measured at the output terminal when the operating point is changed from the short circuit to open circuit. The figure depicts clearly that the output impedance of the solar cell in the CCR is very much higher than the output impedance in the CVR, which supports the classification of the regions to CCR and CVR.

From the power electronics point of view, the behavior of the dynamic (r_{pv}) and static ($R_{pv} = V_{pv}/I_{pv}$) resistances of the solar cell is very important, because the dynamic changes in the power electronic interfacing converters are dependent on the ratio of the dynamic and static resistances [8]. Figure 10.6a shows the behavior

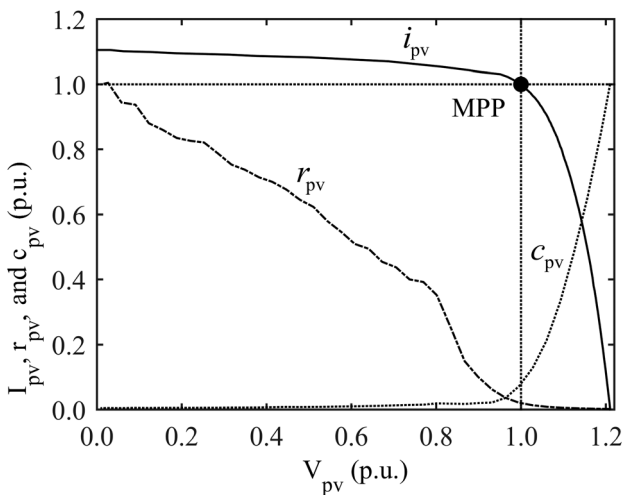


Figure 10.5 The terminal characteristics of a solar cell including the dynamic resistance and capacitance.

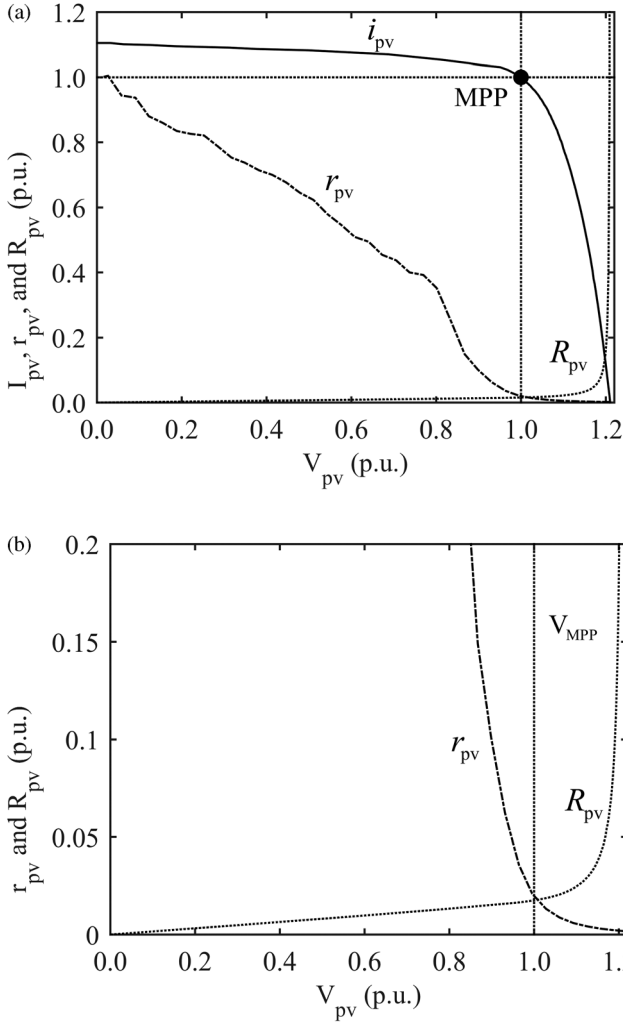


Figure 10.6 The behavior of dynamic (r_{pv}) and static (R_{pv}) resistances. (a) General view. (b) Extended view.

of the dynamic and static resistances when the operating point is varied from short circuit to open circuit. It is quite evident that in the CCR $r_{pv} \gg R_{pv}$, and in the CVR $r_{pv} \ll R_{pv}$.

According to Figure 10.3, it may be obvious that $dp_{pv}/dv_{pv} = 0$ at the MPP. According to this knowledge, we can derive that

$$\left[\frac{dp_{pv}}{dv_{pv}} \right]_{MPP} = \left[\frac{d(i_{pv}v_{pv})}{dv_{pv}} \right]_{MPP} = V_{MPP} \frac{di_{pv}}{dv_{pv}} + I_{MPP} = 0 \tag{10.8}$$

$$\rightarrow -\frac{di_{pv}}{dv_{pv}} = \frac{I_{MPP}}{V_{MPP}}.$$

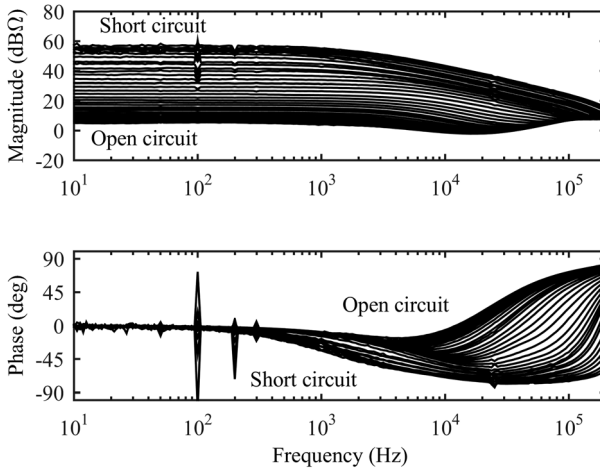


Figure 10.7 Measured output impedance of solar cell when the operating point is varied from short circuit to open circuit.

When the dynamic resistance (r_{pv}) corresponds to the inverse of the derivative of the I–V curve as

$$1/r_{pv} = -\frac{di_{pv}}{dv_{pv}}, \quad (10.9)$$

we can conclude that $r_{pv} = R_{pv}$ at the MPP as well as that the dynamic resistance is also a positive value and not a negative value as the outcome of Eq. (10.8) would imply if not carefully considering the behavior of the I–V curve slope. This can also be extended to the cases of multiple MPPs, that is, $r_{pv-MPP-i} = R_{pv-MPP-i}$.

In many publications, r_{pv} is, however, considered to be a negative incremental resistance value as, for example, in Refs [9,10] based on the behavior of the input impedance in an output-regulated power electronics converters, where the low-frequency input impedance behaves as a negative resistance, as we have discussed in Chapters 2–5. According to the theory we have presented in the previous chapters, the low-frequency output impedance of a constant power-type source equals approximately V_o/I_o , while the low-frequency input impedance of the output side-regulated power electronic converter equals approximately $-V_{in}/I_{in}$. Therefore, r_{pv} clearly equals positive resistance as the measurements in Figure 10.7 also show. The output impedance also resembles an RC circuit, as depicted in Figure 10.4b. In practice, the connection cabling would also introduce some amount of series inductance, and thus, the output of the PV generator may also contain a series resonant circuit, where the resonant frequency varies along the changes in the operating point (cf. Figure 10.5; the behavior of the capacitance).

10.3 PV Generator

The maximum voltage of one solar cell is in the order of 0.5 V, which is usually too low for powering switched-mode converters. Therefore, the practical PV

generators are composed of series connection of solar cells forming *PV modules*, which are further connected in series as *PV panels* [2]. Typical panels compose of three series connected modules having up to 60 cells in series and the output power up to 250 W. The open-circuit voltage of such panels is in the order of 40 V, which is sufficient for certain applications. In the grid-connected applications, the output voltage of the PV generators has to be in the order of the peak of the AC voltage or more [11]. Therefore, a number of PV panels is usually connected in series forming an entity known as a *PV string* to satisfy the higher voltage requirements. To extend the power of the strings, they are usually connected in parallel forming an entity known as *PV array*.

I–V and P–V characteristics of a PV array can be given similarly to a single cell in Eq. (10.6) by using the parameters of a single cell as follows:

$$i_{pv} = N_p i_{ph} - N_p I_s \left(\exp \left(q \left(v_{pv} + \frac{N_s}{N_p} r_s i_{pv} \right) / N_s \eta k T_K \right) - 1 \right) - \frac{v_{pv} + (N_s/N_p) r_s i_{pv}}{(N_s/N_p) r_p}, \quad (10.10)$$

where N_s denotes the number of series-connected cells and N_p the number of parallel-connected strings, i_{pv} and v_{pv} denote the terminal variables of the PV array, and i_{ph} , I_s , r_s , and r_p denote the properties of a single cell, respectively. If the resistive losses are identified from the physical entity, then $(N_s/N_p)r_s$ and $(N_s/N_p)r_p$ in Eq. (10.11) will be substituted with the corresponding identified values.

The series-connected cells will work properly only if the irradiation over the cells is uniformly distributed. In practice, a part of the cells can be shaded by the shadows from the nearby obstacles such as trees, chimneys, flag poles, other structures of the adjacent building, and passing-by clouds [12,13]. As a consequence of the shading effects, the irradiation can vary by large extent. During the shading conditions, a part of the cells can become reverse biased and the rather high power loss can even damage the cells. In order to protect the cells from damage, the modules are provided with a shunt diode limiting the reverse voltage approximately to the forward voltage drop of a diode [11]. Therefore, each panel contains usually three bypass or shunt diodes. Figure 10.8 shows authentic I–V and P–V curves measured from a PV string composing 17 PV panels in series [14]. During the uniform irradiation conditions, there exists only one MPP, as illustrated in Figure 10.8a. Figures 10.8b and c show the effect of shadowing from the passing-by clouds, which can create multiple MPPs. In all the cases in Figure 10.8, the absolute maximum or global maximum MPP occurs at the high voltage. The practical situation can vary so that the global MPP can occur even at the low voltages.

Figure 10.9 shows the measured I–V and P–V curves of two panels composing of 36 cells in series, which are connected in series and exposed to different irradiation levels, that is, Panel 1: 500 W/m^2 and $I_{sc} \approx 1.0 \text{ A}$ and Panel 2: 167 W/m^2 and $I_{sc} \approx 0.3 \text{ A}$. The both of the panels are equipped with a bypass diode. In this case, the global MPP occurs at the low voltage as clearly shown in the figure.

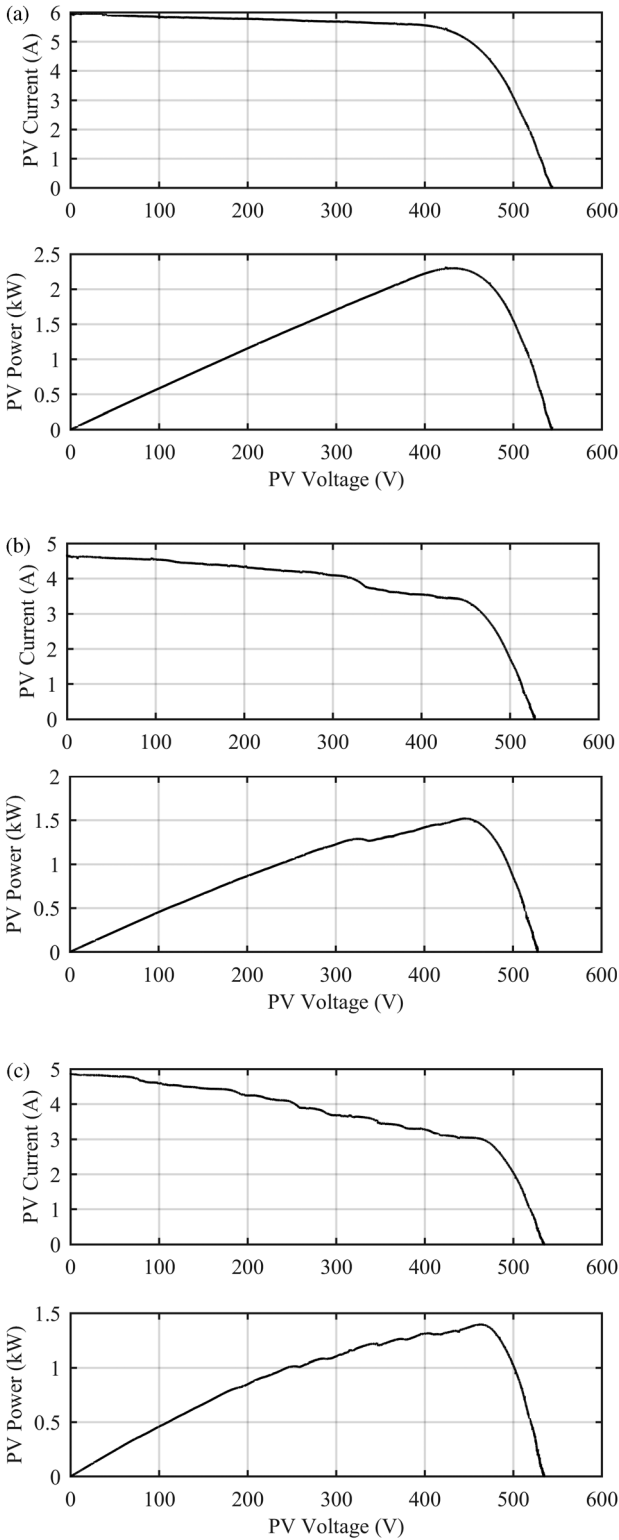


Figure 10.8 Measured I-V and P-V curves from a 17-series panel string. (a) Single MPP. (b) Two MPPs. (c) Multiple MPPs.

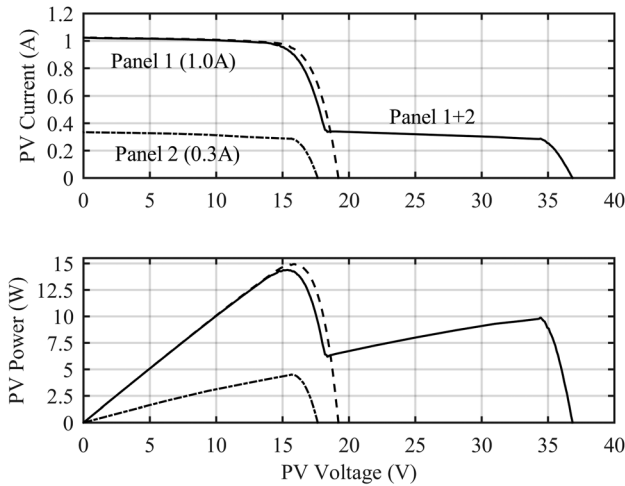


Figure 10.9 The measured I–V and P–V curves of cascaded panels subjected to shading effect.

Figure 10.10 shows the behavior of the dynamic and static resistances when the operating point is varied. According to the figure, the operating range is divided into two CC and CV regions, that is, the CC region exists at the voltages less than the MPP, and the CV region exists at the voltages higher than the MPP. The CV region is clearly the narrowest of the regions between the adjacent MPPs. At the MPPs, $r_{pv} \approx R_{pv}$, as discussed in Section 10.2.

According to Ref. [2], the usual irradiance slope is considered to be $30 \text{ W/m}^2/\text{s}$, which is used for different design purposes such as MPP tracking control. The actual measurements [14] show that the irradiance slope can be even higher than $30 \text{ W/m}^2/\text{s}$ during the irradiance enhancement conditions (cf. Figure 10.11a; the peaks higher than 1 kW/m^2) caused by the passing-by clouds. The maximum peak irradiance in Figure 10.12a is 1343 W , which is close to the values reported in Refs [15–17]. Figure 10.11b shows an extended view around the maximum irradiance peak in Figure 10.11a at noon of the particular day the data were recorded.

An 8-kW single-phase inverter was connected to the PV string subjected to the irradiance changes in Figure 10.11a. The grid-current of the inverter shown in Figure 10.12 indicates clearly that the dynamic behavior of the irradiance directly affects the grid current, which may cause power balance problems in grid if the penetration level of PV-based renewable sources is high. The irradiation enhancement should also be taken into consideration in the design of the inverters and selection of the inverter size in respect to the PV generator power rating, as discussed in Refs [15–17].

10.4 MPP Tracking Methods

The MPP tracking techniques can be classified into passive, hill climbing, perturb and observe, incremental conductance, and stochastic methods [3–6]. The passive methods are usually based on the approximate knowledge on the location

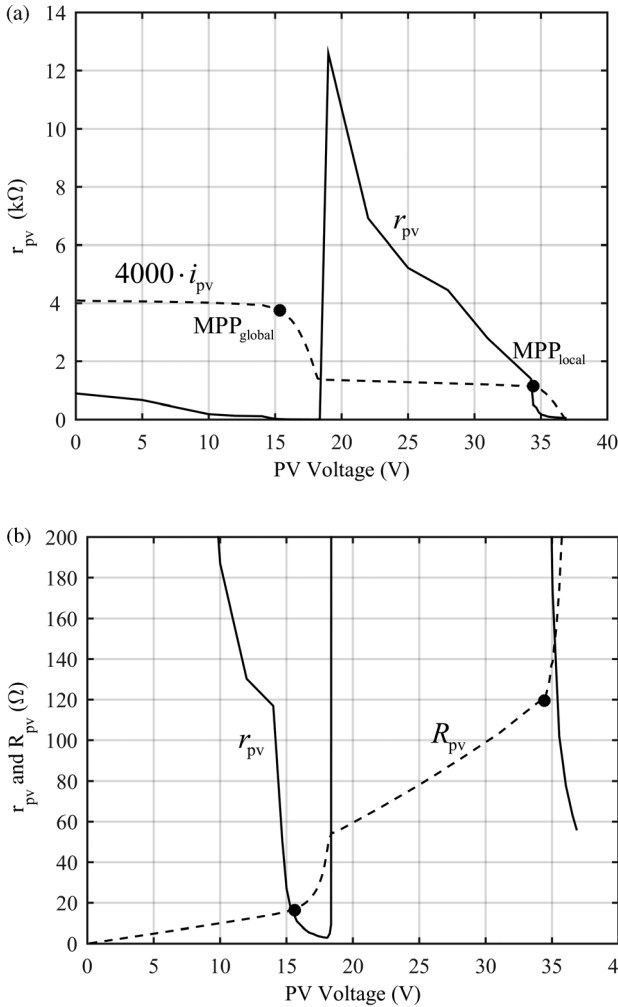


Figure 10.10 Measured behavior of the dynamic and static resistances in shaded condition. (a) Overall behavior r_{pv} . (b) Extended view of the behavior of r_{pv} and R_{pv} when the operating point varies.

of the MPP through the fill factor of the PV array and measurement of short-circuit current and/or open-circuit voltage. The fill factor (FF) is defined as [1]

$$FF = \frac{I_{MPP} V_{MPP}}{I_{sc} V_{oc}}, \quad (10.11)$$

where the denominator corresponds to the maximum theoretical power involved in the conversion process and the numerator to the maximum practical power, which can be taken out of the PV generator. The fill factor typically varies within the range of 0.6–0.8. Based on Figure 10.3, we can compute the fill factor to equal 0.758. Figure 10.3 also indicates that the short circuit current is close to the MPP current. Based on this approximation, the MPP voltage can be computed based on Eq. (10.11). The passive methods can also directly use empirical knowledge to

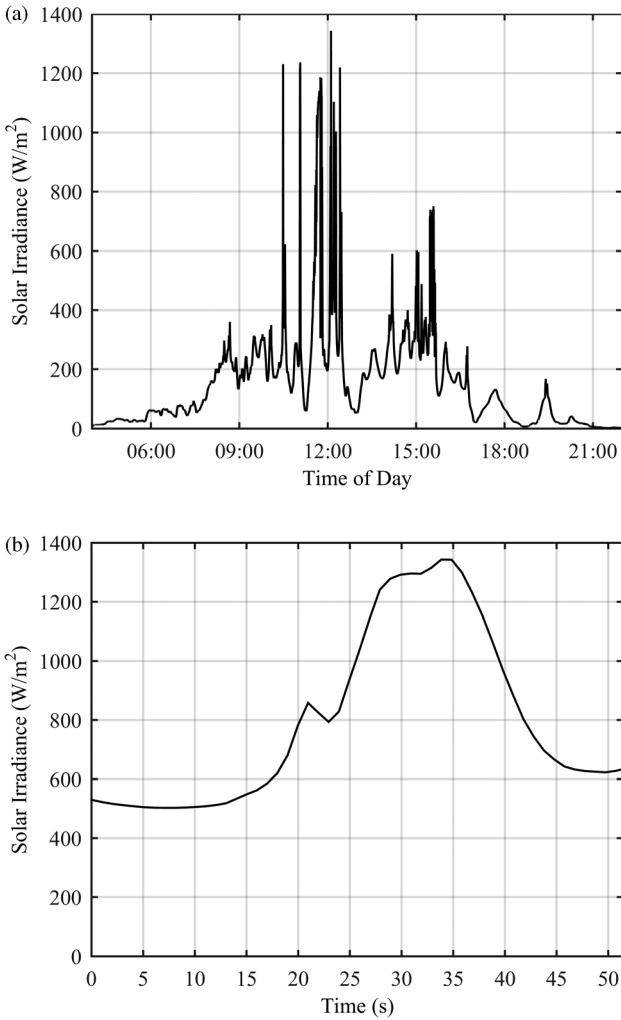


Figure 10.11 The behavior of irradiance during a particular half cloudy day. (a) All day. (b) An extended view around the maximum irradiance peak of 1343 W/m^2 at noon.

relate the MPP voltage and current to the corresponding values of open-circuit voltage and short-circuit current as discussed in Ref. [6] by

$$\begin{aligned} V_{\text{MPP}} &\approx k_1 V_{\text{oc}}, \\ I_{\text{MPP}} &\approx k_2 I_{\text{sc}}, \end{aligned} \quad (10.12)$$

where the factor k_1 has been reported to vary between 0.71 and 0.78 as well as the factor k_2 between 0.78 and 0.92. It should be known that these methods would very seldom give the exact location of the MPP, but only its rough estimation. The MPP can also be naturally found by measuring the whole I–V curve at fixed time intervals and extracting the MPP from the recorded data points. All of these methods require interrupting the energy supply during the measurement of the desired variables, thus wasting the available energy.

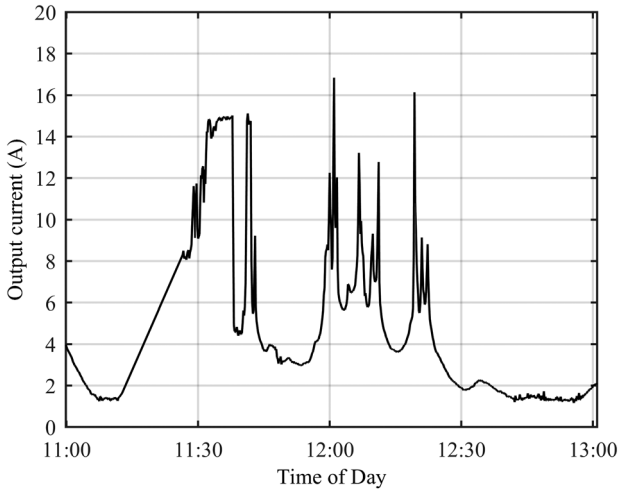


Figure 10.12 The behavior of the inverter grid current during the irradiance changes.

The hill climbing, perturb and observe, and incremental conductance methods are working online. All of them require to inject a step change in one of the PV variables and to observe the corresponding change in the other PV variable. Based on these changes, the change in the PV power (i.e., the derivative of the PV power in terms of the perturbed variable) or the dynamic resistance can be approximated.

Hill climbing and perturb and observe methods will locate the MPP by observing the behavior of the voltage derivative of the PV power (cf. Figure 10.13): If the derivative is positive, the operation point locates at the voltages less than the MPP, and if the derivative is negative, the operation point locates at the voltages

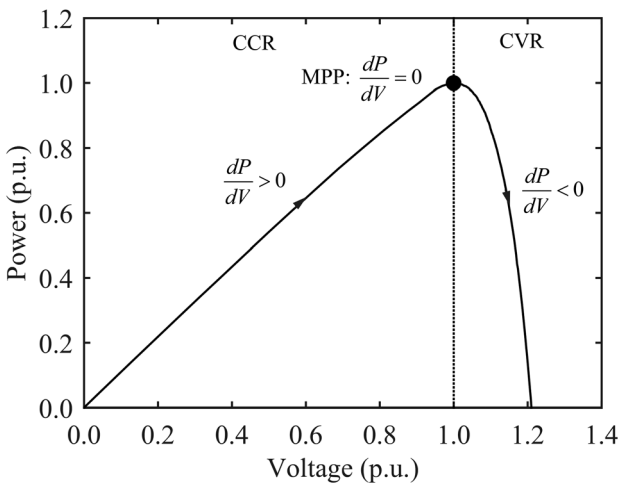


Figure 10.13 The behavior of dP_{pv}/dV_{pv} when the operating point changes due to incrementing V_{pv} .

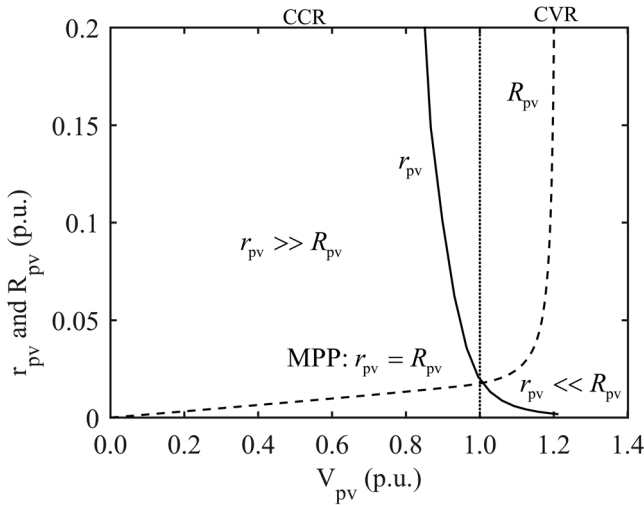


Figure 10.14 The behavior of PV generator dynamic and static resistances when the operating point varies.

higher than the MPP. At the MPP, the derivative is zero. By performing successive perturb and observe cycles, the operation will finally oscillate between three points, which are located so that the middle point is at the MPP and the two others close to the MPP.

The incremental conductance method will apply the same perturb and observe cycles as already described, but observe the relation between the PV generator dynamic and steady-state resistances [18,19]. As shown in Figure 10.14, $r_{pv} \gg R_{pv}$ in the CCR, $r_{pv} = R_{pv}$ at MPP, and $r_{pv} \ll R_{pv}$ in the CVR. The differences in the resistances in the different regions are very clear, and therefore, quite easy to locate the MPP.

The MPP can also be identified by observing the behavior of the PV power ripple when the operating point is varying [20,21], as depicted in Figure 10.15, which is produced by injecting a 100-Hz ripple component at PV voltage at each operating point. The MPP can be found by identifying the location of the minimum ripple point at the PV power. The ripple can be induced by the power electronic converters, the pulsating power of the grid, or specially generated by the MPP tracking controller.

There are numerous other methods applying genetic, fuzzy logic, and neural network-based techniques, as introduced in Refs [2–6], but their introduction in the context of the book is not, however, feasible.

10.5 MPP Tracking Design Issues

10.5.1 Introduction

The MPP tracking converters can be operated at open loop, that is, the perturbation is applied directly to the duty ratio of the corresponding converter

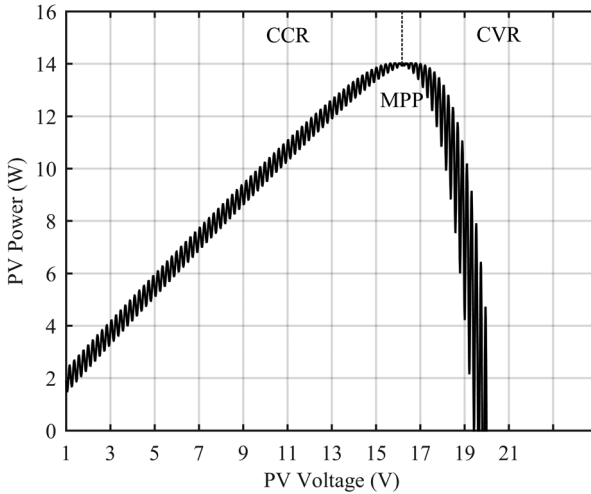


Figure 10.15 The behavior of PV power ripple induced by the ripple at PV voltage when the operating point is varied.

or at closed loop, where the feedback variable is the PV voltage and the perturbation is applied to the reference of PV voltage [22]. The controlled variable cannot actually be the PV current because of the current-source nature of the PV generator, which would cause violation in the Kirchhoff's current law and saturation of the controller especially during the varying climatic conditions, as discussed and demonstrated explicitly in Ref. [23]. The MPP tracking design variables are the size of perturbation step and the sampling frequency of the PV voltage and current, which is usually also the same as the perturbation frequency. If the size of the perturbation step is too small and/or the sampling frequency is too high, then the MPP tracking process can become unstable, because the computed voltage derivative of the PV power does not comply with the real derivative [2,24,25]. The reasons for the errors can be the change of irradiance level, the ripple in the measured variables, or the transient settling process of the corresponding power electronic converters [2].

10.5.2 General Dynamics of PV Power

Figure 10.16 shows a grid-connected two-stage PV system, where PV interface can be disturbed by the change in irradiation (i.e., direct effect on the photovoltaic current i_{ph}), the settling behavior of the DC–DC converter, and the ripple at the

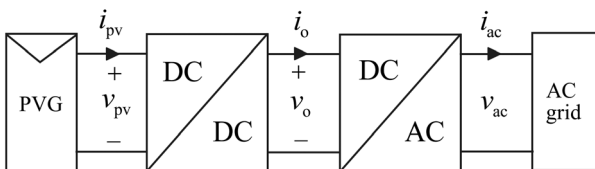


Figure 10.16 A grid-connected two-stage PV system.

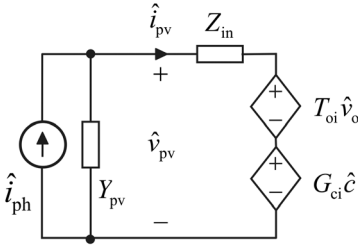


Figure 10.17 The dynamic representation of the PV generator-converter interface. *Source:* Kivimaki 1969. Reproduced with permission of IEEE.

DC-link voltage caused, for example, by the grid power fluctuation at twice the grid frequency. In order to capture the effect of these noise sources on the behavior of the PV power (p_{pv}), voltage (v_{pv}), and current (i_{pv}), the dynamic constellation of the PV generator-converter interface can be given as shown in Figure 10.17, where all the vital elements are considered. The notation \hat{c} in Figure 10.17 denotes the duty ratio (\hat{d}) when the DC-DC converter is applied at open loop and the PV voltage reference (\hat{v}_{ref-pv}) when the DC-DC converter is applied at closed loop. In principle, all the information given below is equally valid for a single-stage PV system but the analysis of such a system may be more challenging due to the complexity of the inverter. It shall also be understood that the controlled source elements (i.e., G_{ci} and T_{oi}) can be affected by the load impedance or the inverter input impedance, which can naturally change the dynamic behavior of the DC-DC converter.

According to Figure 10.17, we can compute that the dynamics related to the PV voltage and current can be given by

$$\hat{v}_{pv} = \frac{Z_{in}}{1 + Z_{in}Y_{pv}} \hat{i}_{ph} + \frac{T_{oi}}{1 + Z_{in}Y_{pv}} \hat{v}_o + \frac{G_{ci}}{1 + Z_{in}Y_{pv}} \hat{c} \quad (10.13)$$

and

$$\hat{i}_{pv} = \frac{1}{1 + Z_{in}Y_{pv}} \hat{i}_{ph} - \frac{Y_{pv}T_{oi}}{1 + Z_{in}Y_{pv}} \hat{v}_o - \frac{Y_{pv}G_{ci}}{1 + Z_{in}Y_{pv}} \hat{c}. \quad (10.14)$$

As discussed earlier, the temperature of the panels has quite significant effect on the PV generator voltage and hence, on the PV power but its dynamics is quite slow due to the large thermal capacity of the PV panels. Therefore, its effect is not taken into account into the dynamic models in Eqs (10.13) and (10.14) but naturally affects the operating point variables and parameters.

The dynamics related to the PV power can be approximated as follows [2]:

$$\hat{p}_{pv} = V_{pv} \hat{i}_{pv} + I_{pv} \hat{v}_{pv} + \hat{i}_{pv} \hat{v}_{pv} \quad (10.15)$$

based on the definition of power in terms of voltage and current (i.e., $p_{pv} = (V_{pv} + \hat{v}_{pv})(I_{pv} + \hat{i}_{pv})$) and discarding the steady-state state value at the operating point. If considering only the dynamic behavior of the PV power

induced by a step-change at the operation point of the DC–DC converter (i.e., $\hat{i}_{\text{ph}}(\hat{G}) = 0$, and $\hat{v}_o = 0$ in Eqs (10.13) and (10.14)), then Eq. (10.15) can be given by

$$\hat{p}_{\text{pv}} \approx V_{\text{pv}} \left(\frac{1}{R_{\text{pv}}} - \frac{1}{r_{\text{pv}}} \right) \hat{v}_{\text{pv}} - \frac{\hat{v}_{\text{pv}}^2}{r_{\text{pv}}} \quad (10.16)$$

because

$$\hat{i}_{\text{pv}} \approx -\frac{1}{r_{\text{pv}}} \hat{v}_{\text{pv}}. \quad (10.17)$$

According to Eq. (10.16), we can state that the PV power ripple can be defined in CCR by $\hat{p}_{\text{pv}} \approx I_{\text{pv}} \hat{v}_{\text{pv}}$ (i.e., $r_{\text{pv}} \gg R_{\text{pv}}$), in CVR by $\hat{p}_{\text{pv}} \approx -(V_{\text{pv}}/r_{\text{pv}}) \hat{v}_{\text{pv}} = V_{\text{pv}} \hat{i}_{\text{pv}}$ (i.e., $r_{\text{pv}} \ll R_{\text{pv}}$), and at MPP by $\hat{p}_{\text{pv}} \approx -(\hat{v}_{\text{pv}}^2/R_{\text{pv}})$ (i.e., $r_{\text{pv}} = R_{\text{pv}}$) based on the behavior of r_{pv} and R_{pv} at the different operating points of the PV generator (cf. Section 10.2).

Figure 10.18 shows the effect of the PV voltage perturbation on the PV power. According to the figure, the ripple of PV power is constant and in phase with the PV voltage ripple in CCR, zero at MPP, and increasing along the increase in PV voltage with 180° phase shift with the PV voltage ripple in CVR. This kind of behavior is exactly as the developed PV power ripple in Eq. (10.15) predicts to be happening. The extended plot of the operating points in the vicinity of the MPP reveals explicitly that the MPP is not just a point but also a narrow region, that is, a constant power region (CPR) as also discussed in Ref. [9]. The MPP tracking parameter design issues are usually treated in CPR [2,24,25], where the PV voltage perturbation effect on the PV power is actually minimized. We will study the validity of the proposed technique in more detail in the subsequent sections by means of the boost power-stage converter (cf. Figure 10.19) modeled in Chapter 8.

10.5.3 PV Interfacing Converter Operating at Open Loop

The power electronic converter operating at open loop exhibits usually resonant behavior in the transient conditions that would extend the settling process. The boost power-stage converter (cf. Figure 10.19) is commonly used as an MPP tracking converter. The discussions in the subsequent paragraphs and sections are not limited by no means only to a boost converter but equally applicable to other type of converters as well.

As discussed earlier, the dynamic resistance r_{pv} of the PV generator is the element in PV generator, which actually significantly affects the dynamic behavior of the power electronic converter. In this case, the control-to-PV-voltage transfer function $G_{\text{ci-o}}$ will be responsible on the transient behavior of the PV interface, as implied explicitly in Eqs (10.13) and (10.14). The detailed modeling of the boost power-stage converter has been presented earlier in Chapter 8.

If assuming that the PV generator is an ideal current source (i.e., in CCR), then $G_{\text{ci-o}}$ can be given by [26]

$$G_{\text{ci-o}} = -\frac{V_e(1 + sr_{\text{C2}}C_2)}{s^2L_1C_2 + sr_eC_2 + 1}, \quad (10.18)$$

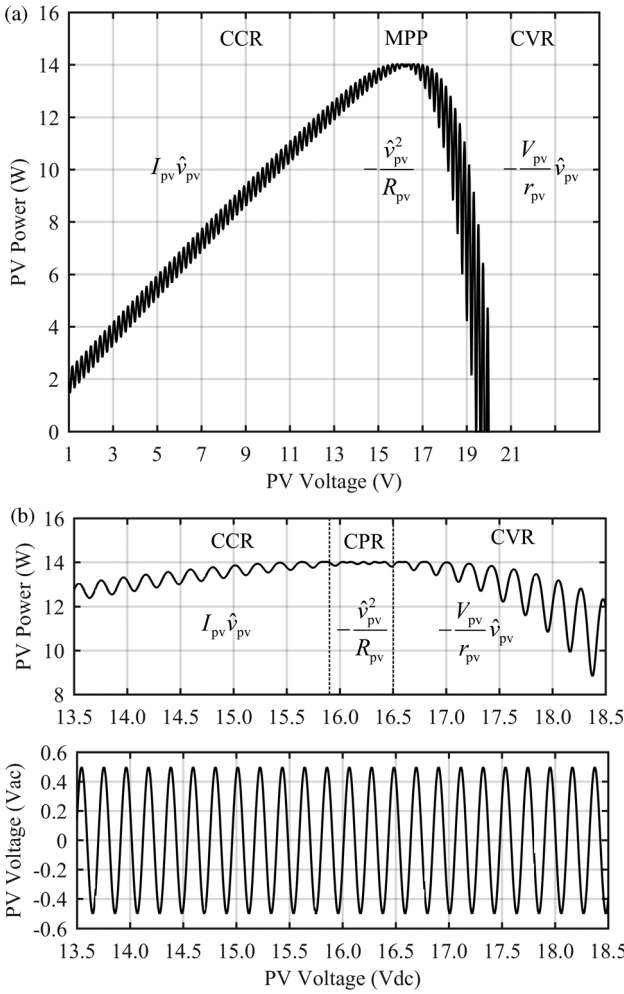


Figure 10.18 Effect of PV voltage perturbation on the PV power. (a) The operation points from short circuit to open circuit. (b) The operation points in the vicinity of the MPP. Source: Kivimaki 1969. Reproduced with permission of IEEE.

where the DC gain of G_{ci-o} (V_e) and the equivalent loss resistance (r_e) are as follows:

$$\begin{aligned} V_e &= V_o + V_D + (r_d - r_{ds})I_{pv}, \\ r_e &= r_{L1} + r_{C2} + Dr_{ds} + D'r_d. \end{aligned} \tag{10.19}$$

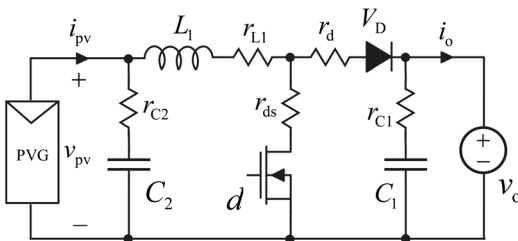


Figure 10.19 PV generator interfacing boost power-stage converter.

The negative sign of G_{ci-o} is the consequence of operating the power-stage switches similarly as in the corresponding voltage-fed converter. This means that the conduction time of the MOSFET has to be decreased for increasing the PV voltage. The positive sign can be recovered by inverting the gate drive signal [27].

The PV generator-affected (i.e., by r_{pv}) G_{ci-o}^{pv} can be given by

$$G_{ci-o}^{pv} = \frac{G_{ci-o}}{1 + Z_{in-o} Y_{pv}}, \quad (10.20)$$

according to Eq. (10.13), where

$$Z_{in-o} = \frac{(r_e - r_{C2} + sL_1)(1 + sr_{C2}C_2)}{s^2L_1C_2 + sr_eC_2 + 1}. \quad (10.21)$$

When replacing Y_{pv} by $1/r_{pv}$, G_{ci-o} by Eq. (10.18), and Z_{in-o} by Eq. (10.21) in Eq. (10.20), we get

$$G_{ci-o}^{pv} = - \left\{ [V_e(1 + sr_{C2}C_2)] / \left[s^2L_1C_2 \left(1 + \frac{r_{C2}}{r_{pv}} \right) + s \left(\frac{L_1}{r_{pv}} + C_2 \left(r_e + \frac{r_{C2}}{r_{pv}}(r_e - r_{C2}) \right) \right) + 1 + \frac{r_e - r_{C2}}{r_{pv}} \right] \right\}. \quad (10.22)$$

Usually $r_{pv} \gg r_{C2}$ and r_e , and hence, Eq. (10.22) can be approximated by

$$G_{ci-o}^{pv} \approx - \frac{V_e(1 + sr_{C2}C_2)}{s^2L_1C_2 + s((L_1/r_{pv}) + C_2r_e) + 1}, \quad (10.23)$$

which means that r_{pv} affects the damping of the resonant behavior in the converter as follows:

$$\zeta_{pv} \approx \frac{1}{2} \left(r_e \sqrt{\frac{C_2}{L_1}} + \frac{1}{r_{pv}} \sqrt{\frac{L_1}{C_2}} \right). \quad (10.24)$$

All the PV generator interfacing converters have to be equipped with an input capacitor (i.e., if not existing in the original converter) to satisfy the terminal constraints stipulated by the constant current input source [8,28]. Therefore, the control-to-input-voltage transfer function will always incorporate an ESR zero at $1/r_{C2}C_2$ as in (11.18). Hence, G_{ci-o}^{pv} in Eq. (10.23) can be given in a generalized form for the second-order converters under direct duty ratio control by

$$G_{ci-o}^{pv} \approx \frac{V_e \omega_n^2 (1 + s/\omega_{z-esr})}{s^2 + s2\zeta_{pv}\omega_n + \omega_n^2}. \quad (10.25)$$

Therefore, the PV voltage transient induced by a step change in the duty ratio can be given in Laplace domain by (cf. Chapter 2)

$$\Delta v_{pv}(s) = \frac{V_e \omega_n^2 (1 + s/\omega_{z-esr})}{s^2 + s2\zeta_{pv}\omega_n + \omega_n^2} \cdot \frac{\Delta d}{s}, \quad (10.26)$$

which can be further developed as

$$\Delta v_{pv}(s) = V_e \Delta d \left(\frac{1}{s} - \frac{s + 2\zeta_{pv}\omega_n - (\omega_n^2/\omega_{z-esr})}{s^2 + s2\zeta_{pv}\omega_n + \omega_n^2} \right), \quad (10.27)$$

for solving the corresponding inverse *Laplace* transform (i.e., the time domain response) as

$$\begin{aligned} \Delta v_{pv}(t) = V_e \Delta d \left(1 - \frac{\sqrt{1 + (\omega_n/\omega_{z-esr})[(\omega_n/\omega_{z-esr}) - 2\zeta_{pv}]}}{\sqrt{1 - \zeta^2}} \exp(-\zeta_{pv}\omega_n t) \right. \\ \left. \cdot \sin \left[\omega_d t + \tan^{-1} \left\{ \frac{\sqrt{1 - \zeta_{pv}^2}}{\zeta_{pv} - (\omega_n/\omega_{z-esr})} \right\} \right] \right), \quad (10.28) \end{aligned}$$

where the damped natural frequency $\omega_d = \omega_n \sqrt{1 - \zeta_{pv}^2}$. The corresponding inverse transform without considering the effect of ESR zero can be given by [2,29]

$$\Delta v_{pv}(t) = V_e \Delta d \left(1 - \frac{1}{\sqrt{1 - \zeta^2}} \exp(-\zeta\omega_n t) \cdot \sin \left[\omega_d t + \tan^{-1} \left\{ \frac{\sqrt{1 - \zeta^2}}{\zeta} \right\} \right] \right). \quad (10.29)$$

According to Eqs (10.28) and (10.29), we can conclude that the ESR zero would only slightly affect the settling time of the transient, because typically $\omega_{z-esr} \gg \omega_n$, and therefore, Eq. (10.28) equals Eq. (10.29).

According to Eqs (10.16) and (10.28), we can estimate the time domain behavior of PV power when a step change in PV voltage (i.e., duty ratio) is applied as follows.

In CCR, the time domain function of PV power can be given by

$$\begin{aligned} \Delta p_{pv}(t) = I_{pv} V_e \Delta d \left(1 - A \cdot \exp(-\zeta_{pv-CCR}\omega_n t) \right. \\ \left. \cdot \sin \left[\omega_d t + \tan^{-1} \left\{ \frac{\sqrt{1 - \zeta_{pv-CCR}^2}}{\zeta_{pv-CCR} - (\omega_n/\omega_{z-esr})} \right\} \right] \right), \quad (10.30) \end{aligned}$$

and in CVR by

$$\begin{aligned} \Delta p_{pv}(t) = -\frac{V_{pv} V_e \Delta d}{r_{pv}} \left(1 - A \cdot \exp(-\zeta_{pv-CVR}\omega_n t) \right. \\ \left. \cdot \sin \left[\omega_d t + \tan^{-1} \left\{ \frac{\sqrt{1 - \zeta_{pv-CVR}^2}}{\zeta_{pv-CVR} - (\omega_n/\omega_{z-esr})} \right\} \right] \right), \quad (10.31) \end{aligned}$$

where

$$A = \frac{\sqrt{1 + (\omega_n/\omega_{z-esr})[(\omega_n/\omega_{z-esr}) - 2\zeta]}}{\sqrt{1 - \zeta^2}}. \quad (10.32)$$

The settling behavior of the PV power transient can be addressed to the behavior of the exponential functions in Eqs (10.30) and (10.31) [29]. Hence, the envelope behavior of the PV power transient in CCR and CVR can be given by

$$\Delta p_{pv}(t)_{env} = I_{pv} V_e \Delta d (1 \pm A \cdot \exp(-\zeta_{pv-CCR} \omega_n t)) \quad (10.33)$$

and

$$\Delta p_{pv}(t)_{env} = -\frac{V_{pv} V_e \Delta d}{r_{pv}} (1 \pm A \cdot \exp(-\zeta_{pv-CVR} \omega_n t)) \quad (10.34)$$

According to Eqs (10.28) and (10.29), we may conclude that the enveloped behavior of the PV voltage transient (i.e., $\Delta \hat{v}_{pv-env}$) can be given in *Laplace* domain by

$$\Delta v_{pv-env}(s) = V_e \Delta d \left(\frac{1}{s} \pm \frac{A}{s + \zeta_{pv} \omega_n} \right). \quad (10.35)$$

In Section 10.5.2, we came up to the conclusion that the transient PV power in CPR can be given by

$$\hat{p}_{pv} \approx -\frac{\hat{v}_{pv}^2}{R_{pv}}. \quad (10.36)$$

Thus, the corresponding time domain power transient behavior can be given by

$$\Delta p_{pv}(t) = -\frac{V_e^2 \Delta d^2}{R_{pv}} \left(1 - A \cdot \exp(-\zeta_{pv-CPR} \omega_n t) \cdot \sin \left[\omega_d t + \tan^{-1} \left\{ \frac{\sqrt{1 - \zeta_{pv-CPR}^2}}{\zeta_{pv-CPR} - (\omega_n/\omega_{z-esr})} \right\} \right] \right)^2, \quad (10.37)$$

and the corresponding time domain envelope behavior can be given by

$$\Delta p_{pv-env}(t) = -\frac{V_e^2 \Delta d^2}{R_{pv}} (1 \pm A \cdot \exp(-\zeta_{pv-CPR} \omega_n t))^2. \quad (10.38)$$

Further development of (10.38) yields

$$\begin{aligned} \Delta p_{pv-env}(t) \approx & -\frac{V_e^2 \Delta d^2}{R_{pv}} (1 \pm 2A_{CPR} \cdot \exp(-\zeta_{pv-CPR} \omega_n t) \\ & \pm A_{CPR}^2 \cdot \exp(-2\zeta_{pv-CPR} \omega_n t)). \end{aligned} \quad (10.39)$$

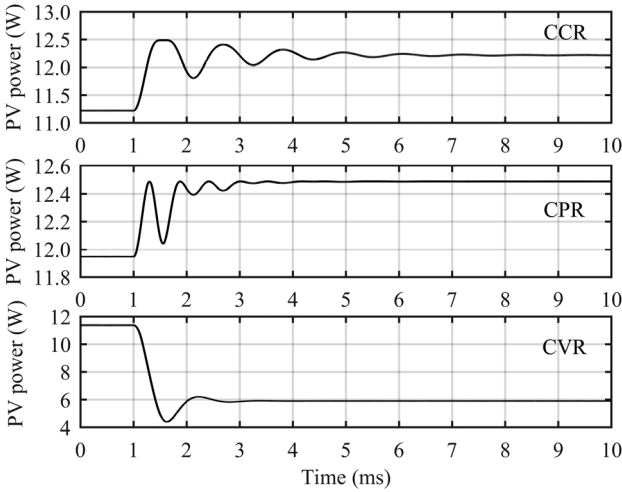


Figure 10.20 The behavior of the PV power transient in different operational regions when a step change of 0.05 in duty ratio is applied.

When the time constant of the second exponential function in Eq. (10.39) is half the time constant of the first exponential function, then the first exponential function will determine the settling time of the PV power transient, and therefore, $\Delta p_{pv-env}(t)$ can be given by

$$\Delta p_{pv}(t)_{env} \approx -\frac{V_e^2 \Delta d^2}{R_{pv}} (1 \pm 2A_{CPR} \cdot \exp(-\zeta_{pv-CPR} \omega_n t)). \quad (10.40)$$

Figure 10.20 shows the simulated PV power responses in different regions when a step change of 0.05 in duty ratio is applied. The converter used in the simulation is specified in Figure 10.23. Figure 10.20 shows clearly that the region where the settling process shall be studied is CCR. As Figure 10.18 implied, the PV power transient is very small in CPR compared to the PV power transient in the other regions. The similar transients are also shown in Figure 10.21 based on experimental measurements validating the comments given based on the simulations and the developed theory in Eq. (10.16). Figure 10.22 shows that the behavior of the PV power transient is only slightly dependent on the level of irradiation in CCR. This makes sense, because $r_{pv} \gg 1$ and therefore, the damping behavior of the resonant circuit would correspond to that of the ideal current-sourced case (cf. $\zeta_{con-in} = (r_e/2)\sqrt{(C_2/L_1)}$ in (10.24)).

Proper operation of the MPP tracking process necessitates that the PV power transient has to be settled down to a certain percentage of the final value before the measurement of i_{pv} and v_{pv} can be performed [2]. The required minimum time between the measurements (i.e., the minimum sampling interval (T_{si})) can be computed based on the exponential function given in Eq. (10.33) and the

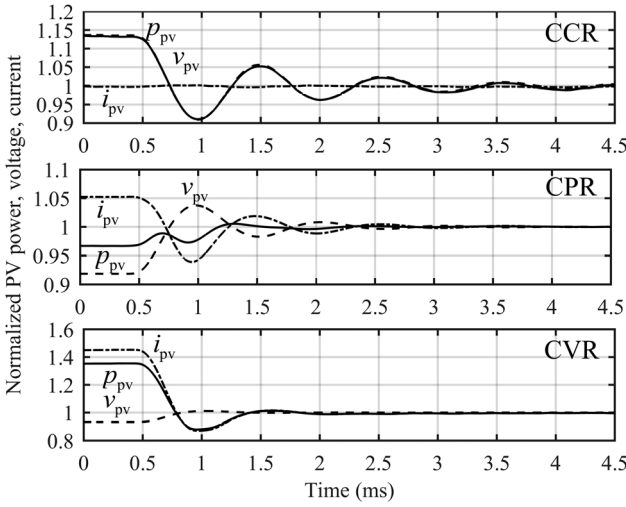


Figure 10.21 The measured transient behaviors of PV voltage, current, and power when a step change in the duty ratio of a converter is applied in CCR, CPR, and CVR. *Source:* Kivimaki 1969. Reproduced with permission of IEEE.

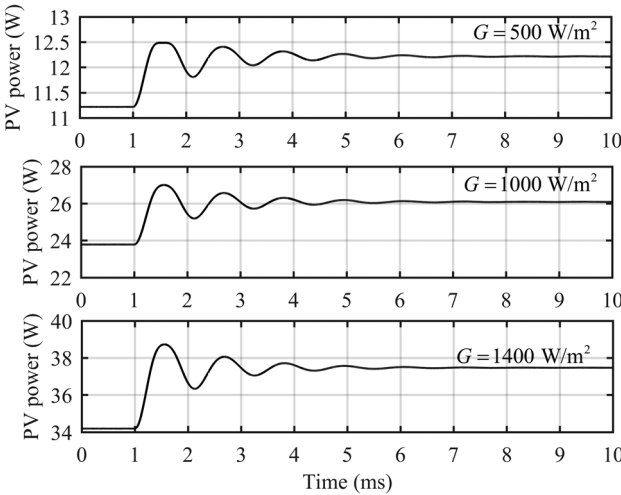


Figure 10.22 The behavior of the PV power transient in CCR when a step change of 0.05 in duty ratio is applied and the level of irradiance is varied.

specified percentage value Δ (i.e., settling band equals $(1 \pm \Delta)$ times the final value), which yields

$$\begin{aligned}
 T_{si} &= \frac{1}{\zeta_{con-in} \omega_n} \ln \frac{\sqrt{1 + (\omega_n / \omega_{z-esr})} [(\omega_n / \omega_{z-esr}) - 2\zeta_{con-in}]}{\Delta \sqrt{1 - \zeta_{con-in}^2}} \\
 &\approx \frac{1}{\zeta_{con-in} \omega_n} \ln \frac{1}{\Delta \sqrt{1 - \zeta_{con-in}^2}},
 \end{aligned}
 \tag{10.41}$$

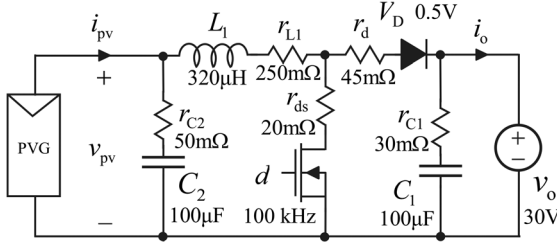


Figure 10.23 The experimental boost power-stage converter.

and which applies also for the settling time in CVR, when the damping factor is to be defined in CVR. The CPR sampling interval can be given by

$$T_{si-CPR} = \frac{1}{\zeta_{CPR}\omega_n} \ln \frac{2}{\Delta\sqrt{1-\zeta_{CPR}^2}}, \tag{10.42}$$

where the damping factor is to be defined, in practice, at the MPP.

Figure 10.23 shows the experimental boost power-stage converter with the relevant power-stage components. The used PV generator is specified as follows: $I_{sc} = 1.65 \text{ A}$, $V_{oc} = 25 \text{ V}$, $I_{MPP} = 1.5 \text{ A}$, and $V_{MPP} = 20 \text{ V}$. The operating points, where we will analyze the transient behavior of the PV power, are selected to be 1.6 A and 15 V (CCR), MPP, and 0.7 A and 23 V (CVR). The measured dynamic resistances (r_{pv}) are 66.0 Ω (CCR), 10.6 Ω (MPP), and 1.4 Ω (CVR).

According to Eqs (10.23)–(10.25), we can conclude that $\omega_n = 1/\sqrt{L_1C_2} \approx 5.56 \times 10^3 \text{ rad/s}$, $\omega_{z-esr} = 1/r_{C2}C_2 \approx 2 \times 10^5 \text{ rad/s}$, $\zeta_{pv} = (1/2r_{pv})\sqrt{(L_1/C_2) + (r_e/2)\sqrt{(C_2/L_1)}}$, and $r_e = r_{L1} + r_{C2} + Dr_{ds} + D'r_d$. The complement of the duty ratio can be solved from

$$D' = \frac{V_{pv} - (r_{L1} + r_{ds})I_{pv}}{V_o + V_D + (r_d - r_{ds})I_{pv}}. \tag{10.43}$$

Based on the given information, the damping factor ζ_{pv} can be computed to be 0.092 in CCR, 0.179 at MPP, and 0.734 in CVR. Hence, the minimum sampling intervals can be computed to be 4.5 ms in CCR, 3.0 in CPR, and 0.65 ms in CVR. Hence, it is quite clear that the CCR value should be used as the base for designing the sampling frequency (i.e., $1/T_{si}$). As discussed earlier, the damping factor ζ , which shall be used for computing the time constant $\tau = 1/\zeta\omega_n$, is the internal damping factor of the converter without the need to consider the source effect. Thus, the design of the sampling frequency is very deterministic and totally governed by the design of the converter. Figure 10.24 shows the behavior of the PV voltage, current, and power when the MPP tracking is in progress. The wave forms in Figure 10.24 show clearly that the operating point will visit all the regions during the MPP tracking operation in vicinity of the MPP, which further emphasizes the necessity to design the sampling frequency in CCR.

As discussed in Refs [24,25], the ripple induced from the DC-link would also disturb the MPP tracking process and would require to be taken into account in

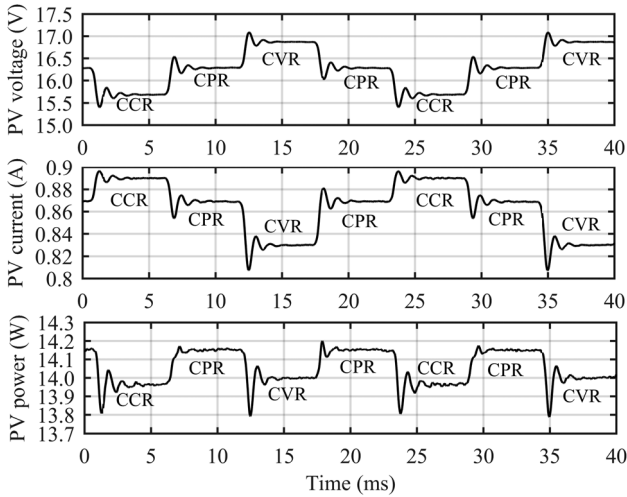


Figure 10.24 The wave forms of PV voltage, current, and power when the MPP tracking is active. Source: Kivimaki 1969. Reproduced with permission of IEEE.

selecting the correct perturbation step in the duty ratio. The attenuation of the DC-link ripple is governed by

$$\frac{\hat{v}_{pv}}{\hat{v}_o} = \frac{T_{oi}}{1 + Z_{in}Y_{pv}}, \quad (10.44)$$

which can be given at open loop for the boost converter by

$$T_{oi-o}^{pv} \approx \frac{D(1 + srC_2C_2)}{s^2L_1C_2 + s((L_1/r_{pv}) + C_2r_e) + 1}. \quad (10.45)$$

Figure 10.25 shows the frequency response of T_{oi-o}^{vp} . If the converter should attenuate sufficiently the DC-link voltage noise, then the resonant frequency should be designed much lower than the frequency of the noise voltage. In order to fulfill this requirement, the input capacitor should be increased significantly. The significant increase in the size of the input capacitor would actually also decrease the settling time of the PV power transient.

As discussed in Section 8.5, the attenuation of the DC-link ripple can be improved at open loop by applying output voltage feedforward technique. Figure 10.26a shows the DC-link ripple of 100 Hz and the corresponding PV voltage ripple when the output voltage feedforward is not active. Figure 10.26b shows the same voltage ripples when the output voltage feedforward is activated in a boost power-stage converter. The effect is significant. The detailed implementation of the scheme in a boost power-stage converter can be found from Ref. [30].

10.5.4 PV Interfacing Converter Operating at Closed Loop

The boost power-stage converter in Figure 10.23 was equipped with an input voltage control loop having crossover frequency of 10 kHz and phase margin (PM) of 50° by using a PID-type controller (Eq. (10.49)) (cf. Figure 10.27) as well as an

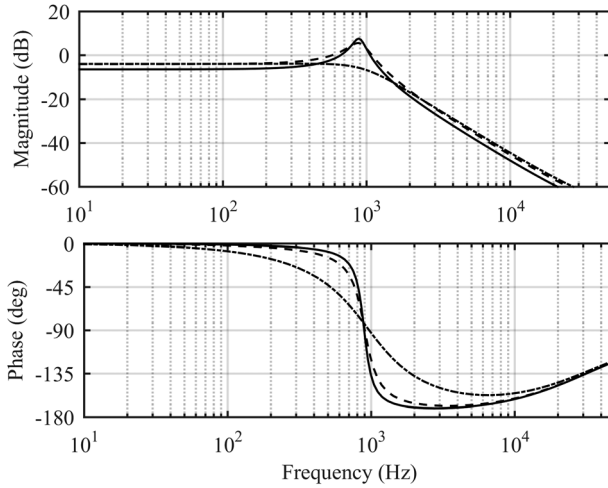


Figure 10.25 The PV generator-affected frequency response of the output-to-input voltage transfer function.

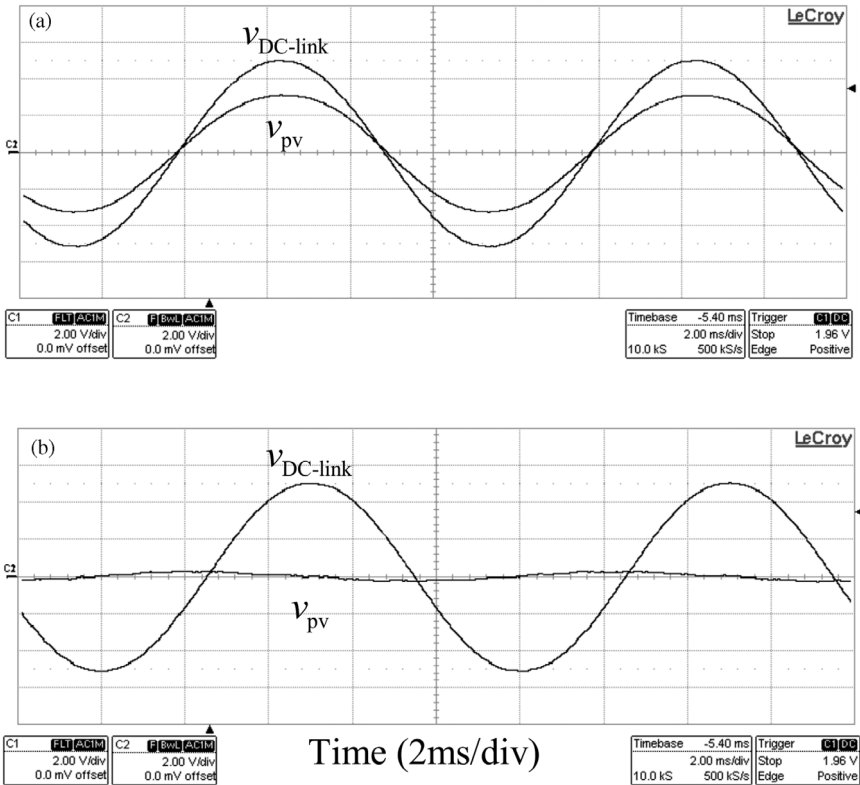


Figure 10.26 Attenuation of DC-link-induced ripple at PV voltage. (a) No DC-link voltage feedforward. (b) Feedforward activated.

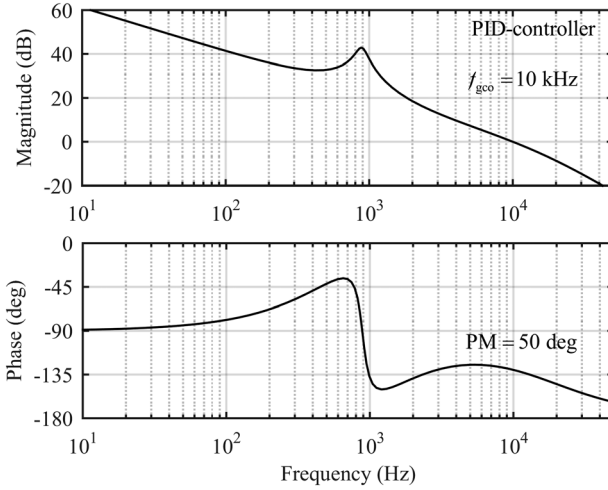


Figure 10.27 The input voltage loop gain with PID controller.

I-type controller (Eq. (10.50)) having the crossover frequency of 50 Hz and PM close to 90° (cf. Figure 10.28). The PV generator-affected loop gain can be given by

$$L_{in}^{PV} = G_{se} G_a G_{cc} G_{ci-o}^{PV}, \tag{10.46}$$

where $G_{se} = 1$, $G_a = 1/3 \text{ V}$, G_{ci-o}^{PV} as defined in Eq. (10.23), and G_{cc} as defined in Eqs (10.47) and (10.48).

$$G_{cc}^{PID} = \frac{K_{cc}(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s(1 + s/\omega_{p1})(1 + s/\omega_{p2})}, \tag{10.47}$$

$$G_{cc}^I = \frac{K_{cc}}{s}. \tag{10.48}$$

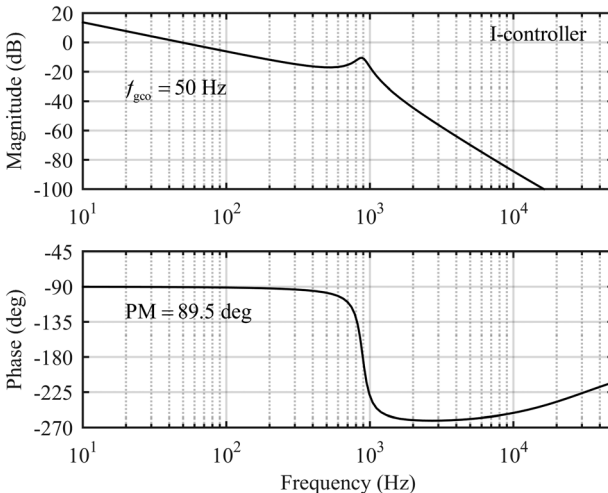


Figure 10.28 The input voltage loop gain with I controller.

The PID controller zeros and poles are placed as follows:

$$\begin{aligned} \omega_{z1} &= \omega_{z2} = 1/\sqrt{L_1 C_2}, \\ \omega_{p1} &= 1/r_{C2} C_2, \\ \omega_{p2} &= \pi f_s/3, \end{aligned} \tag{10.49}$$

and $K_{cc} = 7079$ as well as the I-controller $K_{cc} = 30$. The corresponding input voltage loop gains are given in Figures 10.27 (PID) and 10.28 (I).

In case of PV voltage feedback-controlled MPP tracking converter, the perturbed PV voltage and current in Eqs (10.13) and (10.4) will become as

$$\begin{aligned} \hat{v}_{pv} &= Z_{in-c} \hat{i}_{ph} + T_{oi-c} \hat{v}_o + G_{ci-c} \hat{v}_{pv-ref}, \\ \hat{i}_{pv} &= \hat{i}_{ph} - Y_{pv} T_{oi-c} \hat{v}_o - Y_{pv} G_{ci-c} \hat{v}_{pv-ref}, \end{aligned} \tag{10.50}$$

because $Z_{in-c} Y_{pv} \ll 1$ (cf. Figure 10.28), which means that the settling time of the PV voltage, current, and power is not anymore dependent on the properties of the PV generator and its operating point, as Figures 10.29 and 10.30 also clearly show.

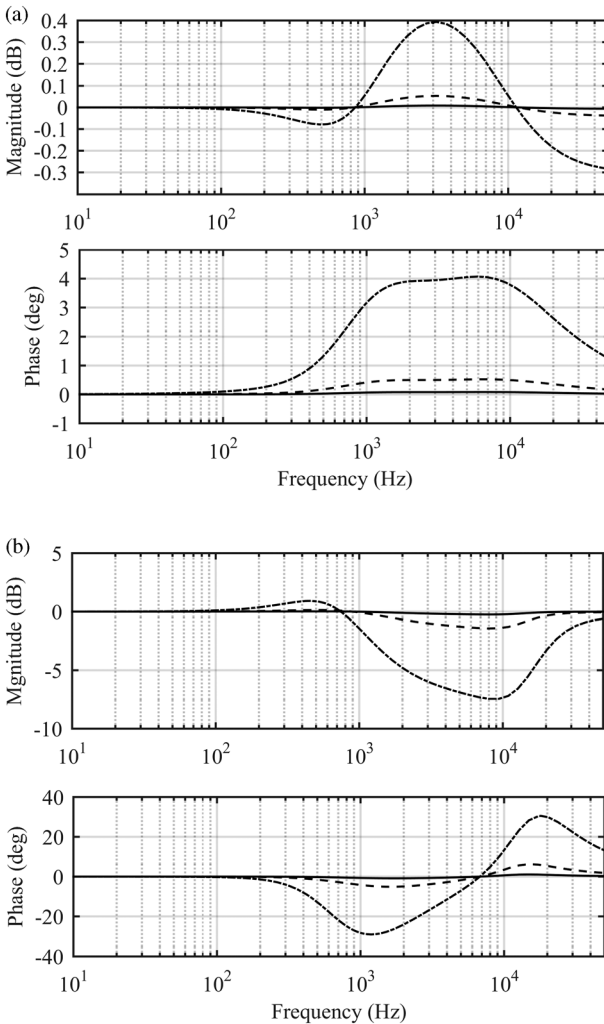


Figure 10.29 The frequency responses of the impedance-based sensitivity functions ($1/(1 + Z_{in-c} Y_{pv})$): (a) with PID control ($f_{gco} = 10$ kHz) and (b) with I control ($f_{gco} = 50$ Hz). Source: Kivimaki 1969. Reproduced with permission of IEEE.

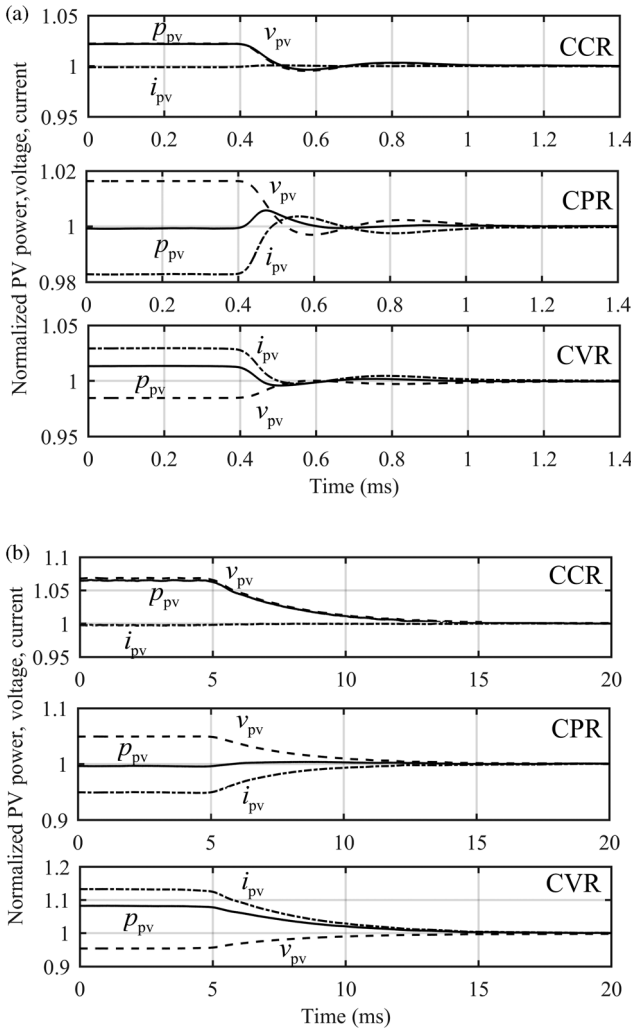


Figure 10.30 The measured PV voltage, current, and power transients (a) with PID controller and (b) I controller.

The overall transient behavior is different depending on the region, where the operating point lies according to the general PV power transient dynamics presented in Section 10.5.2 (cf. Figure 10.30).

According to Section 10.5.2, the relevant elements from the MPP tracking sampling frequency point of view are the last rightmost elements in Eq. (10.50), where G_{ci-c} stands for

$$G_{ci-c} = \frac{1}{G_{se-in}} \frac{L_{in}}{1 + L_{in}} \tag{10.51}$$

Figure 10.31 shows the frequency responses of the closed-loop control-to-input voltage transfer functions (G_{ci-c}) of PID-controlled (Figure 10.31a) and I-controlled (Figure 10.31b) boost power-stage converter, including the effect of PV generator. The input voltage scaling factor (G_{se-in}) in Eq. (10.51) equals unity in Figure 10.31. Figure 10.31a indicates that G_{ci-c} reassembles a second-order

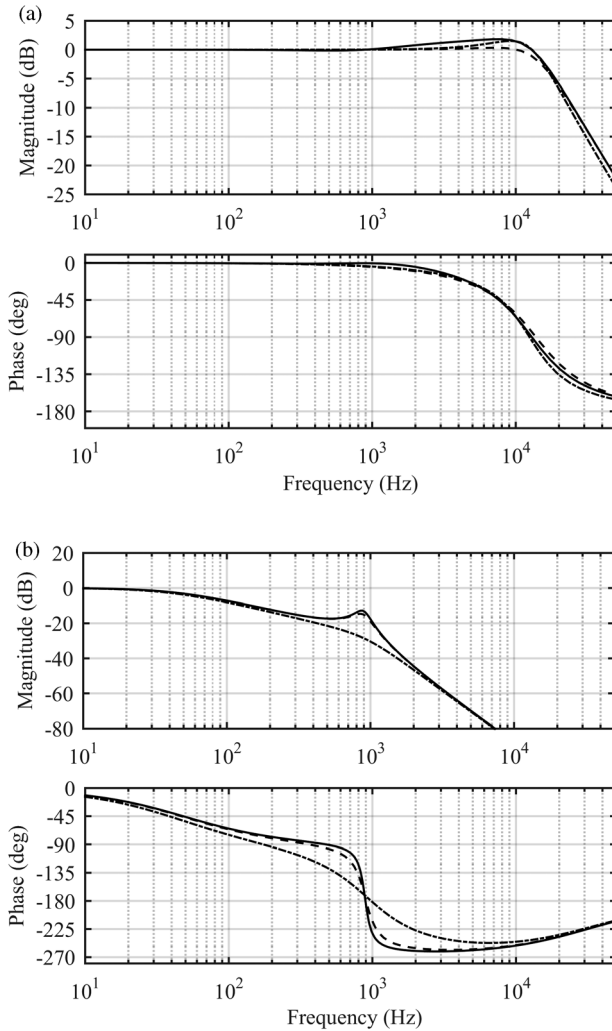


Figure 10.31 Frequency responses of control-to-input-voltage transfer functions. (a) PID control. (b) I control.

resonant system when the phase margin is on the order of 50°. Figure 10.31b indicates that G_{ci-c} resembles a first-order system when the phase margin is rather high. The next subsection will introduce methods to find a reduced-order model for the closed-loop converter, which can be utilized in the designing of the sampling frequency in case of closed-loop MPP tracking converters.

10.5.4.1 Reduced-Order Models: Intuitive Model Reduction

The full-order input voltage loop gains are presented in Eqs (10.46)–(10.48). According to Figure 10.31, the corresponding closed-loop transfer functions in Eq. (10.51) are clearly of second order. Therefore, the input voltage loop gains have to be basically of second-order transfer functions, where the behavior of the transfer functions in vicinity of the loop crossover frequency will determine the dynamic behavior of the closed-loop system. The input voltage loop gains

determining the high-frequency behavior can be approximated in case of PID control by

$$L_{\text{in-RO}}^{\text{PID}} \approx \frac{G_{\text{se}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}{\omega_{z1} \omega_{z2}} \frac{\omega_{\text{n}}^2}{s(1 + s/\omega_{\text{p2}})}, \quad (10.52)$$

and in case of I control by

$$L_{\text{in-RO}}^{\text{I}} \approx \frac{G_{\text{se}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}{s}. \quad (10.53)$$

As a consequence, the closed-loop gains can be given by

$$\begin{aligned} G_{\text{ci-c}}^{\text{RO-PID}} &= \frac{1}{G_{\text{se-in}}} \left\{ \left[\frac{G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}{\omega_{z1} \omega_{z2}} \frac{\omega_{\text{n}}^2}{s(1 + s/\omega_{\text{p2}})} \right] / \left[1 + \frac{G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}{\omega_{z1} \omega_{z2}} \frac{\omega_{\text{n}}^2}{s(1 + s/\omega_{\text{p2}})} \right] \right\} \\ &= \left[\frac{G_{\text{a}} K_{\text{cc}} V_{\text{e}} \omega_{\text{n}}^2}{\omega_{z1} \omega_{z2}} \right] / \left[s^2 + s\omega_{\text{p2}} + \frac{G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}} \omega_{\text{n}}^2}{\omega_{z1} \omega_{z2}} \right], \\ G_{\text{ci-c}}^{\text{RO-I}} &= \frac{1}{G_{\text{se-in}}} \left\{ \left[\frac{G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}{s} \right] / \left[1 + \frac{G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}{s} \right] \right\} = \frac{G_{\text{a}} K_{\text{cc}} V_{\text{e}}}{s + G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}, \end{aligned} \quad (10.54)$$

where $G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}$ equals the feedback loop crossover frequency under I control (cf. Eq. (10.53)).

In general, the second-order transfer function can be given by

$$\frac{\omega_{\text{n}}^2}{s^2 + s2\zeta\omega_{\text{n}} + \omega_{\text{n}}^2}, \quad (10.55)$$

and if the roots of the denominator polynomial are well separated, then Eq. (10.55) can be approximated at low frequencies by

$$\frac{(\omega_{\text{n}}/2\zeta)}{s + (\omega_{\text{n}}/2\zeta)}, \quad (10.56)$$

where ω_{n} denotes the undamped natural frequency and ζ the damping factor. In case of the resonant type system (i.e., Eq. (10.55)), the system time constant $\tau = 1/\zeta\omega_{\text{n}}$, and in case of first-order system (i.e., Eq. (10.56)), the system time constant $\tau = 2\zeta/\omega_{\text{n}}$. As discussed in case of the open-loop operated MPP tracking converter, the system time constant will determine the settling time of the power transient as well. According to Eqs (10.54)–(10.56), the time constants can be given by

$$\begin{aligned} \tau^{\text{PID}} &\approx \frac{2}{\omega_{\text{p2}}}, \\ \tau^{\text{I}} &\approx \frac{1}{G_{\text{se-in}} G_{\text{a}} K_{\text{cc}} V_{\text{e}}}. \end{aligned} \quad (10.57)$$

In case of resonant system, ω_n and ζ can be given based on Eq. (10.54) by

$$\omega_{n-RO}^{PID} = \sqrt{\frac{G_{se}G_aK_{cc}V_e\omega_n^2}{\omega_{z1}\omega_{z2}}}\omega_{p2}, \quad (10.58)$$

$$\zeta_{RO}^{PID} = \frac{1}{2}\sqrt{\frac{\omega_{z1}\omega_{z2}\omega_{p2}}{G_{se}G_aK_{cc}V_e\omega_n^2}}.$$

According to Eq. (10.41), the power transient settling time in CCR and CVR can be given in case of resonant system (i.e., Eq. (10.55)) by

$$T_s^{PID} \approx \frac{2}{\omega_{p2}} \ln \left(1 / \left[\Delta \sqrt{1 - \frac{\omega_{z1}\omega_{z2}\omega_{p2}}{4G_{se}G_aK_{cc}V_e\omega_n^2}} \right] \right), \quad (10.59)$$

and in case of first-order system (i.e., Eq. (10.56)) by

$$T_s^I \approx \frac{1}{G_{se-in}G_aK_{cc}V_e} \ln \left(\frac{1}{\Delta} \right). \quad (10.60)$$

According to Eq. (10.42), the power transient settling time in CPR can be given in case of resonant system (i.e., Eq. (10.55)) by

$$T_s^{PID-CPR} \approx \frac{2}{\omega_{p2}} \ln \left(2 / \left[\Delta \sqrt{1 - \frac{\omega_{z1}\omega_{z2}\omega_{p2}}{4G_{se}G_aK_{cc}V_e\omega_n^2}} \right] \right), \quad (10.61)$$

and in case of first-order system (i.e., Eq. (10.56)) by

$$T_s^{I-CPR} \approx \frac{1}{G_{se-in}G_aK_{cc}V_e} \ln \left(\frac{2}{\Delta} \right). \quad (10.62)$$

It may be obvious that the settling time in CPR is highest and, therefore, the corresponding sampling interval T_{si} shall naturally be higher than the computed settling times (T_s^{x-CPR}) in Eqs (10.61) and (10.62).

10.5.4.2 Reduced-Order Models: Control-Engineering-Based Method

The information, which is clearly visible (i.e., the second-order nature) in Figure 10.31a, is a well-known fact in control engineering [29]. Therefore, the open-loop system gain can be given based on the closed-loop system gain in Eq. (10.55) by

$$L = \frac{\omega_n^2}{s(s + 2\zeta\omega_n)}. \quad (10.63)$$

According to Eq. (10.63), we can compute the loop crossover frequency (ω_{gco}) by setting the magnitude $|L|_{\omega=\omega_{gco}} = 1$ and solving ω_{gco} and the loop phase at ω_{gco}

yielding the phase margin as $PM = L\angle\omega_{gco} + 180^\circ$. According to these procedures, we can obtain

$$\begin{aligned}\omega_{gco} &= \omega_n \sqrt{\sqrt{1 + 4\zeta^4} - 2\zeta^2}, \\ PM &= \tan^{-1} \left(\frac{2\zeta}{\sqrt{\sqrt{1 + 4\zeta^4} - 2\zeta^2}} \right).\end{aligned}\quad (10.64)$$

Based on Eq. (10.64), the closed-loop system in Eq. (10.55) can be characterized by

$$\begin{aligned}\omega_n &= \frac{\omega_{gco}}{\sqrt{\sqrt{1 + 4\zeta^4} - 2\zeta^2}}, \\ \zeta &= \frac{\tan(PM)}{2(1 + \tan^2(PM))^{\frac{1}{4}}},\end{aligned}\quad (10.65)$$

that is, the closed-loop system dynamics will be characterized by designing the loop crossover frequency and PM to be as desired.

According to Eq. (10.55), we can also compute the frequency (i.e., the resonant frequency (ω_{res})), at which the peak magnitude (M_p) will take place as follows:

$$\begin{aligned}\omega_{res} &= \omega_n \sqrt{1 - 2\zeta^2}, \\ M_p &= \frac{1}{2\zeta \sqrt{1 - 2\zeta^2}}.\end{aligned}\quad (10.66)$$

Equation (10.66) shows that the peaking will take place only when $\zeta \leq 1/\sqrt{2}$, which is known in control engineering [29] as the optimal damping. According to Eq. (10.64), we can compute that the optimal damping corresponds to PM of 65.5° .

10.5.4.3 Reduced-Order Model Verification

Figure 10.32 shows the estimated frequency responses of sensitivity (Figure 10.32a) and input-voltage loop gain (Figure 10.32b) versus the corresponding full-scale frequency responses (solid line) under the PID control. The frequency responses originating from the application of the intuitive and control engineering methods are denoted by dashed and dash-dotted lines, respectively. Figure 10.32b indicates that the intuitive method produces a phase response, where the phase margin equals 60° when the original phase margin is 50° . The control engineering method produces naturally correct phase margin. The crossover frequency is the same in all the cases. According to Eq. (10.65), the corresponding undamped natural frequency (ω_n) and the damping factor (ζ) of the full-order system will be 78.4 krad/s and 0.478, respectively. The intuitive method yields 86.7 krad/s and 0.6. Therefore, the corresponding time constants are $26.7 \mu\text{s}$ and $19.2 \mu\text{s}$ as well as the predicted settling times in respect to 5% settling band are $83.4 \mu\text{s}$ and $61.8 \mu\text{s}$, respectively. Figure 10.34a shows the

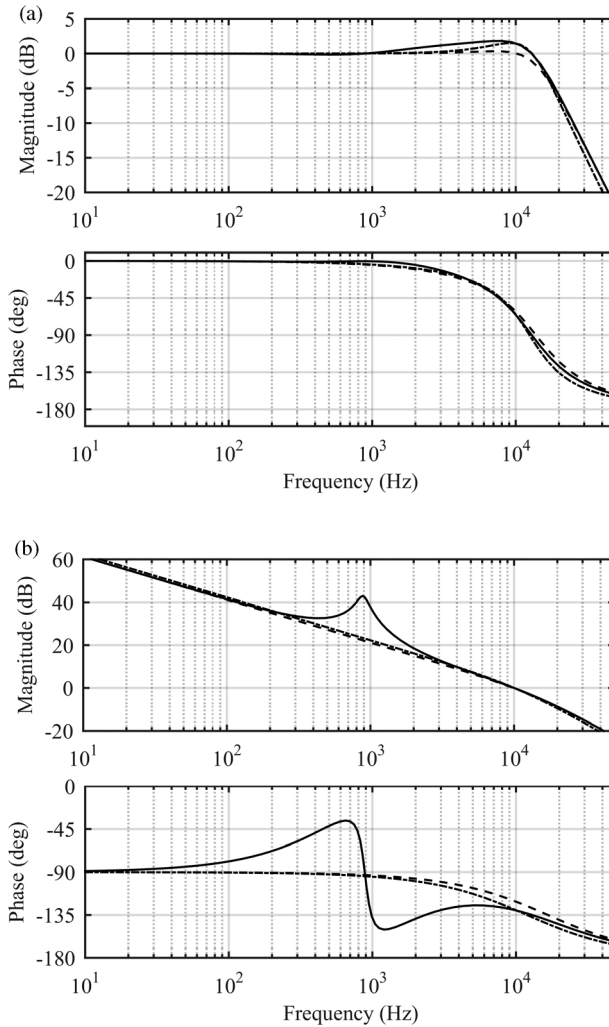


Figure 10.32 The estimated frequency responses (intuitive method: dashed line and control engineering method: dash-dotted line) versus the full-order frequency response (solid line) under PID control. (a) Sensitivity functions. (b) Input voltage loop gains.

corresponding simulated PV power transient from which the settling time can be found to be approximately $80 \mu\text{s}$. This shows that the control engineering method will give very good approximation of the settling time. As the PM of 60° implies, the intuitive method gives too short approximation for the settling time.

Figure 10.33 shows the estimated frequency responses of sensitivity function (Figure 10.33a) and input voltage loop gain (Figure 10.33b) versus the corresponding full-scale frequency responses (solid line) under I control. The frequency responses originating from the application of the intuitive and control engineering methods are denoted by dashed and dash-dotted lines, respectively. Figure 10.33 indicates that both of the methods will yield equal reduced-order responses, which also coincide with the original full-order response in the vicinity of the input voltage loop crossover frequency (i.e., $\omega_{gco} = 2\pi \cdot 50 \text{ Hz}$ and

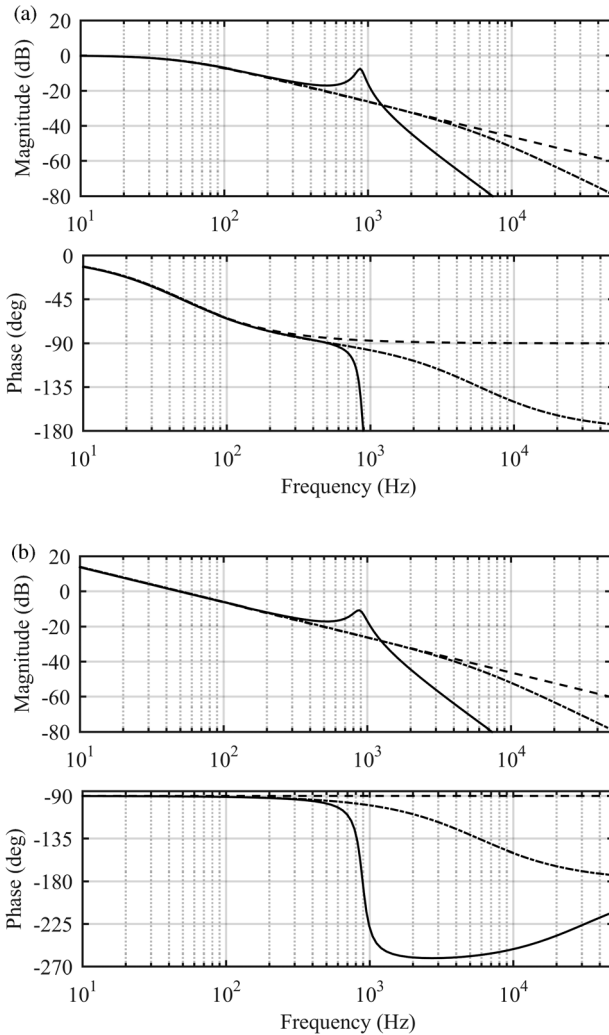


Figure 10.33 The estimated frequency responses (intuitive method: dashed line and control engineering method: dash-dotted line) versus the full-order frequency response (solid line) under I control. (a) Sensitivity functions. (b) Input voltage loop gains.

$PM = 89.5^\circ$). Based on the crossover frequency and the phase margin as well as applying Eq. (10.65), the undamped natural frequency and damping factor can be computed to be 3.36 krad/s and 5.35, respectively. The corresponding time constant (cf. Eq. 10.56) and settling time (cf. Eq. (10.60)) to the 5% settling band can be computed to be 3.18 ms and 9.5 ms, respectively. Figure 10.34b shows the corresponding simulated PV power transient from which the settling time can be found to be approximately 10 ms. This shows that both of the methods will give quite an accurate estimate on the settling time.

Figures 10.35 and 10.36 show the measured frequency responses of input voltage feedback loops of a boost power-stage converter, where the feedback-loop designs have been performed slightly differently from what is shown in the previous subsections. The crossover frequency of the feedback loop in

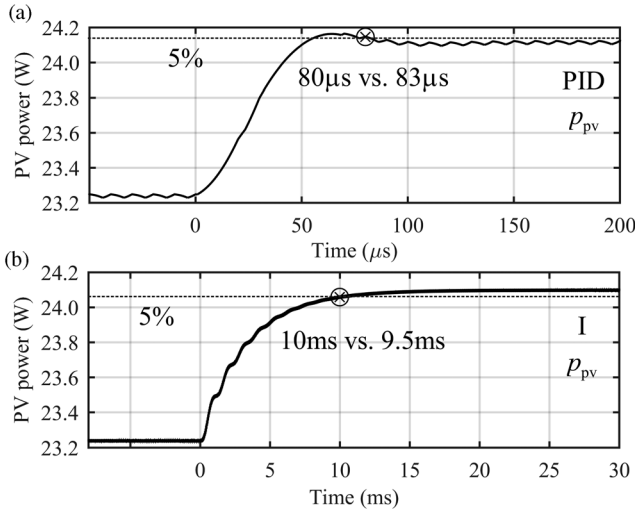


Figure 10.34 The simulated power transients in CCR induced by a step change of 0.5 V in PV voltage in CCR: (a) under PID control and (b) under I control.

Figure 10.35 is approximately 3 kHz. The corresponding phase behaviors indicate that the phase margin will vary slightly along the changes in the PV generator operating point (i.e., CCR: 37°, CPR: 41°, and CVR: 45°), which means that the system time constant will also vary accordingly. The variation does not actually pose problems when selecting the PM corresponding to the CCR operation that will give the longest settling time anyway. The practical evaluation of the converter will also be performed by using a constant current source as an input source, which corresponds to the operation in CCR. When the measured

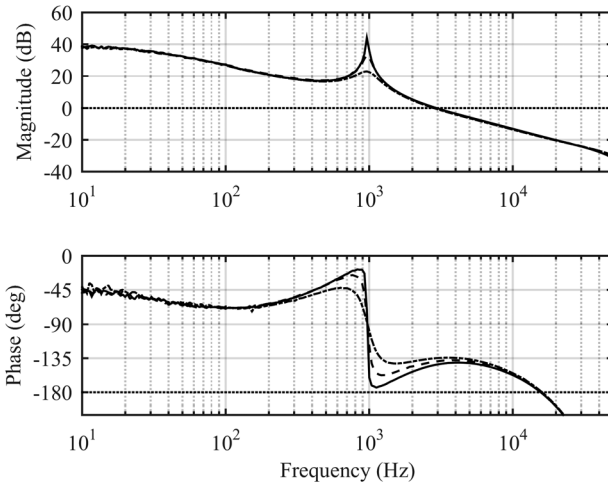


Figure 10.35 The measured PV generator-affected frequency responses of the input voltage feedback loops under PID control (CCR: solid line, CPR: dashed line, and CVR: dash-dotted line). Source: Kivimaki 1969. Reproduced with permission of IEEE.

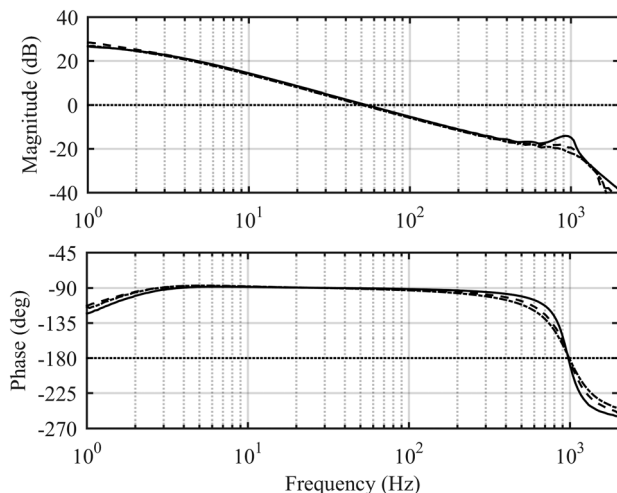


Figure 10.36 The measured PV generator-affected frequency responses of the input voltage feedback loops under I control (CCR: solid line, CPR: dashed line, and CVR: dash-dotted line). *Source:* Kivimaki 1969. Reproduced with permission of IEEE.

feedback-loop crossover and PM are used to estimate the settling time, it will give the worst case settling time as well.

Figure 10.36 shows that the PV generator effect on the low-crossover feedback-loop gain is insignificant and, therefore, the crossover frequencies and PMs will stay practically constant as 50 Hz and 89° , respectively.

Figure 10.37 shows the measured PV power transients for the PID-controlled (Figure 10.37a) and I-controlled (Figure 10.37b), where the first settling time corresponds to the measured value and the last one to the predicted value. The

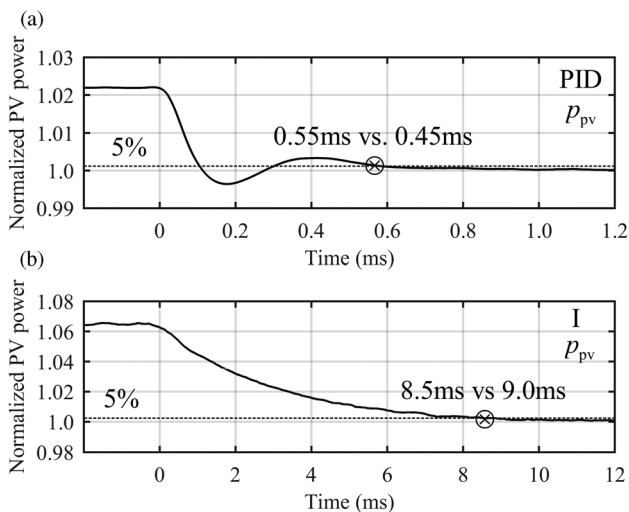


Figure 10.37 The measured power transients in CCR induced by a step change of 0.7 V in PV voltage in CCR: (a) under PID control and (b) under I control. *Source:* Kivimaki 1969. Reproduced with permission of IEEE.

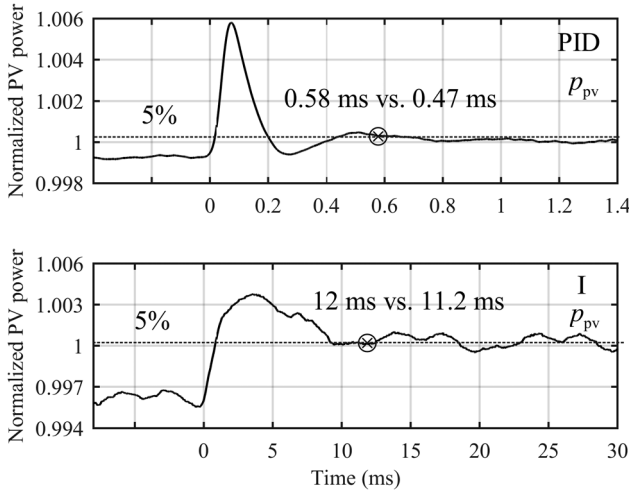


Figure 10.38 The measured power transients in CPR induced by a step change of 0.7 V in PV voltage in CCR: (a) under PID control and (b) under I control. *Source:* Kivimaki 1969. Reproduced with permission of IEEE.

accuracy between the predictions and measured values is quite good. (Note: The normalization in Figure 10.37 is performed by dividing the waveforms by their final values.)

Figures 10.38 and 10.39 show the similar PV power transients as in Figure 10.37, which are measured in CPR and CVR. Figure 10.38 confirms that the longest settling time will take place in CPR as discussed earlier. Therefore, the sampling frequency design shall be performed by using the settling times defined in Eqs (10.61) and (10.62).

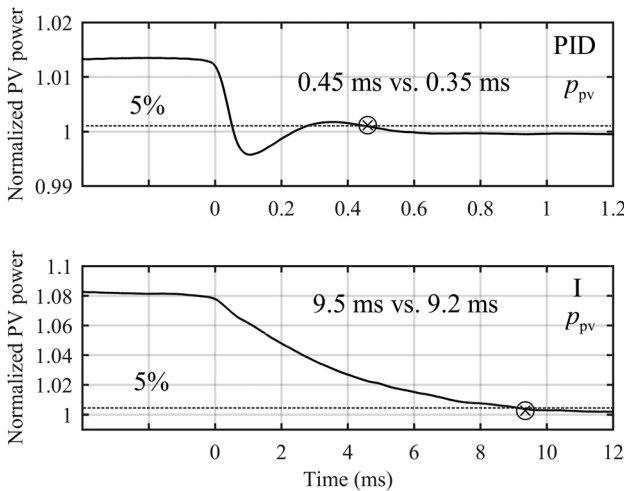


Figure 10.39 The measured power transients in CVR induced by a step change of 0.7 V in PV voltage in CCR: (a) under PID control and (b) under I control. *Source:* Kivimaki 1969. Reproduced with permission of IEEE.

10.6 Concluding Remarks

The material presented in Section 10.5 shows that the design of the sampling frequency can be solely based on the dynamic elements of the interfacing converter, both at open and closed loop. During the MPP tracking process, the operating point of the PV generator lies usually in all of the operating regions. As it was shown explicitly, the PV power transient settling time is longest in CCR region under duty ratio-operated (i.e., open loop) MPP tracking process, which actually determines the design of the sampling frequency. In CCR, the internal resistance is very high, and therefore, the transient behavior of the PV power will be dependent only on the internal dynamics of the PV interfacing converter. In addition, the PV power transient at MPP or in CPR is very small, which further emphasizes that the MPP tracking design should not be based on the characteristics of the PV generator at MPP. When the interfacing converter operates at closed loop, the PV power transient behavior is determined solely by the control design (i.e., the feedback-loop crossover frequency and the feedback-loop phase margin), but the PV power dynamics will determine that the settling time will be longest in CPR although the system time constant stays constant in all the regions. Under open-loop MPP tracking, the system time constant varies significantly, and therefore, the PV power transient settling time will be longest in CCR.

References

- 1 Luque, A. and Hegedus, S. (2003) *Handbook of Photovoltaic Science and Engineering*, John Wiley & Sons, Ltd., Chichester, UK.
- 2 Femia, N., Petrone, G., Spagnuolo, G., and Vitelli, M. (2013) *Power Electronics and Control Techniques for Maximum Energy Harvesting in Photovoltaic Systems*, CRC Press, Boca Raton, FL.
- 3 Jain, S. and Agarwal, V. (2007) Comparison of the performance of maximum power point tracking schemes applied to single-stage grid-connected photovoltaic systems. *IET Electr. Power Appl.*, **1** (5), 753–762.
- 4 Subudhi, B. and Pradhan, R. (2013) A comparative study on maximum power point tracking techniques for photovoltaic power systems. *IEEE Trans. Sustain. Energy*, **4** (1), 89–98.
- 5 Hohm, D.P. and Ropp, M.E. (2003) Comparative study of maximum power point tracking algorithms. *Prog. Photovolt Res. Appl.*, **11** (1), 47–62.
- 6 Esaram, T. and Chapman, P.L. (2007) Comparison of photovoltaic array maximum power point tracking techniques. *IEEE Trans. Energy Convers.*, **22** (2), 439–449.
- 7 Lyi, S. and Dougal, R.A. (2002) Dynamic multiphysics model for solar array. *IEEE Trans. Energy Convers.*, **17** (2), 285–294.
- 8 Nousiainen, L., Puuko, J., Mäki, A., Messo, T., Huusari, J., Jokipii, J., Viinamäki, J., Torres Lobera, D., Valkealahti, S., and Suntio, T. (2013) Photovoltaic generator as an input source for power electronic converters. *IEEE Trans. Power Electron.*, **28** (6), 3028–3038.

- 9 Ziao, W., Dunford, W.G., Palmer, P.R., and Capel, A. (2007) Regulation of photovoltaic voltage. *IEEE Trans. Ind. Electron.*, **54** (3), 1365–1374.
- 10 Xiao, W., Ozog, N., and Dunford, W.G. (2007) Toplogy study of photovoltaic interface for maximum power point tracking. *IEEE Trans. Ind. Electron.*, **54** (3), 1696–1704.
- 11 Romero-Cadaval, E., Spagnuolo, G., Franquelo, L.G., Ramos-Paja, C.A., Suntio, T., and Xiao, W. (2013) Grid-connected photovoltaic generation plants – components and operation. *IEEE Ind. Electron. Mag.*, **7** (3), 6–20.
- 12 Mäki, A., Valkealahti, S., and Leppäaho, J. (2012) Operation of silicon-based photovoltaic modules under partial shading conditions. *Prog. Photovolt. Res. Appl.*, **20** (3), 298–309.
- 13 Mäki, A. and Valkealahti, S. (2012) Power losses in long string and parallel connected short strings of series connected silicon-based photovoltaic modules under partial shading conditions. *IEEE Trans. Energy Convers.*, **27** (1), 173–183.
- 14 Torres-Lobera, D., Mäki, A., Huusari, J., Lappalainen, K., Suntio, T., and Valkealahti, S. (2013) Operation of TUT solar PV station research plant under partial shading caused by snow and buildings. *Int. J. Photoenergy*, **2013**, 1–13.
- 15 Luoma, J., Kleissl, J., and Murray, K. (2012) Optimal inverter sizing considering cloud enhancement. *Solar Energy*, **86** (1), 421–429.
- 16 Chen, S., Li, P., Brady, D., and Lehman, B. (2010) The impact of irradiance time behaviors on inverter sizing and design. Proceedings of the IEEE COMPEL, pp. 1–5.
- 17 Balafas, C.A., Athanassopoulou, M.D., Argyropoulos, Th., Skafidas, P., and Dervos, C.T. (2010) Effect of the diffuse solar radiation on photovoltaic inverter output. Proceedings of the IEEE MELECON, pp. 58–63.
- 18 Hussein, K.H., Muta, I., Hoshino, T., and Osakada, M. (1995) Maximum photovoltaic power tracking: an algorithm for rapidly changing atmospheric conditions. *IEE Proc. Gener. Transm. Distrib.*, **142** (1), 59–64.
- 19 Kjær, S.B. (2012) Evaluation of the ‘hill climbing’ and the ‘incremental conductance’ maximum power point trackers for photovoltaic power systems. *IEEE Trans. Energy Convers.*, **27** (4), 922–929.
- 20 ESRAM, T., Kimball, J.W., Krein, P.T., Chapman, P.L., and Midya, P. (2006) Dynamic maximum power point tracking of photovoltaic arrays using ripple correlation control. *IEEE Trans. Power Electron.*, **21** (5), 1282–1291.
- 21 Brunton, S.L., Rowley, C.W., Kulkarni, S.R., and Clarkson, C. (2010) Maximum power point tracking for photovoltaic optimization using ripple-based extremum seeking control. *IEEE Trans. Power Electron.*, **25** (10), 2531–2540.
- 22 Suntio, T., Leppäaho, J., Huusari, J., and Nousiainen, L. (2010) Issues on solar-generator interfacing with current-fed MPP-tracking converters. *IEEE Trans. Power Electron.*, **25** (9), 2409–2419.
- 23 Suntio, T., Huusari, J., and Leppäaho, J. (2010) Issues on solar-generator interfacing with voltage-fed MPP-tracking converters. *Eur. Power Electron. Drives J.*, **20** (3), 40–47.
- 24 Femia, N., Petrone, G., Spagnuolo, G., and Vitelli, M. (2005) Optimization of perturb and observe maximum power point tracking method. *IEEE Trans. Power Electron.*, **20** (4), 963–973.

- 25 Femia, N., Petrone, G., Spagnuolo, G., and Vitelli, M. (2009) A technique for improving P&O MPPT performance of double-stage grid-connected photovoltaic systems. *IEEE Trans. Ind. Electron.*, **56** (11), 4473–4482.
- 26 Viinamäki, J., Jokipii, J., Messo, T., Suntio, T., Sitbon, M., and Kuperman, A. (2015) Comprehensive dynamic analysis of PV-generator-interfacing DC–DC boost-power-stage converter. *IET Renew. Power Gener.*, **9** (4), 306–314.
- 27 Leppäaho, J., Nousiainen, L., Puukko, J., Huusari, J., and Suntio, T. (2010) Implementing current-fed converters by adding an input capacitor at the input of voltage-fed converter for interfacing solar generator. Proceedings of the EPE-PEMC, pp. 76–80.
- 28 Huusari, J. and Suntio, T. (2012) Interfacing constraints of distributed maximum power point tracking converters in photovoltaic applications. Proceedings of the EPE-PEMC, pp. DS3d.1-1–DS3d1-7.
- 29 Ogata, K. (1997) *Modern Control Engineering*, Prentice Hall, Upper Saddle River, NJ.
- 30 Viinamäki, J., Jokipii, J., and Suntio, T. (2016) Improving double-line-frequency voltage ripple rejection capability of DC/DC converter in grid-connected two-stage PV inverter using DC-link voltage feedforward. Proceedings of the EPE-ECCE Europe, pp. 1–10.
- 31 Wyatt, J.L. and Chua, L.O. (1983) Nonlinear resistive maximum power theorem with solar cell application. *IEEE Trans. Circuits Syst.*, **CAS.30** (11), 824–828.

11

Photovoltaic Generator Interfacing Issues

11.1 Introduction

In this chapter, we will classify the PV systems based on the architecture of the systems, that is, centralized versus distributed architectures. The distributed architectures are later classified based on the level of MPP tracking distribution within the PV generator. The implementation can also be classified according to the way the power is processed in the architecture, that is, full or partial power processing. The rest of the chapter will then concentrate on the dynamics of the PV generator interfacing converters and the stability issues within this constellation.

11.2 Centralized PV System Architecture

Most of the PV systems are grid-connected systems as depicted in Figure 11.1. The centralized system is such that there is only one common MPP tracking device, which forces the system to operate at the MPP of the PV array [1]. This kind of system is also known as grid-parallel system (cf. Figure 11.1a and b), because the grid would determine the AC voltage level as well as the frequency. The main goal of the system would be to transfer maximum available power into the grid. Sometimes the PV system can be commanded to transfer only a certain amount of power into the grid to prevent overvoltage in the grid [2]. This kind of operation is known as power curtailment. This also means that the MPP tracking has to be changed to maximum power (MP) tracking.

The PV system can also be operated as grid-forming system (cf. Figure 11.1c), where the system inverter will determine the ac-voltage level as well as the grid frequency. This kind of operation mode can be induced by a fault in the distribution system, which isolates a part of the grid from the rest of the grid [3] or the grid power supplying is based solely on renewable energy sources [4].

11.3 Distributed PV System Architectures

The distributed PV systems are usually applied to improve the energy yield of PV generator, which would be reduced due to the shading effects of building

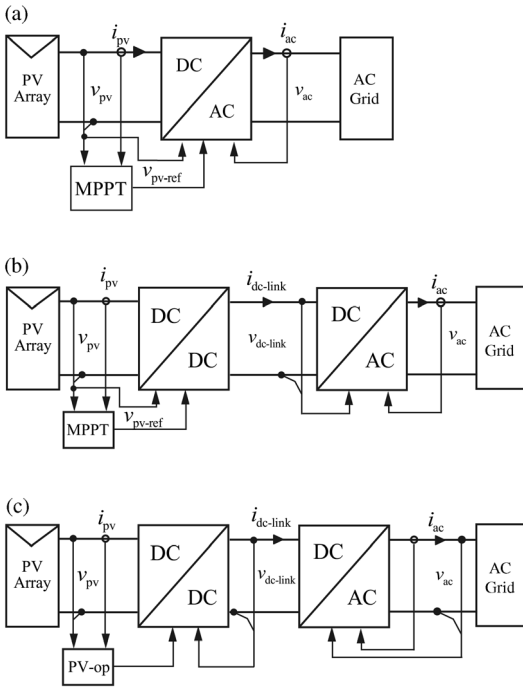


Figure 11.1 Centralized PV system architectures. (a) Single-stage grid-parallel architecture. (b) Two-stage grid-parallel architecture. (c) Two-stage grid-forming architecture.

structure, trees, flag poles, or passing-by clouds, as discussed in Chapter 10 [5,6]. The PV array is usually composed of PV strings connected in parallel. Thus, the first step in increasing the energy output is to provide each parallel string with an individual MPP tracking converter, as illustrated in Figure 11.2. Thus, all the strings will be operated at their respective MPPs, and the total power transferred into the grid is naturally the sum of the PV string powers.

The further improvement of power output will require the use of panel-based MPP tracking converters, which can be connected either in series (cf. Figure 11.3a) or in parallel (cf. Figure 11.3b) [7–13]. The parallel connection

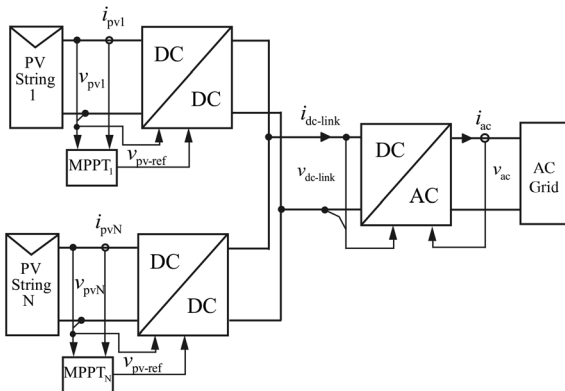


Figure 11.2 String-based PV system architecture.

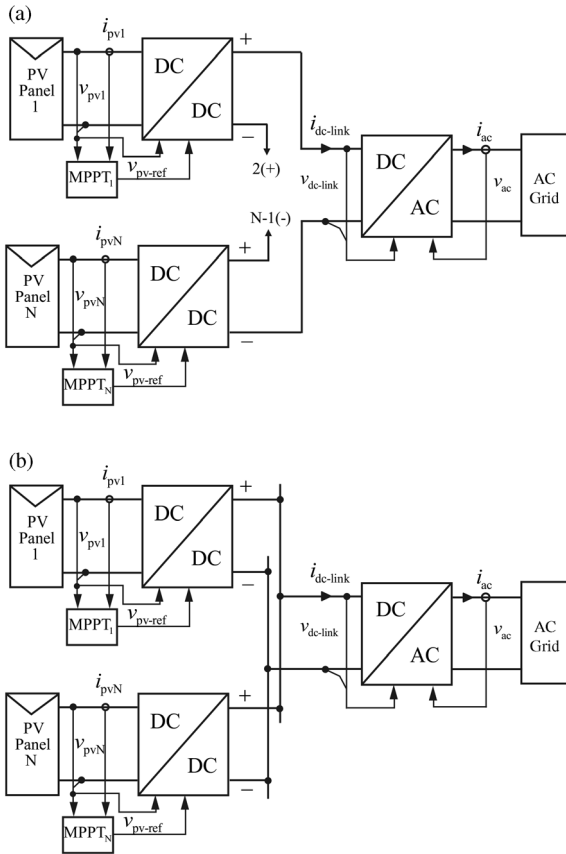


Figure 11.3 PV panel-based distributed systems. (a) Series-connected MPP tracking converters. (b) Parallel-connected MPP tracking converters.

requires using transformer-isolated converters to scale the panel voltage to the DC-link-voltage level [13]. As discussed in Chapter 10, the panel may also be called module in the literature, but in this chapter, the module is the subpart of the panel across which the bypass diode is connected. The output voltage of the series-connected converters (cf. Figure 11.3a) is directly dependent on the corresponding PV panel power and the required DC-link voltage by

$$V_{con-i} = \frac{P_{MPP-i}}{\sum_{i=1}^N P_{MPP-i}} V_{DC-link}, \quad (11.1)$$

which can be easily concluded, because the output-side current is the same for all the converters. Therefore, the rating of the converter output voltage has to be carefully considered, because the output voltage of some of the converters can be zero due to the shading of the panels. It is usually assumed that quite low-voltage output-side components can be used but that may not be true. Another issue is also that only the buck–boost-type power stage can operate satisfactorily, because the output voltage of the series-connected converter can be higher or lower than the input voltage.

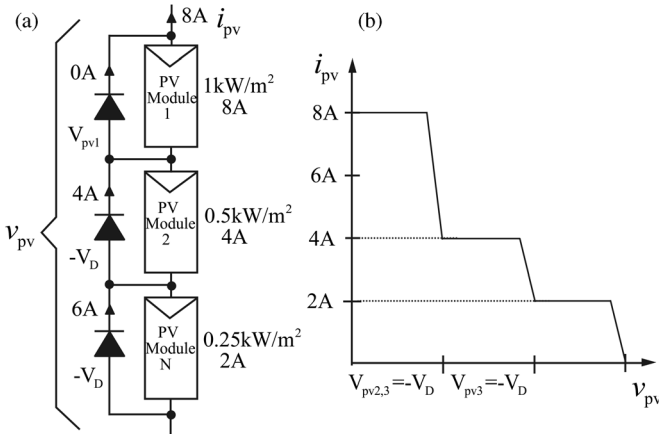


Figure 11.4 Effect of shading on the module behavior. (a) Module currents and voltages. (b) The corresponding I - V curve when the operating point is varied.

If we like to further improve the energy yield, then the actions have to be taken at the module level, as discussed in Refs [11,12,14–19]. Figure 11.4 illustrates the behavior of the modules when the incident irradiation is not unified on the surface of the panel, that is, the incident irradiation varies module by module. As discussed in Chapter 10, a PV cell and module are current sources. Therefore, the differences in the incident irradiation will cause equal differences in the module currents. The series connection of current sources requires the currents to be equal, and if the module current deviate from the maximum current of the modules then the difference current would flow through the shunt diodes dropping the voltage of the modules to the voltage drop of the shunt diode, as indicated in Figure 11.4a. The I - V curve of the panel is illustrated in Figure 11.4b by means of which the power output of the panel can be estimated. In this case, we have three different power levels of which the lowest-voltage MPP would be the global MPP.

It may be obvious that the panel power output can be increased by preventing the module voltages to drop to zero during the partial shading, that is, an additional current corresponding to the shunt-diode current must be produced by another method. The implementation method can be based on full, partial, or differential power processing principles [16–21]. Figure 11.5 illustrates the differences in the full and partial-power processing schemes, Figure 11.6 illustrates two differential power-processing schemes, and Figure 11.7 illustrates a simple differential power-processing scheme.

The partial-power processing scheme in Figure 11.5b necessitates the use of transformer-isolated converter where the output of the converter is added on the top of the input of the converter [21]. The differential power processing schemes in Figure 11.6 also necessitates using transformer-isolated converters [18,19]. The simple differential power processing scheme in Figure 11.17 works in such a manner that the PV module voltages are connected across the inductors depending on which of the switches are turned on [11,12]. Thus, the

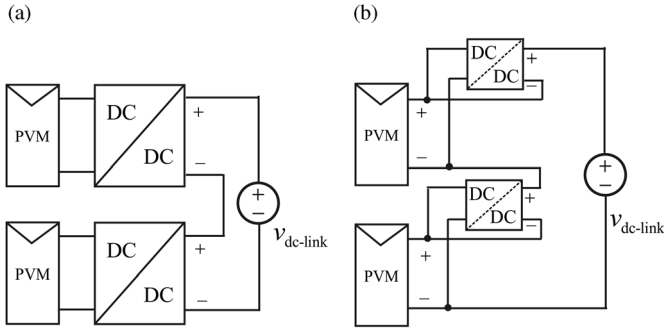


Figure 11.5 Different power processing schemes. (a) Full power processing. (b) Partial power processing.

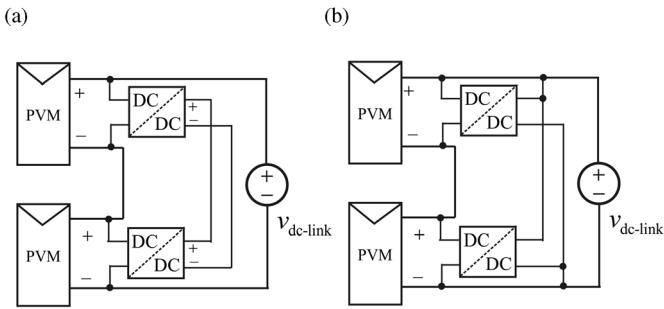


Figure 11.6 Differential power processing schemes. (a) Isolated or floating output port scheme. (b) Trail-to-trail connected output scheme.

module voltages will be equal if the conduction times of the switches are equal. The average inductor current will balance the differences in the module currents. The scheme works well within three modules, but to balance the module voltages within different panels requires connections inside the different panels, as shown in Figure 11.7.

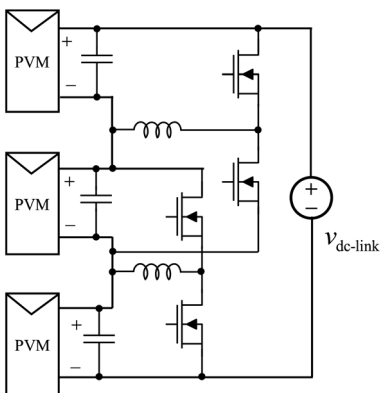


Figure 11.7 Buck-boost converter-based simple differential power processing scheme.

11.4 PV Generator-Induced Effects on Interfacing-Converter Dynamics

11.4.1 Introduction

As discussed in Chapter 10, the PV generator is a highly nonlinear input source with limited output power and operation point-dependent source behavior. Its I - V curve can be divided into three different regions, such as constant current (CCR), constant power (CPR), and constant voltage (CVR) regions as depicted in Figure 11.8, where the point (1,1) denotes the MPP: The CPR is a narrow region around the MPP, where the static (R_{pv}) and dynamic (r_{pv}) resistances are approximately equal [22–25]. The CCR is located at the voltages less than the CPR voltages and is characterized by rather high dynamic resistance (r_{pv}) and low static resistance (R_{pv}) as well as rather small output capacitance (c_{pv}). The CVR is located at the voltages higher than the CPR voltage and is characterized by rather low dynamic resistance (r_{pv}) and high static resistance (R_{pv}) as well as high dynamic capacitance (c_{pv}).

Figure 11.9 shows a simplified small-signal equivalent circuit of the PV generator and the input of the interfacing converter, which has always an input capacitor. The origin of the dynamic effects in the interfacing converter can be

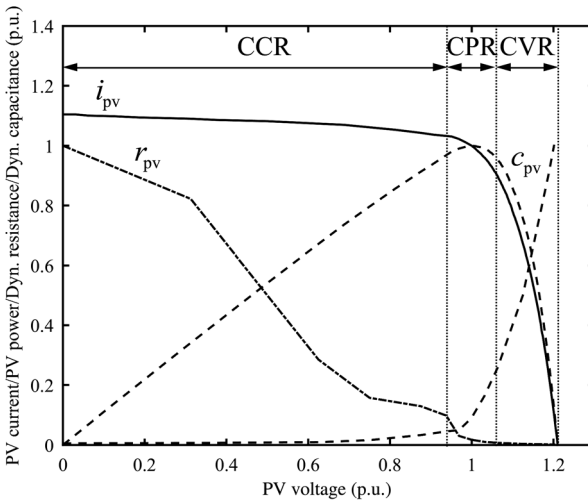


Figure 11.8 Characteristics of PV generator.

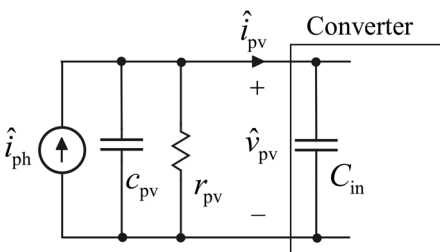


Figure 11.9 A simplified PV generator small-signal equivalent circuit and the input of the interfacing converter.

traced to the way the PV generator affects the dynamic behavior of the input capacitor [22]: In CCR, when the dynamic resistance is high, the full dynamics of the input capacitor is available. In CVR, when the dynamic resistance is low, the dynamics of the input capacitor is effectively shunted by the dynamic resistance, and the input source resembles a voltage source. In practice, the changes in the interfacing converter will take place when the operating point travels through the constant power region. In CCR, the dynamics of the interfacing converter resembles the dynamics introduced in Chapter 8, and in CVR, the dynamics introduced in Chapter 3, respectively. In practical applications, the operating point will locate in all the regions, and therefore, the converter has to be able to operate in them also. When the PV generator is basically a current source, then the current-fed dynamics will dominate in these applications.

At open loop, the dynamic changes do not affect the converter operation in such a way that special design approaches should be done. As discussed in Chapter 8, the active switch control scheme dictates which way the duty ratio has to be changed to increase or decrease the corresponding output variable. At closed loop, the high-bandwidth input voltage feedback loop will always maintain the input source as a current source even in CVR due to the size of the dynamic resistance (i.e., the input source will never be an ideal constant voltage source).

As explicitly demonstrated in Ref. [26], the terminal sources profoundly affect the dynamics of the converter even if the power stage remains the same. The buck power stage converter used in the analyses of Ref. [26] is shown in Figure 11.10 in open-terminal mode with relevant components and operating point definitions. Figures 11.11–11.14 show explicitly what kind of changes the varying terminal sources will generate in the dynamics of the converter for comparison to the PV generator-affected changes.

Figure 11.11 shows the *Bode* plots of the measured control-to-output transfer functions (G_{co-o}) of the buck power stage converter when the terminal sources are varied, where “vf” and “cf” denote voltage and current-type input terminal sources and “vo” and “co” current and voltage-type output terminal sources. Actually, “vo” means voltage output and “co” current output, but the corresponding terminal sources are the duals of them. Figure 11.11 shows explicitly that the dynamic changes are significant, and therefore, it is necessary to use the correct terminal sources when performing modeling or measuring the frequency responses. It also has to be understood that the VF/VO and CF/CO converters can be measured in

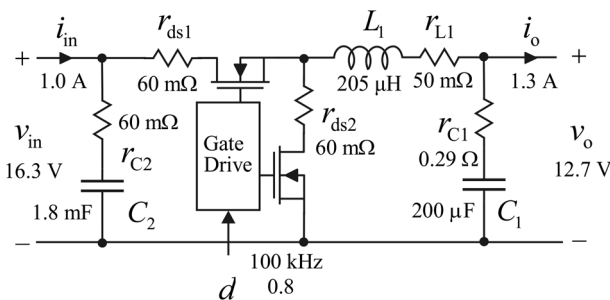


Figure 11.10 Buck power stage in open-terminal mode.

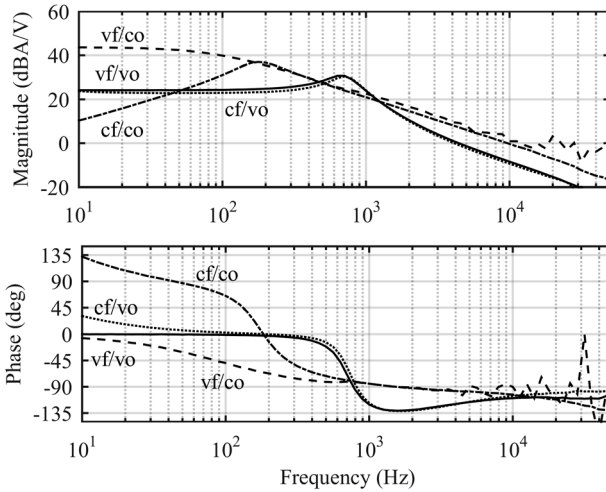


Figure 11.11 All the relevant control-to-output transfer functions (G_{co-o}).

practice by using the correct output terminal sources. The VF/CO and CF/VO converters have to be measured by using a resistor as a load, and the corresponding transfer functions have to be computationally solved from the measured transfer functions applying a proper source-affected formulation.

According to the dynamic models presented in Chapter 3 for the VF converters and in Chapter 8 for the CF converters, the dynamic changes are reality: The phase of the control-to-output converter starts at zero in the VF converter and at 180 degrees in the CF converter, there are no RHP zeros in the VF converter but one RHP zero in the CF converter, and so on.

Figure 11.12 shows the *Bode* plots of the measured control-to-input transfer functions (G_{ci-o}) when the terminal sources are varied, where the denotations are

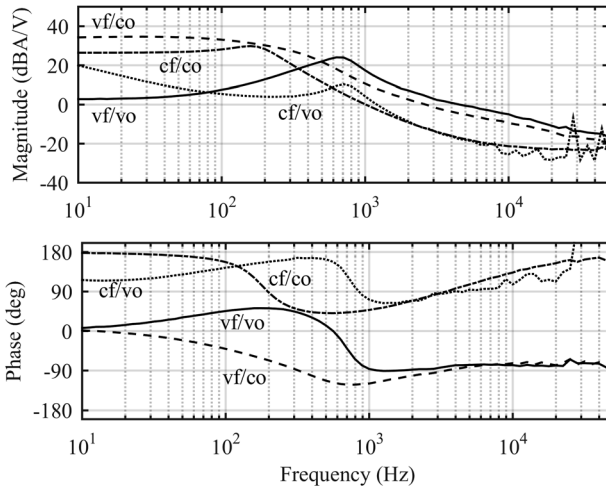


Figure 11.12 All the relevant control-to-input transfer functions (G_{ci-o}).

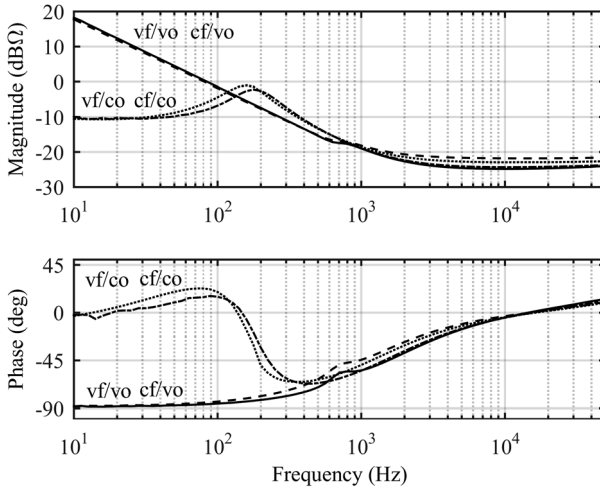


Figure 11.13 All the relevant input impedances (Z_{in-o}).

the same as in Figure 11.11. According to the figure, it is obvious that the control design has to be based on the models developed by using correct terminal sources for ensuring stable operation.

Figure 11.13 shows the *Bode* plots of the measured input impedances when the output terminal source is varied. The figure shows that the input impedances are equal when the output terminal source is the same, which complies with the common sense, because the power stage is the same. When the output terminal source is changed, the input impedance will also change significantly, especially at the low frequencies.

Figure 11.14 shows the *Bode* plots of the measured output impedances when the input terminal source is varied. The figure shows that the output impedances

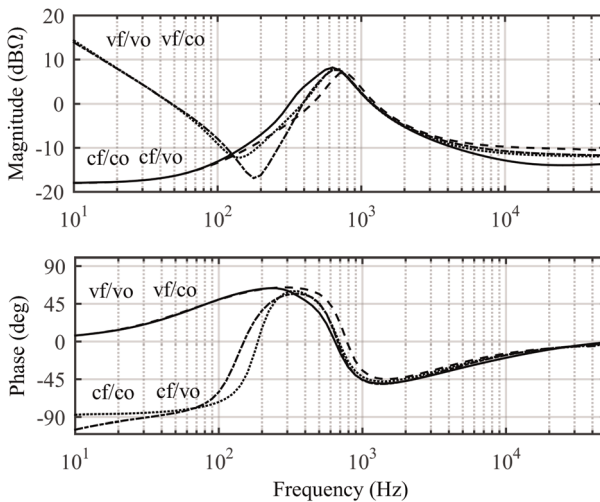


Figure 11.14 All the relevant output impedances (Z_{o-o}).

are equal when the input terminal source is the same, which is also natural when the power stage is the same. The change of the input terminal source will significantly affect the output impedance.

In case of the CF converters, the source-affected transfer functions can be computed (cf. Chapter 8) by

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \frac{Z_{in}^H}{1 + Y_S Z_{in}^H} & \frac{T_{oi}^H}{1 + Y_S Z_{in}^H} & \frac{G_{ci}^H}{1 + Y_S Z_{in}^H} \\ \frac{G_{io}^H}{1 + Y_S Z_{in}^H} & -\frac{1 + Y_S Z_{in-oco}^{H-x}}{1 + Y_S Z_{in-x}^H} Y_{o-x}^H & \frac{1 + Y_S Z_{in-\infty}^H}{1 + Y_S Z_{in}^H} G_{co}^H \end{bmatrix} \begin{bmatrix} \hat{i}_{inS} \\ \hat{v}_o \\ \hat{d} \end{bmatrix} \quad (11.2)$$

According to Chapter 10, the source admittance Y_S in case of PV generator in (11.2) can be substituted with the inverse of the dynamic resistance, that is, $Y_S \approx 1/r_{pv}$. We show some examples of the PV generator effect on the CF converters in the next section based on theory and experiments.

11.4.2 PV Generator Effects on Converter Dynamics

The PV generator is quite challenging input source for the power electronic converters, because its effect on the interfacing converter will change along the changes in the operating point [22]. The environmental and climatic conditions are also varying all the time and sometimes very quickly, as we have discussed in Chapter 10. This actually means that the operating point is varying due to the named changes and can locate in any of the three I - V regions at least temporarily.

As stated earlier, the PV generator is basically a current source, and especially in CCR quite an ideal current source. It was observed earlier that the input-current feedback control does not work as a control method in the PV generator interfacing, because the controller would saturate easily when the irradiation conditions are rapidly changing [24]. Thus, the input voltage feedback control was recommended to be used instead of input current feedback control [24]. The further studies revealed that the origin of the problem is actually the violation of Kirchhoff's current law, which makes the converter to become unstable when the operating point is moved into the CCR [27,28].

Figure 11.15 shows the power stage of an input-current-controlled coupled-inductor superbuck converter, where coupling of the inductors was carried out in such a manner that the input current of the converter is almost ripple free [28]. An additional 1 mF capacitor was connected at the output of the PV generator for satisfying the interfacing constraints of the converter. Figure 11.16 shows the behavior of the PV voltage and current as well as the output current of the converter when the operation point of PV generator is changed.

In Figure 11.16, the operating point is moved from CVR toward CPR and CCR and back. The converter is clearly stable in CVR, but after the MPP (i.e., MPP is visible in the output current) the converter enters into CCR and becomes unstable. The instability is removed when the operating point is moved back into CVR. The origin of the instability is the violation of Kirchhoff's current law, which is quite expected due to constant PV current in CCR.

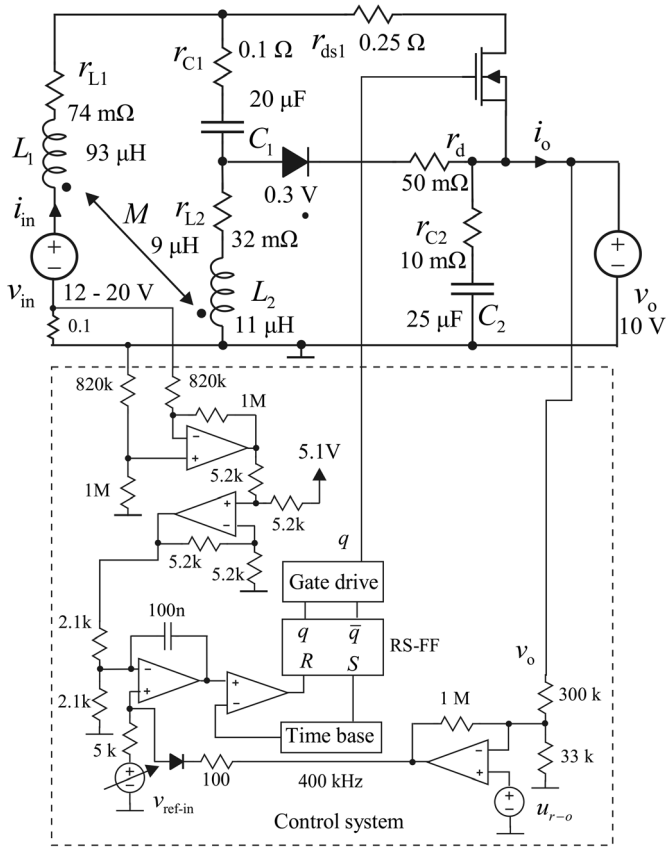


Figure 11.15 The power stage of a coupled inductor superboost converter.

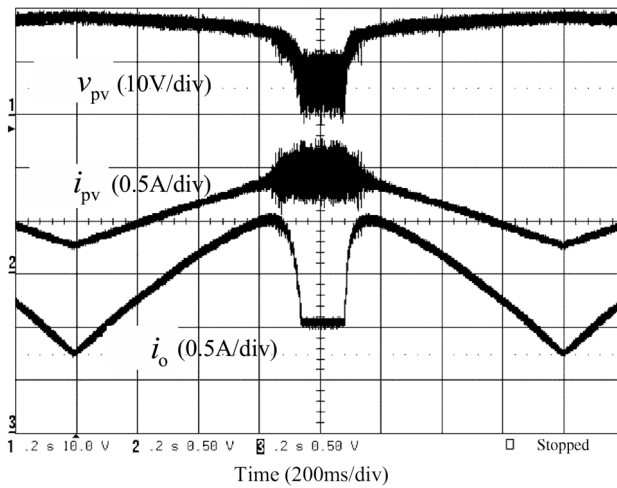


Figure 11.16 The behavior of the PV voltage and current as well as the output current of the coupled-inductor superboost converter, when the operation point is varied.

Reference [28] shows explicitly that the reason for the instability is solely the violation of Kirchhoff's current law and nothing else. We will discuss in more detail in next section the other stability related issues. Hence, it is feasible to limit the further discussions to the real CF converters. The converters that we will treat are the buck power-stage converter [29], the boost power-stage converter [30], and the superbuck converter [31].

11.4.2.1 Buck Power-Stage Converter

The buck power-stage converter used in the experimental measurements is shown in Figure 11.17. In this case, the gate signals of the MOSFETs are inverted compared with the original VF buck converter, as indicated in Figure 11.17. Thus, the relevant transfer functions representing the converter dynamics can be found from Chapter 8 in Eqs (8.75)–(8.78). The input source of the converter has been Raloss SR30-36 PV panel, which is illuminated by an artificial light source producing 500 W/m². The output-voltage feedback control is intended only for limiting the output voltage in case of excess overvoltage at the output. Figure 11.18 shows that the input voltage-controlled converter works well in all the regions of the PV generator. The MPP is clearly visible at the output current.

According to Eq. (11.2), we can compute that the PV generator-affected control-to-input transfer function would be of the form

$$G_{ci-o}^{pv} = \frac{sL_1 I_{in} + D' V_o}{L_1 C_2 (s^2 + s(1/r_{pv} C_2) + (D'^2/L_1 C_2))}, \tag{11.3}$$

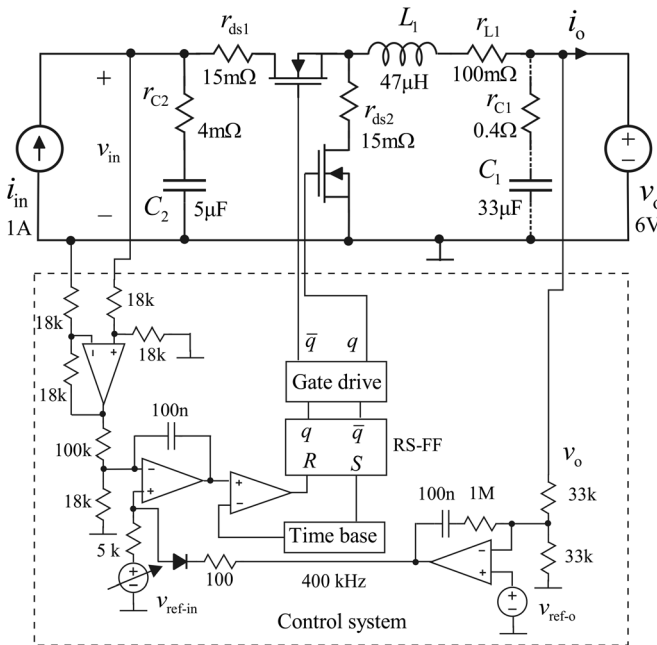


Figure 11.17 The experimental buck power-stage converter.

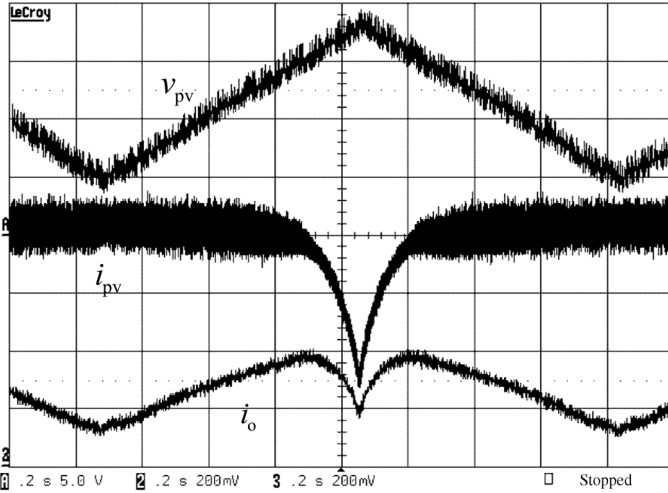


Figure 11.18 The behavior of PV voltage and current as well as converter output current, when the operation point is swept from CCR to CVR and back.

and the PV generator-affected control-to-output transfer of the form

$$G_{co-o}^{pv} = \frac{(I_{in}/V_{in}) - (1/r_{pv}) - sC_2}{L_1 C_2 (s^2 + s(1/r_{pv} C_2) + (D^2/L_1 C_2))} = \frac{(1/R_{pv}) - (1/r_{pv}) - sC_2}{L_1 C_2 (s^2 + s(1/r_{pv} C_2) + (D^2/L_1 C_2))}. \quad (11.4)$$

The parasitic elements are omitted for maximizing the information on the PV generator effect. Eq. (11.3) shows that the sign of G_{ci-o} is positive due to the inverting of the MOSFETs' gate signals. The PV generator clearly affects only the damping of the resonant circuit, that is, the damping is lowest in CCR when r_{pv} is highest. Eq. (11.4) shows that the low-frequency sign of G_{co-o} is positive in CCR, and the RHP zero exists, because $r_{pv} \gg R_{pv}$. When the operating point enters into CPR, the RHP zero moves to the origin, because $r_{pv} \approx R_{pv}$. When the operating point enters into the CVR, the RHP zero disappears but the sign of the transfer function becomes negative at the low frequencies also, because $r_{pv} \ll R_{pv}$. This means that the output-side feedback control would become unstable in CVR. Opposite will take place if the MOSFETs' gate signals are not inverted. Figure 11.19 shows the *Bode* plot of the measured control-to-output transfer functions, which also explicitly proves the mentioned analyses to be correct (i.e., RHP zero, the damping behavior and change of sign).

11.4.2.2 Boost Power-Stage Converter

The experimental boost power stage converter is shown in Figure 11.20 and the measured input voltage loop gains in Figure 11.21. The figure shows that the PV generator similarly affects the resonant damping as in the buck power-stage converter, but only insignificantly the relevant part of the loop gain. The behavior of the control-to-input and control-to-output transfer functions in CCR and CVR are shown in Figures 11.22 and 11.23, respectively.

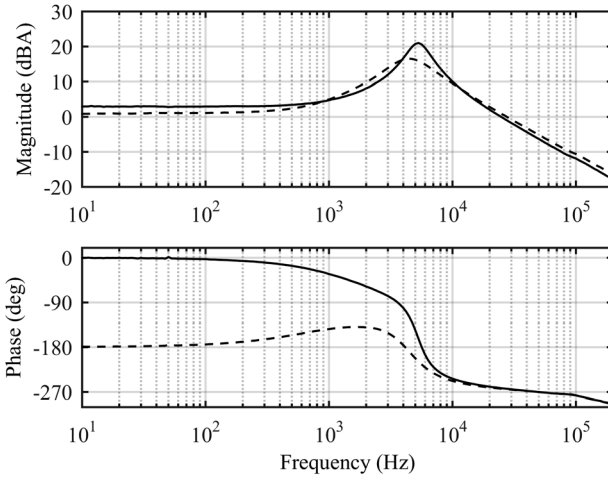


Figure 11.19 The behavior of the control-to-output transfer function (G_{co-o}), when the operating point is moved from CCR (solid line) into CVR (dashed line).

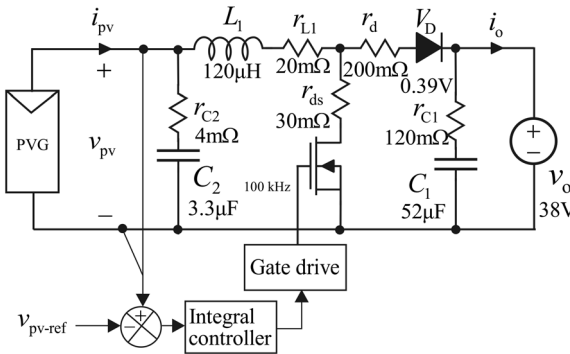


Figure 11.20 The experimental boost power-stage converter.

According to Eq. (11.2), we can compute that the PV-generator-affected control-to-input transfer function would be of the form

$$G_{ci-o}^{pv} = -\frac{V_o}{L_1 C_2 (s^2 + s(1/r_{pv} C_2) + (1/L_1 C_2))}, \tag{11.5}$$

and the PV generator-affected control-to-output transfer of the form

$$G_{co-o}^{pv} = -\left[I_{in} \left(s^2 + s \left(\frac{1}{r_{pv} C_2} - \frac{R_{pv}}{L_1} \right) + \frac{1 - (R_{pv}/r_{pv})}{L_1 C_2} \right) / L_1 C_2 \left(s^2 + s \frac{1}{r_{pv} C_2} + \frac{D^2}{L_1 C_2} \right) \right]. \tag{11.6}$$

The roots of the numerator in Eq. (11.6) can be approximated by

$$\omega_{z-HF} \approx \frac{R_{pv}}{L_1} - \frac{1}{r_{pv} C_2}, \tag{11.7}$$

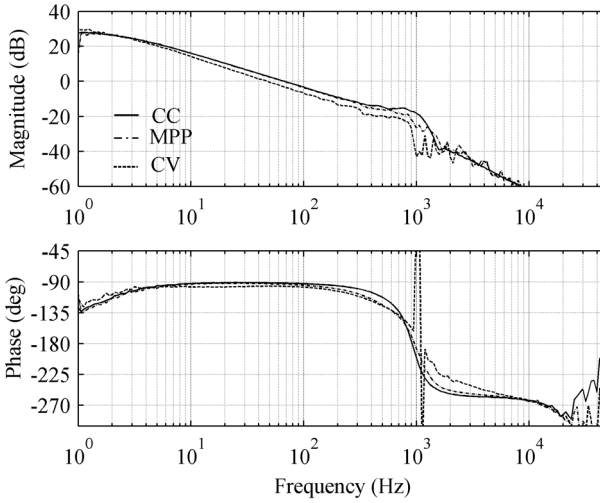


Figure 11.21 The input-voltage loop gains in CCR, CPR (MPP), and CVR.

and

$$\omega_{z-LF} \approx \left(1 - \frac{r_{pv}}{R_{pv}}\right) / \left(\frac{L_1}{R_{pv}} - r_{pv}C_2\right). \quad (11.8)$$

According to Eq. (11.6), the PV generator affects only the resonant damping of the control-to-input transfer function, as also the *Bode* plots in Figure 11.22 clearly shows. The approximated locations of the zeros of the control-to-output transfer functions are shown in Eqs (11.7) and (11.8), respectively. According to Eq. (11.7), we can conclude that the zero lies always in RHP and actually corresponds to the RHP zero of the VF boost converter. The location of the zero in Eq. (11.8) varies depending on the operating point: In CCR, when r_{pv} is high and R_{pv} is low, the

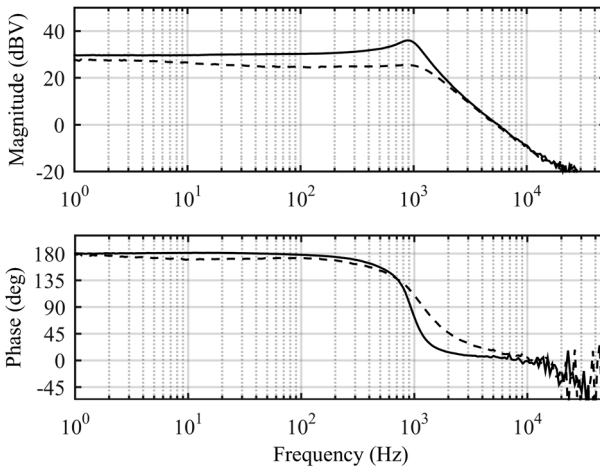


Figure 11.22 The behavior of the control-to-input transfer function (G_{ci-o}), when the operating point is moved from CCR (solid line) into CVR (dashed line).

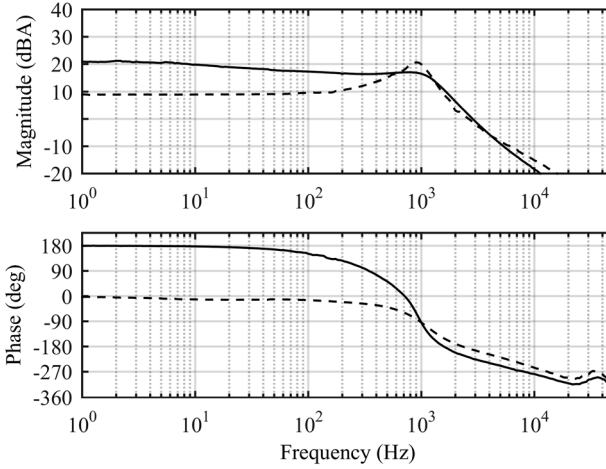


Figure 11.23 The behavior of the control-to-output transfer function (G_{co-o}), when the operating point is moved from CCR (solid line) into CVR (dashed line).

zero locates in RHP; in CPR, the zero locates in the origin; and in CVR, when r_{pv} is low and R_{pv} is high, the zero locates in LHP. The sign of the transfer function also becomes positive when the operating point enters into CVR. Figure 11.23 clearly shows that the above analyses really hold (i.e., change of sign, two RHP zeros in CCR but only one in CVR).

11.4.2.3 CF Superbuck Converter

The experimental CF superbuck converter is shown in Figure 11.24 and the measured input voltage loop gains in Figure 11.25. Figure 11.21 shows that the PV generator affects the resonant damping as well as removing the effect of the input-side capacitor C_1 . The used controller is of type I (i.e., pure integral controller). It may also be quite obvious that the loop crossover frequency has to be less than the parallel resonance visible in the figure.

According to Eq. (11.2), we can compute that the PV generator-affected control-to-input transfer function would be of the form

$$G_{ci-o}^{pv} = \frac{I_{in}}{C_1} \left(s^3 + s^2 \frac{D' V_o}{L_1 I_{in}} + s \frac{D}{L_1 C_2} + \frac{V_o}{L_1 L_2 C_2 I_{in}} \right) / \left(s^4 + s^3 \frac{1}{r_{pv} C_1} + s^2 \frac{(L_1(C_1 + C_2) + L_2(D^2 C_1 + D'^2 C_2))}{L_1 L_2 C_1 C_2} + s \frac{L_1 + D^2 L_2}{L_1 L_2 C_1 C_2 r_{pv}} + \frac{1}{L_1 L_2 C_1 C_2} \right), \quad (11.9)$$

and the PV generator-affected control-to-output transfer of the form

$$G_{co-o}^{pv} = \left(\frac{C_1 + C_2}{C_1 C_2 L_2} I_{in} (s^2 + s \left(\frac{1}{r_{pv}(C_1 + C_2)} - \frac{(DC_1 - D' C_2) R_{pv}}{L_1(C_1 + C_2)} \right) + \frac{1 - (R_{pv}/r_{pv})}{L_1(C_1 + C_2)}) \right) / \left(s^4 + s^3 \frac{1}{r_{pv} C_1} + s^2 \frac{(L_1(C_1 + C_2) + L_2(D^2 C_1 + D'^2 C_2))}{L_1 L_2 C_1 C_2} + s \frac{L_1 + D^2 L_2}{L_1 L_2 C_1 C_2 r_{pv}} + \frac{1}{L_1 L_2 C_1 C_2} \right). \quad (11.10)$$

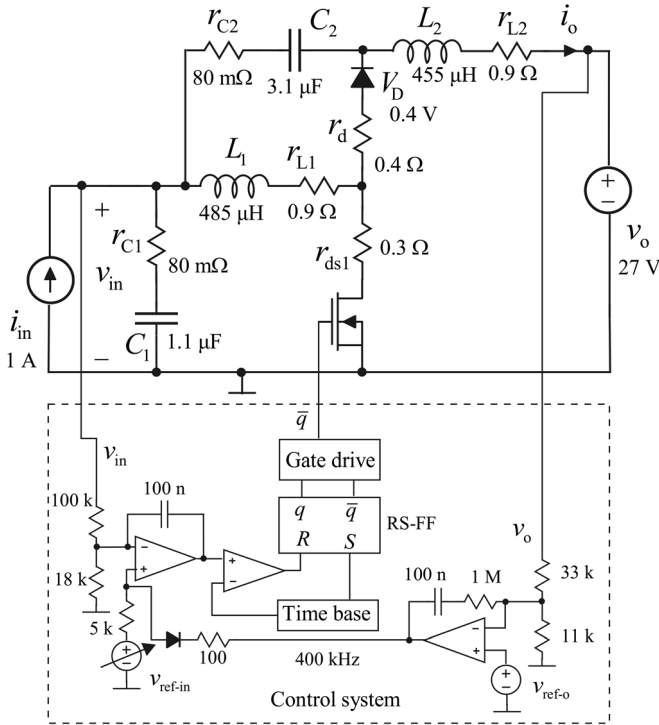


Figure 11.24 The experimental CF superboost converter. Source: Leppäaho 2011. Reproduced with permission of IEEE.

In Figure 11.25, the PV generator-induced changes are naturally the changes taken place in G_{ci-o}^{pv} caused by r_{pv} . If $r_{pv} \gg 1$, then $G_{ci-o}^{pv} \rightarrow G_{ci-o}$ in Chapter 8, which means that the resonances visible in CCR are well damped when the converter enters into CVR. Figure 11.26 shows the behavior of G_{co-o}^{pv} in CCR (solid line) and in CVR

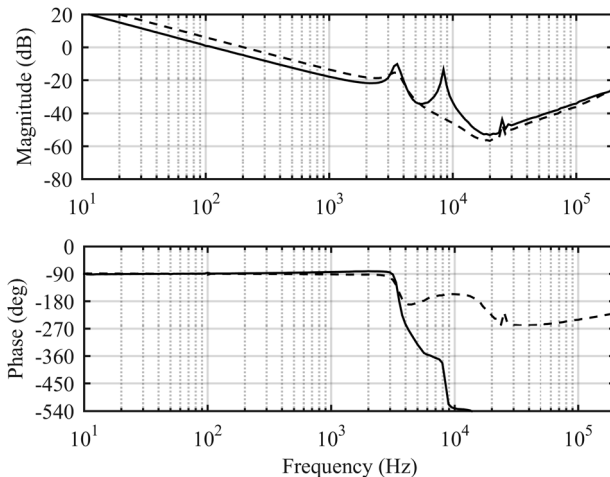


Figure 11.25 The input voltage loop gains in CCR (solid line) and CVR (dashed line).

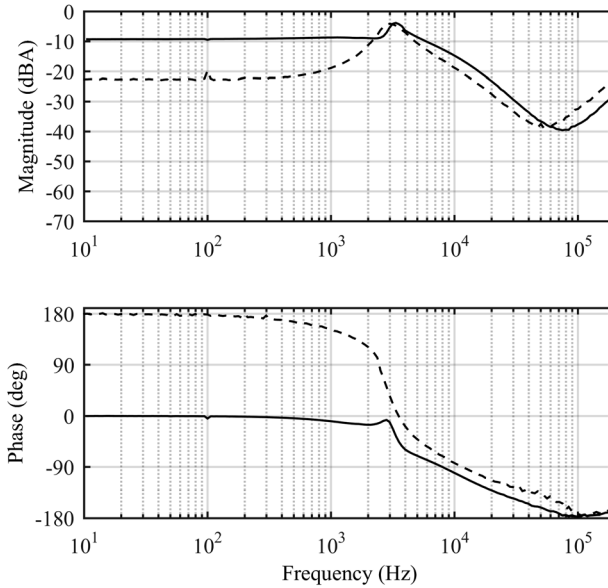


Figure 11.26 The behavior of the control-to-output transfer function (G_{co-o}) when the operating point is moved from CCR (solid line) into CVR (dashed line).

(dashed line). The CVR operating point is quite close to the MPP of the corresponding generator, which is visible in the figure as a drop in the low-frequency magnitude. This phenomenon can also be seen in Eq. (11.10) when we know that $r_{pv} \approx R_{pv}$. If the operating point is moved deeper into CVR then the magnitude would increase, because $r_{pv} \ll R_{pv}$. The change of sign of G_{co-o}^{pv} at the low frequencies and appearing of RHP zeros are also clearly visible, which means that the output current-controlled converter would be unstable in CVR (Figure 11.26).

11.5 Stability Issues in PV Generator Interfacing

The impedance-based stability assessment at the interface between the PV generator and its interfacing converter shall be performed based on the impedance ratio Z_{in-con}/Z_{pv} , which is also known as an inverted minor loop gain [27,32,33]. Stability would exist if the inverted minor loop gain satisfies the *Nyquist* stability criterion (cf. Chapter 2). As stated in Chapter 8, the output impedance of the PV generator equals the parallel connection of a nonlinear resistor and capacitor, respectively. Thus, the instability would take place if the input impedance of the interfacing converter resembles a negative incremental resistance at the low frequencies. This kind of input impedance behavior would exist in the output-side feedback-controlled converters. The PV arrays may need long cables to connect to the interfacing converters, which means that the PV-generator output impedance may also contain a resonant circuit with an operating-point dependent resonance (i.e., the PV generator capacitor would

increase when the operating point moves toward the open-circuit condition) (cf. Figure 10.5). We provide some experimental examples on the instability phenomenon. It may be obvious that if the instability takes place at DC, then there will be no sinusoidal oscillation even in the boundary condition (i.e., $Z_{in-con}/Z_{pv} = -1$). Actually, the phenomenon is usually known as voltage collapse.

11.5.1 Buck Power-Stage Converter

The closed-loop input impedance behavior of the buck power-stage converter (cf. Figure 11.17) is shown in Figure 11.27, when the operating point is varied (i.e., solid line (CCR), dashed line (MPP), and dotted line (CVR)). It may be clear that the converter cannot become unstable when supplied by a PV generator (Figure 10.7) due to the phase behavior of the impedances of a PV generator and the input-voltage-controlled converter.

Figure 11.28 shows the behavior of the input impedance of the output-voltage-controlled converter (solid line) and the corresponding output impedance of the PV generator (dashed line) when the operating point moves from CCR toward MPP. The figure shows that the low-frequency magnitudes of the impedances approach each other and they will be equal at MPP, because $r_{pv} \approx R_{pv}$ at MPP (Note: the low-frequency PV generator impedance equals r_{pv} and the low-frequency converter impedance under output voltage feedback control equals $-R_{pv}$). Figure 11.29 shows the time domain behavior of the PV voltage and current as well as the converter output current when the operating point is placed in CCR and the output voltage feedback controller is activated. The PV voltage drops to the level of output voltage, because the high-side MOSFET is turned permanently on as a consequence of instability and the operating point moved deeply into CCR. The PV and converter output currents are actually equal but the reference

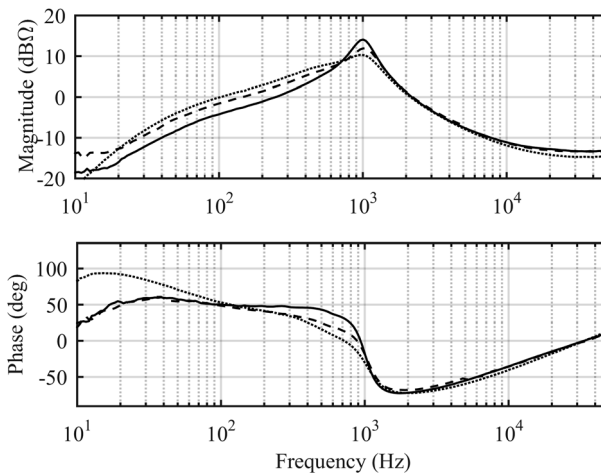


Figure 11.27 The behavior of the closed-loop input impedance (Z_{in-c}) under input-voltage feedback control when the operating point is located in CCR (solid line), at MPP (dashed line), and in CVR (dotted line).

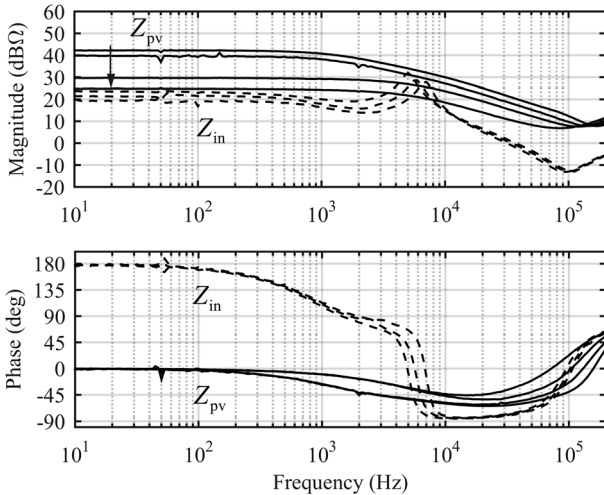


Figure 11.28 The behaviors of the converter closed-loop input impedance (Z_{in}) under output-voltage feedback control (dashed line) and the corresponding output impedance (Z_{pv}) of the PV generator (solid line), when the operating point moves from CCR toward MPP.

level of the PV is slightly shifted below the zero level for visualizing better instability phenomenon.

In Chapter 9, the application of PCM control in PV application was discussed. According to the discussions, the PCM-controlled open-loop buck converter works properly only in CVR. Figure 11.30 shows the measured input impedance of the PCM-controlled buck power stage converter (solid line) and the output impedance of the PV generator when the operating point is moved from CVR to MPP. Similarly as in Figure 11.28, the magnitudes of the impedances become

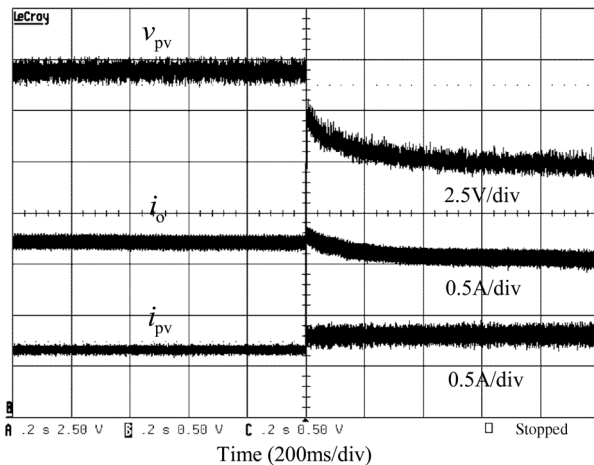


Figure 11.29 The time domain behavior of the PV voltage and current as well as the converter output current when the output-voltage feedback controller is activated in CCR.

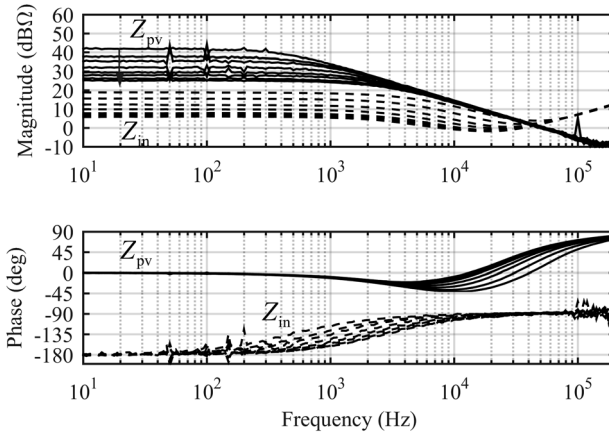


Figure 11.30 The behaviors of the converter open-loop input impedance (Z_{in}) under PCM control (dashed line) and the corresponding output impedance (Z_{pv}) of the PV generator (solid line) when the operating point moves from CVR toward MPP.

equal at MPP and the converter becomes unstable. The time domain behavior of the PV voltage and current as well as the converter output current are shown in Figure 11.31, which indicate clearly that the high-side switch is turned permanently on, and the PV and converter currents become equal.

11.5.2 CF Superbuck Converter

As discussed earlier, the superbuck converter is implemented by applying duality transformation methods and the switch control scheme is also adapted correctly

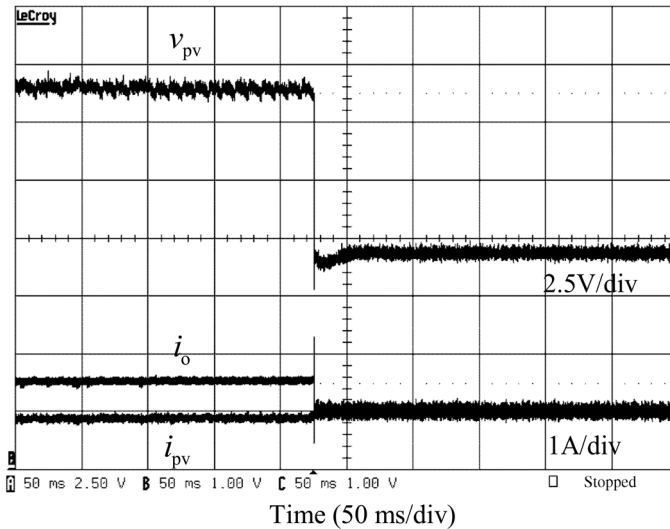


Figure 11.31 The time domain behavior of the PV voltage and current as well as the converter output current when the output-voltage feedback controller is activated in CCR.

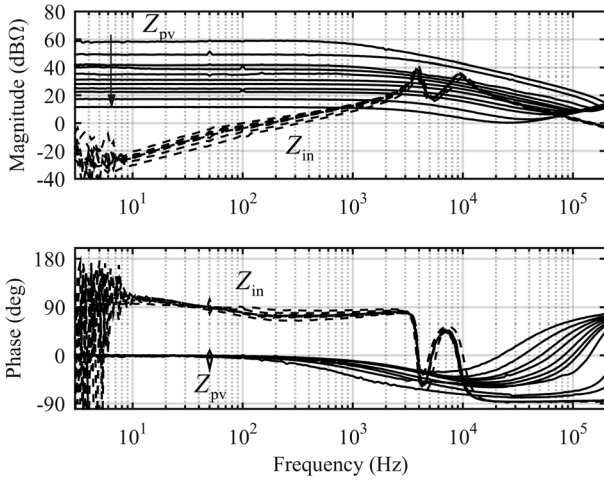


Figure 11.32 The behaviors of the converter closed-loop input impedance (Z_{in}) under input-voltage control (dashed line) and the corresponding output impedance (Z_{pv}) of the PV generator when the operating point moves from CCR into CVR.

to the current-fed application. The power stage of the closed-loop converter is given in Figure 11.24. Figure 11.32 shows the input impedance of the converter under input-voltage feedback control (dashed line) and the output impedance of the PV generator when the operating point is moved from CCR to CVR. The magnitude and phase behavior of the converter and PV generator imply that the instability is not possible to take place.

Figure 11.33 shows the input impedance of the converter under output-voltage feedback control (dashed line) and the output impedance of the PV generator (solid

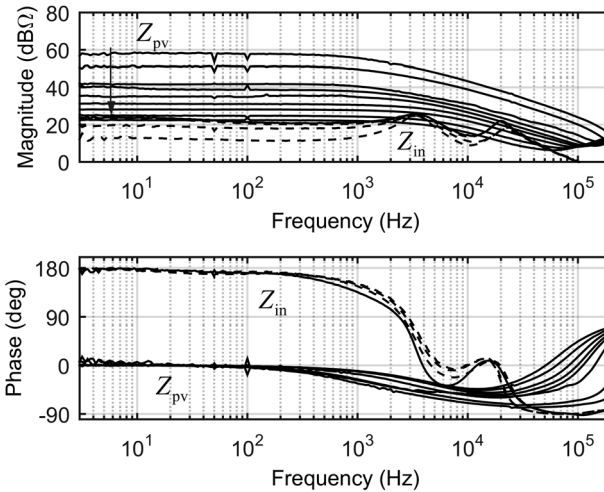


Figure 11.33 The behaviors of the converter closed-loop input impedance (Z_{in}) under output-voltage control (dashed line) and the corresponding output impedance (Z_{pv}) of the PV generator when the operating point moves from CCR toward MPP.

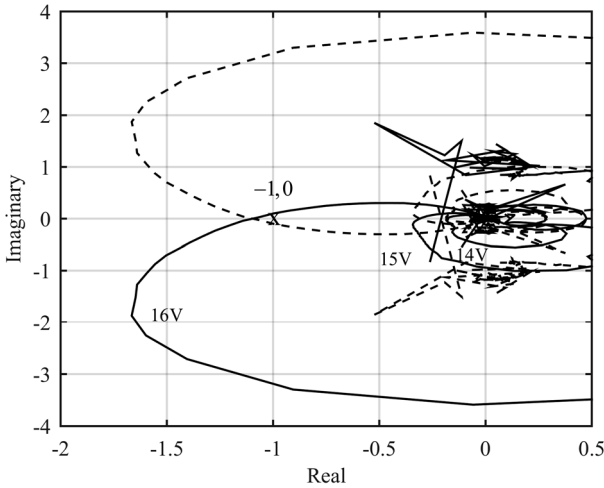


Figure 11.34 Nyquist plots of the impedance ratio Z_{in}/Z_{pv} at $V_{pv} = 14, 15,$ and 16 V.

line) when the operating point is moved from CCR to MPP. The magnitude and phase behavior of the impedances imply that the instability would take place when the operating point enters to MPP. Figure 11.34 shows the corresponding *Nyquist* plots at the PV voltage of 14, 15, and 16 V, which clearly indicate that the converter would be unstable at 16 V, which equals the MPP voltage. Figure 11.35 shows the time domain behavior of the PV voltage and current when the operating point is moved to CVR and the output voltage feedback control is activated. As a consequence of the instability, the operating point is forced to move into CCR, where the operation of the converter will be stable. The power levels of the CRV and CCV operating points are equal. The behavior of the converter after the instability has taken place is quite different compared to the CF converters, where the switch control scheme is adopted from the corresponding VF converters.

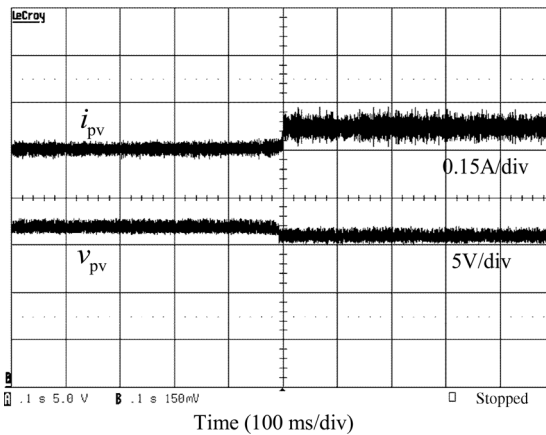


Figure 11.35 The time domain behavior of the PV voltage and current when the output-voltage feedback controller is activated in CVR.

11.5.3 Concluding Remarks

As discussed in Section 11.2, the PV systems can be operated in grid-parallel mode, where the outmost feedback loops are from the input side of the converters. In such cases, the system stability is not compromised. The PV systems can also be operated in grid-forming mode, where the outmost feedback loops are taken from the output side of the converters. In this operation mode, the instability will take place when the operation point is moved to MPP or enters into the region, which is the dual of the intended operation region of the original power stage (i.e., VF power stages in CCR and CF power stages in CVR). As we demonstrated in Section 11.5.1, the instability in VF power stages would cease the operation of the converter totally. In case of CF power stages, the instability would force the operation point to move into the stable region only.

11.6 Control Design Issues

The control design will be performed exactly in a manner similar to that in case of the VF converters discussed in Chapters 2 and 6. In PV applications, an integral (I) controller may suffice and may be sometimes the only working solution as in case of the input voltage control of the superbuck converter (cf. Figure 11.25). In cascaded control schemes (i.e., the inner loop is output current and the outer loop is input voltage), the control design of the current loop will be usually carried out assuming the converter to operate in CVR, and thus the converter is unstable, when the operation point is moved into CCR. The input voltage controller is then designed to stabilize the converter, as discussed in Chapter 9 in case of PCM-controlled buck power stage converter. This kind of issues will be discussed more in the last parts of this book, which are related to the control of grid-connected three-phase converters.

References

- 1 Romero-Cadaval, E., Spagnuolo, G., Franguelo, L.G., Ramos-Paja, C.A., Suntio, T., and Xiao, W.M. (2013) Grid-connected photovoltaic generation plants – components and operation. *IEEE Ind. Electron. Mag.*, 7 (3), 6–20.
- 2 Tonkoski, R., Lopes, L.A.C., and El-Fouly, T.H.M. (2011) Coordinated active power curtailment of grid connected PV inverters for overvoltage prevention. *IEEE Trans. Sustain. Energy*, 2 (2), 139–147.
- 3 Li, C., Savulak, J., and Reinmueller, R. (2014) Unintentional islanding of distributed generation – operating experience from naturally occurred events. *IEEE Trans. Power Deliv.*, 29 (1), 269–274.
- 4 Teodorescu, R., Liserre, M., and Rodriguez, P. (2011) *Grid Converters for Photovoltaic and Wind Power Systems*, John Wiley & Sons, Ltd, Chichester.
- 5 Mäki, A., Valkealahti, S., and Leppäaho, J. (2012) Operation of silicon-based photovoltaic modules under partial shading conditions. *Prog. Photovolt. Res. Appl.*, 20 (3), 298–309.

- 6 Mäki, A. and Valkealahti, S. (2012) Power losses in long string and parallel connected short strings of series connected silicon-based photovoltaic modules under partial shading conditions. *IEEE Trans. Energy Convers.*, **27** (1), 173–183.
- 7 Shmilovitz, D. and Levron, Y. (2012) Distributed maximum power point tracking in photovoltaic systems – emerging architectures and control methods. *Automatika*, **53** (2), 142–155.
- 8 Petrone, G., Spagnuolo, G., and Vitelli, M. (2012) Distributed maximum power point tracking in photovoltaic systems – emerging architectures and control methods. *Automatika*, **53** (2), 128–141.
- 9 Petrone, G., Ramos-Paja, C.A., Spagnuolo, G., and Vitelli, M. (2013) Granular control of photovoltaic arrays by means of a multi-output maximum power point tracking algorithm. *Prog. Photovolt. Res. Appl.*, **21** (5), 918–932.
- 10 Vitelli, M. (2014) On the necessity of joint adoption of both distributed maximum power point tracking and central maximum power point tracking in PV systems. *Prog. Photovolt. Res. Appl.*, **22** (3), 283–299.
- 11 Shimizu, T., Hirakata, M., Kamezava, T., and Watanabe, H. (2001) Generation control circuit for photovoltaic modules. *IEEE Trans. Power Electron.*, **16** (3), 293–300.
- 12 Kadri, R., Gaubert, J.-P., and Champenois, G. (2012) Nondissipative string current diverter for solving the cascaded DC-DC converter connection problem in photovoltaic power generation system. *IEEE Trans. Power Electron.*, **27** (3), 1249–1258.
- 13 Walker, G.R. and Sernia, P.C. (2004) Cascaded DC-DC converter connection of photovoltaic modules. *IEEE Trans. Power Electron.*, **19** (4), 1130–1139.
- 14 Femia, N., Lisi, G., Petrone, G., Spagnuolo, G., and Vitelli, M. (2008) Distributed maximum power point tracking of photovoltaic arrays: novel approach and system analysis. *IEEE Trans. Ind. Electron.*, **55** (7), 2610–2621.
- 15 Huusari, J. and Suntio, T. (2013) Origin of cross-coupling effects in distributed DC-DC converters in photovoltaic applications. *IEEE Trans. Power Electron.*, **28** (10), 5311–5322.
- 16 Pilawa-Podgurski, R.C.N. and Perrault, D.J. (2013) Submodule integrated distributed maximum power point tracking for solar photovoltaic applications. *IEEE Trans. Power Electron.*, **26** (6), 2957–2967.
- 17 Shenoy, P.S., Kim, K.A., Johnson, B.B., and Krein, P.T. (2013) Differential power processing for increased energy production and reliability of photovoltaic systems. *IEEE Trans. Power Electron.*, **28** (6), 2968–2979.
- 18 Olalla, C., Clement, D., Rodriquez, M., and Maksimovic, D. (2013) Architectures and control of submodule integrated DC-DC converters for photovoltaic applications. *IEEE Trans. Power Electron.*, **28** (6), 2980–2997.
- 19 Olalla, C., Deline, C., and Maksimovic, D. (2014) Performance of mismatched PV systems with submodule integrated converters. *IEEE J. Photovolt.*, **4** (1), 396–404.
- 20 Agamy, M.S., Harfman-Todorovic, M., Elasser, A., Chi, S., Steigerwald, R.L., Sabate, J.A., McCann, A.J., Shang, L., and Mueller, F.J. (2014) An efficient partial power processing DC/DC converter for distributed PV architectures. *IEEE Trans. Power Electron.*, **29** (2), 674–686.

- 21 Kasper, M., Bostis, D., and Kolar, J. (2014) Classification and comparative evaluation of PV panel-integrated DC–DC converter concepts. *IEEE Trans. Power Electron.*, **29** (5), 2511–2526.
- 22 Nousiainen, L., Puuko, J., Mäki, A., Messo, T., Huusari, J., Jokipii, J., Viinamäki, J., Torres Lobera, D., Valkealahti, S., and Suntio, T. (2013) Photovoltaic generator as an input source for power electronic converters. *IEEE Trans. Power Electron.*, **28** (6), 3028–3038.
- 23 Wyatt, J.L. and Chua, L.O. (1983) Nonlinear resistive maximum power theorem with solar cell application. *IEEE Trans. Circuits Syst.*, **CAS.30** (11), 824–828.
- 24 Ziao, W., Dunford, W.G., Palmer, P.R., and Capel, A. (2007) Regulation of photovoltaic voltage. *IEEE Trans. Ind. Electron.*, **54** (3), 1365–1374.
- 25 Xiao, W., Ozog, N., and Dunford, W.G. (2007) Toplogy study of photovoltaic interface for maximum power point tracking. *IEEE Trans. Ind. Electron.*, **54** (3), 1696–1704.
- 26 Suntio, T., Viinamäki, J., Jokipii, J., Messo, T., and Kuperman, A. (2014) Dynamic characteristics of power electronic interfaces. *IEEE J. Emerg. Sel. Top. Power Electron.*, **2** (4), 949–961.
- 27 Suntio, T., Leppäaho, J., Huusari, J., and Nousiainen, L. (2010) Issues on solar-generator interfacing with current-fed MPP-tracking converters. *IEEE Trans. Power Electron.*, **25** (9), 2409–2419.
- 28 Suntio, T., Huusari, J., and Leppäaho, J. (2010) Issues on solar-generator interfacing with voltage-fed MPP-tracking converters. *Eur. Power Electron. Drives J.*, **20** (3), 40–47.
- 29 Leppäaho, J., Nousiainen, L., Puukko, J., Huusari, J., and Suntio, T. (2010) Implementing current-fed converters by adding an input capacitor at the input of voltage-fed converter for interfacing solar generator. Proceedings of the EPE-PEMC, pp. 76–80.
- 30 Viinamäki, J., Jokipii, J., Messo, T., Suntio, T., Sitbon, M., and Kuperman, A. (2015) Comprehensive dynamic analysis of PV-generator-interfacing DC–DC boost-power-stage converter. *IET Renew. Power Gener.*, **9** (4), 306–314.
- 31 Leppäaho, J. and Suntio, T. (2011) Dynamic characteristics of current-fed superbuck converter. *IEEE Trans. Power Electron.*, **26** (1), 200–209.
- 32 Leppäaho, J., Huusari, J., Nousiainen, L., Puukko, J., and Suntio, T. (2011) Dynamic properties and stability assessment of current-fed converters in photovoltaic applications. *IEE J Trans. Ind. Appl.*, **131** (8), 976–984.
- 33 Leppäaho, J. and Suntio, T. (2014) Characterizing the dynamics of peak-current-mode-controlled buck-power-stage converter in photovoltaic applications. *IEEE Trans. Power Electron.*, **29** (7), 3840–3847.

Part Four

Three-Phase Grid-Connected Converters

12

Dynamic Modeling of Three-Phase Inverters

12.1 Introduction

This chapter presents a systematic method to obtain dynamic models for three-phase grid-connected inverters. After studying this chapter, the reader should be familiar with the concept of dynamic modeling of three-phase inverters in d - q domain and be able to derive unterminated open-loop models for voltage and current-fed inverters with L and LCL -type filters. Moreover, the reader should be familiar with the methods for evaluating the dynamic effect of nonideal source impedance.

In this chapter, dynamic models of voltage and current-fed inverter are derived without the effect of source [1] and load impedance [2]. Such model is referred as an un-terminated model [3]. The dynamic models are derived in the d - q domain where three-phase sinusoidal signals can be analyzed as equivalent DC signals [4,5]. Moreover, the models do not include the dynamic effects of control functions, such as AC current control or DC voltage control. The open-loop models for voltage and current-fed inverters and current-fed inverter with an LCL -filter are derived. It is also demonstrated how the dynamic effect of source impedance, such as a PV generator or an upstream DC-DC converter, can be included in the dynamic model. The analysis in this book is restricted to two-level inverters. However, the ideas and concepts can be adapted to multilevel inverters, such as neutral-point-clamped three-phase inverters [6,7] that are widely used by the industry.

Grid-connected inverters can be divided into two classes depending on the type of the source. In voltage-fed inverters, the DC source is a constant voltage source, such as a storage battery [8]. In current-fed inverters, the DC source is a constant current source, such as a photovoltaic generator in a single-stage PV inverter [9]. The type of the source is an important feature since it defines how input and output variable at the DC-side is selected. Therefore, voltage-fed and current-fed inverters have different dynamic models. Moreover, when the DC-link voltage is regulated by the inverter control system, the inverter should be analyzed as a current-fed inverter for correct formulations of input and output variables [10].

The open-loop models are first derived analytically and then MATLAB is used to solve the transfer functions numerically (or in some cases in symbolic form).

MATLAB Simulink with SimScape package is used for time domain simulations and for model verification.

The analysis in this chapter is based on the amplitude invariant Clarke's transformation, which can be defined as in Eq. (12.1).

$$\mathbf{T}_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (12.1)$$

12.2 Dynamic Model of Voltage-Fed Inverter

Voltage-fed inverters are found in applications where the inverter input voltage is determined by a stiff source, such as a battery storage depicted in Figure 12.1. The battery usually has some internal impedance that depends on its state of charge. Effect of source impedance Z_{bat} can be included in the model by solving the source-affected transfer functions as discussed later. Grid-connected battery storage should be analyzed as an inverter when it operates in discharging mode feeding power to the grid. In charging mode, power flow reverses and the power stage should be analyzed as an active rectifier. In that case, the AC terminals become input ports and the DC terminal becomes an output port. This chapter only discusses the discharging mode.

12.2.1 Average Model of Voltage-Fed Inverter

A two-level inverter employs six controllable switches, whereas, a three-level NPC inverter has two extra transistors and diodes per phase. Three-level inverters are widely used in grid-connected applications due to lower voltage rating requirement of the transistors and lower switching ripple. Modeling of three-

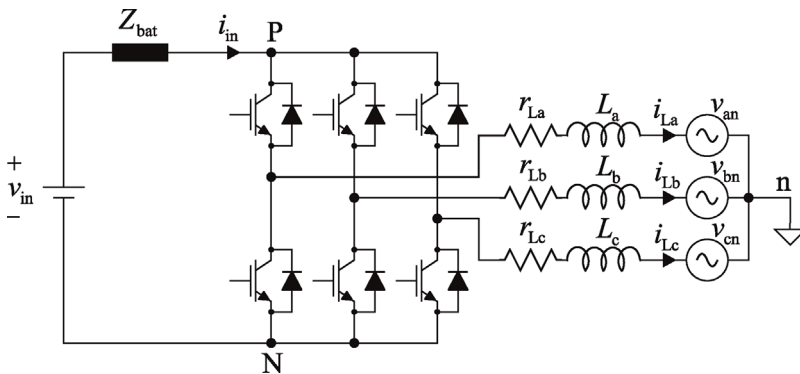


Figure 12.1 Grid-connected battery storage inverter.

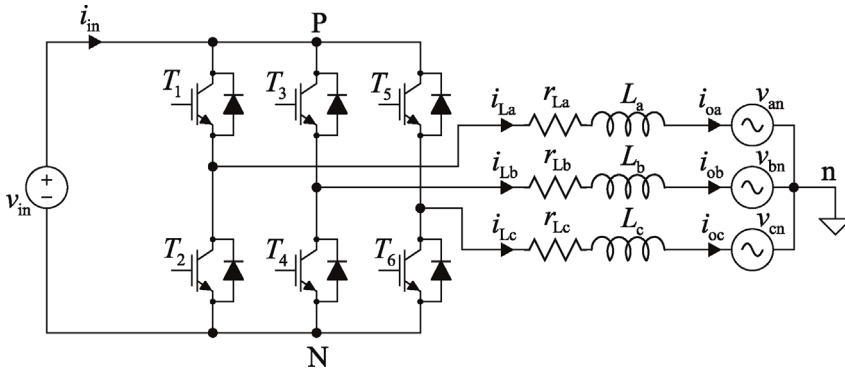


Figure 12.2 Three-phase voltage-fed inverter.

level inverters is out of scope of this book. However, the same modeling methods can be adapted to three-level inverters.

Voltage-fed inverter with an ideal input source and an ideal three-phase voltage-type load is shown in Figure 12.2. The input voltage v_{in} and three-phase grid voltages v_{an} , v_{bn} , and v_{cn} are chosen as input variables, inductor currents i_{L_a} , i_{L_b} , and i_{L_c} are selected as state variables, and the input current i_{in} and three-phase output currents i_{oa} , i_{ob} , and i_{oc} are selected as output variables. The inductor currents are essentially the same as output currents.

Duty ratios of lower switches in each phase-leg are complements of upper switch duty ratios. Therefore, both switches on a phase-leg are never on at the same time. Dead-time (or blanking time) is added near the switching instants to guarantee that the DC source is not short-circuited. During dead-time, control signals of both the upper and lower switches are low, for example, transistors T_1 and T_2 . The dead-time introduces an additional nonlinear element in the circuit, because during the dead-time the phase current flows through an antiparallel diode. The dead-time effect produces similar harmonic components in the grid current as a three-phase diode rectifier. However, the effect of dead-time is neglected in the following to simplify analysis.

For modeling purposes, it is sufficient to treat only the duty ratios of either upper or lower switches as controllable variables. It is customary to select the upper switches as controlled switches and denote their duty ratios as d_A , d_B , and d_C . Duty ratios of low-side switches can be generated by, for example, a DSP-based control platform. Current directions out of the source and toward the three-phase grid are defined positive, as shown in Figure 12.2.

Power stage of the three-phase inverter can be represented as an equivalent switching circuit, as depicted in Figure 12.3. The switch matrix has eight possible switching states, as shorting the voltage source is not allowed. Ohmic losses caused by transistors are modeled by the resistance r_{ds} that represents the on-time resistance of a switch between its drain and source terminals. Switches, such as IGBTs, have an additional constant voltage drop whose polarity depends on direction of the current though the switch that greatly complicates the analysis. It is assumed that the switching losses can be modeled by using parasitic resistance. All inductors are assumed symmetric with equal nonsaturable inductance L and

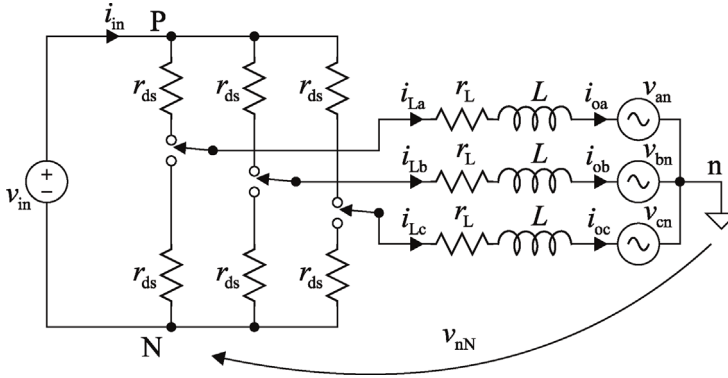


Figure 12.3 Equivalent switching circuit of a voltage-fed inverter.

resistance r_L . Ideally the resistance value should also include the losses generated by eddy current losses [11].

It is possible to analyze each of the eight switching states as a separate subcircuit and to develop the corresponding average model as it is commonly done for DC–DC converters [12]. Fortunately, common-mode voltage v_{nN} can be utilized to simplify derivation of the average model. Voltage over each phase inductor can be defined in both switching states of a phase-leg to find out the inductor current derivatives. The inductor voltage can be obtained by utilizing Kirchhoff's voltage law when the corresponding phase-leg is connected either to the P or N terminal of the power stage.

Voltage over inductor in phase i ($i = a, b, c$) can be given as

$$v_{Li}^P = v_{in} - (r_{ds} + r_L)i_{Li} - v_{in} - v_{nN},$$

when phase-leg i is connected to DC terminal P, and as

$$v_{Li}^N = -(r_{ds} + r_L)i_{Li} - v_{in} - v_{nN},$$

when phase-leg i is connected to DC terminal N.

Average voltage over the inductance in phase i can be obtained by averaging the inductor voltage equations over one switching cycle that corresponds to one period of triangular waveform of the SPWM. The derivatives of averaged inductor currents can be expressed as

$$\frac{d\langle i_{Li} \rangle}{dt} = \frac{1}{L} (d_i \langle v_{in} \rangle - r_{eq} \langle i_{Li} \rangle - \langle v_{in} \rangle - \langle v_{nN} \rangle), \quad (12.2)$$

where ohmic losses of switches and inductors are lumped together as an equivalent parasitic resistance r_{eq} .

Average three-phase inductor current derivatives can be represented using vector notation as

$$\frac{d}{dt} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} = \frac{1}{L} \left(\begin{bmatrix} d_A \\ d_B \\ d_C \end{bmatrix} \cdot \langle v_{in} \rangle - r_{eq} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} - \begin{bmatrix} \langle v_{an} \rangle \\ \langle v_{bn} \rangle \\ \langle v_{cn} \rangle \end{bmatrix} - \begin{bmatrix} \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \end{bmatrix} \right). \quad (12.3)$$

The three-phase variables can be given in stationary reference frame by space vectors by multiplying the equation from the left-hand side by the Clarke's transformation matrix $T_{\alpha\beta}$ as

$$\frac{d}{dt} T_{\alpha\beta} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} = \frac{1}{L} \left(T_{\alpha\beta} \begin{bmatrix} d_A \\ d_B \\ d_C \end{bmatrix} \cdot \langle v_{in} \rangle - r_{eq} \cdot T_{\alpha\beta} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} - T_{\alpha\beta} \begin{bmatrix} \langle v_{an} \rangle \\ \langle v_{bn} \rangle \\ \langle v_{cn} \rangle \end{bmatrix} - T_{\alpha\beta} \begin{bmatrix} \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \end{bmatrix} \right). \quad (12.4)$$

The three-phase variables can be represented in the stationary reference frame (or $\alpha\beta$ -domain) as

$$\frac{d}{dt} \begin{bmatrix} \langle i_{L\alpha} \rangle \\ \langle i_{L\beta} \rangle \\ \langle i_{L0} \rangle \end{bmatrix} = \frac{1}{L} \left(\begin{bmatrix} d_\alpha \\ d_\beta \\ d_0 \end{bmatrix} \cdot \langle v_{in} \rangle - r_{eq} \cdot \begin{bmatrix} \langle i_{L\alpha} \rangle \\ \langle i_{L\beta} \rangle \\ \langle i_{L0} \rangle \end{bmatrix} - \begin{bmatrix} \langle v_{\alpha n} \rangle \\ \langle v_{\beta n} \rangle \\ \langle v_{0n} \rangle \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ \langle v_{nN} \rangle \end{bmatrix} \right). \quad (12.5)$$

The average common-mode voltage $\langle v_{nN} \rangle$ affects only the DC component of inductor current that can be easily proven by applying Clarke's transformation to the vector $[\langle v_{nN} \rangle \ \langle v_{nN} \rangle \ \langle v_{nN} \rangle]^T$. There is no path for zero sequence inductor current $\langle i_{L0} \rangle$ in the three-wire converter. Therefore, the zero sequence components $\langle i_{L0} \rangle$, d_0 , $\langle v_{0n} \rangle$, and $\langle v_{nN} \rangle$ can be neglected.

The derivative of inductor current can be represented in the $\alpha\beta$ -domain by a rotating space vector as in Eq. (12.6), that is, the variables are simply written by using complex notation as, $(x_\alpha + jx_\beta = \mathbf{x}^{\alpha\beta})$. The subscript o is used to denote that the grid voltage space vector represents the voltage at the output terminals of the inverter power stage.

$$\frac{d(\langle \mathbf{i}_L^{\alpha\beta} \rangle)}{dt} = \mathbf{d}^{\alpha\beta} \frac{\langle v_{in} \rangle}{L} - \frac{r_{eq}}{L} \langle \mathbf{i}_L^{\alpha\beta} \rangle - \frac{1}{L} \langle \mathbf{v}_o^{\alpha\beta} \rangle. \quad (12.6)$$

A space vector in the $\alpha\beta$ -domain can be given in the dq-domain by multiplying the space vector with a rotating unit vector according to Eq. (12.7). The angular grid frequency ω_s is assumed to remain constant.

$$\mathbf{x}^{\alpha\beta} = \mathbf{x}^{dq} \cdot \mathbf{e}^{j\theta_s(t)} = \mathbf{x}^{dq} \cdot \mathbf{e}^{j\omega_s t}. \quad (12.7)$$

According to the above relation, the derivative of inductor current can be given in the dq-domain as

$$\frac{d(\langle \mathbf{i}_L^{dq} \rangle \cdot \mathbf{e}^{j\omega_s t})}{dt} = \mathbf{d}^{dq} \cdot \mathbf{e}^{j\omega_s t} \frac{\langle v_{in} \rangle}{L} - \frac{r_{eq}}{L} \langle \mathbf{i}_L^{dq} \rangle \cdot \mathbf{e}^{j\omega_s t} - \frac{1}{L} \langle \mathbf{v}_o^{dq} \rangle \cdot \mathbf{e}^{j\omega_s t}. \quad (12.8)$$

By applying the product rule on the left-hand side of the equation, dividing by $\mathbf{e}^{j\omega_s t}$ and by rearranging, the inductor current can be given in the dq-domain as shown in Eq. (12.9). The inductor current d- and q-components are coupled by the term $j\omega_s$, which is why usually decoupling gains in the current control are used, as will

be explained in more detail in Chapter 13.

$$\frac{d\langle \mathbf{i}_L^{dq} \rangle}{dt} = \mathbf{d}^{dq} \frac{\langle v_{in} \rangle}{L} - j\omega_s \langle \mathbf{i}_L^{dq} \rangle - \frac{r_{eq}}{L} \langle \mathbf{i}_L^{dq} \rangle - \frac{1}{L} \langle \mathbf{v}_o^{dq} \rangle. \quad (12.9)$$

The d- and q-components can be written separately and the average model of the voltage-fed inverter can be given as in Eqs. (12.10)–(12.14). The average model can be used as a fast simulation tool to evaluate the stability and performance of, for example, current controllers prior to actual laboratory tests. However, the model is not suitable for simulations where high-frequency phenomena, such as switching ripple, are of interest.

$$\frac{d\langle i_{Ld} \rangle}{dt} = \frac{1}{L} (d_d \langle v_{in} \rangle + \omega_s L \langle i_{Lq} \rangle - r_{eq} \langle i_{Ld} \rangle - \langle v_{od} \rangle). \quad (12.10)$$

$$\frac{d\langle i_{Lq} \rangle}{dt} = \frac{1}{L} (d_q \langle v_{in} \rangle - \omega_s L \langle i_{Ld} \rangle - r_{eq} \langle i_{Lq} \rangle - \langle v_{oq} \rangle). \quad (12.11)$$

$$\langle i_{in} \rangle = \frac{3}{2} (d_d \langle i_{Ld} \rangle + d_q \langle i_{Lq} \rangle). \quad (12.12)$$

$$\langle i_{od} \rangle = \langle i_{Ld} \rangle. \quad (12.13)$$

$$\langle i_{oq} \rangle = \langle i_{Lq} \rangle. \quad (12.14)$$

An equivalent circuit diagram can be depicted based on the average model as shown in Figure 12.4. The inverter has one DC input port and two output ports that are often referred as the d and q-channels in the literature [10,13]. It is possible to approximate the inverter dynamics by neglecting the q-channel dynamics that gives good approximations at unity power factor [13]. However, control functions, such as grid synchronization, affect only the q-channel dynamics and should be analyzed carefully [14].

Steady-state operating point can be solved in the dq-domain by setting the derivative terms equal to zero and by substituting all variables with their corresponding steady-state values, that is, using uppercase letters. The steady-state operating point is as given in Eqs. (12.15)–(12.19). It should be noted that the steady-state values of inductor current d and q-components are the reference

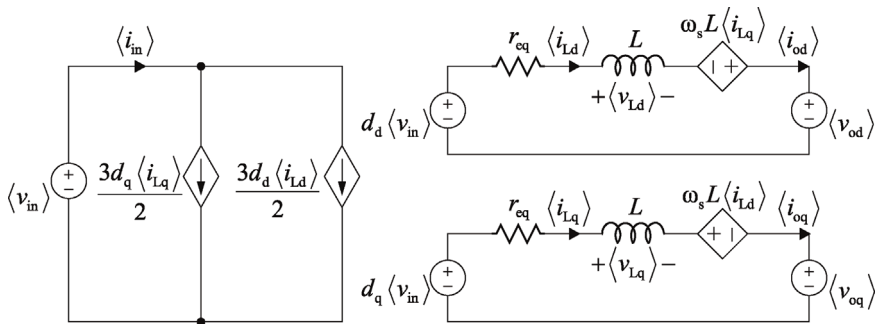


Figure 12.4 Equivalent linearized circuit diagram of voltage-fed inverter in the d-q domain.

values of output currents that are selected based on required real and reactive power.

$$I_{Ld} = I_{od}^* \quad (12.15)$$

$$I_{Lq} = I_{oq}^* \quad (12.16)$$

$$D_d = \frac{V_{od} + r_{eq}I_{Ld} - \omega_s LI_{Lq}}{V_{in}} \quad (12.17)$$

$$D_q = \frac{V_{oq} + r_{eq}I_{Lq} + \omega_s LI_{Ld}}{V_{in}} \quad (12.18)$$

$$I_{in} = \frac{3}{2} (D_d I_{Ld} + D_q I_{Lq}) \quad (12.19)$$

12.2.2 Linearized State-Space and Open-Loop Dynamics

The average model can be linearized at the steady-state operating point by using the first-order expansion of the Taylor series. In other words, the average model is linearized by solving the first-order partial derivatives in respect to each state and input variable. The linearized state-space of the voltage-fed inverter can be given as in Eqs. (12.20)–(12.24).

$$\frac{d\hat{i}_{Ld}}{dt} = -\frac{r_{eq}}{L}\hat{i}_{Ld} + \omega_s\hat{i}_{Lq} + \frac{D_d}{L}\hat{v}_{in} - \frac{1}{L}\hat{v}_{od} + \frac{V_{in}}{L}\hat{d}_d \quad (12.20)$$

$$\frac{d\hat{i}_{Lq}}{dt} = -\omega_s\hat{i}_{Ld} - \frac{r_{eq}}{L}\hat{i}_{Lq} + \frac{D_q}{L}\hat{v}_{in} - \frac{1}{L}\hat{v}_{oq} + \frac{V_{in}}{L}\hat{d}_q \quad (12.21)$$

$$\hat{i}_{in} = \frac{3D_d}{2}\hat{i}_{Ld} + \frac{3D_q}{2}\hat{i}_{Lq} + \frac{3I_{Ld}}{2}\hat{d}_d + \frac{3I_{Lq}}{2}\hat{d}_q \quad (12.22)$$

$$\hat{i}_{od} = \hat{i}_{Ld} \quad (12.23)$$

$$\hat{i}_{oq} = \hat{i}_{Lq} \quad (12.24)$$

Input, output, and state variables can be collected in vectors \mathbf{u} , \mathbf{y} , \mathbf{x} and constant terms in matrices \mathbf{A} , \mathbf{B} , \mathbf{C} , and \mathbf{D} as shown in Eqs. (12.25) and (12.26).

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \end{bmatrix} = \begin{bmatrix} -\frac{r_{eq}}{L} & \omega_s \\ -\omega_s & -\frac{r_{eq}}{L} \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \end{bmatrix} + \begin{bmatrix} \frac{D_d}{L} & -\frac{1}{L} & 0 & \frac{V_{in}}{L} & 0 \\ \frac{D_q}{L} & 0 & -\frac{1}{L} & 0 & \frac{V_{in}}{L} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.25)$$

$$\underbrace{\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix}}_y = \underbrace{\begin{bmatrix} \frac{3D_d}{2} & \frac{3D_q}{2} \\ 1 & 0 \\ 0 & 1 \end{bmatrix}}_C \cdot \underbrace{\begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \end{bmatrix}}_x + \underbrace{\begin{bmatrix} 0 & 0 & 0 & \frac{3I_{Ld}}{2} & \frac{3I_{Lq}}{2} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}}_D \cdot \underbrace{\begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}}_u \quad (12.26)$$

The state-space can be transformed into the frequency domain by replacing the derivative operator with Laplace variable s that allows solving the transfer functions according to Eq. (12.27).

$$\mathbf{G} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}. \quad (12.27)$$

Transfer functions of the voltage-fed inverter should be named according to their function as in Eq. (12.28) where subscript extension $-o$ is used to denote open-loop transfer functions. The transfer functions correspond to the Y -parameters presentation [15]. An example of MATLAB-code for solving the open-loop transfer functions is illustrated in Figure 12.5.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} = \begin{bmatrix} Y_{in-o} & T_{oid-o} & T_{oiq-o} & G_{cid-o} & G_{ciq-o} \\ G_{iod-o} & -Y_{odd-o} & -Y_{oqd-o} & G_{codd-o} & G_{coqd-o} \\ G_{ioq-o} & -Y_{odq-o} & -Y_{oqq-o} & G_{codq-o} & G_{coqq-o} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.28)$$

Transfer functions of the same type, that is, control-to-input-current or input-to-output-current, can be collected into two-by-two submatrices, that is, transfer matrices as demonstrated in Eq. (12.29) that allows writing the dynamics as an equivalent MIMO system as in Eq. (12.30). Such approach enables modeling the cross-coupling dynamics since the model does not have to be simplified by neglecting any dynamics, such as cross-coupling transfer functions between d and q-components. It should be noted that the second element of input current vector \hat{i}_{in} is zero since the input terminal is a DC source. However, the input current of an active rectifier is two-dimensional in which case the input current vector would be defined using d and q-components of a three-phase current, as discussed in Chapter 17.

$$\begin{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ 0 \end{bmatrix} \\ \begin{bmatrix} \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} Y_{in-o} & 0 \\ 0 & 0 \end{bmatrix} \\ \begin{bmatrix} G_{iod-o} & 0 \\ G_{ioq-o} & 0 \end{bmatrix} \end{bmatrix} - \begin{bmatrix} \begin{bmatrix} T_{oid-o} & T_{oiq-o} \\ 0 & 0 \end{bmatrix} \\ \begin{bmatrix} Y_{odd-o} & Y_{oqd-o} \\ Y_{odq-o} & Y_{oqq-o} \end{bmatrix} \end{bmatrix} + \begin{bmatrix} \begin{bmatrix} G_{cid-o} & G_{ciq-o} \\ 0 & 0 \end{bmatrix} \\ \begin{bmatrix} G_{codd-o} & G_{coqd-o} \\ G_{codq-o} & G_{coqq-o} \end{bmatrix} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_{in} \\ 0 \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.29)$$

```

% Open-loop transfer functions of voltage-fed inverter

run parameters %parameters defined in another file
s=tf('s');

A=[-r_eq/L, omega;
   -omega, -r_eq/L];

B=[Dd/L, -1/L, 0, Vin/L, 0;
   Dq/L, 0, -1/L, 0, Vin/L];

C=[3*Dd/2, 3*Dq/2;
   1, 0; 0, 1];

D=[0, 0, 0, 3*ILd/2, 3*ILq/2;
   0, 0, 0, 0, 0;
   0, 0, 0, 0, 0];

G=C*(inv(s*eye(2)-A)*B)+D;

%input dynamics at open-loop
Yin_o=G(1,1);
Toid_o=G(1,2), Toid_o=G(1,3);
Gcid_o=G(1,4), Gciq_o=G(1,5);

%output dynamics (d-channel)
Giod_o=G(2,1);
Yodd_o=-G(2,2), Yoqd_o=-G(2,3);
Gcodd_o=G(2,4), Gcoqd_o=G(2,5);

%output dynamics (q-channel)
Gioq_o=G(3,1);
Yodq_o=-G(3,2), Yoqq_o=-G(3,3);
Gcodq_o=G(3,4), Gcoqq_o=G(3,5);

```

Figure 12.5 Example of MATLAB code for solving the open-loop transfer functions.

$$\begin{bmatrix} \hat{\mathbf{i}}_{in} \\ \hat{\mathbf{i}}_o \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{in-o} & \mathbf{T}_{oi-o} & \mathbf{G}_{ci-o} \\ \mathbf{G}_{io-o} & -\mathbf{Y}_{o-o} & \mathbf{G}_{co-o} \end{bmatrix} \cdot \begin{bmatrix} \hat{\mathbf{v}}_{in} \\ \hat{\mathbf{v}}_o \\ \hat{\mathbf{d}} \end{bmatrix} \quad (12.30)$$

A three-port model can be illustrated based on Eq. (12.29) which has one DC input port and two AC output ports, that is, the d and q-channels as shown in Figure 12.6. Such a linear circuit may not be the most elegant circuit, because the cross-coupling admittance terms Y_{oqd-o} and Y_{odq-o} have to be modeled as controllable current sources that contradicts with their physical interpretation. However, the three-port model is a useful representation in cases when cross-coupling transfer functions can be neglected. The three-port model is used in Chapter 14 to evaluate the dynamic effect of output AC capacitor and in Chapter 16 to evaluate the dynamic effect of load impedance, such as finite grid impedance.

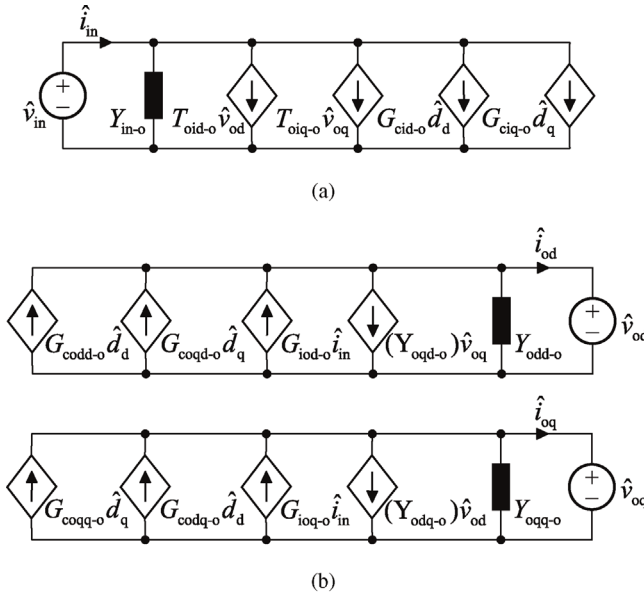


Figure 12.6 Linear three-port model of a voltage-fed inverter. a) Input DC port. b) Output d and q-channels.

A two-port model is shown in Figure 12.7 based on Eq. (12.30) which resembles the small-signal linear equivalent circuit of a DC–DC converter. The main difference with conventional linear two-port model is that system inputs and outputs are defined as two-dimensional vectors and the transfer functions are represented by two-by-two transfer matrices. Both input and output ports are defined as similar to Norton’s equivalent circuit. The two-port model is useful in determining source and load effects, for example, to evaluate the effect of grid impedance or upstream DC–DC converter to control dynamics. Moreover, the cross-coupling transfer functions can be included in the dynamics.

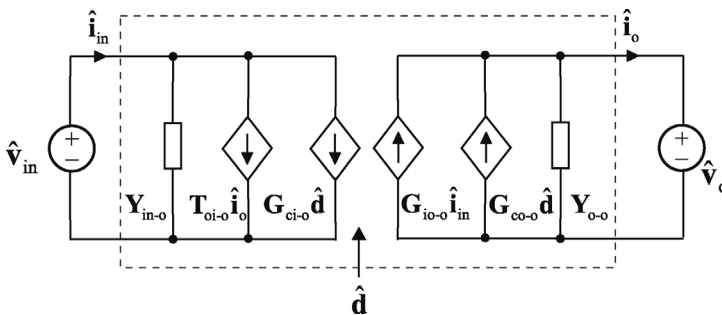


Figure 12.7 Two-port model of voltage-fed inverter.

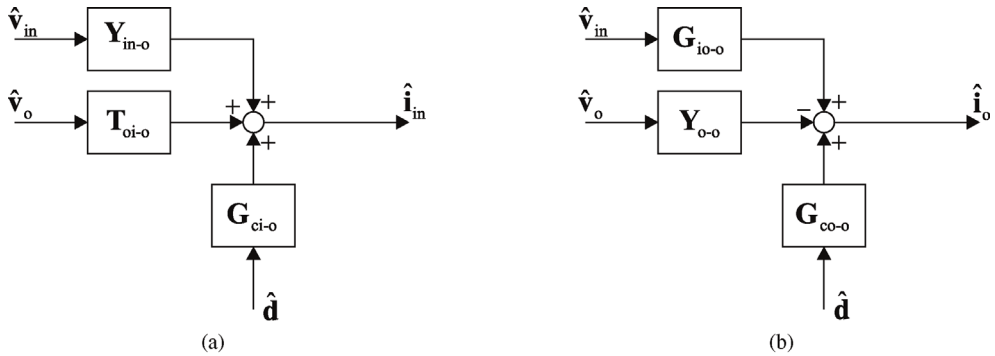


Figure 12.8 Full-order (a) input and (b) output dynamics of the voltage-fed inverter at open loop.

12.2.3 Control Block Diagrams of Voltage-Fed Inverter

Control block diagrams representing the input and output dynamics of a voltage-fed inverter at open loop can be depicted in Figure 12.8. Control block diagrams resemble those that are conventionally used to present dynamics of a DC–DC converter. Solving the closed-loop dynamics requires careful application of matrix algebra and, thus, cannot be easily seen from the control block diagram, as in the case of a DC–DC converter. Controller transfer functions, sensing gains, and feedforward gains can be added in the open-loop control block diagrams to solve the dynamic effect of various control schemes, feedforward loops, and grid synchronization.

The dynamic model can be simplified to reduce the order of transfer functions to reduce computational burden and to obtain results that are easier to interpret. In that case, input dynamics are assumed to be dominated by transfer functions related to d-components and all cross-couplings are neglected in the output dynamics. Such assumptions yield control block diagrams according to Figure 12.9 where the output dynamics are shown as two independent block diagrams. The block diagram can be thought as the linearized version of the equivalent circuit diagram in Figure 12.4, that is, one input port and two decoupled output ports.

12.2.4 Verification of Open-Loop Model

A dynamic model may lead to wrong conclusions in, for example, determining control system stability, if its accuracy has not been verified. The validity of the open-loop model should be verified by measuring all transfer functions from a prototype and by ensuring that the measured frequency responses match the analytical model with sufficient accuracy. However, in real applications, the DC source affects the transfer functions due to source effect and the three-phase AC system affects the dynamics through load effect. Therefore, it is often impossible to verify the unterminated model by other means than a circuit simulator.

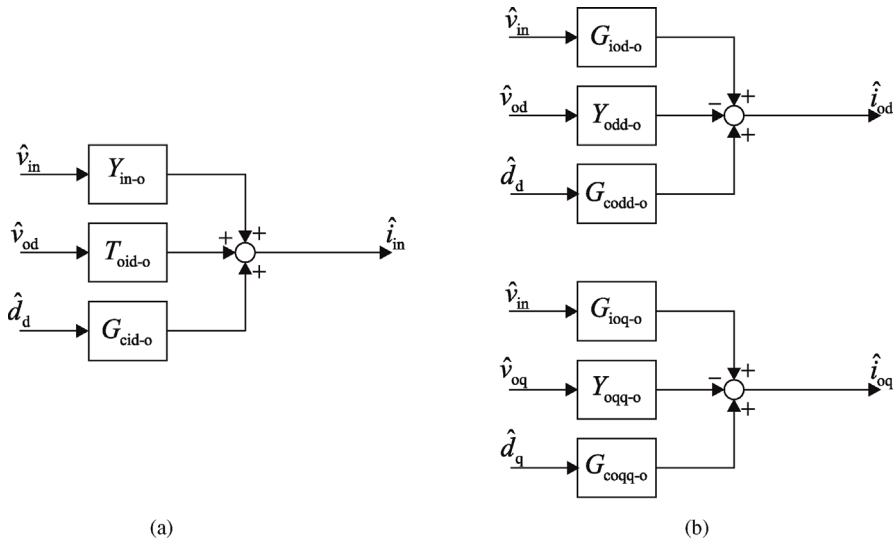


Figure 12.9 Simplified (a) input and (b) output dynamics at open loop.

The open-loop model can be verified by extracting the frequency responses from a circuit simulator or other similar software that can be used to implement a switching model of a three-phase inverter. The switching model was implemented using MATLAB/Simulink and the SimScape component library that can be used for simulating electrical systems. The frequency responses were extracted by using a Pseudo-Random Binary Sequences method (PRBS). Discussing the implementation of the measurement method is out of the scope of this book but the reader can familiarize with the method by going through Ref. [16].

Switching model of a three-phase voltage-fed inverter was implemented in MATLAB/Simulink where the PRBS method was used to extract the frequency responses that correspond to transfer functions solved earlier in Figure 12.5. The parameters of the simulation model are as given in Table 12.1. The angle θ that is used in the dq-transformations was generated inside the simulator by integrating the grid frequency ω_s . The grid voltage q-component steady-state value V_q was set to zero. Therefore, the inverter duty ratios are perfectly synchronized with the grid voltages since the dynamic model does not yet include the effect of grid synchronization (Figure 12.10).

Figure 12.11 shows the measured control-to-output-current transfer function G_{cod-o} that was obtained by making the small-signal perturbation to duty ratio

Table 12.1 Parameters of the voltage-fed inverter simulation model.

P_{in}	5 kW	V_{in}	700 V	V_{od}	325 V
I_{od}^*	10 A	I_{oq}^*	0 A	ω_s	$2\pi \cdot 50$ rad/s
L	5 mH	$r_L + r_{sw}$	100 m Ω	f_{sw}	20 kHz

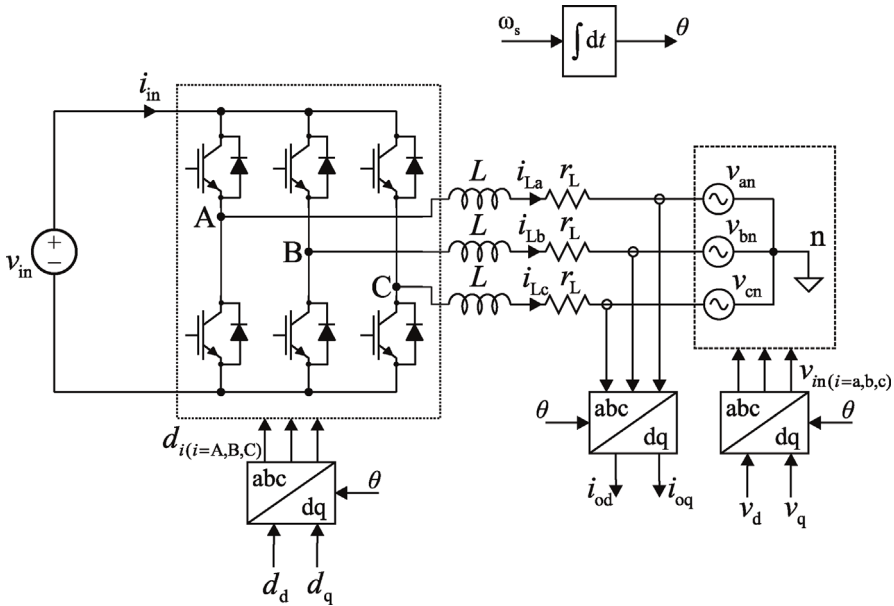


Figure 12.10 Principle of simulation model implemented using Simulink.

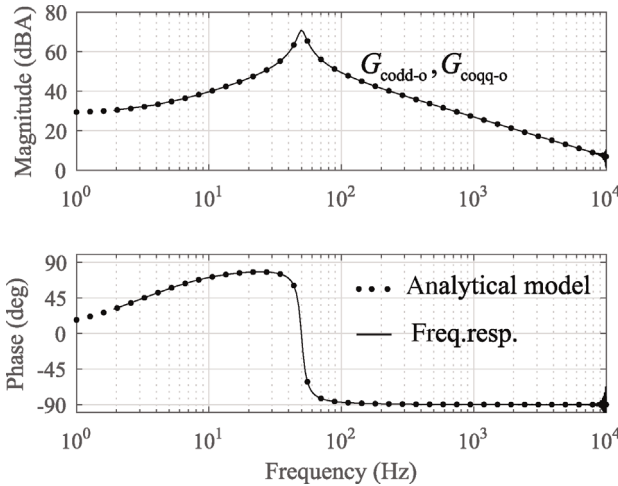


Figure 12.11 Output control dynamics of voltage-fed inverter ($G_{\text{codd-o}}$ and $G_{\text{coqq-o}}$).

d-component d_d and measuring the frequency response from the duty ratio d_d to output current d-component i_{Ld} . The control-to-output-current transfer function $G_{\text{coqq-o}}$ has identical shape and overlaps with $G_{\text{codd-o}}$ in the figure. Therefore, identical controller transfer functions can be used to regulate both currents, that is, d and q-component (Figure 12.12).

Figure 12.13 shows all of the four components of the inverter open-loop output admittance. Of course, the inverter is not intended for open-loop operation and

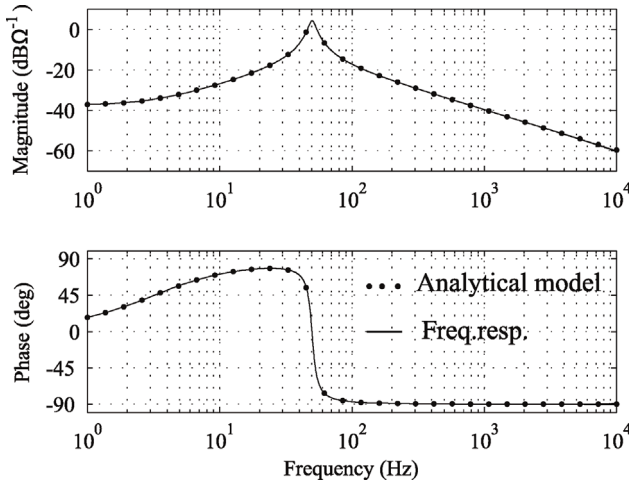


Figure 12.12 Open-loop input admittance Y_{in-o} of voltage-fed inverter.

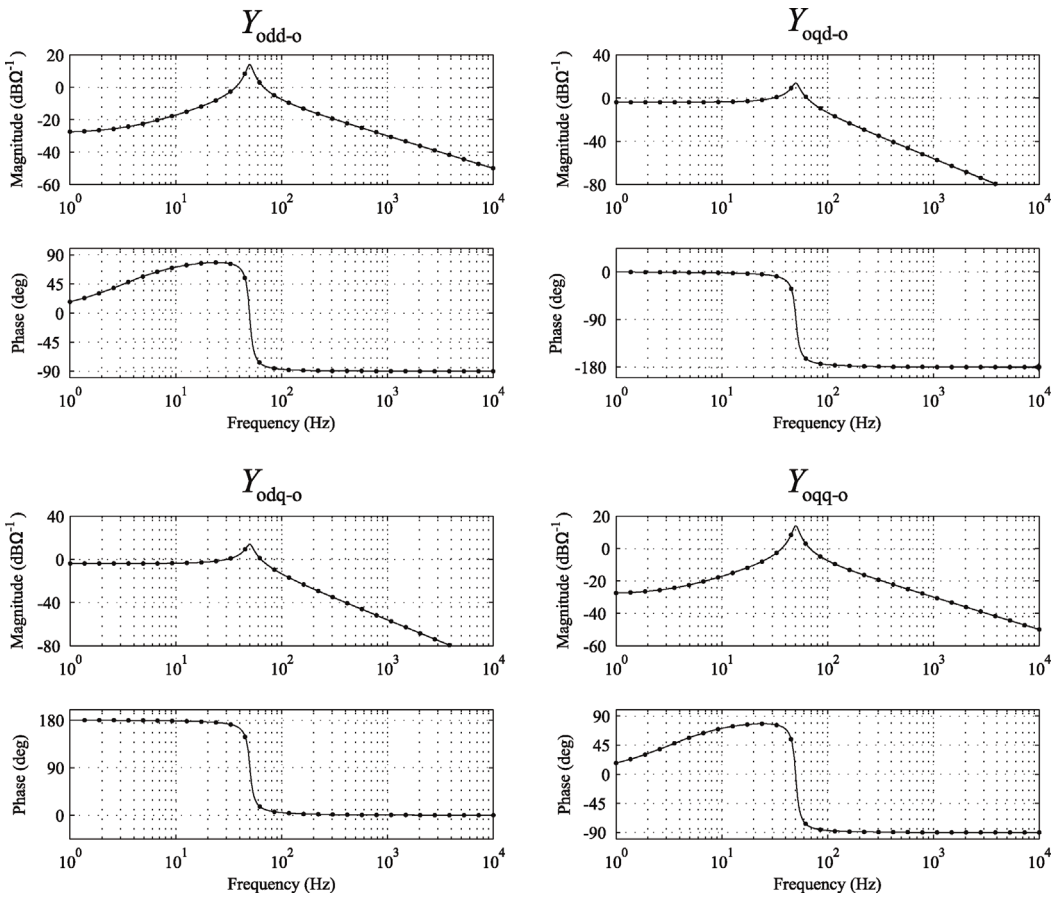


Figure 12.13 Components of the open-loop output admittance.

current control is usually applied to control the power factor. However, the extracted admittances prove that the small-signal is correct and, thus, can be utilized further to examine how different control functions affect the shape of inverter input and output admittances.

12.3 Dynamic Model of Current-Fed Inverter

Current-fed inverters are found in applications where the source is physically a current source such as a photovoltaic generator. Irradiance from the sun excites electrons inside the depletion layer of a pn-junction and creates a continuous DC current. Moreover, from the control theory point of view, the inverter has to be analyzed as a current-fed system when the DC link voltage is controlled. DC voltage control is mandatory for stable operation in grid-connected inverters [17,18] and to guarantee that the input voltage is high enough compared to the grid voltage amplitude to prevent over-modulation that leads to distorted grid currents.

12.3.1 Average Model of Current-Fed Inverter

Multilevel inverters, for example, three-level NPC, are commonly used in grid-connected photovoltaic applications. Moreover, the inverter usually utilizes an LCL or LC-type output filter. However, in this section the analysis is carried out for a two-level inverter with L-type output filter to simplify analysis. However, the same modeling methods can be applied to three-level inverters. Power stage of a current-fed inverter with L-type output filter is depicted in Figure 12.14. The power stage has an additional input capacitor that is required for interfacing the inverter with a current source [19]. Otherwise, there could be no control over the DC-side voltage. Moreover, the current drawn from the photovoltaic generator has to be continuous. There has to be a path for DC current during zero switching states of the inverter bridge, that is, when all upper switches or all lower switches are on simultaneously. Parasitic resistance of the capacitor is usually very small as several capacitors are connected in parallel and is neglected in the analysis.

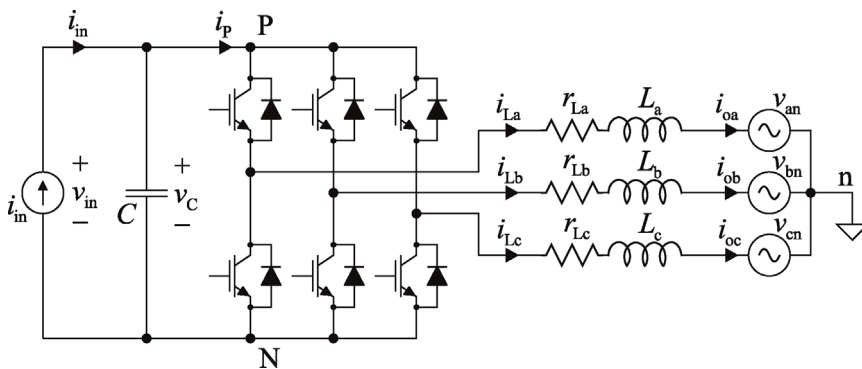


Figure 12.14 Three-phase current-fed inverter.

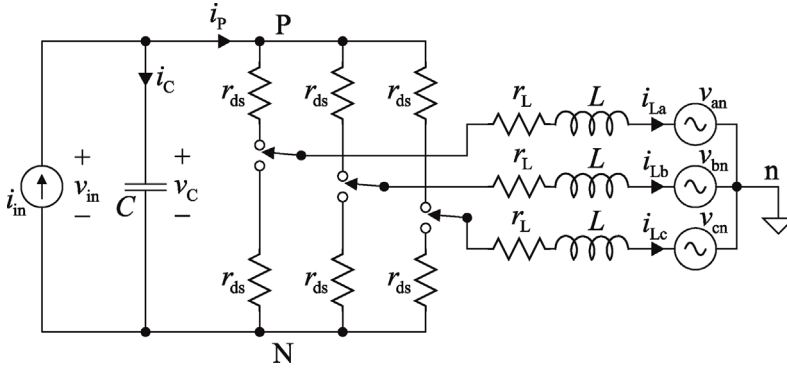


Figure 12.15 Equivalent switching circuit of a current-fed inverter.

The switch matrix can be approximated using the SPDT switches with parasitic resistive elements similarly as for the voltage-fed inverter. The equivalent switching circuit is as depicted in Figure 12.15.

The averaged inductor currents can be solved from Figure 12.15 by utilizing the common-mode voltage, and are the same as for the voltage-fed inverter. However, the input voltage v_{in} is defined as an output variable. Therefore, it has to be represented by using input and state variables for correct formulation of the state-space model. The input voltage equals the voltage over the DC capacitor, that is, $v_{in} = v_C$.

The average input voltage is substituted back in Eqs. (12.10) and (12.11) that allows representing the three-phase inductor currents in the dq-domain, as in Eqs. (12.31) and (12.32). The average state-space can be completed by solving the capacitor voltage derivative and noting that the inductor currents are the output currents.

$$\frac{d\langle i_{Ld} \rangle}{dt} = \frac{1}{L} (-r_{eq}\langle i_{Ld} \rangle + \omega_s L \langle i_{Lq} \rangle + d_d \langle v_C \rangle - \langle v_{od} \rangle). \quad (12.31)$$

$$\frac{d\langle i_{Lq} \rangle}{dt} = \frac{1}{L} (-\omega_s L \langle i_{Ld} \rangle - r_{eq}\langle i_{Lq} \rangle + d_q \langle v_C \rangle - \langle v_{oq} \rangle). \quad (12.32)$$

$$\frac{d\langle v_C \rangle}{dt} = \frac{1}{C} \left(\langle i_{in} \rangle - \frac{3}{2} (d_d \langle i_{Ld} \rangle + d_q \langle i_{Lq} \rangle) \right). \quad (12.33)$$

$$\langle v_{in} \rangle = \langle v_C \rangle. \quad (12.34)$$

$$\langle i_{od} \rangle = \langle i_{Ld} \rangle, \quad \langle i_{oq} \rangle = \langle i_{Lq} \rangle. \quad (12.35)$$

Average model can be depicted in the d–q domain as an equivalent circuit diagram as shown in Figure 12.16.

Steady-state operating point of current-fed inverter can be solved from the average model by setting derivative terms equal to zero and is shown in Eqs. (12.36)–(12.40). The most straightforward way of solving the steady state is to first solve duty ratio q-component D_q from the inductor current q-component from Eq. (12.32) that yields Eq. (12.40). Duty ratio q-component is substituted in Eq. (12.33) allowing the output current d-component to be solved as given in Eq. (12.39). Finally, the current d-component I_{Ld} is substituted in Eq. (12.31) yielding a second-order polynomial as a function of duty ratio

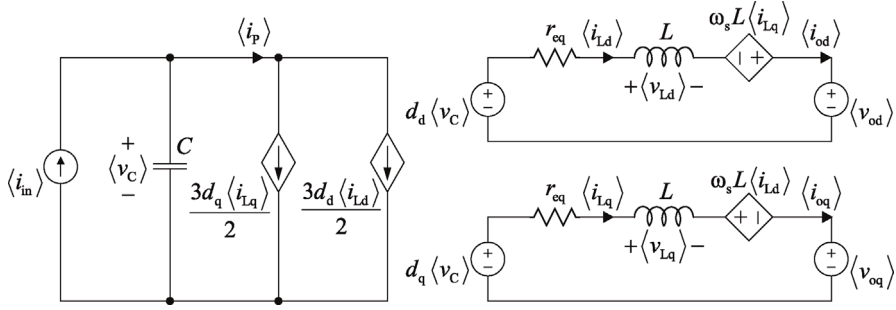


Figure 12.16 Equivalent linearized circuit diagram of current-fed inverter in the d-q domain.

d-component D_d as given in Eq. (12.38).

$$V_C = V_{in}. \quad (12.36)$$

$$I_{Lq} = I_{Lq}^*. \quad (12.37)$$

$$\begin{aligned} & V_{in}^2 D_d^2 + V_{in} (2\omega_s L I_{Lq}^* - V_{od}) D_d \\ & + \left((r_{eq}^2 + \omega_s^2 L^2) I_{Lq}^{*2} + r_{eq} \left[V_{oq} I_{Lq}^* - \frac{2}{3} V_{in} I_{in} \right] - \omega_s L V_{od} I_{Lq}^* \right) = 0. \end{aligned} \quad (12.38)$$

$$I_{Ld} = \frac{(2/3) V_{in} I_{in} - V_{oq} I_{Lq}^* - r_{eq} I_{Lq}^{*2}}{D_d V_{in} + \omega_s L I_{Lq}^*}. \quad (12.39)$$

$$D_q = \frac{V_{oq} + r_{eq} I_{Lq}^* + \omega_s L I_{Ld}}{V_{in}}. \quad (12.40)$$

It should be mentioned that steady-state value of output current q-component I_{Lq} does not depend on the processed power, that is, power from input PV source, and can be selected freely as long as the modulation index of the inverter does not exceed unity, that is, $\sqrt{D_d^2 + D_q^2} < 0.5$. Therefore, its steady-state value is equal to its reference value that is denoted by an asterisk. Current-fed inverters, such as photovoltaic inverters, often operate at unity power factor and, therefore, the reference of output current q-component I_{Lq}^* is set to zero. However, the reference can be nonzero to compensate reactive power drawn by the LCL-filter. Additionally, the inverter can be used to support grid voltage by injecting or drawing reactive power from the grid. The steady-state value of output voltage q-component V_{oq} is zero due to phase-locked loop as will be discussed later. Operation at unity power factor simplifies the steady-state solution because the effect of reactive current component I_{Lq} can be neglected. Steady-state operating point at unity power factor can be defined as in Eqs. (12.41)–(12.44).

$$I_{Lq} = I_{Lq}^* = 0 \text{ A}. \quad (12.41)$$

$$D_d = \frac{V_{od} + \sqrt{V_{od}^2 + (8/3) V_{in} I_{in} r_{eq}}}{2 V_{in}}. \quad (12.42)$$

$$I_{Ld} = \frac{2 I_{in}}{3 D_d}. \quad (12.43)$$

$$D_q = \frac{\omega_s L I_{Ld}}{V_{in}}. \quad (12.44)$$

12.3.2 Linearized Model and Open-Loop Dynamics

Average model of current-fed inverter is linearized at the predefined steady-state operating point yielding the linearized state-space as given in Eqs. (12.45)–(12.49).

$$\frac{d\hat{i}_{Ld}}{dt} = -\frac{r_{eq}}{L}\hat{i}_{Ld} + \omega_s\hat{i}_{Lq} + \frac{D_d}{C}\hat{v}_C - \frac{1}{L}\hat{v}_{od} + \frac{V_C}{L}\hat{d}_d. \quad (12.45)$$

$$\frac{d\hat{i}_{Lq}}{dt} = -\omega_s\hat{i}_{Ld} - \frac{r_{eq}}{L}\hat{i}_{Lq} + \frac{D_q}{L}\hat{v}_C - \frac{1}{L}\hat{v}_{oq} + \frac{V_C}{L}\hat{d}_q. \quad (12.46)$$

$$\frac{d\hat{v}_C}{dt} = -\frac{3D_d}{2C}\hat{i}_{Ld} - \frac{3D_q}{2C}\hat{i}_{Lq} + \frac{1}{C}\hat{i}_{in} - \frac{3I_{Ld}}{2C}\hat{d}_d - \frac{3I_{Lq}}{2C}\hat{d}_q. \quad (12.47)$$

$$\hat{v}_{in} = \hat{v}_C. \quad (12.48)$$

$$\hat{i}_{od} = \hat{i}_{Ld}, \quad \hat{i}_{oq} = \hat{i}_{Lq}. \quad (12.49)$$

Input, output, and state variables are collected in vectors \mathbf{u} , \mathbf{y} , and \mathbf{x} and constant terms are collected in matrices \mathbf{A} , \mathbf{B} , \mathbf{C} , and \mathbf{D} as shown in Eqs. (12.50) and (12.51).

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} = \overbrace{\begin{bmatrix} -\frac{r_{eq}}{L} & \omega_s & \frac{D_d}{L} \\ -\omega_s & -\frac{r_{eq}}{L} & \frac{D_q}{L} \\ -\frac{3D_d}{2C} & -\frac{3D_q}{2C} & 0 \end{bmatrix}}^{\mathbf{A}} \cdot \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} + \overbrace{\begin{bmatrix} 0 & -\frac{1}{L} & 0 & \frac{V_{in}}{L} & 0 \\ 0 & 0 & -\frac{1}{L} & 0 & \frac{V_{in}}{L} \\ \frac{1}{C} & 0 & 0 & -\frac{3I_{Ld}}{2C} & -\frac{3I_{Lq}}{2C} \end{bmatrix}}^{\mathbf{B}} \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}. \quad (12.50)$$

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} = \overbrace{\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}}^{\mathbf{C}} \cdot \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} + \overbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}}^{\mathbf{D}} \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.51)$$

Open-loop transfer functions can be solved symbolically or numerically in the frequency domain according to Eq. (12.27). The transfer functions are named after their physical interpretation as shown in Eq. (12.52).

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} = \overbrace{\begin{bmatrix} Z_{in-o} & T_{oid-o} & T_{oiq-o} & G_{cid-o} & G_{ciq-o} \\ G_{iod-o} & -Y_{odd-o} & -Y_{oqd-o} & G_{codd-o} & G_{coqd-o} \\ G_{ioq-o} & -Y_{odq-o} & -Y_{oqq-o} & G_{codq-o} & G_{coqq-o} \end{bmatrix}}^{\mathbf{G}_H} \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.52)$$

Transfer functions can be collected in submatrices as in Eq. (12.53) and finally the open-loop dynamics of current-fed inverter can be written by accounting the multivariable nature of the inverter as in Eq. (12.54).

$$\begin{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ 0 \end{bmatrix} \\ \begin{bmatrix} \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} Z_{in-o} & 0 \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} T_{oid-o} & T_{oiq-o} \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} G_{cid-o} & G_{ciq-o} \\ 0 & 0 \end{bmatrix} \\ \begin{bmatrix} G_{iod-o} & 0 \\ G_{ioq-o} & 0 \end{bmatrix} & -\begin{bmatrix} Y_{odd-o} & Y_{oqd-o} \\ Y_{odq-o} & Y_{oqq-o} \end{bmatrix} & \begin{bmatrix} G_{codd-o} & G_{coqd-o} \\ G_{codq-o} & G_{coqq-o} \end{bmatrix} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{in} \\ 0 \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.53)$$

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{\mathbf{i}}_o \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{in-o} & \mathbf{T}_{oi-o} & \mathbf{G}_{ci-o} \\ \mathbf{G}_{io-o} & -\mathbf{Y}_{o-o} & \mathbf{G}_{co-o} \end{bmatrix} \cdot \begin{bmatrix} \hat{\mathbf{i}}_{in} \\ \hat{\mathbf{v}}_o \\ \hat{\mathbf{d}} \end{bmatrix} \quad (12.54)$$

The linear three-port model of current-fed inverter can be depicted as in Figure 12.17. The cross-coupling admittances are modeled as controllable current sinks.

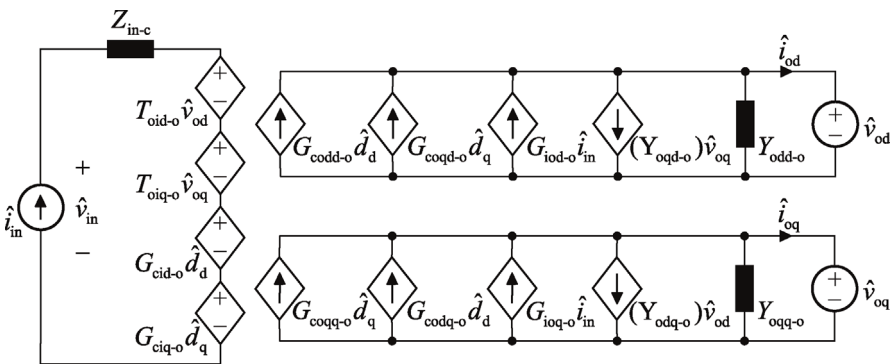


Figure 12.17 Linear three-port model of current-fed inverter.

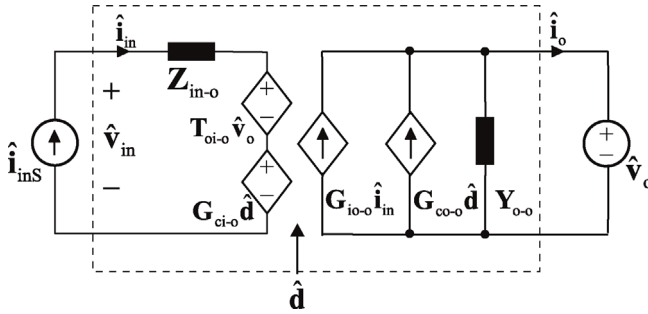


Figure 12.18 Two-port model of current-fed inverter.

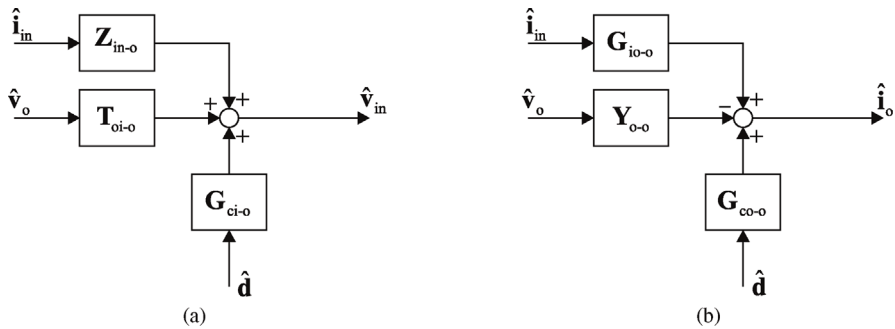


Figure 12.19 Full-order (a) input and (b) output dynamics of the current-fed inverter at open loop.

The linear two-port model of current-fed inverter is depicted in Figure 12.18. The output port is defined as a Norton's equivalent circuit similar to the voltage-fed inverter. However, the input is defined as the Thevenin's equivalent circuit since the source is of current type.

12.3.3 Control Block Diagrams of Current-Fed Inverter

Control block diagrams that represent the input and output dynamics of the inverter at open loop can be depicted as in Figure 12.19, where the transfer functions are equivalent to two-by-two matrices. Similarly, to voltage-fed inverter, a reduced-order model can be developed where the input dynamics are assumed to be dominated by the d-components and cross-coupling transfer functions are neglected. The reduced-order control block diagrams are as shown in Figure 12.20.

12.3.4 Verification of Open-Loop Model

The open-loop model was verified by extracting the frequency responses from a current-fed inverter that was implemented in MATLAB/Simulink using the SimScape library components, according to Figure 12.21. There is no grid synchronization algorithm in the model as it will be included later in

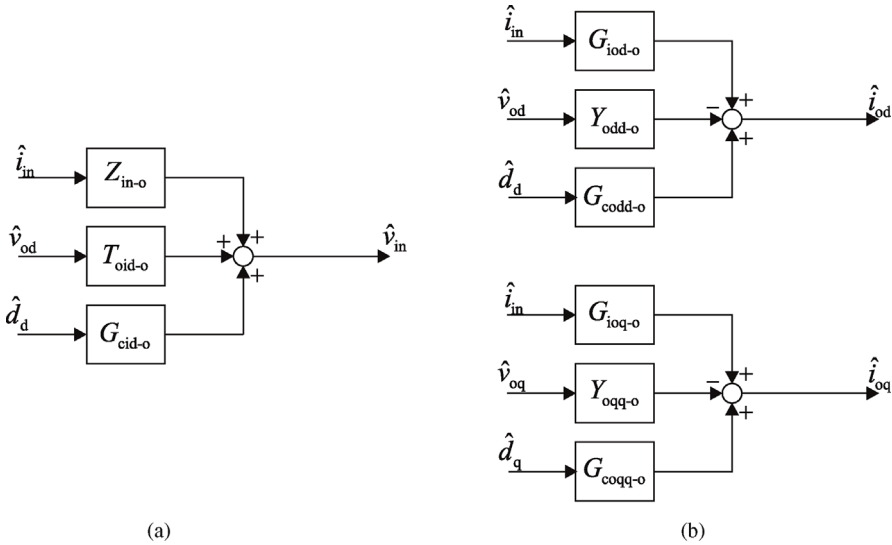


Figure 12.20 Reduced-order (a) input and (b) output dynamics at open loop.

Chapter 13. Therefore, the angle of the grid voltages θ is assumed to be a known variable.

The parameters of the current-fed inverter are collected in Table 12.2 that are the same as for one of the experimental setups introduced later in the book.

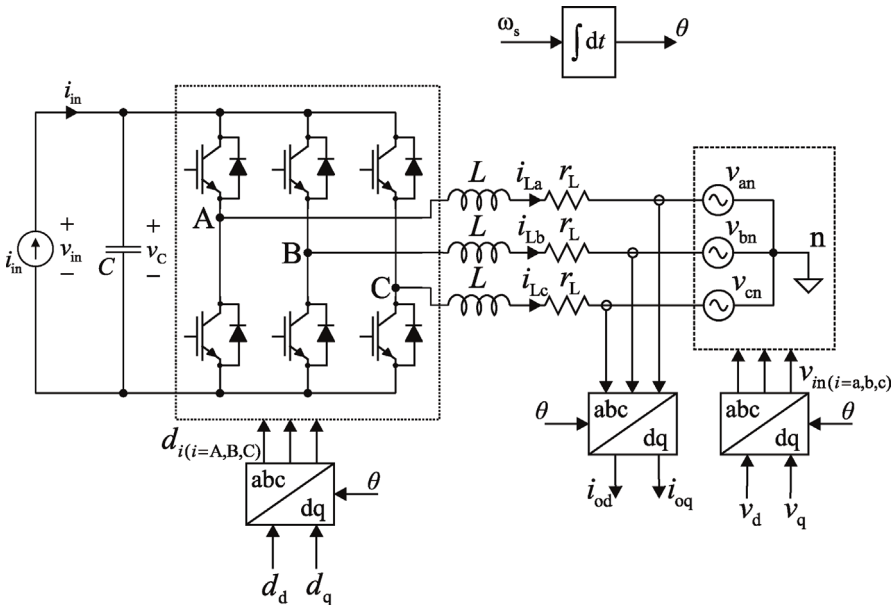


Figure 12.21 Principle of simulation model implemented using Simulink.

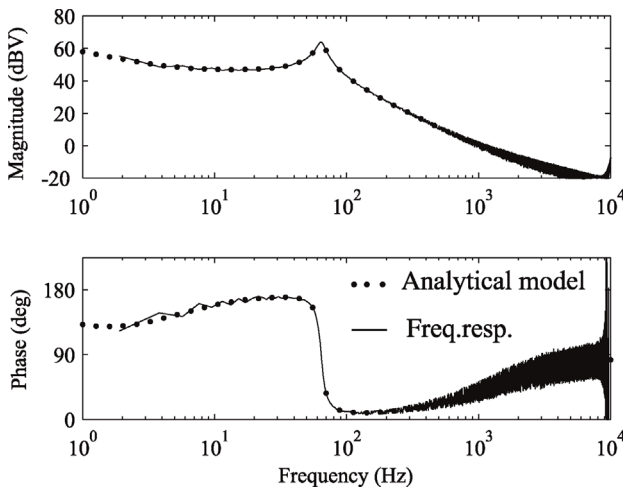
Table 12.2 Parameters of the current-fed inverter simulation model.

P_{in}	1.5 kW	V_{in}	571.9 V	V_{od}	$\sqrt{2} \cdot 120$ V
I_{in}	2.69 A	I_{oq}^*	0 A	ω_s	$2\pi \cdot 60$ rad/s
L	4 mH	$r_L + r_{sw}$	100 m Ω	f_{sw}	20 kHz
C	1.95 mF				

Figure 12.22 shows the control-to-input transfer function G_{cid-o} that is extracted from the switching model and the predicted frequency response given by the analytical model according to Eq. (12.52). The transfer function given by the small-signal model corresponds accurately with the extracted frequency response and, therefore, the model is correctly formulated.

Figure 12.23 shows the control-to-output-current transfer functions G_{codd-o} and G_{coqq-o} , which are later used in tuning of output current control loops. The two transfer functions have totally different low-frequency behavior when compared to voltage-fed inverter, where they had identical shape. This is due to a right-half plane zero in G_{codd-o} that will cause a control design constraint for the DC voltage control, as will be discussed in more detail in Chapter 13.

Figure 12.24 shows the input impedance at open loop. The impedance resembles a capacitor that is expected due to large DC capacitance of 1.95 mF. However, the impedance also includes a resonance that is caused by the AC output filter. Therefore, the input impedance should not be approximated using a simple capacitor impedance.

**Figure 12.22** Control-to-input-voltage transfer function G_{cid-o} .

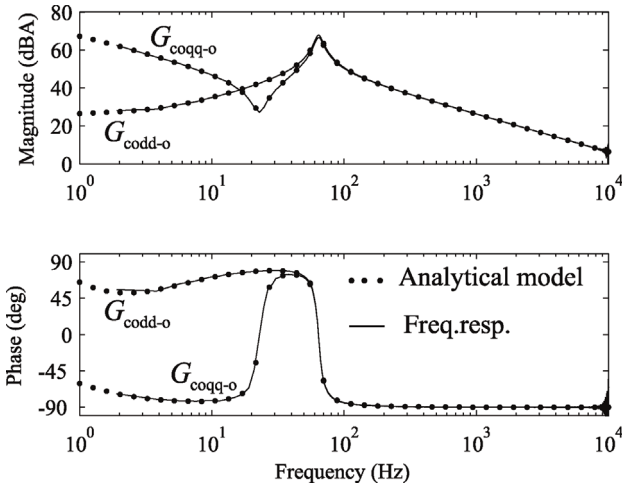


Figure 12.23 Control-to-output-current transfer functions ($G_{\text{codd-o}}$ and $G_{\text{coqq-o}}$).

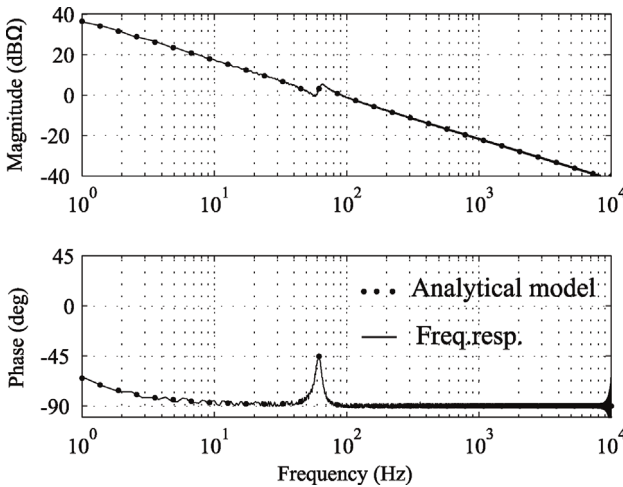


Figure 12.24 Input impedance $Z_{\text{in-o}}$ of current-fed inverter.

12.4 Source-Affected Dynamics of Current-Fed Inverter

Current-fed inverter is usually connected to a source that has finite output impedance, such as, photovoltaic generator [20–22], upstream DC–DC converter [23–25], EMI-filter, long DC cable [26], or a passive or an active rectifier in wind power applications. The source impedance may affect the inverter control system performance if it is not taken into account properly [18,27]. The inverter control system should be designed with the knowledge on impedance characteristics of the source as early as possible to prevent instabilities imposed by, for example, resonances in the source impedance. Measuring the source impedance is an easy task since one does only have to measure DC signals.

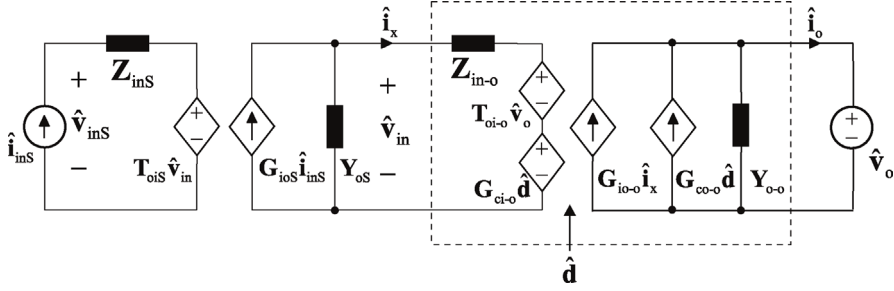


Figure 12.25 Linear network equivalent with nonideal source subsystem.

In this section, a method to include the effect of source impedance to inverter open-loop dynamics is presented. The method can be easily adapted to voltage-fed inverters or current-fed inverters with LCL-filter. The linear network equivalent of the current-fed inverter with nonideal source is depicted in Figure 12.25. The H -parameter model is used to represent the source dynamics to develop general equations for solving the source effect. The source can be considered as an input filter, upstream DC–DC converter, long DC cabling, a photovoltaic generator, and so on.

One is most often interested in how the source affects the control dynamics of the inverter or output admittance of the inverter. In most cases, the inverter controls its DC-side voltage. Therefore, the output variables of the system should be selected as the input voltage of inverter power stage \hat{v}_{in} and the grid current \hat{i}_o . Input variables are selected as the input current of the source system \hat{i}_{inS} , load voltage \hat{v}_o , and the duty ratio \hat{d} . Selecting the output variables in this manner produces transfer functions according to Eq. (12.55) where superscript “S” denotes that the corresponding transfer matrix is affected by dynamics of the source. Note that transfer function \mathbf{G}_{in-o}^S does not represent impedance, because the current and voltage are not defined at the same terminal.

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} \mathbf{G}_{in-o}^S & \mathbf{T}_{oi-o}^S & \mathbf{G}_{ci-o}^S \\ \mathbf{G}_{io-o}^S & -\mathbf{Y}_{o-o}^S & \mathbf{G}_{co-o}^S \end{bmatrix} \begin{bmatrix} \hat{i}_{inS} \\ \hat{v}_o \\ \hat{d} \end{bmatrix} \quad (12.55)$$

Current at the interface between the source system and the inverter \hat{i}_x can be given according to Figure 12.25 and Eq. (12.56).

$$\hat{i}_x = \mathbf{G}_{ioS} \hat{i}_{inS} - \mathbf{Y}_{oS} \hat{v}_{in}. \quad (12.56)$$

Source-affected dynamics can be formulated by substituting \hat{i}_x as the input current of the inverter power stage \hat{i}_{in} in Eq. (12.54). The input dynamics can be given using transfer matrices as in Eqs. (12.57)–(12.59).

$$\mathbf{G}_{in-o}^S = (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{Z}_{in-o} \mathbf{G}_{ioS}. \quad (12.57)$$

$$\mathbf{T}_{oi-o}^S = (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{T}_{oi-o}. \quad (12.58)$$

$$\mathbf{G}_{ci-o}^S = (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{G}_{ci-o}. \quad (12.59)$$

The source-affected output dynamics can be given as in Eqs. (12.60)–(12.62).

$$\mathbf{G}_{io-o}^S = \mathbf{G}_{io-o} \mathbf{G}_{ioS} - \mathbf{G}_{io-o} \mathbf{Y}_{oS} (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{Z}_{in-o} \mathbf{G}_{ioS}. \quad (12.60)$$

$$\mathbf{Y}_{o-o}^S = \mathbf{Y}_{o-o} + \mathbf{G}_{io-o} \mathbf{Y}_{oS} (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{T}_{oi-o}. \quad (12.61)$$

$$\mathbf{G}_{co-o}^S = \mathbf{G}_{co-o} - \mathbf{G}_{io-o} \mathbf{Y}_{oS} (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{G}_{ci-o}. \quad (12.62)$$

The output variables should be selected as $\hat{\mathbf{v}}_{inS}$ and $\hat{\mathbf{i}}_o$ if the inverter employs an input filter and controls the voltage preceding the input filter. Transfer functions can be defined as in Eq. (12.63) while the output dynamics are the same as given in Eqs. (12.60)–(12.62). Note that now the transfer function \mathbf{Z}_{in-o}^S represents impedance since current $\hat{\mathbf{i}}_{inS}$ and voltage $\hat{\mathbf{v}}_{inS}$ are defined at the same terminal.

$$\begin{bmatrix} \hat{\mathbf{v}}_{inS} \\ \hat{\mathbf{i}}_o \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{in}^S & \mathbf{T}_{oi-o}^S & \mathbf{G}_{ci-o}^S \\ \mathbf{G}_{io-o}^S & -\mathbf{Y}_{o-o}^S & \mathbf{G}_{co-o}^S \end{bmatrix} \begin{bmatrix} \hat{\mathbf{i}}_{inS} \\ \hat{\mathbf{v}}_o \\ \hat{\mathbf{d}} \end{bmatrix} \quad (12.63)$$

Voltage of the source can be given as

$$\hat{\mathbf{v}}_{inS} = \mathbf{Z}_{inS} \hat{\mathbf{i}}_{inS} + \mathbf{T}_{ois} \hat{\mathbf{v}}_{in}. \quad (12.64)$$

Input voltage of the inverter power stage $\hat{\mathbf{v}}_{in}$ can be given according to Eq. (12.55) as

$$\hat{\mathbf{v}}_{in} = \mathbf{Z}_{in}^S \hat{\mathbf{i}}_{inS} + \mathbf{T}_{oi-o}^S \hat{\mathbf{v}}_o + \mathbf{G}_{ci-o}^S \hat{\mathbf{d}}, \quad (12.65)$$

which is substituted in Eq. (12.64) to solve the source-affected input dynamics defined on the first row of the matrix in Eq. (12.63). Source-affected input dynamics can be given as in Eqs. (12.66)–(12.68).

$$\mathbf{Z}_{in-o}^S = \mathbf{Z}_{inS} + \mathbf{T}_{ois} (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{Z}_{in-o} \mathbf{G}_{ioS}. \quad (12.66)$$

$$\mathbf{T}_{oi-o}^S = \mathbf{T}_{ois} (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{T}_{oi-o}. \quad (12.67)$$

$$\mathbf{G}_{ci-o}^S = \mathbf{T}_{ois} (\mathbf{I} + \mathbf{Z}_{in-o} \mathbf{Y}_{oS})^{-1} \mathbf{G}_{ci-o}. \quad (12.68)$$

12.4.1 Source Effect: Photovoltaic Generator

A photovoltaic generator has nonlinear operating point-dependent terminal characteristics [28]. A typical IV -curve of a photovoltaic generator (PVG) is shown in Figure 12.26. The impedance of the PVG can be approximated by using the operating point-dependent dynamic resistance as in Eq. (12.69). The value of dynamic resistance equals the static resistance V_{PV}/I_{PV} at the maximum power point (MPP). In the constant current region (CC), the generator has current source-like properties and the dynamic resistance is large. In the constant voltage region (CV), the behavior is the opposite, that is, the value of dynamic resistance is small [20]. The operating point dependency of the value of dynamic resistance is summarized in Eq. (12.70).

$$r_{pv} = -\frac{dv_{pv}}{di_{pv}}. \quad (12.69)$$

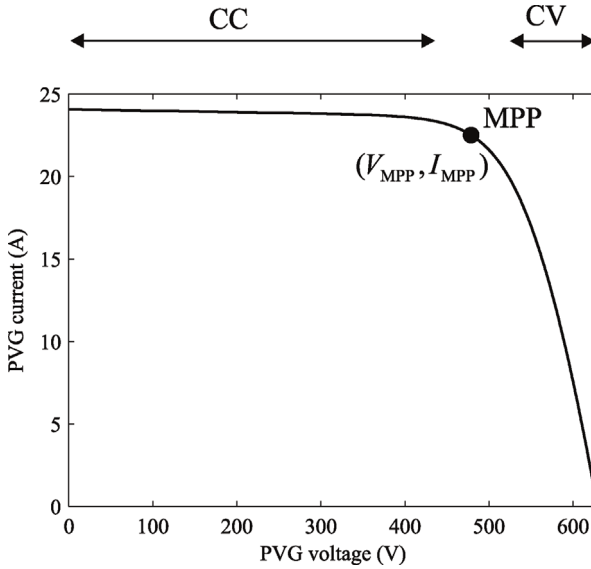


Figure 12.26 Typical I/V -curve.

$$r_{PV} = \begin{cases} r_{PV} > \frac{V_{PV}}{I_{PV}}, & V_{PV} < V_{MPP}, \\ r_{PV} = \frac{V_{PV}}{I_{PV}}, & V_{PV} = V_{MPP}, \\ r_{PV} < \frac{V_{PV}}{I_{PV}}, & V_{PV} > V_{MPP}, \end{cases} \quad (12.70)$$

The source-affected control-to-output dynamics can be evaluated by solving the source-affected control-to-output transfer function in Eq. (12.62). The output admittance of the PV generator is equal to the inverse of dynamic resistance r_{PV} and can be formulated in matrix form as

$$\mathbf{Y}_{oS} = \begin{bmatrix} (r_{PV})^{-1} & 0 \\ 0 & 0 \end{bmatrix} \quad (12.71)$$

As an example, the source-affected control-to-output dynamics can be given as

$$\begin{aligned} \mathbf{G}_{co-o}^S &= \begin{bmatrix} G_{codd-o}^S & G_{coqd-o}^S \\ G_{codq-o}^S & G_{coqq-o}^S \end{bmatrix} \\ &= \begin{bmatrix} G_{codd-o} - \frac{G_{iod-o} G_{cid-o} (r_{PV})^{-1}}{1 + Z_{in-o} (r_{PV})^{-1}} & G_{coqd-o} - \frac{G_{iod-o} G_{ciq-o} (r_{PV})^{-1}}{1 + Z_{in-o} (r_{PV})^{-1}} \\ G_{codq-o} - \frac{G_{ioq-o} G_{cid-o} (r_{PV})^{-1}}{1 + Z_{in-o} (r_{PV})^{-1}} & G_{coqq-o} - \frac{G_{ioq-o} G_{ciq-o} (r_{PV})^{-1}}{1 + Z_{in-o} (r_{PV})^{-1}} \end{bmatrix} \end{aligned} \quad (12.72)$$

Model of the PVG was implemented in Simulink. The derivation of the model is out of the scope of this book and the reader is urged to see the work carried out in Ref. [29] for further studies. The PVG is operated in two different operating

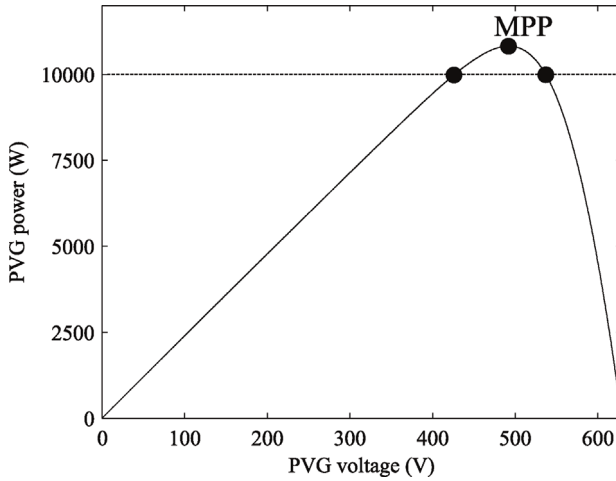


Figure 12.27 Limited-power operation at 10 kW.

Table 12.3 PVG operating points.

I_{PV}^{CCR}	23.43 A	I_{PV}^{CVR}	18.63 A
V_{PV}^{CCR}	426.7 V	V_{PV}^{CVR}	536.8 V
r_{PV}^{CCR}	116 Ω	r_{PV}^{CVR}	8.8 Ω

points: at voltage less than the MPP and higher than the MPP. The output power of PVG is 10 kW in both of these cases, as shown in Figure 12.27. Such operation is required when the output power of PVG is limited by a limit power-tracking algorithm [30]. The dynamic resistance of the PVG differs significantly between the operating points and, therefore, the source effect should be considered according to Eq. (12.72). The operating point values are given in Table 12.3.

Figure 12.28 shows the source-affected transfer function $G_{\text{codd-o}}^S$ solved using Eq. (12.72) in both operating points. The high-frequency part of the transfer function is not affected much by the dynamic resistance. However, the low-frequency phase experiences a phase shift of 180° between the operating points in the CC and CV regions. This indicates that a low-frequency zero must shift from the right-half to the left-half of a complex plane.

The effect of dynamic resistance on inverter control dynamics can be explained by solving the source-affected control-to-output-current transfer function $G_{\text{codd-o}}^S$ in symbolic form. The parasitic resistances associated with the inverter are neglected in order to simplify the result, that is, r_{eq} is set equal to zero. The transfer function can be given in symbolic form as in Eq. (12.73).

$$G_{\text{codd-o}(r_{\text{eq}}=0)}^S = \left[\frac{V_{\text{in}}}{L} s \left(s - \frac{1}{C} \left(\frac{I_{\text{in}}}{V_{\text{in}}} - \frac{1}{r_{\text{pv}}} \right) \right) \right] / \left[s^3 + \frac{1}{r_{\text{pv}}C} s^2 + \left[\frac{3}{2LC} (D_{\text{d}}^2 + D_{\text{q}}^2) + \omega_s^2 \right] s + \frac{\omega_s^2}{r_{\text{pv}}C} \right]. \quad (12.73)$$

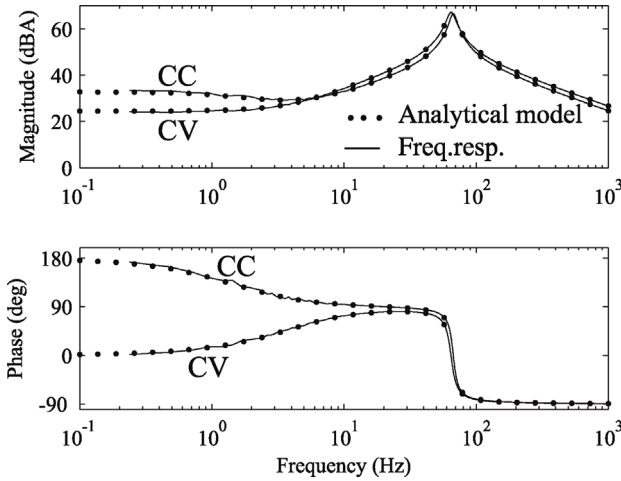


Figure 12.28 Source-affected control-to-output-current transfer function $G_{\text{codd-o}}^S$ in two different operating points of the PV generator.

The transfer function has a low-frequency zero given by Eq. (12.74) that depends on the value of dynamic resistance. The zero can have either a positive or negative value depending on the value of dynamic resistance.

$$\omega_{\text{zero}} = \frac{1}{C} \left(\frac{I_{\text{in}}}{V_{\text{in}}} - \frac{1}{r_{\text{pv}}} \right). \quad (12.74)$$

The zero is located in the right-half of the complex plane when ω_{zero} has a positive value, that is, when dynamic resistance is larger in value than the ratio of PVG voltage and current, as given in Eq. (12.75). In fact, this occurs only when the PVG operates at voltages lower than the MPP. The RHP-zero imposes a control design constraint for the DC voltage control, which is discussed in Chapter 13.

$$\omega_{\text{zero}} > 0, \quad \text{when} \quad r_{\text{pv}} > \frac{V_{\text{PV}}}{I_{\text{PV}}}. \quad (12.75)$$

The zero shifts to the left-half of the complex-plane when its value becomes negative, according to Eq. (12.76). Thus, the constraint related to control design disappears when the PVG is operated at voltages higher than the MPP.

$$\omega_{\text{zero}} < 0, \quad \text{when} \quad r_{\text{pv}} < \frac{V_{\text{PV}}}{I_{\text{PV}}}. \quad (12.76)$$

12.4.2 Source Effect: Experimental Validation

The source-affected small-signal model has been validated in the laboratory using a scaled-down prototype setup. The setup is depicted in Figure 12.29 where the PVS7000 PV emulator feeds a three-phase two-level inverter connected to a three-phase grid emulator. The grid and PV emulators are operated at lowered voltages. The parameters of the setup are summarized in Table 12.4.

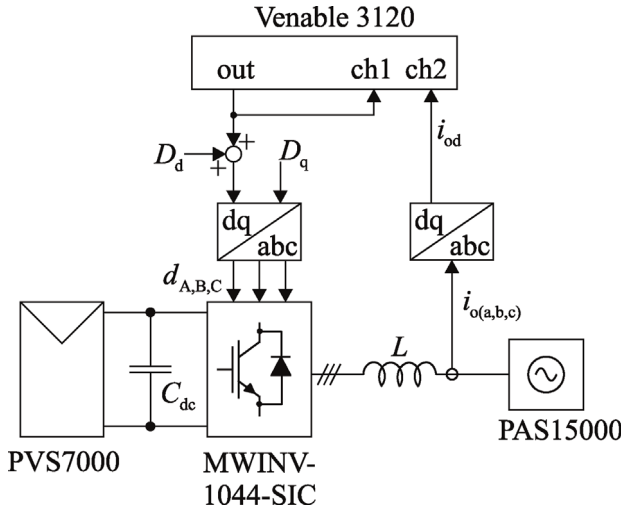


Figure 12.29 Setup for measuring open-loop transfer functions.

Table 12.4 Parameters of the low-voltage experimental laboratory setup.

P_{MPP}	180 W	V_{in}	30–84 V	V_{od}	10 V
C_{dc}	1.95 mF	I_{oq}^*	0 A	ω_s	$2\pi \cdot 60$ rad/s
L	5.2 mH	$r_L + r_{sw}$	100 m Ω	f_{sw}	20 kHz

In the initial setup, an isolation transformer is connected between the inverter and the grid emulator. However, for evaluating the source effect, the isolation transformer was removed from the setup that allowed excluding the load effect. As a tradeoff, the voltage levels needed to be lowered to mitigate common-mode currents that may cause damage to the expensive laboratory equipment such as the PV emulator. However, for the purpose of verifying the source-affected small-signal model, the setup is justifiable.

Photovoltaic generator has current source-like properties at voltages lower than the MPP, voltage source-like properties at voltages higher than the MPP, and behaves as a constant power source at the MPP. Output impedance of the PV generator depends on the operating point and environmental conditions and is continuously changing in value. The impedance is characterized by the dynamic resistance, internal capacitance of the generator, and possibly inductance and resistance from the DC cabling. Figure 12.30 depicts the IV -curve of the PV simulator that was used during validation of source-affected open-loop model. “CCR” refers to constant current region and “CVR” to constant voltage region and “MPP” marks the position of the maximum power point.

The output impedance of the PV emulator was measured by using a frequency response analyzer. The small-signal excitation was made in the d -component of the duty ratio, while the inverter was operated at open loop. Perturbing D_d affects the power drawn from the PV emulator terminals causing

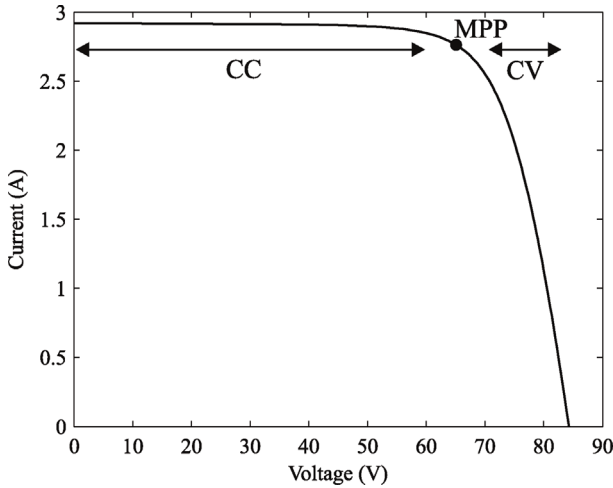


Figure 12.30 *IV*-curve of the photovoltaic emulator.

the current and voltage of the PV emulator to oscillate at the frequency of the perturbation. The measured input current and voltage of the PV emulator were fed to a frequency response analyzer (FRA) to measure the emulator output impedance.

The measured output impedance of the PV emulator is shown in Figure 12.31 in three different operating points, that is, in the CC and CV regions and at the MPP. In the CC region, the low-frequency magnitude of impedance corresponds to 330 ohms, at the MPP 24.6 ohms, and 4.2 ohms in the CV region. The dynamic behavior of the PV emulator corresponds to typical characteristics of a real PV generator [21].

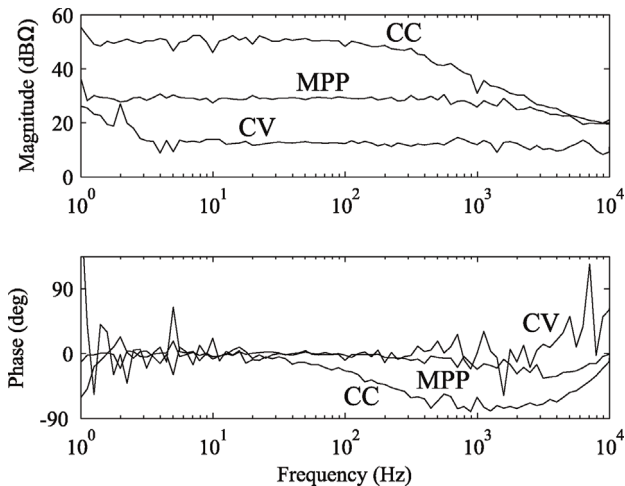


Figure 12.31 Measured output impedance of the photovoltaic emulator.

Table 12.5 Operating point and approximated dynamic resistance values.

	$V_{in}(V)$	$I_{in}(A)$	$r_{pv}(\Omega)$
CC	53.5	2.89	330
MPP	66.8	2.71	25
CV	79.6	1.21	4

Operating point values and the approximate values of dynamic resistances that are obtained from the measured impedances of Figure 12.31 are collected in Table 12.5. The values are substituted in Eq. (12.72) to obtain the predicted frequency response.

Figures 12.32 and 12.33 show the measured and predicted control-to-output-current transfer function G_{codd-o}^S in the CC and CV regions, respectively. The predicted transfer functions match well with the measured frequency responses. Moreover, the shifting of the low-frequency zero from RHP to LHP can be seen as a 180° phase-flip between the frequency responses measured in the CC and CV regions. In Figure 12.32, the low-frequency phase is close to 180° that implies the transfer function has a RHP-zero. However, the phase of the transfer function starts from zero when the PV emulator is operated in the CV region, which implies that the low-frequency zero has shifted to the LHP.

A current-fed inverter employs a RHP-zero in its control dynamics that has to be taken into account in the control design. However, a nonideal current source, such as a PV generator, can effectively hide these problematic dynamics in certain operating conditions. In the case of a photovoltaic inverter, the RHP-zero disappears in the CV region that may produce false conclusions on the stability

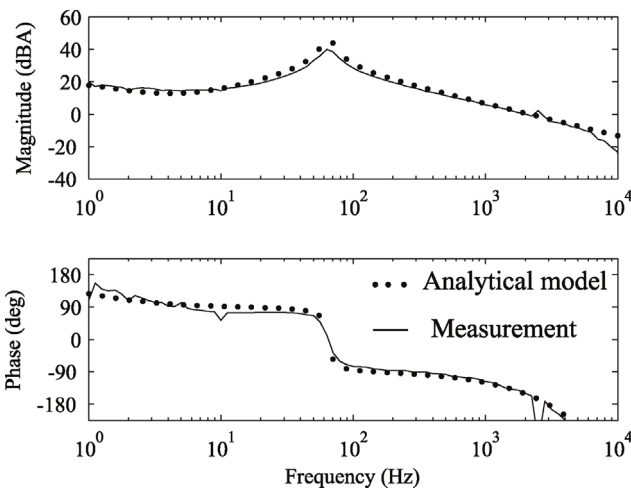


Figure 12.32 Measured and predicted control-to-output-current transfer function G_{codd-o}^S in CC region.

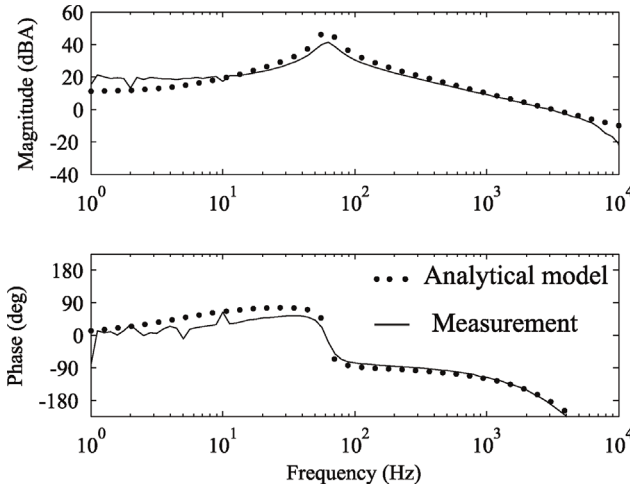


Figure 12.33 Measured and predicted control-to-output-current transfer function $G_{\text{codd-o}}^S$ in CV region.

of control system, for example, if the control system is tested only in the CV region and near the MPP.

12.5 Dynamic Model of Current-Fed Inverter with LCL-Filter

In this section, the dynamic model of a current-fed inverter with LCL-type output filter at open loop is developed. The power stage is as shown in Figure 12.34. Passive damping is realized by connecting resistors in series with the AC-side capacitors. Parasitic resistances of AC-side capacitors are neglected. However, their effect can be easily taken into account by increasing the value of damping resistance. Damping is required to stabilize the current control loops and to mitigate low impedance in inverter output impedance at the resonant frequency. The model is developed by assuming passive damping. However, the open-loop

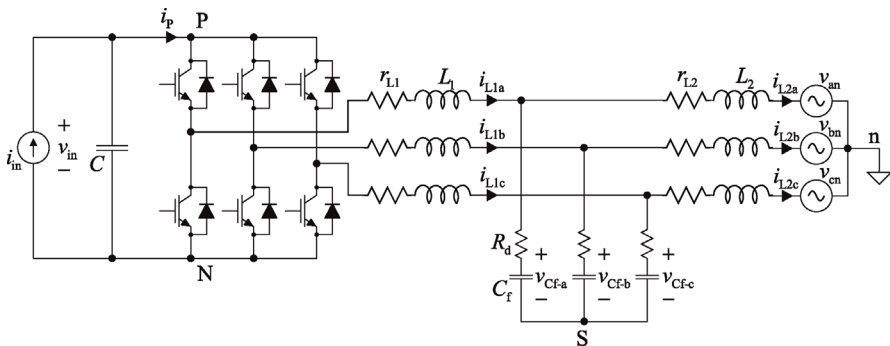


Figure 12.34 Current-fed inverter with LCL-type output filter.

model can be easily developed without passive damping by simply replacing the damping resistors with parasitic resistance of AC-capacitors or assuming ideal capacitors, that is, resistances are equal to zero. Therefore, the model can be used to evaluate dynamics of three-phase inverters with active damping [31–33].

12.5.1 Average Model of Current-Fed Inverter with LCL-Filter

Developing an average model for inverter with LCL filter follows the same principle as previously for inverters with L-type output filter. However, the amount of state variables (in the dq-domain) increases from four to ten as all capacitor voltages and inductor currents are selected as state variables. The averaged inductor currents and capacitor voltages for an arbitrary phase i can be defined as

$$\frac{d}{dt} \langle i_{L1i} \rangle = \frac{1}{L_1} [d_i \langle v_C \rangle - (r_{L1} + R_d) \langle i_{L1i} \rangle + R_d \langle i_{L2i} \rangle - \langle v_{Cf-i} \rangle - \langle v_{SN} \rangle], \quad (12.77)$$

$$\frac{d}{dt} \langle i_{L2i} \rangle = \frac{1}{L_2} [\langle v_{Cf-i} \rangle + R_d \langle i_{L1i} \rangle - (r_{L2} + R_d) \langle i_{L2i} \rangle - \langle v_{in} \rangle - \langle v_{NS} \rangle], \quad (12.78)$$

$$\frac{d}{dt} \langle v_{Cf-i} \rangle = \frac{1}{C_f} [\langle i_{L1i} \rangle - \langle i_{L2i} \rangle]. \quad (12.79)$$

Note that the voltage $\langle v_{in} \rangle$ refers to average voltage in phase i , not the input voltage. The average input capacitor voltage $\langle v_C \rangle$ is defined as

$$\frac{d}{dt} \langle v_C \rangle = \frac{1}{C} [\langle i_{in} \rangle - d_A \langle i_{L1a} \rangle - d_B \langle i_{L1b} \rangle - d_C \langle i_{L1c} \rangle]. \quad (12.80)$$

Output variables are defined as the DC-capacitor voltage and currents through grid-side inductors as $\langle v_{in} \rangle = \langle v_C \rangle$, $\langle i_{o-i} \rangle = \langle i_{L2i} \rangle$. The common-mode voltages $\langle v_{SN} \rangle$ and $\langle v_{NS} \rangle$ disappear in the d–q transformation and the average state-space can be given in the dq-domain as

$$\begin{aligned} \frac{d}{dt} \langle \mathbf{i}_{L1}^{dq} \rangle &= \frac{1}{L_1} \left[\mathbf{d}^{dq} \langle v_C \rangle - (r_{L1} + R_d + j\omega_s L_1) \langle \mathbf{i}_{L1}^{dq} \rangle + R_d \langle \mathbf{i}_{L2}^{dq} \rangle - \langle \mathbf{v}_{Cf}^{dq} \rangle \right], \\ \frac{d}{dt} \langle \mathbf{i}_{L2}^{dq} \rangle &= \frac{1}{L_2} \left[\langle \mathbf{v}_{Cf}^{dq} \rangle + R_d \langle \mathbf{i}_{L1}^{dq} \rangle - (r_{L2} + R_d + j\omega_s L_2) \langle \mathbf{i}_{L2}^{dq} \rangle - \langle \mathbf{v}_o^{dq} \rangle \right], \\ \frac{d}{dt} \langle \mathbf{v}_{Cf}^{dq} \rangle &= \frac{1}{C_f} \left[\langle \mathbf{i}_{L1}^{dq} \rangle - \langle \mathbf{i}_{L2}^{dq} \rangle - j\omega_s C_f \langle \mathbf{v}_{Cf}^{dq} \rangle \right]. \end{aligned} \quad (12.81)$$

The averaged state-space can be expressed in the dq-domain as in Eqs. (12.82)–(12.91).

$$\frac{d}{dt} \langle i_{L1d} \rangle = \frac{1}{L_1} [d_d \langle v_C \rangle - (r_{L1} + R_d) \langle i_{L1d} \rangle + \omega_s L_1 \langle i_{L1q} \rangle + R_d \langle i_{L2d} \rangle - \langle v_{Cfd} \rangle]. \quad (12.82)$$

$$\frac{d}{dt} \langle i_{L1q} \rangle = \frac{1}{L_1} [d_q \langle v_C \rangle - \omega_s L_1 \langle i_{L1d} \rangle - (r_{L1} + R_d) \langle i_{L1q} \rangle + R_d \langle i_{L2q} \rangle - \langle v_{Cfq} \rangle]. \quad (12.83)$$

$$\frac{d}{dt} \langle i_{L2d} \rangle = \frac{1}{L_2} [\langle v_{Cfd} \rangle + R_d \langle i_{L1d} \rangle - (r_{L2} + R_d) \langle i_{L2d} \rangle + \omega_s L_2 \langle i_{L2q} \rangle - \langle v_{od} \rangle]. \quad (12.84)$$

$$\frac{d}{dt} \langle i_{L2q} \rangle = \frac{1}{L_2} [\langle v_{Cfq} \rangle + R_d \langle i_{L1q} \rangle - (r_{L2} + R_d) \langle i_{L2q} \rangle - \omega_s L_2 \langle i_{L2d} \rangle - \langle v_{oq} \rangle]. \quad (12.85)$$

$$\frac{d}{dt} \langle v_{Cfd} \rangle = \frac{1}{C_f} [\langle i_{L1d} \rangle - \langle i_{L2d} \rangle + \omega_s C_f \langle v_{Cfq} \rangle]. \quad (12.86)$$

$$\frac{d}{dt} \langle v_{Cfq} \rangle = \frac{1}{C_f} [\langle i_{L1q} \rangle - \langle i_{L2q} \rangle - \omega_s C_f \langle v_{Cfd} \rangle]. \quad (12.87)$$

$$\frac{d}{dt} \langle v_C \rangle = \frac{1}{C} \left(\langle i_{in} \rangle - \frac{3}{2} (d_d \langle i_{L1d} \rangle + d_q \langle i_{L1q} \rangle) \right). \quad (12.88)$$

$$\langle v_{in} \rangle = \langle v_C \rangle. \quad (12.89)$$

$$\langle i_{od} \rangle = \langle i_{L2d} \rangle. \quad (12.90)$$

$$\langle i_{oq} \rangle = \langle i_{L2q} \rangle. \quad (12.91)$$

Steady-state operating point can be solved from the average model. However, obtaining the steady state symbolically is not useful since the formulas will be very complicated. Therefore, to obtain the numerical value of the steady-state operating point, computer program, such as MATLAB with Symbolic Toolbox, can be utilized. An example MATLAB code for solving the steady-state operating point numerically with parasitic resistances and with arbitrary grid current q-component I_{L2q} can be found in Appendix 12.A.

Deriving the exact steady-state operating point is quite laborious and requires a long series of substitutions. However, a good estimate for the real steady-state operating point can be derived easily for the case when all resistive losses are neglected and grid-voltage q-component V_{oq} is assumed zero. Moreover, the inverter is assumed to operate at unity power factor where the grid-side current q-component I_{L2q} is equal to zero. The symbolic steady-state operating point defined in Eqs. (12.92)–(12.96) gives values that are in most cases very close to the actual steady state.

$$D_d = \frac{(1 - (\omega_s)^2 L_1 C_f) V_{od}}{V_{in}}, \quad (12.92)$$

$$D_q = \frac{(1 - (1 - (\omega_s)^2 C_f L_2)(1 - (\omega_s)^2 C_f L_1))(2/3) I_{in}}{\omega_s C_f V_{od}}, \quad (12.93)$$

$$I_{L1d} = \frac{2}{3D_d} I_{in} - \frac{D_q}{D_d} \omega_s C_f V_{od}, \quad I_{L1q} = \omega_s C_f V_{od}, \quad (12.94)$$

$$I_{L2d} = \frac{1}{(1 - (\omega_s)^2 C_f L_2)} I_{L1d}, \quad I_{L2q} = 0, \quad (12.95)$$

$$V_{Cfd} = \frac{1}{\omega_s C_f} I_{L1q}, \quad V_{Cfq} = \frac{I_{L2d} - I_{L1d}}{\omega_s C_f}, \quad V_C = V_{in}. \quad (12.96)$$

12.5.2 Linearized State-Space and Open-Loop Dynamics

The linearized state-space can be developed by linearizing the average model in Eq. (12.91) in the predefined steady-state operating point. Inverter-side inductor currents are often controlled instead of grid-side currents. Therefore, it is useful to find out transfer functions from input variables to currents of the inverter-side inductors. The vector containing output variables is defined as

$$\mathbf{y} = [\hat{v}_{in} \quad \hat{i}_{L1d} \quad \hat{i}_{L1q} \quad \hat{i}_{L2d} \quad \hat{i}_{L2q}]^T. \quad (12.97)$$

Linearized state-space can be given as

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{L1d} \\ \hat{i}_{L1q} \\ \hat{i}_{L2d} \\ \hat{i}_{L2q} \\ \hat{v}_{Cfd} \\ \hat{v}_{Cfq} \\ \hat{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1} + R_d}{L_1} & \omega_s & \frac{R_d}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{D_d}{L_1} \\ -\omega_s & -\frac{r_{L1} + R_d}{L_1} & 0 & \frac{R_d}{L_1} & 0 & -\frac{1}{L_1} & \frac{D_q}{L_1} \\ \frac{R_d}{L_2} & 0 & -\frac{r_{L2} + R_d}{L_2} & \omega_s & \frac{1}{L_2} & 0 & 0 \\ 0 & \frac{R_d}{L_2} & -\omega_s & -\frac{r_{L2} + R_d}{L_2} & 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & \omega_s & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega_s & 0 & 0 \\ -\frac{3D_d}{2C} & -\frac{3D_q}{2C} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{L1d} \\ \hat{i}_{L1q} \\ \hat{i}_{L2d} \\ \hat{i}_{L2q} \\ \hat{v}_{Cfd} \\ \hat{v}_{Cfq} \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & \frac{V_{in}}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{V_{in}}{L_1} \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & -\frac{3I_{L1d}}{2C} & -\frac{3I_{L1q}}{2C} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix}. \quad (12.98)$$

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{L1d} \\ \hat{i}_{L1q} \\ \hat{i}_{L2d} \\ \hat{i}_{L2q} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{L1d} \\ \hat{i}_{L1q} \\ \hat{i}_{L2d} \\ \hat{i}_{L2q} \\ \hat{v}_{Cfd} \\ \hat{v}_{Cfq} \\ \hat{v}_C \end{bmatrix} + 0 \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.99)$$

Open-loop transfer functions can be obtained from the matrix \mathbf{G} according to (12.100) and written using transfer matrices as in (12.101).

$$\begin{bmatrix} \hat{v}_{in} \\ \hat{i}_{L1d} \\ \hat{i}_{L1q} \\ \hat{i}_{L2d} \\ \hat{i}_{L2q} \end{bmatrix} = \mathbf{G} \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} = \begin{bmatrix} Z_{in-o} & T_{oid-o} & T_{oiq-o} & G_{cid-o} & G_{ciq-o} \\ G_{iLd-o} & T_{oLdd-o} & T_{oLdq-o} & G_{cLdd-o} & G_{cLqd-o} \\ G_{iLq-o} & T_{oLdq-o} & T_{oLqq-o} & G_{cLdq-o} & G_{cLqq-o} \\ G_{iod-o} & -Y_{odd-o} & -Y_{oqd-o} & G_{codd-o} & G_{coqd-o} \\ G_{ioq-o} & -Y_{odq-o} & -Y_{oqq-o} & G_{codq-o} & G_{coqq-o} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (12.100)$$

$$\begin{bmatrix} \hat{\mathbf{v}}_{in} \\ \hat{\mathbf{i}}_{L1} \\ \hat{\mathbf{i}}_o \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{in-o} & \mathbf{T}_{oi-o} & \mathbf{G}_{ci-o} \\ \mathbf{G}_{iL-o} & \mathbf{T}_{oL-o} & \mathbf{G}_{cL-o} \\ \mathbf{G}_{io-o} & -\mathbf{Y}_{o-o} & \mathbf{G}_{co-o} \end{bmatrix} \cdot \begin{bmatrix} \hat{\mathbf{i}}_{in} \\ \hat{\mathbf{v}}_o \\ \hat{\mathbf{d}} \end{bmatrix} \quad (12.101)$$

12.6 Summary

Three-phase inverters are essential components in modern power systems where grid-connected renewable energy plays an important role. Inverters usually control various electrical parameters such as their output currents and input voltage. Moreover, a phase-locked loop is often used as a means to synchronize currents with grid voltages and to enable controllable power factor. The dynamic behavior of the inverter should be known to enable deterministic control design of the inverter control system.

This chapter presents the methods to obtain dynamic models of grid-connected three-phase inverters in the frequency domain. The dynamic models are derived at open loop with all control loops left open that allows evaluating the effects of nonideal source and load systems on the dynamic behavior of the inverter.

Appendix 12.A

MATLAB-code for solving the steady-state operating point of a current-fed inverter with LCL filter.

```

%operating point                                %passive components
w = 2*pi*60;                                    C1 = 1.95e-3;
Vod=sqrt(2)*120;                                L1=2.2e-3;
Voq = 0;                                         rL1=100e-3;
Vin =414.3;                                     Rd=1;
Iin = 6.577;                                    Cf=25e-6;
IL2q = 0;                                       L2=300e-6;
                                                rL2=65e-3;

syms Dd Dq Vcfd Vcfq IL1d IL2d IL1q %define unknowns as symbolic variables

eq1=Dd*Vin- (rL1+Rd) *IL1d+w*L1*IL1q+Rd*IL2d-Vcfd==0;
eq2=Dq*Vin-w*L1*IL1d- (rL1+Rd) *IL1q+Rd*IL2q-Vcfq==0;
eq3=Vcfd+Rd*IL1d- (rL2+Rd) *IL2d+w*L2*IL2q-Vod==0;
eq4=Vcfq+Rd*IL1q- (rL2+Rd) *IL2q-w*L2*IL2d-Voq==0;
eq5=IL1d-IL2d+w*Cf*Vcfq==0;
eq6=IL1q-IL2q-w*Cf*Vcfd==0;
eq7=Iin-3/(2*)*(Dd*IL1d+Dq*IL1q)==0;

Vcfd_1=solve(eq6,Vcfd);                        %solve for capacitor voltages
Vcfq_1=solve(eq5,Vcfq);
eq1=subs(eq1,[Vcfd Vcfq],[Vcfd_1 Vcfq_1]);     %substitute back in original
eq2=subs(eq2,[Vcfd Vcfq],[Vcfd_1 Vcfq_1]);
eq3=subs(eq3,[Vcfd Vcfq],[Vcfd_1 Vcfq_1]);
eq4=subs(eq4,[Vcfd Vcfq],[Vcfd_1 Vcfq_1]);
eq7=subs(eq7,[Vcfd Vcfq],[Vcfd_1 Vcfq_1]);

IL2d_mid = solve(eq3,IL2d);                    %intermediate result #1
eq1=subs(eq1,IL2d,IL2d_mid);                  %substitute back in original
eq2=subs(eq2,IL2d,IL2d_mid);
eq4=subs(eq4,IL2d,IL2d_mid);
eq7=subs(eq7,IL2d,IL2d_mid);

IL1q_mid=solve(eq4,IL1q);                    %intermediate result #2
eq1=subs(eq1,IL1q,IL1q_mid);                 %substitute back
eq2=subs(eq2,IL1q,IL1q_mid);
eq7=subs(eq7,IL1q,IL1q_mid);

Dq_solved=solve(eq2,Dq);                    %intermediate result #3
eq1=subs(eq1,Dq,Dq_solved);
eq7=subs(eq7,Dq,Dq_solved);

IL1d_solved=solve(eq7,IL1d);                %intermediate result #4
IL1d_solved=simplify(IL1d_solved(1,1));      %change to (2,1) if req.
eq1=subs(eq1,IL1d,IL1d_solved);            %substitute back

Dd_solved=double(solve(eq1,Dd));            %intermediate result #5
eq7 = subs (eq7,Dd,Dd_solved);

IL1d_solved=double(solve(eq7,IL1d));
IL1d_solved=IL1d_solved(1,1);
eq2=subs(eq2,IL1d,IL1d_solved);            %substitute back

Dq_solved=double(solve(eq2,Dq));            %Dq numerical value

eq4=subs(eq4,IL1d_solved);
IL1q_solved=double(solve(eq4,IL1q));        %IL1q numerical value
eq3=subs(eq3,[IL1d IL1q],[IL1d_solved IL1q_solved]); %substitute back

```



```

IL2d_solved=double(solve(eq3,IL2d));           %IL2d numerical value
eq6=subs(eq6,IL1q,IL1q_solved);               %substitute back
VCfd_solved=double(solve(eq6,VCfd));          %VCfd numerical value
eq5=subs(eq5,[IL1d IL2d],[IL1d_solved IL2d_solved]); %substitute back
VCfq_solved=double(solve(eq5,VCfq));          %VCfq numerical value
Dd = double(Dd_solved);                       %final numerical values to be used
Dq = double(Dq_solved);                       %to characterize open-loop transfer
IL1d=double(IL1d_solved);                     %functions
IL1q=double(IL1q_solved);
IL2d=double(IL2d_solved);
VCfd=double(VCfd_solved);
VCfq=double(VCfq_solved);

```

References

- 1 Nousiainen, L., Puukko, J., and Suntio, T. (2011) Simple VSI-based single-phase inverter: dynamical effect of photovoltaic generator and multiplier-based grid synchronization. IET Conference on Renewable Power Generation (RPG 2011), pp. 51–51.
- 2 Puukko, J. and Suntio, T. (2012) Modelling the effect of non-ideal load in three-phase converter dynamics. *Electron. Lett.*, **48** (7), 402.
- 3 Cvetkovic, I., Jaksic, M., Boroyevich, D., Mattavelli, P., Lee, F.C., Shen, Z., Ahmed, S., and Dong, D. (2011) Un-terminated, low-frequency terminal-behavioral d–q model of three-phase converters. IEEE Energy Conversion Congress and Exposition, 791–798.
- 4 Harnefors, L. (2007) Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices. *IEEE Trans. Ind. Electron.*, **54** (4), 2239–2248.
- 5 Yazdani, A., Di Fazio, A.R., Ghoddami, H., Russo, M., Kazerani, M., Jatskevich, J., Strunz, K., Leva, S., and Martinez, J.A. (2011) Modeling guidelines and a benchmark for power system simulation studies of three-phase single-stage photovoltaic systems. *IEEE Trans. Power Deliv.*, **26** (2), 1247–1264.
- 6 Bordonau, J., Cosan, M., Borojevic, D., Mao, H., and Lee, F.C. (1997) A state-space model for the comprehensive dynamic analysis of three-level voltage-source inverters. PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970–71. Power Processing and Electronic Specialists Conference 1972, 2, pp. 942–948.
- 7 Alepuz, S., Busquets-Monge, S., Bordonau, J., Gago, J., Gonzalez, D., and Balcells, J. (2006) Interfacing renewable energy sources to the utility grid using a three-level inverter. *IEEE Trans. Ind. Electron.*, **53** (5), 1504–1511.
- 8 Chatzinikolaou, E. and Rogers, D.J. (2016) A comparison of grid-connected battery energy storage system designs. *IEEE Trans. Power Electron.*, **32**, 1–1.
- 9 Jain, S. and Agarwal, V. (2007) A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking. *IEEE Trans. Power Electron.*, **22** (5), 1928–1940.

- 10 Figueres, E., Garcerá, G., Sandía, J., González-espín, F., and Rubio, J.C. (2009) Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter. *IEEE Trans. Ind. Electron.*, **56** (3), 706–717.
- 11 Dowell, P.L.L. (1966) Effects of eddy currents in transformer windings. *Proc. Inst. Electr. Electron. Eng.*, **113** (8), 1387.
- 12 Middlebrook, R. and Cuk, S. (1976) A general unified approach to modelling switching-converter power stages. 1970 IEEE Power Electronics Specialists Conference, **21** (1), pp. 18–34.
- 13 Mao, H., Boroyevich, D., and Lee, F.C. (1998) Novel reduced-order small-signal model of a three-phase PWM rectifier and its application in control design and system analysis. *IEEE Trans. Power Electron.*, **13** (3), 511–521.
- 14 Messo, T., Jokipii, J., Makinen, A., and Suntio, T. (2013) Modeling the grid synchronization induced negative-resistor-like behavior in the output impedance of a three-phase photovoltaic inverter. 2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 1–7.
- 15 Tse, C.K. (1998) *Linear Circuit Analysis*, Addison Wesley Longman, Harlow, England.
- 16 Roinila, T., Vilkkö, M., and Suntio, T. (2010) Frequency-response measurement of switched-mode power supplies in the presence of nonlinear distortions. *IEEE Trans. Power Electron.*, **25** (8), 2179–2187.
- 17 Espinoza, J.R., Joos, G., Perez, M., and Moran, T.L.A. (2000) Stability issues in three-phase PWM current/voltage source rectifiers in the regeneration mode. ISIE'2000. Proceedings of the 2000 IEEE International Symposium on Industrial Electronics (Cat. No.00TH8543), 2, pp. 453–458.
- 18 Messo, T., Jokipii, J., Puukko, J., and Suntio, T. (2014) Determining the value of DC-link capacitance to ensure stable operation of a three-phase photovoltaic inverter. *IEEE Trans. Power Electron.*, **29** (2), 665–673.
- 19 Capel, L., Marpinard, J.C., Valentin, M., and Jalade, J. (1983) Current fed and voltage fed switching DC/DC converters – steady state and dynamic models their applications in space technology. Telecommunication Energy Conference 1983. INTELEC '83, pp. 421–430.
- 20 Maki, A., Valkealahti, S., and Suntio, T. (2010) Dynamic terminal characteristics of a photovoltaic generator. Proceedings of 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010, (1), pp. 76–80.
- 21 Nousiainen, L., Puukko, J., Mäki, A., Messo, T., Huusari, J., Jokipii, J., Viinamäki, J., Lobera, D.T., Valkealahti, S., and Suntio, T. (2013) Photovoltaic generator as an input source for power electronic converters. *IEEE Trans. Power Electron.*, **28** (6), 3028–3038.
- 22 Puukko, J. and Suntio, T. (2012) Dynamic properties of a voltage source inverter-based three-phase inverter in photovoltaic application. *IET Renew. Power Gener.*, **6** (6), 381–391.
- 23 Ho, C.N.-M., Breuninger, H., Pettersson, S., Escobar, G., Serpa, L.A., and Coccia, A. (2012) Practical design and implementation procedure of an interleaved boost converter using SiC diodes for PV applications. *IEEE Trans. Power Electron.*, **27** (6), 2835–2845.

- 24 Messo, T., Puukko, J., and Suntio, T. (2012) Effect of MPP-tracking DC/DC converter on VSI-based photovoltaic inverter dynamics. 6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012), pp. D44–D44.
- 25 Xiao, W., Ozog, N., and Dunford, W.G. (2007) Topology study of photovoltaic interface for maximum power point tracking. *IEEE Trans. Ind. Electron.*, **54** (3), 1696–1704.
- 26 Zhang, S., Jiang, S., Lu, X., Ge, B., and Peng, F.Z. (2014) Resonance issues and damping techniques for grid-connected inverters with long transmission cable. *IEEE Trans. Power Electron.*, **29** (1), 110–120.
- 27 Puukko, J., Messo, T., and Suntio, T. (2011) Effect of photovoltaic generator on a typical VSI-based three-phase grid-connected photovoltaic inverter dynamics. IET Conference on Renewable Power Generation (RPG 2011), pp. 72–72.
- 28 Liu, Shengyi and Dougal, R.A. (2002) Dynamic multiphysics model for solar array. *IEEE Trans. Energy Convers.*, **17** (2), 285–294.
- 29 Villalva, M.G., Gazoli, J.R., and Filho, E.R. (2009) Comprehensive approach to modeling and simulation of photovoltaic arrays. *IEEE Trans. Power Electron.*, **24** (5), 1198–1208.
- 30 Wang, H., Blaabjerg, F., Simões, M.G., and Yang, Y. (2016) Power control flexibilities for grid-connected multi-functional photovoltaic inverters. *IET Renew. Power Gener.*, **10** (4), 504–513.
- 31 Aapro, A., Messo, T., and Suntio, T. (2015) An accurate small-signal model of a three-phase VSI-based photovoltaic inverter with LCL-filter. 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), pp. 2267–2274.
- 32 Aapro, A., Messo, T., and Suntio, T. (2015) Effect of active damping on the output impedance of PV inverter. 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), pp. 1–8.
- 33 Aapro, A., Messo, T., and Suntio, T. (2016) Effect of single-current-feedback active damping on the output impedance of grid-connected inverter. 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), pp. 1–10.

13

Control Design of Grid-Connected Three-Phase Inverters

13.1 Introduction

After studying this chapter, the reader should be familiar with the most common inverter control functions. Moreover, the readers should be able to apply the dynamic model and loop-shaping technique to design stable control loops. In this chapter, the most fundamental control functions of a three-phase grid-connected inverter are included in the dynamic model such as the AC current control, phase-locked-loop, and DC voltage control. The concepts of decoupling gains and proportional grid voltage feedforward are introduced. Moreover, the principle of tuning the control loops by using loop-shaping technique is discussed and demonstrated by several simulation and experimental examples.

The dynamic model of the SRF-PLL is developed and included in the closed-loop model of three-phase inverters. The control design of SRF-PLL is discussed and demonstrated by design examples from a simulator and a laboratory prototype. The dynamic models of voltage- and current-fed inverters are used to tune stable AC current control for voltage-fed inverter and cascaded control for current-fed inverter. Selection of decoupling gains of the current controller and proportional feedforward gains are discussed.

13.2 Synchronous Reference Frame Phase-Locked-Loop

Three-phase converter transforms DC electricity into three-phase AC when they operate in inverter mode and from AC to DC when they operate in rectifier mode. The produced three-phase AC current needs to have the same fundamental frequency as the AC system in which the inverter is connected to. Power systems are usually designed to operate at 50 or 60 Hz. Phase shift between AC currents and voltages determines how much real and reactive power is transferred. Therefore, the converter must have a method to determine the frequency and phase angle of the AC voltages to synchronize its AC-side currents with the grid voltages. However, there are numerous applications, such as ship and airplane power systems, that may have fundamental frequencies of several hundreds of hertz. Selecting the control parameters for grid synchronization depends on the

application. Therefore, there is no general guideline to tune the grid synchronization algorithm that applies for every application.

A vast amount of different grid synchronization methods have been developed. The simplest methods include zero-crossing detection algorithms that try to identify the zero-crossing instant of the AC voltage signal [1]. The frequency of the AC system can be calculated from the amount of time that separates two zero-crossings. The method based on zero-crossing is easy to implement but has several drawbacks. Detecting the zero-crossing is not easy if the AC voltage is distorted or there is noise in the measurement circuits. Moreover, the bandwidth of the synchronization control is limited below the fundamental frequency of the AC system since the zero-crossing algorithm has to wait half of the fundamental period for the zero-crossing before taking any action.

Phase-locked-loops have been conventionally used in signal processing and telecommunication applications [2]. The phase angle that is required for the control system (Park's transformation) can be generated as a repeating ramp that increases from zero to 2π radians and is synchronized with the AC voltage as illustrated in Figure 13.1. Grid synchronization methods for three-phase converters are based on the *synchronous reference frame phase-locked loop* or, in short, the *SRF-PLL* [3]. The method is based on the *amplitude-invariant* Park's transformation that is used to sense the magnitude of grid voltage d and q-components. The control block diagram of SRF-PLL is depicted in Figure 13.2. The SRF-PLL is composed of Park's transformation, PI controller, and an integrator. The PI-controller is often referred to as a loop-filter due to the fact that its parameters affect how much measurement noise and distortion due to phase unbalance affect the output angle of the PLL.

The SRF-PLL is a controlled process that adjusts the angle θ' to have a value that eliminates the error signal e . The sensed q-component of the grid voltage is effectively controlled to zero by the PI controller. The output of the controller can be interpreted as a frequency that is transformed into an angle by using an integrator. The angle is fed back to the Park's transformation, which accounts for the name *phase-locked-loop*. The constant term ω_{ff} should be added as the initial output of the PI-controller to speed up the start transient, that is, to avoid long settling time at start-up. Reference of the sensed q-component v_q^* is not usually drawn in control diagrams since it is zero. However, it is included here to underline the operating principle of SRF-PLL as a controlled process.

Alternatively, the control diagram can be depicted as in Figure 13.3 by neglecting the reference value v_q^* (since it is zero). In this case there is no

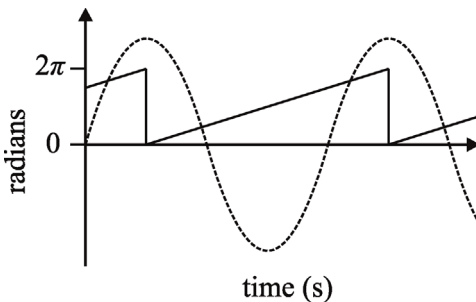


Figure 13.1 Synchronized angle of a phase-locked loop.

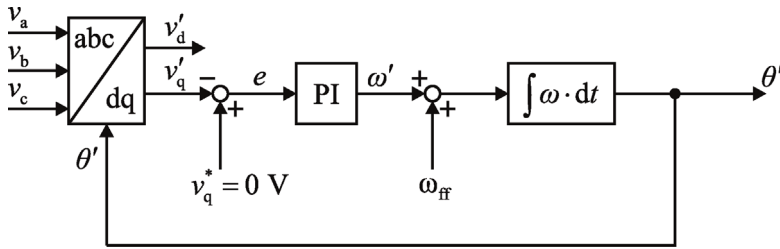


Figure 13.2 Control diagram of synchronous reference frame phase-locked loop.

need for the summation block that calculates the error signal and, thus, it can be removed. It should be noted that the PLL of Figure 13.2 requires inverted control signal to be used, whereas the PLL in Figure 13.3 does not. However, the purpose of this subchapter is to emphasize the PLL as a controlled process. Therefore, the control diagram in Figure 13.2 will be analyzed instead.

The SRF-PLL synchronizes its internal frequency and phase angle with the AC system by controlling the sensed grid voltage q-component to zero. By the definition of Park's transformation, the angle is equal to zero at the peak of the voltage at phase A, when balanced and symmetrical AC voltages are assumed. The angle increases from zero to 2π in radians at the rate of ω' , as illustrated in Figure 13.1. Such waveform can be used to verify that the PLL is synchronized to grid voltages before the inverter is turned on.

The SRF-PLL is not the optimal choice for grids that experience unbalance between phase voltages or has distorted voltage waveforms. Sudden dips and glitches in grid voltages can be amplified by the control loop that distorts the generated AC currents. Therefore, bandwidth of the SRF-PLL is usually on the order of few tens of hertz [3]. Moreover, bandwidth of the SRF-PLL should be limited to minimize risk of impedance-based instability [4–6], as will be discussed in Chapter 16.

More sophisticated synchronization methods have been developed which can mitigate the effect of unbalance, such as the *synchronous double reference frame PLL* and *dual second-order generalized integrator PLL* [7,8]. The principle is to mitigate the effect of unbalance by synchronizing the PLL to the positive sequence component of grid voltage space vector. However, all the abovementioned methods are modifications of the basic SRF-PLL. It is important to understand

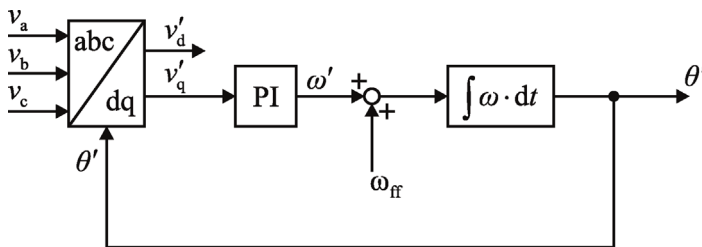


Figure 13.3 Simplified control diagram of SRF-PLL.

the operating principle and the dynamic effect of SRF-PLL, since it allows modeling and designing of the advanced synchronization methods.

13.2.1 Linearized Model of SRF-PLL

At steady state, the PLL frequency is equal to the fundamental frequency of the grid voltages, and the angle difference between sensed and the actual grid voltage space-vector is zero (since grid voltage q-component is zero). However, the angle experiences small deviation around the steady-state operating point when considering its small-signal behavior, because PLL's bandwidth is not infinite. Figure 13.4 shows the space-vector of grid voltage \mathbf{v}_g that is defined parallel with the real-axis of the *ideal grid reference frame*. The sensed grid voltage space-vector \mathbf{v}'_g leads the grid voltage space-vector by a small angle difference θ_Δ . Therefore, the reference frame in which controllers are implemented leads the ideal grid reference frame by the same angle θ_Δ . Real and imaginary axes of the *control system reference frame* are denoted using Re' and Im' , respectively. It should be noted that at steady state the reference frames have no phase shift in relation to each other. However, to understand the principle of linearizing the PLL, it is important to understand that in small-signal sense the phase difference can have a nonzero value.

Three-phase variables that are transformed using Park's transformation are affected by the dynamics of the PLL. The space vector \mathbf{x}^s in Figure 13.4 can be projected along the real and imaginary axes of the control system reference frame Re' and Im' . In other words, the sensed d and q-components that are transformed into the control system reference frame can be given as a function of the angle difference θ_Δ and the d and q-components tied to the ideal grid reference frame. Developing the small-signal model of the PLL requires that the dependency between the two reference frames is solved and linearized.

Let us consider an arbitrary space vector \mathbf{x}^s that has been defined in the original reference frame tied to grid voltages. The space vector can be projected along the real and imaginary axes of the control system reference frame. The space vector $\mathbf{x}^{s'}$ can be given as a function of the angle θ_Δ and space vector in the grid reference frame by utilizing the *Euler's formula* as

$$\mathbf{x}^{s'} = \mathbf{x}^s \cdot e^{-j\theta_\Delta} = \mathbf{x}^s \cdot (\cos \theta_\Delta - j \sin \theta_\Delta)$$

from which the real and imaginary components can be solved as

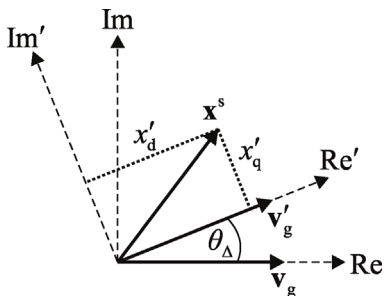


Figure 13.4 Grid voltage space vectors tied to two synchronous reference frames.

$$\begin{aligned} x'_d &= x_d \cos \theta_\Delta + x_q \sin \theta_\Delta, \\ x'_q &= x_q \cos \theta_\Delta - x_d \sin \theta_\Delta. \end{aligned} \quad (13.1)$$

The relation in Eq. (13.1) is equivalent to the average relation between d and q-components of the space vectors tied to grid reference frame and to control system reference frame. Equation (13.1) can be linearized by solving the partial derivatives and by developing the proper first-order partial derivatives as

$$\begin{aligned} \hat{x}'_d &= \cos \Theta_\Delta \hat{x}_d + \sin \Theta_\Delta \hat{x}_q + (X_q \cos \Theta_\Delta - X_d \sin \Theta_\Delta) \delta_\Delta, \\ \hat{x}'_q &= -\sin \Theta_\Delta \hat{x}_d + \cos \Theta_\Delta \hat{x}_q - (X_q \sin \Theta_\Delta + X_d \cos \Theta_\Delta) \delta_\Delta. \end{aligned} \quad (13.2)$$

The steady-state value of the angle difference Θ_Δ is zero. Therefore, the relationship simplifies to

$$\begin{aligned} \hat{x}'_d &= \hat{x}_d + X_q \hat{\theta}_\Delta, \\ \hat{x}'_q &= \hat{x}_q - X_d \hat{\theta}_\Delta. \end{aligned} \quad (13.3)$$

The values of sensed d and q-components \hat{x}'_d and \hat{x}'_q in the control system reference frame depend on the steady-state values of the corresponding d and q-components X_d and X_q and on the small-signal variable $\hat{\theta}_\Delta$ which is still unknown. The subscript “ Δ ” shall be omitted hereafter and the small-signal angle is denoted simply by $\hat{\theta}$. A linear control block diagram can be drawn to solve the unknown small-signal angle. The PI-controller and the integrator in Figure 13.4 can be linearized and represented in the frequency domain. However, the Park’s transformation has to be treated carefully. The sensed grid voltage q-component v'_q can be given as a function of the grid voltage q-component and the small-signal angle by applying Eq. (13.3) as

$$\hat{v}'_q = \hat{v}_q - V_d \hat{\theta}. \quad (13.4)$$

The linear control block diagram can be represented in the frequency domain as shown in Figure 13.5. The small-signal angle can be solved from the control block diagram and is given in Eq. (13.5) where the loop gain of PLL is defined in Eq. (13.6). As can be seen in Eq. (13.6), the SRF-PLL (cf. Figure 13.2) is basically an inverting and integrating process. Moreover, the gain of the process depends linearly on the amplitude of the balanced three-phase voltages V_d that is a well-known drawback of the SRF-PLL [3,9]. It should be emphasized that the PLL becomes a noninverting process when the control diagram is defined as in Figure 13.3.

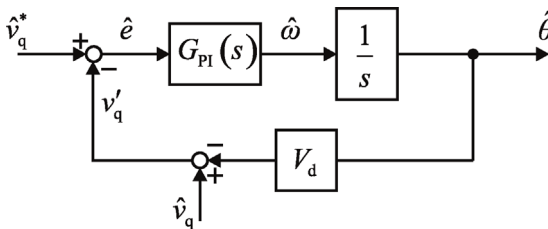


Figure 13.5 Linearized control block diagram of the SRF-PLL.

$$\hat{\theta} = \frac{1}{V_d} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_q - \frac{1}{V_d} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_q^* \quad (13.5)$$

$$L_{PLL} = G_{PI} \left(-\frac{V_d}{s} \right) = G_{PI} G_p. \quad (13.6)$$

The reference of the PI controller v_q^* is set to zero in order to synchronize the control system reference frame with the grid voltage space-vector. The closed-loop transfer function of the PLL can be given as in Eq. (13.7), which is obtained by noting that the reference v_q^* is always zero.

$$\hat{\theta} = \frac{1}{V_d} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_q. \quad (13.7)$$

The small-signal d and q-components \hat{x}'_d and \hat{x}'_q , which are affected by the PLL, can be given as in Eq. (13.8) which is obtained by substituting Eq. (13.7) in Eq. (13.3). This is the relation that shall be later used to include the dynamic effect of the PLL in the closed-loop models of voltage and current-fed inverters.

$$\hat{x}'_d = \hat{x}_d + \frac{X_q}{V_d} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_q, \quad (13.8)$$

$$\hat{x}'_q = \hat{x}_q - \frac{X_d}{V_d} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_q.$$

13.2.2 Control Design of SRF-PLL

The linearized control block diagram of SRF-PLL can be rearranged as shown in Figure 13.6 by noting that the sensed grid voltage q-component \hat{v}'_q is the actual controlled variable and that the grid voltage q-component \hat{v}_q presents a disturbance to the system. The closed-loop dynamics can be solved from the block diagram and is given in Eq. (13.9).

$$\hat{v}'_q = \frac{L_{PLL}}{1 + L_{PLL}} \hat{v}_q^* + \frac{1}{1 + L_{PLL}} \hat{v}_q. \quad (13.9)$$

PI-controllers are conventionally used in SRF-PLL to eliminate steady-state error. The plant transfer function ($G_p = -V_d/s$) of the SRF-PLL is shown in Figure 13.7 for a three-phase grid (230 V_{rms}, 50 Hz) where the grid voltages are balanced and their amplitude are 325 V. The SRF-PLL presents an inverting,

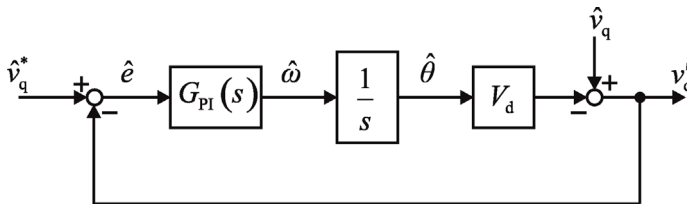


Figure 13.6 Rearranged linearized control block diagram of the SRF-PLL.

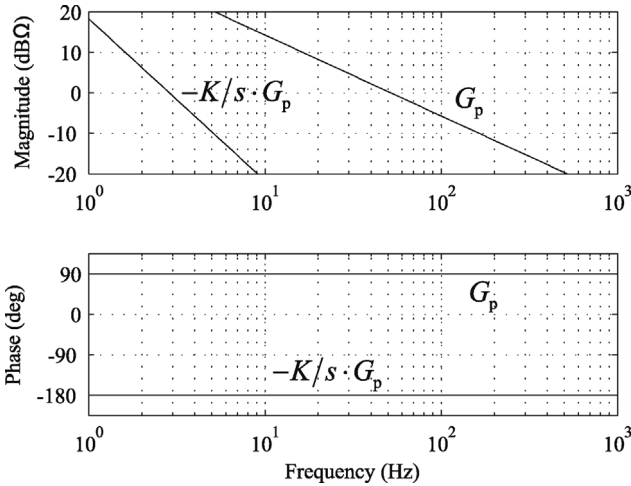


Figure 13.7 Plant transfer function and loop gain with I-type controller.

integrating process with a gain that depends on the grid voltage amplitude V_d . Since it is an inverting process, the phase of the plant transfer function starts from $+90^\circ$ opposed to normal integrator that has a phase of -90° . Inverting process requires inverted control signal that is equivalent to multiplying the controller transfer function with -1 . Figure 13.7 also depicts the loop gain when inverting integral control is applied instead of a PI-type controller ($+K/s \cdot G_p$). The gain of the controller is selected as unity for brevity. As can be deduced from the figure, the loop gain is always marginally stable regardless of the controller gain K . The phase margin of the loop gain is always zero degrees and cannot be increased using an I-type controller.

The phase margin can be increased by adding a low-frequency zero in the controller transfer function. In this example, 100 Hz crossover frequency is planned for the SRF-PLL. Suitable phase margin is selected as 65° that is obtained iteratively by adding first a zero at 10 Hz that is sufficiently below the planned crossover frequency. Frequency of the zero is increased until phase of the loop gain is approximately -115° at 100 Hz. The final value for the zero is found out to be 47 Hz. Figure 13.8 shows the loop gains when the controller zero is placed at 10 and 47 Hz.

The controller gain K is adjusted to a value that satisfies the crossover frequency of 100 Hz. The gain can be easily computed based on the frequency response in Figure 13.8 since the gain K affects only the magnitude of the control loop. One only needs to determine how much the gain curve has to be raised to make it cross the 0 dB line at 100 Hz. Thus, the gain is selected as $10^{(54.3/20)}$. The final control loop gain that fits the initial specification is shown in Figure 13.9. The controller transfer function is given in Eq. (13.10).

$$G_c = (-1) \times \frac{10^{(54.3/20)}((s/2\pi \cdot 47 \text{ rad/s}) + 1)}{s} \quad (13.10)$$

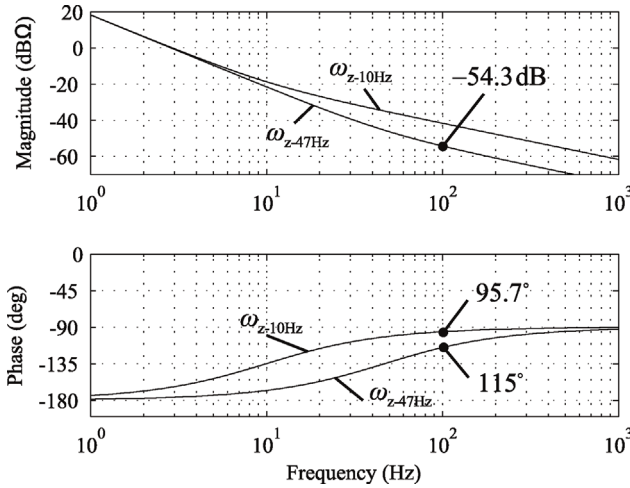


Figure 13.8 Control loop gain with integrator and zero at two different frequencies.

A standard PI-type controller is depicted in Figure 13.10. A PI-controller is usually preferred since it allows easy implementation of integrator wind up by limiting the maximum and minimum value of the integrator output. Moreover, it is easy to implement in discrete form or in a simulation program such as MATLAB/Simulink.

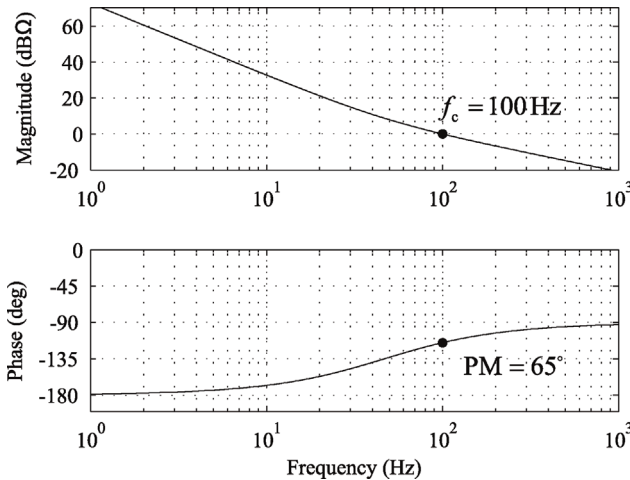


Figure 13.9 The final loop gain of the SRF-PLL.

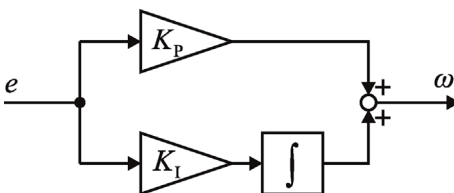


Figure 13.10 PI-type controller.

The parameters of the PI-controller can be derived from (13.10) and can be given as

$$G_{PI} = (-1) \cdot \frac{K_{PLL}(s/\omega_{z-PLL} + 1)}{s} = (-1) \cdot \left(\frac{K_{PLL}}{\omega_{z-PLL}} + \frac{K_{PLL}}{s} \right), \quad (13.11)$$

$$K_{P-PLL} = \frac{K_{PLL}}{\omega_{z-PLL}}, \quad K_{I-PLL} = K_{PLL}. \quad (13.12)$$

13.2.3 Damping Ratio and Undamped Natural Frequency

Transfer function from the reference to controlled variable can be represented as

$$\begin{aligned} \frac{\hat{v}'_q}{\hat{v}^*_q} &= \frac{L_{PLL}}{1 + L_{PLL}} = \left[\frac{(-1) \cdot K_{PLL}(s/\omega_{z-PLL} + 1)}{s} \cdot \left(-\frac{V_d}{s} \right) \right] \\ &/ \left[1 + \frac{(-1) \cdot K_{PLL}(s/\omega_{z-PLL} + 1)}{s} \cdot \left(-\frac{V_d}{s} \right) \right] = \left[\frac{K_{PLL} V_d}{\omega_{z-PLL}} s + K_{PLL} V_d \right] \\ &/ \left[s^2 + \frac{K_{PLL} V_d}{\omega_{z-PLL}} s + K_{PLL} V_d \right]. \end{aligned} \quad (13.13)$$

The closed-loop transfer function can be analyzed as a second-order system as shown in Eq. (13.14) where the damping ratio is given by $\xi = \sqrt{K_{PLL} V_d} / 2\omega_n$ and the natural frequency is given by $\omega_n = \sqrt{K_{PLL} V_d}$.

$$\frac{\hat{v}'_q}{\hat{v}^*_q} = \frac{L_{PLL}}{1 + L_{PLL}} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}. \quad (13.14)$$

In terms of PI-controller parameters, the damping ratio and natural frequency can be given as in Eq. (13.15) [7]. These parameters are important in control design because damping ratio determines the overshoot after a step test and natural frequency defines the frequency of oscillation in the controlled variable after a step test.

$$\xi = \frac{K_{P-PLL}}{2} \cdot \sqrt{\frac{V_d}{K_{I-PLL}}}. \quad (13.15)$$

$$\omega_n = \sqrt{K_{I-PLL} V_d}. \quad (13.16)$$

The damping ratio in Eq. (13.15) can be selected iteratively by changing the values for the controller gain K_{PLL} and the frequency of the controller zero ω_{z-PLL} . The damping ratio $1/\sqrt{2}$ is often considered as the optimal damping ratio that provides good compromise between the settling time and overshoot of the systems step response [9]. The natural frequency of the closed-loop transfer function in Eq. (13.16) depends on the crossover-frequency of the loop gain.

13.2.4 Control Design Example and Experimental Verification

Phase-locked-loop of a 3 kW three-phase inverter intended for a 120 V_{rms}/60 Hz AC grid is designed as an example. The loop gain is designed using the previously

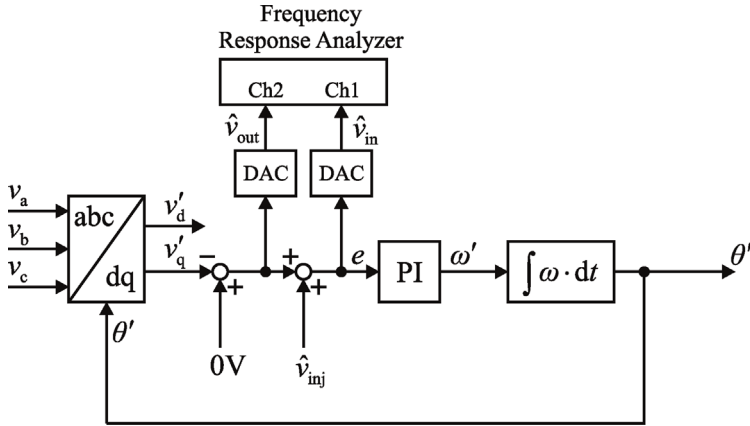


Figure 13.11 Measurement setup for extracting PLL loop gain.

presented loop-shaping techniques for crossover frequencies of 20 and 200 Hz. The phase margin is set to 65° in both cases.

The control system of the inverter was implemented using a dSPACE real-time simulator that made measuring the loop gain straightforward using a frequency response analyzer since small-signal variables are easily accessible. The principle of measurement setup is depicted in Figure 13.11. A sinusoidal small-signal injection was added in the error signal of the PI-controller that is a perfect injection point since the steady-state value of the error signal is zero. Therefore, it is easier to prevent the AD converters from saturating. Signals before and after the injection point were fed to a frequency response analyzer to calculate the loop gain. The principle of the loop gain measurement is the same as in Ref. [10].

Figure 13.12 shows the measured and predicted loop gains. The loop gain is affected by delay of analog-to-digital conversion of the measured three-phase

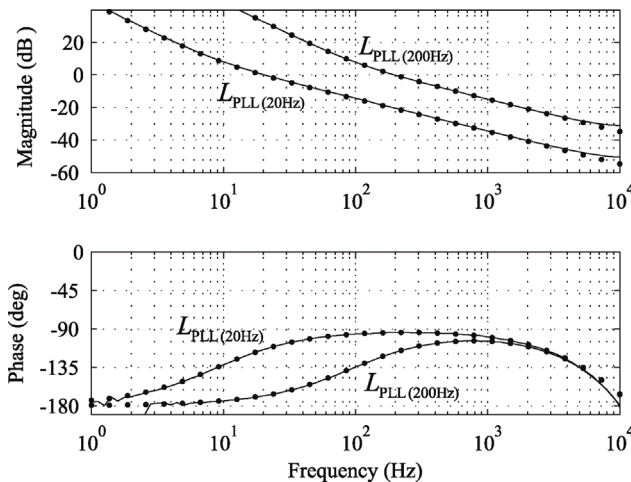


Figure 13.12 Measured and predicted PLL loop gains.

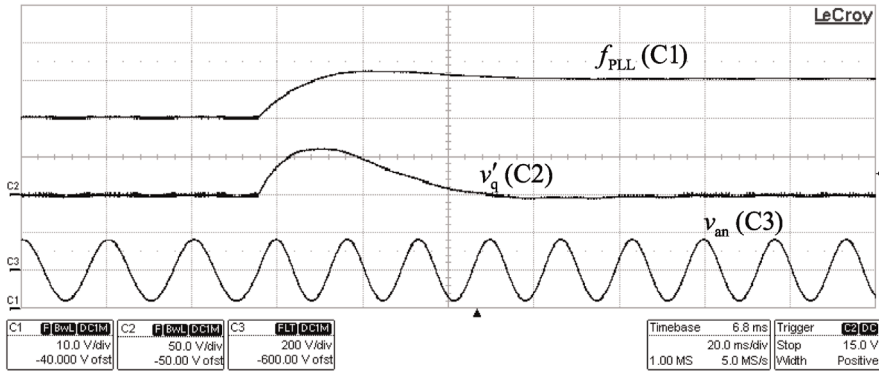


Figure 13.13 Step response of the PLL with 20 Hz crossover frequency.

voltages. The real-time simulator was sampling at the frequency of 20 kHz, which is the same as inverter switching frequency. Analog-to-digital conversion of three-phase voltages introduces an average delay of half the switching period $T_{\text{del}} = 0.5 \cdot T_s = 0.5/f_s$. The first-order Padé approximation was used to represent the delay transfer function in the frequency domain, as given in Eq. (13.17). The sampling delay does not affect the magnitude of loop gain. However, the phase starts decreasing after 1 kHz that sets the upper boundary for theoretically achievable crossover frequency. In practical applications, there are also other limiting factors regarding the maximum crossover frequency such as the effect of unbalanced grid voltages and the risk of impedance-based instability.

$$G_{\text{del}} = \left[1 - \frac{T_{\text{del}}}{2}s \right] / \left[1 + \frac{T_{\text{del}}}{2}s \right] = \left[1 - \frac{s}{4f_s} \right] / \left[1 + \frac{s}{4f_s} \right]. \quad (13.17)$$

Control performance of the PLL was tested by making a step change in the grid frequency from 50 to 60 Hz. The grid voltages were generated using a three-phase grid emulator. The inverter was disconnected while making the step test to allow evaluating the PLL performance without the effect of the inverter. Figure 13.13 shows the step response when PLL was tuned to have crossover frequency of 20 Hz and phase margin of 65° . The sensed grid frequency experiences an overshoot of roughly 23% while the calculated damping ratio is 0.710.

The PLL controller was modified to have 200 Hz crossover frequency and 65° phase margin. The step response is as shown in Figure 13.14. The overshoot in the estimated grid frequency is roughly 25% and the calculated damping ratio is equal to 0.688. The PLL with 200 Hz crossover frequency can track the step change in grid frequency faster. However, it also picks up noise at twice the fundamental frequency that is caused by small gain differences in the AC voltage probes and small unbalance in three-phase voltages, that is, the PLL loop gain amplifies any noise that is located below its crossover frequency. High-quality voltage probes should be used if high-bandwidth PLL is to be used.

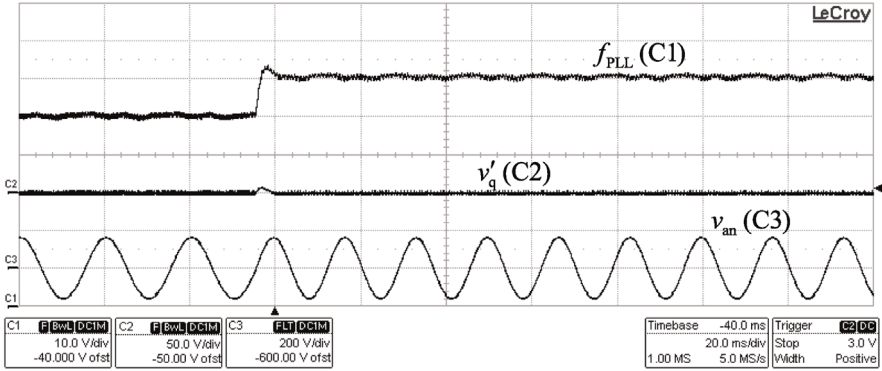


Figure 13.14 Step response of the PLL with 200 Hz crossover frequency.

13.2.5 The Effect of Unbalanced Grid Voltages

Unbalance in grid voltages is a common source of disturbances, such as ripple in DC voltage at twice the fundamental frequency. Moreover, the gains of voltage probes can differ and, therefore, the inverter control system sees an unbalanced grid. Unbalanced grid voltages cause the estimated grid frequency and phase angle to have a second-harmonic component [7] and the three-phase converter to produce harmonic currents at the third harmonic [11].

An unbalanced three-phase system can be described using positive and negative sequence components as in Eq. (13.18) where the space vector \mathbf{V}_{abc+} denotes the positive and \mathbf{V}_{abc-} the negative sequence component.

$$\mathbf{V}_{abc} = V^+ \begin{bmatrix} \cos(\omega_s t) \\ \cos\left(\omega_s t - \frac{2\pi}{3}\right) \\ \cos\left(\omega_s t + \frac{2\pi}{3}\right) \end{bmatrix} + V^- \begin{bmatrix} \cos(\omega_s t) \\ \cos\left(\omega_s t + \frac{2\pi}{3}\right) \\ \cos\left(\omega_s t - \frac{2\pi}{3}\right) \end{bmatrix} = \mathbf{V}_{abc+} + \mathbf{V}_{abc-}. \quad (13.18)$$

Clarke's transformation can be applied to the unbalanced grid as

$$\begin{aligned} \mathbf{V}_{\alpha\beta} &= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} (\mathbf{V}_{abc+} + \mathbf{V}_{abc-}) \\ &= V^+ \begin{bmatrix} \cos(\omega_s t) \\ \sin(\omega_s t) \\ 0 \end{bmatrix} + V^- \begin{bmatrix} \cos(\omega_s t) \\ -\sin(\omega_s t) \\ 0 \end{bmatrix} = \mathbf{V}_{\alpha\beta+} + \mathbf{V}_{\alpha\beta-}. \end{aligned} \quad (13.19)$$

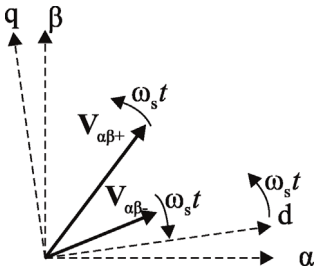


Figure 13.15 Positive and negative sequence voltages in the stationary reference frame.

Figure 13.15 illustrates the space-vectors of positive and negative sequence components in the stationary reference frame. As the name suggest, the positive sequence component $V_{\alpha\beta+}$ rotates in the positive direction and the negative sequence component $V_{\alpha\beta-}$ rotates in the opposite direction.

The unbalanced voltages in the stationary reference frame can be given in the synchronous reference frame (assuming ideal grid synchronization) that is rotating in the same direction as the positive sequence component according to Eq. (13.20). The zero-sequence component is neglected for brevity.

$$\mathbf{V}_{dq} = \mathbf{V}_{\alpha\beta} \cdot e^{-j\omega_s t} = \begin{bmatrix} V^+ + V^- \cos(2\omega_s t) \\ -V^- \sin(2\omega_s t) \end{bmatrix}. \quad (13.20)$$

The d-component of the sensed grid voltage is equal to the amplitude of the positive sequence voltage, but has an additional sinusoidal component at the second harmonic that is determined by the amplitude of negative sequence component. Moreover, the sensed q-component has zero DC value as expected but also includes the sinusoidal component at the second harmonic. The sinusoidal component caused by the unbalance is either amplified or attenuated by the PLL, depending on the magnitude of the PLL control loop gain at the second-harmonic frequency.

A photovoltaic inverter was connected to a 120 V/60 Hz grid in which one phase had 20% smaller amplitude. The SRF-PLL was tuned to have crossover frequencies of 200 and 20 Hz, as in the previous example. Figure 13.16 shows the estimated grid frequency and the unbalanced three-phase grid voltages. The estimated grid frequency contains a large component at twice the fundamental frequency, that is, at 120 Hz. This is due to the fact that the control loop in Figure 13.12 is tuned to have a crossover frequency of 200 Hz and, therefore, disturbance at the second harmonic, and any other distortion for that matter, gets amplified.

Figure 13.17 shows the grid currents of the inverter and the corresponding spectrum obtained by FFT. Spectrum analysis reveals that there is large third harmonic when fast PLL is used. The rest of the harmonic components are caused by the dead-time effect of IGBT bridge and small offsets in the current and differential voltage probes. The inverter switching frequency was set to 8 kHz and the dead-time was selected as 4 μ s (maximum turn-off time according to

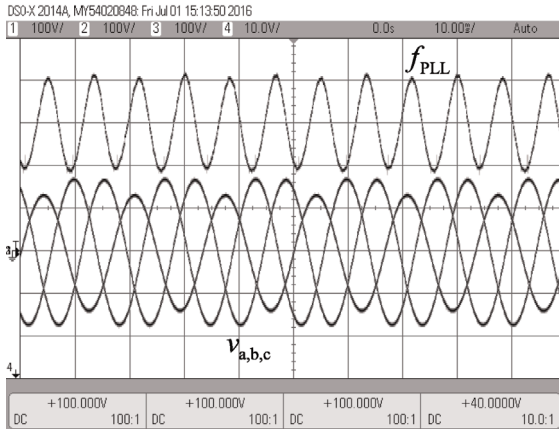


Figure 13.16 Estimated grid frequency in unbalanced grid with fast PLL.

datasheet is 3.6 μ s). Amplitude of the fundamental component is 7 A, but it is not shown in the figure for readability.

The effect of unbalance can be somewhat mitigated by decreasing the PLL crossover frequency. Figure 13.18 shows the estimated grid frequency and grid voltages when the PLL was tuned to have a crossover frequency of 20 Hz. The second-harmonic distortion in the estimated grid frequency is decreased significantly because the loop gain provides roughly 16 dB attenuation at 120 Hz.

Grid current waveforms are significantly improved due to “cleaner” estimation of the grid angle, or to be precise, the angle of grid voltage positive-sequence component. Three-phase grid currents and the corresponding spectrum are shown in Figure 13.19 with the slow PLL.

Slower PLL will generate less third harmonics in grid current during unbalance. However, the ability of the inverter to follow variations in grid voltage amplitude and frequency is worse. This is an important aspect to recognize since

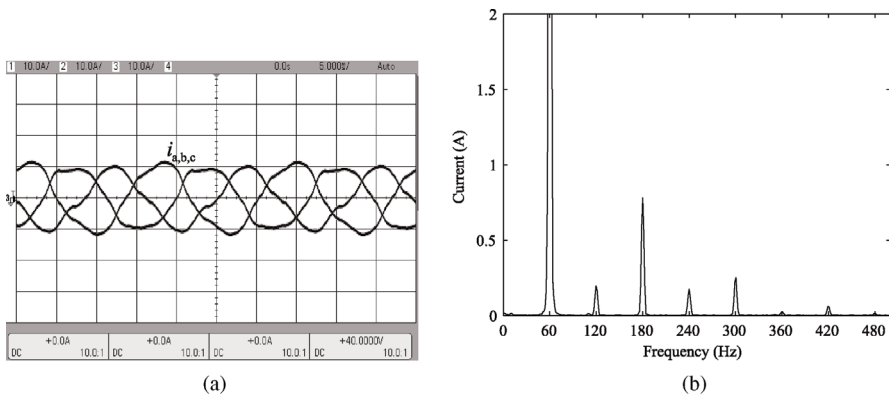


Figure 13.17 Grid currents and the corresponding spectrum with fast PLL.

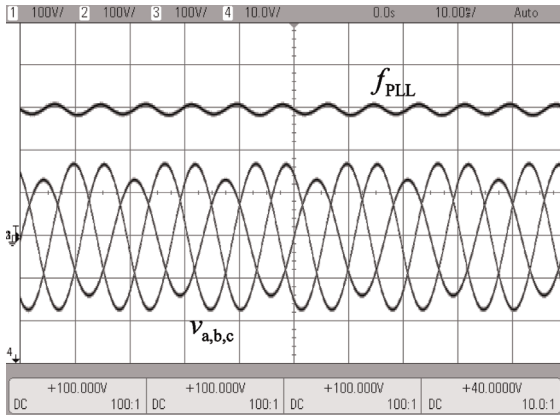


Figure 13.18 Estimated grid frequency in unbalanced grid with slow PLL.

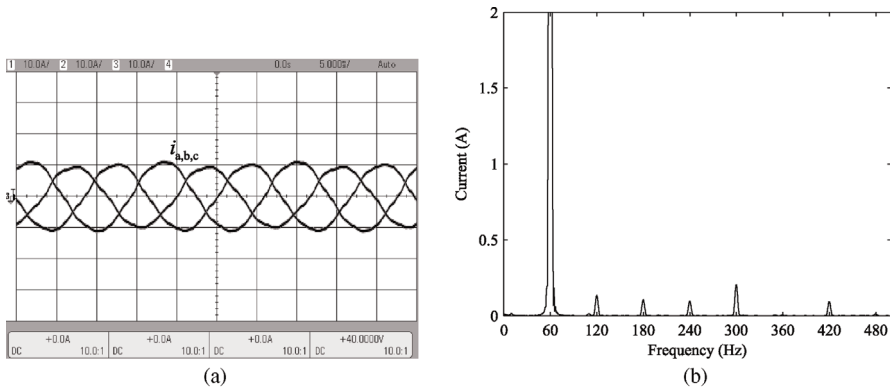


Figure 13.19 Grid currents and the corresponding spectrum with slow PLL.

many islanding protection schemes and other grid monitoring functions rely on the grid frequency estimation of the PLL. The tendency is to use more sophisticated PLL schemes, such as decoupled double reference frame PLL that aim to reduce the second harmonic component from appearing in the sensed grid angle to avoid power quality problems in unbalanced grids. However, most of the recent synchronization methods are based on the SRF-PLL that makes understanding of its operation crucial. Moreover, the other methods can be linearized and added in the inverter dynamic model by applying similar methods as presented in this chapter.

13.3 AC Current Control

Ideally, a grid-parallel three-phase inverter should resemble a three-phase AC current source. Interfacing such converter to a stiff voltage-type load, such as a

stiff power system, does not produce any problems in the view of Kirchhoff's laws, since an ideal current source can feed any current to the grid. As a result, the output currents of a three-phase inverter are usually controlled with high bandwidth. The current control not only provides correct interfacing for a voltage-type load, but fast current control is also used to limit the amplitude of output currents during transients and faults. Moreover, the amount of real and reactive power can be controlled separately by regulating the grid current d and q-components.

There are numerous ways to implement current control [12]. Three most widely adopted methods include current control in dq-domain using PI-controllers, in $\alpha\beta$ -domain using a proportional resonant controller (PR), and several methods based on model predictive control (MPC). The PR and MPC are not discussed in this chapter but the reader is advised to see, for example, Refs [13–17] for further studies. The modeling and design methods presented in this chapter concentrate on the control in dq-domain, since it is the most often used method as it is inherited from motor control applications.

13.3.1 Current Control in the dq-Domain

Main advantage of current control in the dq-domain is the fact that real and reactive power can be controlled separately using simple PI controllers. The magnitudes of current d and q-components determine the amount of real and reactive power fed to (or drawn from) the grid, respectively. The instantaneous apparent power can be defined using space-vectors in the dq-domain as in Eq. (13.21), which is based on the instantaneous power theory introduced by Akagi *et al.* [18].

$$s = \mathbf{v} \cdot \mathbf{i}^* = (v_d i_d + v_q i_q) + j(v_q i_d - v_d i_q) \quad (13.21)$$

The apparent power has real and imaginary components that correspond to instantaneous real and reactive powers, respectively. The phase-locked-loop discussed in the previous chapter aligns the dq-reference frame to a position where the grid voltage q-component v_q seen by the inverter control system is zero. Therefore, the real and imaginary powers can be defined as in Eq. (13.22) from which it is rather easy to see that current d-component determines the amount of active power and current q-component determines the amount of reactive power.

$$p = v_d i_d, \quad q = -v_d i_q. \quad (13.22)$$

13.3.2 Current Control in Voltage-Fed Inverters

Control design of a voltage-fed inverter is discussed first since it is much easier to analyze than a current-fed inverter. Current-fed inverter employs a cascaded control structure where the DC voltage controller gives a reference value for the

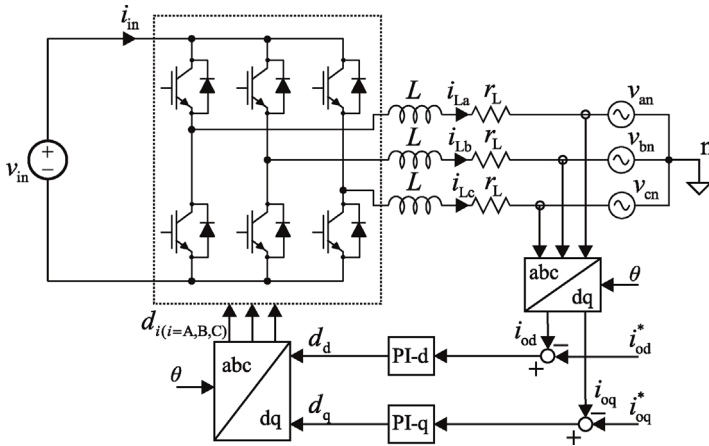


Figure 13.20 Voltage-fed inverter with output-current control implemented in the dq-domain.

d-component of output current. Therefore, the dynamics of DC voltage control affect the low-frequency characteristics of current control.

Figure 13.20 depicts an output-current-controlled voltage-fed inverter. The inverter output currents are controlled in the dq-domain by using negative feedback and PI-type controllers. The control laws can be simply given as in Eqs. (13.23) and (13.24) when the effects of current sensing circuits are neglected. The grid voltage angle θ is determined by the phase-locked-loop, which is omitted from the figure for brevity. Reference values for output current d and q-components are determined by a higher control function, for example, battery charging algorithm or AC voltage controller, and are analyzed as system inputs. Usually decoupling gains are used which aim to reduce cross-coupling effects between d and q-components during transients. The decoupling gains are added in the model and the selection of their parameters is discussed later. To keep it simple, only two current controllers are included in the model at first.

$$d_d = G_{\text{PI-d}}(i_{\text{od}}^* - i_{\text{od}}). \quad (13.23)$$

$$d_q = G_{\text{PI-q}}(i_{\text{oq}}^* - i_{\text{oq}}). \quad (13.24)$$

Cross-couplings between d and q-components are assumed weak enough to be neglected in the following analysis. Although, this is not usually the case, the assumption allows us to build the dynamic model in a more comprehensible manner and makes it easy to identify the control loop gains. Thus, the cross-coupling transfer functions between the d and q-components are neglected, that is, transfer functions $Y_{\text{oqd-o}}$, $Y_{\text{odq-o}}$, $G_{\text{coqd-o}}$, and $G_{\text{codq-o}}$ in Eq. (12.28) are replaced by zeros. Moreover, it is assumed that the input dynamics depend only

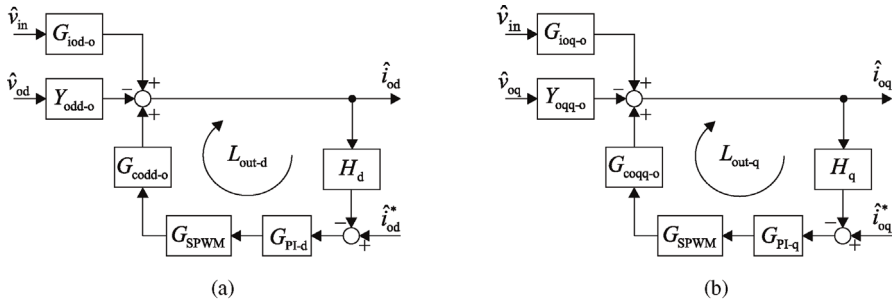


Figure 13.21 Reduced-order output dynamics of (a) d-channel and (b) q-channel.

on d-components, which is a justifiable assumption when the inverter operates close to unity power factor [19]. As will be discussed later, such assumptions are not needed when the small-signal model is built by noting the MIMO nature of the inverter and using transfer matrices [20]. However, these simplifications allow us to develop a reduced-order model of the voltage-fed inverter where, for example, the dynamic effects of control loop gains are easier to interpret. The reduced-order input dynamics and output dynamics of d and q-components can be given as in Eqs. (13.25)–(13.27). The open-loop transfer functions of the voltage-fed inverter with L-type filter can be derived using the method presented in Chapter 12.

$$\hat{i}_{in} = Y_{in-o} \hat{v}_{in} + T_{oid-o} \hat{v}_{od} + G_{cid-o} \hat{d}_d. \tag{13.25}$$

$$\hat{i}_{od} = G_{iod-o} \hat{v}_{in} - Y_{odd-o} \hat{v}_{od} + G_{codd-o} \hat{d}_d. \tag{13.26}$$

$$\hat{i}_{oq} = G_{ioq-o} \hat{v}_{in} - Y_{oqq-o} \hat{v}_{oq} + G_{coqq-o} \hat{d}_q. \tag{13.27}$$

It is assumed that the controller and sensing circuits are linear and their transfer functions are known. Current controller transfer functions are denoted using G_{PI-d} and G_{PI-q} whereas, transfer functions of sensing circuits are denoted as H_d and H_q and modulator gain as G_{SPWM} . The control block diagrams are given in Figure 13.21 for output dynamics and in Figure 13.22 for input dynamics.

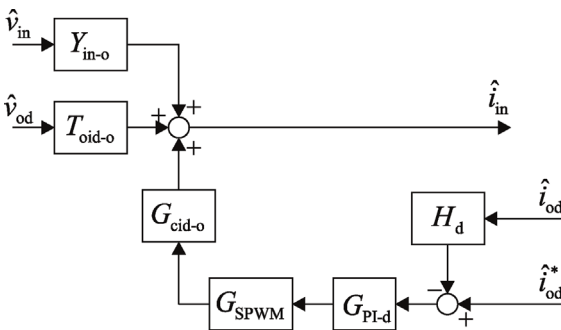


Figure 13.22 Reduced-order input dynamics.

The current control loop gains can be identified from Figure 13.21 and given as

$$L_{\text{out-d}} = G_{\text{codd-o}} G_{\text{SPWM}} G_{\text{PI-d}} H_{\text{d}}, \quad (13.28)$$

$$L_{\text{out-q}} = G_{\text{coqq-o}} G_{\text{SPWM}} G_{\text{PI-q}} H_{\text{q}}. \quad (13.29)$$

The control dynamics $G_{\text{codd-o}}$ and $G_{\text{coqq-o}}$ have to be predicted or measured accurately before selecting the controller transfer functions. Moreover, the gains of the modulator and sensing circuits have to be known since they affect directly the magnitude of the control loop gain. For simplicity, it is assumed that the sensing gain and modulator gain are unity. DC gains can be easily compensated, for example, inside the control algorithm running on a DSP. Sampling delays introduced by DA and AD conversion and low-pass-filter of the sensing circuit should be included in the model if they are expected to have considerable effect on the inverter control performance. For now, it is assumed that we have a system without delay and ideal measurement circuits. Parameters of the studied inverter switching model are collected in Table 13.1. The inverter is operated at unity power factor and utilizes a SRF-PLL with 20 Hz crossover frequency.

The inverter simulation model was implemented in MATLAB Simulink using the SimScape component library and is shown in Figure 13.23. The model includes two manual switches that can be used to exclude the effect of PLL and to operate the inverter either in open loop or under output-current control.

The simulation model was operated at open loop by setting the “Manual Switch1” in the position shown in Figure 13.23. Moreover, the PLL was bypassed by the other manual switch, that is, the angle fed to the dq-transformation blocks was calculated straight from the grid angular frequency using an integrator. The open-loop control dynamics were extracted by using a PRBS-injection method where the small-signal injection was summed to the steady-state value of duty ratios D_{d} and D_{q} .

Figure 13.24 shows the control-to-output-current transfer functions $G_{\text{codd-o}}$ extracted from the switching model. The q-component $G_{\text{coqq-o}}$ has identical shape and is, therefore, not shown in the figure. The dynamic model predicts the shape of the transfer function accurately since there are no unknown elements in the simulator. Only the passive and active electrical components that are essential to implement the inverter model are used. The transfer functions $G_{\text{codd-o}}$ and $G_{\text{coqq-o}}$ frequency response in Figure 13.24 shall be used as the plant transfer function to design the current controllers.

Table 13.1 Parameters of the voltage-fed inverter simulation model.

P_{in}	5 kW	V_{in}	700 V	V_{od}	325 V
I_{od}^*	10 A	I_{oq}^*	0 A	ω_{s}	$2\pi \cdot 50 \text{ rad/s}$
L	5 mH	$r_{\text{L}} + r_{\text{sw}}$	100 m Ω	f_{sw}	20 kHz

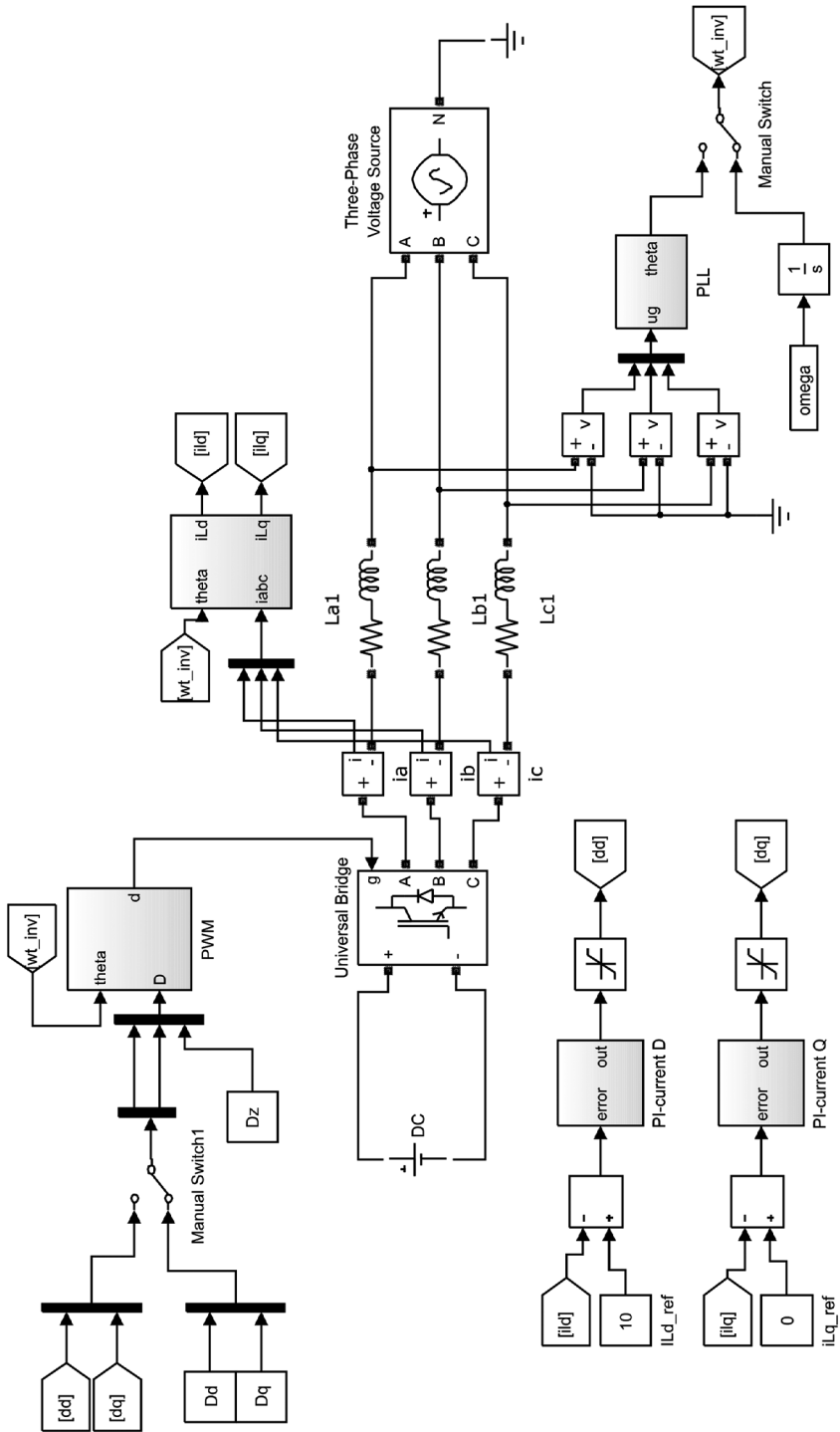


Figure 13.23 Voltage-fed inverter simulation model implemented in Simulink.

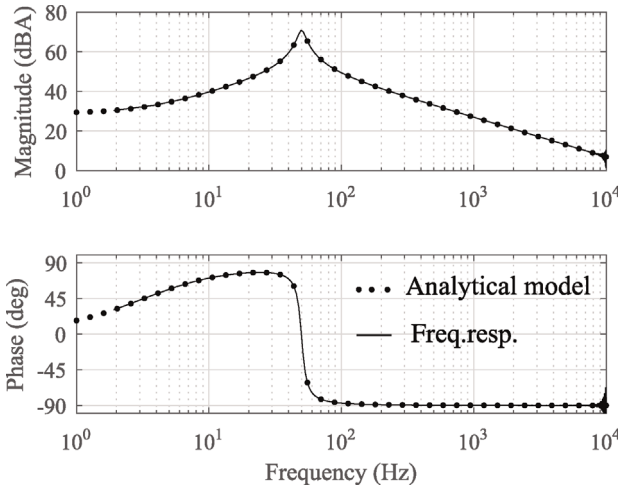


Figure 13.24 Output control dynamics $G_{\text{codd-o}}$ and $G_{\text{coqq-o}}$ of a voltage-fed inverter.

Phase of the plant transfer function starts from zero degrees which implies that a conventional negative feedback control can be used to stabilize the control loop. An integrator is used to eliminate steady-state error that can be simply given as $1/s$ in the frequency domain. Figure 13.25 shows the predicted current control loop gain when an integrator with unity gain is included in the small-signal loop gains of Eqs. (13.28) and (13.29). It is impossible to implement high-bandwidth current control using pure I-type control since the phase drops to -180° after the resonant frequency. Therefore, even though the crossover frequency could be set to, for example, 1 kHz by increasing gain of the integrator, the phase margin would still be zero.

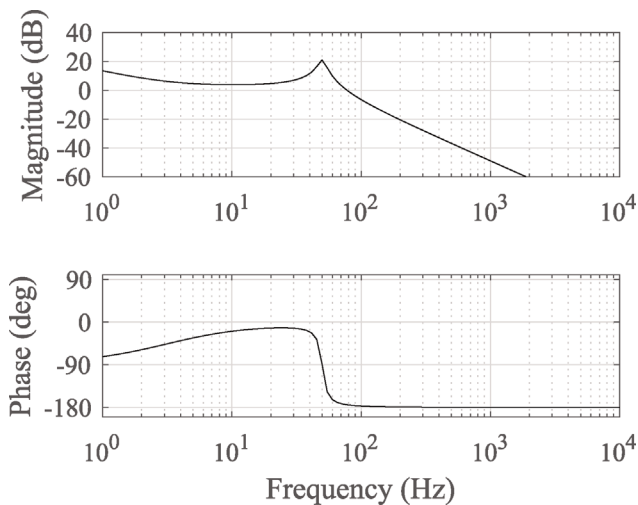


Figure 13.25 Current control loop gain with unity-gain integrative feedback control.

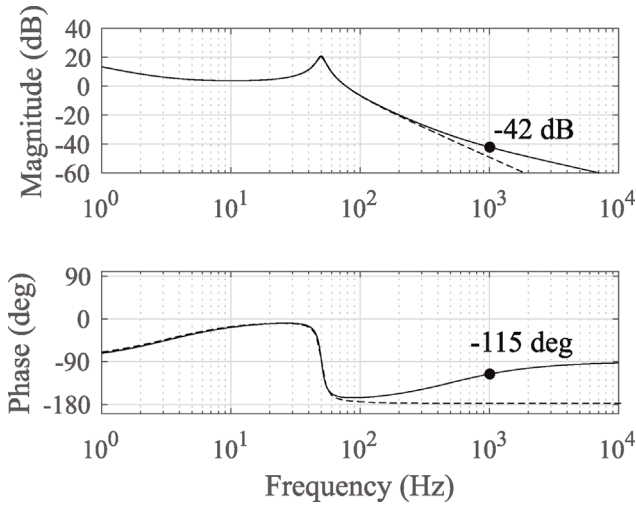


Figure 13.26 Current control loop with unity-gain integrator and LHP-zero at 500 Hz.

The controller transfer function is multiplied by an LHP-zero at 500 Hz to boost the phase around the desired crossover frequency, which in this case is 1 kHz. The resulting loop gain is as shown in Figure 13.26 where the phase boost is illustrated compared to the previous case. The phase has now a value of approximately -115° at 1 kHz that translates into 65° phase margin if crossover frequency would be increased to 1 kHz.

The crossover frequency can be easily increased or decreased by selecting an appropriate controller gain. According to Figure 13.26, a $+42$ dB boost is required to have 1 kHz crossover frequency. The final controller transfer function can be given in the frequency domain as in Eq. (13.30) or, alternatively as the equivalent PI-type controller in Eq. (13.31). The final predicted loop gain is as shown in Figure 13.27.

$$G_{\text{PI-d}} = G_{\text{PI-q}} = 10^{42/20} \cdot \frac{(s/(2\pi \cdot 500) + 1)}{s}. \quad (13.30)$$

$$G_{\text{PI-d}} = G_{\text{PI-q}} = \frac{10^{42/20}}{2\pi \cdot 500} + \frac{10^{42/20}}{s} = K_p + \frac{K_I}{s}. \quad (13.31)$$

The validity of control design was tested using the switching model. Both the d and q currents were controlled using identical PI-controllers. Figure 13.28 shows the inverter output currents in the dq-domain when a step from 8 to 10 A was made in the reference of the current d-component. The reference value of output current q-component is set to zero. The control is stable and settles around the new reference in approximately 1.5 ms. The PLL was tuned to have a crossover of 20 Hz and phase margin on 65° .

Figure 13.29 shows the three-phase grid currents and voltages during the step test. The amplitude increases from 8 to 10 A just as expected. Moreover, the phase

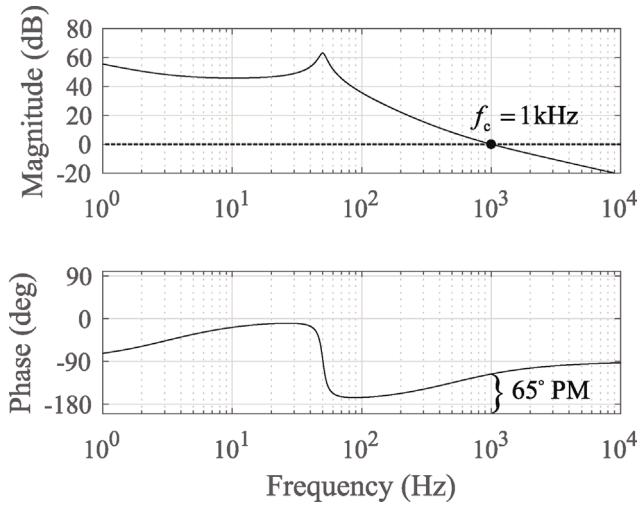


Figure 13.27 Finalized loop gain with 1 kHz crossover frequency and 65° phase margin.

currents are in phase with grid voltages as the reference of the current q -component is zero.

The loop gain was extracted from the simulator using the PRBS-method. As can be seen from Figure 13.30, the loop gain predicted by the dynamic model gives very good estimates at high frequencies. However, there is a resonance in the predicted loop gain that does not appear in the actual inverter dynamics. However, the accuracy of dynamic model in predicting the plant transfer functions $G_{\text{codd-o}}$ and $G_{\text{coq-o}}$ was verified earlier in Figure 13.24, which shows that the open-loop model was correctly formulated. At this point, it should be noted that the loop gains were derived by neglecting the cross-coupling transfer

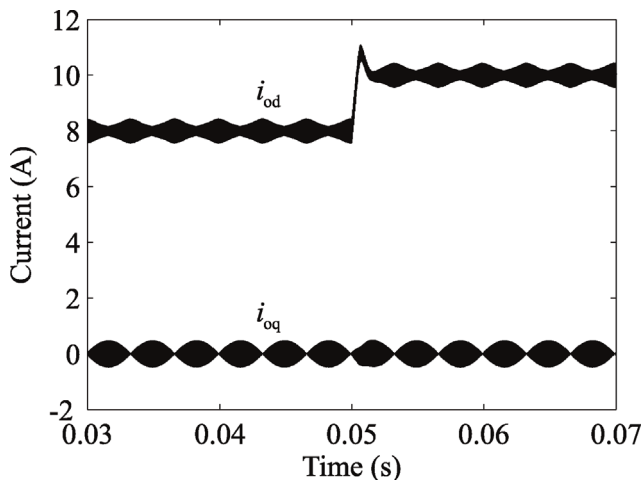


Figure 13.28 Response of the designed current control to a step change from 8 to 10 A.

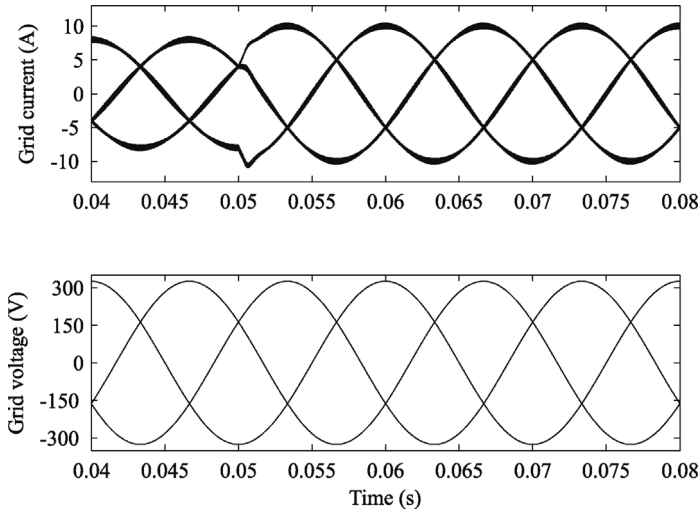


Figure 13.29 Step response in the abc-domain.

functions and this, of course, comes with a price. However, the crossover frequency and phase margin can be accurately predicted since the reduced-order model is valid at frequencies higher than the resonance at approximately 50 Hz.

The control loop gains can be obtained from the full-order output control block diagram of Figure 13.31. For simplicity, sensing and modulator gains are neglected. Such model can be useful if for some reason very low crossover frequency is wanted. Only the control dynamics are included in the figure for brevity since other inputs, such as \hat{v}_{in} , \hat{v}_{od} , and \hat{v}_{oq} can be assumed zero. As mentioned earlier, the inverter model in dq-domain is essentially a MIMO-system, that is, the controllers interact with each other. The control loop gain of the d-component can be solved from the control block diagram by cutting the

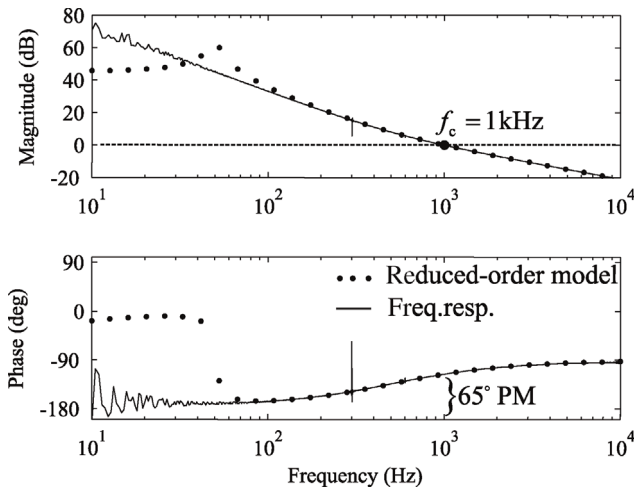


Figure 13.30 Measured current control loop gain of d-component.

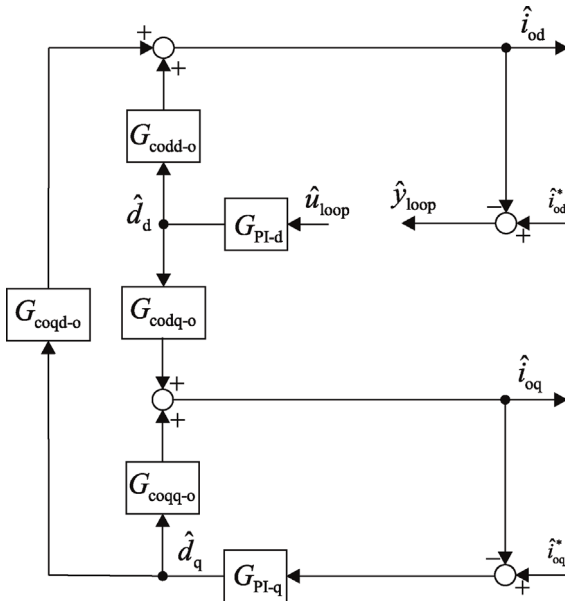


Figure 13.31 Control block diagram describing the current control loop gain with cross-couplings.

signal path at the marked point and solving the transfer function from the input \hat{u}_{loop} to output \hat{y}_{loop} .

The current control loop gain that includes the effect of cross-coupling transfer functions can be given as in Eq. (13.32). Computing the loop gain may at first seem too much of an effort when, in fact, crossover and phase margin can be evaluated by using the reduced-order model. However, the full-order loop gain allows including the dynamic effects of source and load impedances. Figure 13.32 depicts

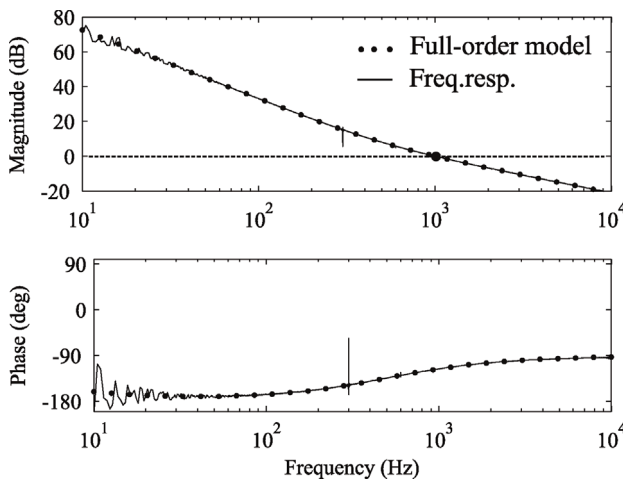


Figure 13.32 Current control loop gain derived with cross-coupling transfer functions.

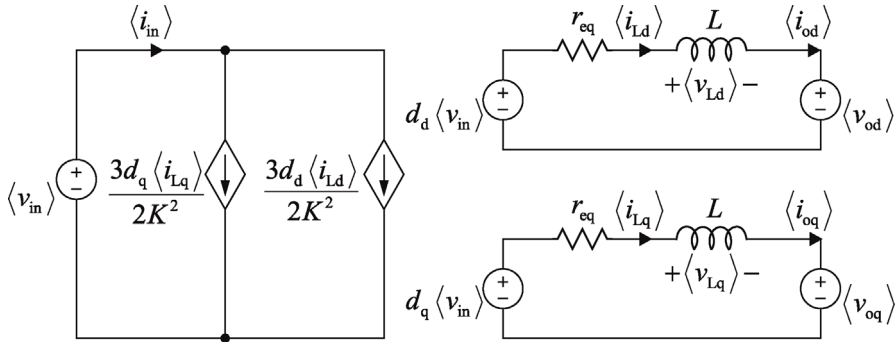


Figure 13.33 Simplified average model without cross-couplings.

the control loop when cross-coupling transfer functions are included in the small-signal model according to (13.32). The resonance has disappeared from the predicted loop gain as can be seen by comparing the analytical model and the obtained frequency response. In summary, neglecting the cross-coupling transfer functions produces additional complexity in the predicted loop gain that is in reality compensated by the cross-coupling transfer functions.

$$L_{\text{out-d}}^{\text{FO}} = \frac{\hat{y}_{\text{loop}}}{\hat{u}_{\text{loop}}} = G_{\text{PI-d}} G_{\text{codd-o}} - \frac{G_{\text{codq-o}} G_{\text{coqd-o}}}{1 + G_{\text{PI-q}} G_{\text{coq-q-o}}} G_{\text{PI-q}} G_{\text{PI-d}}. \quad (13.32)$$

The main goal of this book is to provide a systematic approach to derive dynamic models of three-phase converters. An accurate dynamic model allows source and load effects to be evaluated and closed-loop impedances with different control functions to be solved. However, the control dynamics can be obtained by making very rough approximations on the inverter dynamics. In the literature, it is common to approximate current control dynamics using single-phase equivalent circuit. This is equivalent to neglecting the cross-coupling voltage sources in the average model as shown in Figure 13.33.

The linearized state-space of the simplified average model can be given as in Eqs. (13.33) and (13.34) from which the control-to-output-current transfer functions $G_{\text{codd-o}}$ and $G_{\text{coq-q-o}}$ can be solved and given as in Eqs. (13.35) and (13.36).

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \end{bmatrix} = \begin{bmatrix} -\frac{r_{eq}}{L} & 0 \\ 0 & -\frac{r_{eq}}{L} \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \end{bmatrix} + \begin{bmatrix} \frac{D_d}{L} & -\frac{1}{L} & 0 & \frac{V_{in}}{L} & 0 \\ \frac{D_q}{L} & 0 & -\frac{1}{L} & 0 & \frac{V_{in}}{L} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (13.33)$$

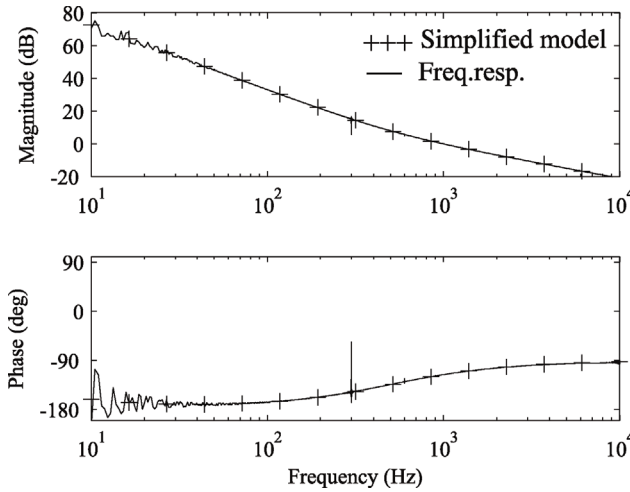


Figure 13.34 Comparison of extracted current control loop gain and the simplified model.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} = \begin{bmatrix} \frac{3D_d}{2K^2} & \frac{3D_q}{2K^2} \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & \frac{3I_{Ld}}{2K^2} & \frac{3I_{Lq}}{2K^2} \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (13.34)$$

$$G_{\text{codd-o}}^{\text{simplified}} = \frac{\hat{i}_{od}}{\hat{d}_d} = \frac{V_{in}}{sL + r_L}. \quad (13.35)$$

$$G_{\text{coq-q-o}}^{\text{simplified}} = \frac{\hat{i}_{oq}}{\hat{d}_q} = \frac{V_{in}}{sL + r_L}. \quad (13.36)$$

Figure 13.34 shows the loop gain extracted from the simulator and the simplified loop gain where $L_{\text{out-d}} = G_{\text{PI-d}} G_{\text{codd-o}}^{\text{simplified}}$. It is certain that the simplified model that does not consider cross-couplings can be used in current control design. However, one should apply the model with caution since it is difficult to include the dynamic effects of source or load impedances in the control dynamics. Moreover, the effect of LCL-filter and active damping should be analyzed carefully.

13.4 Decoupling Gains

Decoupling gains are often used in the AC current control in order to decouple the dynamics of d and q-components from each other. The gains can be derived from the linearized model of the voltage-fed inverter. The linearized output

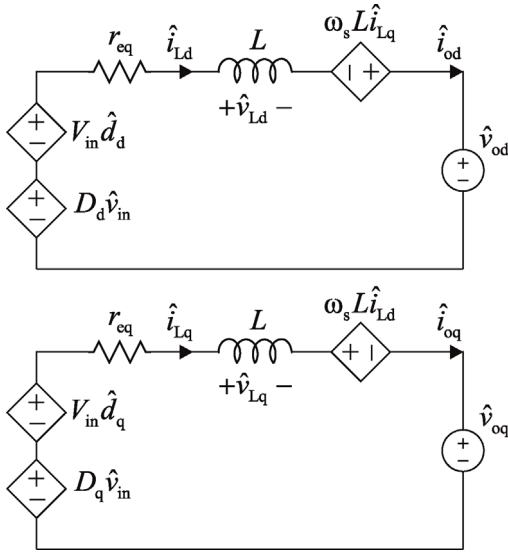


Figure 13.35 Linearized output dynamics of voltage-fed inverter.

dynamics of d and q-components were derived in Chapter 12 and can be expressed as

$$\frac{d\hat{i}_{Ld}}{dt} = \frac{1}{L} \left(-r_{eq}\hat{i}_{Ld} + \omega_s L \hat{i}_{Lq} + D_d \hat{v}_{in} - \hat{v}_{od} + V_{in} \hat{d}_d \right), \quad (13.37)$$

$$\frac{d\hat{i}_{Lq}}{dt} = \frac{1}{L} \left(-\omega_s L \hat{i}_{Ld} - r_{eq}\hat{i}_{Lq} + D_q \hat{v}_{in} - \hat{v}_{oq} + V_{in} \hat{d}_q \right). \quad (13.38)$$

The linear equivalent circuit diagrams representing the dynamics of d and q-channels are shown in Figure 13.35.

The current-controlled voltage sources that have values of $\omega_s L \hat{i}_{Lq}$ and $\omega_s L \hat{i}_{Ld}$ represent the cross-coupling effects of current d and q-components. The principle of decoupling is to add suitable values \hat{d}_{dx} and \hat{d}_{qx} to the duty ratios inside the control system that effectively cancel out the voltage drops caused by the cross-couplings. The values for these duty ratios can be easily solved from Eqs. (13.37) and (13.38) and given as

$$\hat{d}_{dx} = -\frac{\omega_s L}{V_{in}} \hat{i}_{Lq}, \quad (13.39)$$

$$\hat{d}_{qx} = \frac{\omega_s L}{V_{in}} \hat{i}_{Ld}. \quad (13.40)$$

Control laws for current control with decoupling gains can be given as

$$d_d = G_{PI-d} (i_{od}^* - i_{od}) - \frac{\omega_s L}{V_{in}} i_{Lq}, \quad (13.41)$$

$$d_q = G_{PI-q} (i_{oq}^* - i_{oq}) + \frac{\omega_s L}{V_{in}} i_{Ld}. \quad (13.42)$$

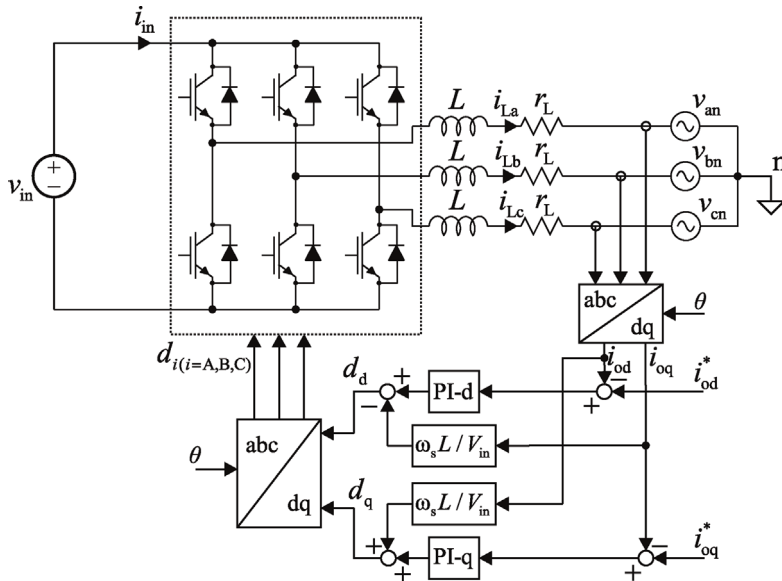


Figure 13.36 Current control with decoupling terms.

The value of the inductance and the steady-state value of input voltage have to be known to realize decoupling of the output currents. Moreover, it is stressed that the decoupling is derived for an inverter employing conventional three-phase SPWM. The gains are different when space-vector modulator is used since the modulator often utilizes measured input voltage to generate the switching vectors. Control system of a voltage-fed inverter with decoupling gains is depicted in Figure 13.36.

The effect of decoupling gains can be demonstrated by making a step change to output current q-component while keeping the d-component constant and vice versa. Figure 13.37 shows the grid currents (in the ideal grid reference

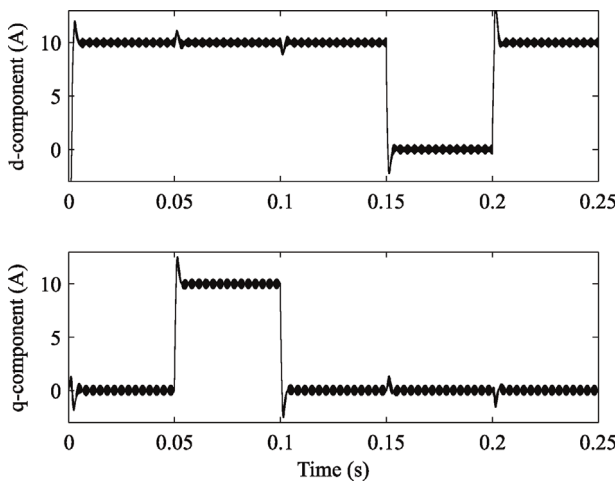


Figure 13.37 Step-response of grid currents without decoupling gains.

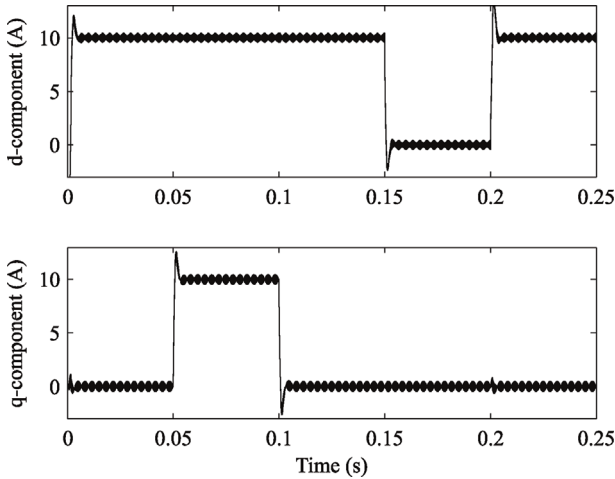


Figure 13.38 Step-response of grid currents with decoupling gains.

frame) when decoupling gains are not used. Reference of the q-component is increased from 0 to 10 A at 0.05 s and decreased back to 0 at 0.1 s. A step change in q-component induces a transient in the d-component. Moreover, the reference of current d-component is decreased from 10 A to 0 at 0.15 s and back to 10 A at 0.2 s. Also the q-component experiences a transient every time the d-component changes which is due to cross-couplings between current d- and q-components.

Figure 13.38 shows the grid current d and q-components when decoupling gains are used. Current d-component remains exactly at 10 A regardless of change in current q-component. Moreover, the current q-component remains at 0 when d-component is stepped down to 0 and back to 10 A. Decoupling gains of the current controller effectively prevent d and q-components from affecting each other. However, the decoupling is not perfect if the steady-state value of DC voltage changes.

13.5 Grid Voltage Feedforward

Grid voltage feedforward is often utilized in grid-connected inverters to improve transient performance and impedance behavior. Originally, the method has been developed to improve dynamic response of electrical drives but due to its benefits and ease of implementation it has also become a popular control method in grid-connected three-phase converters.

The principle of grid voltage feedforward is very simple and easy to understand. The linearized circuit diagram in Figure 13.35 includes grid voltage d and q-components that act as sources of small-signal disturbances. Their effect can be canceled out by measuring the corresponding grid voltage and adding it to the inverter duty ratios. With conventional SPWM, the current control laws

including grid voltage feedforward then become

$$d_d = G_{\text{PI-d}}(i_{\text{od}}^* - i_{\text{od}}) - \frac{\omega_s L}{V_{\text{in}}} i_{\text{Lq}} + \frac{1}{V_{\text{in}}} v_{\text{od}} \quad (13.43)$$

and

$$d_q = G_{\text{PI-q}}(i_{\text{oq}}^* - i_{\text{oq}}) + \frac{\omega_s L}{V_{\text{in}}} i_{\text{Ld}} + \frac{1}{V_{\text{in}}} v_{\text{oq}}. \quad (13.44)$$

The value of proportional feedforward gain is ideally the inverse of input voltage steady-state value when SPWM is used. However, the gain should be reduced, for example, to avoid impedance-based interactions if the control system experiences significant amount of delay, as will be discussed in Chapter 16.

13.6 Cascaded Control Scheme in Current-Fed Inverters

In current-fed inverters, the input voltage is defined as an output variable. In fact, the current-fed inverter employs unstable control dynamics that have to be stabilized by using an outer DC voltage control loop. Figure 13.39 depicts the conventional cascaded control scheme for a current-fed inverter implemented in the dq-domain. The output currents are controlled using the same current control scheme as in the case of a voltage-fed inverter. However, the reference value of output current d-component i_{od}^* is given by the input voltage controller, which is usually a PI-type controller. The control laws can be defined as

$$d_d = G_{\text{PI-d}}(i_{\text{od}}^* - i_{\text{od}}) = G_{\text{PI-d}}((G_{\text{PI-v}}(v_{\text{in}}^* - v_{\text{in}})) - i_{\text{od}}), \quad (13.45)$$

$$d_q = G_{\text{PI-q}}(i_{\text{oq}}^* - i_{\text{oq}}). \quad (13.46)$$

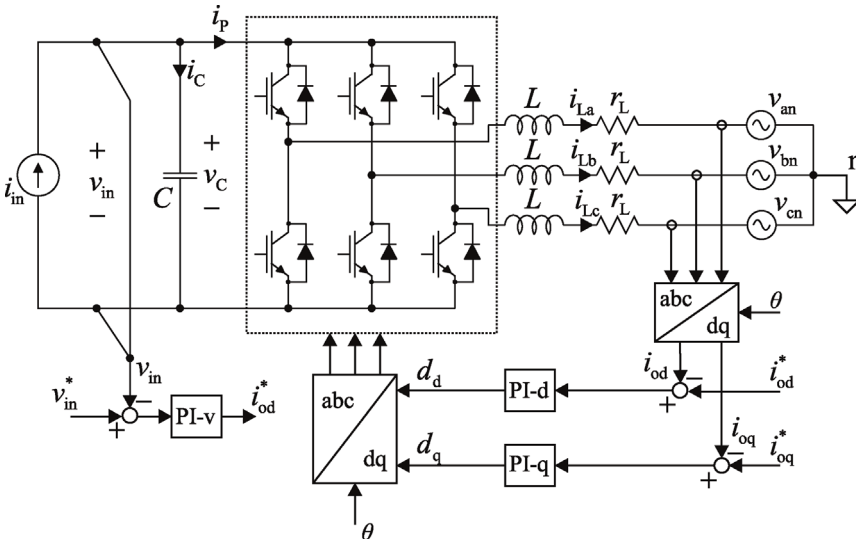


Figure 13.39 Cascaded control scheme of a current-fed inverter.

In a cascaded control structure, the inner control loop has to be fast enough compared to the outer loop. Otherwise, the current controller is not able to follow the reference set by the voltage controller. It is common to tune the inner loop gain to have a crossover frequency of at least one decade higher than the outer voltage control loop gain.

13.6.1 Control Block Diagrams

The reduced-order control dynamics can be derived by neglecting the cross-coupling transfer functions and by assuming that the input dynamics depend only on the d-components. The reduced-order open-loop dynamics can be given as

$$\hat{v}_{in} = Z_{in-o}\hat{i}_{in} + T_{oid-o}\hat{v}_{od} + G_{cid-o}\hat{a}_d, \quad (13.47)$$

$$\hat{i}_{od} = G_{iod-o}\hat{i}_{in} - Y_{odd-o}\hat{v}_{od} + G_{codd-o}\hat{a}_d, \quad (13.48)$$

$$\hat{i}_{oq} = G_{ioq-o}\hat{i}_{in} - Y_{oqq-o}\hat{v}_{oq} + G_{coqq-o}\hat{a}_q. \quad (13.49)$$

Variables that are seen as disturbances, such as the input current and output voltage d and q-components, are neglected in the following analysis because the aim of this chapter is to identify the control loop gains. The input and output control block diagrams can be developed based on Eqs. (13.47)–(13.49). Figure 13.40 shows the control block diagram of the cascaded control structure where G_{SPWM} is the modulator gain and H_d and H_v are the gains related to output current and the DC voltage sensors, respectively.

Figure 13.41 depicts the control function H_q is the output current sensing gain.

Input voltage control loop gain can be solved from the control block diagram in Figure 13.40 and can be given as

$$L_{in} = \frac{G_{cid-o}}{G_{codd-o}} \cdot \frac{L_{out-d}}{1 + L_{out-d}} \cdot \frac{H_v}{H_d} \cdot G_{PI-v}, \quad (13.50)$$

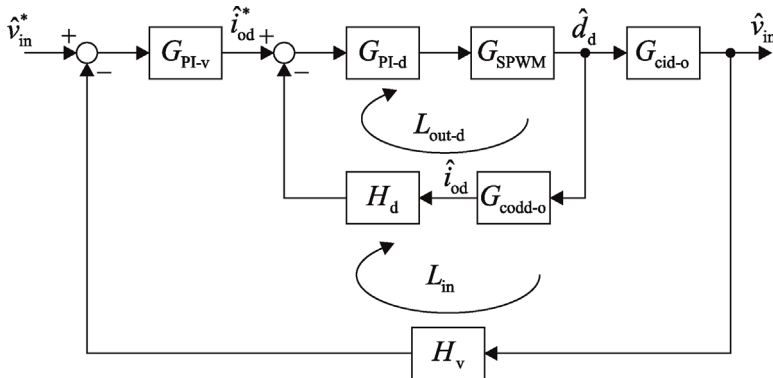


Figure 13.40 Control block diagram of the cascaded control scheme.

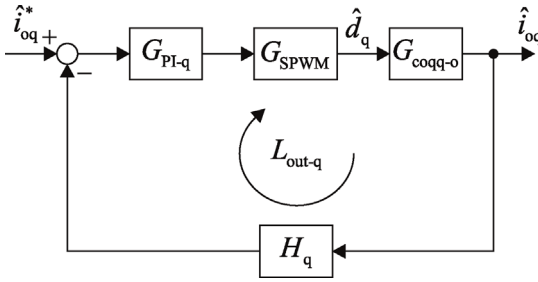


Figure 13.41 Control block diagram of the output current control of q-component.

where the output current control loop gain of the d-component is given by

$$L_{\text{out-d}} = G_{\text{PI-d}} G_{\text{SPWM}} G_{\text{codd-o}} H_{\text{d}}. \quad (13.51)$$

The plant transfer function based on which the input voltage controller is designed can be given as

$$G_{\text{cid-cc}} = \frac{\hat{v}_{\text{in}}}{\hat{i}_{\text{od}}^*} = \frac{G_{\text{cid-o}}}{G_{\text{codd-o}}} \cdot \frac{L_{\text{out-d}}}{1 + L_{\text{out-d}}} \cdot \frac{1}{H_{\text{d}}}. \quad (13.52)$$

The reference of the output current q-component i_{oq}^* is usually set equal to zero to operate the inverter at unity power factor. Alternatively, the reference can be given by an outer control loop, such as an AC voltage controller. However, at this point it is assumed that the reference of current q-component is an independent input variable. The current control loop gain can be given as

$$L_{\text{out-q}} = G_{\text{PI-q}} G_{\text{SPWM}} G_{\text{coqq-o}} H_{\text{q}}. \quad (13.53)$$

The output current control loop of the q-component can be designed by following exactly the same principles as with a voltage-fed inverter. However, designing the cascaded control loops requires careful considerations due to special dynamic properties of the current-fed inverter. The control-to-output-current transfer function $G_{\text{codd-o}}$ can be solved symbolically using, for example, MATLAB Symbolic Toolbox yielding the transfer function as shown in Eq. (13.54). Parasitic resistances are neglected since they have no significant effect on the low-frequency behavior of the transfer function.

$$G_{\text{codd-o}}(s) = \left[V_{\text{in}} \left(s - \frac{I_{\text{in}}}{CV_{\text{in}}} \right) \right] / \left[L \left(s^2 + \frac{3(D_{\text{d}}^2 + D_{\text{q}}^2)}{2CL} + \omega_{\text{s}}^2 \right) \right]. \quad (13.54)$$

The transfer function has a RHP-zero at the frequency given by Eq. (13.55) that is usually on the order of few hertz, since large DC-link capacitors are preferred and input voltage is quite large compared to input current.

$$\omega_{\text{z-RHP}} = \frac{I_{\text{in}}}{CV_{\text{in}}}. \quad (13.55)$$

The RHP-zero becomes a RHP-pole of the input voltage control loop gain of Eq. (13.50), because the loop gain is divided by the transfer function $G_{\text{codd-o}}$, that

is, the input voltage control loop gain has a RHP-pole at $\omega_{p\text{-RHP}} = I_{in}/(CV_{in})$. The input voltage control loop gain can be approximated by Eq. (13.56) at low frequencies where the current control loop is expected to have a large magnitude. From this form it is easier to see how the RHP-zero becomes a RHP-pole. Similar observations have been made in active rectifiers operated in regenerative mode in Ref. [21].

$$L_{in} \approx \frac{G_{cid-o}}{G_{codd-o}} \cdot G_{PI-v}. \quad (13.56)$$

A process that employs a RHP-pole can be stabilized by enclosing the unstable dynamics with an outer control loop and by setting the crossover frequency of the control loop higher than the RHP-pole [22].

13.6.2 Control Design of Cascaded Loops

Control design of a current-fed inverter starts by first tuning the current control loops. The control loops, or at least the control loop of the current d-component should have high enough bandwidth in respect to the expected bandwidth of the input voltage control. The predicted open-loop current control dynamics G_{codd-o} and G_{coqq-o} are shown in Figure 13.42 where the low-frequency behavior of transfer functions can be clearly seen. The parameters of the current-fed inverter are the same as used in the prototype later in Table 13.2. The control-to-output-current transfer function G_{coqq-o} suggests that normal noninverted control signal, that is, negative feedback, should be used since its low-frequency phase starts from zero degrees, that is, its DC gain is positive. However, the transfer function that describes the control dynamics related to output current d-component has a low-frequency phase of 180° . Normally, this would imply inverted control signals, but since we know that the

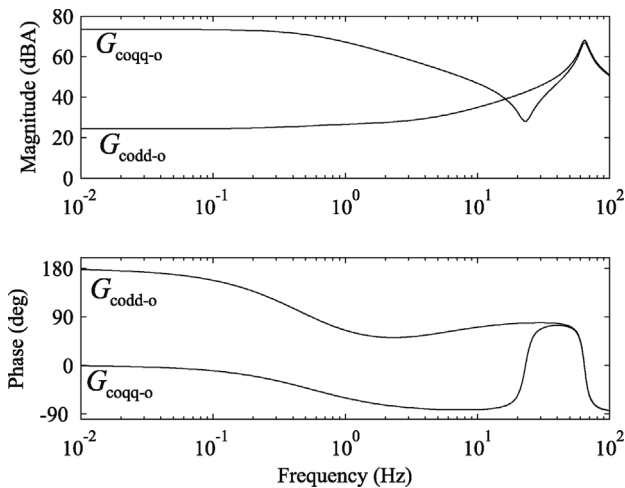


Figure 13.42 Open-loop output current control dynamics.

Table 13.2 Parameters of the photovoltaic inverter.

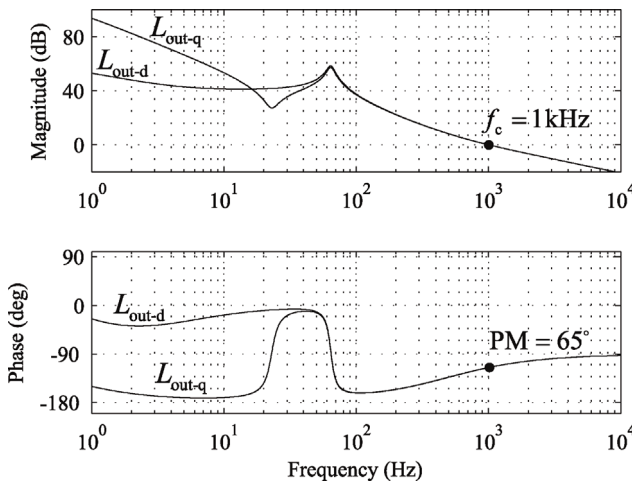
P_{in}	1.5 kW	V_{in}	400–716 V	V_{od}	$\sqrt{2} \cdot 120$ V
I_{in}	0–2.9 A	I_{oq}^*	0–3 A	ω_s	$2\pi \cdot 60$ rad/s
L	4 mH	$r_L + r_{sw}$	100 m Ω	f_{sw}	20 kHz
C	1.95 mF				

transfer function has a RHP-zero that is later stabilized by an outer control loop, we choose to use noninverted control signals for both control loops.

The design of current control loop follows the exact same steps as in the case of a voltage-fed inverter. The goal is to have current control crossover frequency of 1 kHz with 65° of phase margin. The loop gains are first plotted with just an integrator as the controller transfer function, second, a LHP-zero is added at 480 Hz to boost the phase curve, and third, the gain of the controller is adjusted to reach the desired crossover frequency. Finally, the controller transfer functions according to Eq. (13.57) are selected that yield predicted current control loop gains as shown in Figure 13.43. At this stage the RHP-zero is neglected since it will be later stabilized by the outer input voltage control loop. The equivalent PI-controller is as given in Eq. (13.58). Identical controller transfer functions are used to control both d and q-components.

$$G_{PI-d} = G_{PI-q} = 10^{(42/20)} \cdot \frac{(s/2\pi \cdot 480 + 1)}{s}. \quad (13.57)$$

$$G_{PI-d} = G_{PI-q} = \frac{10^{42/20}}{2\pi \cdot 480} + \frac{10^{42/20}}{s}. \quad (13.58)$$

**Figure 13.43** Predicted current control loop gains.

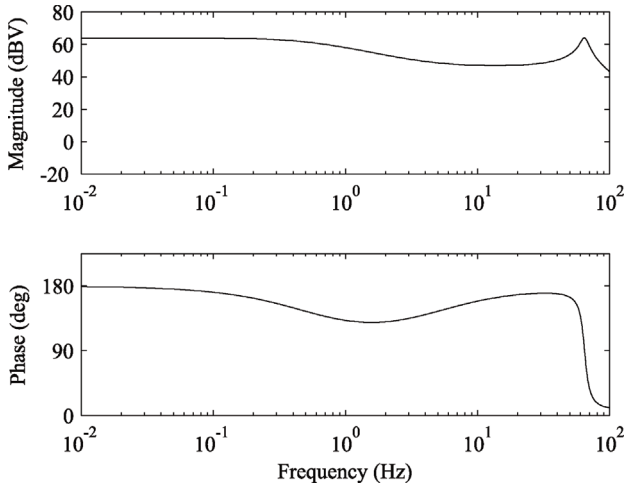


Figure 13.44 Low-frequency part of control-to-input-voltage transfer function G_{cid-o} .

The next task is to stabilize the unstable current control loop L_{out-d} by selecting an appropriate input voltage controller transfer function. The low-frequency part of control-to-input-voltage transfer function G_{cid-o} is as shown in Figure 13.44. The phase of the transfer function starts from 180° that implies that the control signal has to be inverted. However, the inner current control loop gain has to be taken into account in control design according to Eq. (13.50).

The input voltage control loop gain is plotted with inverted control signal and an integrator that eliminates the steady-state error as

$$L_{in} = \frac{(-1)}{s} \cdot \left(\frac{G_{cid-o}}{G_{codd-o}} \cdot \frac{L_{out-d}}{1 + L_{out-d}} \cdot \frac{H_v}{H_d} \right). \quad (13.59)$$

The predicted input voltage loop gain is as shown in Figure 13.45. The crossover frequency is just few hertz where the phase of the loop gain is less than -180° indicating the loop is unstable. However, the phase stays close to -180° over the whole frequency range. Therefore, the phase of the loop gain has to be boosted by a low-frequency zero that is placed at 10 Hz. Moreover, the gain of the loop is adjusted to yield a crossover frequency of 20 Hz. The final loop gain is as shown in Figure 13.46 and the controller transfer function is as given in Eq. (13.60). Moreover, the input voltage loop gain extracted from the switching model is shown in the figure as the solid line.

$$G_{PI-v} = -10^{(30/20)} \cdot \frac{(s/(2\pi \cdot 10) + 1)}{s}. \quad (13.60)$$

Figure 13.47 shows the response of the inverter input voltage to a step change in reference value from the initial value of 571.9 to 600 V. The current reference value, that is, the output of the input voltage controller was limited to values between 0 and 20 A, since larger currents would trip protection in a real inverter. The rise time of the input voltage is, therefore, limited by the fact that current

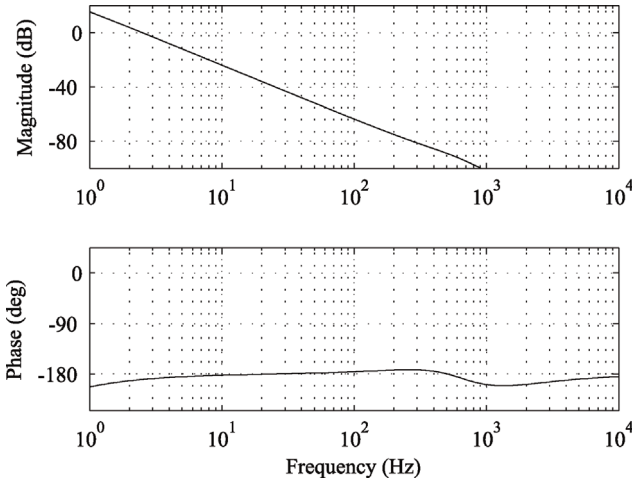


Figure 13.45 Predicted input voltage control loop gain L_{in} with unity-gain integrator and inverted control signal.

reference is not allowed to go negative. The step response indicates that the inverter is stable in a simulator.

Inverter output currents are shown in Figure 13.48 in the phase and dq-domains. The reference of output current d-component drops suddenly and the fast current control loop can track the reference very quickly as it has been tuned to have much higher crossover frequency than the input voltage control loop. The q-component of the output current is maintained at zero during the step test.

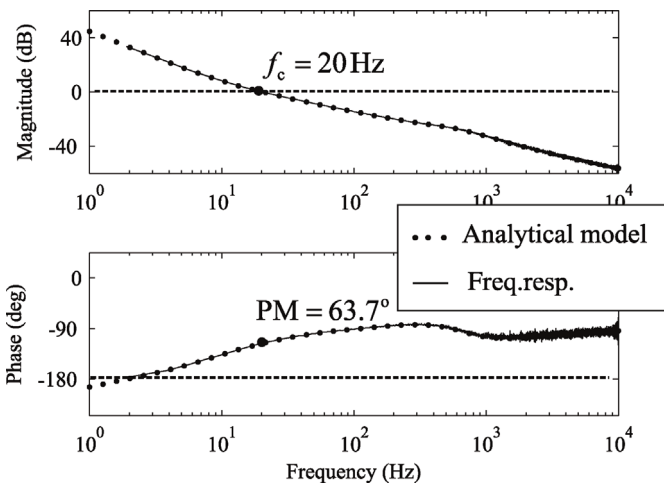


Figure 13.46 Predicted loop gain and the extracted frequency response.

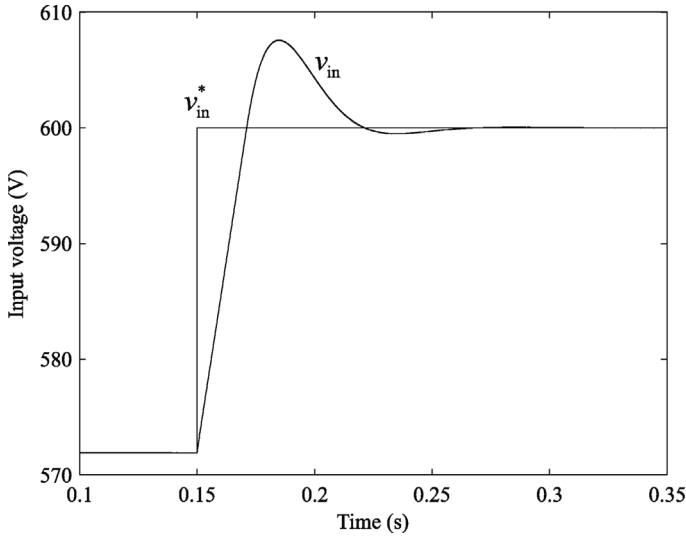


Figure 13.47 Step response of input voltage.

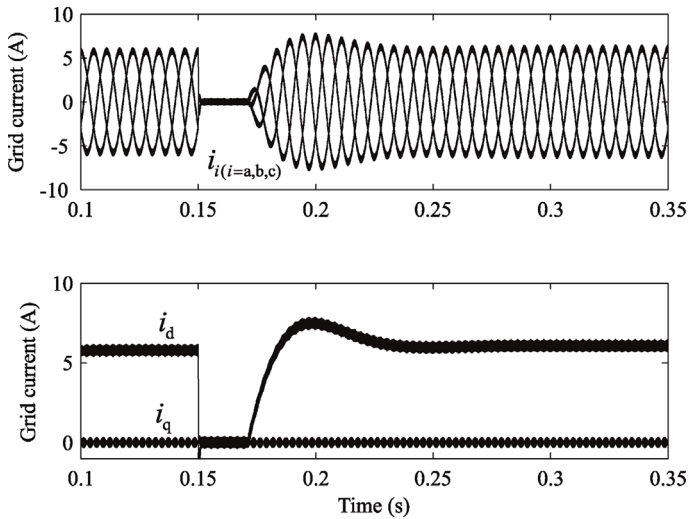


Figure 13.48 Step response of output currents.

13.6.3 Instability Caused by RHP-Pole

The control system is stable as can be seen from the simulation results and the extracted control loop gain. However, a current-fed inverter with small input capacitor may become unstable due to the RHP-pole in the input voltage control loop gain [23]. The input capacitance of the inverter was decreased to $100 \mu\text{F}$. The value of input current is initially 2.6 A that can be used to determine the frequency

of the RHP-pole to be 7.2 Hz as

$$\omega_{p\text{-RHP1}} = \frac{2.6 \text{ A}}{571.9 \text{ V} \times 100 \mu\text{F}} = 2\pi \cdot 7.2 \text{ rad/s.}$$

The RHP-pole can be seen in the plant transfer function of the input voltage control $G_{\text{cid-cc}}$ of Eq. (13.52) as illustrated in Figure 13.49 as a solid line. Due to the RHP-pole, the magnitude starts to drop 20 dB per decade after approximately 7 Hz, and opposite to a LHP-pole, the phase starts to increase at the rate of 45° per decade. The dashed line illustrates the plant transfer function when input current is increased to 8 A that effectively increases the frequency of RHP-pole to 22 Hz.

Designing the loop gain to have a 20 Hz crossover frequency and 65 phase margin requires a LHP-zero at a lower frequency than in the previous case to yield sufficient phase boost. Moreover, the controller gain has to be readjusted. The controller transfer function is as given in Eq. (13.61). The predicted input loop gains with the initial 2.6 A input current and the increased current of 8 A are shown in Figure 13.50 as solid and dashed lines, respectively. The loop gain is stable when input current is 2.6 A. However, the phase margin becomes slightly negative when input current is increased to 8 A that indicates that the control loop is unstable.

$$G_{\text{PI-v}} = -10^{(-8.4/20)} \cdot \frac{(s/(2\pi \cdot 2) + 1)}{s}. \quad (13.61)$$

Figure 13.51 depicts the step response of the input voltage to a reference step from 571.9 to 600 V when the input current is 2.6 A. The settling time is significantly longer than in the previous case in Figure 13.47 because the loop gain has much lower magnitude below its crossover frequency. However, the step response shows that the system is stable.

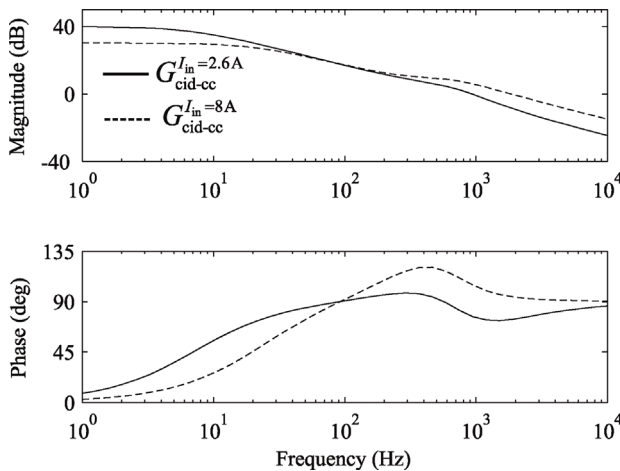


Figure 13.49 Plant transfer function of the input voltage control with small input capacitance and two values of input current.

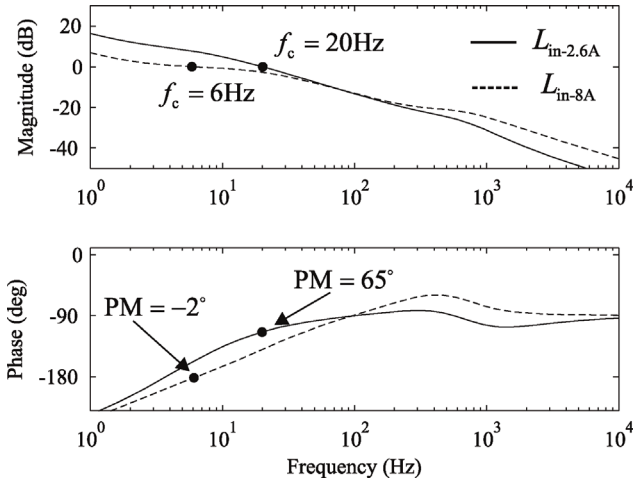


Figure 13.50 Input voltage control loop gains with less input capacitance and input current of 2.6 (solid) and 8 A (dashed).

Figure 13.52 depicts the input voltage when the input current is increased from 2.6 to 8 A at a steady ramp over 3 s. The input voltage experiences a steady-state error during the ramp that is a well-known drawback when using PI-type control. The input voltage becomes unstable when input current reaches approximately 8 A and starts to oscillate at 6.5 Hz which is due to negative phase margin of the control loop gain L_{in-8A} in Figure 13.50. Moreover, the frequency of oscillation is exactly the same as the frequency at which the unstable loop gain has a phase of -180° . The oscillation is reflected to output

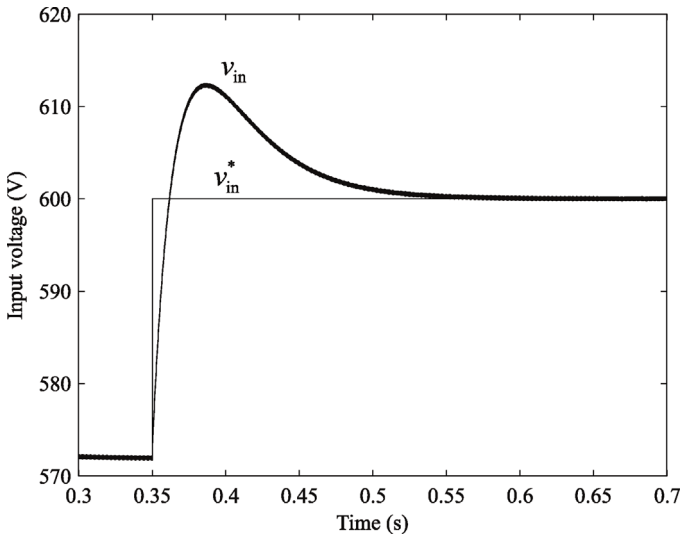


Figure 13.51 Step response of the input voltage with smaller input capacitance.

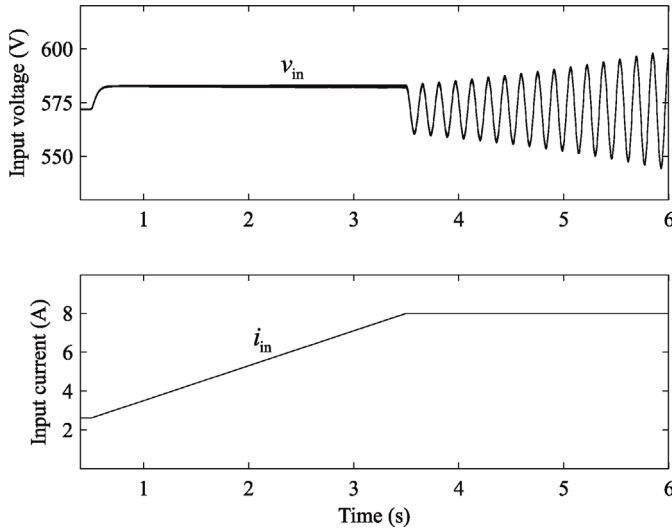


Figure 13.52 Input voltage when instability due to RHP-pole occurs.

currents because the input voltage controller directly affects the reference of output current d-component. The output currents are shown in Figure 13.53 in the phase and dq-domains. The amplitudes of phase currents experience growing low-frequency oscillation.

FFT analysis reveals that the output currents in the dq-domain experience the same low-frequency oscillation of 6.5 Hz as is expected since the current d-component follows the reference value given by the input voltage controller. However, the currents in the phase-domain have sub and interharmonic components at 53.5 and 66.5 Hz. This can be understood by studying the

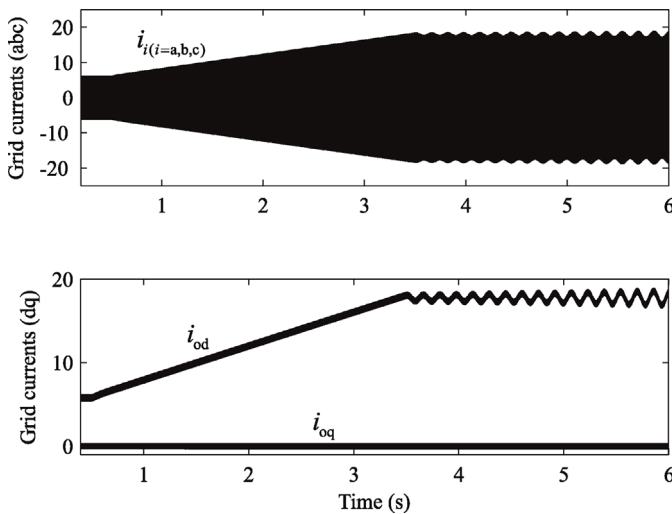


Figure 13.53 Output currents when instability due to RHP-pole occurs.

inverse Park's transformation. The current in phase A can be given as in Eq. (13.62) when the q and zero-components of output current are assumed equal to zero.

$$i_a = \cos(\omega_s t) [I_{od} + I_{d-ac} \cdot \cos(\omega_1 t + \varphi_1)]. \quad (13.62)$$

In Eq. (13.62), I_{od} is the steady-state value of output current d-component, I_{d-ac} is the peak value of the AC component caused by the unstable control loop, ω_1 and φ_1 are the angular frequency and phase angle of the AC component, respectively.

The product-to-sum identity of a cosine function can be given as

$$2 \cos \theta \cos \varphi = \cos(\theta - \varphi) + \cos(\theta + \varphi). \quad (13.63)$$

The phase current can be defined as in Eq. (13.64) from which it can be seen that the inverse Park's transformation produces two AC components in the phase currents centered symmetrically around the fundamental frequency of 60 Hz. Therefore, the output currents in abc-domain have components at $60 - 6.5 = 53.5$ Hz and $60 + 6.5 = 66.5$ Hz.

$$i_a = \cos(\omega_s t) I_{od} + \frac{I_{d-ac}}{2} [\cos(\omega_s t - \omega_1 t - \varphi_1) + \cos(\omega_s t + \omega_1 t + \varphi_1)]. \quad (13.64)$$

13.6.4 Stability Assessment Using the Nyquist Stability Criterion

Stability of the control loop was evaluated directly from the loop gains in the frequency domain. However, to be precise, the stability of a loop gain with a RHP-pole should be predicted by using the Nyquist stability criterion.

The Nyquist stability criterion states that the number of RHP-zeros in a control loop gain is given by Eq. (13.65) where P is the number of RHP-poles and N is the number of clockwise encirclements around the $(-1,0)$ point on the imaginary plane. Note that the RHP-zeros of an open-loop system (control-loop gain) are the poles of the closed-loop system. Therefore, the input voltage control is unstable if the loop gain has one or more RHP-zeros.

$$Z = N + P. \quad (13.65)$$

The inverter is known to have one unstable pole (RHP-pole) in its input voltage control dynamics and, therefore, $P = 1$. For the control loop to be stable the value for N should be -1 , that is, the contour in the imaginary plane should encircle the $(-1,0)$ point once in the counterclockwise direction. Figure 13.54 shows the input voltage loop gains of Figure 13.50 plotted on the imaginary plane. The control loop becomes unstable when input current reaches 8 A, because the contour does not encircle the $(-1,0)$ point.

13.6.5 Design Example: Three-Phase Photovoltaic Inverter

A grid-connected three-phase photovoltaic inverter is one common example of an application where the inverter is modeled as a current-fed inverter and which utilizes cascaded control scheme to stabilize the input voltage. The parameters of

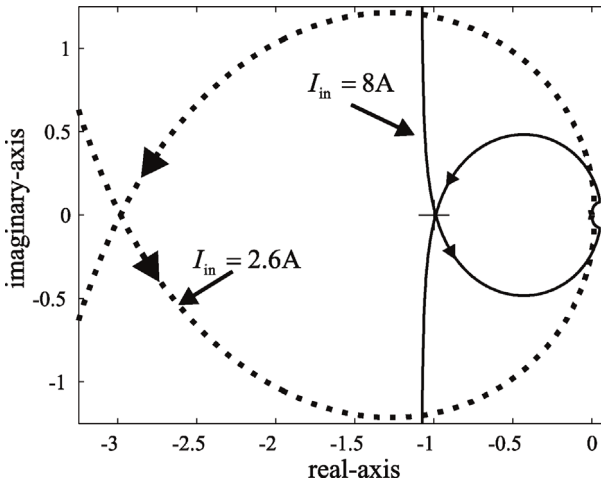


Figure 13.54 Input voltage control loop gains on complex plane.

the experimental current-fed inverter are given in Table 13.2. The laboratory setup is as depicted in Figure 13.55.

A two-level three-phase inverter bridge MWINV-1044-SIC manufactured by Myway with L-type output filter was used to interface a photovoltaic emulator to a three-phase grid emulator. The control system was implemented using a dSPACE real-time simulator. The bridge incorporates six SiC-MOSFET switches of type SCH2080KE that have recommended dead time of $0.3 \mu\text{s}$. The dead time was generated by the dSPACE. The switching frequency of the inverter was selected as 20 kHz. The inverter was fed from the solar array emulator PVS7000 by Spitzenberger & Spies and loaded by a three-phase 4-quadrant amplifier PAS15000 from the same manufacturer. The three-phase linear amplifier can sink approximately 5 kW of real power. Therefore, additional resistive load was not required. The inverter was isolated from the load using a delta-woye-type isolation transformer to mitigate common-mode currents flowing through ground loops.

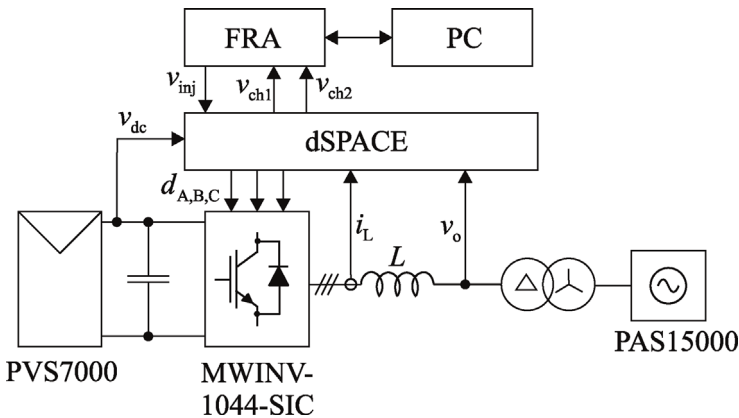


Figure 13.55 Laboratory test setup.

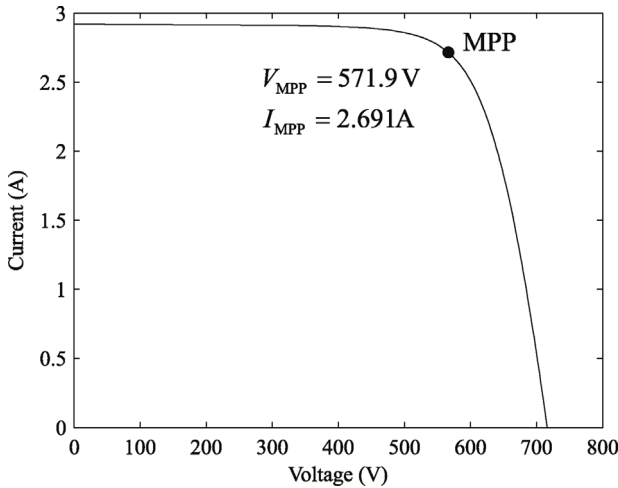


Figure 13.56 IV -curve of the PV emulator.

The IV -curve of the solar array emulator is shown in Figure 13.56. At voltages below the maximum power point, the source resembles a DC current source with constant current of approximately 2.9 A. Therefore, the inverter can be thought to be fed by an ideal current source when operating point is sufficiently below the MPP. From the dynamical point of view the constant current region is the most critical operation region since the control dynamics incorporate a RHP-pole that may destabilize the inverter and distort the output currents.

The input voltage control loop gain was tuned to have a crossover frequency of 20 Hz and phase margin of 65° by using the dynamic model and assuming an ideal DC current source. Moreover, the stability was evaluated earlier using a switching model. The input voltage controller transfer function was given previously in Eq. (13.60). The output current control loop gains were tuned to have 1 kHz crossover frequency and 65° phase margin, and their transfer functions were previously given in Eq. (13.57). The inverter was first tested using these controllers but it was found out that the reference of grid current d-component was corrupted by noise. Therefore, the input voltage control loop needed to be redesigned.

The measured and predicted input voltage control loop gains are shown in Figure 13.57 when the inverter was operated in the CC region at voltage of 400 V. The initial control loop had higher crossover frequency, which means that it will pass noise more easily and deteriorate the reference of the output current d-component. The input voltage controller was redesigned to have lower magnitude at the frequency of the expected noise component (50 Hz). The LHP-zero of the controller was set to a lower frequency to maintain a sufficient phase margin. The redesigned controller transfer function is

$$G_{PI-V} = K \frac{(s/\omega_z + 1)}{s} = -10^{(1.65/20)} \cdot \frac{(s/(2\pi \cdot 2) + 1)}{s}. \quad (13.66)$$

Figure 13.58 shows the measured phase current and the reference of the d-current controller with the initial and redesigned input voltage controller.

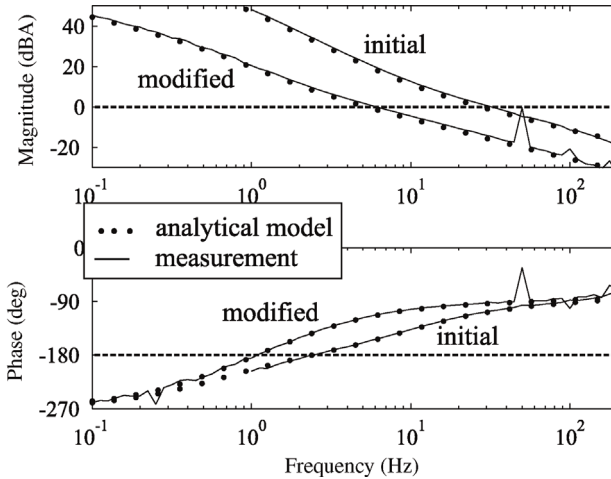
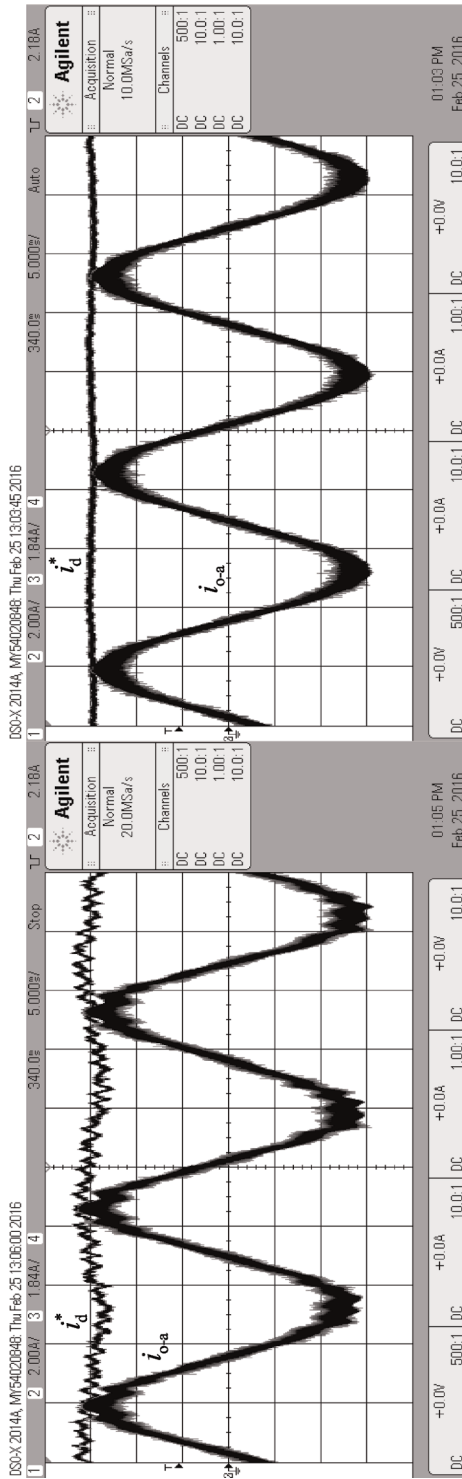


Figure 13.57 Original and redesigned input voltage control loop gains.

Figure 13.58a shows a distorted current where the reference has a lot of noise and a large 50 Hz component. In the example case, the 50 Hz noise originates from the laboratory environment since the grid emulator was operated at 60 Hz. That is, the utility grid in which the laboratory is connected to has a fundamental frequency of 50 Hz. As discussed previously, the noise in the reference produces distortion in the output current at $60 - 50 = 10$ Hz and $60 + 50 = 110$ Hz; the main reason why the phase current was of poor quality. Moreover, the DC voltage contains harmonics due to the dead-time effect that further reduces power quality. The problem can be effectively mitigated by reducing the crossover frequency of the input voltage control loop. The redesigned controller attenuates noise at 50 Hz, 10 times better than the initial loop gain, as its magnitude in Figure 13.57 is 20 dB less at 50 Hz. The reference in Figure 13.58b has a significantly cleaner waveform since the 50 Hz component and harmonics caused by dead-time are diminished. Therefore, the output current waveform has much less distortion. Note that similar problems occur when grid voltages are unbalanced. Unbalanced grid voltages produce ripple in the DC voltage at twice the fundamental frequency that may corrupt the reference of the current d-component.

The output current control loop gains were measured using the same principle as in Figure 13.59. The measured and predicted current control loop gains are as shown in Figure 13.11 when the inverter is operated at the MPP. The crossover frequency is slightly less than 1 kHz, that is, in reality the crossover frequency is approximately 800 Hz. This is due to the fact that the effect of the isolation transformer was not taken into account in the small-signal model. The isolation transformer has some inductance that decreases the crossover frequency through load effect.

Stability of the cascaded control system was evaluated by making a step change to the input voltage reference from 400 to 500 V. The step response of the input voltage is as shown in Figure 13.60. Even though the input voltage control was made slower, the input voltage reaches its new reference in approximately 300 ms, which is equivalent to 18 periods of the fundamental grid voltage. The step response of the



(a) (b)
Figure 13.58 Output current waveform and d-current reference (a) before and (b) after the modification of voltage controller parameters.

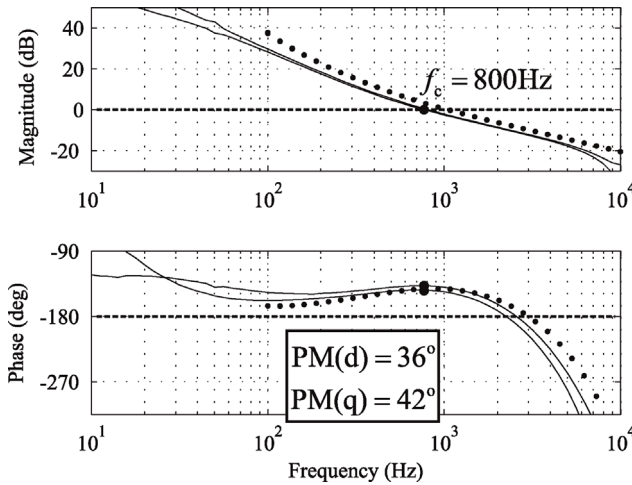


Figure 13.59 Measured and predicted output current control loop gains.

input voltage could be made faster if the reference of the output current d-component would be allowed to drop below zero. However, in the current case, the input capacitor charges according to available power from the PV simulator, that is, the charging current is limited by the short-circuit current of the PV simulator. Moreover, the inverter usually has a voltage boosting DC–DC converter that is responsible of maximum power point tracking and the reference of the inverter is kept constant. Thus, the settling speed is considered adequate.

Output currents of the inverter are shown in Figure 13.61 during the step test. The voltage controller drops the reference of the d-component quickly to zero and no power is transferred to the grid. Moreover, the inverter operates at unity power factor and current q-component is zero. The output currents are stable, new operating point is reached smoothly, and no excessive overcurrents are observed.

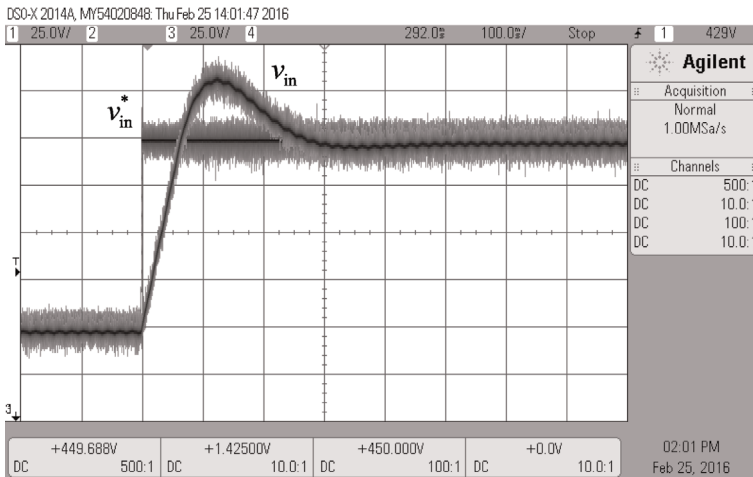


Figure 13.60 Step response of input voltage.

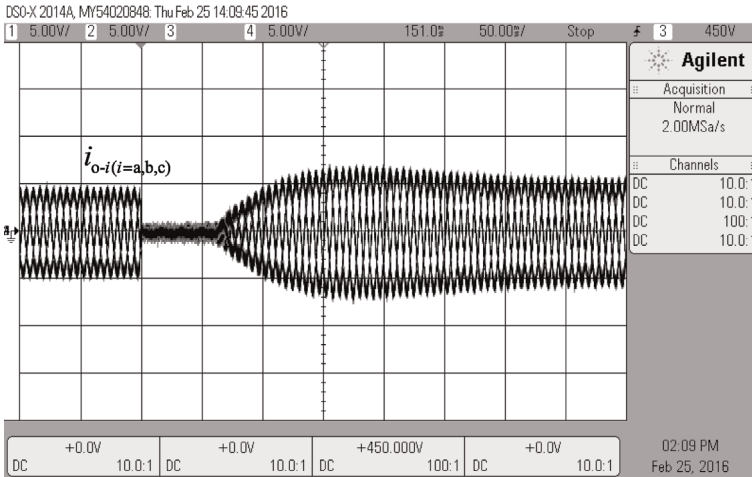


Figure 13.61 Step response of output currents.

Until now the inverter has been analyzed and operated at unity power factor. However, the inverter can also be used to supply or draw reactive power from the grid. The performance q-current control was tested by making a step change in its reference from 0 to 3 A. The step response is shown in Figure 13.62. Speed of the current control is evident from the measured waveforms, that is, the current q-component settles around the new steady state in less than 2 ms, which is roughly one tenth of the period of fundamental component of grid voltage. As can be seen in the figure, the current is in phase with the grid voltage before the step changes, as the q-current reference is equal to zero. After the positive step change in q-current reference, the inverter supplies reactive power to the grid as the phase current leads the phase voltage.

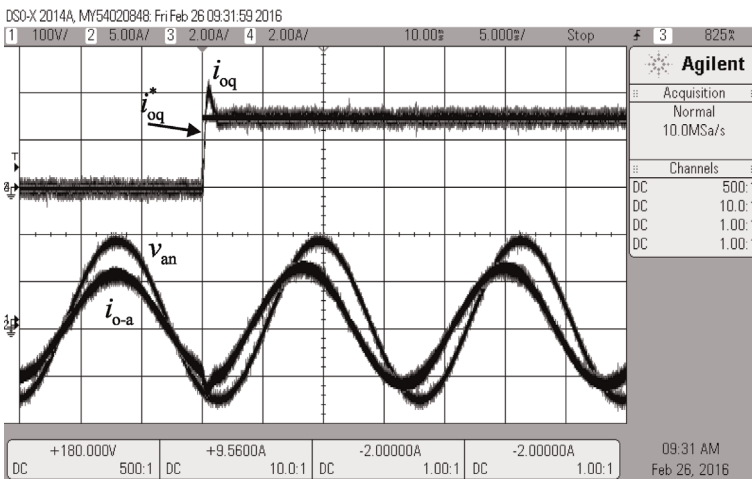


Figure 13.62 Step response of output current q-component.

13.7 Case Study: Instability Due to RHP-Pole

Crossover frequency of the input voltage control loop was intentionally reduced to demonstrate the unstable behavior caused by the RHP-pole in control dynamics. It should be noted that the control system could also be destabilized by reducing the DC capacitance or increasing the source current. Figure 13.63 shows the predicted input voltage loop gain when the controller gain K in (13.66) is reduced to one tenth of its original value. The crossover frequency is set to 1 Hz and the phase margin is effectively zero. Thus, the control loop is marginally stable.

Current and phase voltage in phase A are shown in Figure 13.64. The grid current has a large low-frequency component superimposed to its amplitude. A

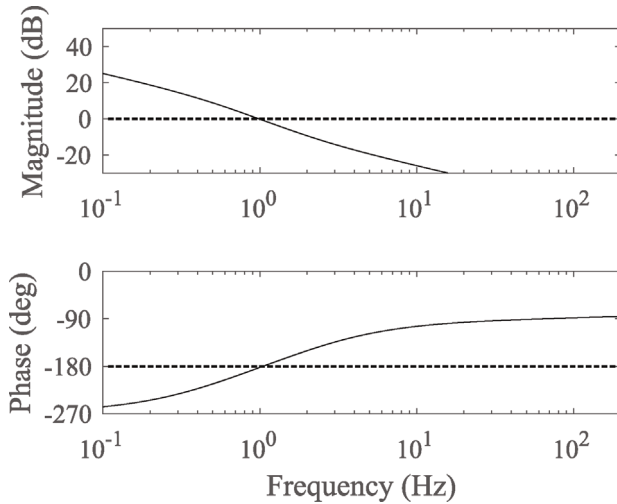


Figure 13.63 Predicted unstable loop gain.

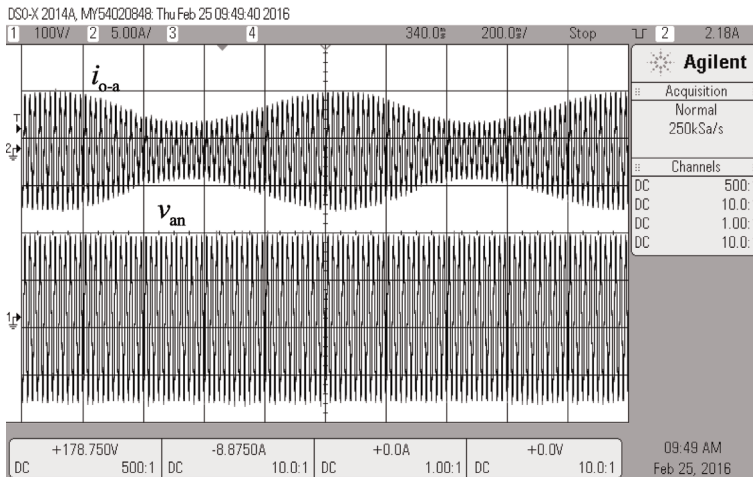
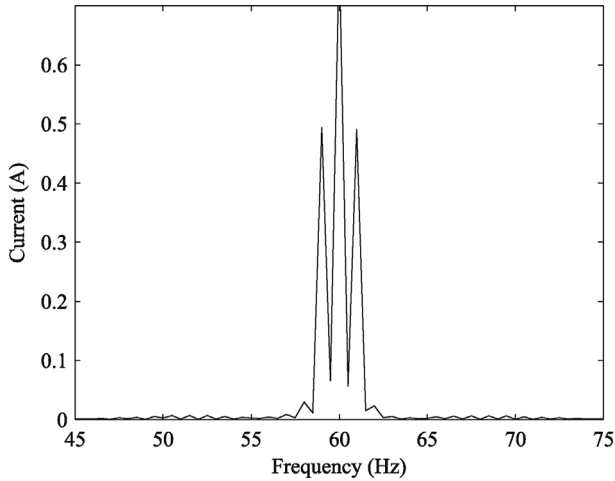
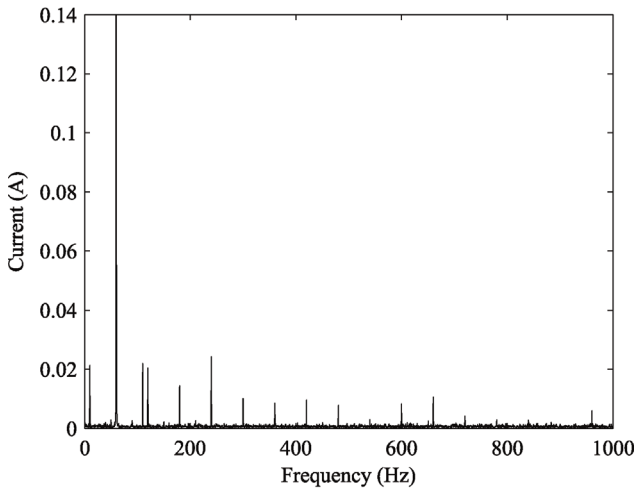


Figure 13.64 Instability due to RHP-pole in input voltage control loop.



(a)



(b)

Figure 13.65 FFT of the grid current in (a) unstable and (b) stable cases.

closer look to the spectrum of the phase current in Figure 13.65a reveals that the grid current contains significant amount of distortion at 59 and 61 Hz that is in-line with Eq. (13.64).

Figure 13.66 shows the current and voltage of phase A when the inverter is operated at the MPP with the same control parameters. The current is stable and does not include excessive low- or high-frequency harmonics, except some harmonics due to measurement noise and dead time effect. The spectrum of the phase current is as shown in Figure 13.65b. Evidently, the source impedance, that is, the dynamic resistance of PV generator, has a significant effect on the inverter stability. However, its effect on the control dynamics can be evaluated

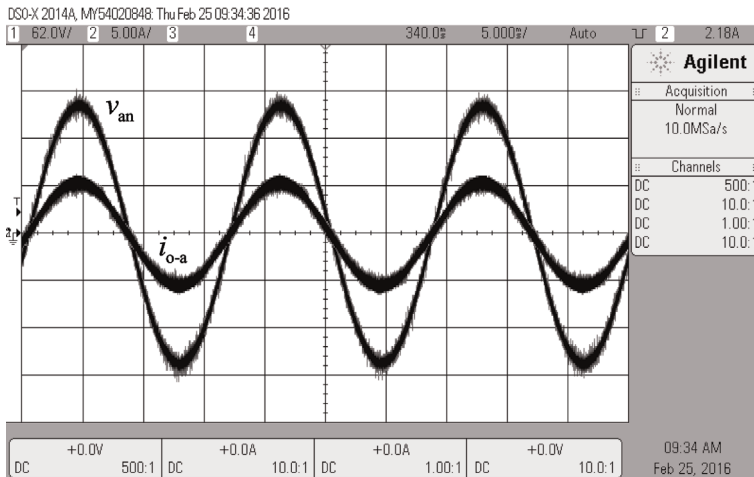


Figure 13.66 Grid current and phase voltage at the MPP.

by solving the source-affected transfer functions according to methods presented in Chapter 12.

13.8 Summary

In this chapter it has been shown that the dynamic modeling method can be effectively used to design stable control loops for grid-connected three-phase inverters. The control design has been verified by frequency response measurements and time-domain tests. A grid-connected photovoltaic inverter was used as a case study. The inverter was shown to become unstable due to an inherent RHP-pole in the control dynamics. Instability can be prevented by utilizing the presented dynamic model.

References

- 1 Begovic, M.M., Djuric, P.M., Dunlap, S., and Phadke, A.G. (1993) Frequency tracking in power networks in the presence of harmonics. *IEEE Trans. Power Deliv.*, **8** (2), 480–486.
- 2 Hsieh, G. (1996) Phase-locked loop techniques – a survey. *IEEE Trans. Ind. Electron.*, **43** (6), 609–615.
- 3 Kaura, V. and Blasko, V. (1997) Operation of a phase locked loop system under distorted utility conditions. *IEEE Trans. Ind. Appl.*, **33** (1), 58–63.
- 4 Cespedes, M. and Sun, J. (2014) Impedance modeling and analysis of grid-connected voltage-source converters. *IEEE Trans. Power Electron.*, **29** (3), 1254–1261.
- 5 Messo, T., Jokipii, J., Makinen, A., and Suntio, T. (2013) Modeling the grid synchronization induced negative-resistor-like behavior in the output

- impedance of a three-phase photovoltaic inverter. 2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 1–7.
- 6 Wen, B., Dong, D., Boroyevich, D., Burgos, R., Mattavelli, P., and Shen, Z. (2016) Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters. *IEEE Trans. Power Electron.*, **31** (1), 26–38.
 - 7 Rodriguez, P., Sainz, L., and Bergas, J. (2002) Synchronous double reference frame PLL applied to a unified power quality conditioner. *10th International Conference on Harmonics and Quality of Power*, IEEE, 2, pp. 614–619.
 - 8 Rodriguez, P., Teodorescu, R., Candela, I., Timbus, A.V., Liserre, M., and Blaabjerg, F. (2006) New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions. 37th IEEE Power Electronics Specialists Conference, pp. 1–7.
 - 9 Chung, S.K. (2000) A phase tracking system for three phase utility interface inverters. *IEEE Trans. Power Electron.*, **15** (3), 431–438.
 - 10 Castello, J. and Espi, J.M. (2012) DSP implementation for measuring the loop gain frequency response of digitally controlled power converters. *IEEE Trans. Power Electron.*, **27** (9), 4113–4121.
 - 11 Moran, L., Ziogas, P.D., and Joos, G. (1992) Design aspects of synchronous PWM rectifier-inverter systems under unbalanced input voltage conditions. *IEEE Trans. Ind. Appl.*, **28** (6), 1286–1293.
 - 12 Timbus, A., Liserre, M., Teodorescu, R., Rodriguez, P., and Blaabjerg, F. (2009) Evaluation of current controllers for distributed power generation systems. *IEEE Trans. Power Electron.*, **24** (3), 654–664.
 - 13 Teodorescu, R., Blaabjerg, F., Liserre, M., and Loh, P.C. (2006) Proportional-resonant controllers and filters for grid-connected voltage-source converters. *IEE Proc. Electr. Power Appl.*, **153** (5), 750.
 - 14 Rawlings, J.B. (2000) Tutorial overview of model predictive control. *IEEE Control Syst. Mag.*, **20** (3), 38–52.
 - 15 Rodriguez, J., Pontt, J., Silva, C.A., Correa, P., Lezana, P., Cortes, P., and Ammann, U. (2007) Predictive current control of a voltage source inverter. *IEEE Trans. Ind. Electron.*, **54** (1), 495–503.
 - 16 Zeng, Q. and Chang, L. (2008) An advanced SVPWM-based predictive current controller for three-phase inverters in distributed generation systems. *IEEE Trans. Ind. Electron.*, **55** (3), 1235–1246.
 - 17 Kouro, S., Cortes, P., Vargas, R., Ammann, U., and Rodriguez, J. (2009) Model predictive control – a simple and powerful method to control power converters. *IEEE Trans. Ind. Electron.*, **56** (6), 1826–1838.
 - 18 Akagi, H., Watanabe, E.H., and Aredes, M. (2007) Instantaneous Power Theory and Applications to Power Conditioning.
 - 19 Mao, H., Boroyevich, D., and Lee, F.C. (1998) Novel reduced-order small-signal model of a three-phase PWM rectifier and its application in control design and system analysis. *IEEE Trans. Power Electron.*, **13** (3), 511–521.
 - 20 Harnefors, L. (2007) Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices. *IEEE Trans. Ind. Electron.*, **54** (4), 2239–2248.

- 21 Espinoza, J.R., Joos, G., Perez, M., and Moran, T.L.A. (2000) Stability issues in three-phase PWM current/voltage source rectifiers in the regeneration mode. *ISIE'2000. Proceedings of the 2000 IEEE International Symposium on Industrial Electronics (Cat. No.00TH8543)*, IEEE, 2, pp. 453–458.
- 22 Skogestad, S. and Postlethwaite, I. (1998) *Multivariable Feedback Control: Analysis and Design*, John Wiley & Sons Ltd., Chichester.
- 23 Messo, T., Jokipii, J., Puukko, J., and Suntio, T. (2014) Determining the value of DC-link capacitance to ensure stable operation of a three-phase photovoltaic inverter. *IEEE Trans. Power Electron.*, **29** (2), 665–673.

14

Reduced-Order Closed-Loop Modeling of Inverters

14.1 Introduction

This chapter provides methods to develop closed-loop inverter models that include the dynamics of mostly used voltage and current control functions. Closed-loop models of voltage- and current-fed inverters are developed with L- and LCL-type output filters with passive components. Basic control functions such as AC current, DC voltage control, grid synchronization, that is, the SRF-PLL, and grid voltage feedforward are included in the dynamic model. Derivation of closed-loop model starts by studying the voltage-fed inverter with L-type filter since this is easiest to understand due to simple dynamic model. Derivation of more complex closed-loop models, such as current-fed inverter with LCL, follows exactly the same steps, the only difference being the more complex dynamics as the number of open-loop transfer functions increases.

Closed-loop models produce a lot of useful information for a design engineer, whether working with power stage, control design, or system-level issues. Most useful outcomes of the closed-loop model are evidently DC and AC side impedances that can be used to evaluate impedance-based stability and response of the inverter to harmonic distortion in grid voltages. Moreover, closed-loop models can be used to characterize how disturbances are reflected through the inverter, for example, from AC to DC voltage.

14.2 Reduced-Order Model of Voltage-Fed Inverter

From here on, it will be assumed that the control design of the inverter is made based on the loop-shaping method discussed in Chapter 13. Therefore, all control loops are assumed to be stable.

The aim in developing the closed-loop model is simply to merge the control functions and all the associated sensing and modulator gains with the open-loop dynamics presented in Chapter 12. In this chapter, the transfer functions developed in Chapters 12 and 13 are merged into a model that represents the closed-loop behavior of the inverter in the frequency domain.

14.2.1 Closed-Loop Model with AC Current Control

The reduced-order control block diagrams of a voltage-fed inverter with L-type output filter were depicted in Figures 13.21 and 13.22 for output and input dynamics. To find out the closed-loop transfer functions, one should first solve the block diagrams that include the inner-most control loops. In the case of voltage-fed inverter, the output dynamics are solved first. The input variables are the input voltage \hat{v}_{in} , output voltage d and q-components \hat{v}_{od} and \hat{v}_{oq} , respectively, and output current reference values \hat{i}_{od}^* and \hat{i}_{oq}^* . The output variables are the output current d and q-components \hat{i}_{od} and \hat{i}_{oq} and input current \hat{i}_{in} . Developing the closed-loop model requires solving transfer functions between all input and output variables. Output dynamics can be solved from the block diagram of Figure 13.21 and given as

$$\hat{i}_{od} = \frac{G_{iod-o}}{(1 + L_{out-d})} \hat{v}_{in} - \frac{Y_{odd-o}}{(1 + L_{out-d})} \hat{v}_{od} + \frac{1}{H_d} \cdot \frac{L_{out-d}}{(1 + L_{out-d})} \hat{i}_{od}^*, \quad (14.1)$$

$$\hat{i}_{oq} = \frac{G_{ioq-o}}{(1 + L_{out-q})} \hat{v}_{in} - \frac{Y_{oqq-o}}{(1 + L_{out-q})} \hat{v}_{oq} + \frac{1}{H_q} \cdot \frac{L_{out-q}}{(1 + L_{out-q})} \hat{i}_{oq}^*, \quad (14.2)$$

where the current control loop gains are defined as

$$L_{out-d} = G_{codd-o} G_{SPWM} G_{PI-d} H_d, \quad (14.3)$$

$$L_{out-q} = G_{coqq-o} G_{SPWM} G_{PI-q} H_q. \quad (14.4)$$

The transfer functions from input voltage to output current correspond to closed-loop input-to-output transfer function. Transfer function from output voltage to output current corresponds to output admittance. Transfer function from reference to output current corresponds to a transfer function often referred to as the “closed-loop transfer function” in control engineering that can be used to determine the control bandwidth. The closed-loop output dynamics can be simply written as

$$\hat{i}_{od} = G_{iod-c} \hat{v}_{in} - Y_{odd-c} \hat{v}_{od} + G_{codd-c} \hat{i}_{od}^*, \quad (14.5)$$

$$\hat{i}_{oq} = G_{ioq-c} \hat{v}_{in} - Y_{oqq-c} \hat{v}_{oq} + G_{coqq-c} \hat{i}_{oq}^*, \quad (14.6)$$

where the subscript “c” is used to define that the transfer function represents closed-loop dynamics.

Closed-loop input dynamics can be solved from the control block diagram in Figure 13.22 by substituting the output dynamics in Eq. (14.1) as the output current \hat{i}_{od} . Note that it is assumed that input dynamics depend mainly on d-components and cross-coupling transfer functions can be neglected [1]. The closed-loop input dynamics can be given as follows:

$$\begin{aligned} \hat{i}_{in} = & \left(Y_{in-o} - \frac{G_{cid-o} G_{iod-o}}{G_{codd-o}} \cdot \frac{L_{out-d}}{(1 + L_{out-d})} \right) \hat{v}_{in} + \left(T_{oid-o} + \frac{G_{cid-o} Y_{odd-o}}{G_{codd-o}} \cdot \frac{L_{out-d}}{(1 + L_{out-d})} \right) \hat{v}_{od} \\ & + \left(\frac{1}{H_d} \cdot \frac{G_{cid-o}}{G_{codd-o}} \cdot \frac{L_{out-d}}{(1 + L_{out-d})} \right) \hat{i}_{od}^*, \end{aligned} \quad (14.7)$$

which can be written as

$$\hat{i}_{in} = Y_{in-c}\hat{v}_{in} + T_{oid-c}\hat{v}_{od} + G_{cid-c}\hat{i}_{od}^* \quad (14.8)$$

The closed-loop transfer functions derived from the reduced-order control block diagrams can be represented as

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} = \begin{bmatrix} Y_{in-c} & T_{oid-c} & \dots & G_{cid-c} & \dots \\ G_{iod-c} & -Y_{odd-c} & \dots & G_{codd-c} & \dots \\ G_{ioq-c} & \dots & -Y_{oqq-c} & \dots & G_{coqq-c} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{i}_{od}^* \\ \hat{i}_{oq}^* \end{bmatrix} \quad (14.9)$$

As can be seen from Eq. (14.9), the reduced-order model does not provide information on cross-admittance terms, how the q-components affect input dynamics, or how the changes in current reference values affect the output currents between the d and q-components. However, it is often enough to consider the output admittance d and q-components when determining impedance-based interactions in the grid side [2]. Moreover, input admittance depends mainly on the d-components at unity power factor allowing the model to be used for stability analysis at the DC side.

The effect of output current control on the magnitude of output admittance can be determined by studying the closed-loop output admittances Y_{odd-c} and Y_{oqq-c} that are defined as follows:

$$Y_{odd-c} = \frac{Y_{odd-o}}{(1 + L_{out-d})}, \quad (14.10)$$

$$Y_{oqq-c} = \frac{Y_{oqq-o}}{(1 + L_{out-q})}. \quad (14.11)$$

The current control loop gains affect the denominator of the transfer function. Therefore, the larger the magnitude of the loop gain at a specific frequency, the smaller the magnitude of output admittance. Figure 14.1 shows the output admittance d-component Y_{odd-c} when current control is tuned to have a crossover frequency of 1 kHz and phase margin of 65°. The admittances are extracted from the simulation model studied in Section 13.3.2. The second frequency response in Figure 14.1 illustrates the output admittance when current crossover is reduced to 500 Hz while keeping the same phase margin. It is evident that high bandwidth current control provides an output admittance with low magnitude that makes the inverter less prone to grid-induced interactions.

Figure 14.2 shows the equivalent impedances, that is, $Z_{odd-c} = 1/Y_{odd-c}$ since impedance provides better physical interpretation. From here on, admittances are presented as impedances to enhance readability. As stated earlier, an ideal current source should have infinite output impedance. Increasing the crossover frequency of current control indeed makes the inverter behave more like an ideal current source as the output impedance increases in magnitude. Grid-connected inverter operating in output-current-control mode should have as large output impedance as possible to avoid impedance-based interactions [3] and to prevent

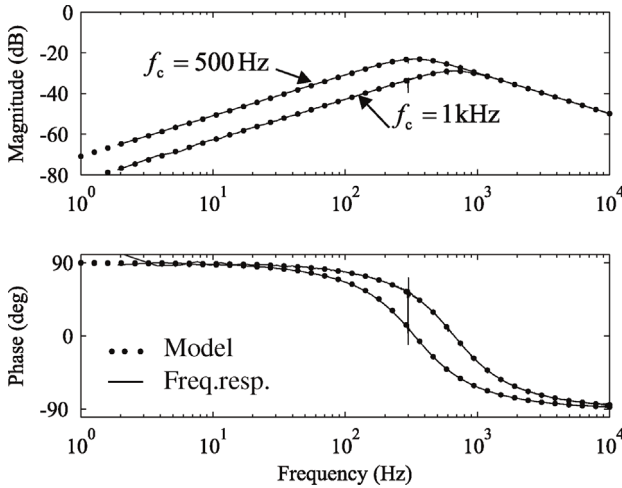


Figure 14.1 Output admittance d-component $Y_{\text{odd-c}}$ with two different current controller settings.

amplification of harmonic distortion. It is not, however, possible to make the current control infinitely fast because in practical applications, control delay can destabilize the control system.

To be specific, output current control makes the inverter output impedance capacitive within the bandwidth of current control while it remains inductive outside the bandwidth due to the L-type output filter. In between the capacitive and inductive regions, there is a region where impedance behaves as a resistor that is determined by the PI controller parameters. The output impedance can, therefore, be approximated as a series RLC circuit equivalent to Figure 14.3,

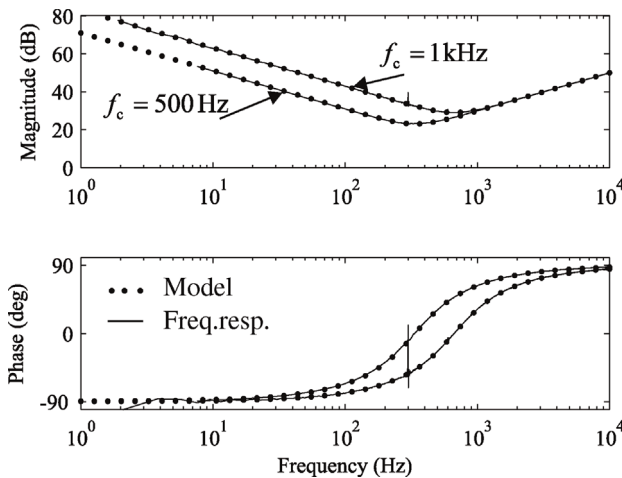


Figure 14.2 Output impedance d-component $Z_{\text{odd-c}}$ with two different current control crossovers.

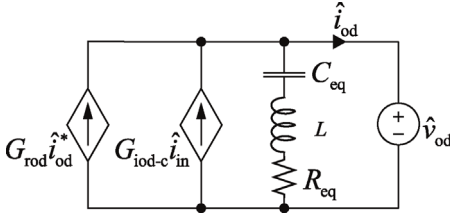


Figure 14.3 Linearized output dynamics of output current d-component.

however, this applies only to the output impedance d-component because the q-component is affected by the SRF-PLL.

The symbolic form of the closed-loop output impedance can be solved by using the Symbolic Toolbox of MATLAB. Parasitic resistances of the output filter will be neglected to simplify the analysis since their effect is anyway enclosed inside the frequencies where current controller dominates over the output impedance. Moreover, ideal measurement circuits and zero control delay are assumed. The equivalent series RLC circuit can be given as in Eq. (14.12) where K_{CC} is the controller gain and ω_{z-CC} is the controller zero that are selected according to (13.31). The controller transfer function is defined as $G_{CC} = K_{CC}(s/\omega_{z-CC} + 1)/s$.

$$Z_{odd-c} = L_{eq}s + \frac{1}{C_{eq}s} + R_{eq} = Ls + \frac{1}{(L\omega_s^2 + K_{CC}V_{in})^{-1}s} + \frac{K_{CC}V_{in}}{\omega_{z-CC}}. \quad (14.12)$$

The analytical impedance already given is very user-friendly in terms of checking the shape of output impedance d-component during control design without the need to derive the whole dynamic model.

14.2.2 Closed-Loop Model with SRF-PLL

The phase-locked-loop affects the output admittance of the voltage-fed inverter and its effect should be included in the closed-loop model. The effect of grid synchronization can be included in the model by utilizing the linearized model of the PLL in Figure 13.5. Figure 14.4 depicts the closed-loop dynamics of the q-channel. From the small-signal viewpoint, the control system inside the dashed rectangle rotates in its own reference frame that is coupled in the ideal grid reference frame by the PLL. It is pointed out that the signals going from reference frame to another are equal in their steady-state values but not by their small-signal content, which is why there are additional signal paths from the grid voltage q-component to duty ratio and the sensed current.

The relationship between variables in the two reference frames, that is, the control system reference frame and the ideal grid voltage reference frame can be obtained by applying Eq. (13.8) to each of the d- and q-components. The currents and duty ratios can be given in the control system reference frame according to Eqs. (14.13) and (14.14). It is assumed that the PLL works as intended, that is, the sensed voltage q-component V_{oq} equals to zero, and that the inverter operates at the unity power factor, that is, the output current q-component I_{oq} is equal to zero. Moreover, it is assumed that the duty ratio q-component D_q is small enough

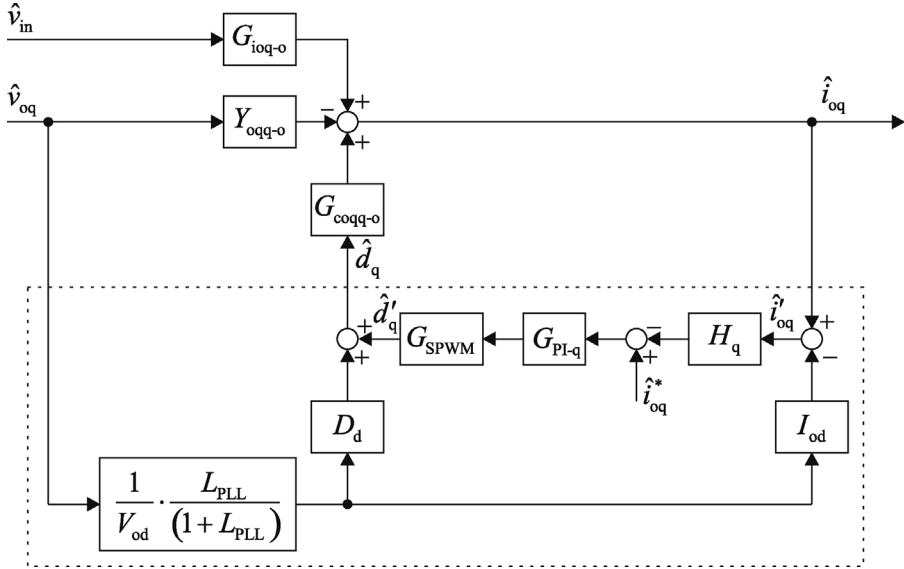


Figure 14.4 Output dynamics related to the q-components with SRF-PLL.

in value to be neglected. Therefore, the PLL affects only the q-components and the impedance d-component can be given as in Eq. (14.12).

$$\hat{i}'_{od} = \hat{i}_{od}, \quad \hat{d}'_d = \hat{d}_d. \quad (14.13)$$

$$\hat{i}'_{oq} = \hat{i}_{oq} - \frac{I_{od}}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{oq}, \quad \hat{d}'_q = \hat{d}_q - \frac{D_d}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{oq}. \quad (14.14)$$

The closed-loop dynamics can be solved from the block diagram in Figure 14.4 and given as

$$\begin{aligned} \hat{i}_{oq} &= \frac{G_{ioq-o}}{(1 + L_{out-q})} \hat{v}_{in} + \frac{1}{H_q} \cdot \frac{L_{out-q}}{(1 + L_{out-q})} \hat{i}_{oq}^* \\ &\quad - \left(\frac{Y_{oqq-o}}{(1 + L_{out-q})} - \frac{I_{od}}{V_{od}} \cdot \frac{L_{out-q}}{(1 + L_{out-q})} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} - \frac{D_d}{V_{od}} \cdot \frac{G_{coqq-o}}{(1 + L_{out-q})} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \right) \hat{v}_{oq} \\ &= G_{ioq-c} \hat{v}_{in} + G_{coqq-c} \hat{i}_{oq}^* - Y_{oqq-c} \hat{v}_{oq}. \end{aligned} \quad (14.15)$$

The closed-loop output admittance is defined as in Eq. (14.16) from which the effect of SRF-PLL can be identified. The current control works in the same way as in the case of output admittance d-component, that is, the effect of open-loop output admittance is diminished at frequencies where current control loop gain has large magnitude. However, the second admittance term is produced by the grid synchronization that introduces a parallel negative resistance equal to $-V_{od}/I_{od}$, that is, the term produces a pure resistance at frequencies where

both loop gains $L_{\text{out-q}}$ and L_{PLL} have large magnitudes [4–7]. Having a sum of admittances is equivalent to having two admittances in parallel.

$$Y_{\text{oqq-c}} = \frac{Y_{\text{oqq-o}}}{(1+L_q)} - \frac{I_{\text{od}}}{V_{\text{od}}} \cdot \frac{L_{\text{out-q}}}{(1+L_{\text{out-q}})} \cdot \frac{L_{\text{PLL}}}{(1+L_{\text{PLL}})} - \frac{D_d}{V_{\text{od}}} \cdot \frac{G_{\text{coqq-o}}}{(1+L_{\text{out-q}})} \cdot \frac{L_{\text{PLL}}}{(1+L_{\text{PLL}})} \quad (14.16)$$

Output impedance q-component ($Z_{\text{oqq-c}} = 1/Y_{\text{oqq-c}}$) with two different current control settings is shown in Figure 14.5 when the PLL is tuned to have a crossover frequency of 100 Hz. The impedance behaves as a negative resistor at low frequencies as can be deduced based on Eq. (14.16). Moreover, the current control does not affect the low-frequency behavior where the phase remains close to -180° regardless of the current controller parameters. The model gives accurate predictions on the shape of the impedance without making the model very complex and, thus can be used in impedance-based stability analysis.

Output impedance q-component is shown in Figure 14.6 for two different values of PLL crossover frequency, that is, when the PLL is tuned to have 100 and 20 Hz crossover. Phase margin is set to 65° in both cases. It is evident that the crossover frequency of the PLL has a dominant effect on the impedance behavior at low frequencies. The negative resistor-like behavior is known to cause instability, especially, in inductive and weak grids. Therefore, the speed of grid synchronization should be limited. It is a common practice to select the crossover frequency of the PLL in the range of few tens of Hertz. Faster grid synchronization makes the inverter more vulnerable to instability caused by impedance-based interactions that is treated more in detail in Chapter 16.

The impedance q-component is found out to consist of two components connected in parallel when symbolic analysis is applied. The first term originates from the current control and can be given as in Eq. (14.17). The impedance is

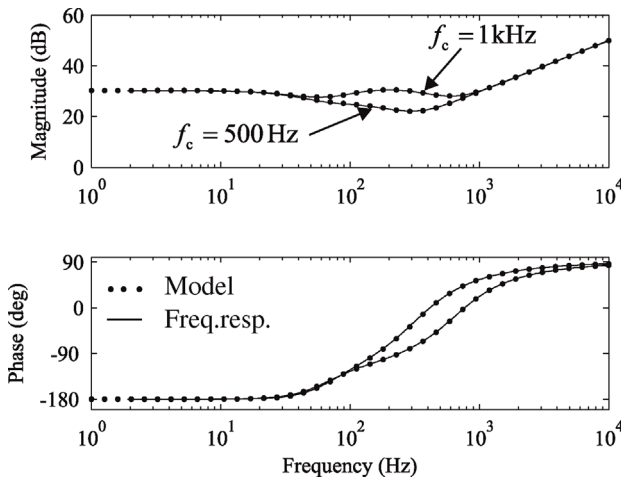


Figure 14.5 Output impedance q-component $Z_{\text{oqq-c}}$ with two current control crossover frequencies.

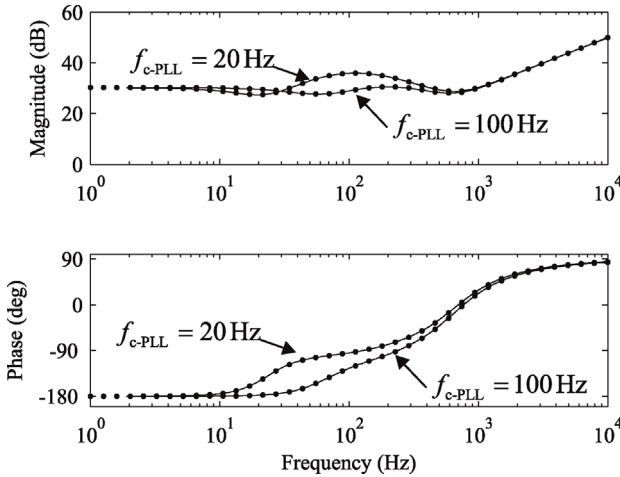


Figure 14.6 Output impedance q-component Z_{oqq-c} with two different PLL settings.

identical to the d-component, that is, it constitutes of a series RLC branch.

$$Z_{oqq-CC} = Ls + \frac{1}{(L\omega_s^2 + K_{CC}V_{in})^{-1}s} + \frac{K_{CC}V_{in}}{\omega_{z-CC}} = L_{eq}s + \frac{1}{C_{eq}s} + R_{eq}. \tag{14.17}$$

The PLL produces an additional parallel impedance component, which can be given as in Eq. (14.18). The negative resistance is caused by the control system and cannot be easily represented using passive components as in the case of the output impedance d-component. The equivalent linear circuit that presents the dynamic behavior of the q-components can be depicted as in Figure 14.7. The output impedance has the same branch made of passive components as in Fig. 14.7. However, the PLL introduces a parallel branch that can be given as in Eq. (14.18).

$$Z_{oqq-PLL} = -\frac{I_{od}K_{CC}K_{PLL}V_{in}(s + \omega_{z-CC})(s + \omega_{z-PLL})}{(\omega_{z-PLL}s^2 + K_{PLL}V_{od}s + K_{PLL}V_{od}\omega_{z-PLL})(L\omega_{z-CC}s^2 + K_{CC}V_{in}s + K_{CC}V_{in}\omega_{z-CC} + L\omega_{z-CC}\omega_s^2)}. \tag{14.18}$$

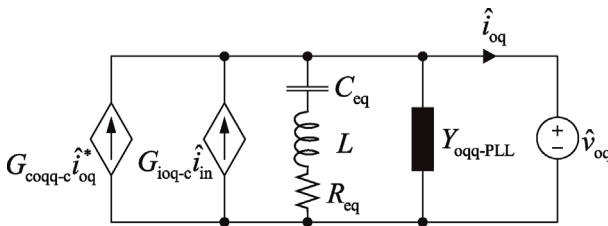


Figure 14.7 Linearized output dynamics of output current q-component.

14.2.3 Closed-Loop Input Admittance

The closed-loop input dynamics can be solved by assuming that the input dynamics depend only on the d-components and that the cross-coupling transfer functions can be neglected. The closed-loop input admittance can be given as in Eq. (14.19).

$$Y_{in-c} = Y_{in-o} - \frac{G_{cid-o}G_{iod-o}}{G_{codd-o}} \cdot \frac{L_{out-d}}{(1 + L_{out-d})}. \quad (14.19)$$

The input admittance can be represented as in Eq. (14.20) to evaluate the effect of control loop gains on the shape of the admittance. The open-loop transfer functions inside the parentheses can be collected to form a special parameter $Y_{in-\infty}$ that will serve as a good shortcut for approximating the admittance behavior inside the current control bandwidth. The term $Y_{in-\infty}$ dominates the shape of the input admittance at frequencies where current control has high gain, that is, at frequencies where the term $L_{out-d}/(1 + L_{out-d})$ is close to unity.

$$\begin{aligned} Y_{in-c} &= \frac{Y_{in-o}}{(1 + L_{out-d})} + \frac{L_{out-d}}{(1 + L_{out-d})} \left(Y_{in-o} - \frac{G_{cid-o}G_{iod-o}}{G_{codd-o}} \right) \\ &= \frac{Y_{in-o}}{(1 + L_{out-d})} + \frac{L_{out-d}}{(1 + L_{out-d})} Y_{in-\infty}. \end{aligned} \quad (14.20)$$

The special parameter $Y_{in-\infty}$ can be solved symbolically and given as in Eq. (14.21) by noting that at unity power factor, the term $I_{Ld}L\omega_s D_q$ is equal to $-V_{in}D_q^2$. This can be verified by substituting the steady-state value of the duty ratio q-component in Eq. (14.21) according to the steady-state operating point solved earlier in Chapter 12.

$$Y_{in-\infty} = -\frac{3(D_d I_{Ld} L s - V_{in} D_q^2 + I_{Ld} L \omega_s D_q)}{2L V_{in} s} = -\frac{3D_d I_{Ld}}{2V_{in}} = -\frac{I_{in}}{V_{in}}. \quad (14.21)$$

The low-frequency value of the inverter input impedance can be given as in Eq. (14.22). The impedance corresponds to a negative static resistance that is a well-known property of a constant power load. Negative resistance due to constant power load characteristics has been discussed extensively in grid-connected rectifiers [8,9] and DC-DC systems. Thus, it is reasonable to expect similar dynamic behavior from an output-current-controlled voltage-fed inverter when studying its dynamics from the DC side.

$$Z_{in-c-LF} = -\frac{2V_{in}}{3D_d I_{Ld}} = -\frac{V_{in}}{I_{in}}. \quad (14.22)$$

Figure 14.8 shows the input impedance ($Z_{in-c} = 1/Y_{in-c}$) of the voltage-fed inverter when current control is tuned to have crossover frequencies of 1 kHz and 500 Hz. The reduced-order model gives accurate predictions on the shape of the input impedance at unity power factor, even though dynamics related to q-components are neglected. Moreover, the line marked using plus signs illustrates the admittance term defined in Eq. (14.21). It gives a good approximation of the low-frequency behavior of the impedance when only the operating point of

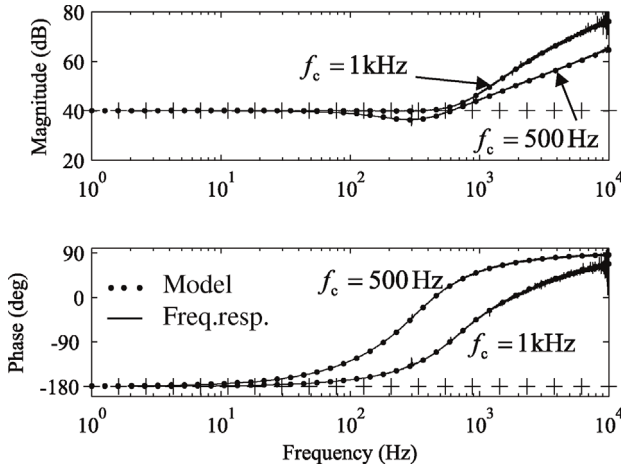


Figure 14.8 The effect of current control on voltage-fed inverter input impedance Z_{in-c} .

the inverter is known. Thus, one does not necessarily have to measure impedances to predict its low-frequency behavior, assuming that the control system is equivalent to the conventional current control in the dq-domain and PI-type controllers are used.

14.2.4 Output Impedance with Grid Voltage Feedforward

The principle of grid voltage feedforward was briefly introduced in Chapter 13. Grid voltage feedforward is implemented by measuring the grid voltage and adding its value to the duty ratios through a feedforward transfer function [10–13]. The value of feedforward gain should be selected close to the inverse of input voltage steady-state value $1/V_{in}$ in the case of a SPWM and inverter with L-filter. The feedforward loop can be included in the reduced-order control block diagram of the output current d-component as depicted in Figure 14.9, where G_{ffd} is the feedforward gain by which the grid voltage d-component is processed. Note that the following analysis does not apply for an inverter employing space-vector modulator where the reference vectors are normalized by DC voltage.

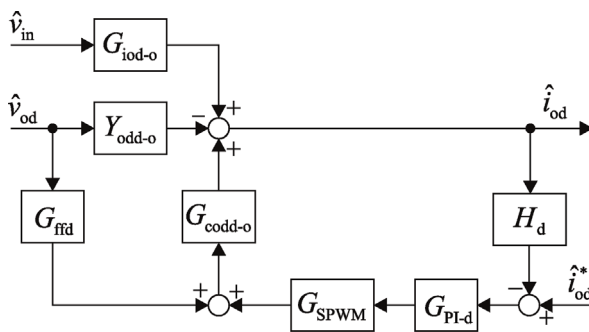


Figure 14.9 Control block diagram related to current d-component with grid voltage feedforward.

The closed-loop transfer functions can be solved from Figure 14.9 and given as

$$\begin{aligned}\hat{i}_{od} &= \frac{G_{iod-o}}{(1 + L_{out-d})} \hat{v}_{in} - \frac{(Y_{odd-o} - G_{codd-o} G_{ffd})}{(1 + L_{out-d})} \hat{v}_{od} + \frac{1}{H_d} \cdot \frac{L_{out-d}}{(1 + L_{out-d})} \hat{i}_{od}^* \\ &= G_{iod-c} \hat{v}_{in} - Y_{odd-c} \hat{v}_{od} + G_{codd-c} \hat{i}_{od}^*\end{aligned}\quad (14.23)$$

The feedforward gain G_{ffd} affects the closed-loop output admittance Y_{odd-c} as can be seen from Eq. (14.23). In fact, ideally the output admittance would be equal to zero when feedforward gain is selected as in Eq. (14.24). This suggests that the magnitude of output impedance d-component becomes infinite.

$$G_{ffd} = \frac{Y_{odd-o}}{G_{codd-o}} = \frac{1}{V_{in}}. \quad (14.24)$$

It is not possible to extract the impedance d-component from the simulator as its value is ideally infinite. However, its effect can be seen by making a perturbation on the grid voltage d-component and examining the effect of this disturbance on the output current d-component. Perturbation to the grid voltage d-component is equal to making a perturbation to amplitude of three-phase grid voltages. Figure 14.10 shows the grid voltage and current waveforms extracted from the simulator before and after activating the feedforward (in d-component). The peak value of three-phase grid voltage is modulated at 350 Hz with an amplitude equal to 10 V. Such modulation generates perturbation only in the d-components since the q-component of grid voltage space vector is defined equal to zero. This approach allows us to verify the effect of feedforward on the impedance d-component without the effect of cross-coupling or q-components of the inverter output impedance.

The grid currents have the same harmonic content as grid voltages prior to activating the feedforward. However, the grid currents become sinusoidal without any signs of harmonics after the feedforward is activated at 0.05 s. This simulation

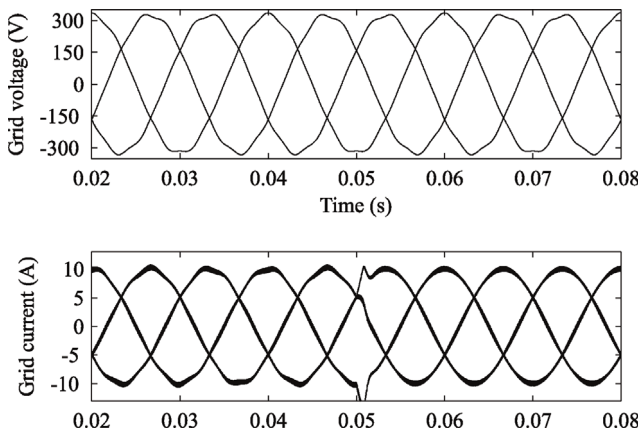


Figure 14.10 Grid currents when feedforward control is activated with gains $G_{ffd} = G_{ffq} = 1/V_{in}$.

study is of course a very theoretical case, but provides valuable insight on the effectiveness of feedforward in shaping the impedance d-component. Thus, ideally the impedance becomes infinite after activating feedforward. Therefore, the inverter does not generate any harmonic currents. Experimental results are presented later with a photovoltaic inverter since identical feedforward method is often utilized in renewable energy inverters.

In reality, various nonidealities affect the feedforward path that are not taken into account in the reduced-order model, such as delays and nonidealities associated with current/voltage sensing circuits. Moreover, the inverter may not always be operated at unity power factor. In addition, in current-fed inverter, the DC voltage control affects the low-frequency behavior of impedance d-component.

The feedforward gain should ideally be selected as the inverse of DC voltage. However, the impedance cannot be extracted from the simulator since it has ideally an infinite value. The feedforward gain was selected as $0.9/V_{in}$ to approximate the dynamic behavior when feedforward gain is close to the optimal value. Figure 14.11 depicts the impedance d-component when feedforward is disconnected, that is, $G_{ffd} = 0$ (lowest magnitude) and when the feedforward gain is selected as $0.9/V_{in}$ (highest magnitude) and as $0.5/V_{in}$. The DC voltage was set to 750 V to avoid overmodulation of the three-phase bridge during the frequency response measurement. Magnitude of impedance is maximized when feedforward gain is selected close to the optimal value. However, decreasing the feedforward gain or deactivating the feedforward control lowers the impedance magnitude significantly.

Increasing the feedforward gain beyond $1/V_{in}$ has detrimental effect on the impedance magnitude as well. Moreover, the impedance loses its passive features. Figure 14.12 shows the impedance d-component when feedforward gain is selected close to the optimal value as $0.9/V_{in}$ (largest magnitude), $1.5/V_{in}$ (center-most magnitude) and twice the optimal value as $2/V_{in}$ (lowest

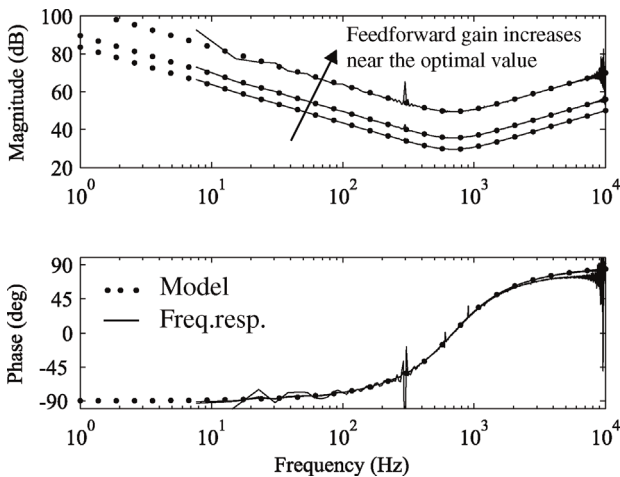


Figure 14.11 Output impedance d-component Z_{odd-c} with feedforward gains smaller than the optimal value.

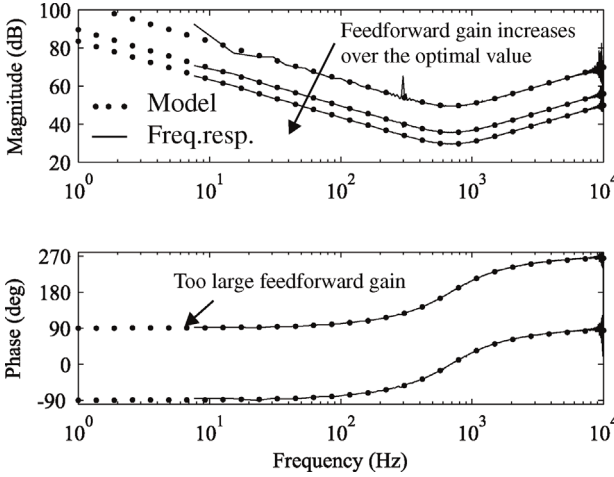


Figure 14.12 Output impedance d-component $Z_{\text{odd-c}}$ with feedforward gains larger than the optimal value.

magnitude). The phase of the impedance experiences a 180° shift upward when feedforward gain is larger than $1/V_{\text{in}}$. Thus, the phase does not stay within -90° and 90° and the impedance does not resemble a passive circuit. Such behavior can introduce impedance-based instability [8] and, therefore, too large feedforward gain should be avoided.

The effect of grid voltage feedforward on the impedance q-component can be evaluated by adding the feedforward path in the block diagram of Figure 14.4. According to Eq. (13.8), the sensed grid voltage d-component \hat{v}'_{oq} can be defined as in Eq. (14.25) based on which the control block diagram can be modified by adding the corresponding feedforward path as depicted in Figure 14.13.

$$\hat{v}'_{\text{oq}} = \hat{v}_{\text{oq}} - \frac{V_{\text{od}}}{V_{\text{od}}(1+L_{\text{PLL}})} L_{\text{PLL}} \hat{v}_{\text{oq}} = \left(1 - \frac{L_{\text{PLL}}}{(1+L_{\text{PLL}})}\right) \hat{v}_{\text{oq}}. \quad (14.25)$$

The closed-loop dynamics can be solved from the block diagram and given as

$$\hat{i}_{\text{oq}} = \frac{G_{\text{ioq-o}}}{(1+L_{\text{out-q}})} \hat{v}_{\text{in}} + \frac{1}{H_{\text{q}}} \frac{L_{\text{out-q}}}{(1+L_{\text{out-q}})} \hat{i}_{\text{oq}}^* - \left\{ \frac{Y_{\text{oq-q-o}} - (G_{\text{coq-q-o}} G_{\text{SPWM}} G_{\text{ffq}})/(1+L_{\text{PLL}})}{(1+L_{\text{out-q}})} - \frac{I_{\text{ld}}}{V_{\text{od}}} \frac{L_{\text{out-q}}}{(1+L_{\text{out-q}})} \frac{L_{\text{PLL}}}{(1+L_{\text{PLL}})} - \frac{D_{\text{d}}}{V_{\text{od}}} \frac{G_{\text{coq-q-o}}}{(1+L_{\text{out-q}})} \frac{L_{\text{PLL}}}{(1+L_{\text{PLL}})} \right\} \hat{v}_{\text{oq}}, \quad (14.26)$$

or in short as

$$\hat{i}_{\text{oq}} = G_{\text{ioq-c}} \hat{v}_{\text{in}} + G_{\text{ciq-c}} \hat{i}_{\text{oq}}^* - Y_{\text{oq-c}} \hat{v}_{\text{oq}}. \quad (14.27)$$

The output admittance q-component can be given as in Eq. (14.28) where the feedforward affects the admittance through the term $G_{\text{coq-q-o}} G_{\text{SPWM}} G_{\text{ffq}}/(1+L_{\text{PLL}})$. The effect of the open-loop admittance $Y_{\text{oq-q-o}}$ is canceled when the feedforward gain is selected as in Eq. (14.29). However, the feedforward does not affect the

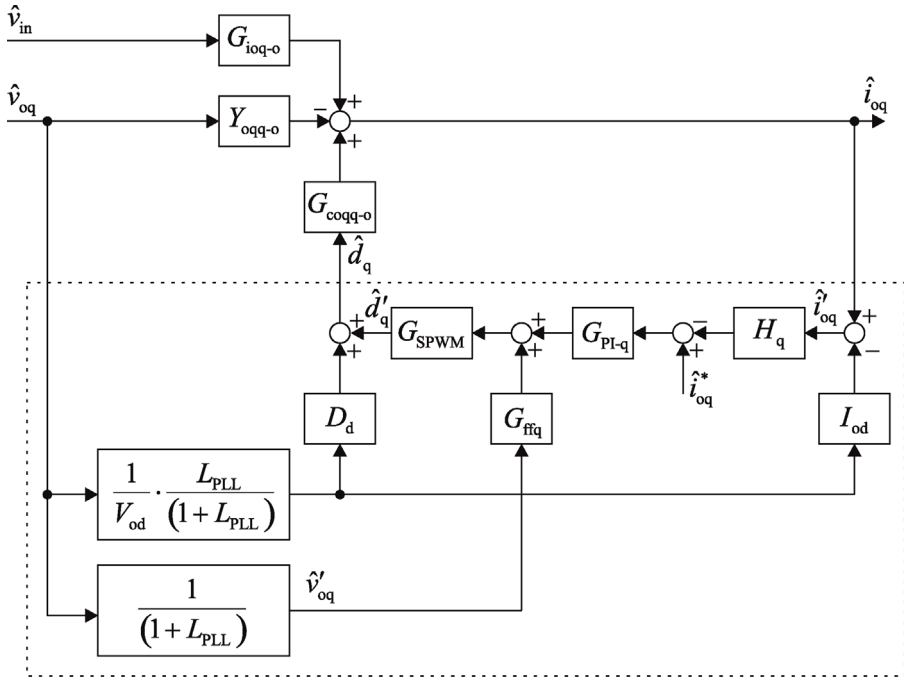


Figure 14.13 Control block diagram related to output current q-component with feedforward.

low-frequency impedance that is determined by the phase-locked loop. This can be deduced from Eq. (14.28) by noting that the feedforward term is divided by the PLL loop gain L_{PLL} .

$$Y_{oq-q-c} = \frac{1}{(1 + L_{out-q})} \left(Y_{oq-q-o} - \frac{G_{coq-q-o} G_{SPWM} G_{ffq}}{(1 + L_{PLL})} \right) - \frac{I_{Ld}}{V_{od}} \frac{L_{out-q}}{(1 + L_{out-q})} \frac{L_{PLL}}{(1 + L_{PLL})} - \frac{D_d}{V_{od}} \frac{G_{coq-q-o}}{(1 + L_{out-q})} \frac{L_{PLL}}{(1 + L_{PLL})}, \tag{14.28}$$

$$G_{ffq} = \frac{Y_{oq-q-o}}{G_{coq-q-o} G_{SPWM}} \approx \frac{1}{V_{in}}. \tag{14.29}$$

Figure 14.14 shows the impedance q-component when feedforward is initially deactivated (lowest magnitude) and feedforward gains of $0.5/V_{in}$ and $0.9/V_{in}$ are used. The impedance magnitude increases in value at high frequencies when the feedforward gain approaches the optimal value defined in Eq. (14.29). However, as deduced earlier, the feedforward has no effect on the impedance at frequencies inside the PLL bandwidth, that is, at frequencies below approximately few tens of Hertz. The low-frequency impedance appears as a negative resistor determined by the ratio $-V_{od}/I_{od}$ due to PLL. Negative resistance is an inherent property of the grid synchronization.

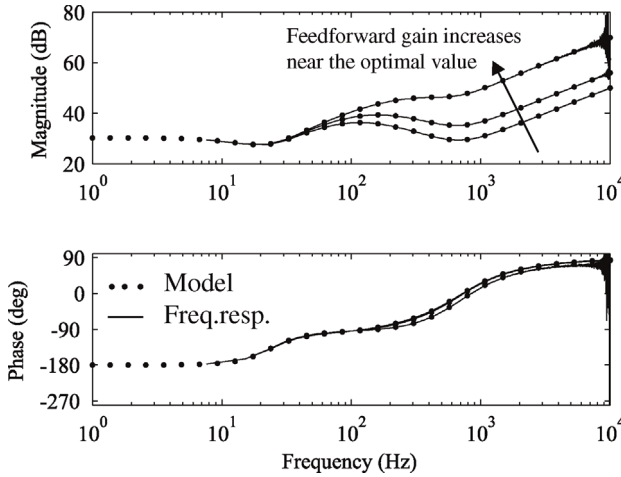


Figure 14.14 Output impedance q-component Z_{oqq-c} with feedforward gains smaller than the optimal value.

Figure 14.15 shows the impedance when feedforward gain is initially $0.9/V_{in}$ and increased beyond the optimal value to $1.5/V_{in}$ and $2/V_{in}$. The low-frequency impedance behaves still as a negative resistance and is not affected by feedforward. However, large feedforward gain produces a sharp resonant spike and decreases the phase of the impedance significantly. The impedance loses its passive characteristics at frequencies higher than the resonance since the phase does not stay contained between -90° and 90° lines. Moreover, the magnitude drops significantly at high frequencies that makes the inverter prone to impedance-based instability as will be discussed in Chapter 16.

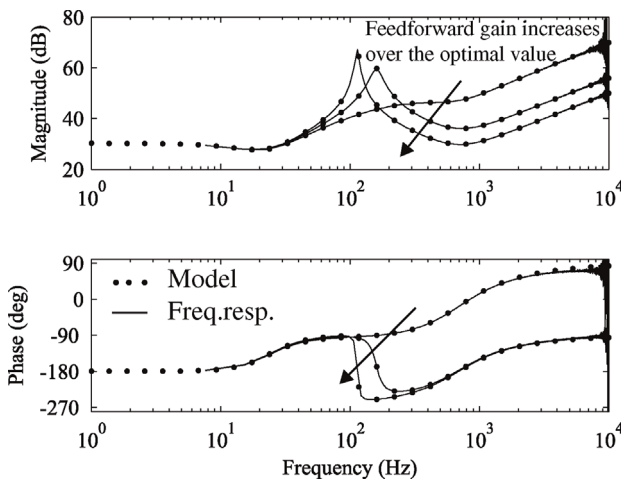


Figure 14.15 Output impedance q-component Z_{oqq-c} with feedforward gains larger than the optimal value.

14.2.5 Impedance Characteristics of Voltage-Fed Inverters

Based on the analysis above, the following guidelines and remarks on impedance behavior of voltage-fed inverters can be given:

- Output current control produces a capacitive element in both impedance components (d- and q-components). The capacitive element increases impedance magnitude, thus making the inverter to resemble more an ideal current source. Higher current control bandwidth produces larger capacitive element. However, in practical applications, current control cannot be tuned faster than switching frequency and the associated control delay allow, to avoid instability of the current control loop.
- Phase-locked-loop produces a negative resistance in the impedance q-component that determines its low-frequency behavior. The magnitude of negative resistance depends on the ratio of voltage and current d-components, or in the case of constant grid voltage, the processed power. The negative resistance region can be limited to low frequencies by using low-bandwidth PLL that, however, reduces the dynamic performance of the PLL. The negative resistance is not affected by current control or feedforward. The negative resistance is an inherent property of any grid synchronization algorithm and cannot be removed.
- Grid voltage feedforward increases the magnitude of both impedance components (d- and q-components). However, the feedforward gain should not be selected larger than the optimal value that is equal to the inverse of DC voltage steady-state value $1/V_{in}$. A value smaller than the optimal reduces the effectiveness of feedforward by decreasing the magnitude of the impedance. However, increasing the feedforward gain beyond the optimal value will result the decrease of both, the magnitude and the phase. This can be harmful for impedance-based stability since the impedance loses its passive features, that is, the phase does not stay between -90° and 90° .

14.3 Reduced-Order Model of Current-Fed Inverter with L-Type Filter

14.3.1 Closed-Loop Model with Cascaded Control Scheme

Current-fed inverter utilizes a cascaded control scheme where the outer input voltage control loop sets the reference value for the inner d-current control loop. The inverter with L-type output filter is analyzed first to demonstrate the method how the cascaded control scheme is included in the closed-loop model. First the closed-loop dynamics with current control are solved and secondly the outer control loop is included in the model. This allows the effects of different control loops on the closed-loop dynamics to be identified more easily.

Figure 14.16 depicts the inverter control block diagram when the current control loop of the d-component is closed. It is assumed that the cross-coupling transfer functions Y_{oqd-o} and G_{coqd-o} can be neglected and that the input dynamics depend mainly on real power [1]. Thus, the transfer functions T_{oiq-o} and G_{ciq-o} are

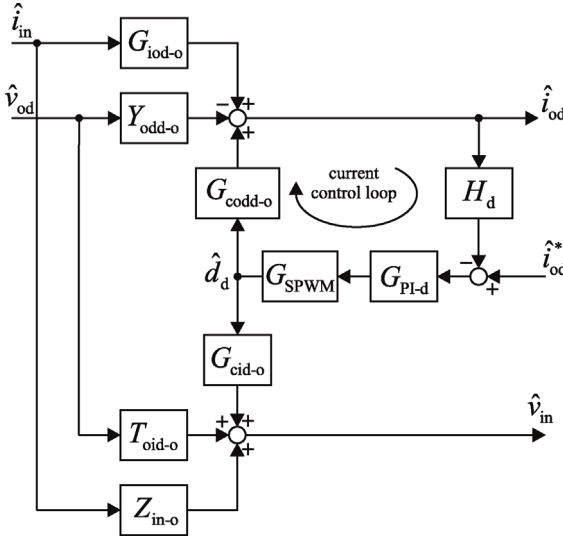


Figure 14.16 Reduced-order d-channel and input dynamics with current control.

neglected. Moreover, it is assumed that the d-channel dynamics are not affected by the PLL. Such model is referred as a reduced-order model.

Closed-loop transfer functions can be solved from Figure 14.16 and defined as in Eqs. (14.30–14.35) where the superscript “cc” is used to denote that transfer functions include the dynamic effect of current control.

$$G_{iod}^{cc} = \frac{\hat{i}_{od}}{\hat{i}_{in}} = \frac{G_{iod-o}}{(1 + L_{out-d})}, \quad (14.30)$$

$$Y_{odd}^{cc} = -\frac{\hat{i}_{od}}{\hat{v}_{od}} = \frac{Y_{odd-o}}{(1 + L_{out-d})}, \quad (14.31)$$

$$G_{codd}^{cc} = \frac{\hat{i}_{od}}{\hat{i}_{od}^*} = \frac{1}{H_d} \cdot \frac{L_{out-d}}{(1 + L_{out-d})}, \quad (14.32)$$

$$Z_{in}^{cc} = \frac{\hat{v}_{in}}{\hat{i}_{in}} = \frac{Z_{in-o}}{(1 + L_{out-d})} + \frac{L_{out-d}}{(1 + L_{out-d})} \left(Z_{in-o} - \frac{G_{cid-o} G_{iod-o}}{G_{codd-o}} \right), \quad (14.33)$$

$$T_{oid}^{cc} = \frac{\hat{v}_{in}}{\hat{v}_{od}} = \frac{T_{oid-o}}{(1 + L_{out-d})} + \frac{L_{out-d}}{(1 + L_{out-d})} \left(T_{oid-o} + \frac{G_{cid-o} Y_{odd-o}}{G_{codd-o}} \right), \quad (14.34)$$

$$G_{cid}^{cc} = \frac{\hat{v}_{in}}{\hat{i}_{od}^*} = \frac{1}{H_d} \cdot \frac{G_{cid-o}}{G_{codd-o}} \cdot \frac{L_{out-d}}{(1 + L_{out-d})}. \quad (14.35)$$

The current control loop gain can be defined as in Eq. (14.36) where H_d is the current sensing gain and G_{SPWM} is the modulator gain of the SPWM. The effect of a low-pass filter in the sensing circuit and delay from analog-to-digital converters can be taken into account by modifying the sensing gain transfer function. Moreover, the effect of a nonunity modulator gain and the corresponding delay

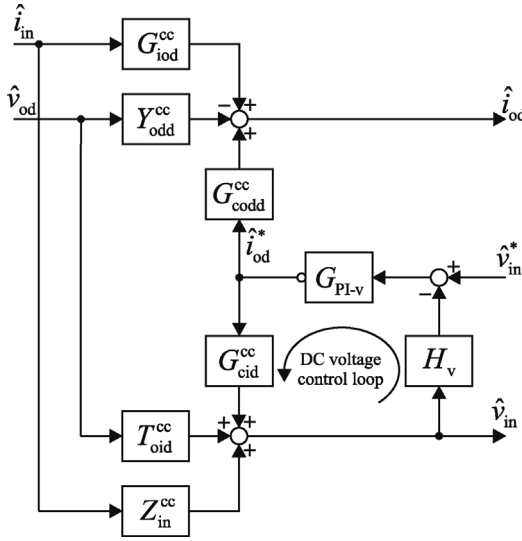


Figure 14.17 Reduced-order control dynamics (d-component) with input voltage control.

can be taken into account by modifying the modulator transfer function.

$$L_{out-d} = G_{codd-o} G_{SPWM} G_{PI-d} H_d. \quad (14.36)$$

The input voltage control loop can be included in the closed-loop model by considering the output-current controlled inverter as an open-loop system from the perspective of the outer voltage control loop. The corresponding control block diagram can be depicted as in Figure 14.17. H_v is the sensing gain of the input voltage measurement circuit and G_{PI-v} is the transfer function of input voltage controller. The dot at the controller output denotes that inverted control signal is used and is equivalent to a “-1” in the loop gain.

Closed-loop transfer functions can be solved from Figure 14.17 and given according to Eqs. (14.37–14.42).

$$Z_{in-c} = \frac{\hat{v}_{in}}{\hat{i}_{in}} = \frac{Z_{in-o}}{(1 + L_{in})(1 + L_{out-d})} + \frac{L_{out-d}}{(1 + L_{in})(1 + L_{out-d})} \left(Z_{in-o} - \frac{G_{cid-o} G_{iod-o}}{G_{codd-o}} \right), \quad (14.37)$$

$$T_{oid-c} = \frac{\hat{v}_{in}}{\hat{v}_{od}} = \frac{T_{oid-o}}{(1 + L_{in})(1 + L_{out-d})} + \frac{L_{out-d}}{(1 + L_{in})(1 + L_{out-d})} \left(T_{oid-o} + \frac{G_{cid-o} Y_{od-o}}{G_{codd-o}} \right), \quad (14.38)$$

$$G_{cid-c} = \frac{\hat{v}_{in}}{\hat{v}_{in}^*} = \frac{1}{H_v} \cdot \frac{L_{in}}{(1 + L_{in})}, \quad (14.39)$$

$$G_{iod-c} = \frac{\hat{i}_{od}}{\hat{i}_{in}} = \frac{G_{iod-o}}{(1 + L_{in})(1 + L_{out-d})} + \frac{L_{in}}{(1 + L_{in})} \left(G_{iod-o} - \frac{G_{codd-o} Z_{in-o}}{G_{cid-o}} \right), \quad (14.40)$$

$$Y_{\text{odd-c}} = -\frac{\hat{i}_{\text{od}}}{\hat{v}_{\text{od}}} = \frac{Y_{\text{odd-o}}}{(1 + L_{\text{in}})(1 + L_{\text{out-d}})} + \frac{L_{\text{in}}}{(1 + L_{\text{in}})} \left(Y_{\text{odd-o}} + \frac{G_{\text{codd-o}} T_{\text{oid-o}}}{G_{\text{cid-o}}} \right), \quad (14.41)$$

$$G_{\text{codd-c}} = \frac{\hat{i}_{\text{od}}}{\hat{v}_{\text{in}}^*} = \frac{1}{H_v} \cdot \frac{L_{\text{in}}}{(1 + L_{\text{in}})} \cdot \frac{G_{\text{codd-o}}}{G_{\text{cid-o}}}. \quad (14.42)$$

The input voltage control loop gain is defined as in Eq. (14.43) where the inverted control signal is taken into account by multiplying the loop gain by minus one.

$$L_{\text{in}} = (-1) \cdot \frac{H_v}{H_d} \cdot \frac{G_{\text{cid-o}}}{G_{\text{codd-o}}} \cdot \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})} \cdot G_{\text{PI-v}}. \quad (14.43)$$

14.3.2 Effect of Input Voltage Control Bandwidth

Effect of the input voltage control bandwidth on the inverter output impedance d-component is studied in this section. The parameters of the studied photovoltaic inverter used for impedance model verification are as given in Table 14.1 that are used in the simulation model and as the parameters of the actual experimental setup.

The output admittance d-component is as defined by Eq. (14.41) where the first terms corresponds to the open-loop admittance $Y_{\text{odd-o}}$ divided by both control loop gains L_{in} and $L_{\text{out-d}}$. The current control effectively tries to make the inverter to look like an ideal current source with high output impedance. At low-frequencies, the first term is close to zero due to the fact that both loop gains have large magnitudes. Therefore, the second term of Eq. (14.41) defines the low-frequency behavior of the impedance and can be defined as in Eq. (14.44). At low frequencies, the term $L_{\text{in}}/(1 + L_{\text{in}})$ is close to unity, that is, inside the input voltage control bandwidth.

$$Y_{\text{odd-c}}^{\text{low-freq}} = \frac{L_{\text{in}}}{(1 + L_{\text{in}})} \left(Y_{\text{odd-o}} + \frac{G_{\text{codd-o}} T_{\text{oid-o}}}{G_{\text{cid-o}}} \right) = \frac{L_{\text{in}}}{(1 + L_{\text{in}})} \cdot Y_{\text{od-}\infty}. \quad (14.44)$$

The open-loop transfer functions inside the brackets in Eq. (14.44) are defined using the special parameter $Y_{\text{od-}\infty}$. The special parameter in the operating point defined in Table 14.1 can be drawn in the frequency-domain as shown in Figure 14.18. The transfer function has a special meaning since it defines the low-frequency value of admittance d-component $Y_{\text{odd-c}}$.

The transfer function has a value of approximately $I_{\text{od}}/V_{\text{od}}$ up to 100 Hz. Therefore, the low-frequency impedance, below the input voltage control bandwidth, can be approximated by Eq. (14.45). The same result can be obtained by

Table 14.1 Parameters of the photovoltaic inverter.

V_{mpp}	414.3 V	$L_{\text{a,b,c}}$	5 mH	V_{od}	$\sqrt{(2)} \cdot 120 \text{ V}$
I_{mpp}	6.58 A	C_{dc}	1.5 mF	ω_s	$2\pi \cdot 60 \text{ rad/s}$
P_{mpp}	2.7 kW	r_{eq}	100 m Ω	f_{sw}	8 kHz

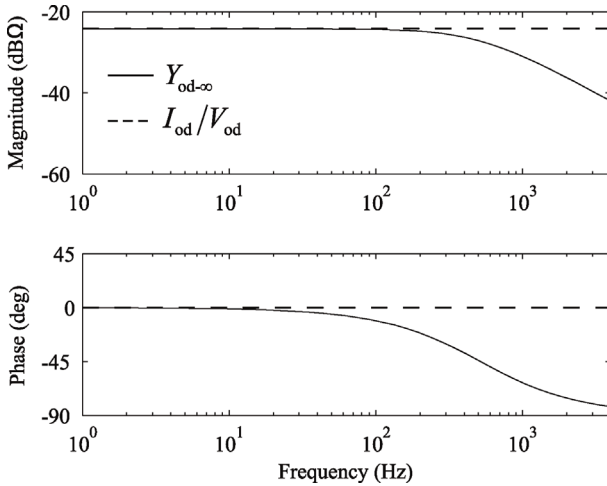


Figure 14.18 The special term $Y_{od-\infty}$ and its approximated value.

applying symbolic analysis to Eq. (14.44). Based on the analysis, one should expect that the low-frequency impedance behaves as a resistor at frequencies below the input voltage control bandwidth and its value depends on the processed power. The value of the resistance decreases with increasing output current, assuming the grid voltage amplitude remains constant. This corresponds to the well-known behavior of a constant power source. This result is very beneficial in determining the low-frequency impedance since one only has to know the grid voltage amplitude and the amount of real power supplied by the inverter.

$$Z_{\text{odd-c}}^{\text{low-freq}} = \left(Y_{\text{odd-c}}^{\text{low-freq}} \right)^{-1} \approx \frac{V_{\text{od}}}{I_{\text{od}}}. \quad (14.45)$$

Figure 14.19 shows the output impedance d-components extracted from the switching model in two cases. The input voltage control is tuned to have crossover frequencies f_c of 10 and 50 Hz with 65° phase margin, correspondingly. The current control is tuned to have a crossover frequency of 500 Hz in both cases. The impedance resembles a resistor at frequencies below the bandwidth of the input voltage control. However, one should remember that the inverter also employs current control that has to be tuned to have faster dynamics than the input voltage control. In principle, the passive resistance region cannot be extended over few tens of hertz. Wide-bandwidth DC voltage control amplifies noise, such as the DC voltage ripple at second harmonic during unbalance that easily corrupts the output current references as discussed in Chapter 13. The low-frequency resonant spike can be shifted by changing the voltage control crossover frequency.

14.3.3 Effect of AC Current Control Bandwidth

The AC current control is usually tuned to have crossover frequency of at least one decade higher than the input voltage control loop. The current control

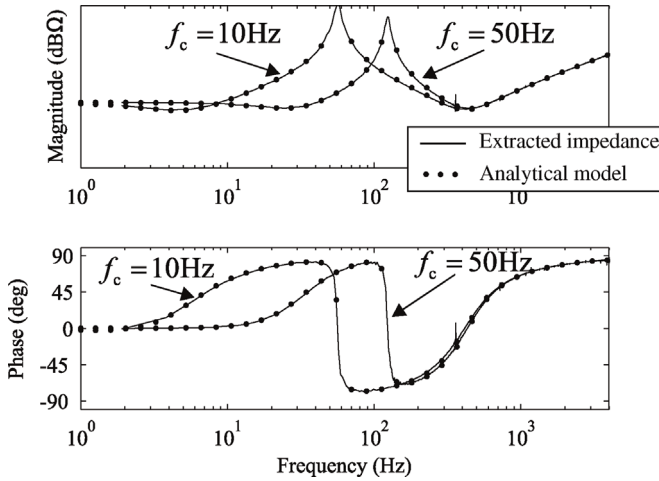


Figure 14.19 Effect of input voltage control bandwidth on inverter output impedance d-component $Z_{\text{odd-c}}$.

effectively makes the inverter to appear as a current source, that is, the current control increases the magnitude of inverter output impedance. It should be noted that the simulation model does not include delay and, therefore, the current control is stable even with very large bandwidth. However, in real applications delays originating from sampling and the modulator may destabilize the current control, whereas, higher switching frequency reduces the delay and enables faster current control.

Figure 14.20 shows the output impedance d-component when the current control is tuned to have crossover frequencies of 500 Hz and 1 kHz and 65° phase margin. The input voltage control is tuned to have a crossover frequency of 10 Hz

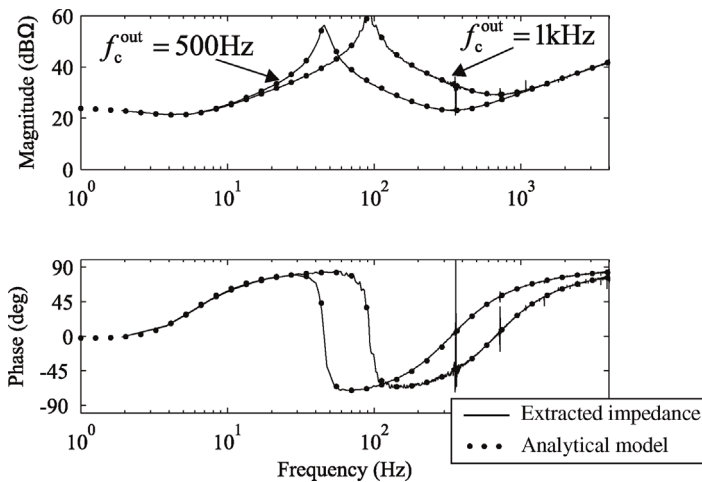


Figure 14.20 Effect of current control bandwidth on inverter output impedance d-component $Z_{\text{odd-c}}$.

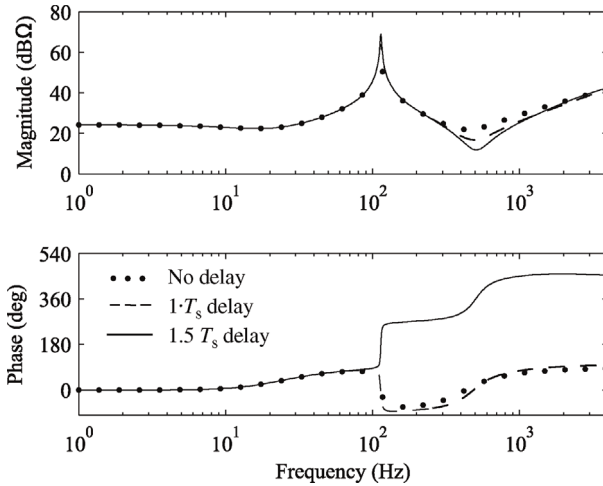


Figure 14.21 Effect of control delay on inverter output impedance d-component $Z_{\text{odd-c}}$.

in both cases. The low-frequency impedance is determined by the input voltage control, that is, by the constant power nature of the inverter, and cannot be modified by current control. The current control starts affecting the impedance magnitude at frequencies that are outside the input voltage control bandwidth. Moreover, increasing the current control bandwidth increases the resonant frequency.

The effect of control delay on the impedance was evaluated by multiplying the loop gain with the delay transfer function. A second-order Pade-approximation was used to define the delay transfer function. Figure 14.21 shows the impedance with three values of delay. The dotted line depicts the impedance when no delay is present, dashed line depicts the impedance when delay is selected as one switching cycle $1/f_{\text{sw}}$, and the solid line depicts the impedance when delay is selected as $1.5/f_{\text{sw}}$. The delay decreases the magnitude only slightly. However, the phase of the impedance experiences a jump of $+360^\circ$ at the resonant frequency. Therefore, the impedance loses its passive features that is generally seen as a precondition for impedance-based interactions when the grid has finite impedance.

14.3.4 Experimental Verification: Measured Impedance d-Component

Figure 14.22 shows the measured impedance d-component from the 2.7 kW laboratory setup. The frequency response given by the analytical model in Eq. (14.41) is shown as the dotted line. The analytical model includes a control system delay of $1.5 T_s$. The current control was tuned to have a crossover frequency of 500 Hz and the input voltage control had a crossover frequency of 40 Hz. The impedance does not resemble a passive circuit due to the control delay as discussed earlier. The impedance measured from the prototype includes many spikes in the magnitude and phase that are caused by measurement noise and harmonics generated by the dead-time effect. The dead-time was used to

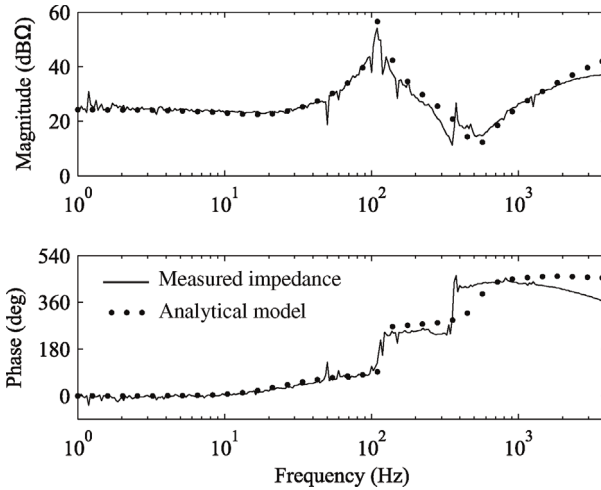


Figure 14.22 Measured output impedance d-component Z_{odd-c} .

avoid simultaneous conduction of current in upper and lower switches in a phase-leg. The inverter utilizes an IGBT-IPM module type 7MBP50RJ120 based on IGBT switches that has recommended dead-time of $4 \mu\text{s}$.

14.3.5 Effect of SRF-PLL

The phase-locked-loop affects the output dynamics related to the q-components and should be included in the closed-loop model. The control block diagram is as shown in Figure 14.23 that is very similar to the one depicted in Figure 14.4 in the

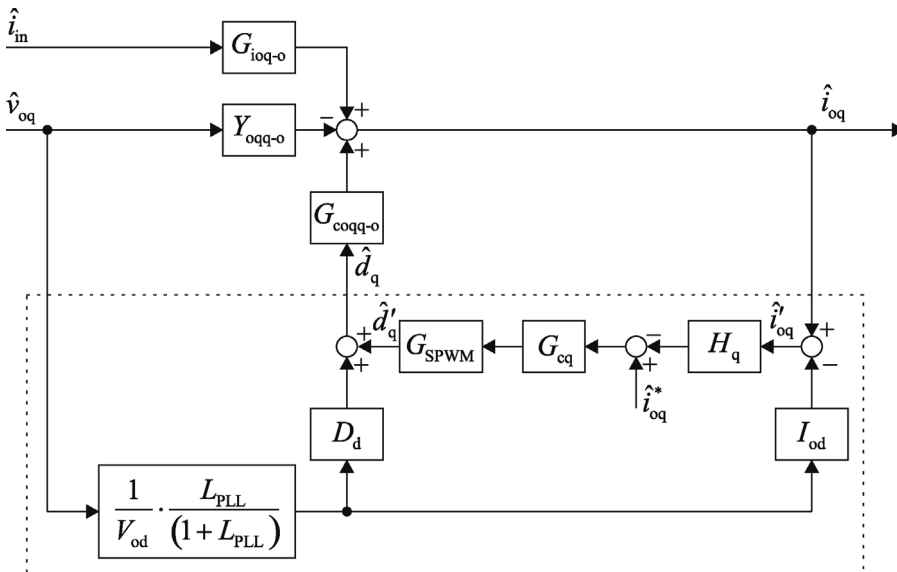


Figure 14.23 Control block diagram describing q-channel output dynamics.

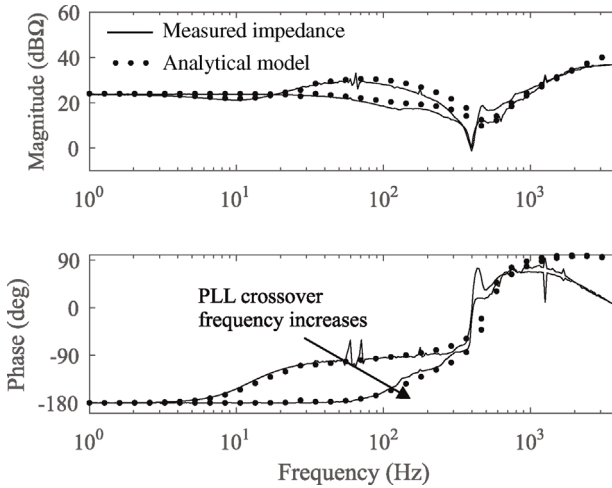


Figure 14.24 Measured output impedance q-component Z_{oqq-c} .

case of a voltage-fed inverter. The only difference is that the input voltage \hat{v}_{in} is treated as an output variable and input current \hat{i}_{in} as an input variable.

The closed-loop output impedance q-component Y_{oqq-c} can be solved from the block diagram by solving the transfer function from output voltage q-component to output current q-component and is given by Eq. (14.46). The transfer function seems to be identical with the output impedance of voltage-fed inverter in Eq. (14.16). However, the open-loop transfer functions of current-fed inverter are of higher order since they include the dynamic effect of DC capacitor.

$$Y_{oqq-c} = \frac{\hat{i}_{oq}}{\hat{v}_{oq}} = \frac{Y_{oqq-o}}{(1+L_{out-q})} - \frac{I_{Ld}}{V_{od}} \frac{L_{out-q}}{(1+L_{out-q})(1+L_{PLL})} - \frac{L_{PLL}}{V_{od}} \frac{D_d}{(1+L_{out-q})(1+L_{PLL})} \frac{G_{coqq-o}}{(1+L_{PLL})} \frac{L_{PLL}}{(1+L_{PLL})}. \quad (14.46)$$

Figure 14.24 shows the measured and predicted impedance q-component when PLL was tuned to have crossover frequencies of 20 and 200 Hz. Increasing the PLL crossover makes the phase to stay close to -180° over a wider frequency range. Moreover, the magnitude stays constant at frequencies below the crossover frequency. Thus, the impedance resembles a negative resistance of $-V_{od}/I_{od}$ at low frequencies.

The negative resistance can easily destabilize a grid-connected inverter. Therefore, the PLL bandwidth should be limited. However, the question of maximum allowed PLL crossover frequency depends on many factors such as processed power and shape of grid impedance and requires a case-specific evaluation of impedance-based stability. An example case study is presented in Chapter 16.

14.3.6 Effect of Grid Voltage Feedforward on Impedance d-Component

Similarly, as with a voltage-fed inverter, the current-fed inverter often utilizes feedforward measurements from grid voltages to improve its output impedance behavior. The grid voltage feedforward can be included in the reduced-order

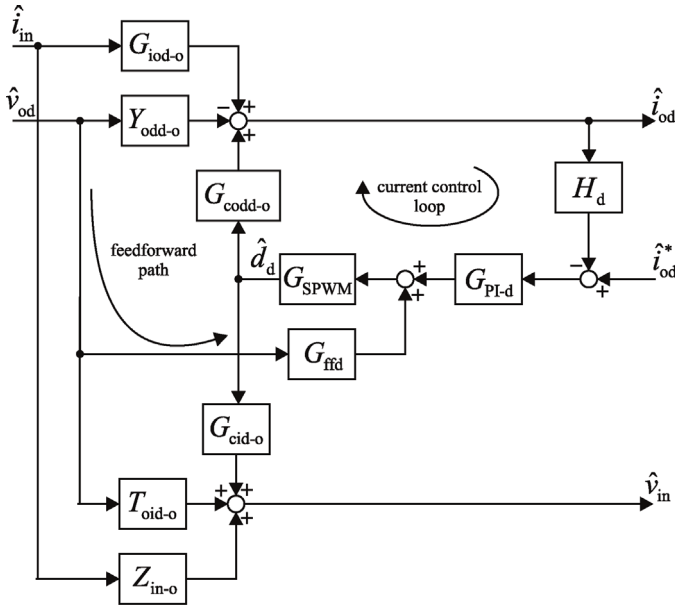


Figure 14.25 Current-fed inverter output dynamics (d-component) with current control and grid voltage feedforward.

closed-loop model (of d-components) by using the same approach as before when solving the effect of cascaded control scheme. The current control and feedforward loops are first closed as illustrated in Figure 14.25. The closed-loop transfer functions are solved from the block diagram.

The most convenient way of solving the transfer functions is to use the principle of superposition. For example, output voltage d-component \hat{v}_{od} and output current reference \hat{i}_{od}^* are set equal to zero that allows drawing the control block diagram as in Figure 14.26. From this form, it is easier to find the closed-loop transfer function from input current to output current d-component as given in Eq. (14.47). The superscript “cc-ff” is used to denote that the transfer

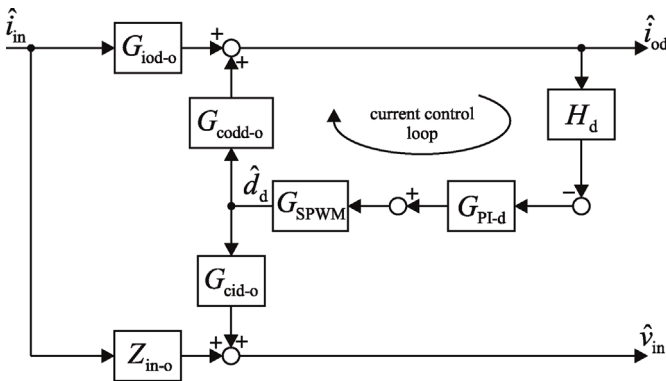


Figure 14.26 Control block diagram to solve G_{iod}^{cc-ff} .

function includes the dynamic effects of output current control and grid voltage feedforward.

$$G_{\text{iod}}^{\text{cc-ff}} = \frac{\hat{i}_{\text{od}}}{\hat{i}_{\text{in}}} = \frac{G_{\text{iod-o}}}{(1 + L_{\text{out-d}})}. \quad (14.47)$$

Transfer function from input current to input voltage can be solved by noting that the duty ratio is given by

$$\hat{d}_d = -G_{\text{SPWM}} G_{\text{PI-d}} H_d \hat{i}_{\text{od}} = -\frac{G_{\text{iod-o}}}{G_{\text{codd-o}}} \cdot \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})} \hat{i}_{\text{in}}. \quad (14.48)$$

Therefore, the input voltage can be defined as

$$\hat{v}_{\text{in}} = G_{\text{cid-o}} \hat{d}_d + Z_{\text{in-o}} \hat{i}_{\text{in}} = -\frac{G_{\text{cid-o}} G_{\text{iod-o}}}{G_{\text{codd-o}}} \cdot \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})} \hat{i}_{\text{in}} + Z_{\text{in-o}} \hat{i}_{\text{in}}, \quad (14.49)$$

which can be simplified as

$$\hat{v}_{\text{in}} = \left(\frac{Z_{\text{in-o}}}{(1 + L_{\text{out-d}})} - \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})} \cdot \left(Z_{\text{in-o}} + \frac{G_{\text{cid-o}} G_{\text{iod-o}}}{G_{\text{codd-o}}} \right) \right) \hat{i}_{\text{in}}, \quad (14.50)$$

and finally the closed-loop transfer function from input current to input voltage, that is, the input impedance $Z_{\text{in}}^{\text{cc-ff}}$, can be given as

$$Z_{\text{in}}^{\text{cc-ff}} = \frac{\hat{v}_{\text{in}}}{\hat{i}_{\text{in}}} = \frac{Z_{\text{in-o}}}{(1 + L_{\text{out-d}})} - \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})} \cdot \left(Z_{\text{in-o}} + \frac{G_{\text{cid-o}} G_{\text{iod-o}}}{G_{\text{codd-o}}} \right). \quad (14.51)$$

By using the same approach, the rest of the closed-loop dynamics can be solved and given as

$$Y_{\text{odd}}^{\text{cc-ff}} = -\frac{\hat{i}_{\text{od}}}{\hat{v}_{\text{od}}} = \frac{Y_{\text{odd-o}} - G_{\text{codd-o}} G_{\text{ffd}}}{(1 + L_{\text{out-d}})}, \quad (14.52)$$

$$G_{\text{codd}}^{\text{cc-ff}} = \frac{\hat{i}_{\text{od}}}{\hat{i}_{\text{od}}^*} = \frac{1}{H_d} \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})}, \quad (14.53)$$

$$T_{\text{oid}}^{\text{cc-ff}} = \frac{\hat{v}_{\text{in}}}{\hat{v}_{\text{o}}} = \frac{T_{\text{oid-o}} + G_{\text{cid-o}} G_{\text{SPWM}} G_{\text{ffd}}}{(1 + L_{\text{out-d}})} + \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})} \left(T_{\text{oid-o}} + \frac{G_{\text{cid-o}} Y_{\text{odd-o}}}{G_{\text{codd-o}}} \right), \quad (14.54)$$

$$G_{\text{cid}}^{\text{cc-ff}} = \frac{\hat{v}_{\text{in}}}{\hat{i}_{\text{od}}^*} = \frac{1}{H_d} \frac{G_{\text{cid-o}}}{G_{\text{codd-o}}} \frac{L_{\text{out-d}}}{(1 + L_{\text{out-d}})}, \quad (14.55)$$

where the current control loop is given as

$$L_{\text{out-d}} = G_{\text{codd-o}} G_{\text{SPWM}} G_{\text{PI-d}} H_d. \quad (14.56)$$

The input voltage control can be added in closed-loop dynamics by treating the output-current controlled converter as an open-loop system from the view-point of the input voltage controller, that is, the control input of the “open-loop” system is the reference value of output current d-component. Control block diagram with input voltage control is depicted in Figure 14.27.

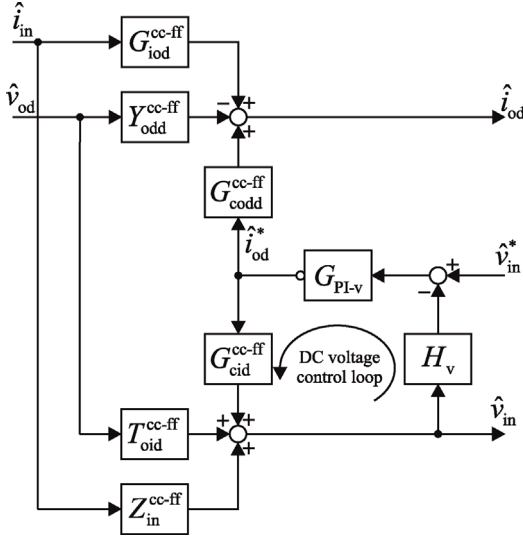


Figure 14.27 Current-fed inverter output dynamics (d-component) with input voltage control.

The output signal of input voltage controller G_{PI-v} is inverted that equals a gain of minus one. Closed-loop transfer functions can be solved from the block diagram and given as in Eqs. (14.57–14.62).

$$Z_{in-c}^{ff} = \frac{\hat{v}_{in}}{\hat{i}_{in}} = \frac{Z_{in-o}}{(1+L_{in})(1+L_{out-d})} + \frac{1}{(1+L_{in})(1+L_{out-d})} \left(Z_{in-o} - \frac{G_{cid-o}G_{iod-o}}{G_{codd-o}} \right), \quad (14.57)$$

$$T_{oid-c}^{ff} = \frac{\hat{v}_{in}}{\hat{v}_{od}} = \frac{T_{oid-o} + G_{cid-o}G_{SPWM}G_{ffd}}{(1+L_{in})(1+L_{out-d})} + \frac{1}{(1+L_{in})(1+L_{out-d})} \left(T_{oid-o} + \frac{G_{cid-o}Y_{odd-o}}{G_{codd-o}} \right), \quad (14.58)$$

$$G_{cid-c}^{ff} = \frac{\hat{v}_{in}}{\hat{v}_{in}^*} = \frac{1}{H_v(1+L_{in})} L_{in}, \quad (14.59)$$

$$G_{iod-c}^{ff} = \frac{\hat{i}_{od}}{\hat{i}_{in}} = \frac{G_{iod-o}}{(1+L_{in})(1+L_{out-d})} + \frac{1}{(1+L_{in})} \left(G_{iod-o} - \frac{G_{codd-o}}{G_{cid-o}} Z_{in-o} \right), \quad (14.60)$$

$$Y_{odd-c}^{ff} = \frac{\hat{i}_{od}}{\hat{v}_{od}} = \frac{Y_{odd-o} - G_{codd-o}G_{SPWM}G_{ffd}}{(1+L_{in})(1+L_{out-d})} + \frac{1}{(1+L_{in})} Y_{od-\infty}, \quad (14.61)$$

$$G_{codd-c}^{ff} = \frac{\hat{i}_{od}}{\hat{v}_{in}^*} = \frac{1}{H_v} \frac{G_{codd-o}}{G_{cid-o}} \frac{L_{in}}{(1+L_{in})}. \quad (14.62)$$

The input voltage control loop gain is defined as

$$L_{in} = H_v(-1)G_{PI-v}G_{cid}^{cc-ff} = (-1) \cdot \frac{H_v}{H_d} G_{PI-v} \frac{G_{cid-o}}{G_{codd-o}} \frac{L_{out-d}}{(1+L_{out-d})}, \quad (14.63)$$

and the special parameter $Y_{\text{od-}\infty}$ as

$$Y_{\text{od-}\infty} = Y_{\text{odd-o}} + \frac{G_{\text{codd-o}} T_{\text{oid-o}}}{G_{\text{cid-o}}}. \quad (14.64)$$

The output admittance in Eq. (14.61) is affected by the grid voltage feedforward similarly, as in the case of a voltage-fed inverter. The low-frequency behavior of the admittance is determined by the term $Y_{\text{od-}\infty}$ and cannot be influenced by the feedforward. At low frequencies, where the ratio $L_{\text{in}}/(1 + L_{\text{in}})$ is close to unity, the admittance d-component depends on the inverter output power according to the ratio $I_{\text{od}}/V_{\text{od}}$ as demonstrated earlier in Figure 14.19.

The output admittance at frequencies over the input voltage control bandwidth is affected by the feedforward. According to Eq. (14.61) the feedforward gain cancels out the open-loop admittance when its value is selected according to

$$G_{\text{ffd}}^{\text{ideal}} = \frac{Y_{\text{odd-o}}}{G_{\text{codd-o}} G_a} \approx \frac{1}{V_{\text{in}}}. \quad (14.65)$$

It is easy to see that with optimal feedforward gain (and negligible delay) the output impedance d-component is given by

$$Y_{\text{odd-c}}^{\text{ideal-ff}} = \frac{L_{\text{in}}}{(1 + L_{\text{in}})} Y_{\text{od-}\infty} \quad (14.66)$$

Therefore, the output impedance d-component can be approximated as in Eq. (14.67) when the input voltage control bandwidth is known and current control is tuned to be sufficiently fast. The pole $\omega_{\text{BW-dc}}$ is placed according to the voltage control bandwidth which is defined as the -3 dB point from $L_{\text{in}}/(1 + L_{\text{in}})$.

$$Z_{\text{odd-c}}^{\text{approx}} = \left(\frac{I_{\text{od}}}{V_{\text{od}}} \cdot \frac{1}{(s/\omega_{\text{BW-dc}} + 1)} \right)^{-1}. \quad (14.67)$$

Figure 14.28 shows the impedance d-component extracted from a switching model and the simplified analytical approximation according to Eq. (14.67). The input voltage control bandwidth is 13.6 Hz (or 85.3 rad/s). The solid line is the impedance

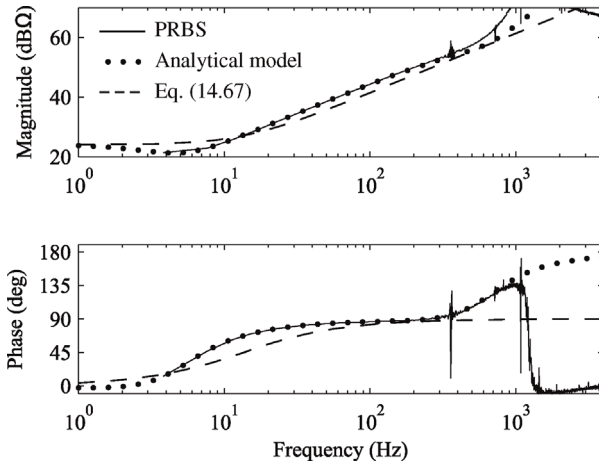


Figure 14.28 Output impedance d-component $Z_{\text{odd-c}}$ with optimal grid voltage feedforward.

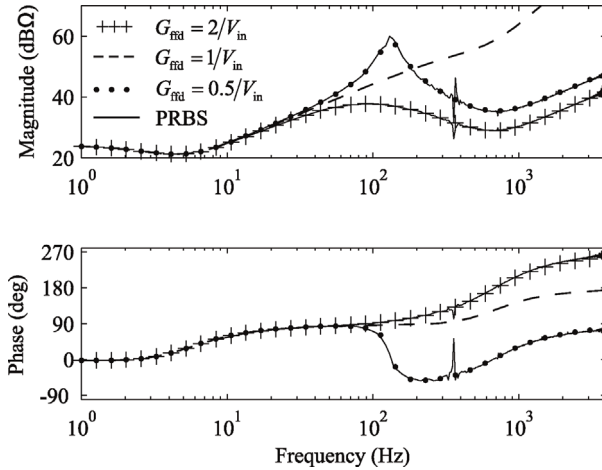


Figure 14.29 Output impedance d-component $Z_{\text{odd-c}}$ with different feedforward gains.

extracted using PBRs-method, dots represent the analytical impedance according to transfer function of Eq. (14.61), and the dashed line depicts the simplified form according to Eq. (14.67). The feedforward gain was selected as $1/V_{\text{in}}$ according to the previous analysis. Current control with a crossover of 1 kHz and phase margin of 65° was used. The gain and phase of the analytical model deviates from the simulated impedance at high frequencies. This is caused by the fact that cross-coupling dynamics were neglected when deriving the closed-loop impedance. A full-order model can be used that predicts the shape of the impedance also at higher frequencies that is discussed in the next chapter. The simplified impedance model of Eq. (14.67) gives a prediction with a reasonable accuracy up to a few hundred hertz.

The feedforward gain should be selected as the inverse of DC voltage to obtain output impedance with the highest magnitude. Figure 14.29 shows the analytical impedance according to Eq. (14.61) and the simulated impedance when the feedforward gain is selected as $0.5/V_{\text{in}}$, $1/V_{\text{in}}$, and $2/V_{\text{in}}$. As can be seen by comparing the results, increasing the feedforward gain makes the feedforward to lose its effectiveness, since the magnitude drops compared to the previous case. Moreover, using a feedforward gain smaller than the optimal value makes the feedforward to lose its effectiveness as well. Small feedforward gain makes the impedance to resemble more like the case when feedforward is deactivated. Moreover, the low-frequency resonance appears back in the impedance.

14.3.7 Effect of Grid Voltage Feedforward on Impedance q-Component

The output impedance q-component can be solved from the block diagram in Figure 14.30. The block diagram is modified from Figure 14.23 by noting that the q-components (current, voltage or duty ratio) inside the control system reference frame are affected by the PLL and can be given according to Eq. (14.68).

$$\hat{x}'_q = \hat{x}_q - \frac{X_d}{V_d} \frac{L_{\text{PLL}}}{(1 + L_{\text{PLL}})} \hat{v}_q. \quad (14.68)$$

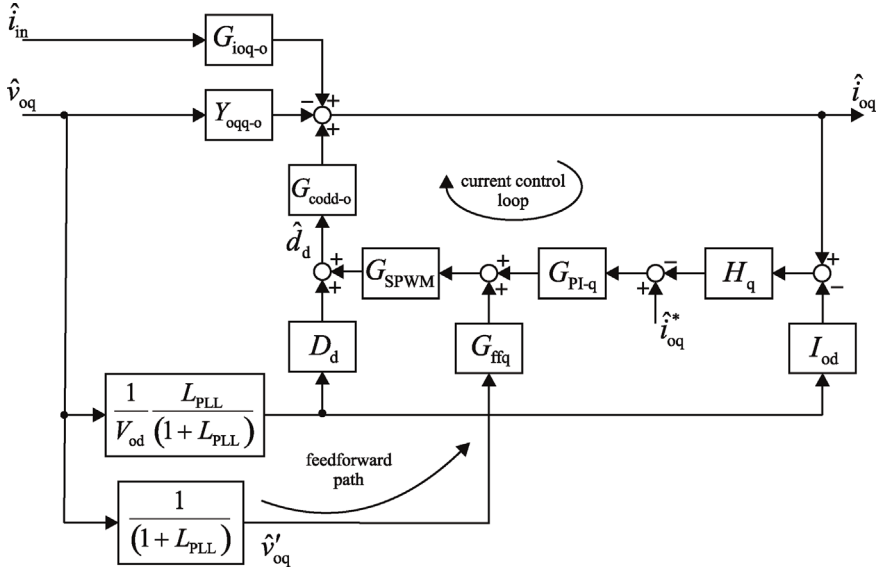


Figure 14.30 Current-fed inverter output dynamics (q-component) with PLL, output current control, and grid voltage feedforward.

The grid voltage q-component inside the control system reference frame can, therefore, be given as

$$\hat{v}'_q = \hat{v}_q - \frac{V_d}{V_d(1+L_{PLL})} \hat{v}_q = \frac{1}{(1+L_{PLL})} \hat{v}_q. \quad (14.69)$$

The sensed grid voltage q-component is multiplied by the feedforward gain G_{ffq} and the control block diagram of the output dynamics can be depicted as in Figure 14.30.

Closed-loop transfer functions can be solved from the block diagram by using the principle of superposition and given as in Eqs. (14.70–14.72).

$$G_{ioq-c}^{ff} = \frac{\hat{i}_{oq}}{\hat{i}_{in}} = \frac{G_{ioq-o}}{(1+L_{out-q})}, \quad (14.70)$$

$$Y_{oqq-c}^{ff} = -\frac{\hat{i}_{oq}}{\hat{v}_{oq}} = \frac{(Y_{oqq-o} - (G_{coqq-o} G_{SPWM} G_{ffq} / (1+L_{PLL})))}{(1+L_{out-q})} - \frac{I_{od}}{V_{od}} \frac{L_{out-q}}{(1+L_{out-q})} \frac{L_{PLL}}{(1+L_{PLL})} - \frac{D_d}{V_{od}} \frac{G_{coqq-o}}{(1+L_{out-q})} \frac{L_{PLL}}{(1+L_{PLL})}, \quad (14.71)$$

$$G_{coqq-c}^{ff} = \frac{\hat{i}_{oq}}{\hat{i}_{oq}^*} = \frac{1}{H_q} \frac{L_{out-q}}{(1+L_{out-q})}. \quad (14.72)$$

Let us consider the first term in the output admittance q-component in Eq. (14.71), assuming unity modulator gain as in Eq. (14.74). It is easy to show that if the PLL has negligible gain at the frequencies of interest, the numerator is equal to zero when

feedforward gain is selected as $G_{\text{ffq}} = Y_{\text{oqq-o}}/G_{\text{coqq-o}}$. The ideal feedforward gain G_{ffq} can be solved from the transfer functions and is as given by Eq. (14.74) that has the same value as in the case of feedforward gain G_{ffd} affecting the d-components, as one could expect.

$$Y_{\text{oqq-c}}^{\text{1st term}} = \frac{(Y_{\text{oqq-o}} - (G_{\text{coqq-o}}G_{\text{ffq}}/(1 + L_{\text{PLL}}))) \text{ (with very slow PLL)}}{(1 + L_{\text{out-q}})} \approx \frac{(Y_{\text{oqq-o}} - G_{\text{coqq-o}}G_{\text{ffq}})}{(1 + L_{\text{out-q}})}, \quad (14.73)$$

$$G_{\text{ffq}}^{\text{ideal}} = \frac{Y_{\text{oqq-o}}}{G_{\text{coqq-o}}} \approx \frac{1}{V_{\text{in}}}. \quad (14.74)$$

However, the PLL diminishes the effect of feedforward at frequencies inside its control bandwidth because the term $G_{\text{coqq-o}}G_{\text{ffq}}$ is effectively divided by the PLL loop gain L_{PLL} in Eq. (14.71). Figure 14.31 shows the PLL loop gains and the corresponding output admittance q-component when the crossover frequency of the PLL is selected as 10, 100, and 1000 Hz. The PLL phase margin is kept at 65° in all cases. Using faster PLL pushes the negative resistance region toward higher frequencies. At the same time the effect of the grid voltage feedforward is diminished, that is, the magnitude of the output impedance is smaller over the whole frequency range when fast PLL is used. As a conclusion, the grid voltage feedforward cannot be used to remove the negative resistance from the inverter output impedance. The negative resistance is an inherent property of the PLL and is caused by the fact that the PLL inverter tries to force the sensed grid voltage q-component to zero. The only feasible way of avoiding the negative resistance-behavior is to limit the PLL bandwidth.

Figure 14.32 shows the impedance q-components when grid voltage feedforward is deactivated and when the feedforward gain is selected according to Eq. (14.74). The impedances were also extracted from a switching model by using the PRBS injection method. The PLL was tuned to have a crossover frequency of 10 Hz and current control a crossover frequency of 1 kHz. The feedforward with optimal gain increases the impedance magnitude significantly compared to the case when it is deactivated. As deduced earlier, the negative resistance appears at low frequencies due to the PLL. However, the feedforward effectively increases the impedance at high frequencies. The impedance model was developed by neglecting the cross-coupling transfer functions. This is the reason why the model cannot reproduce the impedance magnitude correctly at high frequencies. In reality, the cross-coupling transfer functions, although small in their magnitude, start to have an effect on the impedance at high frequencies. Their effect can be taken into account by using the multivariable small-signal model as discussed more in detail in Chapter 15.

A rough approximation for the output impedance q-component can be given as in Eq. (14.75) when the feedforward gain is selected as $1/V_{\text{in}}$. The pole $\omega_{\text{BW-PLL}}$ is placed according to the PLL control bandwidth that is defined as the -3 dB point from transfer function $L_{\text{PLL}}/(1 + L_{\text{PLL}})$. Figure 14.33 shows a comparison of the impedance extracted from the simulator, given by the reduced-order impedance model in Eq. (14.71) and the approximation in Eq. (14.75). The approximation gives quite good approximation on the shape of the impedance and can be used to

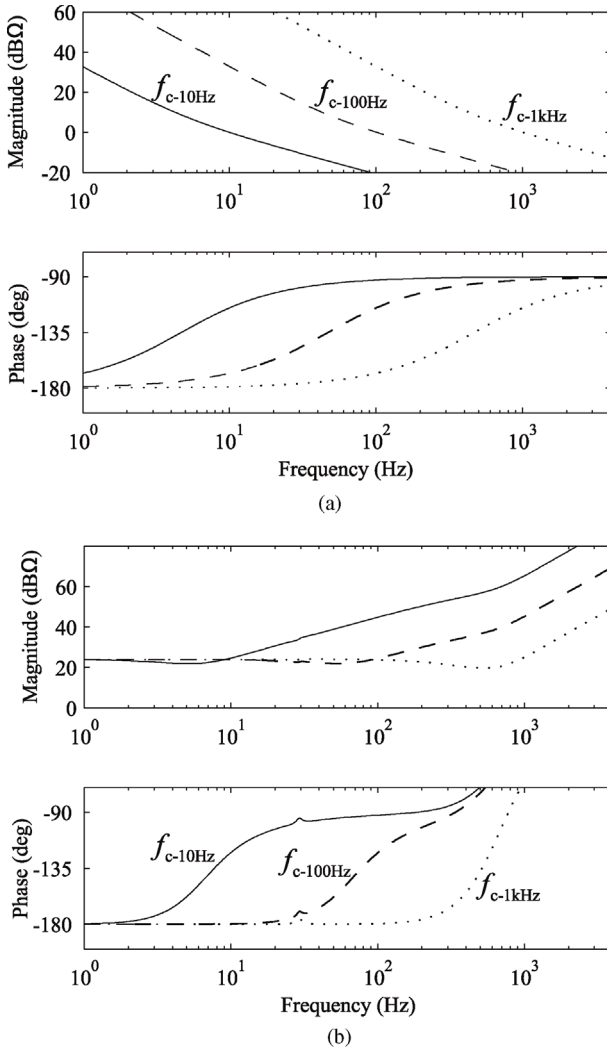


Figure 14.31 (a) PLL with different crossover frequencies. (b) The corresponding output impedance q-component.

get a rough idea, for example, on the negative resistance region without needing to derive the whole dynamic model. However, the approximation only applies to inverter with L-type output filter in the case when switching frequency is high enough to allow the control delay to be neglected.

$$Z_{\text{oqq-c}}^{\text{approx.}} = \left(-\frac{I_{\text{od}}}{V_{\text{od}}} \frac{1}{(s/\omega_{\text{BW-PLL}} + 1)} \right)^{-1} \quad (14.75)$$

The grid voltage feedforward evidently increases inverter output impedance that is in line with the studies showing that the feedforward improves current quality when grid voltages experience harmonic components, that is, the inverter

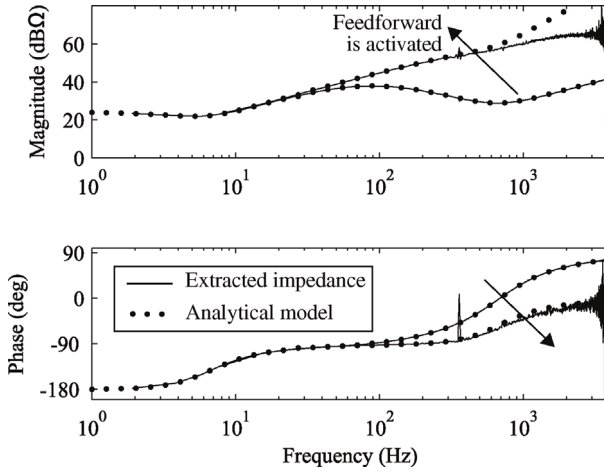


Figure 14.32 Impedance q-component Z_{oqq-c} extracted from the switching model with and without grid voltage feedforward.

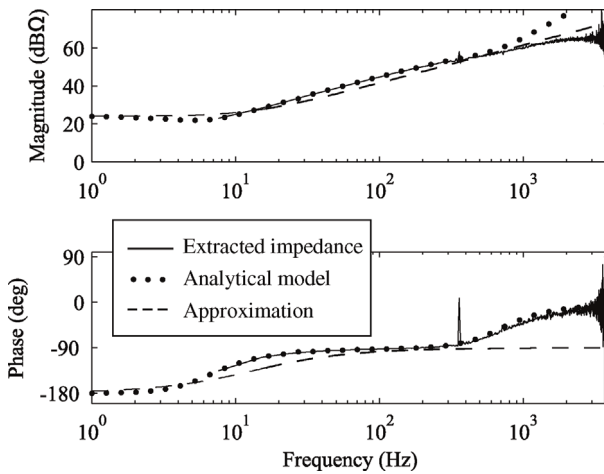


Figure 14.33 Comparison of output impedance q-component (14.75) with measurement and reduced-order model.

is operated as a current source and should have as large output impedance as possible. These results apply to the current-fed inverter utilizing an L-type output filter. Impedance model for inverter with LCL-filter require more complex small-signal model that is derived in the next chapter.

14.4 Closed-Loop Model of Current-Fed Inverter with LC-Type Filter

In state-of-the-art inverters an LCL-type output filter is used to reduce the physical size of inductive elements and cost [14,15]. Moreover, an LCL-filter

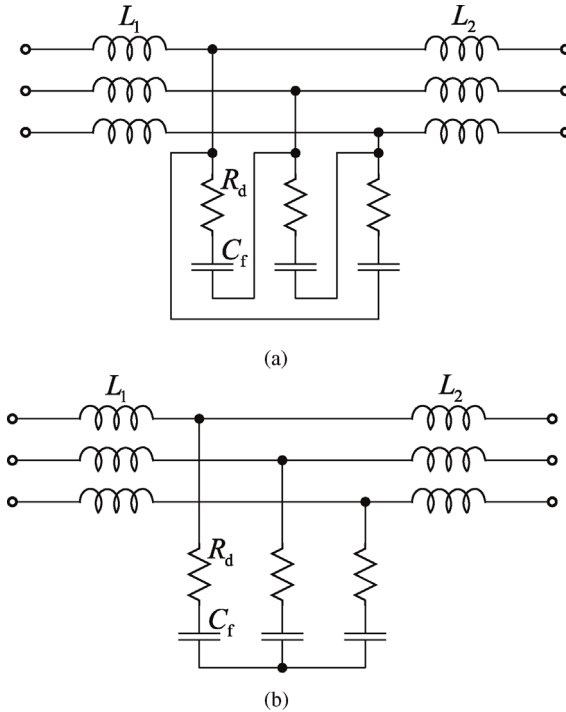


Figure 14.34 Passively damped LCL-filter with (a) delta-connected and (b) star-connected AC capacitor.

provides better attenuation of switching harmonics. Figure 14.34 shows two typical three-phase LCL-filters with passive damping. The AC capacitors can be connected to either star or delta configuration. The operational principle of these two types of filters is basically the same and in this book the emphasis is on the star-connected LCL-filter in Figure 14.34b.

In some cases the inverter utilizes an LC-type output filter where the leakage inductance of an isolation transformer effectively forms the grid-side inductive filter element. A transformer isolated inverter is illustrated in Figure 14.35, where L_{tf} denotes the internal inductance of the transformer. It could be possible to derive the whole model of the inverter again by analyzing the AC capacitors as a part of the power stage. However, the filter can also be added as a load effect to avoid lengthy derivation of a new dynamic model.

The AC capacitor can be depicted in the phase-domain as in Figure 14.36. The capacitor is assumed to be fed from an ideal three-phase current source and loaded by ideal three-phase voltage source. The capacitor voltage in phase i is determined by the capacitor current that again depends on the difference in capacitor voltage and grid voltage and the value of the damping resistor R_d according to Eq. (14.76). The average voltage v_{nS} is virtually zero in a balanced grid and can be neglected in the analysis for simplicity.

$$C_f \frac{d}{dt}(v_{Cfi}) = \frac{(v_{in} - v_{Cfi} - v_{nS})}{R_d}. \quad (14.76)$$

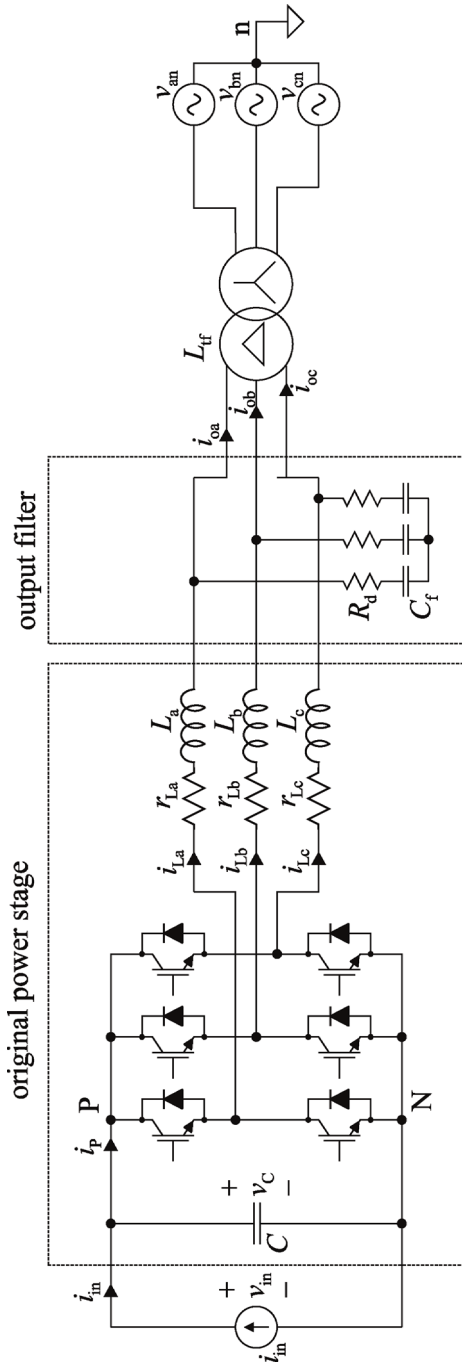


Figure 14.35 Grid-connected inverter with LC-filter.

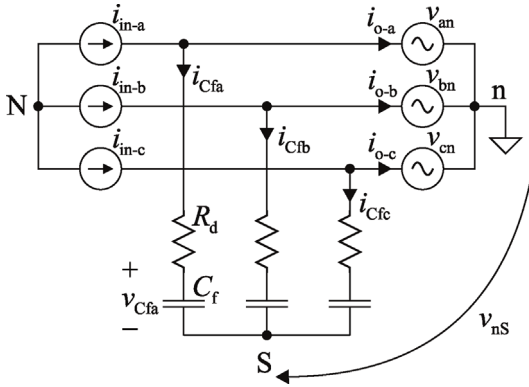


Figure 14.36 Star-connected AC capacitor in the phase-domain.

The three-phase voltage and currents can be written using vectors as

$$C_f \frac{d}{dt} \begin{bmatrix} v_{Cfa} \\ v_{Cfb} \\ v_{Cfc} \end{bmatrix} = \frac{1}{R_d} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} - \frac{1}{R_d} \begin{bmatrix} v_{Cfa} \\ v_{Cfb} \\ v_{Cfc} \end{bmatrix} - \frac{v_{nS}}{R_d}. \quad (14.77)$$

Capacitor voltages can be represented in the stationary reference frame by multiplying the current and voltage vectors by the Clarke's transformation matrix and given as in Eqs. (14.78) and (14.79).

$$C_f \frac{d}{dt} \begin{bmatrix} v_{Cf\alpha} \\ v_{Cf\beta} \\ v_{Cf0} \end{bmatrix} = \frac{1}{R_d} \begin{bmatrix} v_{o\alpha} \\ v_{o\beta} \\ v_0 \end{bmatrix} - \frac{1}{R_d} \begin{bmatrix} v_{Cf\alpha} \\ v_{Cf\beta} \\ v_{Cf0} \end{bmatrix}. \quad (14.78)$$

$$C_f \frac{d}{dt} \mathbf{v}_{Cf}^{\alpha\beta} = \frac{1}{R_d} \mathbf{v}_o^{\alpha\beta} - \frac{1}{R_d} \mathbf{v}_{Cf}^{\alpha\beta}. \quad (14.79)$$

After applying Eq. (12.6), the capacitor voltage can be given in the dq-domain as

$$C_f \frac{d}{dt} v_{cd} = \frac{(v_{od} - v_{cd})}{R_d} + \omega_s C_f v_{cq}, \quad (14.80)$$

$$C_f \frac{d}{dt} v_{cq} = \frac{(v_{oq} - v_{cq})}{R_d} - \omega_s C_f v_{cd}. \quad (14.81)$$

The capacitor currents depend on the voltage difference between output voltage and capacitor voltage and the value of damping resistor, similarly as in Eq. (14.76). However, the capacitor has cross-couplings between the d and q-components that are represented as current sources parallel to each capacitor. The capacitor can be depicted in the dq-domain as in Figure 14.37.

It is assumed that the cross-coupling terms $\omega_s C_f v_{cq}$ and $-\omega_s C_f v_{cd}$ are small enough to be neglected in the following analysis. After all, the goal of this chapter is to provide a reduced-order model of the inverter with less complexity. The output current controlled inverter with L-type output filter, or the “original power stage” in Figure 14.35 can be treated as a source system. Moreover, the AC capacitor can be treated as a load system. The transformer is left out of the analysis since the interest

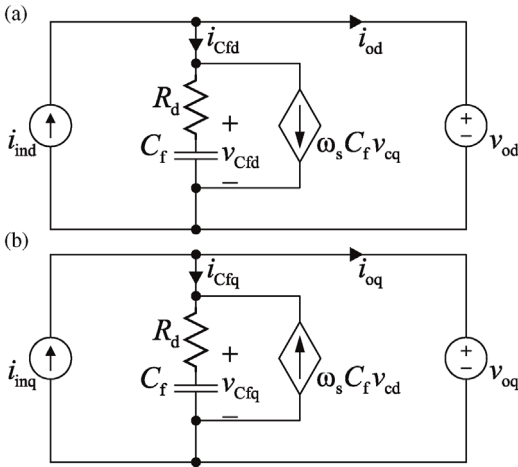


Figure 14.37 (a) d-components and (b) q-components of a star-connected capacitor in the d-q domain.

lies in how the AC capacitor affects the inverter impedance. The linear equivalent circuit of the inverter with AC capacitor is as shown in Figure 14.38. The circuit includes only the transfer functions that were derived in the previous section and that are relevant for the reduced-order model.

Admittance of the output capacitor can be given as

$$Y_{\text{Cap-d}} = Y_{\text{Cap-q}} = \frac{sC_f}{(R_d C_f s + 1)}. \tag{14.82}$$

According to basic circuit theory, admittances connected in parallel can be summed together to get the total admittance of the circuit. Therefore, the output impedance d- and q-components of the current-fed inverter with LC output filter can be given as in (14.83) and (14.84), where $Y_{\text{odd-c}}$ and $Y_{\text{oqq-c}}$ are the closed-loop admittances of the inverter with L-type output filter. The closed-loop admittances include all control functions, such as the grid voltage feedforward, and can be modeled based on the previous section.

$$Z_{\text{odd-c}}^{\text{LC}} = (Y_{\text{odd-c}} + Y_{\text{Cap-d}})^{-1}. \tag{14.83}$$

$$Z_{\text{oqq-c}}^{\text{LC}} = (Y_{\text{oqq-c}} + Y_{\text{Cap-q}})^{-1}. \tag{14.84}$$

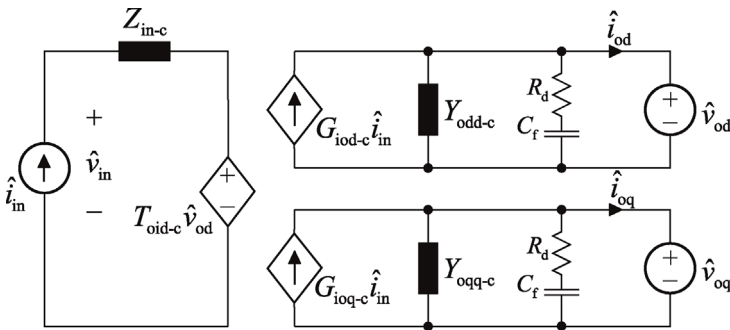


Figure 14.38 Reduced-order linear equivalent circuit of the inverter with LC-filter.

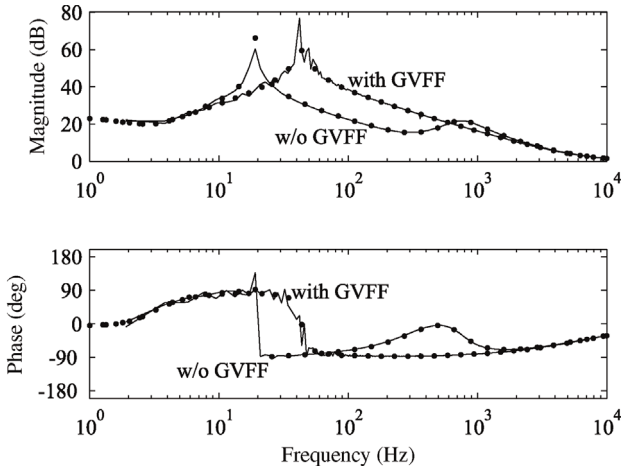


Figure 14.39 Analytical (dotted) and simulated (solid) output impedance d-component.

Figure 14.39 shows the inverter output impedance d-component with and without grid voltage feedforward when the inverter has an output LC-filter. The impedances were extracted from a simulator. In the previous chapter, it was shown that the magnitude of inverter output impedance tends to infinity at high frequencies. However, the situation is different when the inverter is interfaced with an AC capacitor. The high-frequency impedance is determined by the parallel connected capacitor as can be analyzed by studying Figure 14.38. Therefore, it is natural to expect that the impedance magnitude decreases as frequency increases. The same applies regardless whether the proportional grid voltage feedforward is used or not. Actually, the grid voltage feedforward gain should be a transfer function of higher order to increase the impedance at frequencies higher than the resonant frequency of the output filter, as discussed, for example, in Refs [16–18] (Figure 14.40).

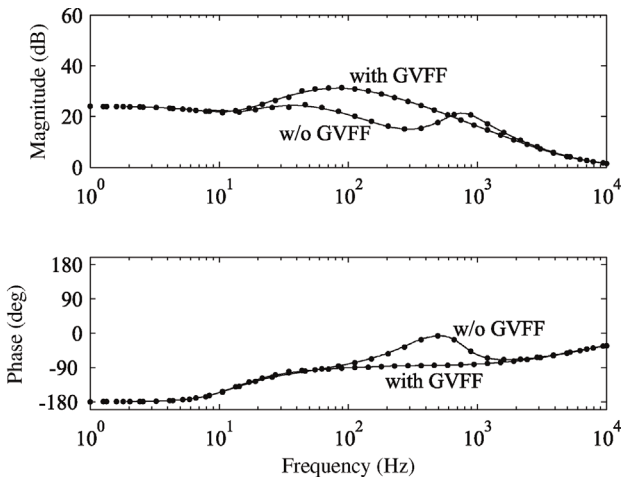


Figure 14.40 Output impedance q-component with and without grid voltage feedforward.

14.4.1 Experimental Verification of Impedance Model

Figure 14.41 shows the experimental setup that was used to measure inverter output impedance in the dq-domain. Moreover, the effect of feedforward on power quality was demonstrated. The inverter was fed from an electrical PV emulator and loaded by a three-phase grid emulated. An isolation transformer was connected between the inverter and the grid emulator to mitigate common-mode currents. The control system was implemented using dSPACE real-time simulator. The FRA stands for a sine-sweep frequency response analyzer. Photograph of the laboratory setup is shown in Figure 14.42. The principle of impedance measurement is described in Ref. [19].

Figure 14.43 shows the grid currents of a photovoltaic inverter with and without grid voltage feedforward. The currents are sinusoidal and symmetric in both cases, which demonstrate that the feedforward does not diminish the quality of grid currents under normal operating conditions.

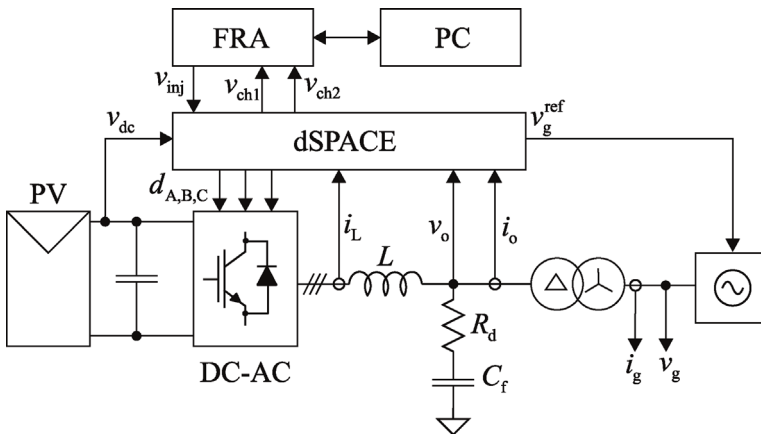


Figure 14.41 Experimental measurement setup.

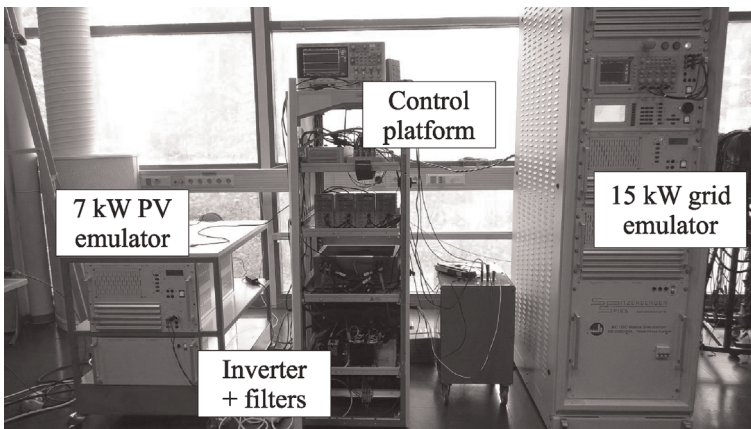


Figure 14.42 Photograph of the measurement setup.

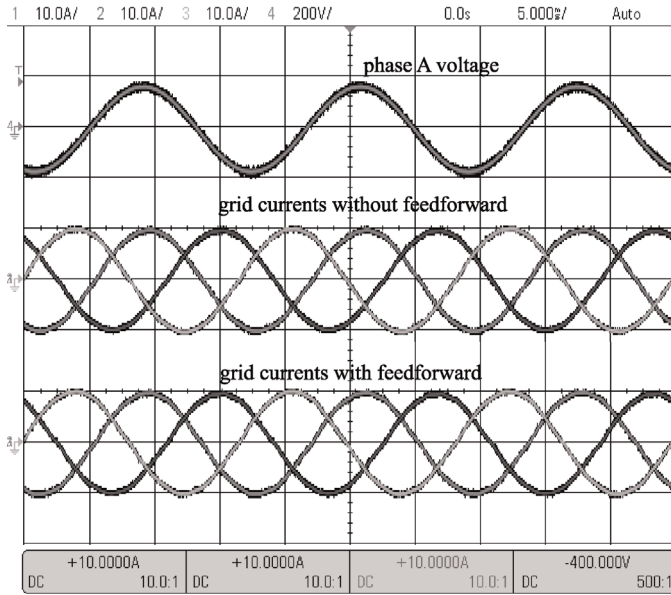


Figure 14.43 Grid currents of photovoltaic inverter in a clean grid with and without feedforward.

Figures 14.44 and 14.45 show the measured impedance d and q-components with and without feedforward. The shape is essentially the same as in the impedances that were extracted from a switching model. The inverter impedance has significantly larger magnitude when the grid voltage feedforward is used. Due to measurement noise, it is challenging to extract the impedance d-component around the fundamental frequency. The inverter was operated at 60Hz frequency, while the grid where laboratory equipment is connected into has 50 Hz frequency. The noise prevents extracting the impedance at these frequencies.

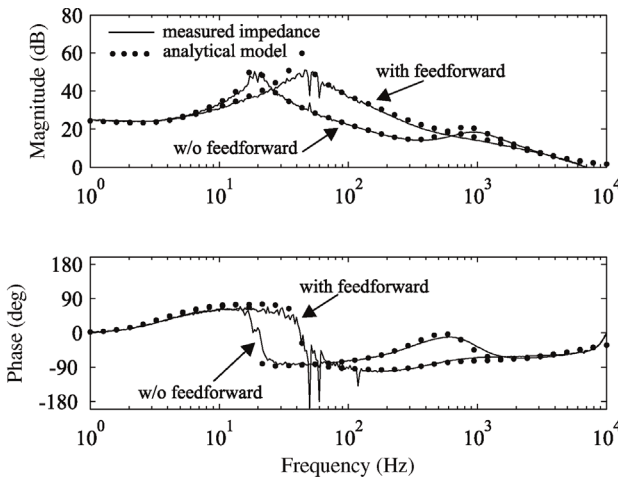


Figure 14.44 Measured inverter output impedance d-component with LC-filter Z_{odd-c}^{LC} .

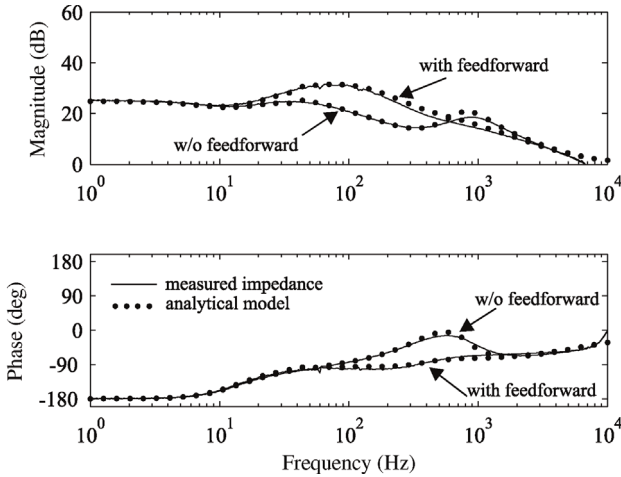


Figure 14.45 Measured inverter output impedance q-component with LC-filter Z_{oqq-c}^{LC} .

The references of three-phase grid voltages are generated by the dSPACE real-time simulator that allows arbitrary waveforms to be generated. 3% of fifth harmonic was added to each phase voltage reference to study the effect of feedforward on the power quality in a distorted grid. The fifth harmonic can be given in the stationary reference frame as

$$\mathbf{v}_{fifth}^{\alpha\beta} = V_{fifth}(\cos(5\omega_s t) + j\sin(5\omega_s t)), \tag{14.85}$$

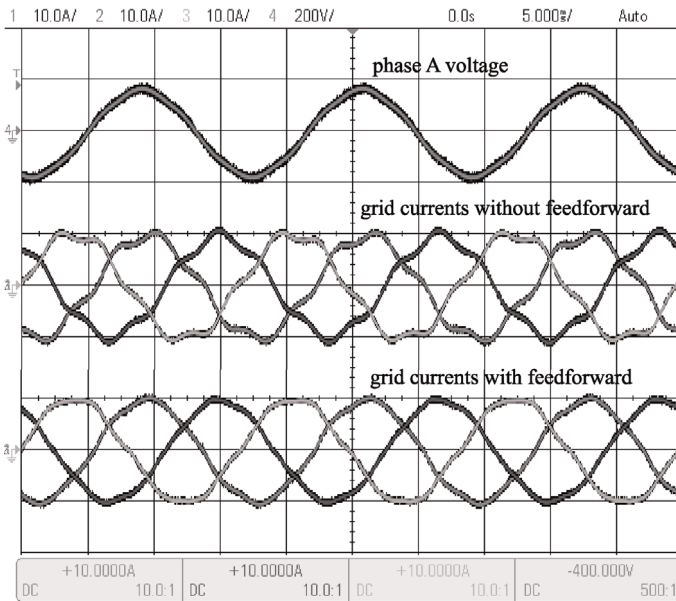


Figure 14.46 Grid currents when grid voltages have fifth harmonic.

which can be further given in the dq-domain as

$$\mathbf{v}_{\text{fifth}}^{\text{dq}} = \mathbf{v}_{\text{fifth}}^{\alpha\beta} \cdot e^{-j\omega_s t} = V_{\text{fifth}}(\cos(5\omega_s t) + j \sin(5\omega_s t)) \cdot (\cos(\omega_s t) - j \sin(\omega_s t)). \tag{14.86}$$

By using trigonometric identities, the fifth harmonic can be given as

$$\mathbf{v}_{\text{fifth}}^{\text{dq}} = V_{\text{fifth}}(\cos(4\omega_s t) + j \sin(4\omega_s t)), \tag{14.87}$$

which corresponds to a frequency component of 240 Hz in the dq-domain. Both impedance d and q-component have significantly larger magnitude at 240 Hz when feedforward is activated as can be seen by studying the impedances in Figures 14.44 and 14.45. Therefore, the inverter produces significantly less harmonic currents at the fifth harmonic when feedforward is used. Figure 14.46 shows the grid currents when grid voltages were intentionally distorted. The use of grid voltage feedforward is often supported by observations that it improves inverter transient response by compensating the effect of changing grid voltage. However, it is important to also consider the effect of feedforward on inverter output impedance.

The impedance magnitude of output-current-controlled inverter, such as a photovoltaic inverter, determines how much the inverter produces harmonic currents in distorted grid. Thus, an inverter with large output impedance generates less distortion to the grid. However, the magnitude is not the only property to consider in grid-connected inverters. Another important property that deserves attention is the passive/nonpassive properties of the impedance. Sufficient condition to guarantee stability of a grid-connected inverter is to assure that its output impedance remains passive, assuming the grid impedance also presents passive characteristics.

Figure 14.47 shows the measured inverter output impedance q-component when the feedforward gain was selected as $0.5/V_{\text{in}}$, $1/V_{\text{in}}$, and $1.5/V_{\text{in}}$. The optimal value for the feedforward is the inverse of DC voltage steady-state value.

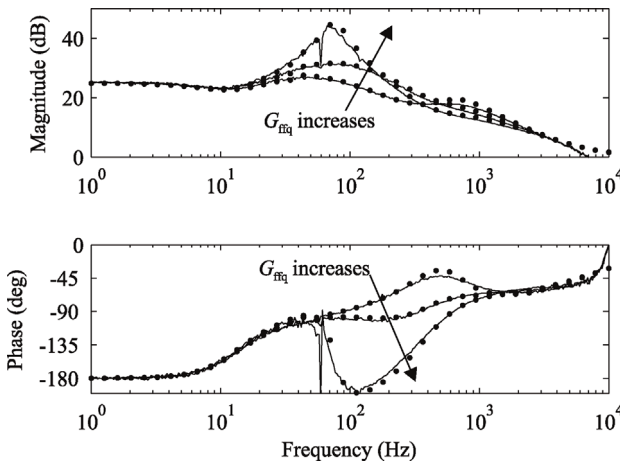


Figure 14.47 Measured output impedance q-component $Z_{\text{oq-q-c}}^{\text{LC}}$ with different values of feedforward gain.

The impedance magnitude increases when the feedforward gain is selected beyond the optimal value. Large feedforward gain also introduces an additional resonance around 70 Hz. However, the impedance loses its passive characteristics. The phase of the impedance experiences a severe drop after approximately few tens of hertz. Such behavior should be avoided to reduce the possibility of unstable impedance-based interactions. Therefore, the feedforward gain should be kept below $1/V_{in}$.

Another concern with the feedforward is the control system delay. The delay is caused by the control system and the SPWM modulator. Commonly, the delay is approximated as $1.5 \times$ the switching period. The SPWM modulator causes on the average a delay of half a switching cycle, and the control system (DSP-based) causes a delay equal to one switching cycle when its execution is synched to AD-conversion.

Figure 14.48 shows the measured impedance d-component and the impedance given by the analytical impedance model. The control delay was approximated as 1.5 times the switching cycle T_s during the first impedance measurement. An additional delay of 1.5 times the switching cycle was added in the control system running on dSPACE to demonstrate the detrimental effect of large delay, that is, the total delay corresponds to three times the switching cycle. The switching frequency was set to 20 kHz. The delay was included in the analytical model as a second-order Padé approximation as given in Eq. (14.88), where T_d is the total amount of delay. Impedance magnitude experiences a slight drop when delay increases. The effect of delay in the phase behavior is more severe. The phase impedance is already nonpassive around 100 Hz, that is, having phase less than -90° . However, when the delay is increased the phase drops down to approximately -115° as can be seen from the zoomed figure.

$$G_{ffd} = G_{ffq} = \frac{1}{V_{in}} \cdot \left\{ \left[1 - \frac{T_d}{2}s + \frac{T_d^2}{12}s^2 \right] / \left[1 + \frac{T_d}{2}s + \frac{T_d^2}{12}s^2 \right] \right\}. \quad (14.88)$$

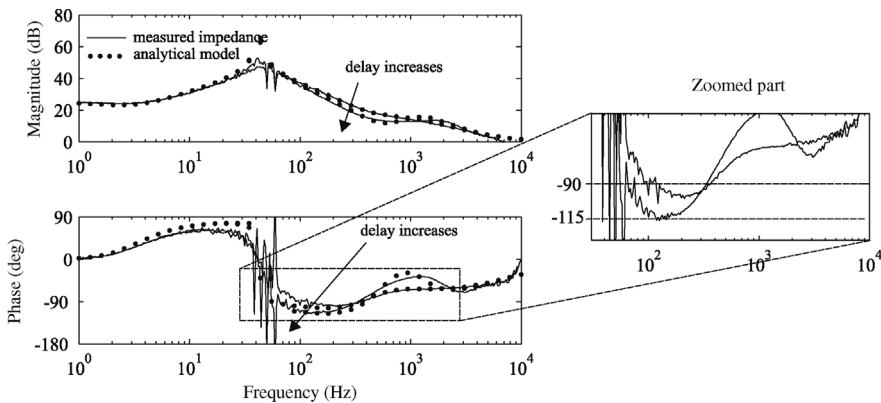


Figure 14.48 Measured output impedance d-component Z_{odd-c}^{LC} with feedforward and increasing control delay.

14.4.2 Impedance Characteristics of Inverter with LC-Filter and Feedforward

Based on the above discussion, few key features and challenges of grid voltage feedforward should be pointed out.

- Feedforward increases the magnitude of both impedance d and q-components. However, the high-frequency magnitude of the impedance is determined by the AC capacitor and cannot be influenced by conventional proportional feedforward.
- Large output impedance naturally means that the inverter generates less harmonic distortion in a distorted grid. Thus, inverter with grid voltage feedforward generally provides better power quality than inverter without feedforward.
- The feedforward gain should not be selected larger than the inverse of DC voltage $1/V_{in}$ when conventional SPWM is used. The situation may be different when space-vector-based modulator (SV-PWM) is used since these modulators often utilize the measured DC voltage in determining suitable switching vectors. However, SV-PWM is out of the scope of this book. Too large feedforward gain causes the inverter impedance to lose its passive characteristics that can cause impedance-based interactions and instability, as will be discussed more in detail in Chapter 16.
- Control delay caused the impedance to lose its passive characteristics by decreasing the impedance phase below -90° . The effect of delay can be somewhat mitigated by reducing the feedforward gain.

14.5 Summary

Closed-loop models of voltage and current-fed inverters were derived in this chapter to characterize the effect of different control functions to inverter output impedance. The models were developed by assuming that the cross-coupling transfer functions can be neglected. Impedances were extracted from simulation models and prototype inverters to verify the accuracy of the closed-loop models. The impedances given by the model were found out to correlate very well with the measurements. Thus, the impedance models presented in this chapter are suitable to be used in impedance-based stability analysis of grid-connected inverters and for evaluating the amount of generated harmonic currents in distorted grid conditions.

References

- 1 Mao, H., Boroyevich, D., and Lee, F.C. (1998) Novel reduced-order small-signal model of a three-phase PWM rectifier and its application in control design and system analysis. *IEEE Trans. Power Electron.*, **13** (3), 511–521.

- 2 Burgos, R., Boroyevich, D., Wang, F., Karimi, K., and Francis, G. (2010) On the Ac stability of high power factor three-phase rectifiers. 2010 IEEE Energy Conversion Congress and Exposition, pp. 2047–2054.
- 3 Sun, J. (2011) Impedance-based stability criterion for grid-connected inverters. *IEEE Trans. Power Electron.*, **26** (11), 3075–3078.
- 4 Messo, T., Jokipii, J., Makinen, A., and Suntio, T. (2013) Modeling the grid synchronization induced negative-resistor-like behavior in the output impedance of a three-phase photovoltaic inverter. 2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 1–7.
- 5 Wen, B., Boroyevich, D., Burgos, R., Mattavelli, P., and Shen, Z. (2016) Analysis of D - Q small-signal impedance of grid-tied inverters. *IEEE Trans. Power Electron.*, **31** (1), 675–687.
- 6 Alawasa, K.M., Mohamed, Y.A.-R.I., and Xu, W. (2014) Active mitigation of subsynchronous interactions between PWM voltage-source converters and power networks. *IEEE Trans. Power Electron.*, **29** (1), 121–134.
- 7 Cespedes, M. and Sun, J. (2011) Modeling and mitigation of harmonic resonance between wind turbines and the grid. 2011 IEEE Energy Conversion Congress and Exposition, pp. 2109–2116.
- 8 Harnefors, L., Bongiorno, M., and Lundberg, S. (2007) Input-admittance calculation and shaping for controlled voltage-source converters. *IEEE Trans. Ind. Electron.*, **54** (6), 3323–3334.
- 9 Wen, B., Boroyevich, D., Burgos, R., and Mattavelli, P. (2013) Input impedance of voltage source converter with stationary frame linear current regulators and phase-locked loop. 2013 IEEE Energy Conversion Congress and Exposition, pp. 4207–4213.
- 10 Timbus, A., Liserre, M., Teodorescu, R., Rodriguez, P., and Blaabjerg, F. (2009) Evaluation of current controllers for distributed power generation systems. *IEEE Trans. Power Electron.*, **24** (3), 654–664.
- 11 Xue, M., Zhang, Y., Kang, Y., Yi, Y., Li, S., and Liu, F. (2012) Full feedforward of grid voltage for discrete state feedback controlled grid-connected inverter with LCL filter. *IEEE Trans. Power Electron.*, **27** (10), 4234–4247.
- 12 Park, S.Y., Chen, C.L., Lai, J.S., and Moon, S. R. (2008) Admittance compensation in current loop control for a Grid-Tie LCL fuel cell inverter. *IEEE Trans. Power Electron.*, **23** (4), 1716–1723.
- 13 Li, W., Ruan, X., Pan, D., and Wang, X. (2013) Full-feedforward schemes of grid voltages for a three-phase LCL-type grid-connected inverter. *IEEE Trans. Ind. Electron.*, **60** (6), 2237–2250.
- 14 Rockhill, A.A., Liserre, M., Teodorescu, R., and Rodriguez, P. (2011) Grid-filter design for a multimewatt medium-voltage voltage-source inverter. *IEEE Trans. Ind. Electron.*, **58** (4), 1205–1217.
- 15 Liserre, M., Blaabjerg, F., and Hansen, S. (2005) Design and control of an LCL-filter-based three-phase active rectifier. *IEEE Trans. Ind. Appl.*, **41** (5), 1281–1291.
- 16 Xue, M., Zhang, Y., Kang, Y., Yi, Y., Li, S., and Liu, F. (2012) Full feedforward of grid voltage for discrete state feedback controlled grid-connected inverter with LCL filter. *IEEE Trans. Power Electron.*, **27** (10), 4234–4247.

- 17 Messo, T., Aapro, A., Suntio, T., and Roinila, T. (2016) Design of grid-voltage feedforward to increase impedance of grid-connected three-phase inverters with LCL-filter. 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), pp. 2675–2682.
- 18 Wang, X., Ruan, X., Liu, S., and Tse, C.K. (2010) Full feedforward of grid voltage for grid-connected inverter with LCL filter to suppress current distortion due to grid voltage harmonics. *IEEE Trans. Power Electron.*, **25** (12), 3119–3127.
- 19 Jokipii, J., Messo, T., and Suntio, T. (2014) Simple method for measuring output impedance of a three-phase inverter in dq-domain. 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), pp. 1466–1470.

15

Multivariable Closed-Loop Modeling of Inverters

15.1 Introduction

In the previous chapters, closed-loop models were derived by assuming that cross-coupling transfer functions can be neglected and that inverter input dynamics depend only on the d-components [1]. This is a good trade-off between complexity of the model and its accuracy. However, the cross-coupling transfer functions may affect the dynamic behavior and stability of the inverter, for example, on impedance-based stability margins [2].

This chapter demonstrates how the closed-loop model can be formulated without the need to neglect any dynamics. The model is solved by using two-by-two transfer matrices rather than reduced-order dynamics [3,4]. The reader is urged to familiarize with the modeling of multivariable systems by referring to Refs [5,6]. The multivariable model can be used to get more accurate predictions on impedance-based stability [7–9] and to include the effect of decoupling gains that are usually part of the current controller. The model is derived for an inverter with simple L-type output filter and with passively damped LCL-type output filter.

15.2 Full-Order Model of Current-Fed Inverter with L-Type Filter

Figure 15.1 shows a current-fed inverter with PLL, cascaded control scheme, and decoupling gains. The decoupling gains are chosen as in Eqs. (15.1) and (15.2) according to Ref. [10] and as discussed in Chapter 13.

$$G_{\text{dec-dq}} = \frac{\omega_s L}{V_{\text{in}}}, \quad (15.1)$$

$$G_{\text{dec-qd}} = -\frac{\omega_s L}{V_{\text{in}}}. \quad (15.2)$$

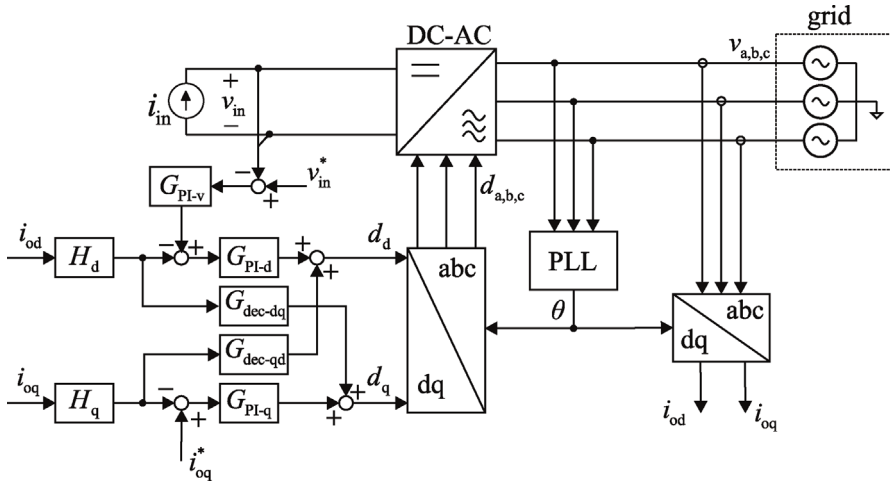


Figure 15.1 Inverter control system with decoupling gains.

The current controller defines the values of duty ratio d and q -components according to control laws in Eqs. (15.3) and (15.4):

$$\hat{d}_d = G_{PI-d} \left(\hat{i}_{od}^* - H_d \hat{i}_{od}^c \right) - \frac{\omega_s L}{V_{in}} H_q \hat{i}_{oq}^c, \quad (15.3)$$

$$\hat{d}_q = G_{PI-q} \left(\hat{i}_{oq}^* - H_q \hat{i}_{oq}^c \right) + \frac{\omega_s L}{V_{in}} H_d \hat{i}_{od}^c. \quad (15.4)$$

The superscript c denotes that the current is defined in the control system reference frame, that is, it is affected by the PLL. The PLL-affected d and q -components can be given in the control system reference frame according to Eq. (13.8) as follows:

$$\hat{x}_d^c = \hat{x}_d + \frac{X_q}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{oq}, \quad (15.5)$$

$$\hat{x}_q^c = \hat{x}_q - \frac{X_d}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{oq}. \quad (15.6)$$

Therefore, the current d and q -components can be given in the control system reference frame as

$$\hat{i}_{od}^c = \hat{i}_{od} + \frac{I_{oq}}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{oq}, \quad (15.7)$$

$$\hat{i}_{oq}^c = \hat{i}_{oq} - \frac{I_{od}}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{oq}. \quad (15.8)$$

Output current d and q -components can be given as a two-dimensional vector and defined in the control system reference frame according to Eq. (15.9), where

I_{oq} and I_{od} are the steady-state values of grid current.

$$\begin{bmatrix} \hat{i}_d^c \\ \hat{i}_q^c \end{bmatrix} = \begin{bmatrix} \hat{i}_d \\ \hat{i}_q \end{bmatrix} + \begin{bmatrix} 0 & I_{oq} \\ 0 & -I_{od} \end{bmatrix} \cdot \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (15.9)$$

Output current can be defined using vectors as

$$\mathbf{i}_o^c = \mathbf{i}_o + \mathbf{I}_L \cdot \mathbf{G}_{PLL} \cdot \mathbf{v}_o. \quad (15.10)$$

The closed-loop model should be defined in the ideal grid reference frame, in order to include the effect of PLL in the model. The principle is exactly the same as in Section 14.3. However, in this case, the closed-loop model is formulated by using two-by-two transfer matrices to include the cross-coupling transfer functions and decoupling gains. The duty ratio is determined by the current controller in the control system reference frame and can be given in the grid reference frame by applying Eqs. (15.5) and (15.6) and given as

$$\hat{d}_d = \hat{d}_d^c - \frac{D_q}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{oq}, \quad (15.11)$$

$$\hat{d}_q = \hat{d}_q^c + \frac{D_d}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \hat{v}_{od}. \quad (15.12)$$

The duty ratio vector can be defined in the grid reference frame as

$$\begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} = \begin{bmatrix} \hat{d}_d^c \\ \hat{d}_q^c \end{bmatrix} + \begin{bmatrix} 0 & -D_q \\ 0 & D_d \end{bmatrix} \cdot \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (15.13)$$

or as

$$\mathbf{d} = \mathbf{d}^c + \mathbf{D} \cdot \mathbf{G}_{PLL} \cdot \mathbf{v}_o. \quad (15.14)$$

The output of the current controller, that is, the duty ratio in the control system reference frame can be defined as in Eq. (15.15) by taking into account the control laws in Eqs. (15.3) and (15.4).

$$\begin{aligned} \begin{bmatrix} \hat{d}_d^c \\ \hat{d}_q^c \end{bmatrix} &= \begin{bmatrix} G_{PI-d} & 0 \\ 0 & G_{PI-q} \end{bmatrix} \left(\begin{bmatrix} \hat{i}_{od}^* \\ \hat{i}_{oq}^* \end{bmatrix} - \begin{bmatrix} H_d & 0 \\ 0 & H_q \end{bmatrix} \begin{bmatrix} \hat{i}_{od}^c \\ \hat{i}_{oq}^c \end{bmatrix} \right) \\ &+ \begin{bmatrix} 0 & -\frac{\omega_s L}{V_{in}} \\ \frac{\omega_s L}{V_{in}} & 0 \end{bmatrix} \begin{bmatrix} H_d & 0 \\ 0 & H_q \end{bmatrix} \begin{bmatrix} \hat{i}_{od}^c \\ \hat{i}_{oq}^c \end{bmatrix} \end{aligned} \quad (15.15)$$

Duty ratio can be written using vectors as

$$\mathbf{d}^c = \mathbf{G}_{c-out} (\mathbf{i}_o^* - \mathbf{H}_{out} \mathbf{i}_o^c) + \mathbf{G}_{dec} \mathbf{H}_{out} \mathbf{i}_o^c. \quad (15.16)$$

The full-order control block diagram that represents the inverter output dynamics can be depicted by including Eqs. (15.10), (15.14), and (15.16) in the inverter open-loop output dynamics, as shown in Figure 15.2.

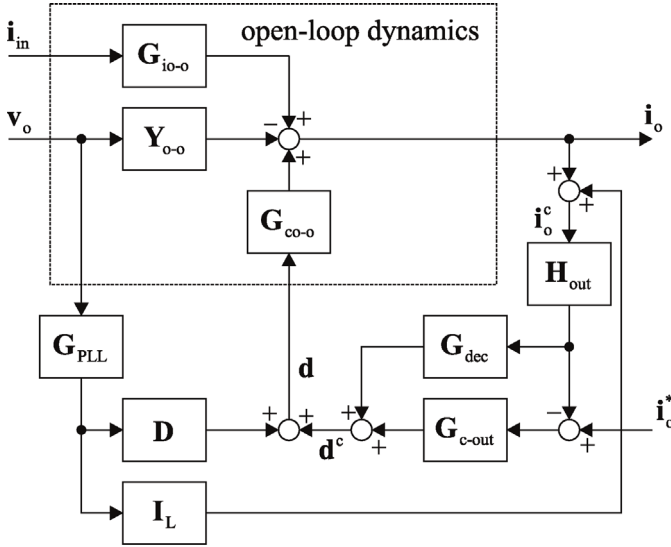


Figure 15.2 Full-order closed-loop model with current control and PLL (output dynamics).

Closed-loop model is solved using the same approach that was used to derive the reduced-order model. First, the transfer matrices are solved from Figure 15.2 when all the inner control loops are closed, that is, PLL and current control. As an example, the input-to-output transfer matrix G_{io}^{cc} is solved by setting all inputs other than i_{in} to zero (i.e., v_o and i_o^*) and solving the closed-loop transfer matrix from input current i_{in} to output current i_o that can be given according to Eq. (15.17):

$$G_{io}^{cc} = (I + L_{cc} - L_{dec})^{-1} G_{io-o}. \tag{15.17}$$

The loop gains are defined as $L_{cc} = G_{co-o} G_{c-out} H_{out}$ and $L_{dec} = G_{co-o} G_{dec} H_{out}$. Transfer matrix G_{io-o} is defined as in Eq. (15.18) and G_{co-o} as in Eq. (15.19). The transfer functions inside the matrices are solved based on the methods presented in Chapter 12.

$$G_{io-o} = \begin{bmatrix} G_{iod-o} & 0 \\ G_{ioq-o} & 0 \end{bmatrix}, \tag{15.18}$$

$$G_{co-o} = \begin{bmatrix} G_{codd-o} & G_{coqd-o} \\ G_{codq-o} & G_{coqq-o} \end{bmatrix}. \tag{15.19}$$

Transfer matrix from output voltage v_o to output current i_o , that is, the output admittance matrix, can be solved from Figure 15.3 using the same principle and given as

$$Y_o^{cc} = (I + L_{cc} - L_{dec})^{-1} (Y_{o-o} + Y_{PLL}). \tag{15.20}$$

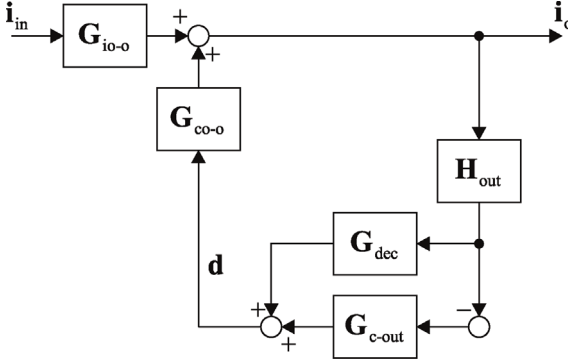


Figure 15.3 Block diagram to solve input-to-output transfer matrix \mathbf{G}_{io-c} .

The admittance term caused by the PLL can be defined as in Eq. (15.21) and the open-loop output admittance matrix as in Eq. (15.22):

$$\mathbf{Y}_{PLL} = ((\mathbf{L}_{cc} - \mathbf{L}_{dec})\mathbf{I}_L - \mathbf{G}_{co-o}\mathbf{D})\mathbf{G}_{PLL}, \quad (15.21)$$

$$\mathbf{Y}_{o-o} = \begin{bmatrix} Y_{odd-o} & Y_{oqd-o} \\ Y_{odq-o} & Y_{oqq-o} \end{bmatrix}. \quad (15.22)$$

Transfer matrix from output current reference \mathbf{i}_o^* to output current \mathbf{i}_o can be given as

$$\mathbf{G}_{co}^{cc} = (\mathbf{I} + \mathbf{L}_{cc} - \mathbf{L}_{dec})^{-1}\mathbf{L}_{cc}(\mathbf{H}_{out})^{-1}. \quad (15.23)$$

Finally, the output dynamics can be given as

$$\mathbf{i}_o = \mathbf{G}_{io}^{cc}\mathbf{i}_{in} - \mathbf{Y}_o^{cc}\mathbf{v}_o + \mathbf{G}_{co}^{cc}\mathbf{i}_o^*. \quad (15.24)$$

The input current is defined as a vector $\mathbf{i}_{in} = [\hat{i}_{in} \ 0]^T$, output voltage as $\mathbf{v}_o = [\hat{v}_{od} \ \hat{v}_{oq}]^T$, and output current reference as $\mathbf{i}_o^* = [\hat{i}_{od}^* \ \hat{i}_{oq}^*]^T$.

The input dynamics can be depicted as in Figure 15.4, where the duty ratio \mathbf{d} is determined by current controllers. The duty ratio can be solved from the closed-loop output dynamics in Figure 15.2 and given according to Eq. (15.25).

$$\mathbf{d} = (\mathbf{D} - (\mathbf{G}_{co-o})^{-1}(\mathbf{L}_{cc} - \mathbf{L}_{dec})\mathbf{I}_L)\mathbf{G}_{PLL}\mathbf{v}_o + \mathbf{G}_{c-out}\mathbf{i}_o^* - (\mathbf{G}_{co-o})^{-1}(\mathbf{L}_{cc} - \mathbf{L}_{dec})\mathbf{i}_o. \quad (15.25)$$

According to Eq. (15.25) and Figure 15.4, the input dynamics can be redrawn as in Figure 15.5 that accounts for the effect of the PLL and the output current control. The transfer matrices from output voltage and output current to duty ratio are defined as in Eqs. (15.26) and (15.27) to simplify the notation.

$$\mathbf{G}'_{PLL} = (\mathbf{D} - (\mathbf{G}_{co-o})^{-1}(\mathbf{L}_{cc} - \mathbf{L}_{dec})\mathbf{I}_L)\mathbf{G}_{PLL}, \quad (15.26)$$

$$\mathbf{G}'_{cc} = (\mathbf{G}_{co-o})^{-1}(\mathbf{L}_{cc} - \mathbf{L}_{dec}). \quad (15.27)$$

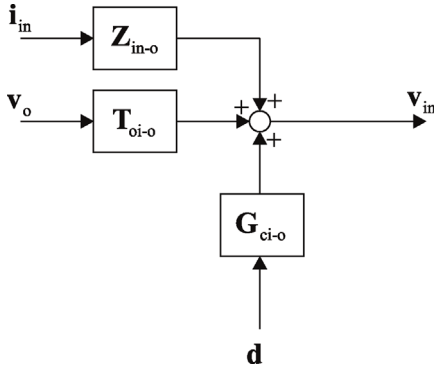


Figure 15.4 Input dynamics at open loop.

The closed-loop input dynamics can be solved by applying the results obtained earlier, that is, by substituting the closed-loop output dynamics of Eq. (15.24) into the block diagram in Figure 15.5. The resulting block diagram can be depicted as in Figure 15.6.

The input impedance can be solved from the block diagram by setting output voltage v_o and output current reference i_o^* equal to zero and solving the transfer matrix from input current i_{in} to input voltage v_{in} . Input impedance can be given as

$$Z_{in}^{cc} = Z_{in-o} - G_{ci-o} G'_{cc} G_{io}^{cc} \tag{15.28}$$

Accordingly, the output-to-input voltage and reference-to-input-voltage transfer matrices can be solved and given as in Eqs. (15.29) and (15.30). Finally, the input dynamics can be given as in Eq. (15.31) which includes the dynamic effects of PLL and output current control.

$$T_{oi}^{cc} = T_{oi-o} + G_{ci-o} (G'_{PLL} + G'_{cc} Y_o^{cc}), \tag{15.29}$$

$$G_{ci}^{cc} = G_{ci-o} G_{c-out} - G_{ci-o} G'_{cc} G_{co}^{cc}, \tag{15.30}$$

$$v_{in} = Z_{in}^{cc} i_{in} + T_{oi}^{cc} v_o + G_{ci}^{cc} i_o^* \tag{15.31}$$

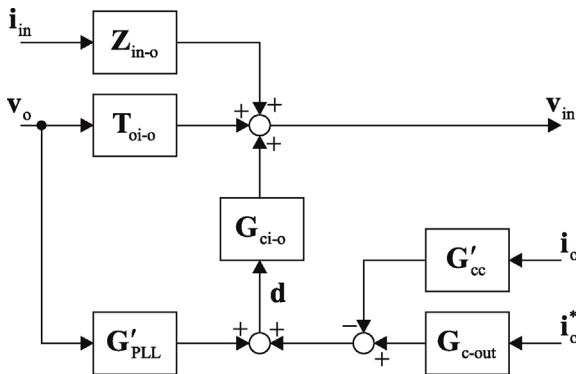


Figure 15.5 Input dynamics with the PLL loop closed and the feedback from output current.

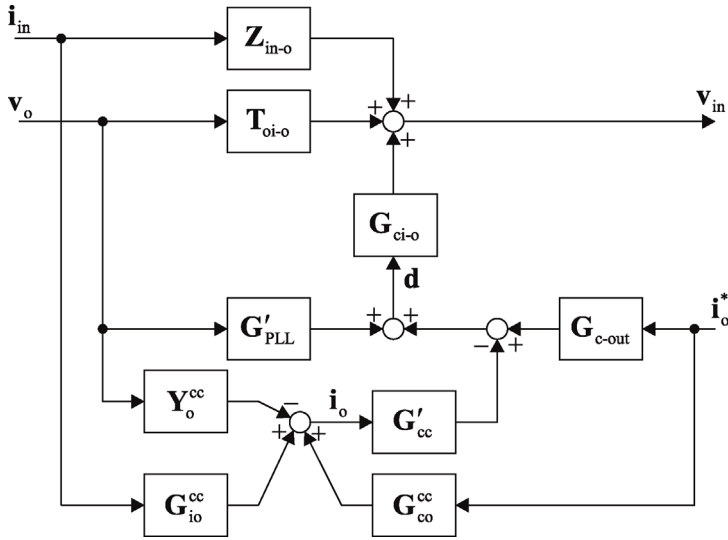


Figure 15.6 Control block diagram representing the closed-loop dynamics with PLL and output current control.

The DC voltage control loop is included in the dynamic model next. As can be seen in Figure 15.1, the DC voltage controller G_{PI-v} determines the reference value of the output current d -component. The q -component is set to zero, for unity power factor operation or, alternatively, set by an outer control algorithm, such as a grid voltage support function. However, for the purpose of the dynamic model presented in this book, the reference of output current q -component can be assumed as an input variable.

For the correct formulation of the full-order model, the voltage controller has to be defined as in (15.32), where G_{PI-v} is the transfer function of input voltage controller and the unity gain on the second row passes the reference of output current q -component through the matrix unchanged. The input voltage \mathbf{v}_{in} is treated as a two-dimensional vector, even though its second component is evidently zero, that is, $\mathbf{v}_{in} = [\hat{v}_{in} \ 0]$. Moreover, the input voltage sensing gain is defined as in Eq. (15.33) because the inverter input terminal is a DC system, rather than a three-phase system defined in the dq -domain.

$$\mathbf{G}_{c-in} = \begin{bmatrix} G_{PI-v} & 0 \\ 0 & 1 \end{bmatrix}, \quad (15.32)$$

$$\mathbf{H}_{in} = \begin{bmatrix} H_v & 0 \\ 0 & 0 \end{bmatrix}. \quad (15.33)$$

Input dynamics can be represented as a control block diagram according to Figure 15.7 after closing the DC voltage control loop.

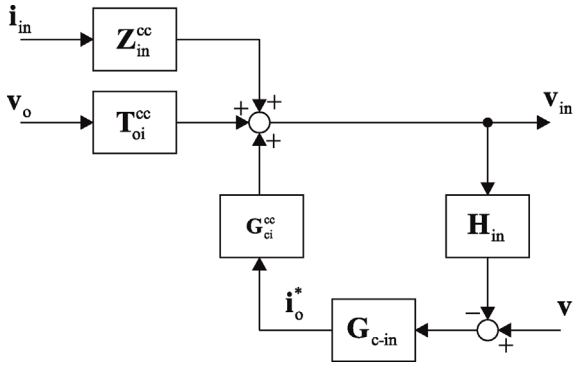


Figure 15.7 Input dynamics with DC voltage control loop closed.

The input dynamics can be solved from Figure 15.7 and given as in Eqs. (15.34)–(15.36):

$$\mathbf{Z}_{in-c} = (\mathbf{I} + \mathbf{L}_{in})^{-1} \mathbf{Z}_{in}^{cc}, \quad (15.34)$$

$$\mathbf{T}_{oi-c} = (\mathbf{I} + \mathbf{L}_{in})^{-1} \mathbf{T}_{oi}^{cc}, \quad (15.35)$$

$$\mathbf{G}_{ci-c} = (\mathbf{I} + \mathbf{L}_{in})^{-1} \mathbf{G}_{ci}^{cc} \mathbf{G}_{c-in}. \quad (15.36)$$

The input control loop gain is defined as

$$\mathbf{L}_{in} = \mathbf{G}_{ci}^{cc} \mathbf{G}_{c-in} \mathbf{H}_{in}. \quad (15.37)$$

Finally, the input voltage \mathbf{v}_{in} can be written as

$$\mathbf{v}_{in} = \mathbf{Z}_{in-c} \mathbf{i}_{in} + \mathbf{T}_{oi-c} \mathbf{v}_o + \mathbf{G}_{ci-c} \mathbf{v}^*. \quad (15.38)$$

Figure 15.8 shows the control block diagram that describes the output dynamics when DC voltage control loop is closed and the closed-loop transfer matrices of Eqs. (15.34)–(15.36) are included in the block diagram.

Closed-loop transfer matrices can be solved from Figure 15.8 and given as in Eqs. (15.39)–(15.41):

$$\mathbf{G}_{io-c} = \mathbf{G}_{io}^{cc} - \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} \mathbf{H}_{in} \mathbf{Z}_{in-c}, \quad (15.39)$$

$$\mathbf{Y}_{o-c} = \mathbf{Y}_o^{cc} + \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} \mathbf{H}_{in} \mathbf{T}_{oi-c}, \quad (15.40)$$

$$\mathbf{G}_{co-c} = \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} (\mathbf{I} - \mathbf{H}_{in} \mathbf{G}_{ri}). \quad (15.41)$$

Example m-files for solving the closed-loop transfer functions are shown in Figures 15.9 and 15.10. Parameter values, for example, values of passive

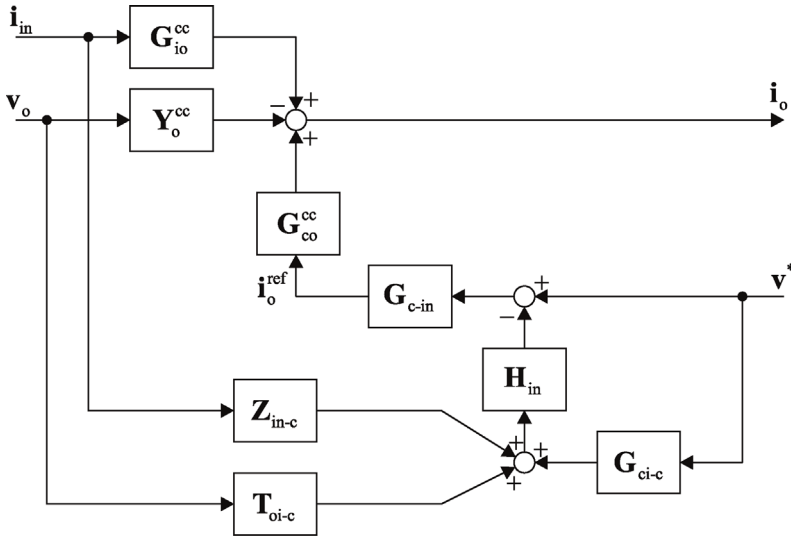


Figure 15.8 Output dynamics with DC voltage control loop closed.

```

% Open-loop transfer functions of current-fed inverter with L-
type output filter

run parameters %parameters defined in another file

s=tf('s');

A=[-r_eq/L, w_s, Dd/L;
   -w_s, -r_eq/L, Dq/L;
   -3*Dd/2/C, -3*Dq/2/C, 0];

B=[0, -1/L, 0, Vin/L, 0;
   0, 0, -1/L, 0, Vin/L;
   1/C, 0, 0, -3*ILd/2/C, -3*ILq/2/C];

C=[0, 0, 1;
   1, 0, 0;
   0, 1, 0];

D=0;

G=C*inv(s*eye(3)-A)*B+D;

% input dynamics at open-loop
Zin_o = [G(1,1), 0; 0, 0];
Toi_o = [G(1,2), G(1,3); 0, 0];
Gci_o = [G(1,4), G(1,5); 0, 0];

% output dynamics at open-loop
Gio_o = [G(2,1), 0; G(3,1), 0];
Yo_o = [-G(2,2), -G(2,3); -G(3,2), -G(3,3)];
Gco_o = [G(2,4), G(2,5); G(3,4), G(3,5)];

```

Figure 15.9 Example MATLAB file to solve open-loop transfer functions.

```

% Closed-loop transfer functions of current-fed inverter with L-
type output filter

run ctrl_tfs %controller parameters & -transfer
            %functions

%effect of PLL
G_pll = [0, 0; 0, 1/Vod*Lpll/(1+Lpll)];
D_ss = [0, -Dq; 0, Dd];
I_ss = [0, ILq; 0, -ILD];

%controller and sensing gain matrices
Gc_out = [GPId, 0; 0, GPIq];
Gc_dec = [0, Gdec_qd; Gdec_dq, 0];
H_out = [Hd, 0; 0, Hq];
Gc_in = [GPIv, 0; 0, 1];
H_in = [Hv, 0; 0, 0];

%loop gains and special transfer matrices
L_cc = Gco_o*Gc_out*H_out;
L_dec = Gco_o*Gc_dec*H_out;
I = [s, 0; 0, s];
Gp_pll = (D_ss-inv(Gco_o)*(L_cc-L_dec))*I_ss)*G_pll;
Gp_cc = inv(Gco_o)*(L_cc-L_dec);

%transfer functions with current control & PLL
Gio_cc = inv(I+Lcc-Ldec)*Gio_o;
Y_pll = ((L_cc-L_dec)*I_ss-Gco_o*D_ss)*G_pll;
Yo_cc = inv(I+L_cc-L_dec)*(Yo_o+Y_pll);
Gco_cc = inv(I+L_cc-L_dec)*L_cc*inv(H_out);
Zin_cc = Zin_o-Gci_o*Gp_cc*Gio_cc;
Toi_cc = Toi_o+Gci_o*(Gp_pll+Gp_cc*Yo_cc);
Gci_cc = Gci_o*Gc_out-Gci_o*Gp_cc*Gro_cc;

%transfer functions with input voltage control
L_in = Gri_cc*Gc_in*H_in;
Zin_c = inv(I+L_in)*Zin_cc;
Toi_c = inv(I+L_in)*Toi_cc;
Gci_c = inv(I+L_in)*Gri_cc*Gc_in;
Gio_c = Gio_cc-Gro_cc*Gc_in*H_in*Zin_c;
Yo_c = Yo_cc+Gro_cc*Gc_in*H_in*Toi_c;
Gco_c = Gro_cc*Gc_in*(I-H_in*Gri_c);

```

Figure 15.10 Example MATLAB file to solve closed-loop transfer functions.

components and steady-state operating point, are solved in an external file according to Eqs. (12.41)–(12.44), which is executed by running the line “run parameters.” Moreover, the controller transfer functions and the values for PI controller parameters are defined in an external file “ctrl_tfs.” The transfer functions should be converted to frequency-response data by using the `frd()` function of MATLAB to avoid inaccuracy due to high number of poles and zeros. Obtaining symbolic transfer functions with the cross-coupling dynamics is a far more complicated problem and is not covered in this book.

The closed-loop transfer matrices are elements of the resulting transfer matrix \mathbf{G}_H . Equation (15.42) illustrates the transfer matrices and Eq. (15.43) the individual transfer functions inside the transfer matrices. Note that some of the elements are zero due to the fact that input port of the corresponding

H -parameter model is a DC terminal.

$$\begin{bmatrix} \mathbf{v}_{in} \\ \mathbf{i}_o \end{bmatrix} = \overbrace{\begin{bmatrix} \mathbf{Z}_{in-c} & \mathbf{T}_{oi-c} & \mathbf{G}_{ri} \\ \mathbf{G}_{io-c} & -\mathbf{Y}_{o-c} & \mathbf{G}_{ro} \end{bmatrix}}^{\mathbf{G}_H} \begin{bmatrix} \mathbf{i}_{in} \\ \mathbf{v}_o \\ \mathbf{v}^* \end{bmatrix} \quad (15.42)$$

$$\begin{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ 0 \end{bmatrix} \\ \begin{bmatrix} \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} Z_{in-c} & 0 \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} T_{oid-c} & T_{oiq-c} \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} G_{cid-c} & G_{ciq-c} \\ 0 & 0 \end{bmatrix} \\ \begin{bmatrix} G_{iod-c} & 0 \\ G_{ioq-c} & 0 \end{bmatrix} & -\begin{bmatrix} Y_{odd-c} & Y_{oqd-c} \\ Y_{odq-c} & Y_{oqq-c} \end{bmatrix} & \begin{bmatrix} G_{codd-c} & G_{coqd-c} \\ G_{codq-c} & G_{coqq-c} \end{bmatrix} \end{bmatrix} \begin{bmatrix} \hat{i}_{in} \\ 0 \\ \hat{v}_{od} \\ \hat{v}_{oq} \\ \hat{v}_{in}^* \\ \hat{i}_{oq}^* \end{bmatrix} \quad (15.43)$$

The input impedance Z_{in-c} can be used to analyze impedance-based interactions on the DC side. Output-to-input transfer functions T_{oid-c} and T_{oiq-c} can be used to analyze how the input voltage is affected by variations in the grid voltage d and q-components. Control-to-input-voltage transfer function G_{cid-c} can be used to define the bandwidth of input voltage control and G_{ciq-c} can be used to analyze how changes in the reference of reactive current component affect the input voltage. Input-to-output transfer functions G_{iod-c} and G_{ioq-c} can be used to analyze how variations in input current affect the output current d and q-components, that is, how much rapid changes or oscillations in input current affect power quality. The output admittance terms Y_{odd-c} , Y_{oqd-c} , Y_{odq-c} , and Y_{oqq-c} can be used to analyze impedance-based interactions on the AC side. Control-to-output-current transfer functions G_{codd-c} , G_{coqd-c} , G_{codq-c} , and G_{coqq-c} can be used to analyze how well different decoupling schemes succeed and to evaluate control bandwidth of the output current control.

15.2.1 Verification of Dynamic Model

The closed-loop model was verified by extracting the transfer functions from a simulation model. The parameters of the switching model are collected in Table 15.1. As an example, Figure 15.11 shows the cross-coupling transfer function G_{coqd-c} from the reference of output current q-component \hat{i}_{oq}^* to output

Table 15.1 Parameters of the simulation model.

V_{in}	700 V	$V_{a,b,c-rms}$	230 V	L	2.46 mH
I_{in}	14.65 A	ω_s	$2\pi \cdot 50$ rad/s	r_L	25.8 m Ω
P_{in}	10.25 kW	C	2.6 mF	r_{sw}	20 m Ω
f_s	10 kHz	I_{Lq}	5 A	I_{Ld}	20.95 A

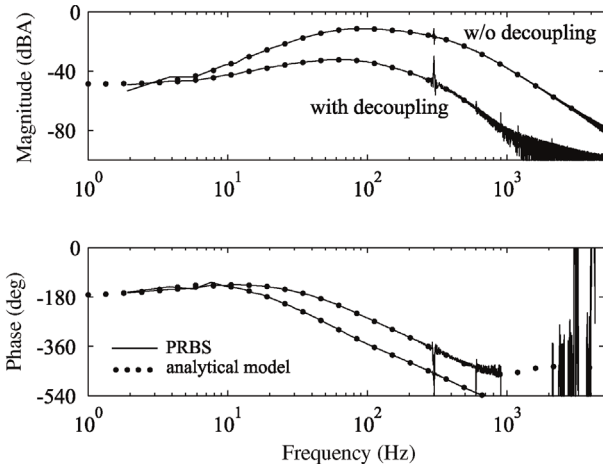


Figure 15.11 Transfer function from reference of current q-component to output current d-component G_{c0qd-c} with and without decoupling gains.

current d-component \hat{i}_{od} with and without the decoupling terms. The cross-coupling between q and d-channels is much smaller when decoupling terms are used since the magnitude of the transfer function is much smaller. Such transfer functions cannot be obtained by using the reduced-order model.

Figure 15.12 shows time-domain behavior of inverter output currents when a step change is applied to output current q-component from 5 to 0 A at time 0.1 s. The decoupling effectively reduces the amount of oscillation observed in the current d-component. Therefore, the full-order dynamic model can also be utilized to evaluate the effect of decoupling gains on control performance.

The real power fed to the grid experiences some oscillation when the reference of current q-component is changed from 5 to 0 A when decoupling is not used. However, the real power remains constant during the step test when decoupling

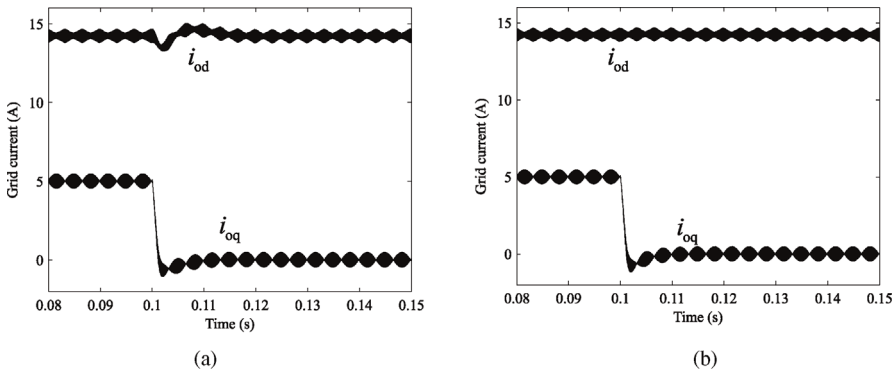


Figure 15.12 Inverter output current d- and q-components (a) without and (b) with decoupling gains.

network is activated. The difference in time-domain behavior can be explained by studying the transfer functions in Figure 15.11. The decoupling gains reduce the cross-coupling from reference of current q-component to output current d-component by approximately 20 dB over a wide frequency range.

The full-order model also allows evaluating the cross-diagonal terms of the admittance matrix \mathbf{Y}_{o-c} , that is, the cross-coupling admittances Y_{oqd-c} and Y_{odq-c} . A reduced-order model is often considered to yield adequate accuracy in, for example, impedance-based stability analysis. However, the accuracy can be improved by considering the full-impedance matrix in the stability analysis [2]. All the components of the admittance matrix were extracted from a switching model by using the PRBS method. The decoupling terms were included in the simulation model as, $G_{dec-qd} = -\omega_s L/V_{in}$, $G_{dec-dq} = \omega_s L/V_{in}$. Crossover frequencies of current control loops, PLL, and DC voltage control were selected as 500, 20, and 30 Hz respectively. All control loops were tuned to have phase margin of 65° .

The admittance d and q-components Y_{odd-c} and Y_{oqq-c} are shown in Figure 15.13. The d and q-components are not affected by the decoupling gains. Therefore, their magnitudes are not dependent on the value of decoupling gains. The positive resistance behavior due to DC voltage control makes the phase of admittance d-component to remain close to zero at low frequencies. The admittance q-component, however, behaves as a negative resistor due to PLL that can be seen in the low frequencies where the phase is close to 180° .

Figure 15.14 shows the admittance d- and q-components with and without the decoupling terms: ($G_{dec-qd} = -\omega_s L/V_{in}$, $G_{dec-dq} = \omega_s L/V_{in}$). The decoupling does not affect the low-frequency magnitude of cross-admittance term Y_{oqd-c} , as can be deduced by studying Figure 15.14a. However, the high-frequency gain is reduced that suggests that decoupling effectively mitigates high-frequency coupling between q and d-channels. The cross-admittance term Y_{odq-c} is shown in Figure 15.14b. The decoupling reduces the admittance magnitude over the whole frequency spectrum. The developed closed-loop admittance model gives very precise results, as can be seen in Figures 15.13 and 15.14.

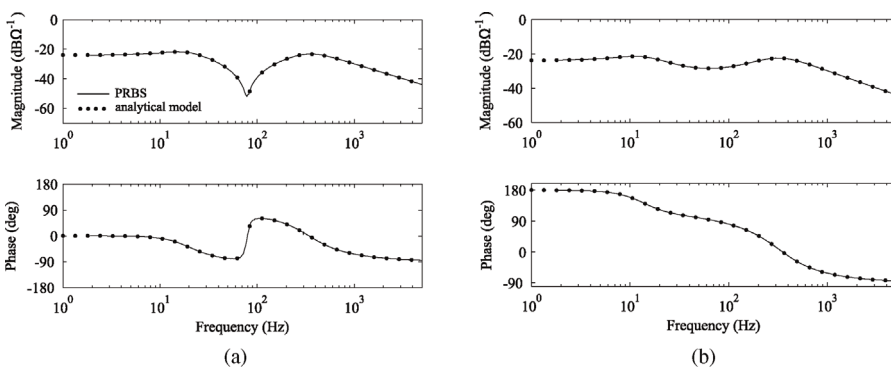


Figure 15.13 Inverter output admittance (a) d- and (b) q-components.

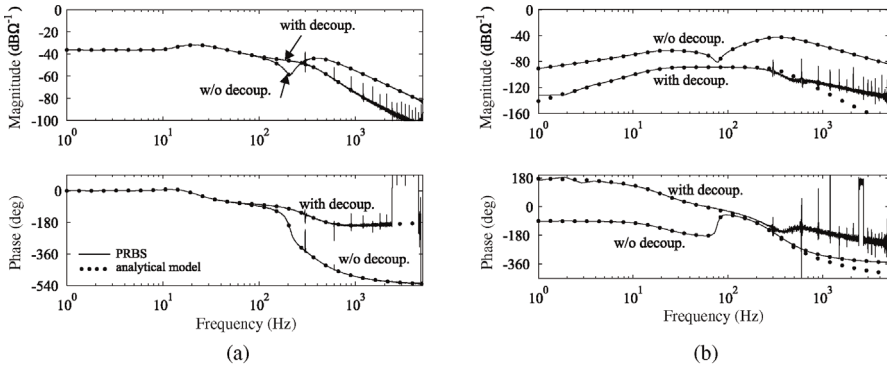


Figure 15.14 Cross-coupling admittance terms (a) Y_{0qd-c} and (b) Y_{0dq-c} .

15.3 Experimental Verification of Admittance Model

The admittance model was verified from an experimental grid-connected photovoltaic inverter. A two-level inverter bridge was used to interface a PV simulator to a three-phase voltage source according to Figure 15.15. Resistive three-phase load was connected between the voltage source and the inverter to dissipate the power generated by the PV simulator because the three-phase voltage source could not sink power. Such measurement setup can be used when grid emulator with power-sinking capabilities is not available. The control system was implemented using a dSPACE real-time simulator. The admittance measurement is accurate down to -50 dB, after which measurement noise makes extracting the admittance impossible. The decoupling gains G_{dec-qd} and G_{dec-dq} were set equal to zero, which increases the cross-coupling admittance magnitudes, but also makes it possible to measure them and, thus, verify the admittance model. Moreover, the admittance can be extracted up to half the switching frequency (4 kHz) since the admittance measurement algorithm runs on the same real-time simulator.

Current control loops were tuned to have crossover frequencies of 500 Hz. DC voltage control loop and the PLL were tuned to have crossover frequencies of 10 Hz. The inverter was operated at unity power factor, that is, the reference of output current q-component was set to zero. The parameters of the experimental setup are given in Table 15.2. The DC voltage reference was set equal to the MPP voltage of the PV emulator. Thus, the dynamic effect of MPPT algorithm is not considered.

Figure 15.16 shows the measured admittance d and q-components Y_{0dd-c} and Y_{0qq-c} . The phase of the admittance d-component is close to zero degrees below

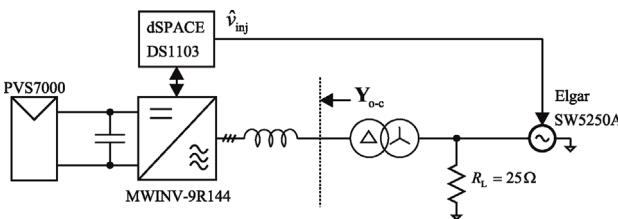
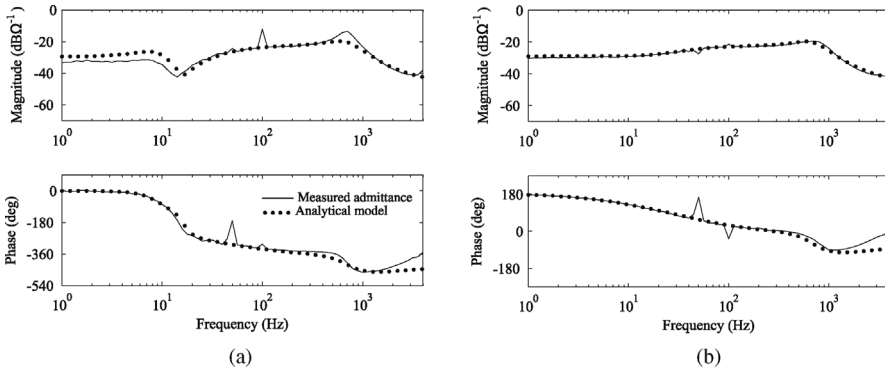


Figure 15.15 Experimental setup to measure inverter output admittance.

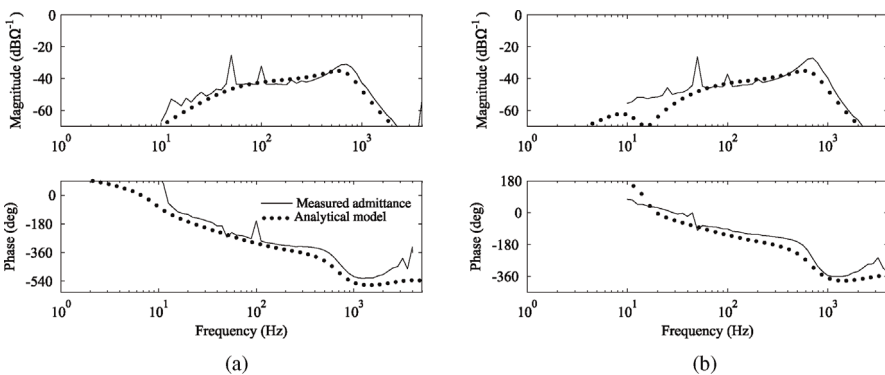
Table 15.2 Parameters of the experimental setup.

V_{in}	729 V	$V_{a,b,c-rms}$	230 V	L	5.2 mH
I_{in}	7.3 A	ω_s	$2\pi \cdot 50$ rad/s	r_L	100 m Ω
P_{in}	5.3 kW	C	1.5 mF	r_{sw}	10 m Ω
f_s	8 kHz	I_{Lq}	0 A	I_{Ld}	10.9 A


Figure 15.16 Measured admittance (a) d- and (b) q-components.

10 Hz and a value of approximately I_{od}/V_{od} . Thus, the impedance d-component behaves as a positive resistor. Moreover, the phase of admittance q-component is close to 180° at low frequencies having a value of $-I_{od}/V_{od}$. Thus, the impedance q-component resembles a negative resistor. The grid voltage was higher than 230 V due to the isolation transformer that explains why the low-frequency magnitude of the measured admittances differ slightly from the frequency responses solved from the dynamic model.

Figure 15.17 shows the measured cross-coupling admittances Y_{oqd-c} and Y_{odq-c} . The admittance cannot be extracted by the experimental setup when the magnitude of the admittance component drops below approximately 50 dB


Figure 15.17 Measured cross-coupling admittances (a) Y_{oqd-c} and (b) Y_{odq-c} .

due to measurement noise. Therefore, the cross-coupling admittances could be measured only at frequencies over few tens of Hertz. The sine-sweep method was used to extract the admittances. The cross-coupling admittances have magnitudes of over -30 dB near 1 kHz, which suggest that they may have some effect on impedance-based stability margins [2].

15.4 Full-Order Model of Current-Fed Inverter with LCL-Type Filter

Current-fed three-phase inverter with passively damped LCL filter is depicted in Figure 15.18. The inverter utilizes cascaded control scheme, SRF-PLL, and proportional grid voltage feedforward. The feedforward signals d_{ffd} and d_{ffq} are obtained from the measured grid voltage d and q-components v_{od}^c and v_{oq}^c according to Eqs. (15.44) and (15.45). The feedforward gains G_{ffd} , G_{ffq} are omitted from the figure for readability:

$$d_{ffd} = G_{ffd}v_{od}^c, \tag{15.44}$$

$$d_{ffq} = G_{ffq}v_{oq}^c. \tag{15.45}$$

The control laws for inverter-side inductor current control can be given as in Eqs. (15.46) and (15.47), where the superscript c denotes that the corresponding variable is affected by the PLL, that is, the variables are defined in the control system reference frame.

$$\hat{d}_d^c = G_{PI-d}(\hat{i}_{L1d}^* - \hat{i}_{L1d}^c) + G_{ffd}v_{od}^c, \tag{15.46}$$

$$\hat{d}_q^c = G_{PI-q}(\hat{i}_{L1q}^* - \hat{i}_{L1q}^c) + G_{ffq}v_{oq}^c. \tag{15.47}$$

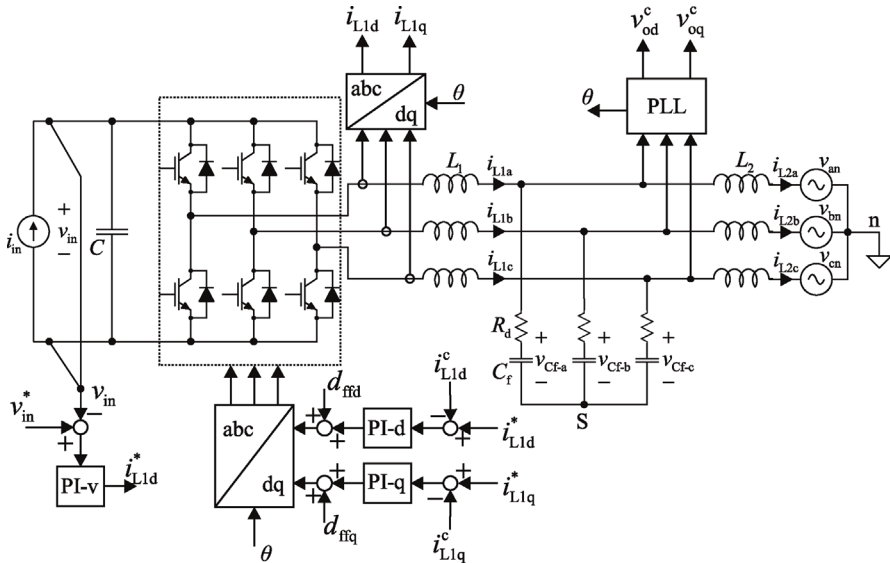


Figure 15.18 Three-phase inverter with LCL-type output filter.

Decoupling gains and current sensing gains are left out of the analysis to simplify the results, but they can be included in the model by modifying the control laws above. The duty ratio can be given in the control system reference frame as

$$\begin{bmatrix} \hat{d}_d^c \\ \hat{d}_q^c \end{bmatrix} = \begin{bmatrix} G_{PI-d} & 0 \\ 0 & G_{PI-q} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1d}^* \\ \hat{i}_{L1q}^* \end{bmatrix} - \begin{bmatrix} G_{PI-d} & 0 \\ 0 & G_{PI-q} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1d}^c \\ \hat{i}_{L1q}^c \end{bmatrix} + \begin{bmatrix} G_{ffd} & 0 \\ 0 & G_{ffq} \end{bmatrix} \begin{bmatrix} \hat{v}_{od}^c \\ \hat{v}_{oq}^c \end{bmatrix}, \quad (15.48)$$

and by using vectors as

$$\mathbf{d}^c = \mathbf{G}_{c-out} \mathbf{i}_{L1}^* - \mathbf{G}_{c-out} \mathbf{i}_{L1}^c + \mathbf{G}_{ff} \mathbf{v}_o^c. \quad (15.49)$$

The duty ratio can be given in the grid reference frame as in Eq. (15.50) by including the dynamic effect of PLL.

$$\begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} = \begin{bmatrix} \hat{d}_d^c \\ \hat{d}_q^c \end{bmatrix} + \begin{bmatrix} 0 & -D_q \\ 0 & D_d \end{bmatrix} \cdot \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (15.50)$$

Duty ratio in the grid reference frame can be given as

$$\mathbf{d} = \mathbf{d}^c + \mathbf{D} \cdot \mathbf{G}_{PLL} \cdot \mathbf{v}_o. \quad (15.51)$$

The inverter-side inductor current \mathbf{i}_{L1}^c can be given in control system reference frame as in Eqs. (15.52) and (15.53) when the effect of PLL is taken into account.

$$\begin{bmatrix} \hat{i}_{L1d}^c \\ \hat{i}_{L1q}^c \end{bmatrix} = \begin{bmatrix} \hat{i}_{L1d} \\ \hat{i}_{L1q} \end{bmatrix} + \begin{bmatrix} 0 & I_{L1q} \\ 0 & -I_{L1d} \end{bmatrix} \cdot \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (15.52)$$

The inductor current can be defined using vectors as

$$\mathbf{i}_{L1}^c = \mathbf{i}_{L1} + \mathbf{I}_{L1} \cdot \mathbf{G}_{PLL} \cdot \mathbf{v}_o. \quad (15.53)$$

Finally, the grid voltage \mathbf{v}_o^c can be defined in the control system reference frame as in Eqs. (15.54) and (15.55)

$$\begin{bmatrix} \hat{v}_{od}^c \\ \hat{v}_{oq}^c \end{bmatrix} = \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & -V_{od} \end{bmatrix} \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{V_{od}} \cdot \frac{L_{PLL}}{(1 + L_{PLL})} \end{bmatrix} \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (15.54)$$

$$\mathbf{v}_o^c = \mathbf{v}_o + \mathbf{V}_o \cdot \mathbf{G}_{PLL} \mathbf{v}_o. \quad (15.55)$$

The duty ratio can be given in the control system reference frame according to Eq. (15.49) as

$$\mathbf{d}^c = \mathbf{G}_{c-out} \mathbf{i}_{L1}^* - \mathbf{G}_{c-out} (\mathbf{i}_{L1} + \mathbf{I}_{L1} \cdot \mathbf{G}_{PLL} \cdot \mathbf{v}_o) + \mathbf{G}_{ff} (\mathbf{v}_o + \mathbf{V}_o \cdot \mathbf{G}_{PLL} \mathbf{v}_o), \quad (15.56)$$

and in the grid reference frame as in Eq. (15.57) by applying the relation in Eq. (15.51).

$$\mathbf{d} = \mathbf{G}_{c-out} \mathbf{i}_{L1}^* - \mathbf{G}_{c-out} (\mathbf{i}_{L1} + \mathbf{I}_{L1} \cdot \mathbf{G}_{PLL} \cdot \mathbf{v}_o) + \mathbf{G}_{ff} (\mathbf{I} + \mathbf{V}_o \cdot \mathbf{G}_{PLL}) \mathbf{v}_o + \mathbf{D} \cdot \mathbf{G}_{PLL} \cdot \mathbf{v}_o. \tag{15.57}$$

It is possible to build the control block diagram directly based on Eq. (15.57). However, the representation can be somewhat simplified to reduce the amount of signal loops in the block diagram. Finally, the duty ratio can be defined using transfer matrices according to Eq. (15.58):

$$\begin{aligned} \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} &= \begin{bmatrix} G_{PI-d} & 0 \\ 0 & G_{PI-q} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1d}^* \\ \hat{i}_{L1q}^* \end{bmatrix} - \begin{bmatrix} G_{PI-d} & 0 \\ 0 & G_{PI-q} \end{bmatrix} \left(\begin{bmatrix} \hat{i}_{L1d} \\ \hat{i}_{L1q} \end{bmatrix} + \begin{bmatrix} 0 & \frac{I_{L1q} L_{PLL}}{V_{od} (1 + L_{PLL})} \\ 0 & \frac{-I_{L1d} L_{PLL}}{V_{od} (1 + L_{PLL})} \end{bmatrix} \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \right) \\ &+ \begin{bmatrix} G_{ffd} & 0 \\ 0 & G_{ffq} \left(1 - \frac{L_{PLL}}{(1 + L_{PLL})} \right) \end{bmatrix} \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} + \begin{bmatrix} 0 & \frac{-D_q L_{PLL}}{V_{od} (1 + L_{PLL})} \\ 0 & \frac{D_d L_{PLL}}{V_{od} (1 + L_{PLL})} \end{bmatrix} \begin{bmatrix} \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \end{aligned} \tag{15.58}$$

Duty ratio can now be defined as in Eq. (15.59), which is a far more friendlier form to draw the control block diagram from. The control block diagram that represents the dynamics related to inductor current control can be depicted as in Figure 15.19. Transfer matrices \mathbf{G}_{iL-o} , \mathbf{T}_{oL-o} , and \mathbf{G}_{cL-o} are defined as in Eqs. (15.60)–(15.62). The open-loop transfer functions can be obtained by using MATLAB or similar software by applying the principles presented

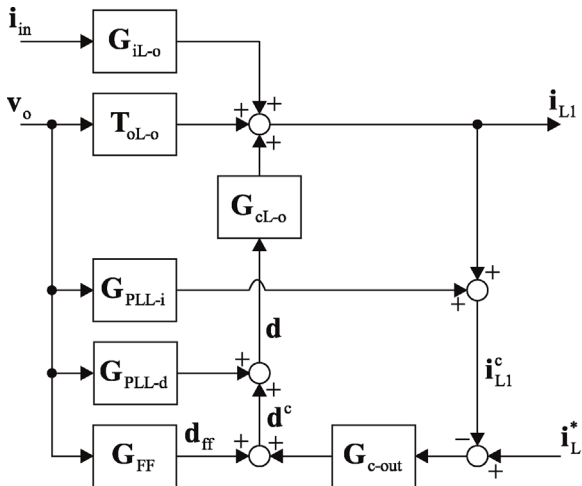


Figure 15.19 Control block diagram of the inverter-side inductor current control.

in Chapter 12.

$$\mathbf{d} = \mathbf{G}_{c\text{-out}}\mathbf{i}_{L1}^* - \mathbf{G}_{c\text{-out}}(\mathbf{i}_{L1} + \mathbf{G}_{\text{PLL-}i}\mathbf{v}_o) + \mathbf{G}_{\text{FF}}\mathbf{v}_o + \mathbf{G}_{\text{PLL-d}}\mathbf{v}_o. \quad (15.59)$$

Open-loop transfer matrices related to inverter-side inductor current are as follows:

$$\mathbf{G}_{iL\text{-}o} = \begin{bmatrix} G_{iLd\text{-}o} & 0 \\ G_{iLq\text{-}o} & 0 \end{bmatrix}, \quad (15.60)$$

$$\mathbf{T}_{oL\text{-}o} = \begin{bmatrix} T_{oLdd\text{-}o} & T_{oLqd\text{-}o} \\ T_{oLdq\text{-}o} & T_{oLqq\text{-}o} \end{bmatrix}, \quad (15.61)$$

$$\mathbf{G}_{cL\text{-}o} = \begin{bmatrix} G_{cLdd\text{-}o} & G_{cLqd\text{-}o} \\ G_{cLdq\text{-}o} & G_{cLqq\text{-}o} \end{bmatrix}. \quad (15.62)$$

The key to solving closed-loop inverter transfer functions is to solve first the duty ratio \mathbf{d} from Figure 15.19 when all the control loops are closed, that is, current control loop, PLL, and grid voltage feedforward. The duty ratio can be given as

$$\mathbf{d} = -(\mathbf{I} + \mathbf{L}_{cc})^{-1}\mathbf{G}_{c\text{-out}}\mathbf{G}_{iL\text{-}o}\mathbf{i}_{in} + (\mathbf{I} + \mathbf{L}_{cc})^{-1}\mathbf{G}_{c\text{-out}}\mathbf{i}_{L1}^* + (\mathbf{I} + \mathbf{L}_{cc})^{-1}(\mathbf{G}_{\text{PLL-d}} + \mathbf{G}_{\text{FF}} - \mathbf{G}_{c\text{-out}}(\mathbf{T}_{oL\text{-}o} - \mathbf{G}_{\text{PLL-}i}))\mathbf{v}_o, \quad (15.63)$$

where the current control loop gain \mathbf{L}_{cc} can be defined as

$$\mathbf{L}_{cc} = \mathbf{G}_{c\text{-out}}\mathbf{G}_{cL\text{-}o}. \quad (15.64)$$

As explained in Chapter 12, the input and output dynamics can be given according to Eqs. (15.65) and (15.66) and illustrated using the control block diagrams in Figure 15.20.

$$\mathbf{v}_{in} = \mathbf{Z}_{in\text{-}o}\mathbf{i}_{in} + \mathbf{T}_{oi\text{-}o}\mathbf{v}_o + \mathbf{G}_{ci\text{-}o}\mathbf{d}, \quad (15.65)$$

$$\mathbf{i}_o = \mathbf{G}_{io\text{-}o}\mathbf{i}_{in} - \mathbf{Y}_{o\text{-}o}\mathbf{v}_o + \mathbf{G}_{co\text{-}o}\mathbf{d}. \quad (15.66)$$

The duty ratio, as defined earlier in Eq. (15.63), includes the effect of all the control functions except the DC voltages control. Closed-loop dynamics with current control loops closed can be obtained by substituting duty ratio \mathbf{d} in Eqs. (15.65)

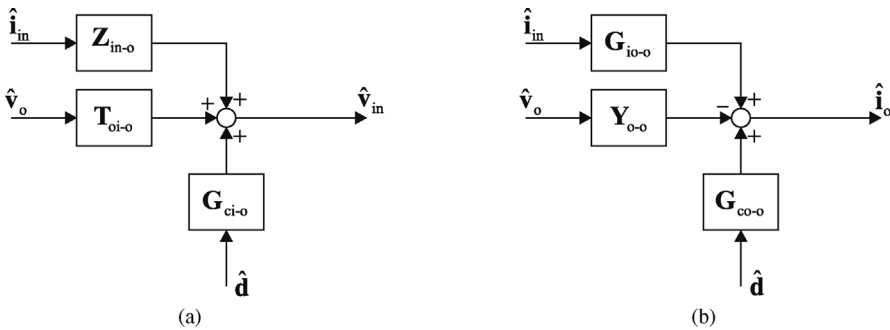


Figure 15.20 Input and output dynamics of current-fed inverter as control block diagrams.

and (15.66) and by solving the input voltage \mathbf{v}_{in} and output current \mathbf{i}_o in terms of input variables \mathbf{i}_{in} , \mathbf{v}_o , and \mathbf{i}_{L1}^* .

The input dynamics can be given as in Eqs. (15.67)–(15.69) when current control loops are closed.

$$\mathbf{Z}_{in}^{cc} = \mathbf{Z}_{in-o} - \mathbf{G}_{ci-o}(\mathbf{I} + \mathbf{L}_{cc})^{-1}\mathbf{G}_{c-out}\mathbf{G}_{iL-o}, \quad (15.67)$$

$$\mathbf{T}_{oi}^{cc} = \mathbf{T}_{oi-o} + \mathbf{G}_{ci-o}(\mathbf{I} + \mathbf{L}_{cc})^{-1}(\mathbf{G}_{PLL-d} + \mathbf{G}_{FF} - \mathbf{G}_{c-out}(\mathbf{T}_{oL-o} + \mathbf{G}_{PLL-i})), \quad (15.68)$$

$$\mathbf{G}_{ci}^{cc} = \mathbf{G}_{ci-o}(\mathbf{I} + \mathbf{L}_{cc})^{-1}\mathbf{G}_{c-out}. \quad (15.69)$$

The output dynamics can be given as in Eqs. (15.70)–(15.72) when current control loops are closed.

$$\mathbf{G}_{io}^{cc} = \mathbf{G}_{io-o} - \mathbf{G}_{co-o}(\mathbf{I} + \mathbf{L}_{cc})^{-1}\mathbf{G}_{c-out}\mathbf{G}_{iL-o}, \quad (15.70)$$

$$\mathbf{Y}_o^{cc} = \mathbf{Y}_{o-o} - \mathbf{G}_{co-o}(\mathbf{I} + \mathbf{L}_{cc})^{-1}(\mathbf{G}_{PLL-d} + \mathbf{G}_{FF} - \mathbf{G}_{c-out}(\mathbf{T}_{oL-o} - \mathbf{G}_{PLL-i})), \quad (15.71)$$

$$\mathbf{G}_{co}^{cc} = \mathbf{G}_{co-o}(\mathbf{I} + \mathbf{L}_{cc})^{-1}\mathbf{G}_{c-out}. \quad (15.72)$$

Next, the input voltage control loop is included in the control block diagram as shown in Figure 15.21. The input voltage controller transfer matrix is defined as in Eq. (15.73) and input voltage sensing gain as in Eq. (15.74), similarly as in the case of the full-order model of inverter employing L-type output filter in Chapter 14.

$$\mathbf{G}_{c-in} = \begin{bmatrix} \mathbf{G}_{PI-v} & \mathbf{0} \\ \mathbf{0} & \mathbf{1} \end{bmatrix}, \quad (15.73)$$

$$\mathbf{H}_{in} = \begin{bmatrix} \mathbf{H}_v & \mathbf{0} \\ \mathbf{0} & \mathbf{0} \end{bmatrix}. \quad (15.74)$$

Closed-loop input dynamics can be solved from Figure 15.21a and given as

$$\mathbf{Z}_{in-c} = (\mathbf{I} + \mathbf{L}_{in})^{-1}\mathbf{Z}_{in}^{cc}, \quad (15.75)$$

$$\mathbf{T}_{oi-c} = (\mathbf{I} + \mathbf{L}_{in})^{-1}\mathbf{T}_{oi}^{cc}, \quad (15.76)$$

$$\mathbf{G}_{ci-c} = (\mathbf{I} + \mathbf{L}_{in})^{-1}\mathbf{G}_{ci}^{cc}\mathbf{G}_{c-in}, \quad (15.77)$$

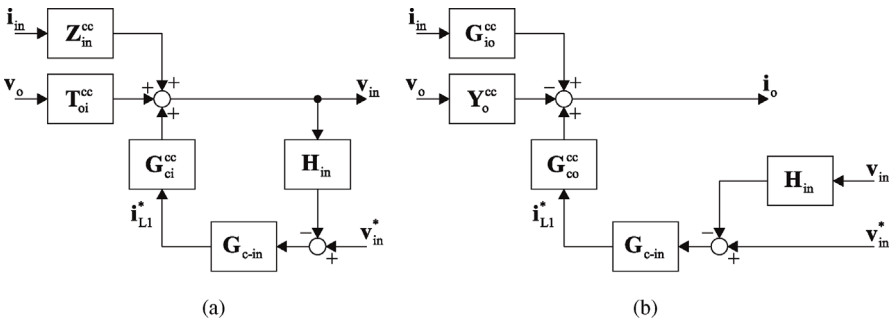


Figure 15.21 Control block diagrams when input voltage control loop is closed.

where the input voltage control loop gain is defined as

$$\mathbf{L}_{in} = \mathbf{G}_{ci}^{cc} \mathbf{G}_{c-in} \mathbf{H}_{in}. \quad (15.78)$$

Closed-loop transfer matrices from Figure 15.21b can be solved by noting that the input voltage can be represented using input variables as in Eq. (15.79) and substituted in the output dynamics given by Eq. (15.80).

$$\mathbf{v}_{in} = \mathbf{Z}_{in-c} \mathbf{i}_{in} + \mathbf{T}_{oi-c} \mathbf{v}_o + \mathbf{G}_{ci-c} \mathbf{v}_{in}^*, \quad (15.79)$$

$$\mathbf{i}_o = \mathbf{G}_{io}^{cc} \mathbf{i}_{in} - \mathbf{Y}_o^{cc} \mathbf{v}_o + \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} (\mathbf{v}_{in}^* - \mathbf{H}_{in} \mathbf{v}_{in}). \quad (15.80)$$

Closed-loop output dynamics can be given as

$$\mathbf{G}_{io-c} = \mathbf{G}_{io}^{cc} - \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} \mathbf{H}_{in} \mathbf{Z}_{in-c}, \quad (15.81)$$

$$\mathbf{Y}_{o-c} = \mathbf{Y}_o^{cc} + \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} \mathbf{H}_{in} \mathbf{T}_{oi-c}, \quad (15.82)$$

$$\mathbf{G}_{co-c} = \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} - \mathbf{G}_{co}^{cc} \mathbf{G}_{c-in} \mathbf{H}_{in} \mathbf{G}_{ci-c}. \quad (15.83)$$

15.4.1 Verification of Closed-Loop Model

Input impedance and all four components of the output admittance matrix were extracted from a simulation model to validate the closed-loop model. The Simulink model is as shown in Figure 15.22. Proportional grid voltage feedforward is applied and the feedforward gain is selected as the inverse of DC voltage steady-state value. Grid voltage d and q-components are estimated by using the Park's transformation block inside the PLL.

Simulation parameters are as shown in Table 15.3, which are the same as in the experimental setup discussed in the next section. Steady-state solved operating point can be solved from the average model presented in Chapter 12. An example m-file for solving the operating point is provided in Appendix 12.A and the numerical values are given in Table 15.4. The grid current q-component I_{L2q} is zero and the inverter provides the reactive current I_{L1q} required by the LCL filter. Therefore, from the grid's perspective, the inverter operates at unity power factor.

Current control loop gains were tuned to have crossover frequencies of 500 Hz; DC voltage control loop gain and PLL were both tuned to have crossover frequency of 20 Hz. All control loops were designed to have 65° phase margin.

Figure 15.23 shows the input impedance that is obtained by using the PRBS method. The perturbation is made in the input current, that is, in the input signal of the controlled current source. The figure also shows the input impedance given by the closed-loop model in Eq. (15.75). The input impedance can be obtained from the first row and first column of \mathbf{Z}_{in-c} , whereas all the other elements have zero value. The frequency response given by the closed-loop model follows exactly the shape of the extracted input impedance. Thus, the model can be used

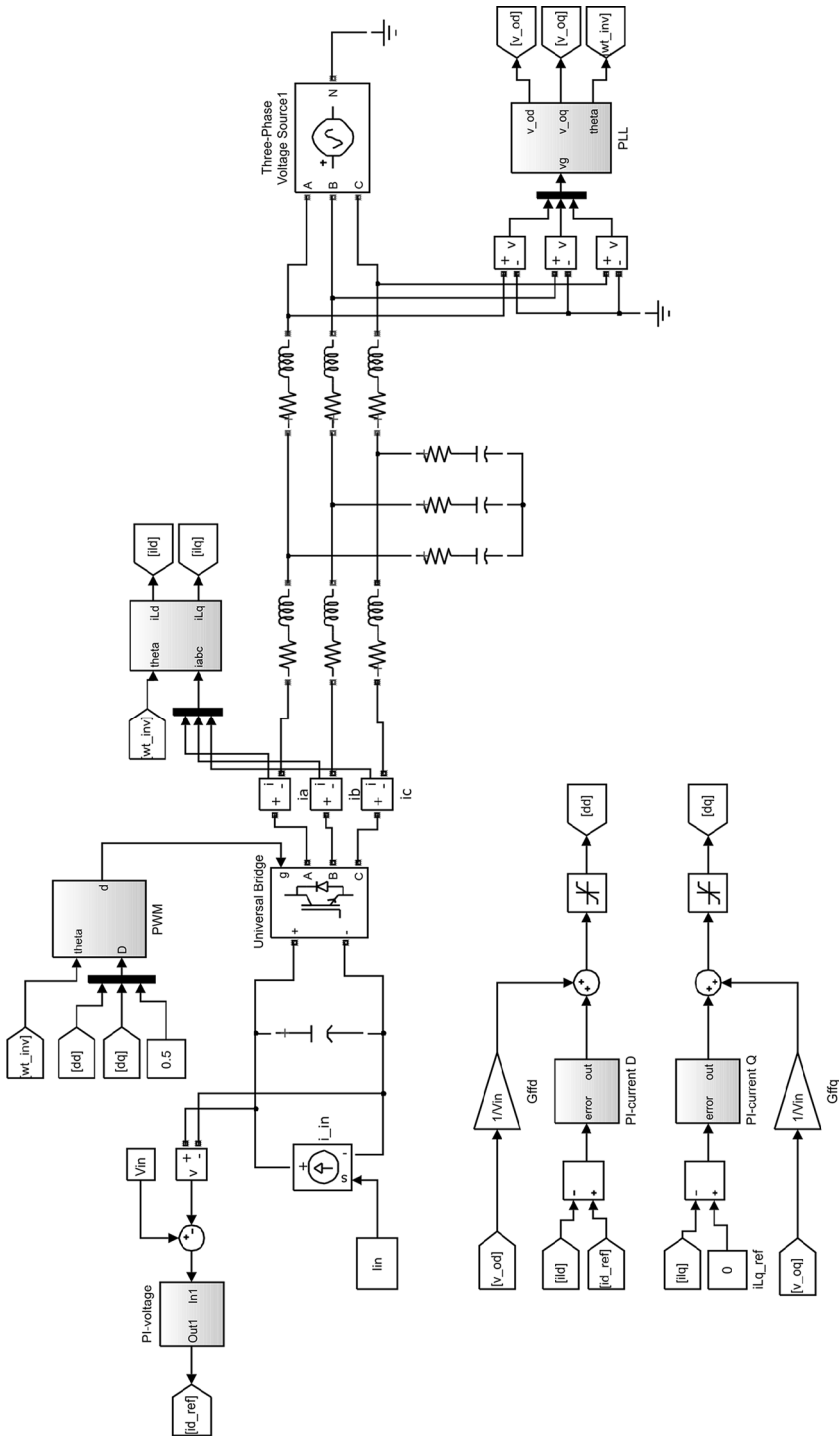


Figure 15.22 Simulation model.

Table 15.3 Inverter parameters.

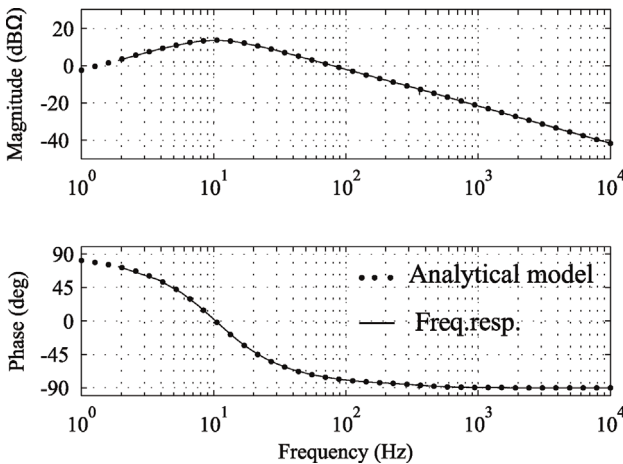
C	1.95 mF	C_f	25 μ F	R_d	1 Ω
L_1	2.2 mF	r_{L1}	100 m Ω	f_{sw}	30 kHz
L_2	0.3 mF	r_{L2}	65 m Ω	ω_s	$2\pi \cdot 60$ rad/s

Table 15.4 Steady-state operating point.

V_{in}	414.3 V	I_{L1d}	10.583 A	V_{Cfd}	170.4 V
I_{in}	6.577 A	I_{L1q}	1.606 A	V_{Cfq}	-0.4 V
V_{od}	169.7 V	I_{L2d}	10.579 A	D_d	0.4106
V_{oq}	0 V	I_{L2q}	0 A	D_q	0.0245

in characterizing impedance-based instability on the DC side of the inverter; for example, when the inverter utilizes a DC–DC converter or when the inverter is used as an interface between the grid and a microgrid.

Figure 15.24 shows the components of the output admittance matrix Y_{o-c} when grid voltage feedforward is deactivated, that is, when gains G_{ffd} and G_{ffq} are zero. The admittance model defined in Eq. (15.82) can predict the shape of all admittance components accurately. The positive low-frequency resistance in Y_{odd-c} and negative resistance in Y_{oqq-c} are both correctly captured by the closed-loop model. Moreover, the cross-coupling admittances are accurately predicted and include the resonance caused by the LCL filter. Figure 15.25 shows the output admittance components when proportional feedforward is used. Also in this case, all the admittance components are accurately predicted by the closed-loop model.


Figure 15.23 Input impedance.

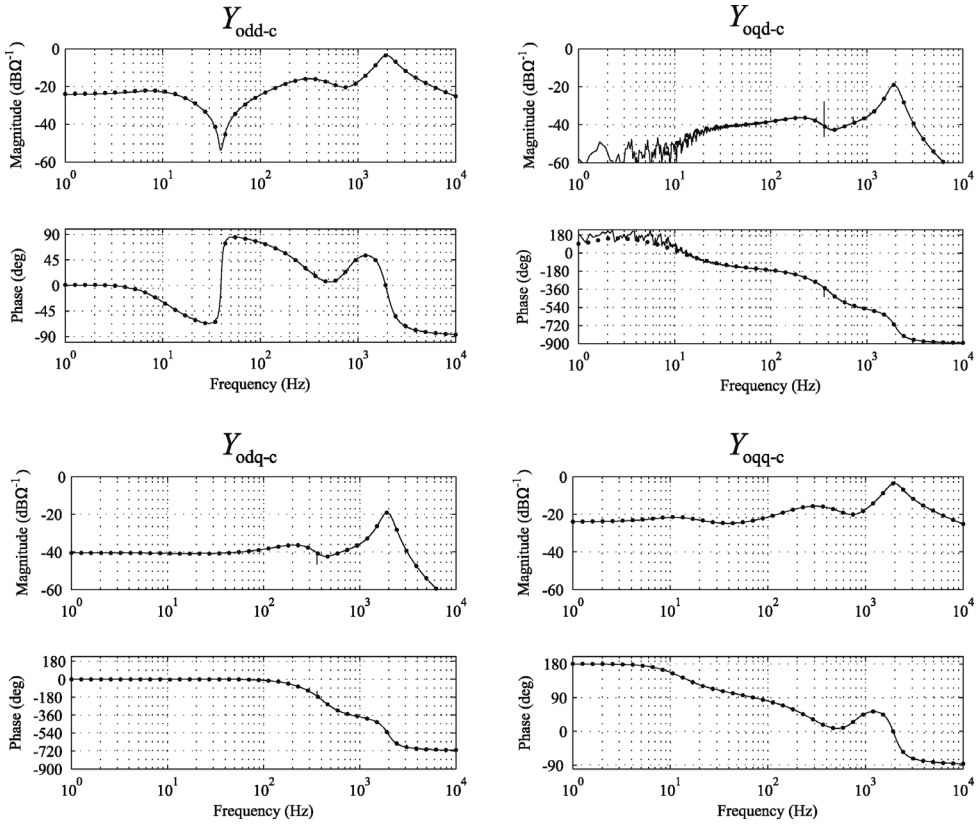


Figure 15.24 Inverter output admittance with grid voltage feedforward deactivated.

15.4.2 Measured Output Impedance of PV Inverter

Three-phase photovoltaic inverter with passively damped LCL filter was studied in the laboratory. The laboratory setup is as illustrated in Figure 15.26. The inverter employed SiC-MOSFET switches in its power stage, which enabled using higher switching frequency. The controllers were implemented using the dSPACE real-time simulator and the switching frequency was set to 30 kHz. Photograph of the setup is shown in Figure 14.42 where the LC-type filter was replaced with an LCL filter. The DC voltage control loop was redesigned to have a lower crossover frequency of 4 Hz to reduce the effect of low-frequency ripple in DC voltage and to improve output current quality as explained in Chapter 13.

Figure 15.27 shows the waveforms recorded from the primary-side of the transformer, that is, on the inverter side. The inverter was operated with the proportional grid voltage feedforward activated. The output current is sinusoidal and has low amount of harmonics when the grid voltage is clean.

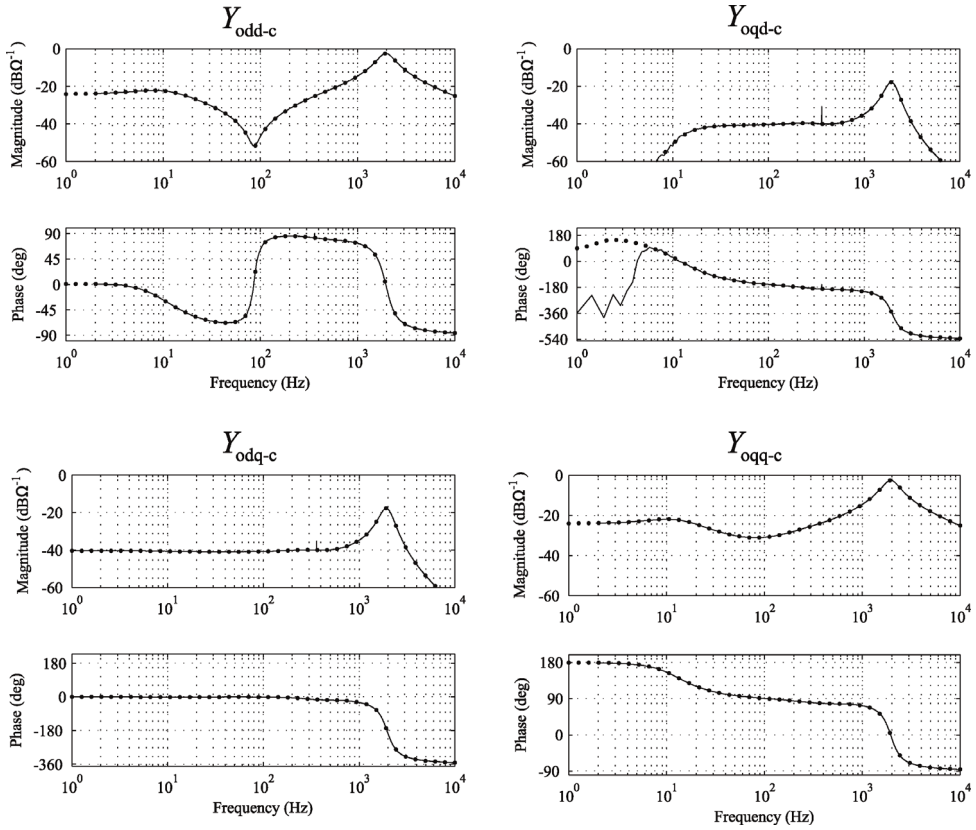


Figure 15.25 Inverter output admittance with proportional feedforward.

Output impedance d and q-components of the inverter were measured using a frequency-response analyzer based on the sine-sweep method. Figure 15.28 shows the measured impedances as solid lines, while the dotted lines represent the impedance solved using the closed-loop model (obtained as the inverse of admittances $Y_{\text{odd-c}}$ and $Y_{\text{oqd-c}}$).

The proportional grid voltage feedforward has a significant effect on the shape of both impedance d and q-components. The magnitude increases from few tens of Hertz up to frequencies close to the resonant frequency of the LCL filter that is approximately at 2 kHz. At higher frequencies, the grid-side inductance starts to increase the impedance magnitude. However, proportional feedforward cannot boost the impedance magnitude at frequencies over the resonant frequency.

Larger output impedance magnitude naturally means that the inverter generates less harmonics in a distorted grid. Figure 15.29 shows the inverter waveforms when grid voltage is corrupted with fifth and seventh harmonics. The inverter produces much more harmonic currents when proportional feedforward is

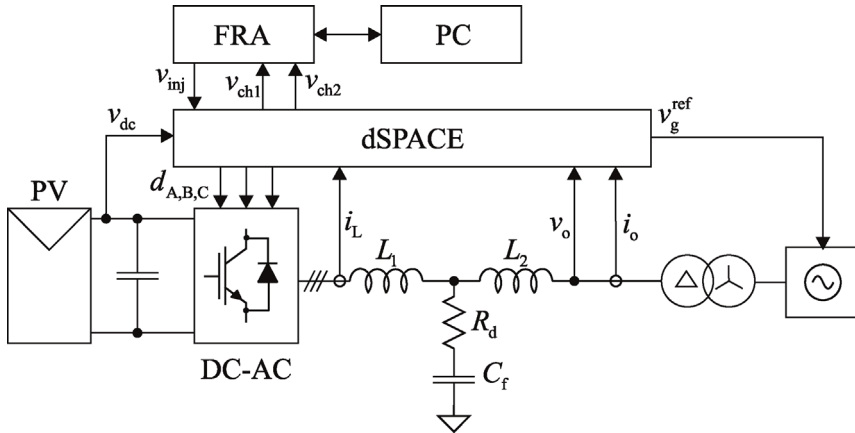


Figure 15.26 Illustration of the experimental laboratory setup.

deactivated due to the fact that both impedance d and q-components have smaller magnitude.

The feedforward transfer function should ideally be a third-order transfer function to affect inverter impedance near the LCL filter resonance [11,12]. This is due to the fact that the dynamics of the inverter with LCL filter are of higher order than the inverter with L-type filter. However, the high-order grid voltage feedforward should be designed carefully since it may easily pick up noise that corrupts the control signals. Moreover, the effect of control delay should be treated carefully since it may degrade the performance of the feedforward loop [13].

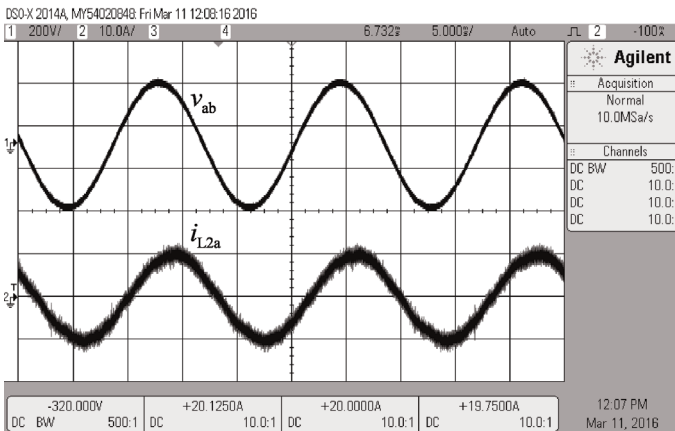


Figure 15.27 Inverter output current in a clean grid (only phase A shown).

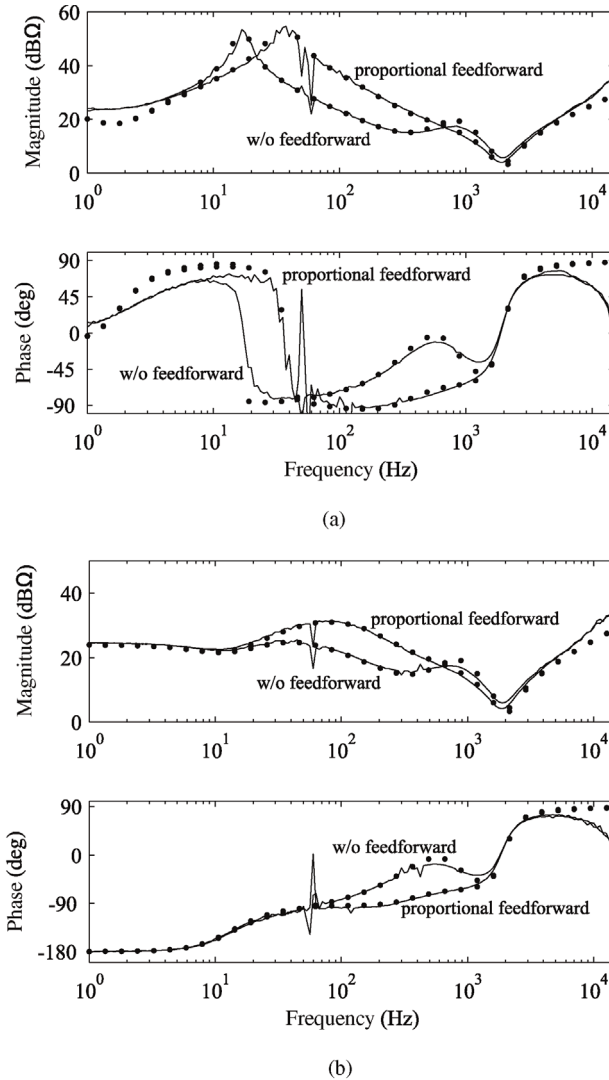


Figure 15.28 Measured impedance (a) d and (b) q-components with and without proportional feedforward.

15.5 Summary

In this chapter, the closed-loop model of three-phase current-fed inverter was derived with all the cross-coupling transfer functions. The model allows evaluating the shape of all four admittance components in the case of L-type and passively damped LCL filter. Moreover, the model can be easily adapted to include, for example, the effect of active damping [14–16]. The admittance models were verified by extracting frequency responses from a simulator and by measuring admittances from an experimental prototype.

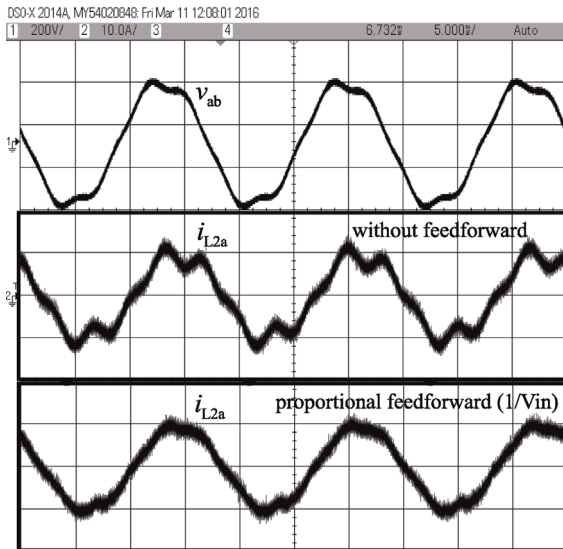


Figure 15.29 Inverter waveforms in distorted grid.

References

- 1 Mao, H., Boroyevich, D., and Lee, F.C. (1998) Novel reduced-order small-signal model of a three-phase PWM rectifier and its application in control design and system analysis. *IEEE Trans. Power Electron.*, **13** (3), 511–521.
- 2 Messo, T., Aapro, A., and Suntio, T. (2015) Generalized multivariable small-signal model of three-phase grid-connected inverter in DQ-domain. *IEEE 16th Workshop on Control and Modeling for Power Electronics*, pp. 1–8.
- 3 Harnefors, L. (2007) Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices. *IEEE Trans. Ind. Electron.*, **54** (4), 2239–2248.
- 4 Wen, B., Boroyevich, D., Burgos, R., Mattavelli, P., and Shen, Z. (2016) Analysis of D–Q small-signal impedance of grid-tied inverters. *IEEE Trans. Power Electron.*, **31** (1), 675–687.
- 5 Maciejowski, J.M. (1994) *Multivariable Feedback Design*, Addison-Wesley Publishers Ltd.
- 6 Skogestad, S. and Postlethwaite, I. (1998) *Multivariable Feedback Control: Analysis and Design*, John Wiley & Sons, Ltd., Chichester.
- 7 MacFarlane, A.G.J. and Postlethwaite, I. (1977) The generalized Nyquist stability criterion and multivariable root loci. *Int. J. Control*, **25** (1), 81–127.
- 8 Belkhat, M. (1997) *Stability Criteria for AC Power Systems with Regulated Loads*, Purdue University, West Lafayette, NI.
- 9 Wen, B., Boroyevich, D., Burgos, R., Mattavelli, P., and Shen, Z. (2015) Small-signal stability analysis of three-phase AC systems in the presence of constant power loads based on measured d–q frame impedances. *IEEE Trans. Power Electron.*, **30** (10), 5952–5963.

- 10 Cespedes, M. and Sun, J. (2014) Mitigation of inverter-grid harmonic resonance by narrow-band damping. *IEEE J. Emerg. Sel. Top. Power Electron.*, **2** (4), 1024–1031.
- 11 Messo, T., Apro, A., Suntio, T., and Roinila, T. (2016) Design of grid-voltage feedforward to increase impedance of grid-connected three-phase inverters with LCL-filter. *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 2675–2682.
- 12 Wang, X., Ruan, X., Liu, S., and Tse, C.K. (2010) Full feedforward of grid voltage for grid-connected inverter with LCL filter to suppress current distortion due to grid voltage harmonics. *IEEE Trans. Power Electron.*, **25** (12), 3119–3127.
- 13 Yan, Q., Wu, X., Yuan, X., and Geng, Y. (2016) An improved grid-voltage feedforward strategy for high-power three-phase grid-connected inverters based on the simplified repetitive predictor. *IEEE Trans. Power Electron.*, **31** (5), 3880–3897.
- 14 Apro, A., Messo, T., and Suntio, T. (2016) Effect of single-current-feedback active damping on the output impedance of grid-connected inverter. *18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, pp. 1–10.
- 15 Apro, A., Messo, T., and Suntio, T. (2015) An accurate small-signal model of a three-phase VSI-based photovoltaic inverter with LCL-filter. *9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, pp. 2267–2274.
- 16 Apro, A., Messo, T., and Suntio, T. (2015) Effect of active damping on the output impedance of PV inverter. *IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–8.

16

Impedance-Based Stability Assessment

16.1 Introduction

Grid-connected three-phase power electronic converters have been reported to suffer from power quality problems since the introduction of mercury-arc thyristor-based converters. In the work carried out by Ainsworth in 1967, abnormal harmonics were reported in a HVDC system that did not correspond to normal odd harmonics caused by normal operation of such converter [1]. The problems were reported to be most severe in a weak AC system. Moreover, the used control scheme had a significant impact on converter stability. Similar “harmonic instability” has been reported later, for example, in Ref. [2] related to a traction power system. The term “harmonic instability” or “harmonic resonance” might not be the optimal choice for discussing such phenomena since the frequency content of the voltage and current waveforms during such an abnormal operation may not be anyhow linked to actual fundamental frequency of the power system. This has been discussed in Ref. [3] where a scaled-down prototype inverter was demonstrated to generate subharmonic, interharmonic, and harmonic components depending on its control parameters. However, the term harmonic resonance has been widely used in the literature.

In recent years, power quality problems and unstable behavior have been reported in photovoltaic installations with high penetration level [4] and in grid-connected wind power systems [5]. In many cases, the control functions of grid-connected converter have been blamed to be at least partially responsible for producing the abnormal operation. It should be noted that modern power systems are becoming increasingly complex and, therefore, analyzing such problems or eliminating the problem source may become a tremendous challenge. However, failing to alleviate the harmonic stability problems may lead to unfortunate problems such as the case with the *BARD Offshore 1* wind farm [6].

Preventing harmonic resonances in grid-connected power electronic converters is not a trivial task and, therefore, this chapter does not even try to give an extensive analysis on how to succeed in this matter. The following analysis is based on the assumption that the power system is balanced and that the grid impedance seen by the grid-connected converter is either known or its worst-case behavior can be predicted [7] [8]. Moreover, the presented control systems and

topologies are still quite conventional [9] (without harmonic compensators) and may not represent the ones adopted by industry in high-end products.

This chapter demonstrates how impedance-based stability analysis can be utilized to find out whether there may be a risk for unstable behavior by applying the impedance models presented in Chapters 14 and 15. There are many other methods to model three-phase inverters and to evaluate stability, such as sequence-domain models [10], component connection method [11], and eigenvalue-based analysis [12]. The following analysis exploits the impedance models derived in the dq -domain [13–15]. The purpose of this chapter is not to make comparisons with other methods, merely just to walk the reader through one of the available methods. Moreover, the chapter aims to help the reader to understand the fundamental cause of the reported stability problems.

16.2 Modeling of Three-Phase Load Impedance in the dq -Domain

Load impedance seen by the grid-connected inverter should be modeled or measured to enable evaluating impedance-based stability margins. Figure 16.1 shows a general overview of an electrical three-phase source system connected to a three-phase load system. It is assumed that the source can be modeled as a Norton equivalent and the load as a Thevenin equivalent circuit. Stability problems can arise when the impedances at the interface between the source and load systems interact, much as in the case of interconnected DC–DC systems [16].

The closed-loop output admittance of grid-connected inverter can be derived in the dq -domain by using the methods presented in previous chapters. Reduced-order models were developed in Chapter 14 where cross-couplings between d and q - components were neglected. Therefore, the reduced-order model cannot be used to obtain cross-coupling admittances Y_{oqd-c} and Y_{odq-c} (assuming the source system represents a grid-connected inverter). Full-order models were discussed in Chapter 15, which can also be used to obtain the cross-coupling admittance terms and to include, for example, the effect of decoupling gains in the current controller.

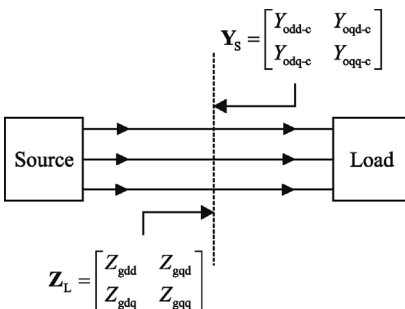


Figure 16.1 General overview of interconnected three-phase system.

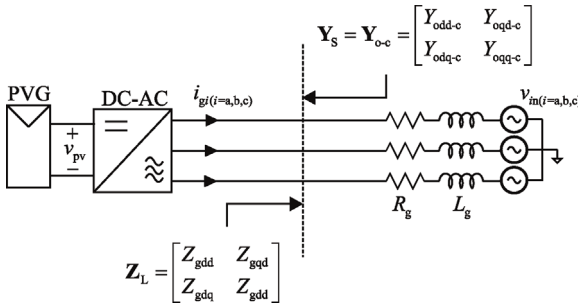


Figure 16.2 Inverter connected to a resistive-inductive grid.

Figure 16.2 shows a three-phase inverter connected to a grid impedance that behaves as a series RL branch. Such impedance model is generally used for evaluating inverter performance and stability in a weak grid where inverter is located in a rural area [7]. The “DC-AC” block contains all the feedback measurements and output filters of the inverter, that is, the inverter may have L, LC, or LCL-type output filter, while the emphasis in this section is to give an approximate model for the grid impedance.

Impedance of the resistive-inductive grid can be given as the input impedance of an equivalent single-phase system as in Eqs. (16.1) and (16.2) when cross-couplings between *d* and *q*-components are neglected.

$$Z_{gdd} = R_g + sL_g. \tag{16.1}$$

$$Z_{gqq} = R_g + sL_g. \tag{16.2}$$

Figure 16.3 shows a three-phase inverter connected to an inductive-resistive grid. The inverter inside “DC-AC” block contains an L-type output filter and the PLL synchronizes to the voltages over the passively damped AC capacitors. Therefore, the interface between the source and load systems can be selected according to the dashed line. The AC capacitors with passive damping, grid-side filter inductors, and the resistive-inductive grid impedance can be lumped together as the equivalent load impedance seen by the inverter. This simplifies the analysis since one only has to develop the admittance model for an inverter with L-type output filter. The admittance model can be obtained using the methods presented in Section 15.2.

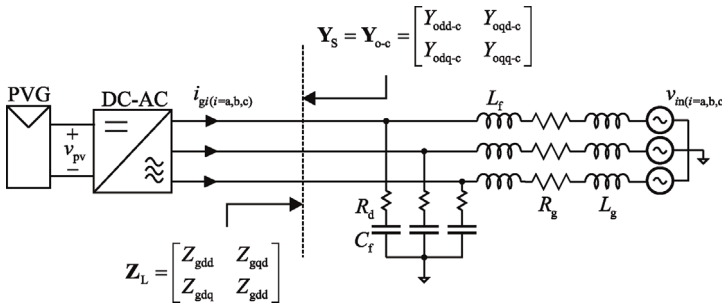


Figure 16.3 Inverter with LCL-type filter connected to resistive-inductive grid.

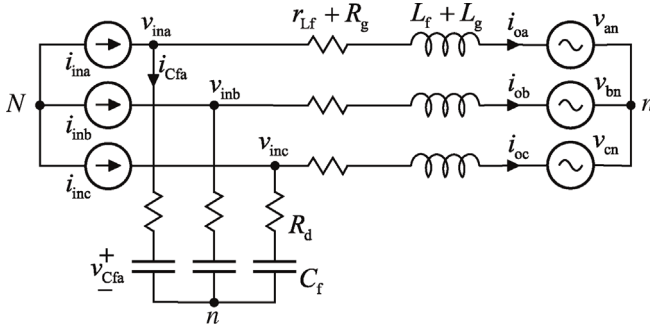


Figure 16.4 Three-phase CL filter connected to resistive–inductive grid.

The CL filter can be depicted as in Figure 16.4 by assuming it is fed by an ideal three-phase current source and loaded by ideal three-phase voltage source. Grid-side filter inductance L_f , grid inductance L_g , filter parasitic resistance r_{Lf} , and grid resistance R_g can be lumped together as an equivalent three-phase RL branch.

Three-phase inductor currents can be solved from Figure 16.4 and given as in (16.3) where subscript i denotes the corresponding phase variable a , b , or c .

$$\frac{di_{Li}}{dt} = \frac{1}{L_f + L_g} (-(R_g + r_{Lf})i_{Li} + v_{Cfi} + R_d i_{in} + v_{in}). \quad (16.3)$$

Capacitor voltages can be defined as in (16.4):

$$\frac{dv_{Cfi}}{dt} = \frac{1}{C_f} (i_{ini} - i_{Li}). \quad (16.4)$$

The linearized state-space can be given in the d – q domain as in (16.5) and (16.6):

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_{Cfd} \\ \hat{v}_{Cfq} \end{bmatrix} = \begin{bmatrix} -\frac{R_d + r_{Lf}}{L_g + L_f} & \omega_s & \frac{1}{L_g + L_f} & 0 \\ -\omega_s & -\frac{R_d + r_{Lf}}{L_g + L_f} & 0 & \frac{1}{L_g + L_f} \\ -\frac{1}{C_f} & 0 & 0 & \omega_s \\ 0 & -\frac{1}{C_f} & -\omega_s & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_{Cfd} \\ \hat{v}_{Cfq} \end{bmatrix} + \begin{bmatrix} \frac{R_d}{L_g + L_f} & 0 & -\frac{1}{L_g + L_f} & 0 \\ 0 & \frac{R_d}{L_g + L_f} & 0 & -\frac{1}{L_g + L_f} \\ \frac{1}{C_f} & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{ind} \\ \hat{i}_{inq} \\ \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (16.5)$$

$$\begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} = \begin{bmatrix} -R_d & 0 & 1 & 0 \\ 0 & -R_d & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_{Cfd} \\ \hat{v}_{Cfq} \end{bmatrix} + \begin{bmatrix} R_d & 0 & 0 & 0 \\ 0 & R_d & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{ind} \\ \hat{i}_{inq} \\ \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (16.6)$$

Transfer functions of the CL filter can be solved by using (12.26) and collected from the resulting transfer matrix \mathbf{G} according to (16.7). The input impedance d and q -components Z_{indd} , Z_{inqd} , Z_{indq} , and Z_{inqq} can be used to evaluate the impedance-based stability margins.

$$\begin{bmatrix} \hat{v}_{ind} \\ \hat{v}_{inq} \\ \hat{i}_{od} \\ \hat{i}_{oq} \end{bmatrix} = \begin{bmatrix} Z_{indd} & Z_{inqd} & T_{oidd} & T_{oiqd} \\ Z_{indq} & Z_{inqq} & T_{oidq} & T_{oiqq} \\ G_{iodd} & G_{ioqd} & -Y_{odd} & -Y_{oqd} \\ G_{iodq} & G_{ioqq} & -Y_{odq} & -Y_{oqq} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{ind} \\ \hat{i}_{inq} \\ \hat{v}_{od} \\ \hat{v}_{oq} \end{bmatrix} \quad (16.7)$$

16.3 Impedance-Based Stability Criterion

Figure 16.5 depicts the linear equivalent three-port model of a current-fed inverter when cross-coupling dynamics are neglected and it is assumed that input dynamics depend mainly on the d -components. Moreover, it is assumed that the grid impedance has only d and q -components. Thus, the cross-diagonal terms in the grid impedance matrix are neglected. The control inputs are the references of input voltage \hat{v}_{in}^* and output current q -component \hat{i}_{oq}^* . Inverter dynamics at closed loop can be given as in Eqs. (16.8)–(16.10):

$$\hat{v}_{in} = Z_{in-c} \hat{i}_{in} + T_{oid-c} \hat{v}_{od} + G_{cid-c} \hat{v}_{in}^* \quad (16.8)$$

$$\hat{i}_{od} = G_{iod-c} \hat{i}_{in} - Y_{odd-c} \hat{v}_{od} + G_{codd-c} \hat{v}_{in}^* \quad (16.9)$$

$$\hat{i}_{oq} = G_{ioq-c} \hat{i}_{in} - Y_{oqq-c} \hat{v}_{oq} + G_{coqq-c} \hat{i}_{oq}^* \quad (16.10)$$

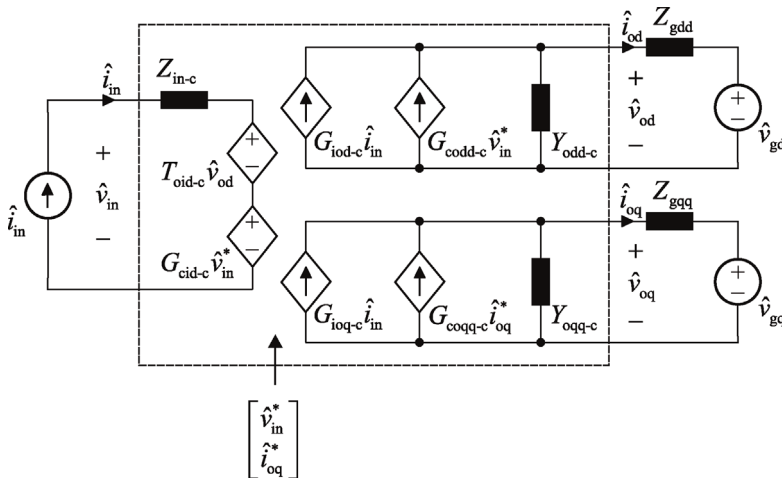


Figure 16.5 Three-port model with grid impedance.

Load-affected transfer functions can be solved from Figure 16.5 by noting that the AC voltage d and q -components seen by the inverter are affected by the grid impedance as in Eqs. (16.11) and (16.12) [17]:

$$\hat{v}_{od} = \hat{v}_{gd} + Z_{gdd}\hat{i}_{od}, \quad (16.11)$$

$$\hat{v}_{oq} = \hat{v}_{gq} + Z_{gqq}\hat{i}_{oq}. \quad (16.12)$$

The voltage d and q -components \hat{v}_{od} and \hat{v}_{oq} are substituted in Eqs. (16.8)–(16.10), which yields the load-affected transfer functions as given in Eqs. (16.13)–(16.15). The transfer functions can be used to analyze how grid impedance affects the inverter dynamics, such as input impedance or control bandwidth.

$$\begin{aligned} \hat{v}_{in} = & \frac{(1 + Z_{gdd}(Y_{odd-c} + [(T_{oid-c}G_{iod-c})/Z_{in-c}]))}{(1 + Y_{odd-c}Z_{gdd})} Z_{in-c}\hat{i}_{in} \\ & + \frac{1}{(1 + Y_{odd-c}Z_{gdd})} T_{oid-c}\hat{v}_{gd} \\ & + \frac{(1 + Z_{gdd}(Y_{odd-c} + [(T_{oid-c}G_{codd-c})/G_{cid-c}]))}{(1 + Y_{odd-c}Z_{gdd})} G_{cid-c}\hat{v}_{in}^*. \end{aligned} \quad (16.13)$$

$$\hat{i}_{od} = \frac{G_{iod-c}}{(1 + Y_{odd-c}Z_{gdd})}\hat{i}_{in} - \frac{Y_{odd-c}}{(1 + Y_{odd-c}Z_{gdd})}\hat{v}_{gd} + \frac{G_{codd-c}}{(1 + Y_{odd-c}Z_{gdd})}\hat{v}_{in}^*. \quad (16.14)$$

$$\hat{i}_{oq} = \frac{G_{ioq-c}}{(1 + Y_{oqq-c}Z_{gqq})}\hat{i}_{in} - \frac{Y_{oqq-c}}{(1 + Y_{oqq-c}Z_{gqq})}\hat{v}_{gq} + \frac{G_{coqq-c}}{(1 + Y_{oqq-c}Z_{gqq})}\hat{i}_{oq}^*. \quad (16.15)$$

All load-affected transfer functions have the same terms in the denominator, that is, the product of inverter output admittance and input impedance of the grid $Y_{odd-c}Z_{gdd}$ or $Y_{oqq-c}Z_{gqq}$. Each of the transfer functions is stable on their own when interactions with the grid impedance are not considered. However, both inverse minor loop gains $Y_{odd-c}Z_{gdd}$ and $Y_{oqq-c}Z_{gqq}$ can make the inverter unstable if the Nyquist stability criterion is not satisfied. If that is the case, each of the transfer functions in Eqs. (16.14) and (16.15) have an unstable pole and, thus, the inverter becomes unstable. To obtain stable operation, inverse minor loop gains in both Eq. (16.16) and Eq. (16.17) should be analyzed by plotting the corresponding Nyquist diagrams [18,19]:

$$ML_d = Y_{odd-c}Z_{gdd} = \frac{Z_{gdd}}{Z_{odd-c}}. \quad (16.16)$$

$$ML_q = Y_{oqq-c}Z_{gqq} = \frac{Z_{gqq}}{Z_{oqq-c}}. \quad (16.17)$$

16.4 Case Studies

16.4.1 Instability Due to High-Bandwidth PLL in Weak Grid

The current-fed inverter with L-type output filter of Section 15.3 is used as an example on how to evaluate impedance-based stability using the reduced-order impedance model. The simulation model is as shown in Figure 16.6. Controller parameters are the same as in Section 15.3 with the exception that two different PLL settings were used; in the first case, the PLL has crossover frequency of 20 Hz and in the second case 200 Hz. In both cases, the phase margin was set to 65° . In fact, this means that the q -component of inverter output admittance $Y_{\text{oqq-c}}$ will have a negative value $-I_{\text{od}}/V_{\text{od}}$ below the PLL bandwidth, which are approximately 10 and 100 Hz. Thus, the inverter output impedance q -component behaves as a negative resistance.

The grid impedance is assumed to be dominated by resistive and inductive parts with an R/X ratio of 1 to demonstrate that large grid resistance does not damp out oscillations caused by impedance-based interactions. Capacitance of the line impedance is neglected for brevity, because it generally affects only the high-frequency part of grid impedance [8]. The inverter may see large grid inductance when the inverter is used in a weak grid in rural area at the end of long medium voltage line [7]. Moreover, the inverter may be connected to the MV/LV transformer using underground cable that has dominantly resistive properties [8]. A transformer with low power rating may also introduce additional inductance.

A weak grid is characterized by a small short circuit ratio (SCR) [20] [21]. The short circuit ratio can be obtained as a ratio of theoretical short circuit current to nominal grid current or as the ratio of short circuit and nominal powers. The grid is assumed to resemble a series RL-circuit with inductance of 10 mH and resistance of 3.14 ohm, which corresponds approximately to a SCR of 5. The grid impedance d - and q -components can be given as in (16.18) by assuming that the cross-diagonal impedance terms Z_{gqd} and Z_{gdq} can be neglected.

$$Z_{\text{gdd}} = Z_{\text{gqq}} = 3.14 + s \cdot 10 \times 10^{-3}. \quad (16.18)$$

Inverter output admittance d -component is shown in Figure 16.7 as the equivalent impedance $Z_{\text{odd-c}} = (Y_{\text{odd-c}})^{-1}$. The solid line depicts the inverter impedance and the dashed line depicts the d -component of grid impedance. The inverter impedance d -component was obtained by using the reduced-order model in Eq. (14.41). The dashed line depicts the grid impedance d -component according to Eq. (16.18). The d -component of inverter output impedance is not affected by the PLL and has the same shape with both PLL settings. The low-frequency phase of the impedance is zero due to constant power source properties introduced by the DC voltage control. The grid and inverter impedances overlap at 262 Hz, that is, the impedances have the same magnitude. This is equivalent to having the inverse minor loop gain ML_d in Eq. (16.16) to cross the unity circle on the complex plane. However, the phase difference is much less than 180° and, therefore, the inverse minor loop gain does not encircle the $(-1,0)$ point.

Figure 16.8 shows the product of inverter admittance and grid impedance d -components on the complex plane, that is, the inverse minor loop $Y_{\text{odd-c}}Z_{\text{gdd}}$.

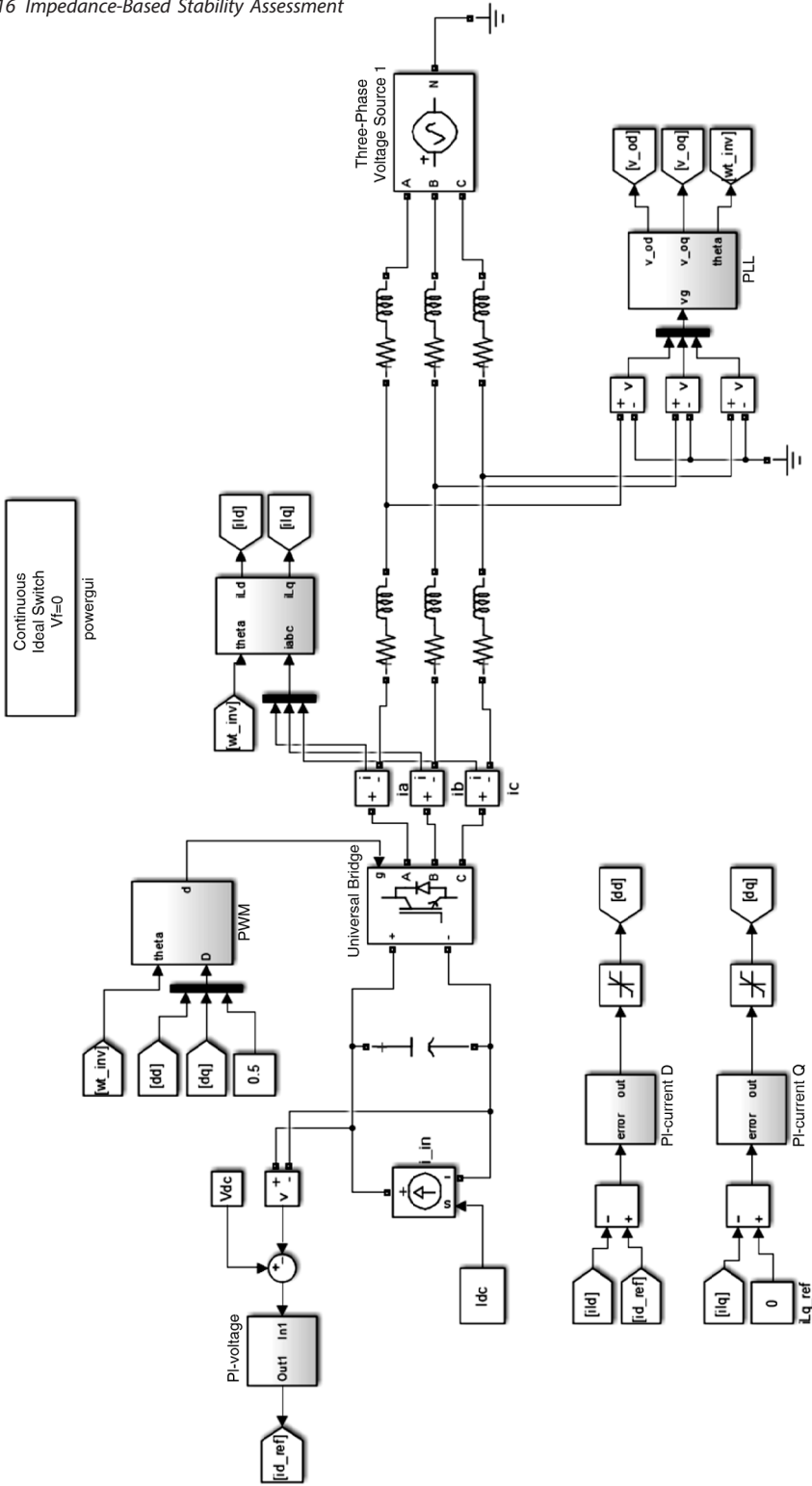


Figure 16.6 Simulation model to evaluate the effect of PLL bandwidth in weak grid.

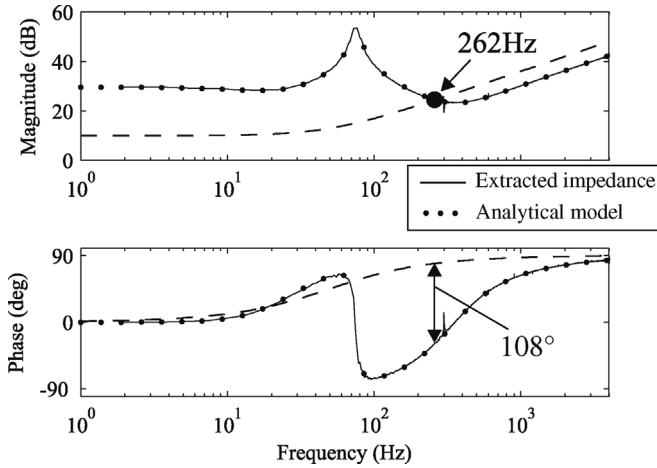


Figure 16.7 d -Components of grid (dashed) and inverter impedance (solid).

The contour does not encircle the $(-1,0)$ point and, thus, the inverter seems to be stable when only d -components are analyzed. Both impedances have their phase contained between -90 and $+90^\circ$, which means they behave as passive circuits. Therefore, the impedance d -component obviously cannot cause instability. In fact, inverter impedance should be designed to have characteristics as close to a passive circuit as possible to avoid impedance-based interactions [22,23].

Figure 16.9 shows the q -components of inverter output impedance ($Z_{oqq-c} = (Y_{oqq-c})^{-1}$) and the grid impedance q -component Z_{gqq} . The inverter impedance is shown as a solid line with the two different PLL parameters. The dots represent the impedance extracted from simulator. The impedances overlap at 139 Hz when PLL crossover frequency is set to 200 Hz, and at 243 Hz when PLL crossover frequency is set to 20 Hz. Overlapping impedances is an indication of

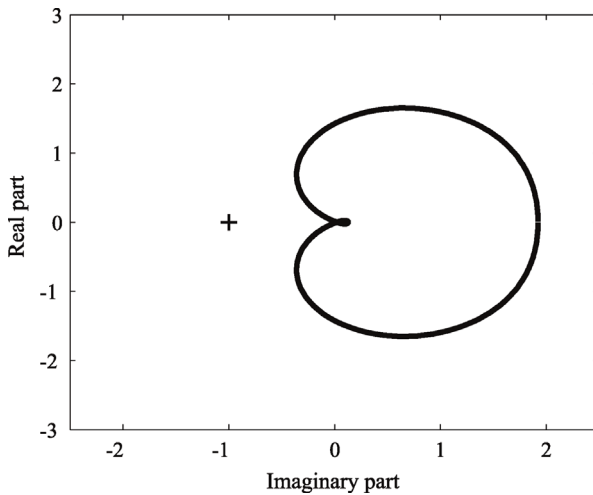


Figure 16.8 Ratio of impedance d -components ML_d on the complex plane.

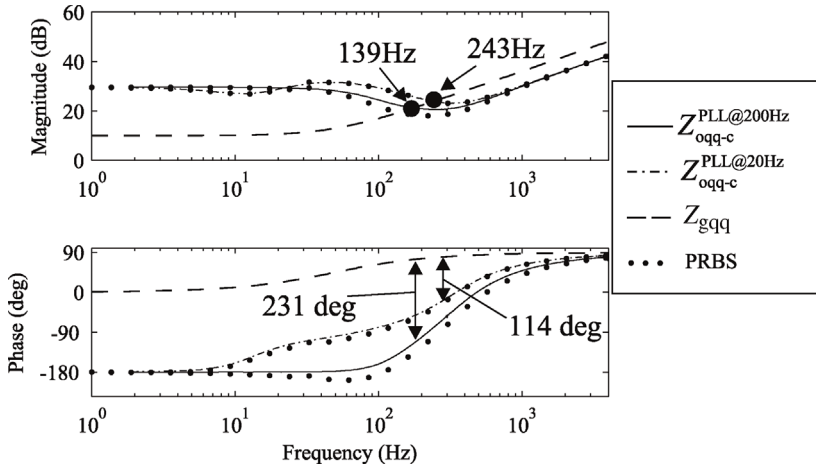


Figure 16.9 q -Components of grid (dashed) and inverter impedance (solid).

possible impedance-based interactions. However, the phase difference is 114° with slower PLL and 231° with faster PLL. The Nyquist stability criterion is violated if the phase difference is more than 180° at the frequency where impedances overlap. Thus, the inverter is unstable when the PLL is tuned to have 200 Hz crossover frequency.

Figure 16.10 shows the product of inverter admittance and grid impedance q -components on the complex plane, that is, the other inverse minor loop $Y_{oqq-c}Z_{gqq}$. The contour encircles the $(-1,0)$ point in clockwise direction once it indicates the minor loop has one RHP zero. Therefore, the load-affected dynamics in Eqs. (16.13)–(16.15) have a RHP pole when PLL crossover is selected

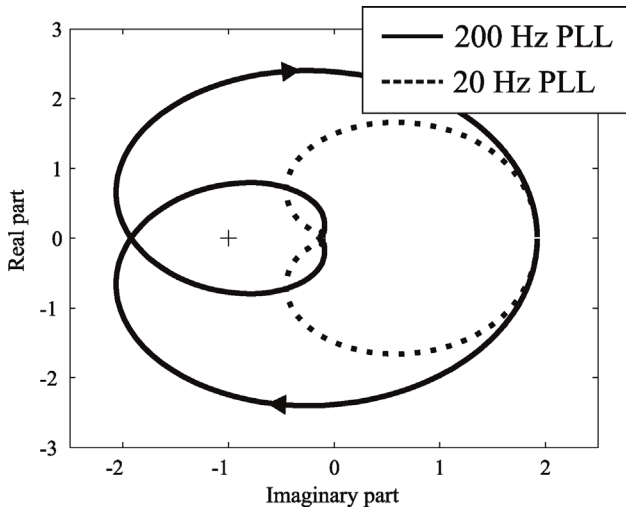


Figure 16.10 Ratio of impedance q -components when PLL crossover is 20 Hz (dashed) and 200 Hz (solid).

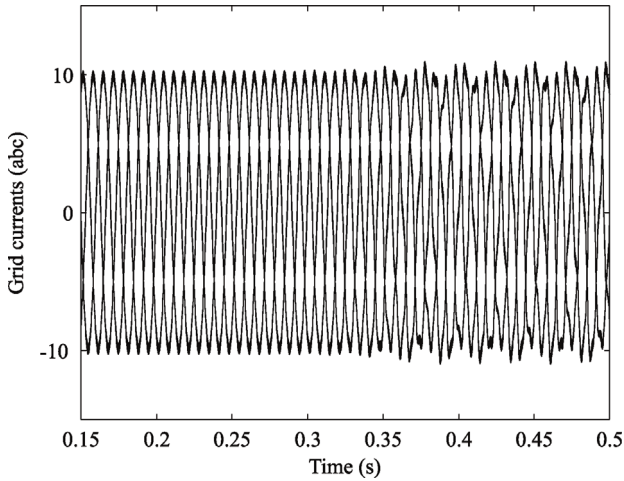


Figure 16.11 Grid currents with steadily growing oscillation.

as 200 Hz and, thus, the inverter becomes unstable. However, the inverter is stable when the PLL crossover frequency is reduced to 20 Hz.

Figure 16.11 shows the simulated grid current waveforms when PLL controller parameters are switched at 0.2 s to increase crossover frequency from 20 to 200 Hz. The oscillation in grid current increases gradually after 0.2 s. The inverter output currents become distorted after the PLL parameters are changed due to unstable interaction on impedance q -components.

Figure 16.12a shows zoomed waveforms in the stable case and Figure 16.12b in the unstable case. The impedance-based interaction appears as a sustained resonance rather than conventional instability where current or voltage tries

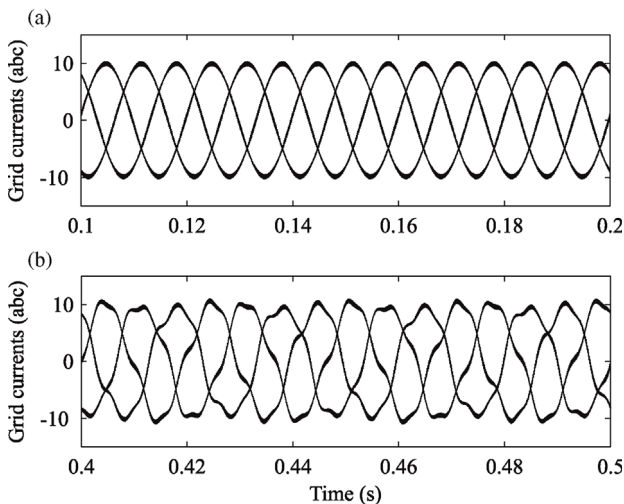


Figure 16.12 Grid currents in stable (a) and unstable (b) cases.

to ramp to infinity. This feature can make it very hard to identify if the power quality problem is caused by impedance-based interactions or, for example, background harmonics in grid voltage. After all, the waveform looks very much the same as the grid current in Figure 14.46, where the distortion was caused by low inverter impedance at the harmonic frequency. FFT analysis is an effective tool to determine whether the distortion is caused by grid harmonics or interactions of inverter and grid impedance. However, there is always the possibility that distortion caused by impedance-based interaction is located at the harmonic frequencies in which case it may be hard to identify the source of the problem [3].

It should be noted that the reduced-order model was used in this example to evaluate impedance-based stability margins. However, as can be seen by comparing the predicted impedance with the actual impedance in Figure 16.9, there is a slight difference in the phase of the impedance with faster PLL settings. Therefore, the reduced-order model may have somewhat limited accuracy in predicting the stability margin. However, the reduced-order model can still give a good indication whether there is a risk for impedance-based instability or not. The full-order dynamic model presented in Chapter 15 can be used to improve the accuracy of stability analysis as discussed in Refs [15,24,25], which is, however, beyond the scope of this book.

16.4.2 Instability Due to Control Delay in Feedforward Path

Impedance-based interactions of the inverter discussed in Section 14.4 are studied. The inverter employs an LC-type output filter. Such filter can be used when inverter is connected to the grid using a transformer. In the example case, the transformer was measured to have inductance of approximately $600\ \mu\text{H}$ and resistance of $400\ \text{m}\Omega$. Therefore, the LC filter and the transformer act effectively as an LCL-type filter.

Impedance-based stability of the inverter was studied by adding a $5\ \text{mH}$ three-phase inductor between the grid emulator and the isolation transformer, as depicted in Figure 16.13. The control delay originating from the DSP-based control platform decreases the phase of inverter output impedance when proportional grid voltage feedforward is used, as discussed in Section 14.4. Therefore,

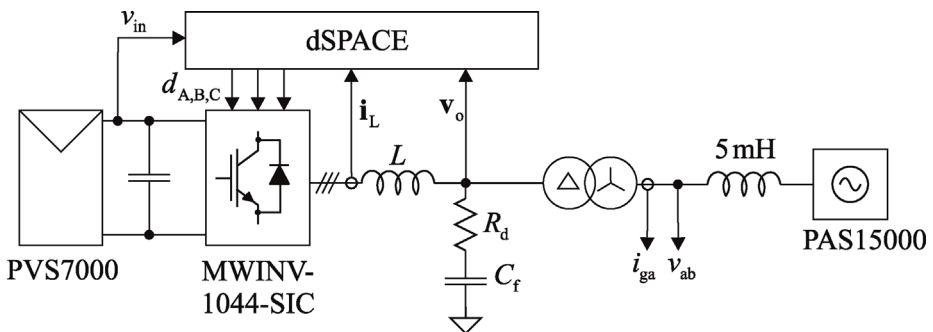


Figure 16.13 Inverter connected to an inductive load impedance.

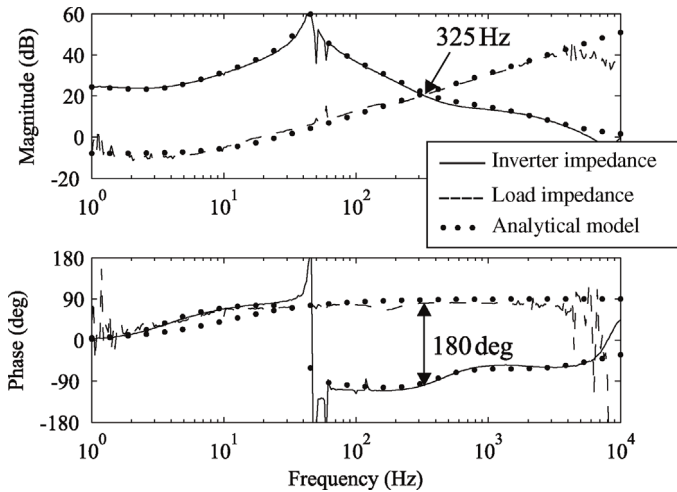


Figure 16.14 Impedance d -components with initial proportional feedforward gain.

the inverter may be vulnerable to impedance-based instability in the case when grid impedance has a large magnitude, such as in the weak grid case. As a matter of fact, the inverter was observed to become unstable when switching frequency was reduced from 20 to 16 kHz because this causes control delay to increase.

The proportional feedforward gains were selected as the inverse of inverter DC voltage, while the PV generator was operated at the MPP, 414.3 V.

Figure 16.14 shows the initial impedance d -components together with the measured impedances when the switching frequency was selected as 16 kHz and proportional feedforward gains G_{ffd} and G_{ffq} as the inverse of DC voltage $1/414.3$. The solid line depicts the d -component of inverter output impedance and the dashed line is the total impedance of the load (transformer and the series inductor.) The load impedance was approximated as in Eq. (16.19), which includes the impedance of the isolation transformer:

$$Z_{\text{gdd}} = 0.4 + s \cdot 5.6 \times 10^{-3}. \quad (16.19)$$

The impedance d -components overlap at approximately 325 Hz and their phase difference is 180° , which indicates instability. The instability is caused by delay of the control system together with too large proportional feedforward gain. The grid voltage feedforward decreases the phase of the inverter output impedance below -90° around few hundreds of Hertz due to control delay, as discussed in Chapter 14.

Three-phase grid currents are shown in Figure 16.15 (middle of the figure) together with phase-to-phase voltage. Interaction of impedance d -components can be seen as large oscillations in the grid current. The inverter impedance was reshaped by reducing the value of proportional feedforward gain G_{ffd} to $0.8/414.3$, which effectively reduces the detrimental effect of control delay.

The reshaped impedances are shown in Figure 16.16 where grid and inverter impedances overlap at 316 Hz. However, the phase difference is less than 180° and the inverter is stable, as can be seen in Figure 16.15 (lower current waveforms). It

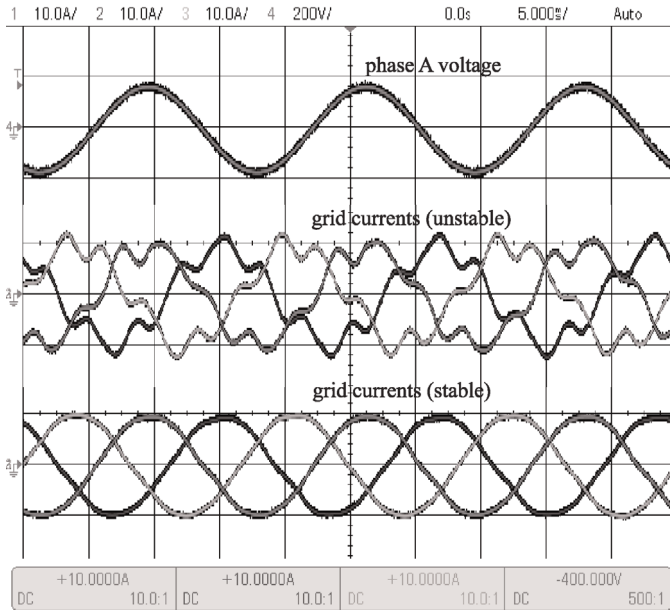


Figure 16.15 Grid currents in unstable and stable cases.

should be noted that even though the inverter is stable at steady state, the stability margin (derived from impedance d -components) is just 21° . Therefore, large oscillations would still be seen during transients, but these oscillations are damped out after a short transient.

Figure 16.17 shows the ratio of impedance d -components on the complex plane in both cases. The impedance ratio is obtained by using the analytical inverter impedance d -component in Eq. (14.83) and the grid impedance in Eq. (16.19).

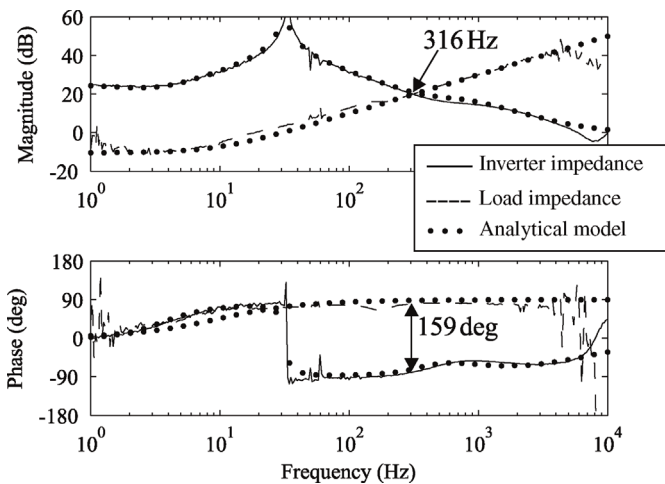


Figure 16.16 Impedance d -components with reduced proportional feedforward gain.

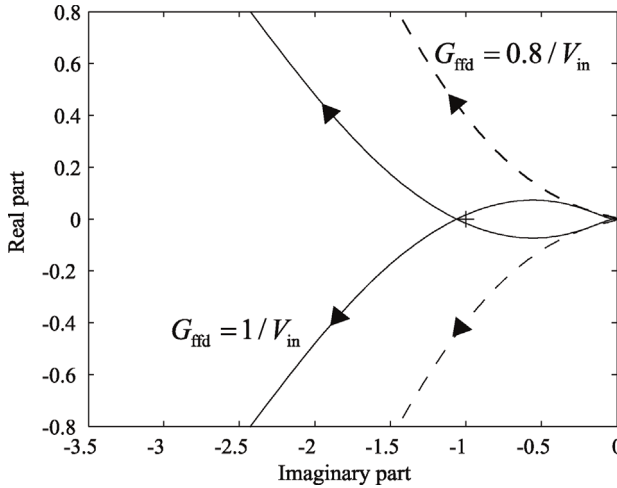


Figure 16.17 Ratio of impedance d -components obtained using the dynamic model.

The impedance ratio encircles the $(-1,0)$ point with the initial feedforward gain and, thus, the inverter becomes unstable. However, the inverter is stable when the feedforward gain is reduced by 20% as the contour does not encircle the $(-1,0)$ point.

As already mentioned, it was observed that in the example case, the instability was caused by the impedance d -components. However, the q -components can also cause impedance-based interactions, as demonstrated by the wide-bandwidth PLL in the previous section. Figure 16.18 shows the impedance q -component given by the reduced-order model according to Eq. (14.84), the grid impedance model Eq. (16.19), and the corresponding measured impedances. The impedance q -components overlap at 335 Hz, but the phase difference is less than 180° . Thus, the q -components do not cause instability.

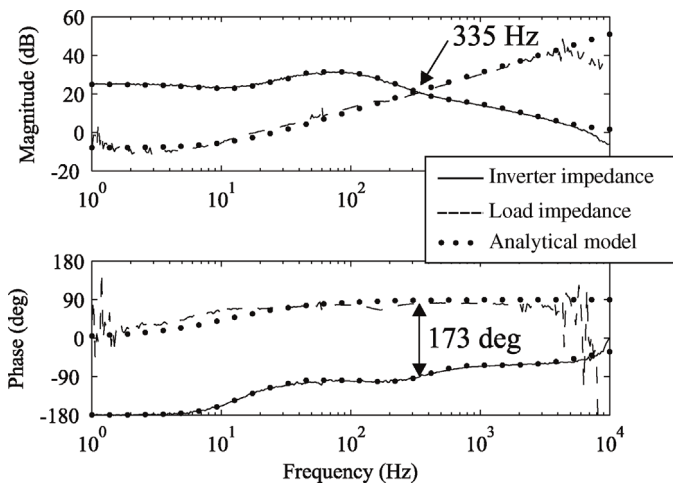


Figure 16.18 Impedance q -components.

However, it would be beneficial for the transient behavior to also reduce the feedforward gain G_{ffq} in order to increase the stability margin.

16.5 Summary

In this chapter, the impedance models developed earlier were applied to evaluate impedance-based stability of a grid-connected inverter. As a first case study, a fast PLL control loop was demonstrated to cause instability in a weak grid due to the negative resistance behavior. As a second case study, the grid voltage feedforward loop was shown to cause instability due to nonpassive impedance behavior caused by control delay. However, in both cases, the inverter could be stabilized by reshaping the inverter output impedance by changing the control parameters. The dynamic model presented in this book provides a necessary and accurate tool for impedance shaping of grid-connected converters in order to avoid instability.

References

- 1 Ainsworth, J.D. (1967) Harmonic instability between controlled static convertors and A.C. networks. *Proc. Inst. Electr. Eng.*, **114** (7), 949–957.
- 2 Mollerstedt, E. and Bernhardsson, B. (2000) Out of control because of harmonics: an analysis of the harmonic response of an inverter locomotive. *IEEE Control Syst.*, **20** (4), 70–81.
- 3 Messo, T., Jokipii, J., Aapro, A., and Suntio, T. (2014) Time and frequency-domain evidence on power quality issues caused by grid-connected three-phase photovoltaic inverters 16th European Conference Power Electronics and Applications (EPE-ECCE Europe).
- 4 Enslin, J.H.R. and Heskes, P.J.M. (2004) Harmonic interaction between a large number of distributed power inverters and the distribution network. *IEEE Trans. Power Electron.*, **19** (6), 1586–1593.
- 5 Belkin, P. (2010) Event of 10/22/09. CREZ Technical Conference on Electrical Reliability, Council of Texas.
- 6 GmbH, W. (2014) Rätselhafter Defekt legt größten Windpark lahm. Available at <https://www.welt.de/wirtschaft/article131879638/Ra> (accessed December 12, 2016).
- 7 Liserre, M., Teodorescu, R., and Blaabjerg, F. (2006) Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values. *IEEE Trans. Power Electron.*, **21** (1), 263–271.
- 8 Jessen, L. and Fuchs, F.W. (2015) Modeling of inverter output impedance for stability analysis in combination with measured grid impedances. *IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1–7.
- 9 Blaabjerg, F., Teodorescu, R., Liserre, M., and Timbus, A.V. (2006) Overview of control and grid synchronization for distributed power generation systems. *IEEE Trans. Ind. Electron.*, **53** (5), 1398–1409.

- 10 Cespedes, M. and Sun, J. (2014) Impedance modeling and analysis of grid-connected voltage-source converters. *IEEE Trans. Power Electron.*, **29** (3), 1254–1261.
- 11 Wang, X., Blaabjerg, F., Chen, Z., and Wu, W. (2014) Modeling and analysis of harmonic stability in an AC power-electronics-based power system. *IEEE Trans. Power Electron.*, **29** (12), 6421–6432.
- 12 Hu, J., Huang, Y., Wang, D., Yuan, H., and Yuan, X. (2015) Modeling of grid-connected DFIG-based wind turbines for DC-link voltage stability analysis. *IEEE Trans. Sustain. Energy*, **6** (4), 1325–1336.
- 13 Messo, T., Jokipii, J., Makinen, A., and Suntio, T. (2013) Modeling the grid synchronization induced negative-resistor-like behavior in the output impedance of a three-phase photovoltaic inverter. 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 1–7.
- 14 Messo, T., Jokipii, J., and Suntio, T. (2014) Effect of conventional grid-voltage feedforward on the output impedance of a three-phase photovoltaic inverter. 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 – ECCE ASIA), No. 1, pp. 514–521.
- 15 Messo, T., Aapro, A., and Suntio, T. (2015) Generalized multivariable small-signal model of three-phase grid-connected inverter in DQ-domain. IEEE 16th Workshop on Control and Modeling for Power Electronics, pp. 1–8.
- 16 Middlebrook, R.D. (1976) Input filter considerations in design and application of switching regulators. Proceedings of the IEEE Industry Applications Society Annual Meeting, pp. 366–382.
- 17 Puukko, J. and Suntio, T. (2012) Modelling the effect of non-ideal load in three-phase converter dynamics. *Electron. Lett.*, **48** (7), 402.
- 18 Sun, J. (2011) Impedance-based stability criterion for grid-connected inverters. *IEEE Trans. Power Electron.*, **26** (11), 3075–3078.
- 19 Wen, B., Boroyevich, D., Burgos, R., Mattavelli, P., and Shen, Z. (2017) Inverse Nyquist stability criterion for grid-tied inverters. *IEEE Trans. Power Electron.*, **32** (2), 1548–1556.
- 20 Gavrilovic, A. (1991) AC/DC system strength as indicated by short circuit ratios. International Conference on AC and DC Power Transmission, pp. 27–32.
- 21 IEEE Std 551–2006 (2006) Recommended Practice for Calculating AC Short-Circuit Currents in Industrial and Commercial Power Systems, [The Violet Book], pp. 1–308.
- 22 Harnefors, L., Wang, X., Yepes, A., and Blaabjerg, F. (2015) Passivity-based stability assessment of grid-connected VSCs: an overview. *IEEE J. Emerg. Sel. Top. Power Electron.*, **4** (1), 116–125.
- 23 Harnefors, L., Bongiorno, M., and Lundberg, S. (2007) Input-admittance calculation and shaping for controlled voltage-source converters. *IEEE Trans. Ind. Electron.*, **54** (6), 3323–3334.
- 24 MacFarlane, A.G.J. and Postlethwaite, I. (1977) The generalized Nyquist stability criterion and multivariable root loci. *Int. J. Control*, **25** (1), 81–127.
- 25 Belkhat, M. (1997) *Stability Criteria for AC Power Systems with Regulated Loads*, Purdue University, West Lafayette, NI.

17

Dynamic Modeling of Three-Phase Active Rectifiers

17.1 Introduction

This chapter provides an introduction to modeling of active rectifiers. Further analysis such as control design and derivation of closed-loop models [1–7] is beyond the scope of the book because the active rectifier is a perfect topic for self-studies and provides a good basis for homework topics for students at university-level courses. Moreover, a grid-connected active rectifier serves as a good platform for implementing laboratory assignments, since one does not require expensive grid or PV emulators.

17.2 Open-Loop Dynamics

Active rectifiers are commonly found in motor drive applications. They have been used to replace the three-phase diode bridge enabling significantly better power quality and the possibility for four quadrant operation with regenerative braking. The dynamic model of an active rectifier can be obtained by using identical methods as in modeling of three-phase inverters. Main difference is the reversed power flow. Moreover, the grid voltages act as the source system and the DC link as a load system.

Power stage of the active rectifier is shown in Figure 17.1. The three-phase grid acts as a source system and current sink connected at the DC side acts as a load system. The rectifier has a DC capacitor to enable control of the load voltage. The DC load can be, for example, a storage battery or a motor drive. However, for obtaining the dynamic model without the effect of load, the load is modeled as an ideal current sink with current i_o . The DC voltage is selected as an output variable v_o and grid voltages v_{an} , v_{bn} , and v_{cn} as input variables.

The equivalent switch matrix is depicted in Figure 17.2 where the transistors are modeled as SPDT switches and losses are modeled by parasitic resistances.

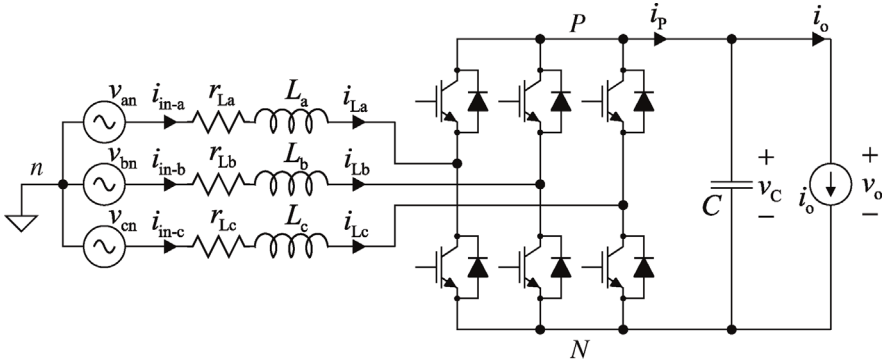


Figure 17.1 Power stage of an active rectifier.

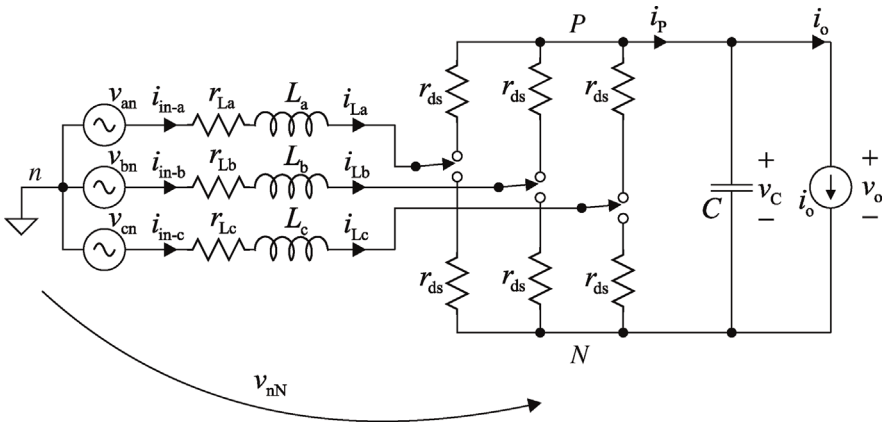


Figure 17.2 Equivalent switch matrix of an active rectifier.

The average voltage over each phase inductance can be defined as in Eq. (17.1) where i denotes the corresponding phase, that is, a, b, or c:

$$\frac{d\langle i_{Li} \rangle}{dt} = \frac{1}{L} (\langle v_{in} \rangle - (r_L + r_{ds}) \langle i_{Li} \rangle - d_i \langle v_o \rangle + \langle v_{nN} \rangle). \quad (17.1)$$

Three-phase inductor currents can be given by three-dimensional vectors as in Eq. (17.2) where the equivalent resistance r_{eq} is the sum of parasitic resistances r_L and r_{ds} .

$$\frac{d}{dt} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} = \frac{1}{L} \left(\begin{bmatrix} \langle v_{an} \rangle \\ \langle v_{bn} \rangle \\ \langle v_{cn} \rangle \end{bmatrix} - r_{eq} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} - \begin{bmatrix} d_A \\ d_B \\ d_C \end{bmatrix} \langle v_o \rangle + \begin{bmatrix} \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \end{bmatrix} \right). \quad (17.2)$$

The three-phase inductor currents are transformed into stationary reference frame by using Clarke's transformation as in Eq. (17.3), which yields the inductor currents in stationary reference frame given in Eq. (17.4). The amplitude-invariant

transformation is assumed. The subscript “-in” is used to denote that the grid voltage is treated as an input voltage of the power stage.

$$\frac{d}{dt} T^{\alpha\beta} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} = \frac{1}{L} \left(T^{\alpha\beta} \begin{bmatrix} \langle v_{an} \rangle \\ \langle v_{bn} \rangle \\ \langle v_{cn} \rangle \end{bmatrix} - r_{eq} T^{\alpha\beta} \begin{bmatrix} \langle i_{La} \rangle \\ \langle i_{Lb} \rangle \\ \langle i_{Lc} \rangle \end{bmatrix} - T^{\alpha\beta} \begin{bmatrix} d_A \\ d_B \\ d_C \end{bmatrix} \langle v_o \rangle \right. \\ \left. + T^{\alpha\beta} \begin{bmatrix} \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \\ \langle v_{nN} \rangle \end{bmatrix} \right). \quad (17.3)$$

$$\frac{d}{dt} \begin{bmatrix} \langle i_{L\alpha} \rangle \\ \langle i_{L\beta} \rangle \\ \langle i_{L0} \rangle \end{bmatrix} = \frac{1}{L} \left(\begin{bmatrix} \langle v_{\alpha-in} \rangle \\ \langle v_{\beta-in} \rangle \\ \langle v_{0-in} \rangle \end{bmatrix} - r_{eq} \begin{bmatrix} \langle i_{L\alpha} \rangle \\ \langle i_{L\beta} \rangle \\ \langle i_{L0} \rangle \end{bmatrix} - \begin{bmatrix} d_\alpha \\ d_\beta \\ d_0 \end{bmatrix} \langle v_o \rangle + \begin{bmatrix} 0 \\ 0 \\ \langle v_{nN} \rangle \end{bmatrix} \right). \quad (17.4)$$

The zero component is neglected, which allows defining the inductor current as a rotating space-vector as

$$\frac{d}{dt} \mathbf{i}_L^{\alpha\beta} = \frac{1}{L} \mathbf{v}_{in}^{\alpha\beta} - \frac{r_{eq}}{L} \mathbf{i}_L^{\alpha\beta} - \mathbf{d}^{\alpha\beta} \frac{\langle v_o \rangle}{L}. \quad (17.5)$$

The inductor current can be given in the synchronous reference frame, that is, in the dq -domain by noting the relationship between a rotating and a stationary reference frame ($\mathbf{x}^{\alpha\beta} = \mathbf{x}^{dq} \cdot e^{j\omega_s t}$). The transformation produces cross-couplings between inductor current d and q -components. The inductor currents can be defined as

$$\frac{d}{dt} \mathbf{i}_L^{dq} = \frac{1}{L} \mathbf{v}_{in}^{dq} - \frac{r_{eq}}{L} \mathbf{i}_L^{dq} - j\omega_s \mathbf{i}_L^{dq} - \mathbf{d}^{dq} \frac{\langle v_o \rangle}{L}. \quad (17.6)$$

Average voltage of the output capacitor can be solved by utilizing the Kirchhoff's current law as

$$\frac{d\langle v_C \rangle}{dt} = \frac{1}{C} (\langle i_p \rangle - \langle i_o \rangle) = \frac{1}{C} \left(\frac{3}{2} (d_d \langle i_{Ld} \rangle + d_q \langle i_{Lq} \rangle) - \langle i_o \rangle \right). \quad (17.7)$$

Finally, the average state-space model can be written by using the equivalent variables in the dq -domain as in Eqs. (17.8)–(17.13):

$$\frac{d\langle i_{Ld} \rangle}{dt} = \frac{\langle v_{ind} \rangle}{L} - \frac{r_{eq}}{L} \langle i_{Ld} \rangle + \omega_s \langle i_{Lq} \rangle - \frac{d_d}{L} \langle v_C \rangle, \quad (17.8)$$

$$\frac{d\langle i_{Lq} \rangle}{dt} = \frac{\langle v_{inq} \rangle}{L} - \frac{r_{eq}}{L} \langle i_{Lq} \rangle - \omega_s \langle i_{Ld} \rangle - \frac{d_q}{L} \langle v_C \rangle, \quad (17.9)$$

$$\frac{d\langle v_C \rangle}{dt} = \frac{3}{2C} d_d \langle i_{Ld} \rangle + \frac{3}{2C} d_q \langle i_{Lq} \rangle - \frac{1}{C} \langle i_o \rangle, \quad (17.10)$$

$$\langle i_{ind} \rangle = \langle i_{Ld} \rangle, \quad (17.11)$$

$$\langle i_{inq} \rangle = \langle i_{Lq} \rangle, \quad (17.12)$$

$$\langle v_o \rangle = \langle v_C \rangle. \quad (17.13)$$

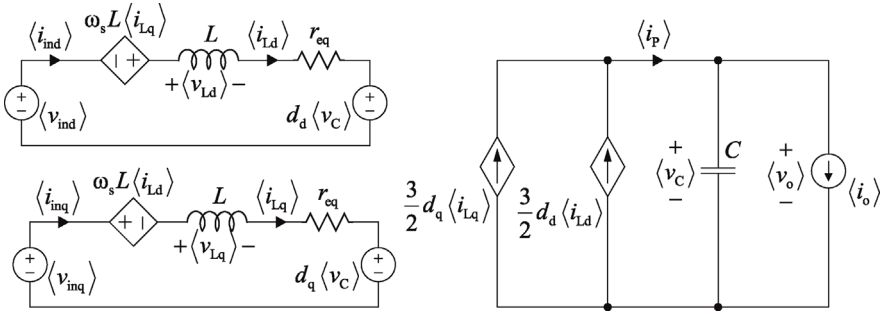


Figure 17.3 Equivalent circuit model of an active rectifier.

The equivalent circuit model of the active rectifier can be depicted as in Figure 17.3. The average model can be used for simulation studies and evaluating control system stability, because control loops are usually tuned to have much smaller bandwidths than the switching frequency. Therefore, the simulation step size can be significantly longer. Such model can represent the dynamic behavior of the control system with sufficient accuracy.

Steady-state operating point of the active rectifier can be solved from the average model given in Eqs. (17.8)–(17.13) by noting that in steady state all derivatives are zero, that is, all transients have disappeared. Moreover, all the variables are replaced by their steady-state values (uppercase letters) yielding Eqs. (17.14)–(17.16)

$$0 = V_{ind} - r_{eq}I_{Ld} + \omega_s L I_{Lq} - D_d V_C, \quad (17.14)$$

$$0 = V_{inq} - r_{eq}I_{Lq} - \omega_s L I_{Ld} - D_q V_C, \quad (17.15)$$

$$0 = \frac{3}{2}D_d I_{Ld} + \frac{3}{2}D_q I_{Lq} - I_o. \quad (17.16)$$

The q -component of grid voltage V_{inq} (or inverter input voltage q -component to be precise) is equal to zero due to the PLL. Moreover, it is assumed that the rectifier operates at unity power factor; thus, grid current q -component I_{Lq} is zero. It is also assumed that the output voltage V_o and output current I_o are known. The steady-state operating point can be given as in Eqs. (17.17)–(17.20).

$$I_{Ld} = \frac{2I_o}{3D_d}, \quad (17.17)$$

$$V_C = V_o, \quad (17.18)$$

$$D_q = -\frac{2\omega_s L I_o}{3D_d V_o}, \quad (17.19)$$

$$V_o(D_d)^2 - V_{ind}D_d + \frac{2}{3}r_{eq}I_o = 0. \quad (17.20)$$

The duty ratio d -component can be solved numerically by applying the solution of a second-order polynomial as in Eq. (17.21) after which the numerical values of inductor current d -component and duty ratio q -component can be solved from Eqs. (17.17) and (17.19), respectively.

$$D_d = \frac{V_{\text{ind}} + \sqrt{(V_{\text{ind}})^2 - \frac{8}{3} r_{\text{eq}} V_o I_o}}{2V_o}. \quad (17.21)$$

The linearized state-space can be obtained from the average model by developing the proper first-order partial derivatives with respect to each state and input variable and can be given as in Eqs. (17.22)–(17.27):

$$\frac{d\hat{i}_{Ld}}{dt} = -\frac{r_{\text{eq}}}{L} \hat{i}_{Ld} + \omega_s \hat{i}_{Lq} - \frac{D_d}{L} \hat{v}_C + \frac{1}{L} \hat{v}_{\text{ind}} - \frac{V_C}{L} \hat{d}_d. \quad (17.22)$$

$$\frac{d\hat{i}_{Lq}}{dt} = -\frac{r_{\text{eq}}}{L} \hat{i}_{Lq} - \omega_s \hat{i}_{Ld} - \frac{D_q}{L} \hat{v}_C + \frac{1}{L} \hat{v}_{\text{in}q} - \frac{V_C}{L} \hat{d}_q. \quad (17.23)$$

$$\frac{d\hat{v}_C}{dt} = \frac{3D_d}{2C} \hat{i}_{Ld} + \frac{3D_q}{2C} \hat{i}_{Lq} - \frac{1}{C} \hat{i}_o + \frac{3I_{Ld}}{2C} \hat{d}_d + \frac{3I_{Lq}}{2C} \hat{d}_q. \quad (17.24)$$

$$\hat{i}_{\text{ind}} = \hat{i}_{Ld}. \quad (17.25)$$

$$\hat{i}_{\text{in}q} = \hat{i}_{Lq}. \quad (17.26)$$

$$\hat{v}_o = \hat{v}_C. \quad (17.27)$$

The state matrices can be given as in Eqs. (17.28) and (17.29):

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{r_{\text{eq}}}{L} & \omega_s & -\frac{D_d}{L} \\ -\omega_s & -\frac{r_{\text{eq}}}{L} & -\frac{D_q}{L} \\ \frac{3D_d}{2C} & \frac{3D_q}{2C} & 0 \end{bmatrix}}_A \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} & 0 \\ 0 & \frac{1}{L} & 0 & 0 & -\frac{V_C}{L} \\ 0 & 0 & -\frac{1}{C} & \frac{3I_{Ld}}{2C} & \frac{3I_{Lq}}{2C} \end{bmatrix}}_B \begin{bmatrix} \hat{v}_{\text{ind}} \\ \hat{v}_{\text{in}q} \\ \hat{i}_o \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (17.28)$$

$$\begin{bmatrix} \hat{i}_{\text{ind}} \\ \hat{i}_{\text{in}q} \\ \hat{v}_o \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}}_C \begin{bmatrix} \hat{i}_{Ld} \\ \hat{i}_{Lq} \\ \hat{v}_C \end{bmatrix} + \underbrace{0}_D \cdot \begin{bmatrix} \hat{v}_{\text{ind}} \\ \hat{v}_{\text{in}q} \\ \hat{i}_o \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (17.29)$$

Transfer function matrix **G** can be solved in the frequency domain by using Eq. (12.27). The dynamic model has five inputs and three outputs, and thus,

15 transfer functions are obtained using MATLAB and collected from matrix \mathbf{G} as shown in Eq. (17.30).

$$\begin{bmatrix} \hat{i}_{\text{ind}} \\ \hat{i}_{\text{inq}} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Y_{\text{indd-o}} & Y_{\text{inqd-o}} & T_{\text{oid-o}} & G_{\text{cidd-o}} & G_{\text{ciqd-o}} \\ Y_{\text{indq-o}} & Y_{\text{inqq-o}} & T_{\text{oiq-o}} & G_{\text{cidq-o}} & G_{\text{ciqq-o}} \\ G_{\text{iod-o}} & G_{\text{ioq-o}} & -Z_{\text{o-o}} & G_{\text{cod-o}} & G_{\text{coq-o}} \end{bmatrix} \cdot \begin{bmatrix} \hat{v}_{\text{ind}} \\ \hat{v}_{\text{inq}} \\ \hat{i}_o \\ \hat{d}_d \\ \hat{d}_q \end{bmatrix} \quad (17.30)$$

The transfer functions can be collected as submatrices, or as transfer matrices as in Eq. (17.31) where part of the matrices are intentionally filled with zeros to have all submatrices as to two-by-two matrices. This modification allows analyzing the rectifier using transfer matrices which is how the dynamics of MIMO systems are usually analyzed.

$$\begin{bmatrix} \begin{bmatrix} \hat{i}_{\text{ind}} \\ \hat{i}_{\text{inq}} \end{bmatrix} \\ \begin{bmatrix} \hat{v}_o \\ 0 \end{bmatrix} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} Y_{\text{indd-o}} & Y_{\text{inqd-o}} \\ Y_{\text{indq-o}} & Y_{\text{inqq-o}} \end{bmatrix} & \begin{bmatrix} T_{\text{oid-o}} & 0 \\ T_{\text{oiq-o}} & 0 \end{bmatrix} & \begin{bmatrix} G_{\text{cidd-o}} & G_{\text{ciqd-o}} \\ G_{\text{cidq-o}} & G_{\text{ciqq-o}} \end{bmatrix} \\ \begin{bmatrix} G_{\text{iod-o}} & G_{\text{ioq-o}} \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} -Z_{\text{o-o}} & 0 \\ 0 & 0 \end{bmatrix} & \begin{bmatrix} G_{\text{cod-o}} & G_{\text{coq-o}} \\ 0 & 0 \end{bmatrix} \end{bmatrix} \begin{bmatrix} \begin{bmatrix} \hat{v}_{\text{ind}} \\ \hat{v}_{\text{inq}} \end{bmatrix} \\ \begin{bmatrix} \hat{i}_o \\ 0 \end{bmatrix} \\ \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} \end{bmatrix} \quad (17.31)$$

The transfer matrices can be given as in Eq. (17.32) where each transfer matrix corresponds to a submatrix collected from Eq. (17.31). Input and output variables are given as input and output vectors, that is, $\mathbf{i}_{\text{in}} = [\hat{i}_{\text{ind}} \ \hat{i}_{\text{inq}}]^T$.

$$\begin{bmatrix} \hat{\mathbf{i}}_{\text{in}} \\ \hat{\mathbf{v}}_o \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{\text{in-o}} & \mathbf{T}_{\text{oi-o}} & \mathbf{G}_{\text{ci-o}} \\ \mathbf{G}_{\text{io-o}} & -\mathbf{Z}_{\text{o-o}} & \mathbf{G}_{\text{co-o}} \end{bmatrix} \begin{bmatrix} \hat{\mathbf{v}}_{\text{in}} \\ \hat{\mathbf{i}}_o \\ \hat{\mathbf{d}} \end{bmatrix} \quad (17.32)$$

A control block diagram can be drawn based on Eq. (17.32) and depicted as in Figure 17.4. The block diagram can be used to include different control functions to the dynamic model and to evaluate the effect of cross-coupling dynamics since none of the transfer functions in Eq. (17.31) have been neglected. However, one should be careful when using the model in deriving closed-loop model since some of the transfer matrices are not invertible, that is, there are zeros located at the diagonal.

A reduced-order control block diagram can be constructed by neglecting the cross-coupling transfer functions between d and q -components, that is, $Y_{\text{inqd-o}}$, $Y_{\text{indq-o}}$, $G_{\text{ciqd-o}}$, $G_{\text{cidq-o}}$, and by assuming that the rectifier operates at unity power factor. Thus, the output dynamics depend mainly on the d -components and transfer functions $G_{\text{ioq-o}}$ and $G_{\text{coq-o}}$ can be neglected. The reduced-order open-loop control block diagrams can be depicted as in Figure 17.5.

An example code for solving the transfer functions using MATLAB is given in Figure 17.6 where the “`frd()`” command is used to transform the transfer functions

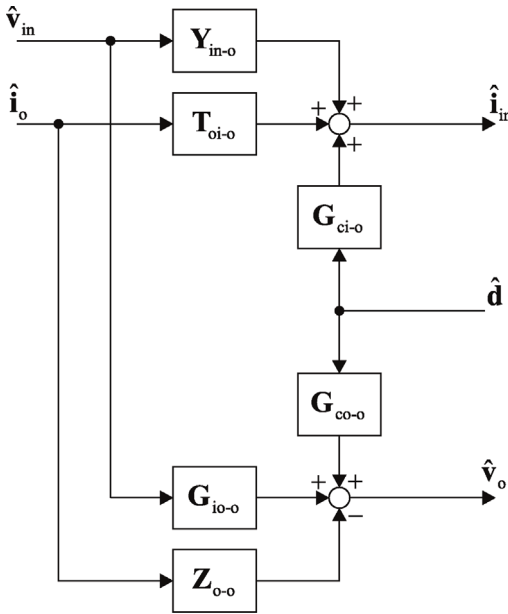


Figure 17.4 Control block diagram of active rectifier drawn using the transfer matrices.

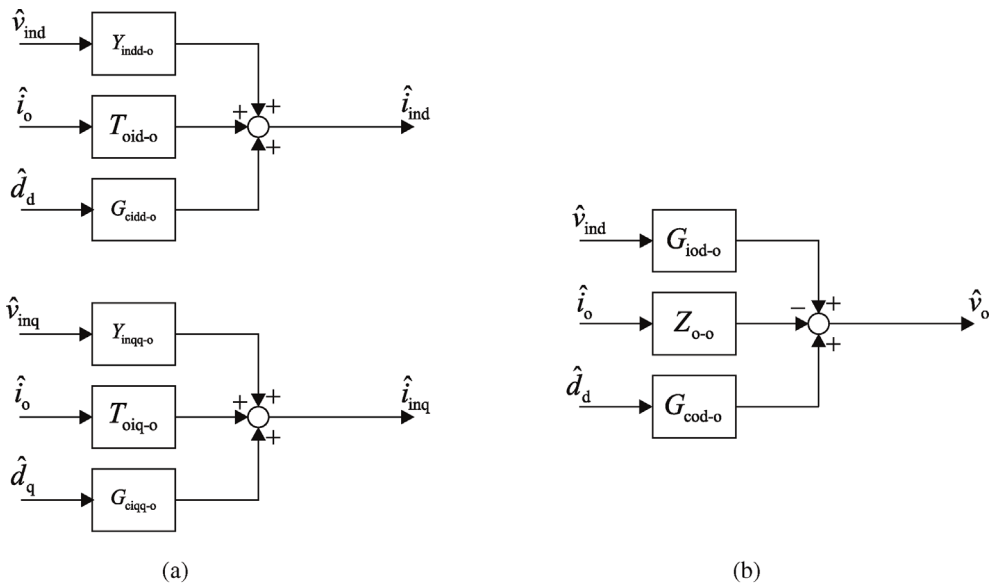


Figure 17.5 Reduced-order (a) input and (b) output dynamics of the active rectifier as a control block diagram.

into frequency-response data vectors. By using this command, all information about the frequencies of poles and zeros are lost. However, analyzing the dynamics as frequency-response data prevents the order of closed-loop transfer functions from getting too high, which may cause problems in solving the closed-loop transfer functions.

```

% Open-loop transfer functions of an active rectifier with L-
type input filter

run parameters %parameters defined in another file
freq_points = 1000; %the number of frequency points
fl = logspace(0, 4, freq_points); %evenly spaced between
                                %1 and 10 kHz
w1 = 2*pi*f; %frequency points in radians

s=tf('s');

A=[-r_eq/L, w_s, -Dd/L;
   -w_s, -r_eq/L, -Dq/L;
   3*Dd/2/C, 3*Dq/2/C, 0];

B=[1/L, 0, 0, -Vc/L, 0;
   0, 1/L, 0, 0, -Vc/L;
   0, 0, -1/C, 3*ILd/2/C, 3*ILq/2/C];

C=[1, 0, 0;
   0, 1, 0;
   0, 0, 1];

D=0;

G=C*inv(s*eye(3)-A)*B+D;

% input dynamics at open-loop
Yind_o = frd(G(1,1),w1); %transfer functions are
"sampled" by frd-function
Yinqd_o = frd(G(1,2),w1);

%...and so one...

```

Figure 17.6 Example *m*-file to solve transfer functions of an active rectifier.

17.3 Verification of Open-Loop Model

The open-loop model was verified by using a switching model implemented using the SimScape package of MATLAB Simulink, which is shown in Figure 17.7. The parameters of the simulation model are given in Table 17.1. The model does not include the PLL as the purpose of this chapter is to present the open-loop model without the effect of any of the control functions. Therefore, it is assumed that the grid voltage is known and it is derived by integrating the grid angular frequency “omega” in Figure 17.7.

The open-loop transfer functions were verified by extracting the corresponding frequency responses from the switching model by using the PRBS injection

Table 17.1 Parameters of the simulation model.

P_o	2.2 kW	$V_{g(a,b,c)-rms}$	230 V	L	8.1 mH
V_o	700 V	ω_s	$2\pi \cdot 50$ rad/s	$r_L + r_{sw}$	100 m Ω
I_o	3.14 A	I_{Lq}	0 A	C	1.5 mF
		I_{Ld}	4.52 A	f_{sw}	10 kHz

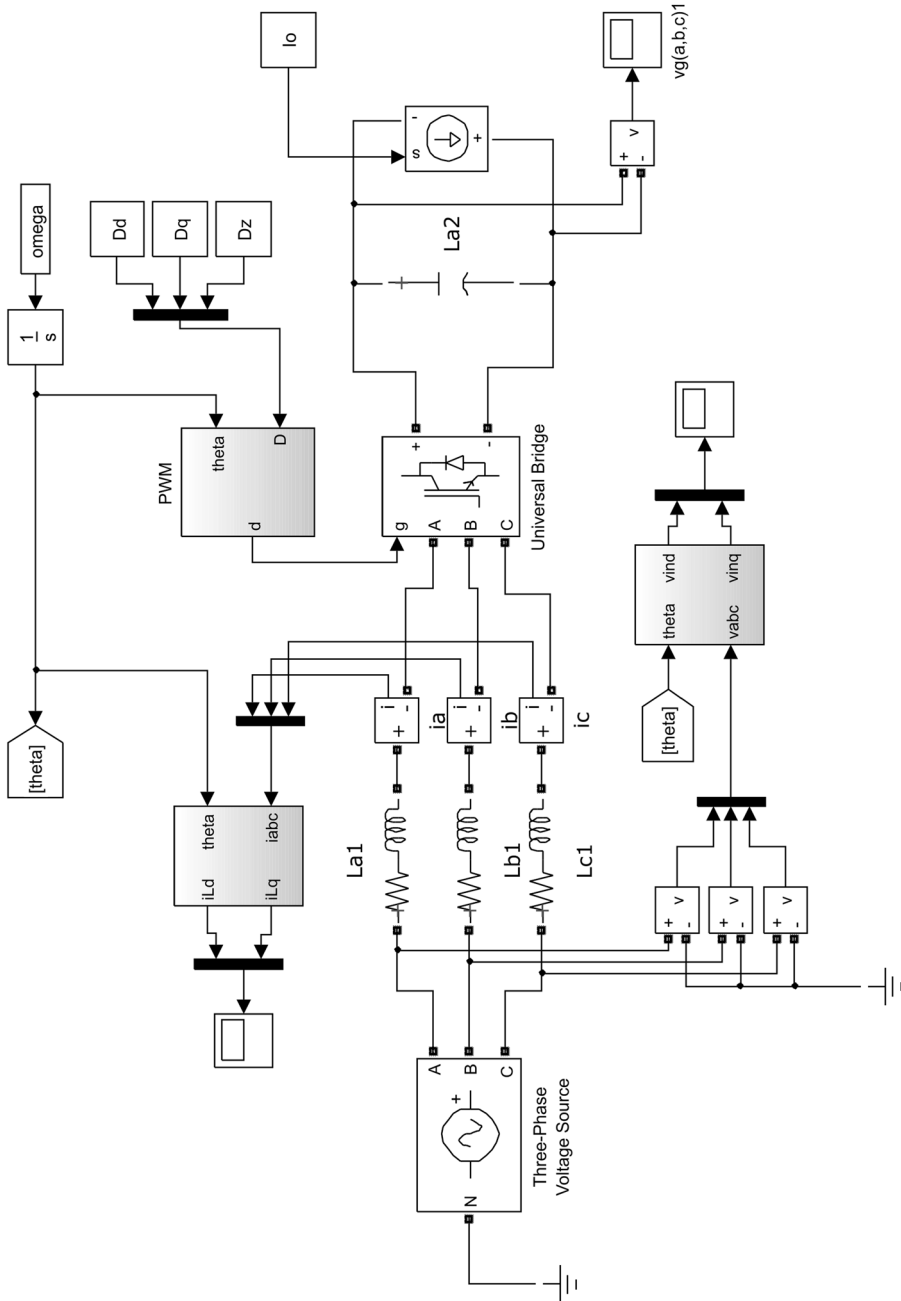


Figure 17.7 Simulink (SimScape) model of an active rectifier.

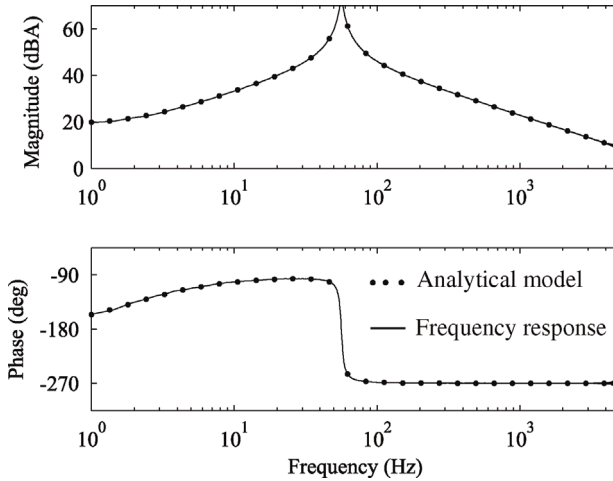


Figure 17.8 Control-to-input transfer function, $G_{cid-d-o}$.

method. As an example, the transfer function from duty ratio d -component d_d to input current d -component i_{ind} can be obtained by perturbing the steady-state value of the duty ratio D_d and extracting the corresponding frequency response. The transfer function G_{cid-o} describes the small-signal dependency of duty ratio d -component to input current d -component and is as shown in Figure 17.8. The low-frequency phase of the frequency response starts from -180° , which indicates that inverted control signal should be used when input current is controlled using conventional feedback control. Moreover, the developed small-signal model gives an accurate prediction on the shape of the transfer function.

Figure 17.9 shows the output impedance of the active rectifier at open loop. The impedance is mostly capacitive due to large DC capacitor as one would expect.

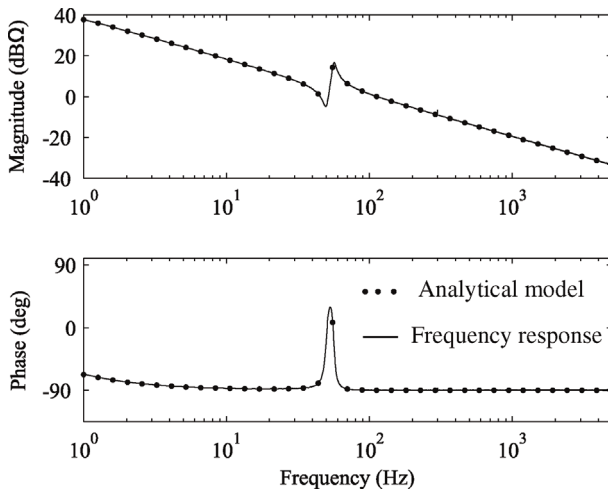


Figure 17.9 Rectifier output impedance Z_{o-o} at open loop.

However, the rectifier is usually controlled using a cascaded control scheme that affects the shape of the output impedance. Open-loop transfer functions provide a good starting point for control design. However, it is also useful to analyze the closed-loop transfer functions, such as closed-loop input admittance and output impedance, because they can be used to determine the impedance-based stability of the rectifier [8] and for designing stable input filters [9].

17.4 Experimental Results

Active rectifier is often controlled using a cascaded control scheme according to Figure 17.10 where the DC voltage controller G_{PI-v} sets the reference value of input current d -component i_{ind}^* . The input current q -component is kept at zero amperes to operate the rectifier at unity power factor. Thus, the reference of input current q -component i_{inq}^* is zero. The current control loops are designed first followed by the design of the outer voltage control loop. The control design of PLL, current control loops, and cascaded control loops follows exactly the same principle as in the case of current-fed inverters in Chapter 13.

Designing stable controllers for the active rectifier acts as a perfect homework for someone who wants to learn how to utilize the dynamic modeling method. Therefore, the procedure is not shown here. However, the suggested design steps can be given as follows:

- 1) Solving the open-loop transfer functions.
- 2) Drawing the required control block diagrams.
- 3) Identifying the loop gains related to PLL, AC current control, and cascaded control.
- 4) Selecting PI controller parameters using the loop-shaping technique.
- 5) Verifying the rectifier stability by step tests.

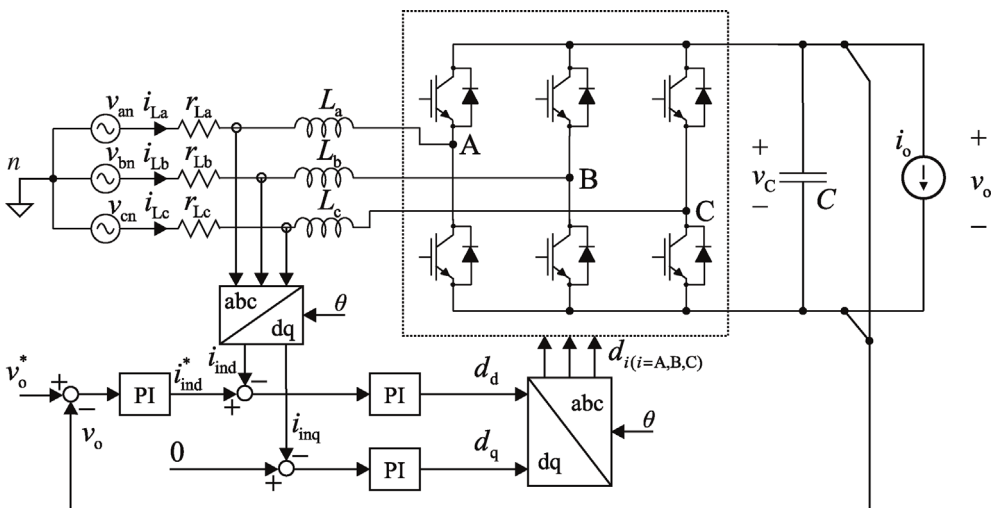


Figure 17.10 Control scheme of an active rectifier.

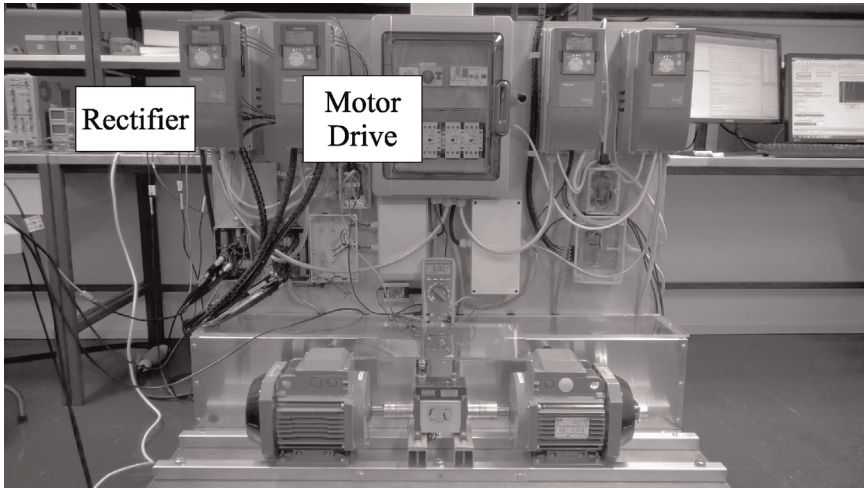


Figure 17.11 Laboratory setup used on a power electronic course.

Control design of the active rectifier is quite straightforward since the control dynamics do not contain any RHP poles or zeros. However, it should be noted that this is not true when the rectifier operates in regenerative operating mode as pointed out in Ref. [6].

Figure 17.11 shows a photograph of a motor test bench at the Laboratory of Electrical Energy Engineering at Tampere University of Technology, Tampere, Finland. The test bench is used to verify the control performance of control systems in a M.Sc. level course, where dynamic modeling of three-phase converters is taught. The active rectifier is located at the left-hand side of the test bench. The rectifier is loaded by a motor drive that rotates the left-hand side induction machine. The right-hand side induction machine is used to produce load torque. The rectifier and motor drive are both controlled by using the dSPACE real-time simulator that can be used to implement controllers designed by students. The converters on the right-hand side control the load motor and utilize their own controllers.

Figure 17.12 shows the DC voltage and grid current waveform when DC voltage is stepped from 600 to 700 V. The rise time is ramp-rate limited inside dSPACE. Settling time of the DC voltage is less than 20 ms. However, the grid current contains excessive harmonics due to dead-time effect. It should be noted that the converters were operated at partial load. Therefore, the relative amount of harmonics in grid current is very large. The rated power of induction machines is 2.2 kW, whereas the rated power of the rectifier is 10 kW.

The crossover frequency of DC voltage loop gain was modified to improve quality of grid current. The measured original and redesigned control loop gains are shown in Figure 17.13. The loop gains were measured using a frequency response analyzer. The goal was to reduce the loop gain magnitude at the frequencies where the DC voltage contains distortion due to dead-time effect. A low-bandwidth DC voltage control can somewhat mitigate the effect of dead-time, as discussed in Chapter 13. The loop gain was measured under no-load

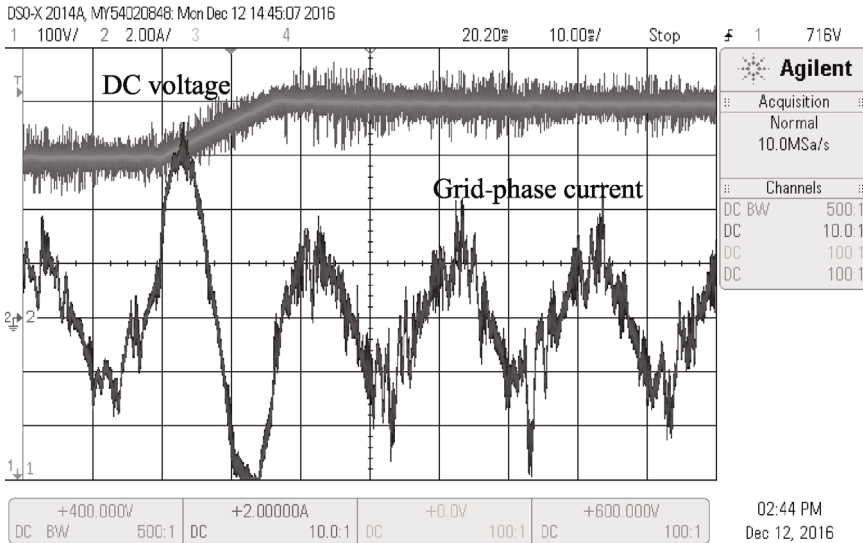


Figure 17.12 Rectifier waveforms with fast DC voltage control.

condition, that is, the motor drive was not drawing any current from the DC link. Therefore, the low-frequency phase starts from -180° and not from -90° as under loaded condition. However, the crossover frequency and phase margin are the same under no-load and loaded conditions.

Figure 17.14 shows the DC voltage and grid current during a DC voltage step test from 600 to 700 V. The settling time is slightly longer due to lower crossover of the DC voltage control loop. The DC voltage settles around the new steady-state value in approximately 90 ms, which is almost four times longer than in the previous test. However, the grid current has much cleaner waveform since the reference of output current contains less harmonics.

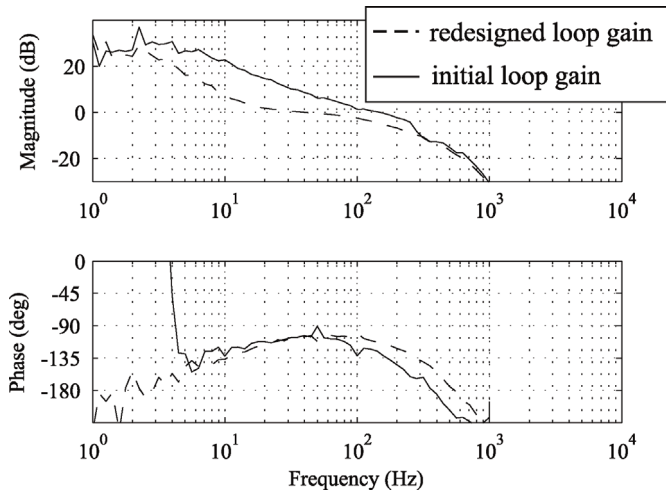


Figure 17.13 Measured DC voltage control loop gains.

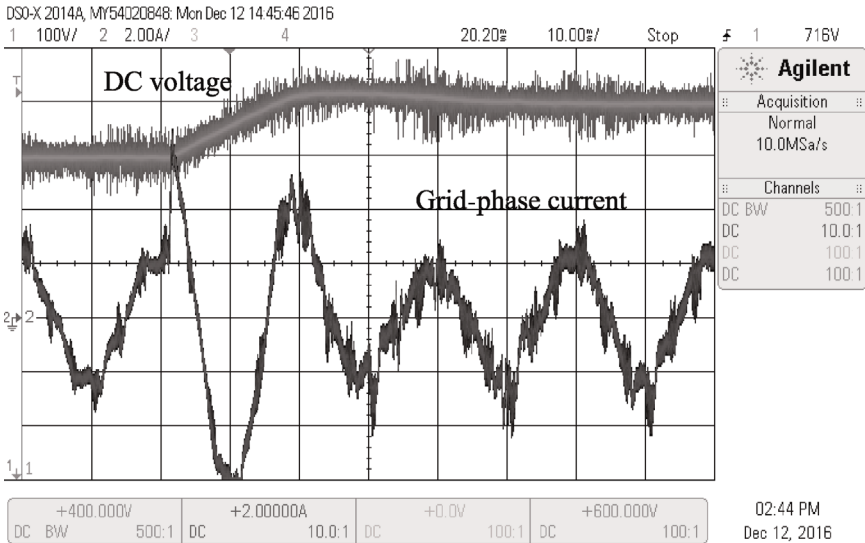


Figure 17.14 Rectifier waveforms with slow DC voltage control.

Figure 17.15 shows the DC voltage and grid current waveforms when the initial control design and a first-order low-pass filter were used to filter out the distortion in DC voltage. The figure shows the turn-on transient of the rectifier after which the overvoltage protection circuit reacts and disconnects the rectifier. The low-pass filter reduces both the magnitude and the phase of the loop gain. Therefore, the phase margin of the loop gain is reduced. The designed loop gain is stable when analyzed in the frequency domain. However, the DC voltage increases

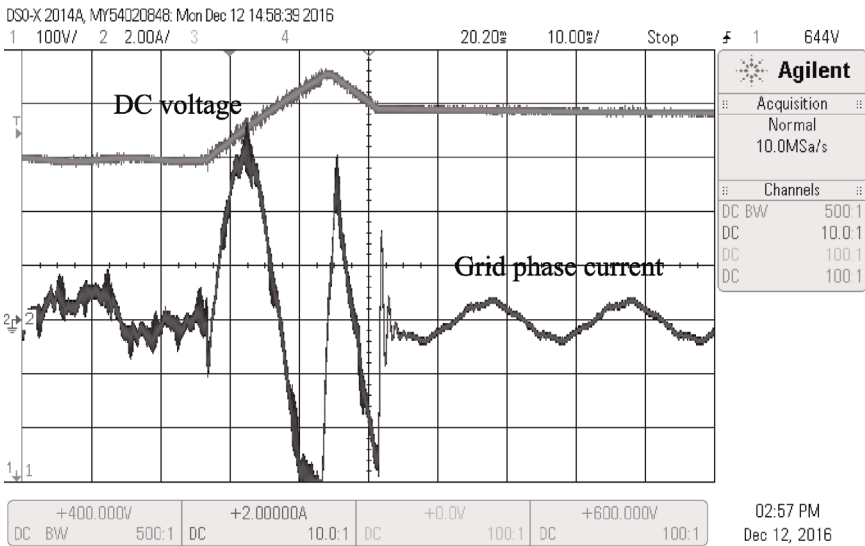


Figure 17.15 Turn-on failure due to poor phase margin in DC voltage control loop gain.

beyond the DC voltage protection limit that was set to 750 V due to inadequate phase margin. Therefore, the rectifier cannot be turned on.

17.5 Summary

This chapter briefly discusses how to obtain the dynamic model of an active rectifier at open loop. Control design of an active rectifier serves as a perfect homework or group work assignment when this book is used as a textbook on a university-level course. Therefore, the rest of the analyses, that is, control design and closed-loop models, are not discussed in this book. Moreover, an active rectifier serves as a perfect topic for a laboratory assignment since one does not have to purchase expensive source and grid emulators.

References

- 1 Harnefors, L., Bongiorno, M., and Lundberg, S. (2007) Stability analysis of converter-grid interaction using the converter input admittance. 2007 European Conference on Power Electronics and Applications, pp. 1–10.
- 2 Harnefors, L., Bongiorno, M., and Lundberg, S. (2007) Input-admittance calculation and shaping for controlled voltage-source converters. *IEEE Trans. Ind. Electron.*, **54** (6), 3323–3334.
- 3 Wen, B., Boroyevich, D., Mattavelli, P., Shen, Z., and Burgos, R. (2013) Influence of phase-locked loop on input admittance of three-phase voltage-source converters. 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 897–904.
- 4 Wen, B., Boroyevich, D., Burgos, R., Mattavelli, P., and Shen, Z. (2015) Small-signal stability analysis of three-phase AC systems in the presence of constant power loads based on measured d–q frame impedances. *IEEE Trans. Power Electron.*, **30** (10), 5952–5963.
- 5 Liserre, M., Blaabjerg, F., and Hansen, S. (2005) Design and control of an LCL-filter-based three-phase active rectifier. *IEEE Trans. Ind. Appl.*, **41** (5), 1281–1291.
- 6 Espinoza, J.R., Joos, G., Perez, M., and Moran, T.L.A. (2000) Stability issues in three-phase PWM current/voltage source rectifiers in the regeneration mode. Proceedings of the 2000 IEEE International Symposium on Industrial Electronics (Cat. No.00TH8543), vol. 2, pp. 453–458.
- 7 Radwan, A.A.A. and Mohamed, Y.A.-R.I. (2013) Analysis and active-impedance-based stabilization of voltage-source-rectifier loads in grid-connected and isolated microgrid applications. *IEEE Trans. Sustain. Energy*, **4** (3), 563–576.
- 8 Wen, B., Boroyevich, D., Mattavelli, P., Shen, Z., and Burgos, R. (2012) Experimental verification of the generalized Nyquist stability criterion for balanced three-phase AC systems in the presence of constant power loads. 2012 IEEE Energy Conversion Congress and Exposition (ECCE), No. 1, pp. 3926–3933.
- 9 Hiti, S., Vlatkovic, V., Borojevic, D., and Lee, F.C.Y. (1994) A new control algorithm for three-phase PWM buck rectifier with input displacement factor compensation. *IEEE Trans. Power Electron.*, **9** (2), 173–180.

Index

a

AC current control
 control loop gains 549
 decoupling gains 559
 active damping 525, 559, 659
 admittance matrix 54, 636, 637, 645,
 653, 655
 amplitude invariance 68
 average-current-mode control
 current-loop amplifier 225
 duty-ratio generation 224–226
 averaged state space 7, 60, 63, 71, 73,
 129, 143, 146, 149, 153, 164, 165,
 167, 170, 233, 234, 279, 287, 362,
 363, 367, 372, 380
 average modeling 57, 60, 142

b

Bode plot 86–88, 90, 91, 312, 316, 322,
 326, 327, 471–473, 477, 479
 boost converter 6, 134, 136, 146, 148,
 149, 167, 199, 201, 206, 211, 213,
 215, 222, 238, 258, 321, 325, 345,
 346, 365, 366, 397, 439, 447, 479
 power-stage 351, 352, 383, 387, 390,
 397, 398, 410, 439, 440, 446, 447,
 451, 457
 boundary conduction mode (BCM) 58,
 157
 buck–boost converter 136, 138, 139,
 149, 151, 170, 199, 202, 206, 207,
 213, 215, 222, 227, 239, 249, 347,
 368, 369, 372, 387, 469
 power-stage 352, 387

buck converter 3, 6, 7, 14, 15, 19, 61, 64,
 97, 126, 127, 131–133, 135, 137,
 140, 142–144, 164, 176–181, 191,
 197–202, 205, 209–211, 213, 215,
 222, 225, 230, 239–242, 244–248,
 251, 253, 254, 269, 272, 274, 279,
 280, 282, 287–289, 291–293, 298,
 301, 307, 308, 312, 315, 330, 345,
 346, 348, 358, 365, 414, 417, 476
 power-stage 351, 377, 380, 386, 387,
 390, 397–399, 405, 406, 410, 411,
 413

c

CLCL filter 112, 115
 complementary sensitivity function 27,
 84, 92
 continuous conduction mode
 (CCM) 57
 control bandwidth
 crossover frequency 92
 RHP pole limitation 102
 RHP zero limitation 86, 163
 control block diagram
 generalized MIMO cascaded
 control 365
 generalized MIMO closed loop 48,
 452
 generalized MIMO impedance-based
 stability assessment 394
 generalized MIMO load
 interaction 391
 generalized MIMO source
 interactions 390

- control block diagram (*Continued*)
 - generalized SISO cascaded control 33
 - generalized SISO closed loop 178
 - generalized SISO impedance-based stability assessment 12
 - generalized SISO load interaction 38
 - generalized SISO source interactions 173
 - control delay, Padé approximation 108
 - control design
 - AC-current control 493
 - coupled-inductor superbuck 64, 474
 - DC-voltage control 493
 - DDR boost converter 213, 215, 321
 - DDR buck converter 174
 - discrete-inductor superbuck 331
 - PCM boost converter 258, 315, 325
 - PCM buck converter 178, 247
 - phase-locked loop 591
 - controller implementations
 - I controller 106, 108, 449, 451
 - P controller 106
 - PI controller 107, 226, 227, 271, 534
 - PID controller 105, 271, 295, 449
 - coupled inductor 19, 64, 65, 157, 160, 205, 219, 221, 330, 332, 475
 - cross-couplings 45, 549, 557–560, 622, 664, 665, 683
 - crossover frequency
 - gain margin 13, 325
 - phase margin 447, 457, 555, 556, 571, 576
 - RHP pole limitation 89
 - RHP zero limitation 325, 326
 - current-fed converter
 - boost converter 345
 - buck-boost converter 347
 - buck converter 342
 - current-fed inverter 515
 - non-inverting buck-boost converter 149
 - quadratic buck converter 348
 - sepic converter 347
 - superbuck converter 372
 - current-mode control
 - average-current-mode control 225
 - peak-current-mode control 190
 - self-oscillation control 125, 231
- d**
- damping ratio, phase-locked loop 543
 - d-channel 550, 603, 644, 645
 - DC UPS, 36, 266, 278
 - DC-voltage control 493, 507, 514, 520, 533, 549, 563, 598, 606, 639, 640, 645, 646, 656, 669, 692–694
 - decoupling gains 497, 533, 549, 559, 561, 562, 633, 634, 644–646, 649, 664
 - differential power processing 468, 469
 - direct component 423
 - direct-duty-ratio 57, 125
 - control 8
 - direct-on-time control 125, 127
 - discontinuous conduction mode (DCM) 7, 57
 - distributed MPP tracking 465
 - dq-domain current control 622
 - duality transformation 6, 9, 20, 341, 342, 358, 377, 485
 - duty ratio 8, 27, 57, 62, 99, 101, 125, 128, 155, 163, 164, 174–176, 189, 190, 192–197, 199, 201–207, 209, 210, 213, 215, 218, 222, 223, 225, 226, 228, 231, 284, 351, 372, 379, 397, 404, 407, 411, 413, 415, 436, 441, 445, 446, 495, 551, 560, 612, 634, 635, 649, 651, 684, 690
 - gain 176, 189, 194, 196, 260, 406
 - dynamics 30, 32, 38, 48, 54, 92, 125, 212, 217, 267, 360, 364, 371, 408, 416, 437, 470, 499, 515, 518, 527, 536, 549, 550, 564, 592, 603, 637, 638, 640, 651, 652, 681, 687
 - capacitance 426, 470
 - modeling 7, 20, 45, 58, 66, 125, 189, 265, 355, 377, 403, 493, 681, 692
 - resistance 426, 429, 446, 470, 474, 518, 519, 523

e

- equivalent circuit
 - canonical equivalent circuit
 - current-fed DC-DC converter 10, 43
 - three-phase AC-DC converter 10
 - three-phase DC-AC converter 10
 - canonical equivalent circuit 8, 11
 - voltage-fed DC-DC converter 9
 - equivalent switching circuit (DC-AC) 508
 - multiport network equivalent circuit (MISO)
 - three-phase voltage-input-current-output converter (Y) 500
 - three-phase voltage-input-voltage-output converter (G) 500
 - multiport network equivalent circuit (SIMO) 87
 - three-phase voltage-input-current-output converter (Y) 622
 - three-phase voltage-input-voltage-output converter (G) 495
 - two-port network equivalent circuit 28
 - current-input-current-output converter 5
 - voltage-input-current-output converter (Y) 189
 - voltage-input-voltage-output converter (G) 268
- error amplifier
 - current-loop amplifier 225
 - I-type 449
 - PID-type 312, 447
 - PI-type 226

f

- feedback
 - complementary sensitivity function 27
 - loop gain 52, 84, 102, 300, 312, 321, 325
 - robustness indices 95
 - sensitivity function 93
- fill factor 433

- fixed-frequency operation 126, 128, 142, 163, 164
- forbidden region 13, 14, 92–95
- frequency response 4, 5, 16, 77, 86, 89, 105–108, 114–117, 226, 227, 249, 258, 259, 397, 450–452, 455–459, 471, 503, 505, 514, 523, 539, 542, 569, 589, 608, 653, 690, 692
 - measurement 583, 598
- full-order model 615, 633, 645, 648, 664
- full-power processing 469

g

- gain-bandwidth product 102
- generalized modeling technique 126, 129
- G parameter 5
- grid-feeding operation 11, 18
- grid-forming operation 18, 50
- grid-parallel operation 17, 50, 53
- grid-supporting operation 509
- grid-voltage feedforward 533, 562, 587, 596, 599, 610, 611, 614, 616, 617, 619, 623, 624, 626, 628, 648, 651, 653, 655, 656, 674, 675

h

- harmonic operation 196, 320

i

- ideal input admittance 174, 237, 242, 305
- ideal input impedance 101, 173, 174, 240, 361, 391, 393
- ideal input-output transfer function 31, 33, 50
- ideal output admittance 392
- ideal output impedance 394
- ideal output-input transfer function 643
- impedance-based stability criterion 667
- impedance shaping 678
- input filter
 - LC filter 95, 112, 349

- input-voltage feedforward 174, 194
 - instability 14, 16, 179
 - interaction
 - load interaction 19, 38, 54, 176, 239, 270, 390, 393
 - source interaction 101, 173, 174, 244, 269, 390, 392
 - inverters 4, 15–18, 47, 50, 111, 351, 432, 435, 465
 - inverting buck-boost 137, 138
 - irradiance 424, 432, 434, 507
 - IV curve 426, 429–432, 434, 468
- j**
- Jacobian matrix 60
- k**
- K value 68, 87, 539
- l**
- LC filter 95, 102, 111, 112, 181, 244, 246, 345, 349, 674
 - LCL filter 111, 113, 525, 528, 648, 653, 655, 656
 - L filter 550
 - linearized model, phase-locked-loop 536, 591
 - load effect 28, 189, 211, 250, 254, 255, 266, 273, 502, 503, 521, 558, 577, 620
 - load-transient response 181
 - loop gain
 - controller 311
 - design constraints 100
 - gain-bandwidth product 102
 - loop shaping 310
- m**
- MATLAB code 500, 501, 526, 528
 - maximum peak criteria (MPC) 94
 - maximum power point (MPP) 4, 395, 579
 - tracking 432, 436, 437, 439, 444, 446, 451, 453
 - mode limit 190, 194, 196, 197, 199, 200, 204, 228, 291, 319
- n**
- model verification
 - inverter output admittance 645, 646, 656, 657, 668, 669
 - inverter output impedance 16, 669, 671, 674
 - open-loop dynamics 499, 510, 527, 681
 - modulator gain 31, 35, 97–99, 128, 129, 321, 325, 551, 587, 616
- o**
- negative incremental resistance 185, 244, 361, 429, 482
 - negative sequence component 544, 545
 - non-inverting buck boost 139, 149, 151, 347, 368, 387
 - Nyquist plot 57, 87–90, 487
 - Nyquist stability criterion 13, 20, 41, 57, 87, 89, 95, 179, 271, 394, 482, 574, 668, 672
- o**
- open-circuit input admittance 270
 - open-circuit input impedance 391, 408, 413
 - open-circuit output admittance 267, 268
 - open-circuit output impedance 177, 215, 217, 221, 241
 - open-circuit voltage 426, 430, 433, 434
 - open-loop control block diagram 503, 686
 - open-loop transfer function 31, 35, 97, 250, 500, 511, 521, 550, 587, 595, 605, 641, 650, 688, 691
 - output-current feedforward 177, 240, 241, 395
 - output filter
 - LC filter 102
 - LCL filter 111
 - L filter 550
 - output impedance 254
 - output-voltage feedforward 394, 447
- p**
- Padé approximation 108, 311, 543, 629
 - passive damping 524, 620, 665

- peak current mode control
 - CCM modeling 244
 - comparator equation 290
 - DCM modeling 222
 - duty-ratio generation 224
 - harmonic operation mode 190
 - mode limit 190
 - peak voltage mode control 403
 - perturb and observe 432, 435
 - perturbation frequency
 - closed-loop converter 244
 - design 437
 - settling time 294
 - phase-locked loop (PLL) 15
 - photovoltaic (PV) cell
 - constant current region 521
 - constant power region 439
 - constant voltage region 521
 - current-voltage curve 517, 522
 - dynamic resistance 435
 - maximum power point (MPP) 521
 - open-circuit voltage 430
 - power-voltage curve 518, 576
 - short circuit current 433
 - photovoltaic (PV) generator
 - MPP tracking 436
 - power dynamics 461
 - stability 465
 - photovoltaic inverter 509, 523, 545, 567, 574, 598, 605, 625, 626, 628, 646, 656
 - PI controllers 106, 107, 226, 227, 278, 534, 538, 548, 590, 642, 691
 - polar plot 86, 87, 89
 - positive sequence component 535, 545
 - power invariance 68
 - pseudo-random binary sequence 249, 504
- q**
- Q-channel 498, 501, 502, 560, 591, 609
 - quadrature component 11, 68
 - quality factor (Q) 113, 146, 149, 153
- r**
- real-time simulator 542, 543, 575, 625, 627, 646, 656, 692
 - rectifier 11, 33, 37, 42, 44, 47, 69, 70, 494, 495, 500, 515, 533, 566, 681, 684, 686, 687, 689–691, 693, 694
 - reduced-order dynamics 633
 - remote sensing 277, 279, 304, 306, 307, 309, 310
 - resonant frequency 81, 102, 112, 113, 181, 304, 312, 321, 322, 326, 361, 368, 395, 447, 524, 553, 657
 - resonant peaking 110
 - RHP pole, control design constraint due to RHP pole 102
 - RHP zero, control design constraint due to RHP zero 102
 - Ridley model 249
 - RMS invariance 68
 - Routh array 85, 87, 88, 159
 - Routh Hurwitz 84–86, 218, 375
- s**
- second-order system estimate
 - damping factor estimate 80, 541
 - feedback-loop crossover
 - frequency 102
 - undamped natural frequency
 - estimate 149, 541
 - settling time 96, 98, 99, 247, 294, 315, 321, 329, 444, 446, 450, 453–456, 459, 534, 541, 571, 692, 693
 - short-circuit current 426, 433, 434, 579
 - short-circuit input admittance 211, 215, 217, 221, 237, 241, 305
 - short-circuit input impedance 15, 242, 243, 246, 306
 - short-circuit output admittance 392, 408, 413
 - short-circuit output impedance 394
 - Simulink average model
 - DRR-controlled buck converter 254
 - PCM-controlled buck converter 253
 - PWM modulator 288
 - Simulink switched model
 - closed-loop converter 285
 - DDR-controlled buck converter 284
 - input filter 285
 - output filter 507, 525

- Simulink switched model (*Continued*)
 - PCM-controlled buck converter 284
 - PWM modulator 284
 - single pole 79, 311
 - single zero 78, 298
 - small-signal modeling
 - average mode 57
 - linearization, Jacobian matrix 60
 - buck converter example 61
 - conduction mode 57
 - coupled-inductor modeling 66
 - three-phase rectifier example 69
 - solar cell 423–427, 429
 - source effect
 - source-affected transfer functions of PV inverter 474
 - stability
 - conditional stability 27
 - generalized Nyquist stability criterion 87
 - instability 305
 - Nyquist criterion 394
 - robustness indices 95
 - Routh array 87
 - Routh Hurwitz 86
 - unconditional stability 27
 - state space 7–9, 59, 60, 63, 65, 73, 74, 76, 126, 130, 132–135, 138–140, 142–145, 147–149, 151, 152, 154, 157, 158, 160, 164, 165, 167, 168, 170, 171, 189, 193, 201, 209, 211–217, 219, 220, 222–224, 232, 234, 235, 279, 287, 288, 355, 360, 361, 363, 367, 370, 374, 378, 380, 384, 385, 388, 406, 411, 415, 418, 419
 - averaging technique 57, 125
 - step response
 - AC current control 493, 559, 606
 - DC voltage control 493, 520
 - phase-locked loop 591, 609
 - synchronous reference frame
 - amplitude invariance 68
 - power invariance 9, 42
 - RMS invariance 68
- t**
- transfer function
 - control-to-input transfer function 375, 472, 479, 480, 690
 - control-to-output transfer function 52, 83, 155, 211, 221, 273, 413, 472, 478–480, 518
 - input admittance 145, 148, 152, 167
 - input impedance 643
 - input-to-output transfer function 637, 643
 - output admittance 392, 637
 - output-to-input transfer function 643
 - second-order transfer function 80
 - single pole 79
 - single zero 298
 - transient performance
 - indices 27, 96
 - load-transient response 95
 - settling time 329
- u**
- unbalanced grid voltages 543, 544, 577
 - underdamped natural frequency
 - phase-locked loop 80
- v**
- variable frequency control 7, 189
 - voltage-fed inverter 111, 493–496, 498, 500, 502–506, 508, 516, 533, 548–553, 560, 563, 567, 587, 588, 591, 595, 596, 602, 610
 - voltage-mode control 125, 231
- y**
- Y-parameters 29, 44, 249, 500
- z**
- Z-parameters 5, 29, 44, 355, 357