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Preface

Nanowires represent the most important group of one-dimensional nanostructures. Due to their special structure-related physical and chemical properties, nanowires have many attractive applications in the field of electronics and optoelectronics. Researches on nanowires developed very fast in the past several years, and the hottest research interests have moved from nanowire synthesis to device applications and system design. It is considered timely to provide a survey of a number of important developments in this field. To this end, *Nanowire Electronics* combines contributions from fabrication and application of nanowires in micro-/nanoelectronics in an attempt to give the readers a feel for the scope of current and potential future developments.

This book contains a selection of 11 chapters contributed by a number of research teams around the world. All the contributors are active researchers in their field of specialization, and thus this book provides an up-to-date survey of the state of nanowire electronics. Although the book is not intended to be comprehensive, specific research topics are selected that reflects the most important possibilities offered by nanowires, including nanowire transistors, nanowire sensors, nanowire generators, nanowire lasers, etc.

In the edition of this book I am indebted to Prof. Di Chen at University of Science and Technology Beijing and Prof. Kai Jiang at Chinese PLA General Hospital for their great supports. I am also extremely grateful to the authors for their excellent contributions. I hope that this book will be a source of inspiration for many graduate students and researchers and stimulate new developments in this challenging field of science and technology.

Beijing, China
2018

Guozhen Shen

Contents

Chapter 1
X-Ray Spectroscopic Analysis of Electronic Properties of One-Dimensional Nanostructured Materials

Han-Wei Chang, Chi Liang Chen, Sofia Ya Hsuan Liou, and Chung-Li Dong

1.1 Introduction

Recent studies of the control of the shape and size of nanomaterials have enabled researchers to explore the development of energy storage and conversion applications in unprecedented detail. Nanomaterials can be exploited into green energy strategies if their surface architectures can be controlled by various treatment processes. Their remarkable behaviors arise in part from their small size, large surface area, and quantum confinement. Nanomaterial science has various implications for environmental science and sustainability. Physical and chemical routes for controlling morphologies, crystal structures, and physical and chemical properties can be exploited to improve performance, expand the function, and extend lifetime of devices with energy storage and conversion applications. Such devices that involve nanomaterials include storage and conversion devices (energy storage, hydrogen generation, water-splitting and dye-sensitized solar cells (DSSC)), optical and electronic devices (semiconductors, photoelectrocatalytic, and waveguides), and environmental devices (sensors and adsorption/separation), among others. Such applications typically rely on emerging electrode designs, which support the realization of energy storage and conversion devices, whose manufacture can be done more efficiently by nanotechnology. The unique features of nanomaterials have been proved to be useful in the development of energy storage and conversion

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applications owing to their effects on the electronic and atomic properties of the surrounding regions, which are revealed by the relationship between the electronic structure and the local atomic environment. Among all energy storage and conversion devices, water-splitting and supercapacitor devices have attracted substantial attention because of their potential use in industry, as well as the potential capability to solve the problem of global environmental change. Recent investigations have highlighted the effect of nanostructured electrode materials on the physical and chemical properties of energy-relevant materials. This chapter focuses on the atomic and electronic structures of one-dimensional nanostructured materials for water-splitting and supercapacitor devices.

Hydrogen generation by photocatalytic and photoelectrochemical (PEC) water splitting has attracted considerable attention as a means of converting and storing solar energy by the direct production of hydrogen. This green synthetic pathway may provide an effective way to solve the problem of global climate change. One-dimensional (1D) nanostructures (nanotubes, nanowires, and nanorods) recently have stimulated great interest in PEC. They improve the photoconversion efficiency of water-splitting material by optimizing charge transport and the recombination properties owing to their direct electric conduction paths. The improvement of photoconversion efficiency in PEC by the use of 1D nanomaterials has been attributed to the suppression of recombination photogenerated electrons/holes in the designed architecture. The separation of photogenerated electron/hole pairs across the interfaces of a 1D nanostructure easily transferred the interfacial charge transfer and then photoconversion efficiency. Transition metal oxides (α-Fe_2O_3, ZnO, TiO_2, and WO_3) have significant advantages in PEC water splitting. Among transition metal oxides, TiO_2 has excellent characteristics over other water-splitting material because of its favorable bandgap (3.0 eV), abundance in nature, low cost, and environmental friendliness. However, TiO_2 has poor electrical conductivity and rapid recombination rate, which limit its efficiency in PEC water splitting. Therefore, attention has been paid to the morphology- and interface-controlled synthesis of TiO_2, and 1D nanostructures thereof have been developed to overcome its limitations. Arrays of TiO_2 1D nanostructures as a substrate have attracted significant interest owing to their favorable properties for PEC water splitting.

Cho et al. developed a branched TiO_2 nanorod structure that provided a structural support with a large electrode/electrolyte contact area, efficient light trapping, and superior charge carrier transport pathways, providing high photocatalytic activity for PEC water splitting. The obtained 1D single-crystalline branched TiO_2 provides more efficient charge separation and transfer than 0D nanoparticles. A high surface-to-volume ratio and unique 1D single-crystalline TiO_2-based nanomaterials are essential for improving photocatalytic activity [1]. Hwang et al. reported the controlling of the length of TiO_2 nanowires using a hydrothermal method. The length of TiO_2 nanowires is controlled by varying the growth time. Photoconversion efficiency increases significantly with nanowire length owing to increased light absorption. However, the photoconversion efficiency of longer nanowires is relatively lower at shorter wavelengths, owing to poor charge collection. To improve photoconversion efficiency, TiO_2 shells of suitable thicknesses are formed around

TiO_2 nanowires to improve their charge collection efficiency because the epitaxial growth of rutile TiO_2 suppresses surface recombination by effectively passivating charge trapping sites [2]. Wang et al. prepared hydrogen-treated TiO_2 (rutile) nanowires for PEC water splitting, showing that this treatment can significantly influence the photoconversion efficiency of rutile TiO_2 nanowires. Unlike pristine TiO_2 nanowires, hydrogen-treated TiO_2 can facilitate both charge separation and transportation, so they have a greater PEC water-splitting effectiveness. The observed IPCE enhancement in the UV region is caused by the increased donor density of the TiO_2 nanowires as a result of the high density of oxygen vacancies following treatment with hydrogen [3]. In photovoltaic or PEC devices, the wide bandgap of TiO_2 limits its absorption within the ultraviolet light, causing it to have a poor ability to convert solar light to current. Therefore, considerable efforts have been made to improve the visible light absorption of TiO_2, including doping with nonmetal, loading with metal, dye or quantum dot (QD) sensitization, and the construction of hybrid structures [4–7]. Some investigations have reported that QDs have large QD extinction coefficients and generate multiple electron/hole pairs per photon, increasing photoconversion efficiency [8, 9]. Liu and Aydil grew TiO_2 nanorod arrays on transparent FTO substrates, allowing the formation of a double-sided tandem structure model for QD co-sensitization. The QD sensitization of TiO_2 photoelectrodes can be achieved by the deposition of semiconducting materials with narrow energy gaps [10]. Some studies have demonstrated that the double-sided structural design serves as an analog of the tandem structure, providing new opportunities for the design and fabrication of PV and PEC devices [11, 12].

The other focused material in this chapter is supercapacitor. Supercapacitor is a highly attractive energy storage device owing to its high power density, rapid charging and discharging capability, excellent cyclic stability, compactness, and high energy efficiency [13, 14]. Two energy storage mechanisms of supercapacitor – electrochemical double-layer capacitance (EDLC) and pseudocapacitance – commonly operate simultaneously. EDLC is associated with an accumulation of electronic charge at the electrode/electrolyte interface by non-Faradaic processes. Carbon materials with a large surface area are considered to be necessary for fabricating EDLC electrodes. Pseudocapacitance is associated with rapid and reversible surface redox reactions that involve Faradaic processes [15]. Transition metal oxides (RuO_2, IrO_2, NiO, Co_3O_4, MnO_2, etc.) and conducting polymers are promising electrode materials for pseudo-capacitors. Pseudo-capacitor materials have low electrical conductivity that can limit their function as supercapacitor electrodes. Pseudo-capacitor materials are decorated on carbon-based materials to improve electrical conductivity and facilitate electron transport and also enhance capacitance. The most extensively studied pseudo-capacitor material that is used in supercapacitors is MnO_2 because of its low cost, high theoretical specific capacitance ($\sim$1100 F g^{-1}), and low environment [16]. Polymorphs of MnO_2 have been synthesized and tested in a neutral electrolytic solution. The several valence states of Mn ions are responsible for its versatile redox-dependent properties and its wide range of electrochemical applications. Nanostructured hybrid carbon materials whose surfaces are decorated with MnO_2 offer efficient transport pathways that

facilitate the transport of electrolyte ions and so exhibit excellent electrochemical performance as electrode materials in supercapacitors, providing a high energy storage capacity. Carbon materials such as carbon nanotubes (CNT) and graphene have been synthesized together with MnO_2 and used as an electrode material in supercapacitors owing to their large surface areas and high conductivity. Du et al. synthesized MnO_2 nanotubes/CNTs to fabricate asymmetric supercapacitors. CNTs provide fast electron transport channels because of their high electric conductivity, facilitating the rapid transport of electrolyte ions or electrons through the electrode/electrolyte interface, optimizing the pseudocapacitance performance of the MnO_2 [17]. Zhao et al. used a self-controlled redox process to form MnO_2/graphene composites with a high surface area and crystallinity. The process prevents the reaggregation of MnO_2 and so enables the homogeneous dispersion of the MnO_2 within the graphene matrix. MnO_2 tends to interact strongly with graphene, favoring its electrochemical utilization [18]. Jin et al. fabricated composites based on CNT/MnO_2/graphene ternary composite paper by electrochemical deposition. The defects on the walls of CNTs provided nucleation sites for the intercalation of MnO, which formed a core-shell structure. The covering of CNT/MnO_2 composite with patches of graphene prevents the shedding of MnO_2, enhancing its cycling stability [19].

Although water splitting using TiO_2 1D nanostructures and a supercapacitor based on carbon/MnO_2 is very effective for energy generation and storage/conversion, their practical applications are limited due to the lacking of a fundamental understanding to their performance. Among various spectroscopic techniques, element-specific X-ray absorption spectroscopy (XAS) is used herein to identify the changes in the electronic and atomic structures that occur in the interfacial region. XAS involves the transition of electrons from their core levels to the unoccupied electronic states and is useful in evaluating changes in the local chemical environment of a constituent element. To obtain more information on changes in atomic and electronic structures of a nanomaterial at an electrode/electrolyte interface, in situ XAS techniques were used herein to provide fascinating insights into photoelectric conversion and energy storage under operational condition. Ex and in situ XAS techniques are widely used synchronization techniques for determining the fundamental atomic and electronic structures of energy storage and conversion materials and can be used to monitor how the surface and bulk properties of a film at an electrode/electrolyte interface in the various charge states. This information can lead to new advanced applications of energy storage and conversion devices. Recently, numerous groups have examined the changes in the electronic and atomic structures of nanomaterials with energy conversion and storage applications under working conditions using ex and in situ XAS techniques.

Zhao et al. reported that ex situ XAS techniques can elucidate the reaction mechanism of the Fe-Mn binary monosulfide compound, which has been studied for potential use in Li-ion batteries. Ex situ XAS spectra, recorded at the Mn and Fe K-edges, reveal that the reaction of Fe-Mn binary monosulfide compound during the

charge-discharge cycle involves asynchronous processes, consistent with the non-flat voltage charging-discharging curve [20]. Pan et al. used ex situ XAS techniques to elucidate the redox mechanism that occurs in an Mg-$LiMn_2O_4$ battery. They verified that the changes in Mn oxidation states in Mg-$LiMn_2O_4$, as a result of the insertion/deinsertion of cations, are reversible in the charging/discharging process. The above observation indicates that Mg-$LiMn_2O_4$ can facilitate the efficient access of ions from electrolyte with the reversible redox reaction between Mn (IV) and Mn(III) [21]. However, some investigations have reported that the extreme air sensitivity of these materials makes analysis of the behavior under working conditions using ex situ XAS techniques impossible because of rapid oxidation in the ambient environment [22]. Xu et al. reported that the use of ex situ XAS to detect Ti^{3+} reduction during lithiation may be difficult owing to its extreme sensitivity to the ambient environment. Therefore, ex situ XAS techniques cannot be used in every experiment to provide the required detailed information: some experiments require in situ monitoring and continuous recording under real operational conditions. Consequently, in situ XAS techniques were used herein to examine the redox mechanism at active redox couple between Ti^{3+} and Ti^{4+} under working conditions. The results demonstrated that in situ XAS techniques are suitable for continuous monitoring and can provide considerable information on changes in the electronic and atomic structures under working conditions.

Lukatskaya et al. elucidated the energy storage mechanism of titanium carbide using in situ XAS techniques. To prove that the charge storage mechanism of titanium carbide is based on pseudocapacitance, in situ XAS at Ti K-edge was carried out during cycling tests on it. The variation of the main edge energy and the average oxidation state of Ti during the charging/discharging process reveal that for titanium carbide, the charge storage is significantly associated with pseudocapacitance. Therefore, the results obtained therein will aid in the development of a new system for energy storage and conversion [23]. Gorlin et al. investigated the electrocatalytic activity of bifunctional manganese oxide (MnO_x) in the oxygen reduction reaction (ORR) and oxygen evolution reaction (OER) using in situ XAS techniques. Their observation indicated that the primary phase of MnO_x is $Mn_3{}^{II,III,III}O_4$ under ORR conditions and that a mixture of two MnO_x phases dominates under OER conditions. Electrocatalysis under OER conditions occurred throughout the structure of MnO_x, indicating that the MnO_x films have great porosity. These results reveal that in situ XAS techniques can be used to observe directly the mechanisms of energy storage and conversion [24].

This work focuses on the elucidation of electronic and atomic properties of nanomaterials by synchrotron X-ray spectroscopies [25] in Sect. 1.2. The nanomaterials include nanostructured titania arrays (tubes and rods) [26] in Sect. 1.3 and nanoflaky MnO_2/functionalized carbon nanotubes [27] in Sect. 1.4. New materials are developed, and basic scientific research is conducted to understand the fundamentals that govern the chemical/physical properties of the nanostructured materials.

1.2 Synchrotron X-Ray Spectroscopies

The most important goal in these studies is how can we search for the optimal material be facilitated for efficient energy generation/conversion/storage? For example, a PEC candidate material will be judged by its ability to split water and to produce hydrogen. To reach this goal, however, individual properties of particular materials need to be understood and optimized, and, in particular, fundamental barriers in one or more of the requirements need to be identified. It is thus crucially important to be able to characterize candidate materials with respect to each material requirement individually, that is, independent of the other requirements. It is the purpose of this proposal to utilize X-ray spectroscopic methods which are very powerful tools to do that: to focus on a specific element in the material and to collect information about the fundamental properties of a candidate material that are of direct relevance to the performance in a PEC material. We will focus on two particular factors: the understanding of the electronic structure of the material surface (and its interface with the electrolyte), as well as the chemical structure relevant for chemical stability.

Therefore, based on the need of a PEC material, a detailed knowledge of the energy level of the CBM (VBM) at the surface of the hydrogen (oxygen) electrode is of great importance of the choice and optimization of an electrode material. However, a direct determination of these levels, especially at the surface of the material, is not straightforward. In general, electronic bandgap and band edge positions at the surface of semiconductor compound (and thus also at the interface with the electrolyte) are different from bulk optical gap and band edge position. For a correct description, it is thus necessary to measure band edge position and gaps directly with XAS, XES, and RIXS which are shown in Fig. 1.1.

Overall the aim of this chapter is to determine the electronic structure of energy-related materials so the fundamental physical properties can be well understood. The use of the relevant method enables experiments at the frontier of the knowledge within the scientific topics. In short, the XAS gives an access to probe the unoccupied electronic states above the Fermi level (conduction band). The XES, however, gives the information of occupied electronic states below the Fermi level (valence band). One can obtain the energy gap and overall electronic structure of matters by combination of XAS and XES. On the other hand, RIXS is sensitive to electron-electron interactions and gives access to element-specific excitations of only a few eV that can arise from local (e.g., d-d), nearest neighbor (e.g., charge transfer (CT)), and collective (e.g., phonon) excitations. In the following, the descriptions of these techniques are briefly described.

XAS is one of the most versatile techniques based on synchrotron radiation. X-ray absorption process is due to the excitation of a core electron by an incident X-ray photon. It provides a direct insight into the electronic structure and local environments at an atomic level around the target atoms. Recently XAS techniques are widely applied in characterization of energy-related materials, for instance, the change of charge state upon physical/chemical reaction. The spectrum can be

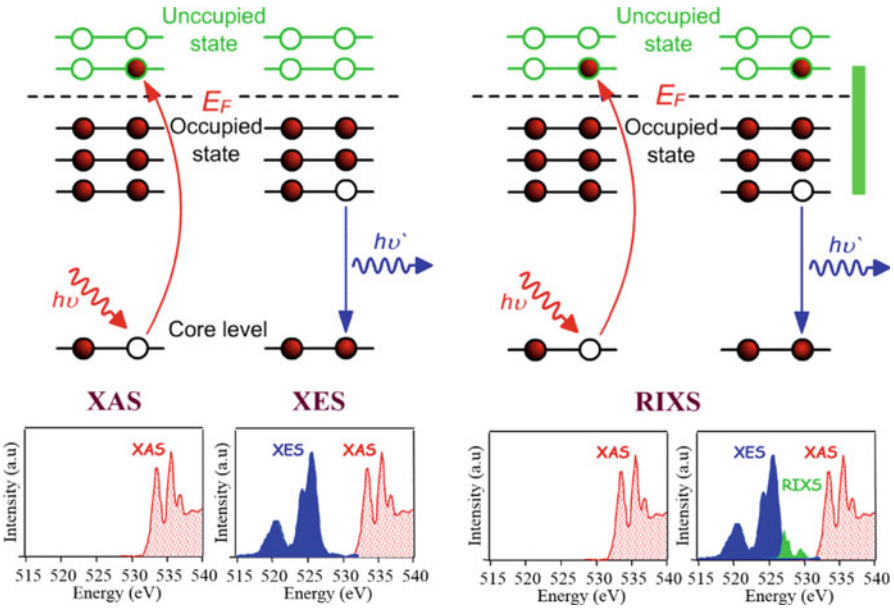

Fig. 1.1 Various synchrotron X-ray spectroscopies: XAS, XES, and RIXS

divided, according to the energy relative to the absorption threshold, into two parts, the near-edge and the extended spectra: X-ray absorption near-edge structure (XANES) and extended X-ray absorption fine structure (EXAFS). XANES mainly provides element-specific information of the electronic and local structure. The photoelectron in this region can be scattered between atoms at larger distances and scattered many times (multiple scattering), providing the information about symmetries and chemical state. The formal valence of the absorbing atom, the degree of hybridization with its neighbors, and the local atomic arrangements can be deduced from these spectra. EXAFS is the absorption spectrum beyond the XANES region. This is an element-specific structural characterization tool. Since the mean free path of the photoelectron is small in this region, single scattering events take place, giving the structural information. Thus, EXAFS provides the information of local environment around the absorbing atom including the type of the neighboring atoms, coordination number, bond lengths, and the Debye-Waller factor.

The basic concept of XES can be illustrated as a core electron is excited by absorption of an incident X-ray photon and creates a core vacancy which is known as XAS process. In turn, this excited state decays via recombination process. That is, a valence electron will fall down to fill the core hole and then emit an X-ray photon. This decay process by emitting a photon can be recorded by XES and is analogous to the absorption process. The energy of the emitted photon is the energy difference between the involved electronic levels. The analysis of the energy dependence of the emitted photons is the aim of the X-ray emission spectroscopy. Briefly, XAS gives the information of the local partial density of states of the unoccupied states, whereas

XES reflects the local partial density of occupied states. Generally, if the core electron is resonantly excited to the vicinity of absorption threshold by the incident photon, the emission spectrum strongly depends on the incident photon energy. This XES process is consequently called resonant X-ray emission spectroscopy. The more complicated situation arises when the incident photon energy hυ is not equal to the emitted photon energy hυ` (h$\upsilon \neq$ h$\upsilon$`). In this situation, so-called RIXS, a photon is inelastically scattered from a bound electron; thus, the atom ends up in an excited state. Since RIXS involves specific core levels, it has elemental selectivity. It also has the same dipole selection rules as X-ray absorption. In RIXS, the dipole approximation will be $\Delta l = 0$, or ± 2, rather than $\Delta l = \pm 1$, because the dipole transition interferes twice. This is quite interesting since it opens up new possibility to the research of low-energy excited state, such as d-d, f-f, and CT excitations. The recent successful development of in situ technique for synchrotron X-ray spectroscopy opens a door to explore the atomic and electronic structure of an energy material under its real working condition.

1.3 Nanostructured Titania Arrays

Nanostructured titania (TiO_2) with unique optical and electronic properties can confine light beyond the diffraction limit of size and quantum effect owing to the excitation of free electron oscillations at their large surfaces. This section concerns highly ordered arrays of 1D TiO_2 nanostructures: Sect. 1.3.1 concerns nanotube arrays and Sect. 1.3.2 concerns double-sided nanorod arrays. The interface and the interior of a nanotube/nanorod array are believed to be critical in the design of photoelectrocatalytic water splitting, improving their light-harvesting ability.

1.3.1 Freestanding TiO_2 Nanotube Array

The growth of highly ordered arrays of TiO_2 1D nanostructures has attracted significant interest owing to the impressive properties of such arrays in the photocatalytic degradation of pollutants [28–30], the generation of hydrogen by the photoelectrocatalytic splitting of water [31–33], dye-sensitized solar cells [34, 35], and gas sensors [30]. In 1999, Zwilling et al. became the first to report on the growth of highly ordered TiO_2 nanotubes (TiNT) with lengths of a few hundred nanometers by the electrochemical anodization of Ti foil in aqueous hydrofluoric acid [36]. The electrochemical conditions during titanium anodization in nonaqueous organic electrolytes have been tuned to grow TiO_2 1D nanostructures of up to hundreds of micrometers in length and to control their shapes [34].

Several methods of detachment have been used to cause TiO_2 nanotube film to flake off an underlying Ti substrate. Such methods include ultrasonic agitation [37], methanol evaporation [38], selective dissolution in various solvents [39], and a self-

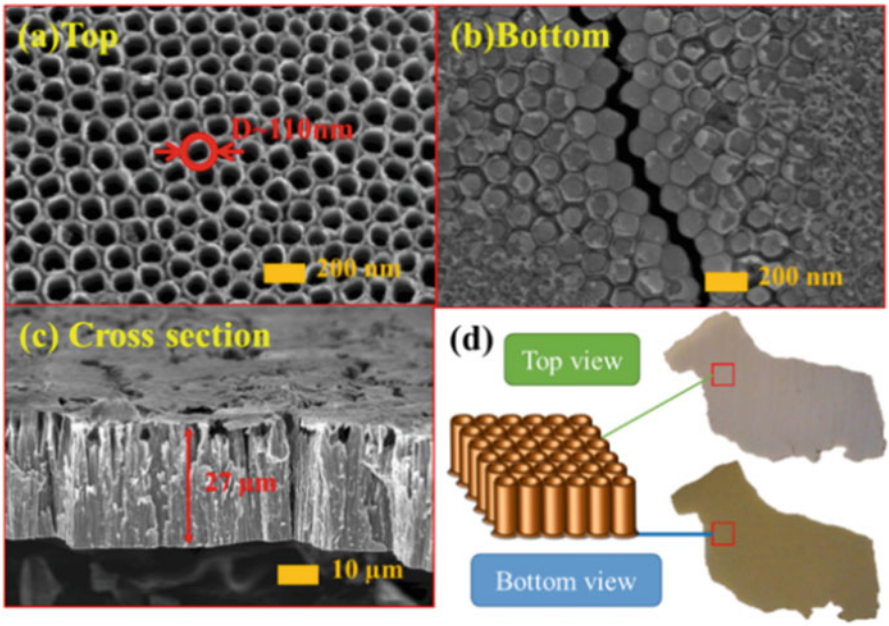

Fig. 1.2 FESEM images; (**a**) top, (**b**) bottom, and (**c**) cross section TiNT film; (**d**) TiNT array and photographic images of top (white) and bottom (yellow) side. (Reproduced from Ref. [25] with permission from the PCCP Owner Societies) (Color figure online)

detaching multistep electrochemical process [40]. The detachment may be induced by the defect structure of TiO_2 nanotubes, the charge state of Ti, or the structural distortion in the region of the metal (Ti foil)-oxide (nanotubes) interface. Freestanding TiNT arrays can be anchored to conductive glass and may exhibit a much wider range of applications and better performance than a nanotube layer on Ti substrate owing to the absence of a blocking layer between the TiNT membrane and the Ti substrate. However, the bottom ends of the tubes are closed. The closed-end interface between the TiNT membrane and the conductive glass may absorb near-UV light, reflect surface light, and block the diffusion of redox regents, reducing photoelectrochemical activity [33]. However, most pertinent investigations have not discussed the transition layers or the electronic and structural properties of the bottom of such tubes. In this section, spectroscopic techniques are used to elucidate the electronic and atomic structural differences between the bottom cap (region between the Ti foil substrate and TiNTs) and the top of highly ordered TiNTs and the cause of the removability of the bottom cap.

Figure 1.2a, b shows the FESEM images of top and bottom sides of the free-standing TiNT film, respectively. The figures display detailed morphologies of the fabricated optically transparent nanotube arrays. The length of each tube is ~27 μm, as revealed by the cross-sectional image in Fig. 1.2c. Figure 1.2d presents a TiNT film and the bottom and top of the film after it was stripped away from the Ti foil.

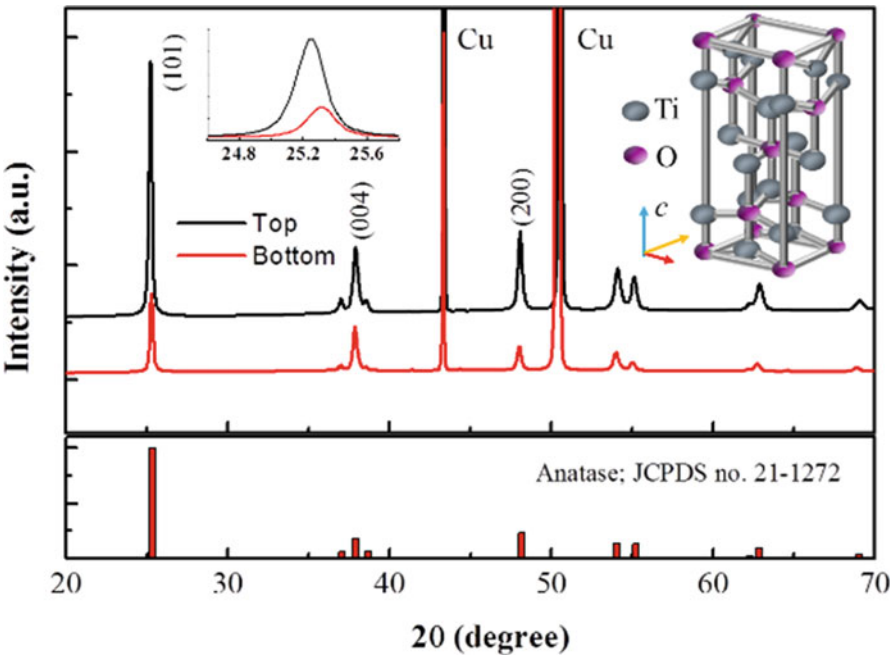

Fig. 1.3 X-ray diffraction patterns of top and bottom of TiNT. All diffraction peaks are indexed to a pure anatase structure. Left inset shows enlarged anatase (101) peak. Right inset shows crystalline structure of anatase TiO_2; gray and purple spheres represent Ti and O ions, respectively.. (Reproduced from Ref. [25] with permission from the PCCP Owner Societies) (Color figure online)

The figure indicates that the bottoms of the tube ends are capped and dark yellow, although pure TiO_2 is white. The top and bottom of the TiO_2 nanotube array consist of mostly the anatase crystal phase, as revealed by the SXRD pattern in Fig. 1.3. The inset in Fig. 1.3 presents the crystal structure of TiO_2, which has the tetragonal space group $I4_1/amd$. The diffraction peak (101) from the bottom of TiNT (at the barrier between the Ti foil and TiNT) has a higher 2θ value than that from the top of TiNT, as presented in the inset in Fig. 1.3. The shift in the (101) peak reflects a decrease in the lattice constant along the c-axis and possible lattice shrinkage along the c-axis at the bottom of TiNT. Additionally, the ratios of the intensities of peak (101) to that of peak (004) and peak (101) to (200) varied significantly between the top and bottom of the TiNT film. According to other investigations, the (101) peak is less intense than the other characteristic peaks because the phase transformation upon annealing either in an oxygen-free environment or at low temperature is incomplete [37, 41]. As depicted in Fig. 1.2d, the color changed from dark yellow at the bottom to gray at the top of the TiNT, consistent with the results of Ghicov et al. [42]. Therefore, defects were formed in the TiO_2 structure by the loss of some of the oxygen, resulting in the formation of oxygen vacancies and Ti^{4+}/Ti^{3+} reduction. Based on these observations, the top and the bottom of the TiNT probably exhibited different

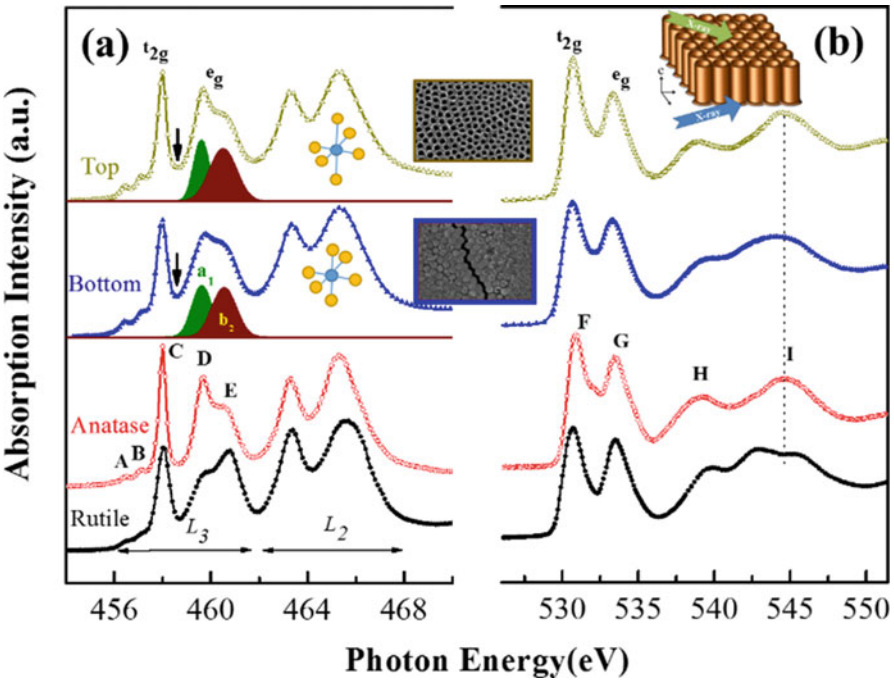

Fig. 1.4 (**a**) Ti $L_{3,2}$-edge ($2p \rightarrow 4p$) and (**b**) O K-edge XANES spectra of top and bottom of TiNT and spectra of TiO_2 anatase and rutile phases. (Reproduced from Ref. [25] with permission from the PCCP Owner Societies)

electronic structures with more of the Ti ($t_{2g}^{\ 0}e_g^{\ 0}$) state at the top and more of the reduced Ti ($t_{2g}^{\ 1}e_g^{\ 0}$) state at the bottom.

Figure 1.4a presents the Ti $L_{3,2}$-edges XAS spectra of the top and bottom of the TiNT. The spectra are determined by excitations of a core electron in the $2p_{1/2}$ or $2p_{3/2}$ orbital to the unoccupied $3d$ state, corresponding to a transition from a ground state $2p^6 3d^n$ to an excited electronic configuration $2p^5 3d^{n+1}$ with different multiplet excitations. On the account of spin-orbit coupling in the $2p$ state, the obtained spectra include two prominent features in the energy ranges 455.6 ~ 461.8 and 462 ~ 469 eV, corresponding to the L_3 ($2p_{3/2} \rightarrow 3d$) and L_2 ($2p_{1/2} \rightarrow 3d$) absorptions, respectively. Five main peaks, A, B, C, D, and E, dominate the spectral evolution of the L_3-edge absorption. In TiO_2, the octahedral symmetry involves a central Ti atom, surrounded by six O atoms (two apical and four base oxygens), and the O_h crystal field splits the $3d$ band in the anatase phase into t_{2g} and e_g [43–45]. The valence states can be obtained from the evolution of the absorption spectra. The ground state of Ti^{4+} is $3d^0$ and absorption peaks that are associated with the $2p^6 3d^0 \rightarrow 2p^5 3d^1$ transition are observed in the L_3-edge absorption spectrum. The sharp resonance C peak that is centered at 458 eV corresponds to the $3d_{t2g}$ final state. The presence of Ti^{3+}, which has one electron in its $3d$ state in the t_{2g} band, may reduce the number of the $3d$ unoccupied states and the intensity of peak C. However, the spectrum of the top resembles that of

the bottom of TiNT, indicating only a small change in intensity. Notably, when the changes in the XAS spectra in the t_{2g} band are small, analyses can involve the spectral deconvolution or RIXS, which can measure the specific electronic state separately [45]. Since the Ti e_g orbitals point directly toward the 2*p* orbitals of the surrounding O atoms (TiO_6), the e_g band is very sensitive to the local environment [46–49]. The e_g-related peak of the L_3 edge is split into two peaks, D (d_z^2, a_1) and E ($d_x^2 - {}_y^2$,b_2). However, the intensity of peak a_1, which is associated with the d_z^2 orbital, is reduced and broadened at the bottom of the TiNT. This change in D/E ratio is caused by noncubic structural distortion and the modulation of the unoccupied electronic state in the e_g band, as depicted in the inset in Fig. 1.4a [46–49]. The oxygen vacancies directly affect the crystal symmetry, Ti-O bond, and O ligand states [49]. Peaks A and B arise from the strong interaction between poorly screened 3*d* electrons and the 2*p* core hole and depend on the structural symmetry [47]. These two peaks are weaker in the spectrum of the bottom of the TiNT by the greater hybridization between Ti 3*d* orbitals and O ligand states and associated solid-state broadening [46]. Figure 1.4b shows the O K-edge XANES of the top and bottom of TiNT. The relatively narrow pre-peak features F and G in the photon energy range 528 ~ 537 eV arise from the transition of electrons from O 1*s* to the unoccupied O 2*p* states that are hybridized with Ti 3*d* states [47, 50]. The spectra of the top and bottom of the TiNT are similar to that of the anatase phase of the reference TiO_2. Moreover, the pre-edge features, F (t_{2g}) and G (e_g), differ slightly between the spectra of the top and bottom of the TiNT. The difference in the t_{2g}/e_g ratio between those spectra suggest mixed valence states of the Ti ions and oxygen vacancies at the bottom. Furthermore, distortion of the TiO_6 crystal symmetry and modification of the *p-d* hybridization states broaden features F, G, H, and I in the spectrum of the bottom of TiNT [47, 50, 51]. The results presented herein indicate the increased incorporation of Ti^{3+} into anatase TiO_2 with the O_h symmetry, and a consequent distortion of the crystal structure, which is related to the dark yellow color in the photographic image of the bottom of the sample in Fig. 1.2d.

Figure 1.5a presents Ti 2*p* RIXS spectra of the top and bottom of TiNT (presented in energy loss scales). The RIXS spectra were obtained using an incident photon energy of 458.6 eV. The first feature at 0 eV corresponds to elastic scattering. The inelastic scattering features in the range 5–10 eV are attributable to complicated charge transfer and excitation from O 2*p* to Ti 3*d* t_{2g} and e_g subbands [52, 53]. Low-energy inelastic scattering features are also observed in the range 0–5 eV; these are absent from the spectrum of pure TiO_2, in which no electron occupies the *d* orbital of Ti^{4+} [46, 54]. The low-energy loss features (0–5 eV) in the spectrum of the bottom of TiNT are associated with Ti^{3+}, whose 3*d* state is occupied by an electron, revealing that the 3*d* t_{2g} orbitals are occupied. The spectrum of the bottom of the TiNT includes an energy loss feature at ~1 eV and is attributed to *d-d* excitation. The intensity of this *d-d* excitation peak in Fig. 1.4a is significant at the particular excitation energy (t_{2g} resonance, 458.6 eV), indicating the strong correlation among the *d*-electrons. Figure 1.5b, c shows the fitted spectra of the top and the bottom of TiNT. Apparently, *d-d* excitation occurs at the bottom of TiNT, and this feature is associated with the electron/hole pairs in the t_{2g} band, as can be understood

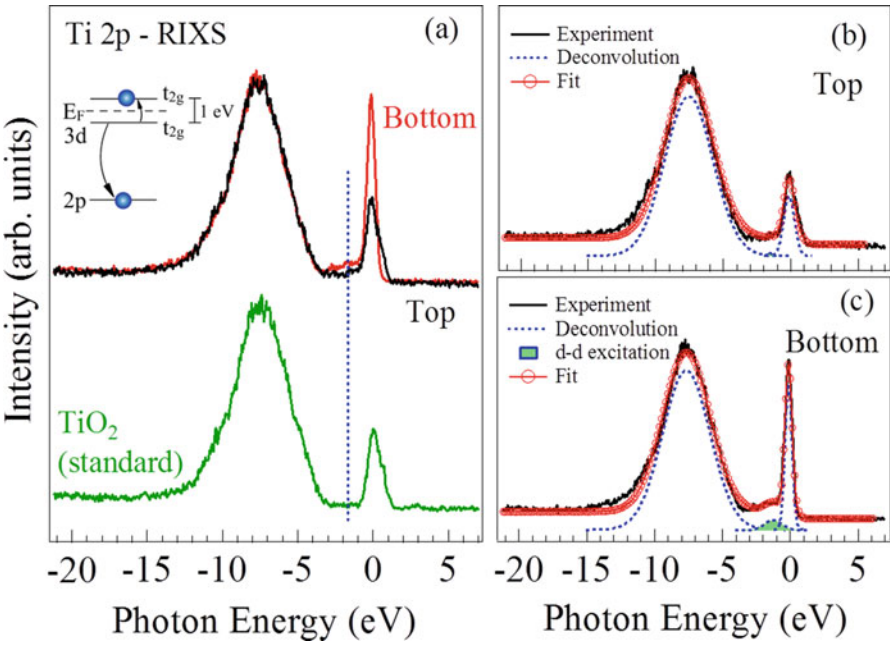

Fig. 1.5 Ti^{3+} t_{2g}-resonance RIXS spectra of (**a**) top and (**b**) bottom of TiNT. Inset in (**b**) presents energy diagram of d-d excitation. (Reproduced from Ref. [25] with permission from the PCCP Owner Societies)

with reference to the Ti^{3+} contributions, which are revealed by the constant initial state (CIS) absorption spectrum [54]. This result reveals the presence of oxygen vacancies at the bottom of TiNT. The energy diagram in the inset in Fig. 1.5a yields the probability of excitation of the t_{2g} electron into the unoccupied t_{2g} states. The appearance of the *d-d* excitation is notable, revealing that the t_{2g} occupation number is changed in the bottom cap, suggesting variations of the Ti valence and the oxygen defects.

Electronic and atomic structures of TiO_2 nanotube arrays were investigated using XAS and RIXS. The analytical results reveal that the electronic structures of the top caps of the TiNT array differ from those of the bottom ones. The mixture of Ti^{3+} and Ti^{4+} valence states is demonstrated in the bottom caps.

The lattice constant along the c-axis drops, and the 3*d* orbital orientations which vary in the bottom caps imply the occurrence of structural distortion and oxygen vacancies. These spectroscopic results afford insights into the fundamental atomic and electronic properties of TiNTs that are fabricated with electrochemical anodization and their potential use of high-performance water-splitting material.

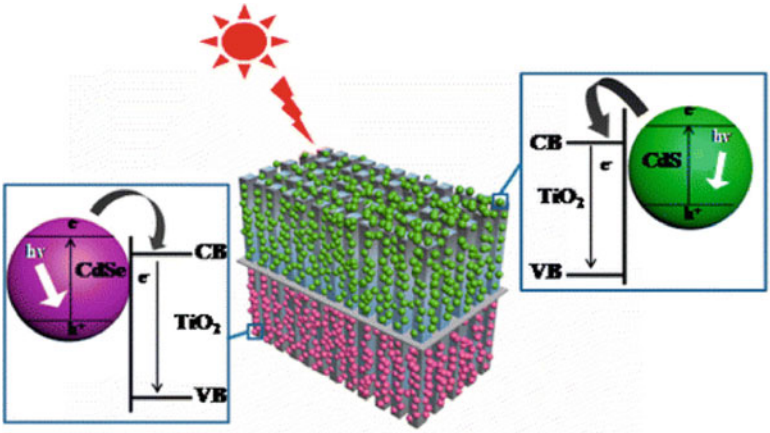

Fig. 1.6 Different bandgaps of photoelectrodes that can be applied to PEC applications. (Reprinted with the permission from Ref. [26]. Copyright 2016 American Chemical Society)

1.3.2 QD Co-sensitized TiO_2 Nanorod Arrays

In this section, X-ray spectroscopy techniques are utilized to reveal the electronic and atomic structures of QD co-sensitized TiO_2 nanorod arrays to elucidate the mechanism of mobile electron charge transfer therein. In situ XAS revealed a defective anatase and rutile phase in QD co-sensitized TiO_2 nanorod array photoelectrodes during electrochemical anodization and nanotube growth. Interfacial charge transfer phenomena (charge migration from TiO_2 to CdS or from TiO_2 to CdSe) are identified using XAS. Given transparent substrates, photoelectrodes with a double-sided tandem structure can be designed. These two QDs were sequentially deposited on TiO_2 to form a co-sensitized tandem structure, which is depicted in Fig. 1.6. The co-sensitized double-sided structure exhibited greater photocatalytic ability than a single or co-sensitized one-sided photoelectrode. The double-sided CdS and CdSe co-sensitized 1D TiO_2 photoelectrode for PEC hydrogen generation substantially improved the efficiency and provided a simple means of simultaneously improving visible light absorption and charge transport.

Figure 1.7a, b presents the FESEM images of TiO_2 nanorod arrays. The top view (Fig. 1.7a) indicates that the entire surface of the FTO substrate was covered uniformly and densely with TiO_2 nanorod arrays. The TiO_2 nanorod arrays were relatively smooth and almost perpendicular to the FTO substrate, as depicted in Fig. 1.7b. The mean length and diameter of the TiO_2 nanorods were ~2.1 μm and 120 nm, respectively. The TiO_2 nanorod arrays were sequentially sensitized using CdS or CdSe by successive ionic layer adsorption and reaction (SILAR) processes. Figure 1.7c, d displays side images of TiO_2 nanorod arrays that were coated with

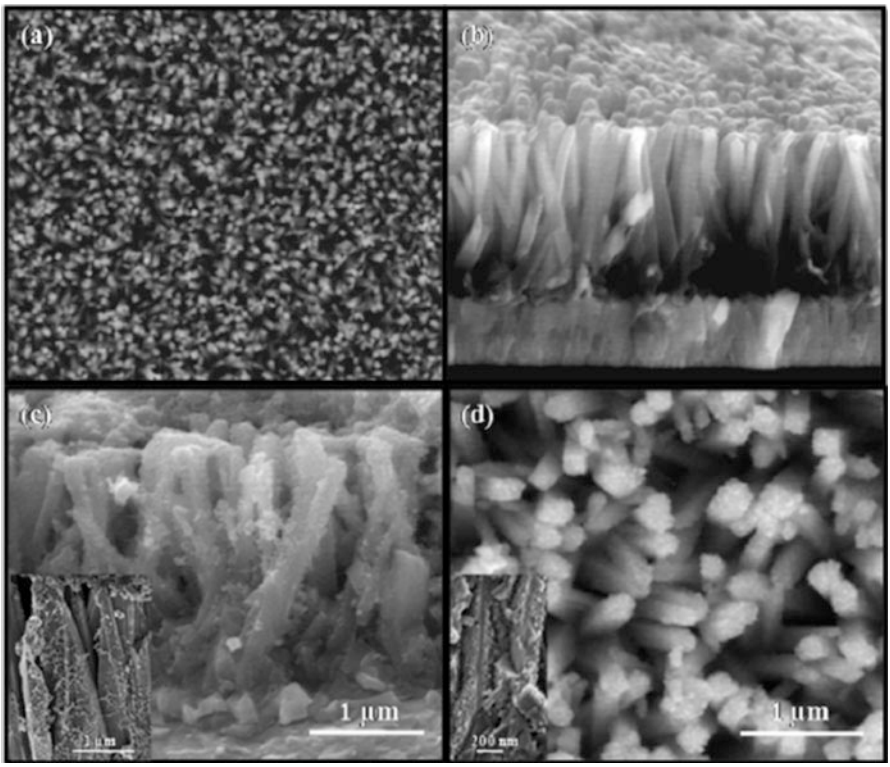

Fig. 1.7 FESEM images of (**a**) top and (**b**) side of TiO_2 nanorod arrays. (**c**) Top and (**d**) side views of CdS and CdSe coated with TiO_2. Insets show magnified images. (Reprinted with the permission from Ref. [26]. Copyright 2016 American Chemical Society)

CdS and CdSe. Nanoparticles of uniform size were observed with the nanorod in the inset, revealing that CdS and CdSe were successfully deposited.

Figure 1.8a shows linear-sweep voltammograms (LSV) under solar light illumination, within the potential range of -1.2 to -0.2 V vs. a reversible hydrogen electrode (RHE). Clearly, all QD-sensitized TiO_2 photoelectrodes exhibited an enhanced photocurrent because QD effectively absorbed the visible light. These two co-sensitized one-sided electrodes yielded similar photocurrent densities but were less efficient than the single QD-sensitized TiO_2. Given the same number of SILAR cycles, excess QD deposition, which prevented the penetration of light, was excluded as a factor in the reduction of photocurrent density. The QD-co-sensitized TiO_2 electrode provided a greater photocurrent density than that of the pristine TiO_2 electrode; however, its maximum photocurrent at -0.2 V, c.a. 0.5 mA cm^{-2}, was quite low. Figure 1.8b plots ln D against time in the transient response of the photocurrent. The obtained transient time constant of CdS_TiO_2 exceeded that of the co-sensitized one-sided photoelectrode, revealing that the single QD model

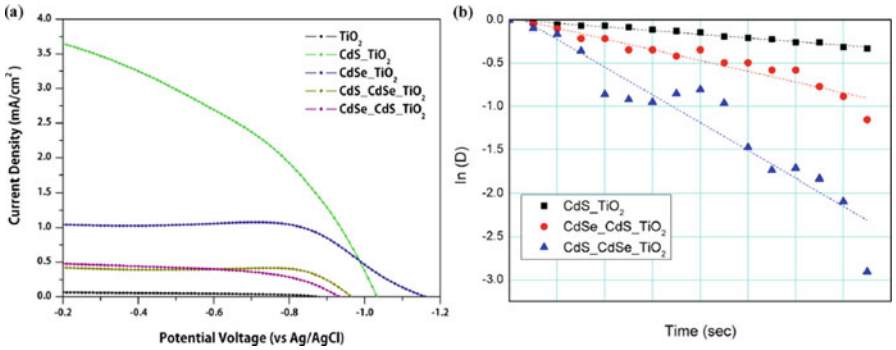

Fig. 1.8 (**a**) PEC measurements of current density-voltage curves at a scan rate of 10 mV s^{-1} under a light intensity of 100 mW cm^{-2}. (**b**) Plot of ln (D) vs. time, obtained from photocurrent dynamics of PEC cells, to compare single QD-sensitized photoelectrodes with co-sensitized one-sided photoelectrodes. (Reprinted with the permission from Ref. [26]. Copyright 2016 American Chemical Society)

provided much more efficient electron transport than did the co-sensitized one-sided model.

CdSe_TiO_2 and CdS_TiO_2 exhibited significantly increased photocurrent densities. The photocurrent density is related to the electronic structure in the conduction band. To reveal the effect of electronic structure on photocurrent density, Fig. 1.8 compares in situ XAS at Ti L- and O K-edges of these photoelectrodes. A remarkable spectral difference exists between CdSe_TiO_2 and CdS_TiO_2 under illumination. The increase in the intensity of peak t_{2g} in the Ti L-edge in Fig. 1.9a upon the light irradiation reveals the increase in the unoccupied states of the Ti 3*d* (t_{2g}) orbitals. Peaks A and B in the O K-edge (lower part of Fig. 1.9a) correspond to electron excitations to O 2*p*-Ti 3*d* (t_{2g}) and O 2*p*-3*d* (e_g) hybridized states, respectively. Notably, the intensity of peak A (peak B) is increased (decreased) upon irradiation, implying more t_{2g} states become unoccupied, consistent with the enhancement of the Ti 3*d* (t_{2g}) state in the Ti L-edge (upper part of Fig. 1.9a). The above results suggest that charge transfer from TiO_2 to CdS may occur. For CdSe_TiO_2, the t_{2g} peak in the Ti L-edge is weakened upon irradiation with light, indicating an increase in charge. With respect to the O K-edge, the hybridized O 2*p*-Ti 3*d* states increased in intensity, revealing probable electron transfer between Ti and O sites. The interfacial charge transfer phenomena that are identified using XAS thus suggest that in CdS_TiO_2, charge migration from TiO_2 to CdS is more efficient than from TiO_2 to CdSe. The charge transfer behaviors in CdSe_TiO_2 and CdS_TiO_2 differ because the oxygen in TiO_2 has different environments when TiO_2 is attached to CdSe and CdS, as revealed by the comparison of the O K-edge of CdSe_TiO_2 with that of CdS_TiO_2 in darkness. The different charge migration paths give rise to different PEC catalytic capacities. Hence, the charge transfer observed herein is a consequence of the higher current density of CdS_TiO_2 than that of CdSe_TiO_2. This success in fabricating a 1D TiO_2 photoelectrode with double-sided tandem

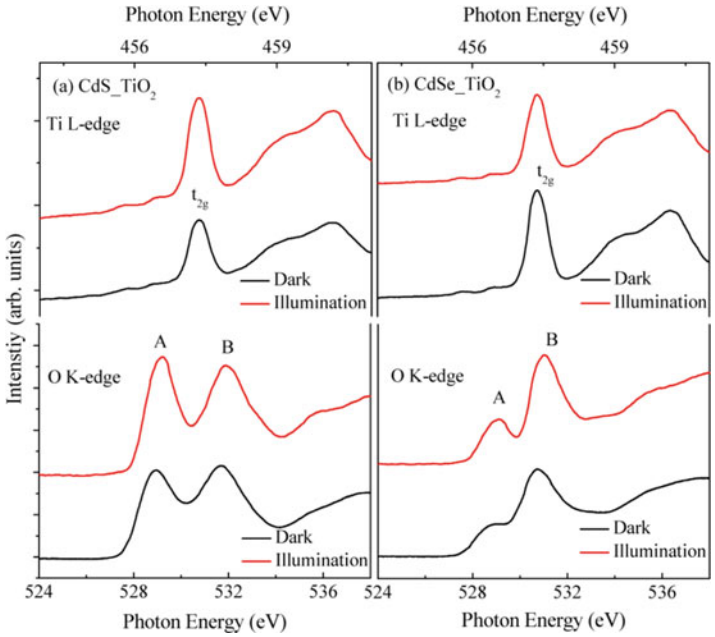

Fig. 1.9 In situ X-ray absorption spectra at Ti L- and O K-edges of (**a**) CdS_TiO_2 and (**b**) CdSe_TiO_2. (Reprinted with the permission from Ref. [26]. Copyright 2016 American Chemical Society)

structure provides an opportunity for designing composite materials with various bandgaps, and this photoelectrode can be further used in other PEC applications.

1.4 Nanoflaky MnO_2/Functionalized Carbon Nanotubes (CNT)

The specific capacitances of electrode materials are strongly govern by the alternations in the local atomic environments and chemical states of the active sites upon the electrochemical charging/discharging, yet information about this dependency is still not fully understood. In a previous study, [27] different functionalized (acid- and amine-functionalized) carbon nanotubes coated with MnO_2 (MnO_2/C-CNT and MnO_2/N-CNT) are fabricated for use in supercapacitors by spontaneous redox synthesis. In situ XAS was exploited to deepen our understanding of the fundamental physical and chemical properties of MnO_2/C-CNT and MnO_2/N-CNT with regard to charge insertion/extraction upon redox reactions. With in situ XAS characterization, how the functionalized surface of a CNT modifies its atomic/electronic structures and how these modifications influence its capacitance. In the following, some experimental results concerning the role of interfaces MnO_2/C-CNT and

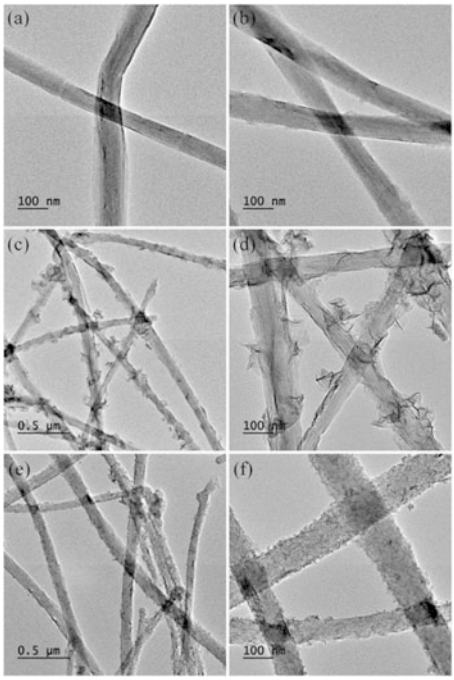

Fig. 1.10 Morphology of MnO_2/functionalized CNT. FETEM images of (**a**) C-CNT, (**b**) N-CNT, (**c** and **d**) MnO_2/C-CNT-24 at different magnifications, and (**e** and **f**) MnO_2/N-CNT-24 at different magnifications. (Reproduced from Ref. [27] with permission from the PCCP Owner Societies)

MnO_2/N-CNT interfaces are discussed, particularly the interfacial properties of MnO_2/functionalized CNT, the changes in the local electronic structures and charge states of these MnO_2/functionalized CNT, and thus the mechanism of charge storage during electrochemical charging/discharging. The MnO_2/C-CNT and MnO_2/N-CNT that are used in this experiment are prepared by the spontaneous deposition of MnO_2 on C-CNT and N-CNT in aqueous $KMnO_4$ for different periods (4 and 24 h); the resulting composites were, respectively, denoted as MnO_2/C-CNT-x and MnO_2/N-CNT-x ($x = 4$ and 24). In situ XAS was carried out using a homemade in situ electrochemical reaction cell to investigate atomic/electronic structure in its working condition. The in situ electrochemical reaction cell was developed with a three-electrode system that comprises MnO_2/functionalized CNT as working electrode, a platinum wire as counter-electrode, and an Ag/AgCl (3 M KCl) as reference electrode in aqueous Na_2SO_4 (1 M). MnO_2 nanostructures coated on various functionalized CNT (C-CNT and N-CNT) present different morphologies. FETWM shown in Fig. 1.10a, d clearly reveal that both of surfaces of C-CNT and N-CNT were rough, especially for the one treated with amine (N-CNT). The coated MnO_2 nanostructures on the surfaces of N-CNT (Fig. 1.10e, f) were more uniform than that on C-CNT (Fig. 1.10c, d). Notably, the MnO_2 nanoflake structures were clearly observed and vertically grown on the C-CNT. The pristine CNT has specific surface area of about ~ 20 $m^2\ g^{-1}$. Following surface treatment, the specific surface areas of MnO_2/C-CNT-24 and MnO_2/N-CNT-24 were estimated to be 87 and 64 $m^2\ g^{-1}$, respectively, by Brunauer-Emmett-Teller (BET) measurement. The MnO_2/C-

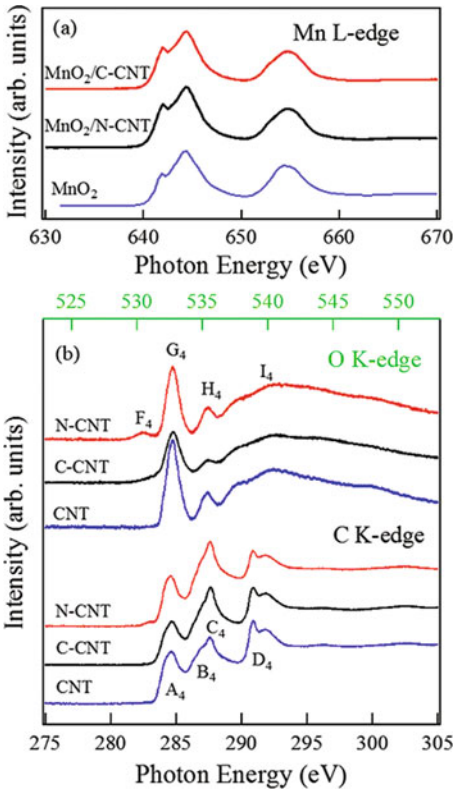

Fig. 1.11 (**a**) Mn $L_{2,3}$-edges of pure MnO_2 and MnO_2 coated on two functionalized CNT (C-CNT and N-CNT). (**b**) C K-edge and O K-edge of pristine CNT, C-CNT, and N-CNT. (Reproduced from Ref. [27] with permission from the PCCP Owner Societies)

CNT-24 that has a higher specific surface area is expected to contribute more active sites for electrochemical reactions, allowing efficient charge insertion/extraction.

XAS experiments were performed to gain more insight on the capacitive behavior of MnO_2/functionalized CNT. Mn $L_{2,3}$-edges XAS of MnO_2/C-CNT-24 and MnO_2/N-CNT-24 are shown in Fig. 1.11a. The Mn $L_{2,3}$-edges describes the electron transitions from the Mn 2*p* core level to the 3*d* empty states. The spectrum splits into two broad peaks, L_3 around 644.4 eV and L_2 around 654.7 eV, as a result of spin-orbital interaction of the Mn 2*p* core hole. The overall spectral profile and the energy position of the peak of both nanocomposites bear a resemblance to the reference MnO_2, suggesting that the MnO_2 was successfully coated on both functionalized CNTs. CNTs were treated with oxidative acid and amine to yield C-CNT and N-CNT and form oxygen-containing functional groups at the CNT surface. The XAS at O K-edge (upper panel) and C K-edge (lower panel) of pristine and functionalized CNTs are shown in Fig. 1.11b. The C K-edge determines the electronic transition from the C 1*s* core hole to the 2*p* empty states. Specifically, peak A_4 (284.6 eV) is owing to electron transitions from C 1*s* to the unoccupied $2p\pi^*$ states of graphitic C-C bonds; peaks D_4 at about 290.9 and 291.9 eV are originated from the C 1*s* to the unoccupied $2p\sigma^*$ state of the C-C bonds. Peaks B_4 and C_4 at

286.9 and 287.6 eV are associated with the C = O π* and C-O σ* states, respectively, and are attributable to the carboxylic functional groups, mainly formed by the oxidation of the CNT [55–57]. It is noted that the intensity of the peaks of the C = O π* and C-O σ* states increases with surface treatment. This fact reflects the increased density of C 2*p* unoccupied states that are associated with chemically functionalized carbon atoms or defect states. The upper panel of Fig. 1.11b compares O K-edge of C-CNT, N-CNT, and pristine CNT, revealing the involvement of oxygen atoms in the interaction between CNT and its functional groups. The different absorption features presented in the O K-edge XAS are resulted from different oxygen-containing groups. Peak G_4 at 532.8 eV has π* character and depends strongly on the local environment of the chemical bond. It is associated with the π* transitions of C = O states that are from carboxylic groups. Peak H_4 (535.5 eV) and the broad peak I_4 (537.0~541.0 eV) are assigned as the σ* transitions of O-H, C-O, or C = O groups of functionalized CNT. The weak absorption feature F_4 shown at about 530.5 eV in N-CNT is related to the π* transitions of C-O in carbon-oxygen species and disordered carbon in CNT. This observation is in line with the weak feature at 283.1 eV in the C K-edge of N-CNT (lower panel of Fig. 1.11), which is originated from the disordered carbon. The analytical C K-edge and O K-edge XAS results demonstrate that different functional groups on the surface of CNTs give rise to different atomic/electronic properties. N-CNT takes a more disordered carbon structure or defect states than C-CNT, and these disordered structure and defect states would modify the morphologies of MnO_2/functionalized CNTs [58, 59]. Thus, surface functionalization of CNT is commonly considered to be an effective way of advancing its specific capacitance of nanocomposites [60].

To shed light on the interfacial electronic properties in MnO_2/functionalized CNT, the C K-edge XAS of different functionalized CNTs (C-CNT and N-CNT) and MnO_2/functionalized CNTs (MnO_2/C-CNT and MnO_2/N-CNT) with different preparation times (4 h and 24 h) are compared in Fig. 1.12a. The peaks (indicated by asterisks) at 296.6 and 299.1 eV are related to the K L_2-edge and L_3-edge, which resulted from the fact that spontaneous redox reaction involves K^+ in the MnO_2 structure [61]. Figure 1.12a exhibits several interesting features. Firstly, peak A_5 (π* transition) in the MnO_2/functionalized CNT suggests that throughout the spontaneous redox process, a highly ordered graphitic structure is preserved, maintaining the good electrical conductivity of MnO_2/functionalized CNT. More states are observed in MnO_2/N-CNT-24 than in MnO_2/C-CNT-24, indicating that MnO_2/N-CNT-24 possesses more conductive paths. Secondly, the charge transfer between MnO_2 to the C 2*p*π* state in functionalized CNT at the interface is evidenced by comparing the C K-edge and Mn L-edge. The intensity of peak A_5 of MnO_2/functionalized CNT is lesser than that of functionalized CNT, and the intensity of the Mn L-edge in MnO_2/functionalized CNT is greater than that in pure MnO_2 (Fig. 1.11a). Thirdly, the intensities of peaks B_5 and C_5 of MnO_2/functionalized CNT are greater that exceed those of functionalized CNT, indicating a significant oxidized carbon species near the interface, which withdraws significant charge from C = O π* and C-O σ* states. A significant interaction between functionalized CNT and MnO_2 implies formation of Mn-O-C bonding, which is evidenced by the presence of peaks B_5

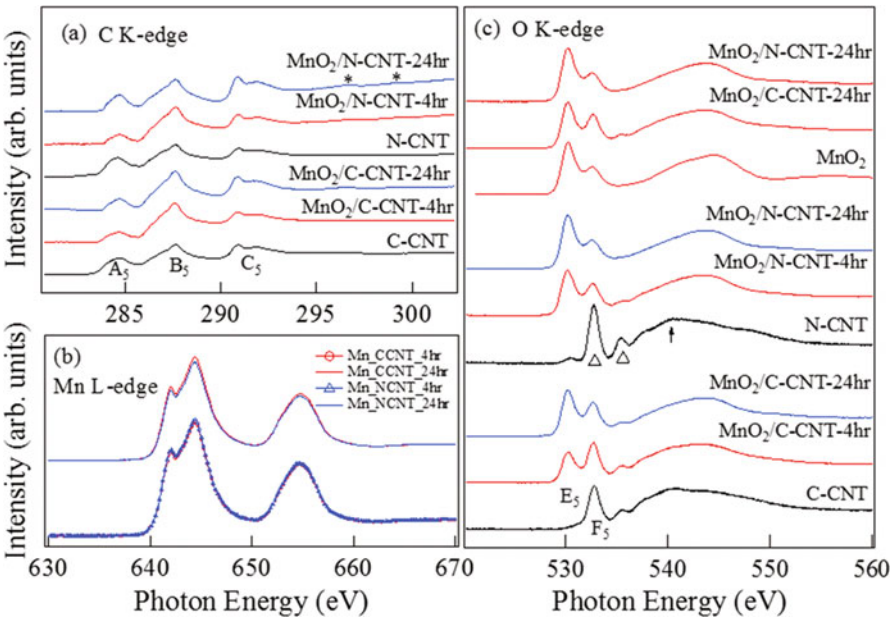

Fig. 1.12 XAS of MnO_2/CNT of different deposition times (4 h and 24 h). (**a**) C K-edge, (**b**) Mn $L_{2,3}$-edges, and (**c**) O K-edge. XAS of functionalized CNTs (C-CNT and N-CNT) are displayed as reference. (Reproduced from Ref. [27] with permission from the PCCP Owner Societies)

and C_5 and the varied intensity of peak A_5 (π^* states). Notably, the peaks associated with C-O and C = O and Mn L_3-edge of C-CNT exhibit higher intensity than those of N-CNT, as these MnO_2 nanoflakes are coated on different functionalized CNTs. Consequently, there are more electrons from MnO_2 transfer to π^* state in C-CNT.

To investigate the interfacial effect during growth, the duration of deposition for MnO_2 is increased (from 4 h to 24 h). For MnO_2 deposited with 4 h on both MnO_2/C-CNT and MnO_2/N-CNT significantly lessens the intensities of C-C π^* peaks, suggesting significant interruption of the carbon bonding in both C-CNT and N-CNT structures. As the deposition time is further increased to 24 h, it is observed that the intensity of the π^* state is enhanced, rather than continuously decreased. Incorporation of MnO_2 increases the degree of graphitization, so the intensity of the C-C π^* states is enhanced [59]. From Mn L-edge (Fig. 1.12b), MnO_2/functionalized CNT-24 has less Mn 3*d* unoccupied states than does MnO_2/functionalized CNT-4. Thus, the analytical results indicate that the Mn 3*d* orbitals gain charge from the σ^* state of functionalized CNT. Then the electrons are back donated to the π^* states of functionalized CNT, lessening the density of π^* states. The back-donation of the charge was also observed by Zhou et al. [62].

To learn more insight into the role of oxygen in the growth of MnO_2, Fig. 1.12c shows the O K-edge of MnO_2 deposited on different functionalized CNTs. Peaks E_5 and F_5 are associated with hybridized O 2*p*-Mn 3*d* t_{2g} and O 2*p*-Mn 3*d* e_g orbitals, respectively. A broad peak G_5 is originated from hybridized O 2*p*-Mn 4*sp* states. The

decrease in the peaks indicated by two triangles and an arrow (532.8, 535.5, and 540 eV) and the increase in the peak E_5 intensity at 530 eV suggest the growth of MnO_2 on the surface of functionalized CNT. Moreover, the ratio of the peak intensity E_5 and F_5 vary greatly for MnO_2/C-CNT and MnO_2/N-CNT-4 which reflects the fact that decorate the MnO_2 on C-CNT and N-CNT at different growth rates. The MnO_2 is nucleated at defect sites or edge planes on the surface of CNTs [61, 62]. The morphologies of MnO_2 coated on C-CNT and N-CNT are strongly influenced by the surface and structural properties of C-CNT and N-CNT. The relatively sluggish growth for MnO_2/C-CNT with few defect sites and a low edge plane structure could assist the vertical growth of MnO_2 on the C-CNT. As increasing the deposition time, ratio of peak intensity E_5 to F_5 is increased until it reached almost same value of pristine MnO_2, indicating that both C-CNT and N-CNTs were uniformly decorated with MnO_2. The area under the O K-edge is larger in MnO_2/N-CNT-24 and MnO_2/C-CNT-24 than in MnO_2, suggesting reduction of electrons in O 2*p* states. Notably, the C π* states (from C K-edge shown in Fig. 1.12a) gain some charges. Thus, the redistribution of charge is observed between MnO_2 and functionalized CNTs. This may create a conduction path and assist the capacitive performance.

Figure 1.13a, b presents the CV curves MnO_2/C-CNT-24 and MnO_2/N-CNT-24 electrodes obtained at different scan rates. The results show that MnO_2/functionalized CNTs have ideal capacitive behavior in the combination of EDLC from functionalized CNTs and pseudocapacitance from MnO_2. It is well known that only the surface layer of MnO_2 has pseudocapacitance [63]. MnO_2/C-CNT is therefore expected to exhibit a higher specific capacitance than MnO_2/N-CNT. The CV curve of MnO_2/N-CNT modifies from square to oval shape progressively as increasing the scan rate over 50 mV s^{-1} which is attributable to the fact that the incorporation of ions is restricted on the active surface layer for charge storage. In situ XAS was then utilized to gain insights into the charge storage mechanism of MnO_2/C-CNT-24 and MnO_2/N-CNT-24 electrodes under their real working conditions.

In situ Mn K-edge XAS spectra (Fig. 1.14a, b) investigate atomic and electronic structures of the MnO_2/C-CNT-24 and MnO_2/N-CNT-24 during the charging-discharging reaction. All spectra have a weak pre-edge feature A_8 (~6542 eV) and a strong main feature B_8 (~ 6563 eV). The weak pre-edge feature is originated from the electric dipole-forbidden 1s-3d transition. This transition becomes partially allowed in a non-centrosymmetric environment of a distorted MnO_6 octahedron, resulting in the electric quadrupole coupling and the hybridized 3*d*-4*p* orbital [64, 65]. The octahedral crystal field splits the pre-edge feature to two peaks (A_{8a} and A_{8b}). The peaks A_{8a} and A_{8b} are associated with the transition $1s \rightarrow 3d$ t_{2g} and $1s \rightarrow 3d$ e_g states, respectively [64, 65], and the main absorption feature B_8 is arising from the dipole-allowed $1s \rightarrow 4p$ transition. The energy shift of the main absorption feature reflects reversible redox reactions, including the reversible changes in the Mn charge state and MnO_2 microstructure of the MnO_2/C-CNT-24 and MnO_2/N-CNT-24 during charging/discharging.

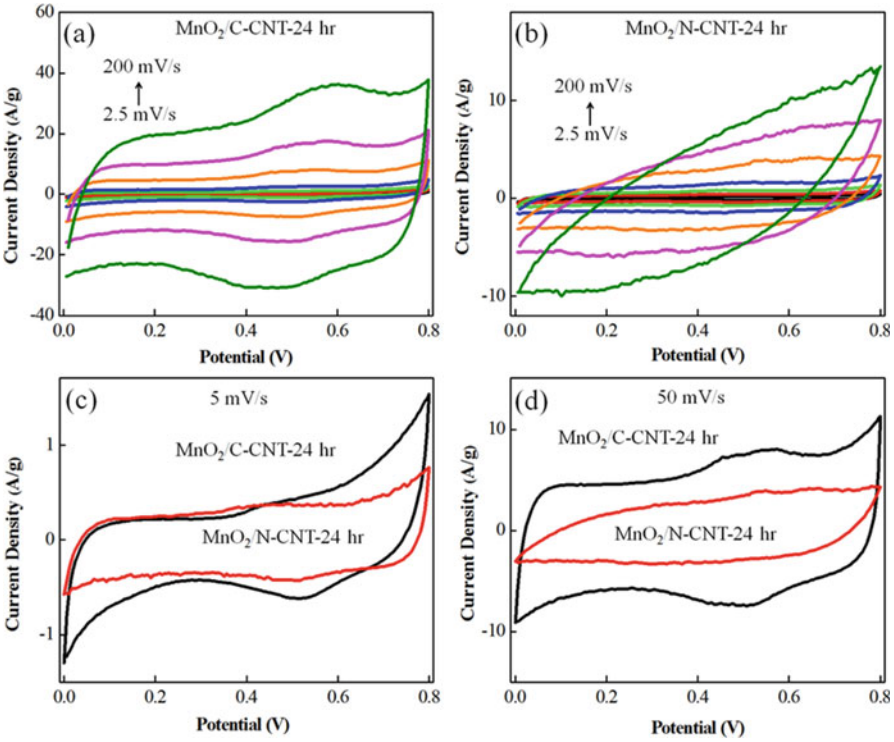

Fig. 1.13 Cyclic voltammetry curves of (**a**) MnO_2/C-CNT-24 and (**b**) MnO_2/N-CNT-24 collected with different scan rates (2.5, 5, 10, 20, 50, 100, and 200 mV s^{-1}). Cyclic voltammetry curves of MnO_2/C-CNT-24 and MnO_2/N-CNT-24 collected with scan rates (**c**) 5 mV s^{-1} and (**d**) 50 mV s^{-1}. (Reproduced from Ref. [27] with permission from the PCCP Owner Societies)

Figure 1.15 compares the pre-edge area following background subtraction from the spectra in Fig. 1.14. The pre-edge area reflects not just the mean charge state but also the local atomic symmetry of targeted element. The electronic structures of the Mn^{4+} and Mn^{3+} ions, respectively, exhibit 3d ($t_{2g}^3e_g^0$) and 3d ($t_{2g}^3e_g^1$) configurations. The distortion of the MnO_6 octahedron could split pre-edge feature of Mn K-edge. The spectral profile and intensity of a pre-edge feature of manganese oxide are strongly related to its structure and can be used to determine the unknown local atomic arrangement [66–69]. MnO_2 was assembled from corner- and edge-sharing MnO_6 octahedrons, forming tunnel structures with various tunnel sizes through the material MnO_2. Variation in the MnO_6 octahedron has a great influence on the absorption intensity of pre-edge feature. The intensity of pre-edge feature is proportional to the ratio of the number of edge-sharing to that of corner-sharing MnO_6 octahedron. Besides, the distortion of MnO_6 octahedron from centrosymmetric to non-centrosymmetric enhances the pre-edge intensity as the size of tunnel structure of MnO_2 decreases. The pseudocapacitance of MnO_2 supercapacitors is associated with the intercalation (de-intercalation) of alkali cations into (from) MnO_2, which is

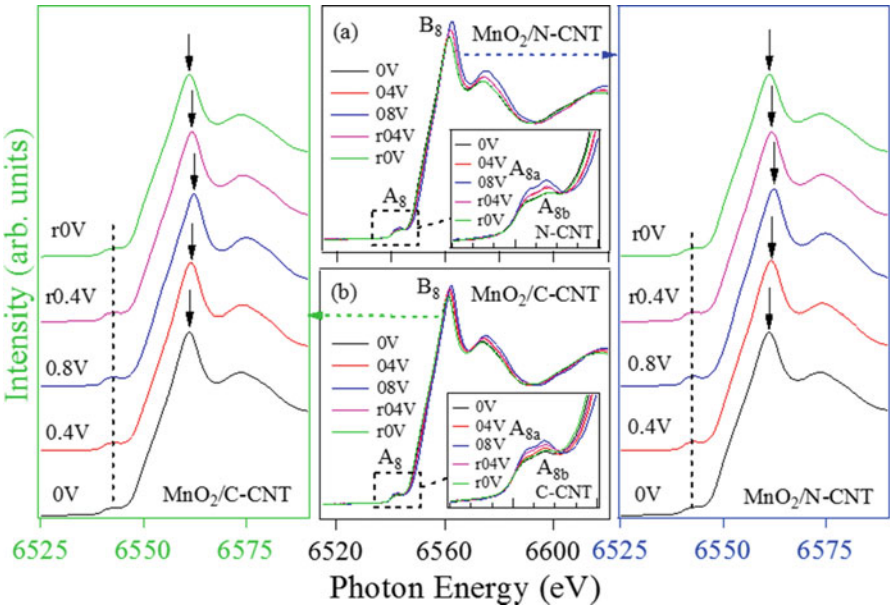

Fig. 1.14 In situ XAS at Mn K-edge of (**a**) MnO_2/N-CNT-24 and (**b**) MnO_2/C-CNT-24 with various bias potentials. Insets expand pre-peak area. (Reproduced from Ref. [27] with permission from the PCCP Owner Societies)

significantly influenced by the crystalline morphology of, as well as the sizes of the tunnel structures in, MnO_2. As a result, the intensity of the pre-edge of MnO_2/N-CNT at 0.8 V surpasses that of MnO_2/C-CNT which indicates that not just the charge state of Mn increases in MnO_2/N-CNT but also MnO_2/N-CNT comprises short Mn-O bonds and small tunnels [66–69]. On the contrary, MnO_2/C-CNT exhibits lower pre-edge intensity and thus has larger tunnel size. The above analytical result may provide an effective route to rise charge transfer and decrease the diffusion length of ion during the charging-discharging process.

Figure 1.15b reveals that the change of the intensity of pre-edge feature of Mn K-edge during charging-discharging is reversible, and the result is consistent with the shift of the main absorption peak in Fig. 1.14a, b. These results demonstrate the reversible change of the mean charge state of manganese ions during the redox reaction which is associated with the Faradaic pseudocapacitance. A closer look at the variation of the pre-edge feature unveils the recurrence of the peak profile and intensity of MnO_2/N-CNT (0-0.4-0.8-r0.4-r0V), suggesting that the electrochemical redox reaction is highly reversible, which is also supported by the favorable capacitive behavior at a low scan rate (Fig. 1.13c). Figure 1.15c shows the relationship between the energy shift and the charge state. The mean charge states of Mn in MnO_2/C-CNT (MnO_2/N-CNT) at different bias potentials of 0, 0.4, 0.8, 0.4, and 0 are 3.25 (3.18), 3.51 (3.51), 3.83 (3.91), 3.42 (3.51), and 3.17 (3.18). The changes in the Mn charge states in MnO_2/C-CNT and MnO_2/N-CNT again demonstrate that

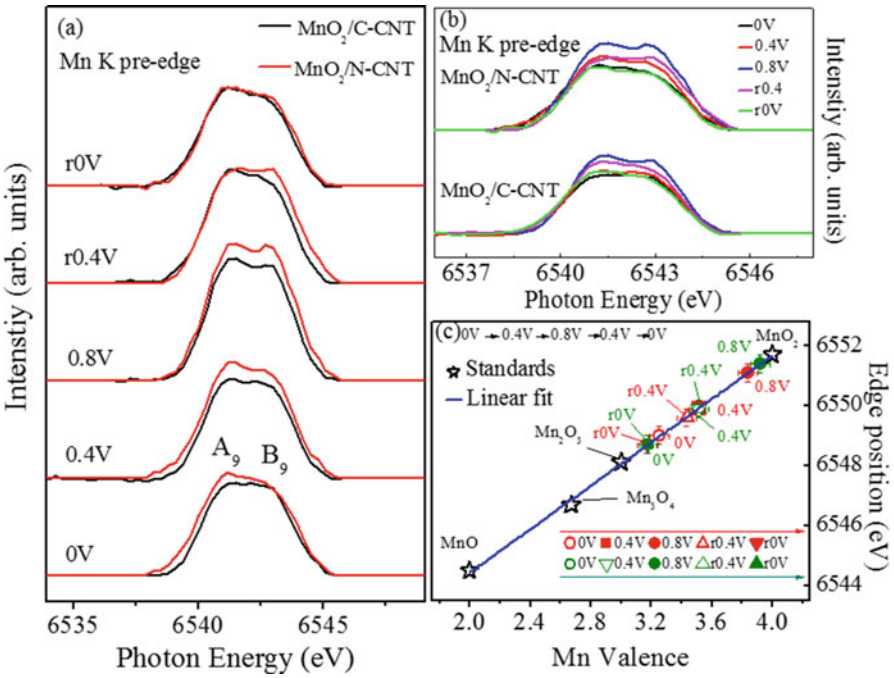

Fig. 1.15 (**a**) Pre-peak area of Mn K-edge of MnO_2/N-CNT-24 and MnO_2/C-CNT-24 with different bias potentials. (**b**) Overlaid Mn K pre-peak area of MnO_2/N-CNT-24 and MnO_2/C-CNT-24 with different bias potentials and (**c**) Mn charge states as a function of bias potentials during redox reaction. (Reproduced from Ref. [27] with permission from the PCCP Owner Societies)

MnO_2/N-CNT exhibited high electronic and ionic conductivity and a reversible redox reaction (Mn^{3+}-Mn^{4+}).

To summarize the above CV and XAS results, MnO_2/N-CNT with enhanced C-C graphitic π* state could offer the ion conduction path and facilitate transport at the electrode/electrolyte interface and thus exhibited a perfectly symmetrical rectangular CV shape at a low scan rate. Yet, at a high scan rate, the CV curve of MnO_2/N-CNT is greatly distorted, which is perhaps owing to the limitation on the incorporation of ions by the small tunnels, hindering ion transport. Although MnO_2/C-CNT comprises large tunnels and has a large specific surface area, its redox reaction is not fully irreversible. The fact that is probably attributable to fewer π* states is revealed in MnO_2/C-CNT. Moreover, MnO_2/C-CNT preserves its rectangular CV curve at a high scan rate which is attributable to its large tunnels and high specific surface area, allowing the swift transport of electrolyte ions and facilitation of rapid charging-discharging. The above analytical results demonstrate the effects of the scan rate on the electrical conduction and ionic transport in MnO_2/functionalized CNTs which is strongly governed by the modification of local atomic structure and electronic structure during the redox reaction. Coupled CV and in situ XAS measurements

could serve as a powerful characterization tool looking into deep insight for electrochemical energy storage materials.

1.5 Conclusion and Future Perspective

The results that are presented herein motivate further spectroscopic study of the effects of nanostructured electrode materials on the atomic and electronic properties of water-splitting and supercapacitor devices in which they are used. In Sect. 1.3, spectroscopic characterization tools were briefly introduced. In Sect. 1.3, spectroscopic techniques and current density-potential measurements were combine to provide new insights into the photoconversion mechanisms of TiO_2 1D nanostructures (a freestanding TiO_2 nanotube array and QD co-sensitized TiO_2 nanorod arrays). In Sect. 1.4, the charge storage mechanism of MnO_2/functionalized CNT during charge/discharge process was examined in detail by combining in situ XAS and electrochemical techniques. The results presented herein indicate the effectiveness of spectroscopic techniques in elucidating interactions in these complex nanocomposites. They also provide important fundamentals in nanoscience and lead to the latest advances in material synthesis and characterization. New perspectives on the mechanism of energy storage and conversion devices are also discussed in this chapter.

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Chapter 2
A Correlated Study of Nanotube/Nanowire Transistor Between TEM Inspection and Electrical Characterization

Yann-Wen Lan and Po-Chun Chen

2.1 Introduction

Nanomaterial is usually defined as smaller than one tenth of a micrometer in at least one dimension. It is studied on the nanoscale and especially those that have special properties originating from their nanoscale dimensions [1–3]. Nowadays, many scientists are interested in this field and reveal possible new quantum mechanical effects, such as quantum size effect. It is indicating that the electronic properties of bulk solids are altered with great reductions in size. Scientists discover the defect on the nanomaterials that is common in the presence of structure when synthesizing nanomaterials. The defect may dominate to physical properties in the nanomaterials at times. Among others, the transport properties of nanomaterials are known to be dramatically altered by the presence of defect such as dislocations, scatterers, or impurities, and hence information about these defects is highly desirable. In the beginning, we introduce our method to do a correlated study between material defects and electrical characterization. And then, some of experiments are demonstrated to support it. The main results show that defect on the nanomaterials is an important issue, leading to a tunable physical property. If one can control or take this advantage, it is possible to create various electronics on the nanomaterial in the future.

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2.2 Experimental Method

The experimental parts include the multi-probe station, how we in situ manipulate nanomaterials, and how we design an innovative through-hole chip and membrane chip for correlation between material structure and electrical characterization.

2.2.1 Multi-probe Stations

Zyvex S100 Nanomanipulator is a multi-probe station system in scanning electron microscope (SEM), which is useful tool for micro- and nanoscale research, development, and production applications. The feature is four positioners that grasp, move, test, and optimally position micro- and nanoscale samples with four axes of movement. Figure 2.1 shows S100 head unit and PC-based system. The head unit is installed in SEM chamber, and thus it is operated by joystick in PC-based system as shown in Fig. 2.2. The advantage of joystick is intuitive three-dimensional control for manipulation. PC-based system is a friendly graphical user interface in a Windows environment.

The head unit dimensions and one of the positioners are schematically shown in Fig. 2.3. The dimensions of head unit are depicted in the figure, and the components in a positioner are pointed out. The technical specifications for range of motion and resolution in coarse actuator, fine actuator, and rotational stage are listed in Table 2.1. It summarized this instrument-related information the operator needed. The real image observed from SEM is shown in Fig. 2.4, which displays the top view

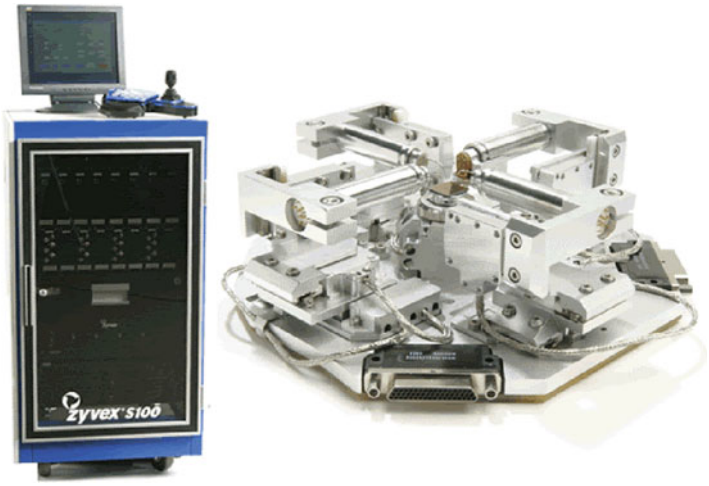

Fig. 2.1 Zyvex S100 Nanomanipulator system. Right image is the PC-based modular design system and left image is the head unit

Fig. 2.2 Joystick and keypad control with user-friendly graphical user interface in a Windows environment

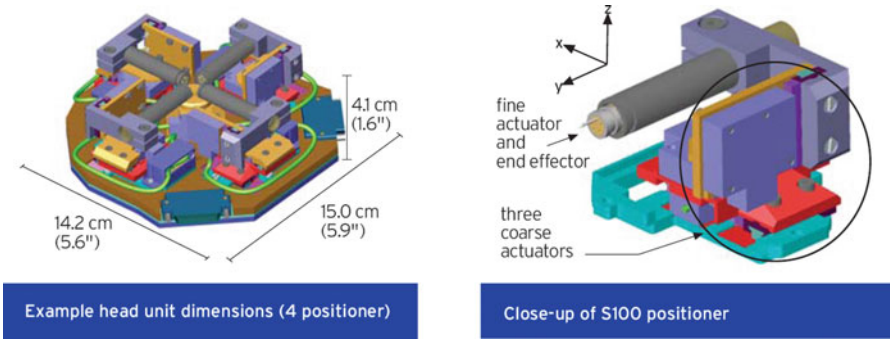

Fig. 2.3 Head unit dimension and one of S100 positioners

Table 2.1 S100 technical specifications

Component (see figures above)	Range of motion	Resolution
Coarse actuator	12 mm in X, Y, and Z axes	100 nm
Fine actuator	100 µm in X and Z axes, 10 µm in Y axis	Better than 5 nm
Rotational stage	360° continuous	3 µradians

image with four tungsten probes in the monitor. The right image of Fig. 2.4 is also showing the nanoelectronics which demonstrate in situ test of electrical characterization on nano-interconnect.

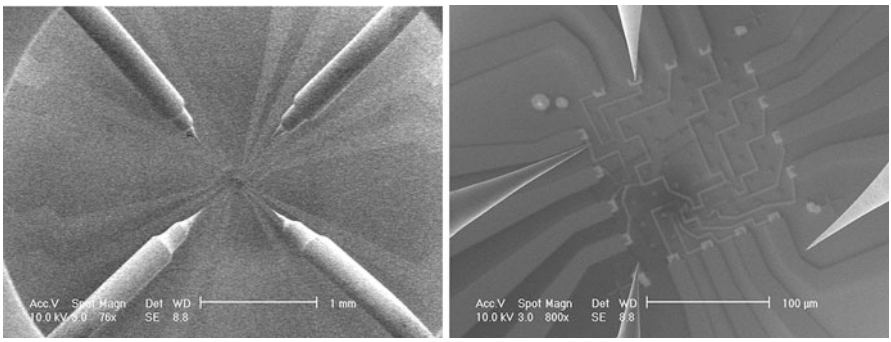

Fig. 2.4 SEM image of four tungsten probes with nanoelectronics displaying in situ test of electrical characterization

2.2.2 In Situ Nano-manipulation

From the description of multi-probe station in Sect. 2.2.1, the pick-and-place manipulation of nanomaterials is under consideration and demonstrated in this subsection. Here, nanowires and carbon nanotubes are proceeding to pick and place by the manipulator. Nanowires usually did not possess the stronger adhesion between probe and themselves. It is convenient to pick and place the nanowires. However, the pick-and-place carbon nanotube and graphene are assisted with electron beam irradiation since the problem of strong adhesion must be overcome. Figures 2.5 and 2.6 show the pick-and-place procedure for carbon nanotube and graphene, respectively. Inset of Fig. 2.5a displays the broken carbon nanotube by focusing e-beam in which the length can be determined by our control. The sample here is about 6 μm, and it is placed on a through-hole chip as shown in Fig. 2.5c, d is a tilt angle image.

The few layers of graphene are manipulated by multi-probe station, and the test results are displayed as shown in Fig. 2.6. The graphene can be picked by Au-probe without e-beam cutting, while the adhesion between knife and graphene is weak. In some cases, the e-beam assists to break the graphene even though e-beam damages the graphene structure at the same time. Figure 2.6b, c shows Au-probe is easy to pick the graphene up and move to the top of the suspended electrodes in the through-hole chip. After the graphene touches with all suspended electrodes, the piece of graphene is automatically expended on electrode surface as shown in Fig. 2.6d.

Nanowire manipulation is presented in Fig. 2.7. The nanowire is picked from the chip edge that is the source of nanowire material. The demonstration here is that the Bi_2Te_3 nanowire is placed on the corner of through-square-hole. Figure 2.7a shows one end of nanowire adhered to an Au-probe located at top of position. The nanowire in the other end is ground to the substrate as the probe moves down slowly. When the probe touches the substrate ground, the nanowire is fallen down on the position as shown in Fig. 2.7b.

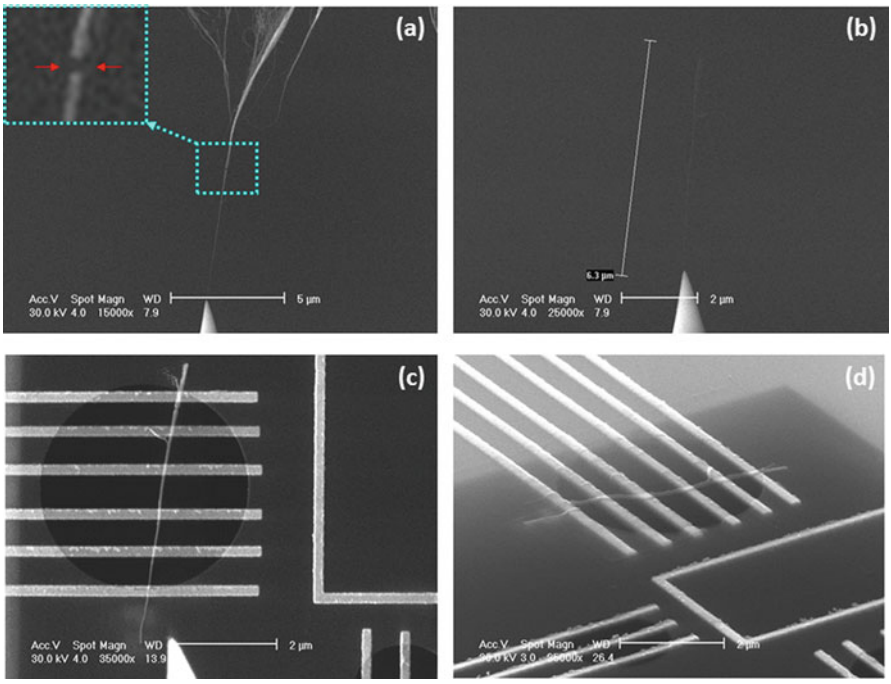

Fig. 2.5 (**a**) A broken CNT bundle with one end attached to a probe (at the bottom). The inset shows a blowup of the broken CNT (indicated by red arrows) cut by a focused electron beam. (**b**) A CNT length of about 6 µm attached to a probe. (**c**) SEM image of the device. The black circular area is the through-hole, and outside it is the 75-nm-thick Si_3N_4 membrane. (**d**) SEM image is a tilted view of the same device

2.3 Fabrication of Through-Hole Chip and Membrane Chip

A 7×7 mm^2 standard chip is designed by ourselves and fabricated by photolithography techniques (Mask aligner EVG-620). It consists of 16 leads connected an area of 68×68 µm^2 in the central part with outermost millimeter-sized 16 contact pads. Electron beam lithography was performed to obtain the nanostructure in central region. These nanostructures provided a bridge between millimeter-scaled electrical probes of the sample holder and nanometer-scaled devices, allowing electrical transport measurements of the devices.

Electron beam lithography (EBL) is a mask-less technique and offers higher patterning resolution than photolithography. The reason for high resolution is the short wavelengths about 0.5 angstroms exhibited by the electrons in the energy range that they are being used by EBL systems.

A standard chip with layout including alignment crisscross keys was coated with e-beam resist (PMMA) and then exposed with the pattern by electron beam. The

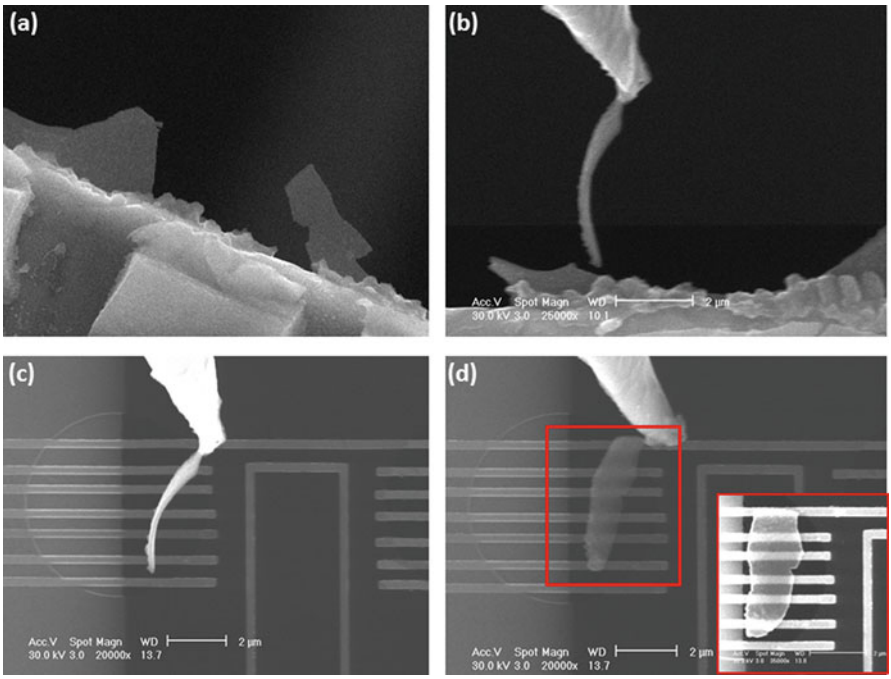

Fig. 2.6 (**a**) SEM image of graphene sticking out of a blade (the bottom white part). (**b**) A piece of graphene adhered to an Au-probe. (**c**) The graphene attached to an Au-probe on the top of suspended electrodes. (**d**) SEM image of the graphene device. The bottom-right inset shows a blowup of the same device located on the top of paralleled suspended electrodes

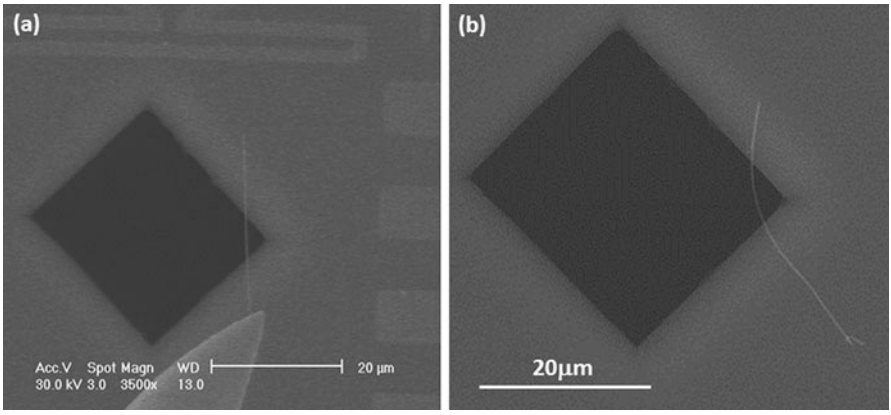

Fig. 2.7 The placement process of Bi_2Te_3 nanowire on the edge of the through-square-hole. (**a**) Nanowire adhered to an Au-probe located on the top of the through-square-hole. (**b**) Bi_2Te_3 nanowire lain right on the position

pattern was designated by a CAD program and then transferred to the control PC of scanning electron microscopy (SEM)-based or commercial electron beam lithography instrument.

In the SEM-based e-beam writer (FEI sirion), Nanometer Pattern Generation System (NPGS) is available from Joe Nabity Lithography Systems in Boxeman, MT. This system interfaces to a personal computer with a digital to analog converter card to generate three voltage signals. Two out of three voltage signals are fed to the input amplifiers of the X and Y scan coils of the SEM. So this will enable us to precisely control the position of the beam with the PC supplying the control signals. The remaining third voltage signal is used to control the beam blanking of the SEM to turn the beam OFF and ON as needed. The switching time of the ON/OFF cycles is used to define the exposure dosage. The patterns are exposed on a point-by-point basis. The beam scan is performed by stopping at points spaced apart by a predetermined distance, unblocked for a time period to give every point the desired dose, blanked, and then moved further to the next point.

The commercial Elionix ELS-7000 e-beam writer system is equipped with a thermal field emission electron beam with a maximum acceleration voltage of 100 KeV. This system is equipped with the position detector based on laser interferometer, which can provide an accuracy of 20 nm in both overlaying and stitching.

In order to correlate the structure with electrical characterization, the through-hole chip is designed to test in the 4-inch wafer. The procedure is combined with a series of semiconducting processes as shown in Fig. 2.8. As a run batch process is done, we can acquire almost 100 7 × 7 mm^2 through-hole chips.

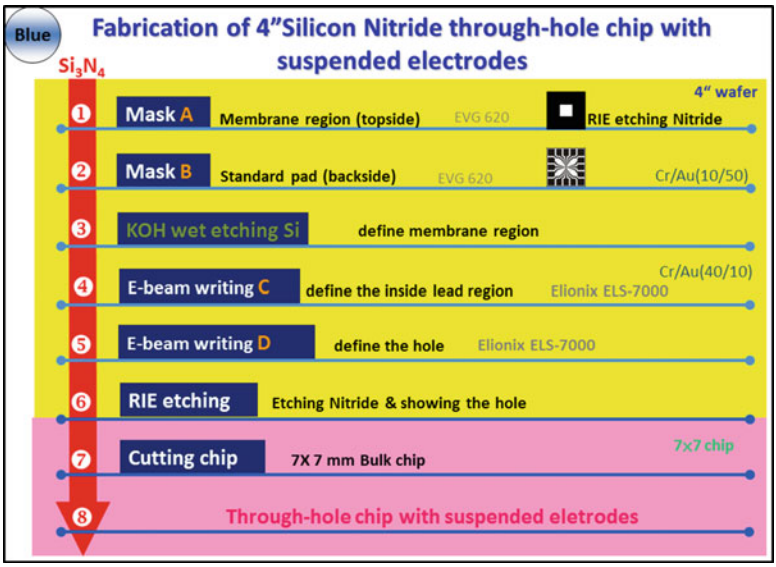

Fig. 2.8 The 4-inch wafer fabrication process of through-hole chip. The sequence of fabrication process follows the flowchart step by step. One hundred 7 × 7 mm^2 through-hole chips are obtained in a run process

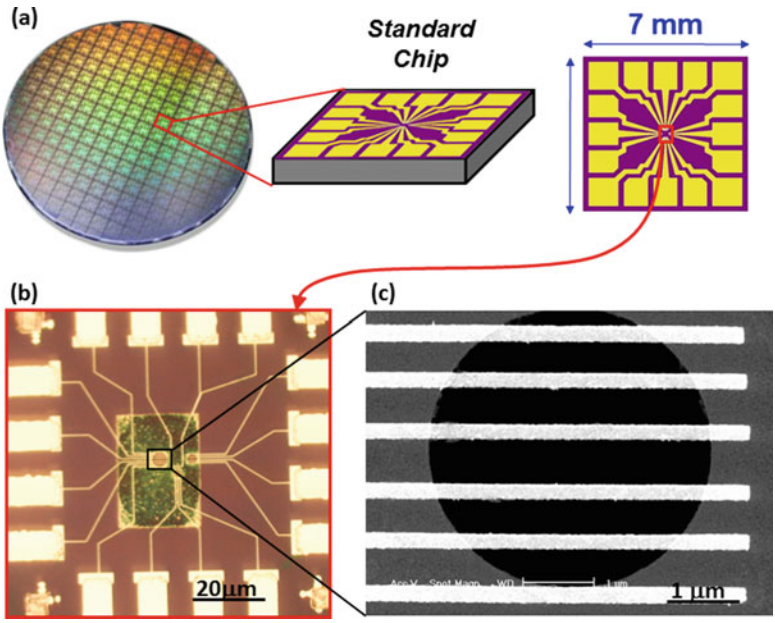

Fig. 2.9 (**a**) Schematic diagrams of 7 × 7 mm^2 standard chips in a 4-inch wafer. (**b**) Top view of center region in the through-hole chip. The inner leads and through-hole are defined by e-beam lithography, and the square region is a thin-layer silicon nitride. (**c**) The SEM image of through-hole with suspended electrodes

Figure 2.9a shows a 4-inch wafer and one of 7 × 7 mm^2 standard chips. The center region is blow up and shown in Fig. 2.9b, which displays the inner leads defined by e-beam and membrane region. The SEM image of through-hole chip is presented in Fig. 2.9c in which the circle is empty and electrodes extend across to the hole.

2.4 Demonstration of the Correlated Study

In this section, we give three examples to demonstrate the correlated study between TEM inspection and electrical characterization as below.

2.4.1 Effects of Oxygen Bonding on Defective Semiconducting and Metallic Single-Walled Carbon Nanotube Bundles

In this subject, in order to convert the pristine carbon nanotube (CNT) (which is p-type transport behavior in air) into a carbon-deficient CNTs (CD-CNTs), this

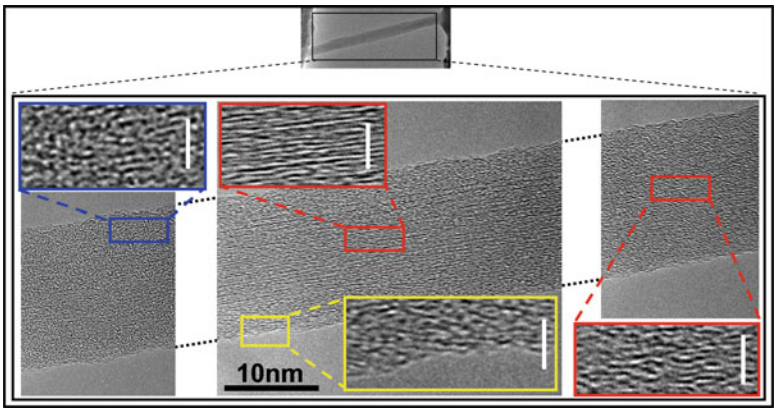

Fig. 2.10 TEM images of the suspended CNT bundle. The top is a low-magnification TEM image. The main panels are high-magnification TEM images of the CNT bundle in the left, center, and right regions. The enlarged red and blue rectangles show areas with missing carbon atoms knocked out by electron irradiation. The enlarged yellow rectangle shows CNT outer shell with carbon dangling bonds, leading to rugged surface. The white scale bars in all insets are 3 nm. (Reprinted from Ref. [1], Copyright 2012, with permission from Elsevier)

particular device was exposed to 200 k*e*V, 100pA electron beam irradiation in a TEM operated in scanning mode with a scanning area of 500 × 500 nm^2. The exposure time was around 1 min and the defective region found to grow with the exposure time. After the "electron knockout process" was complete, the resultant structure was imaged to allow for correlation of physical and electrical characterization. The top part in Fig. 2.10 shows the device after the electron knockout process with enlarged TEM images of defective structure at different locations displayed in the main panels. The measured CNT bundle has a diameter of about 20 nm. Comparing the two enlarged red rectangular areas, the right segment shows more damage than the middle segment; this is due to the TEM annealing process. The outer shell of the CNT bundle shows the most destruction (the blue and yellow rectangular areas) as this is where the bundle is thinnest [4]. In particular, the surface imaged in the yellow rectangular area is quite rugged. Oxygen molecules are attracted to areas within the carbon structure where bonds are broken. They are then absorbed into the structure by either physisorption or chemisorption [5, 6], even at room temperature [7]. In physisorption, van der Waals force allows oxygen molecules to bond with the carbon lattice either where it has been broken or is smooth, though the former is more favored.

The oxygen molecules are about 2.6 Å away from the bound carbon atoms. In chemisorption, oxygen atoms can be absorbed into the lattice occupying carbon vacancies and forming covalent bonds. Compared to physisorption, chemisorption produces a more stable lattice structures due to the formation of strong C–O bonds [5]. A similar result for TEM observations was reported for a CNT bundle bound with oxygen-containing groups [8].

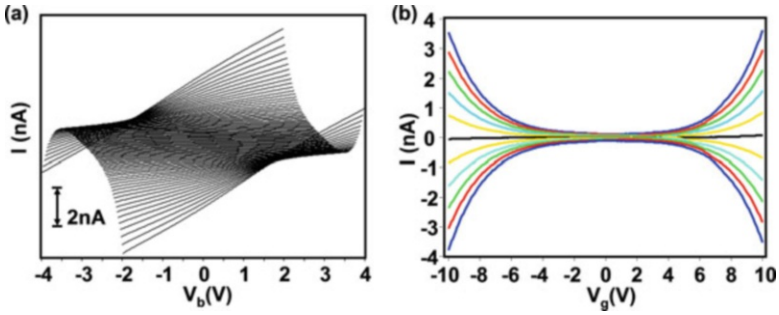

Fig. 2.11 Bipolar characteristics of the CD-CNT bundle. (**a**) I-V_b curves at different gate voltages from 10 V to −10 V; the curves are shifted in respect to the gate voltage for clarity. (**b**) I-V_g curves at different bias voltages from 3 V (top) to −3 V (bottom); the curves are acquired with a step of 0.6 V. (Reprinted from Ref. [1], Copyright 2012, with permission from Elsevier)

The electrical properties in oxygen chemisorbed on CD-CNTs are discussed below. The measured CNT device is the one shown in Fig. 2.11.

Figures 2.11a, b show I-V_b curves at different gate voltages and I-V_g curves at different bias voltages, respectively. Both plots show signatures of bipolar behavior: the conduction of the bundle is enhanced in *both* positive and negative gate voltages. This bipolar behavior is found to be very stable, which can withstand thermal treatment at 200 °C for 10 min and can survive in a vacuum. We thus attribute this change to oxygen chemisorption. This is further supported by theories, which stated that oxygen chemisorption tends to lower the energy bandgap of semiconducting CNTs [9, 10]. For CNTs with a small bandgap, chemisorption can thus tune the character of the tubes into bipolar [11, 12]. This kind of device is stable and convenient for multiple applications and is different from the case of pristine CNTs in which oxygen plasma is necessary for chemisorption.

2.4.2 *Stacking Fault Induced Tunnel Barrier in Platelet Graphite Nanofiber*

In this particular study, a platelet graphite nanofiber (PGNF) was arbitrarily selected and made into an electronic device whose layout is schematically shown in Fig. 2.12a. The fabrication procedures are briefly described as follows. First, 75-nm-thick silicon chips with a 40 × 40 μm^2 Si_3N_4 membrane were constructed by means of photolithography and KOH wet etching. The PGNFs were then positioned atop the Si_3N_4 membrane window using a scanning electron microscopy (SEM)-based nanomanipulator [1]. Subsequently, nanoscaled Ni(20 nm)/Au(70 nm) electrodes made using standard electron beam lithography were placed atop the PGNFs. In addition, an electrode was placed about 1 μm away from the PGNF to serve as a side gate. Current-voltage characteristics were measured using symmetric

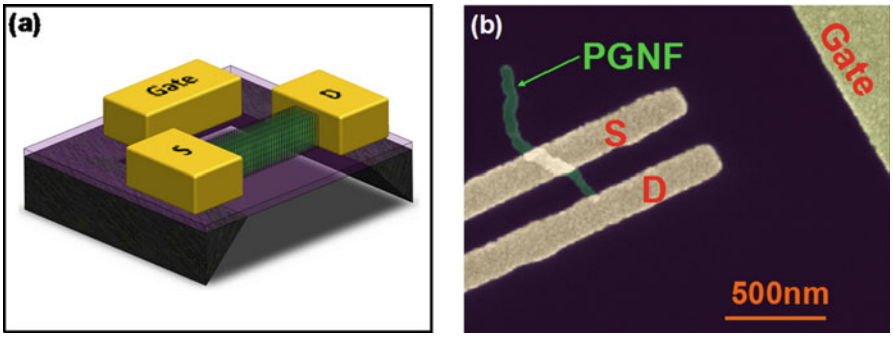

Fig. 2.12 (**a**) Schematic of side-gate PGNF device on top of a thin Si_3N_4 membrane layer. (**b**) SEM image of one of the measured PGNF devices. (Reprinted with permission from Ref. [14]. Copyright 2014, American Institute of Physics)

biasing and an amplifier circuit operated in two-terminal configuration. Figure 2.12b presents an SEM image of one of the measured PGNF devices. The fiber consisted of stacked graphene sheets (sheet size was roughly 50 × 50 nm^2). The length of the fiber between the source and drain electrodes was approximately 170 nm.

Figure 2.13 shows an image of the entire PGNF system between source and drain electrodes together with direct images and diffraction patterns of selected areas. It exhibits ordered stacking graphene layers that are perpendicular to the fiber axis, and the layer-to-layer spacing is 3.4 Å, close to the reported values [13]. However, we also observed in one region a stacking fault with an inflection (Fig. 2.13c), which is located between two perfectly aligned lattice domains [14] (Figs. 2.13e~h). The diffraction pattern of the stacking fault shown in Fig. 2.13d exhibits two lattice axes, and the intersection angle between them is simply the inflection angle. From this, the inflection angle of the stacking fault was precisely determined to be 4°. By contrast, the diffraction pattern of regular lattice domains, shown in the inset of Fig. 2.13e, exhibits a single lattice axis.

The electrical characteristics of this PGNF device were meticulously examined at low temperature. Figure 2.14a displays measured current-voltage (I-V_b) characteristics. As the temperature decreased from 300 K to 2 K, the I-V_b curves changed from a linear curve to a concave nonlinear curve, and zero bias resistance increased from 135 kΩ to 10 MΩ. In addition, the asymptote of the I-V_b curve at 2 K displayed an offset in bias voltage, indicating the presence of charging effect, which could account for the clear observation of Coulomb oscillations in current vs. gate voltage (I-V_g) dependence shown in Fig. 2.14b. At low bias voltages, the traces evidently displayed additional valleys, marked by arrows on the dip positions, along with the usual single-peak oscillation seen in single electron transistors (SETs) with a single island. As bias voltage increased from 0.4 mV to 3 mV, all additional valleys gradually smear, and the single-peak oscillation feature was recovered. Bias voltage dependence of this additional dip structure can be seen clearly in an intensity plot (Fig. 2.14c), in which differential conductance (dI/dV_b) is plotted as a function of both bias and gate voltage. The plot shows alternating large and small Coulomb

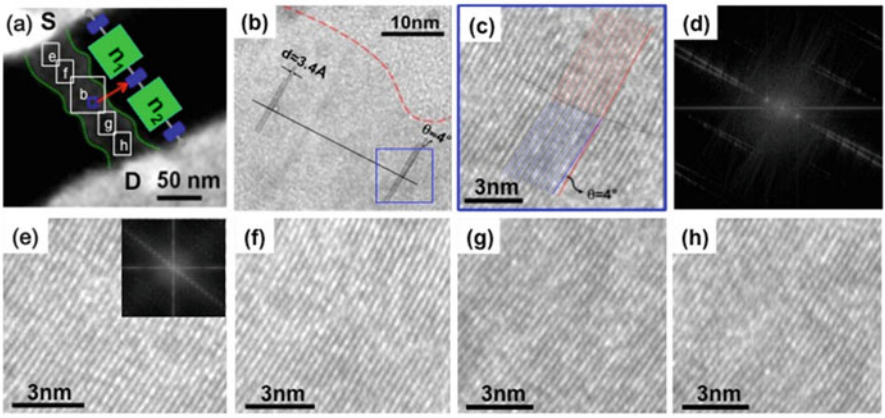

Fig. 2.13 TEM analysis on the PGNF structure of the measured device. (**a**) Image of the PGNF device between source and drain electrodes. The proposed device model is also depicted. The white letters and white frames mark consecutive TEM images in (**e**), (**f**), (**b**), (**g**), and (**h**). In (**b**), the black solid line indicates the long axis of fiber centers. (**c**) A high-resolution TEM image of the blue window in (**b**), showing a stacking fault between two perfectly aligned lattice domains. (**d**) Diffraction pattern of the stacking fault area indicated in (**c**). (**e**)~(**h**) TEM images of perfectly aligned lattice domains. Inset in (**e**) shows diffraction pattern of a perfect lattice domain. (Reprinted with permission from Ref. [14]. Copyright 2014, American Institute of Physics)

blockade diamonds, suggesting that in between the source and drain tunnel junctions, there are two islands coupled through a central tunnel junction. The apexes of the diamonds on the bias voltage axis, i.e., the onset voltage of Coulomb blockade, correspond to twice the charging energy, $2E_C = e^2/C_\Sigma$, with C_Σ as island capacitance. Accordingly, the charging energies of the two islands are $E_{c1} = 1$ mV/2 and $E_{c2} = 0.5$ mV/2 for the small and large islands, respectively. To explain the observed two-peak oscillation behavior, we constructed a circuit model consisting of two serially connected islands, as shown in the inset of Fig. 2a, which is essentially the same as the simulation circuit shown in the inset of Fig. 3a. The two islands are coupled to each other through a tunnel junction with junction capacitance C_C and connected to the source and drain electrodes through two tunnel junctions with capacitances C_S and C_D. With this model, gate voltage modulation of current-voltage characteristics was calculated using the standard master equation approach for a sequential tunneling regime [15].

For calculations, the capacitance value was estimated using a simple parallel-plate model, $C_C = \varepsilon_r \varepsilon_0 A/d$, with a dielectric constant of graphite $\varepsilon_r = 15$. From Fig. 2.13c, the thickness d of the stacking fault was estimated to be about 4 nm, and the fiber dimension A was estimated to be 50×50 nm^2. Furthermore, the two outer junctions (i.e., the source and drain tunnel junctions) that isolate the two domains

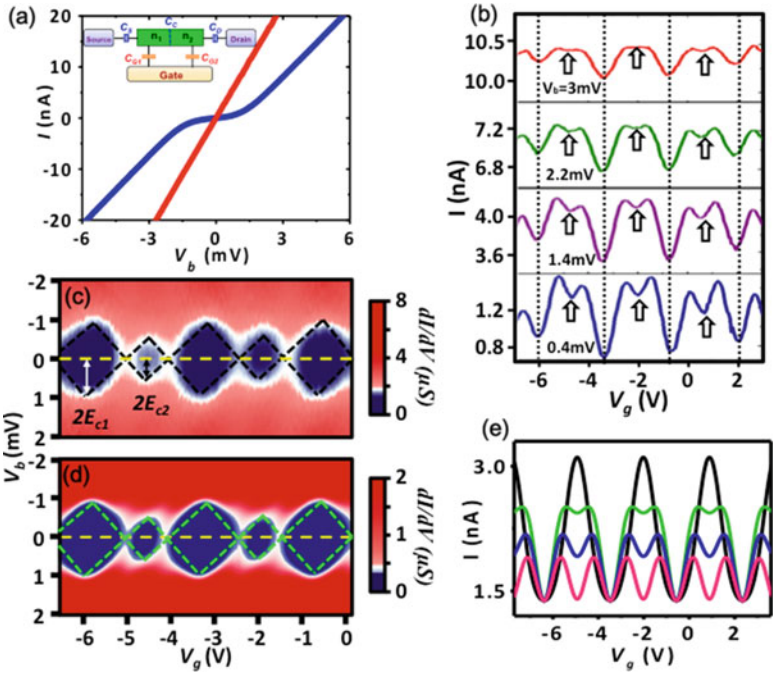

Fig. 2.14 Electrical characteristics of the double-island PGNF device. (**a**) I-V_b characteristics at 2 K (blue) and 300 K (red). Inset shows the model of a double-island SET circuit. (**b**) Coulomb oscillations at $T = 2$ K evidently showing additional valleys at the center of major peaks of lower bias voltages. The vertical dotted lines and arrows mark the position of additional valleys at different bias voltages. (**c**) dI/dV_b as a function of V_g and V_b at $T = 2$ K displaying Coulomb diamonds for two charging energies. (**d**) Calculated diamond structure at $T = 2$ K. The parameters are $C_S = 60$ aF, $R_S = 50$ kΩ, $C_D = 75$ aF, $R_D = 50$ kΩ, $C_C = 85$ aF, and $R_C = 50$ kΩ. The gate capacitances C_{G1} and C_{G2} are set to 0.055 aF. (**e**) Calculated I-V_g curves at $V_b = 2$ mV and T = 2 K for several C_C values: $C_C = 7$ aF (top) and 70 aF, 91 aF, and 175 aF (bottom). (Reprinted with permission from Ref. [14]. Copyright 2014, American Institute of Physics)

from the source and drain electrodes are considered located between the PGNF and the Ni/Au electrodes [16–18]. Junction capacitances C_S and C_D were estimated from the contact areas. The calculated diamond structure, displayed in Fig. 2.14d, shows good agreement with the measured data (Fig. 2.14c) confirming the presence of a central tunnel barrier, which electrically separates the PGNF segments between source and drain electrodes into two areas. The effect of this central coupling junction is illustrated in Fig. 2.14e, which shows the emergence of a valley structure for varying coupling strengths. This suggests the weaker the coupling (i.e., higher tunnel barrier), the deeper the current valleys.

2.4.3 *Self-Aligned Graphene Oxide Nanoribbon Stack with Gradient Bandgap for Visible-Light Photodetection*

In this work, we commence the study with a control experiment based on a suspended multi-walled carbon nanotube (MWCNT) device as shown in Fig. 2.15a, where the pristine nanotubes were placed on top of parallel metallic electrodes (see the lower inset of Fig. 2.15a). The reason we begin with the MWCNT control experiment is to illustrate that the main difference between the MWCNT and the multilayered multi-bandgap graphene oxide nanoribbon (GONR) case is that the photoresponse can be extended to a broader spectral range by unzipping the MWCNTs into GONRs with multiple bandgaps [19]. The active area of the MWCNT device is suspended in air, which eliminates the influence of the substrate on its intrinsic properties. The upper inset of Fig. 2.15a shows the corresponding transmission electron microscopy (TEM) image, which displays a MWCNT with a regular crystalline structure. The main panel of Fig. 2.15a shows the current-voltage (I-V_b) characteristics with and without illumination. Note that the two curves overlap very well, which implies the lack of photoresponse in the pristine MWCNT device. One possible reason for the absence of photoresponse from the MWCNTs could be the involvement of a metallic shell in the carbon nanotubes. Figure 2.15b shows the formation of naturally stacked GONRs via the unzipping of MWCNTs. The nanotube-to-nanoribbon transformation was assisted with microwave energy.

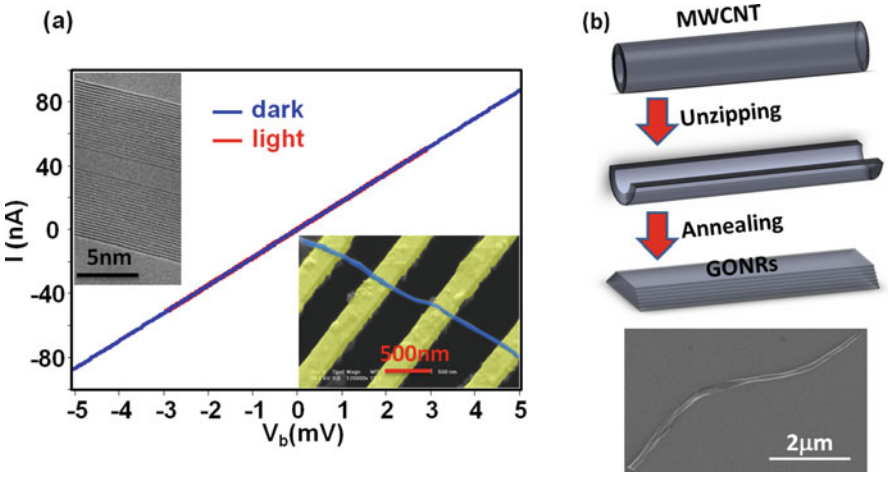

Fig. 2.15 (**a**) I-V_b characteristic for the pristine MWCNT with and without illumination. The lower inset shows the false-colored SEM image of the measured suspended device. The upper inset is the corresponding TEM image, showing a regular crystal structure. (**b**) Representation of the gradual unzipping of the MWCNT to form a multilayer GONR. The bottom SEM image pertains to one of the unzipped MWCNT samples. (Reprinted from Ref. [19], Copyright 2016, with permission from Elsevier)

Based upon a previously published method [20–22], MWCNTs were unzipped to form naturally stacked GONRs. In order to anticipate light absorption in the visible spectrum, MWCNTs with inner diameters of 2~4 nm were implemented (see Fig. 2.15a), which roughly corresponds to 10-nm-width nanoribbons ($W = 2\pi r$) that exhibit a bandgap of a few eV after unzipping. The bottom inset of Fig. 2.15b shows a scanning electron microscopy (SEM) image of one of the naturally stacked GONRs. Since many edges are present in stacked GONRs, both sides of stacked nanoribbons appear bright in the SEM image.

Figure 2.16a–e are typical TEM images of stacked GONRs samples, which reveal both the multilayer GONRs with gradually increasing widths (Fig. 2.17c) and the central planar region away from the edges (Fig. 2.17a, b). In addition, we note that there exist some GONRs with a small width in the central planar regions, as shown in Fig. 2.16d, e, in which case we expect that these narrow nanoribbons (width ≤ 20 nm) should exhibit large bandgaps ($E_g \geq 1$ eV) in the multilayer GONR structure, corresponding to visible-light spectral range absorption.

In order to confirm our speculation, we performed a correlation study between image inspection and photoelectrical characterization for each multi-bandgap GONR stack device. The GONRs were positioned on top of the Si_3N_4 membrane

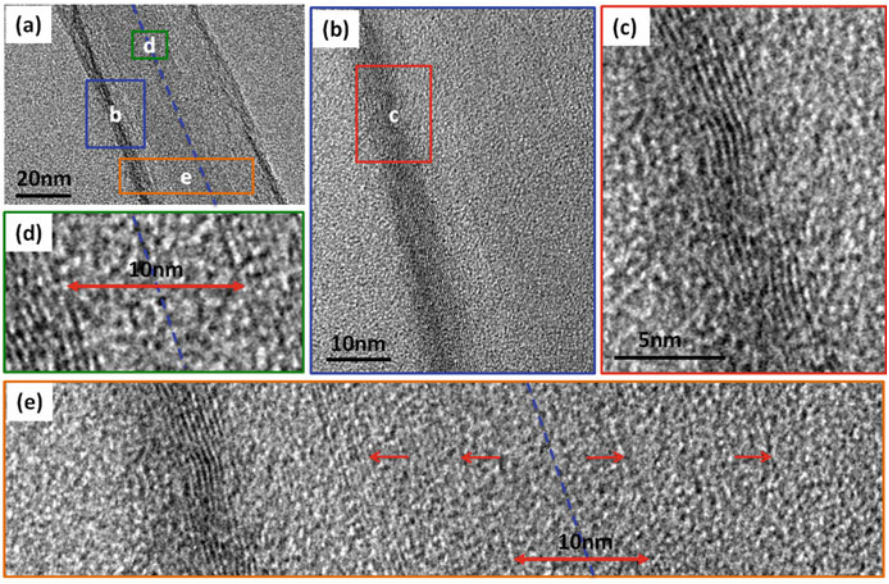

Fig. 2.16 TEM images of multilayer graphene nanoribbons. (**a**) A typical TEM image of stacked multi-bandgap GONRs. (**b**) The enlarged blue window in (**a**) shows both the edges and the central planar regions of the GONRs. (**c**) The enlarged red window in (**b**) shows a multilayer nanoribbon. (**d–e**) The enlarged green and orange windows in (**a**) show multilayer nanoribbons with various widths. Blue dashed lines in (**a**), (**d**), and (**e**) indicate the geometric axes in the multilayer GONRs. The red arrows indicate some of the multilayer GONR edges. (Reprinted from Ref. [19], Copyright 2016, with permission from Elsevier)

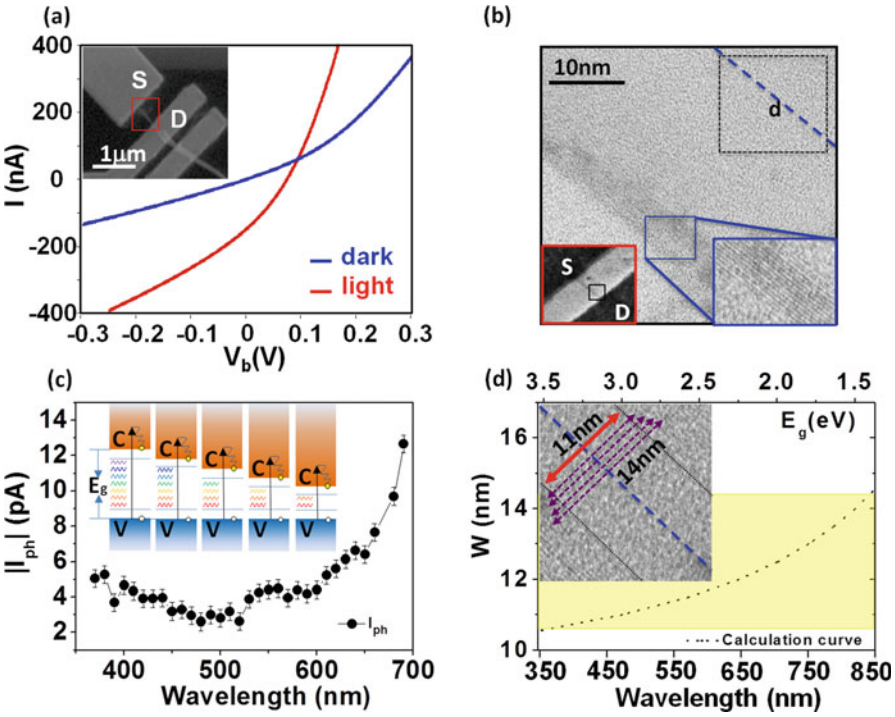

Fig. 2.17 Photoelectrical characterization of unsuspended multi-bandgap GONR photodetectors. (**a**) *I-V*$_b$ curves for the stacked multi-bandgap GONR photodetectors fabricated on top of a Si_3N_4 membrane chip under white light illumination with a fixed optical power of 1 W/cm^2, and in darkness. The inset shows the SEM image of the multi-bandgap GONR devices fabricated on top of the membrane. (**b**) TEM image of the measured multi-bandgap GONR devices, showing multilayer GNRs with gradually increasing widths. The blue dashed line denotes the geometric axis of the multi-bandgap GONRs. The inset shows the corresponding GONR device indicated by the red window in the inset of (**a**). (**c**) I_{ph} as a function of excitation wavelength at a fixed optical intensity of 10 mW/cm^2. Inset shows that multilayer graphene nanoribbons with different bandgaps absorb different spectral regions of the incident light spectrum. (**d**) The calculated relation between wavelength (e.g., bandgap energy) and the ribbon width. The inset is the corresponding TEM image of the ribbon widths marked by the black dashed window in (**b**) for the measured GONR device. (Reprinted from Ref. [19], Copyright 2016, with permission from Elsevier)

window for the membrane chip and on top of the suspended electrodes for the through-hole chip by using an SEM-based nanomanipulator [1, 23]. Nanoscaled Ni/Au electrodes deposited by standard *e*-beam lithographic technique were subsequently placed on top of the stacked GONRs for the membrane chips. The substrate effect will be discussed later when we compare these two cases (e.g., membrane versus through-hole chip). The inset in Fig. 2.17a shows two stacked GONR devices on the same membrane chip. The main panel of Fig. 2.17a displays the rectified *I-V*$_b$ curves with and without illumination for one of the multi-bandgap GONR photodetectors in which the two measured electrodes are marked by a capital *S* (source) and

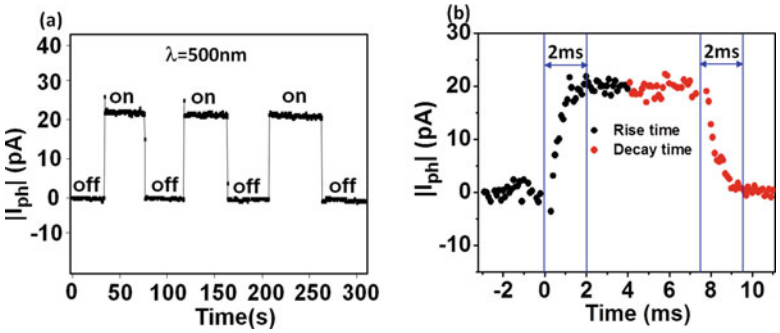

Fig. 2.18 Photoresponse of unsuspended GONR photodetectors fabricated on top of a Si_3N_4 membrane chip. (**a**) Photoswitching behavior and (**b**) photoswitching rate at $\lambda = 500$ nm and a fixed optical power of 10 mW/cm^2 in separated devices. (Reprinted from Ref. [19], Copyright 2016, with permission from Elsevier)

D (drain) in the inset. The device geometry implemented asymmetric contact areas which resulted in the rectified *I*-V_b characteristics, in contrast to the case of symmetric contacts. It is worth mentioning that similar types of structural asymmetry-induced rectification in the *I*-V_b characteristics of nanodevices with different contact areas were previously reported [24–27]. The photocurrent (I_{ph}) is the difference between the current measured in the dark condition and under illumination. Upon illumination, the stacked multi-bandgap GONR devices exhibit a significant photocurrent as shown in Fig. 2.17a. We note that since the typical breakdown current density is around 2.8×10^4 A/cm^2 at $V_b = +1$ V, the maximum applied drain bias is limited to $V_b = \pm 0.3$ V or below in this work in order to avoid electrical breakdown of our GONR devices. The TEM image of the measured multi-bandgap GONR stack device is shown in Fig. 2.18b, which clearly shows the multilayer structure with gradually increasing widths (see the enlarged region). For photocurrent generation to occur, the incident photon energy must be greater than the energy bandgap of the semiconductor. Incident photons with wavelengths corresponding to at least the energy bandgap can excite electrons from the valence band (V) to the conduction band (C) in a semiconductor as shown in the inset of Fig. 2.17c.

Since the widths of the nanoribbons slightly increase in our stacked multilayer GONR photodetectors, this results in the presence of gradually decreasing energy bandgaps in our device structure. The narrower GONRs present in the higher layers of the stacked multilayer GONR structure act as low-pass photon energy filters. Thus, a broader spectrum of incident light could be absorbed by the energy bandgaps of the individual GONRs of varying widths in our stacked multilayer GONR photodetectors. Figure 2.17c shows I_{ph} as a function of excitation wavelength at a fixed optical power without applying any bias voltages. Upon illumination in the visible spectral range, our GONR devices exhibit a photoresponse by generating a photocurrent. Furthermore, the nanoribbons which absorb excitation wavelengths larger than 500 nm primarily dominate in the generation of photocurrent. Hence, there may exist many GONRs with bandgaps ($E_g = hc/\lambda$) smaller than 2.5 eV. On the

basis of previous theoretical and experimental results [28, 29], these bandgaps should roughly correspond to GONR widths of 10 nm or wider. Figure 2.17d plots the theoretical GONR widths in terms of their corresponding bandgap energies and cutoff wavelengths. The dashed black curve is the calculated curve described by $E_{gap} = \alpha/(W - W^*)$, where we obtained $\alpha = 9$ eV nm and $W^* = 8$ nm [30]. The GONR widths ranging between 11 nm and 14 nm, highlighted in yellow in Fig. 2.17d, are the main contributors in the range of visible light. In our multi-bandgap GONR photodetectors, the corresponding image of the stacked multilayer GONR widths shown in the inset of Fig. 2.17d directly corroborates this point. The correlation between these photoelectrical results and the GONR widths observed in the TEM image strongly suggests that the visible-light absorption arises due to the presence of narrow widths in our GONRs. This result is reproducible in many devices and a similar correlation between the TEM image and the photoresponse of another stacked multi-bandgap GONR device. Furthermore, in order to study the photoswitching behavior and the photoswitching rate of our stacked multi-bandgap GONR photodetector, the rate of change of their photoresponse for I_{ph} was recorded at a fixed optical power of 10 mW/cm^2 and incident wavelength of $\lambda = 500$ nm. The stability of this switching behavior is presented in Fig. 2.18a, which clearly displays a stable ON-OFF switching behavior for I_{ph}. Moreover, the observed switching duration is quite fast. Both the rise and the decay times for the measured current are about 2 ms, as shown in Fig. 2.18b.

In order to exclude the substrate effect, the suspended multilayer GONRs were fabricated on a through-hole chip, as is shown in the inset of Fig. 2.19a. The dark regions are air gaps in which the active areas of the GONR devices are suspended. The enlarged portion of the leftmost inset of Fig. 2.19a is a TEM image of the measured device, which clearly shows a multilayer GONR structure with widths ranging from 10 nm to 14 nm. Similarly, this range of widths contributes toward absorption in the visible spectral range according to the calculated relation between wavelength (bandgap energy) and ribbon size shown in the main panel of Fig. 2.19a. Upon illumination in the visible spectral range, the suspended GONR devices exhibit a photoresponse. Figure 2.19b shows the dependence of I_{ph} on the excitation wavelength at a fixed optical power of 100 mW/cm^2. The result is similar to that in membrane chips (e.g., unsuspended case). The ON-OFF photoswitching behavior is shown in Fig. 2.19. As shown in Fig. 2.19d, I_{ph} were reproducible for various optical intensities. I_{ph} increased with increasing light intensity when plotted in a logarithmic scale (see the inset of Fig. 2.19d), indicating that it saturates at high intensities.

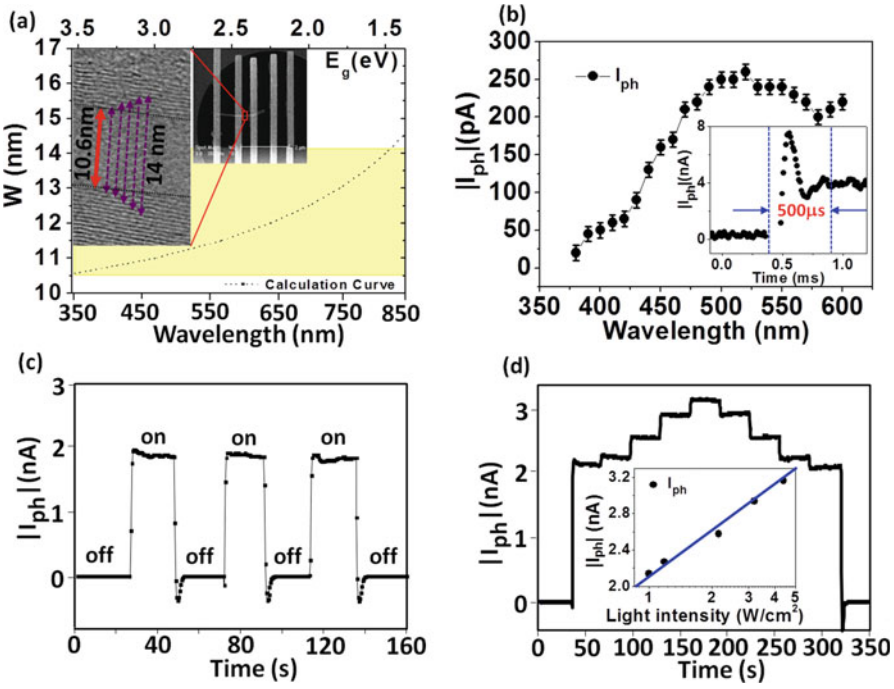

Fig. 2.19 Photoelectrical characterization of suspended multi-bandgap GONR photodetectors. (**a**) The calculated relation between wavelength (e.g., bandgap energy) and the GONR nanoribbon width. The dashed black curve is described by $E_{gap} = \alpha/(W - W^*)$ with $\alpha = 9$ eV nm and $W^* = 8$ nm. The inset is an SEM image of the measured multi-bandgap GONR device, and the enlarged image in the left is the corresponding TEM image, showing the multilayer GONR structure with gradually increasing widths. (**b**) I_{ph} as a function of the excitation wavelength at a fixed optical power of 100 mW/cm^2. The inset shows the rise time of the suspended multi-bandgap GONR photodetector. (**c**) Photoswitching behavior at a fixed optical intensity of 1 W/cm^2 and (**d**) at different optical intensities. The inset of Fig. 2.19 (**d**) shows the dependence of I_{ph} on the incident optical intensity. The blue lines are exponential fits. (Reprinted from Ref. [19], Copyright 2016, with permission from Elsevier)

2.5 Conclusion

We have successfully developed a novel method to study nanowire/nanotube/nanoribbon with a correlated study between electron microscope imaging and electrical measurements. Based on this platform, many nanomaterials could be also performed. If one can take advantages in this system and further combine with near-field scanning optical microscope, the defect issues are examined not only in TEM inspection and electrical characterization but also in optical analysis. There will be more interesting and exciting to take veil off in nanoscience and nanotechnology.

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Chapter 3
Properties Engineering of III–V Nanowires for Electronic Application

Sen Po Yip, Lifan Shen, Edwin Y. B. Pun, and Johnny C. Ho

3.1 Introduction

Semiconductors have been the core materials of many technological advances in recent years. Silicon, the most studied and used semiconducting material, has been the center of semiconductor industry for decades because it is available abundantly and easy to dope, and silicon dioxide is a superior dielectric material in microelectronic industry. This material can be used to make computer chips, optoelectronics devices, and solar cell. Silicon reshapes the way we live and is unarguably one of the most important materials in modern society. Through its dominant role in the semiconductor industry for now, the search for alternatives is fueled by the unstoppable demand for high-performance and low-power electronics. Among different kinds of semiconductors, III–V semiconductor holds promising properties for replacing silicon, and in particular, the NW structure of III–V semiconductor has been studied extensively.

Nanowire is a nanostructure with high aspect ratio (length-to-width ratio, usually over 1000), and the diameter is in the nanometer range. Materials with such dimensions exhibit different properties compared to their bulk counterparts due to the quantum confinement effect. The electrons are confined in two dimensions and cause them to occupy in quantized energy levels that are different from the traditional continuous energy band in bulk form. Different kinds of applications arise from this nanostructure based on their unique properties, such as field-effect transistors (FETs), sensors, energy harvesting, and thermoelectric applications. This book chapter focuses on presenting the strategies in engineering the electrical properties of III–V NWFETs.

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3.1.1 Synthesis of Nanowires

To make use of the NW for different applications, understanding the fabrication process of NWs is very important. Basically, NW fabrication can be divided into two categories, bottom-up approach and top-down approach, regardless of the materials. The fabrication method determines how the device is fabricated and be further engineered. Here, both methods are briefly described below, and for a more extensive review readers can refer to Ref. [1].

3.1.1.1 Bottom-Up Approach

Bottom-up approach is the synthesis of NWs by their constituent atoms. The NW growing process might involve gases or liquids. The source of reactant used to grow the NW is similar to that of growing thin film. Special strategy is needed to confine the growth in only one dimension. One method is to use metal cluster as the catalyst. For example, vapor-liquid-solid (VLS) method is one mechanism for growing NW in chemical vapor deposition (CVD) using metal cluster catalyst. In this method, the source of the constituent atoms of NW is in gas phase (vapor), and the catalyst is in liquid phase (liquid). The source is absorbed in the catalyst until the supersaturation level is reached. By then, the NW (solid) grows at the catalyst-substrate interface and propagates in that direction. Another similar mechanism is vapor-solid-solid (VSS), in which the catalyst is solid phase during the NW growth. Other mechanism like vapor-solid (VS) and oxide-assisted growth (OAG) do not require the existence of catalyst, but diameter control becomes more challenging. Another method is to use prefabricated template such as anodic aluminum oxide (AAO) membrane to guide the NW growth. Manipulating the pore size of the AAO can control the diameter of the NW, but the template needs to be removed after the NW growth. A wide range of NWs, such as Si, Ge, III–V, oxide, and chalcogenides, can be grown using this bottom-up approach.

3.1.1.2 Top-Down Approach

Top-down approach is a simple and relatively straightforward method that involves material removal from a thin or thick film. Patterning is needed prior to the NW synthesis in order to define the shape and dimension. Material removal is done by chemical etching or plasma etching. One example is metal-assisted chemical etching (MaCE), which uses metal film as the catalyst to etch the substrate, say, silicon, anisotropically in order to create high aspect-ratio structure. Compared to the bottom-up approach, the top-down approach gives better control on the shape and dimension. The major challenges are the resolution limit of the diameters and the high facility cost.

3.1.2 Applications of Nanowire Field-Effect Transistor

Among all the versatile device applications of NWs, FETs are the fundamental building blocks in the next generation of nanoelectronics. FET is a three-terminal device, which consists of a source, a drain, and a gate. Electrons flow through the transistor from the source to the drain, and the gate is used to control/modulate the current flow. Transistor based on silicon has been the central part of CPU and is the leading force of technological advance in the last decade. Here, several applications are briefly introduced.

3.1.2.1 Integrated Circuit

Transistor is the central unit of an integrated circuit (IC) and is used as a switch. Complementary metal oxide semiconductor (CMOS) technology, consisting of p-type and n-type transistors, is used in constructing the core of CPU. In the near future, driven by the emergence of the demand of cloud computing, big data analytics, and Internet of Things (IoT), the computing power demand will surge, and the need for high-speed, high-performance, and low-power electronics will only rally and never stop.

3.1.2.2 Photodetector

Semiconductor like III–V material has a direct bandgap, and the energy bandgap varies from infrared (like InAs and InSb) to visible (GaAsP) to UV (GaN) wavelengths. Their NW counterpart has been studied as a building block of photodetector. The advantages of using NW for photodetector are (1) longer photocarrier lifetime due to the deep-level trap states on the NW surface and the large surface-to-volume ratio and (2) shorter carrier transit time due to the reduced dimensionality of the active area [2]. Another advantage is that the bandgap can be engineered by compositional engineering. FET photodetector is a transistor that is light-sensitive; thus, channel current can be amplified when the conducting channel is exposed to light (or other EM waves), since "hot electrons" are created and injected into the conducting channel, and the response is enhanced. Such a device usually needs an electrical gate bias to separate the excited electron-hole pairs created and to improve the carrier recombination lifetime and the sensitivity.

3.1.2.3 Biosensor

FET can be utilized as a biosensor to sense the biomolecule in fluid system. The conducting channel of the FET must be sensitive to the target molecule so that when the molecule are attached to the channel, the channel conductance or resistance

across FET is modulated, i.e., the electrical performance changes, by either (1) functionalizing the channel or (2) replacing the gate electrode by a gate dielectric, an electrolyte, and a reference electrode.

3.1.3 NWFET Structure

The most advanced computer chip we used nowadays is called FinFET, which is a non-planar transistor. It is envisaged that the gate-all-around (GAA) transistor will replace the FinFET technology in the future. (According to ITRS 2.0, More Moore Chapter, lateral GAA transistor is expected in 2019, and vertical GAA transistor is expected in 2021.) The advantages of GAA configuration are better electrostatic control, and hence lower leakage and lower power consumption compared to other gate configurations. NW makes a perfect candidate for GAA device fabrication. The GAA structure would be the final gate structure to scale down the channel length to the shortest possible gate length. Here, both vertical and lateral GAA structure is discussed.

3.1.3.1 Vertical Nanowire FET

Vertical NW with precise diameter and position control are possible and are controlled by lithography and followed by top-down or bottom-up approach of NW synthesis. The source, drain, and gate can be aligned on the same vertical axis along the NW to fabricate the FET. The emergence of such device structure is to reduce the registration of a FET and hence increase the integration density when there is no more room left to reduce the gate length. A gate-all-around gate configuration is commonly used which is important for future high-performance electrical device. For bottom-up NW, the integration of such device structure remains challenging since the circuit design for large-scale integration on a chip is complicated. For example, if the growth substrate is needed to be utilized as the source, the circuit designs and fabrication processes would become very complex. Also, such processes might not be compatible with the existing horizontal device structure fabrication process and require new tools [3].

3.1.3.2 Horizontal Nanowire FET

Horizontal integrated device structure is the common device structure used in semiconductor industry; hence horizontal NWFET might be more suitable for the next-generation electronic integration in the near future without redesigning chip architecture and reinventing the well-established processing technology. However, the integration of NWs remains a challenge. Top-down NW is compatible with the current chip fabrication technology but might be damaged by the complication and the high cost of lithography and etching technique for ultrascale dimension.

On the other hand, NW grown by bottom-up approach can be transferred on to foreign substrate by methods like contact printing, differential roll printing, electric field-assisted orientation, and so on. However, none of these methods can achieve precise controlled and orientated NW arrays or have very long integration times with other sacrifices. (For a more detailed review on the transfer technique, readers can refer to Ref. [4].) One worth noting technique called the selective lateral epitaxy (SLE) [5, 6] can grow III–V NWs on semi-insulating GaAs (100) substrates horizontally and be used to fabricate MOSFET directly without transferring. Although extensive efforts on growth optimization are still required, the technique might be applied for the next-generation device integration.

3.1.4 Advantages of III–V Compound Semiconductor NWs

Due to the ever shrinking in transistor size, silicon will eventually be replaced by other semiconductors. Among different kinds of semiconductor NWs, III–V compound semiconductor NWs have attracted extensive amount of research and development interest due to their excellent physical properties for high-performance nanoelectronics and highly efficient photovoltaics over the last decades [7–16]. Compared with group IV 1D nanostructures, such as Si NWs and CNTs, many III–V NWs exhibit impressive higher intrinsic carrier concentration and mobility for better-performance and high-speed devices that cannot be easily achieved in silicon and other nanostructures [17, 18]. Furthermore, some III–V NWs have larger bandgap which allows operations of power devices at higher temperatures and have lower thermal noise to low-power devices at room temperature. Most III–V NWs have direct bandgap that can be manipulated over a wide range of energy by tailoring their stoichiometry and providing them with better optoelectronic properties compared to indirect bandgap silicon. Due to their inherent mechanical flexibility and optical transparency, III–V NWs have been considered as ideal active materials for high-performance flexible electronics in the development of next-generation display technologies, including "see-through" and conformable products [19–25]. Besides, their remarkably large surface-to-volume ratios make NWs attractive for high-performance sensors. The fascinating combination properties of III–V NWs, such as their high carrier mobility, tunable direct bandgap, excellent mechanical flexibility, and extraordinarily large surface-to-volume ratio, make them ideal and superior candidates for the next-generation electronics, photonics, and sensors and even possibly on flexible substrates.

3.1.5 Requirement on Properties Engineering

Although III–V NWFETs hold promises for the realization of the next-generation nanoelectronics, efforts are still needed on further improvement of NWFETs. Thus,

it is important to understand the electronic properties of these transistors, where photolithographic or e-beam lithographic processing is utilized to define the source/drain contacts, and a top- or back-gate configuration is used to control the electrostatic potential of the active NW channels. In order to further improve the electronic properties of III–V semiconductor NW devices and realize different applications, it is crucial to have rational control of the surface, the contact, and the crystal properties. All these properties might have significant impact on the electrical performances. A brief description of the impact is given below:

(a) Surface: The surface of some III–V semiconductor NWs, such as InAs, are sensitive to ambient due to the large surface-to-volume ratio and the existence of electron accumulation layer, and exposing the NW devices to ambient has negative effect on the electrical performance of the NWFETs, such as hysteresis and negative V_{th} shift.
(b) Contact: The quality of the contact interface of NWFETs affects the total resistance of the transistor and has an impact on the power consumption and the device performance at high frequency.
(c) Crystal quality: The crystal quality of III–V NWs can significantly affect the electrical performance of NW devices. The crystal phase, the crystal orientation, and the crystal defect have a big influence on the transport property of the device. Therefore, crystal manipulation provides a way to control and manipulate the electrical performance of NW devices.

The purposes of the following sessions focus on how to engineer the quality of the surface, the contact, and the crystal properties and also, in some cases, how the techniques can be used to control the electrical properties and, thus, give new functionalities to the III–V NWFETs.

3.2 Surface Modification

One of the most distinguished features of NWs is its high surface-to-volume ratio, that is, with its smaller diameter, more atoms are exposed to the ambient. Hence, the surface becomes more sensitive to nearby surrounding which opens up a way to control the band structure of the NWs. To understand the surrounding effect on the NW, the equation of space charge depletion can be considered,

$$W = \left(\frac{2\varepsilon\varphi}{en}\right)^{\frac{1}{2}} \tag{3.1}$$

where W is the depletion layer thickness, ε is the dielectric constant of the material, φ is the surface potential, and n is the electron concentration. When a large surface potential is built up, a thick depletion layer is created.

Consider a cylindrical NW with 50 nm in diameter, if a 5 nm depletion layer is created around the circumference by a surface potential which leaves an undepleted core with 40 nm in diameter. That is a total 36% of the NW volume is now depleted. This would have an impact on the surface band structure and hence the electrical performance of the NWFET.

The surface potential can naturally occur. For III–V materials, the surface tends to form a thin layer of native oxide. The bonds of the surface atoms are usually not saturated, i.e., surface dangling bonds are formed which are sensitive to environment and will react with other substance like oxygen. The surface of nearly all bulk III–V compounds contains high density of surface states. The surface states, however, act as nonradiative recombination centers or surface charge traps that add more undesirable states in the band structure and pin the Fermi Level. In most III–V compounds except InAs, the surface states pin the Fermi Level within the bandgap and act as acceptors [26]. For InAs, the surface states are donor-like, and the Fermi Level is pinned above the conduction band. These pinned structures create charge accumulation region. Such effect can be used to engineer the transfer properties of the NWFET. For example, for thin GaAs NWs, such surface states deplete the NW channel, and the NWFET exhibits p-type behavior compared to its n-type thicker counterpart [27].

The high densities of the ionized surface states could also hamper the electrical performance of NWFET especially for InAs due to the ionized donor surface states [28]. The donor states form a conduction channel on the surface and are hard to deplete. The movement of free carriers near the surface is restricted. Also, it complicates the gate coupling and lowers the transconductance [29]. The setbacks also give rise to lower mobility [30] and poor subthreshold characteristics and increase hysteresis [31]. To enhance the performance of III–V NWFET, it is necessary to reduce the surface states.

On the other hand, surface potential can build up when the NW surface is in contact with foreign species such as nanoparticles, molecules, or thin films. When the species and the semiconductor have different work functions, the charge transfer creates surface potential. Controlling the species properties allows the precise controlling of the electrical properties of the NW devices and, more importantly, improving the electrical performances and potentially adding further functionalities.

In this chapter, we present several reported methods and the corresponding ideas on how to passivate and modify the III–V surface in order to engineer the electrical properties.

3.2.1 Molecular Passivation

As native oxide introduces negative impact on the electrical performance of III–V NW devices, removing this layer is a sensible way to improve the device performance. However, the surface of III–V compound is so reactive that reoxidation takes

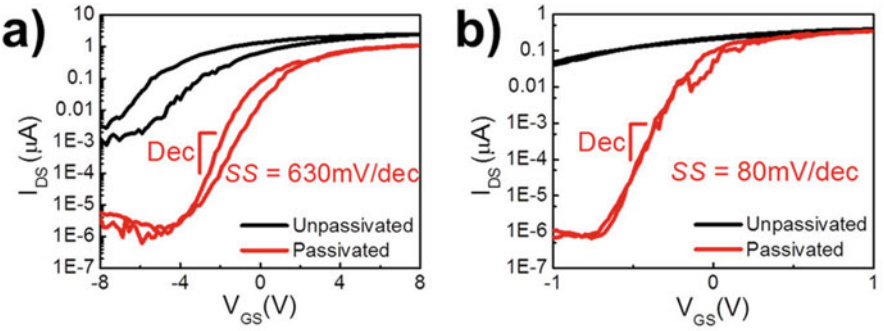

Fig. 3.1 Transfer characteristic of the InGaAs (**a**) back-gated and (**b**) GAA NWFET with and without passivation in logarithmic scale at $V_{DS} = 0.1$ V. (Reprinted with the permission from Ref. [35]. Copyright 2015 Nature Publishing Group)

place in short duration right after native oxide removal. To achieve a stable surface, the native oxide surface must be removed and followed by surface stabilization, i.e., passivation, immediately. Thus, molecules can be used to saturate the surface bonds of the III–V materials.

In bulk III–V semiconductor, passivating the surface by sulfur-containing molecules is well-studied and is universal to all III–V semiconductor [32]. This technique employs sulfur atoms to saturate the surface dangling bonds. For NW, sulfur-containing molecules like 1-octadecanethiol (ODT) [33] and ammonium sulfide ($(NH_4)_2S$) [34, 35] have been studied in passivating the conduction body of the back-gate, the top-gate, and the gate-all-around (GAA) transistor configuration. The benefits of passivating the NW by sulfur-containing molecules are lower off current, steeper subthreshold slope, improved electron mobility, and moving the subthreshold voltage to the positive side (Fig. 3.1). It is worth noting that the passivation effect of $(NH_4)_2S$ on GAA configuration of InGaAs NWs in both reports [34, 35] have shown a close to theoretical subthreshold slope (~60 mV/dec). A sufficiently low subthreshold slope is important for low-power electrical device.

In another study, using aromatic thiolate (ArS^-)-based molecular monolayers, Cheung et al. controlled the threshold voltage (V_{th}) of InAs NWFET by varying the para-substituent of the aromatic ring (Fig. 3.2a) which can be electron-withdrawing (Fig. 3.2b) or electron-donating (Fig. 3.2c) [36]. In the study, the surface oxide of the InAs NW is removed in diluted HF and put in a passivation agent for 12 h. After passivation, the electron mobility of the InAs NWFET is improved, and the OFF current is lowered which can be attributed to the passivation of the surface dangling bonds. Also, the ArS^- with electron-withdrawing para-substituent can significantly shift the V_{Th} toward the positive region (Fig. 3.2c). More importantly, it shows the ability of controlling the V_{Th} by tailoring para-substituent group of the sulfur-containing long-chain molecules, confirming that it is a promising technique in both improving and engineering the NWFET performance.

The surface passivation can also be done in in situ manner. In recent reports, Yang et al. reported using sulfur as surfactant during the growth of very thin and

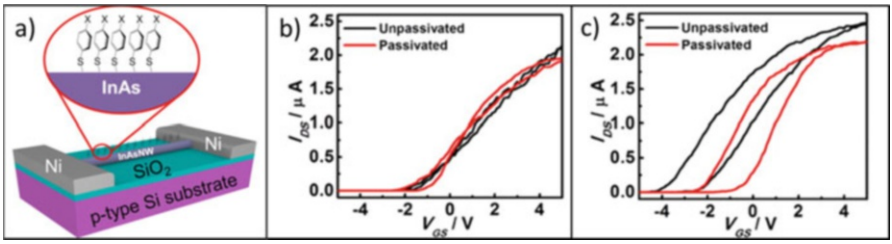

Fig. 3.2 (**a**) Illustrated schematic of InAs NWFET passivated by ArS^{-}. (**b**, **c**) Transfer characteristic of the InAs NW passivated by p-methoxythiophenol and p-nitrothiophenol, respectively. (Reprinted with the permission from Ref. [36]. Copyright 2015 American Chemical Society)

uniform GaSb NWs by surfactant-assisted CVD [14, 37]. Growing thin GaSb NWs is known to be challenging due to the higher group III content required in the catalyst and the surfactant effect of Sb [38]. Also, the Ga vapor will react with the surface unsaturated antimony atoms and causes undesirable radial growth (Fig. 3.3a–c). In the report, the sulfur atoms form stable chemical bonds with unsaturated antimony atoms on the surface and also limit the radial growth of the NW body (Fig. 3.3d–f). Using the sulfur surfactant not only improves the morphology of the NWs but also improves peak hole mobility up to ~400cm^2 V^{-1} s^{-1} approaching the theoretical limit. Achieving high-performance p-type transistor has important implication because good mobility p-type III–V material is rare.

3.2.2 Metal Cluster Decoration

Engineering the electrical properties of semiconductor by metal cluster decoration has been studied in materials like graphene [39], MoS_2 [40, 41], metal oxide [42–44], and so on for various applications such as transistor and photodetector. By decorating the semiconductor surface with metal clusters, the difference between the work functions of the semiconductor and the higher work function of the metal cluster (e.g., 5.31–5.47 eV for Au depending on the orientation) creates a localized Schottky junction and withdraws the electron from the semiconductor, i.e., the work function and electron concentration of the semiconductor are reduced by the charge transfer. The technique has been used to push the V_{th} to enhancement mode in transistor and also enhance the photosensitivity of the photodetector.

There are only few reports on properties engineering by decorating III–V NW with metal cluster. Han et al. have used this technique to modulate the V_{th} of InAs, InGaAs, and InP NWs transistor [9]. In the study, metals with high work function (Au) to low work function (Al) were selected to be deposited on the NW surface. When Au particle is used electrons are withdrawn from the InAs NW, and the V_{th} is positively moved to the enhancement mode which is desirable in reducing the overall power consumption of the circuit design. On the other hand, when Al particle

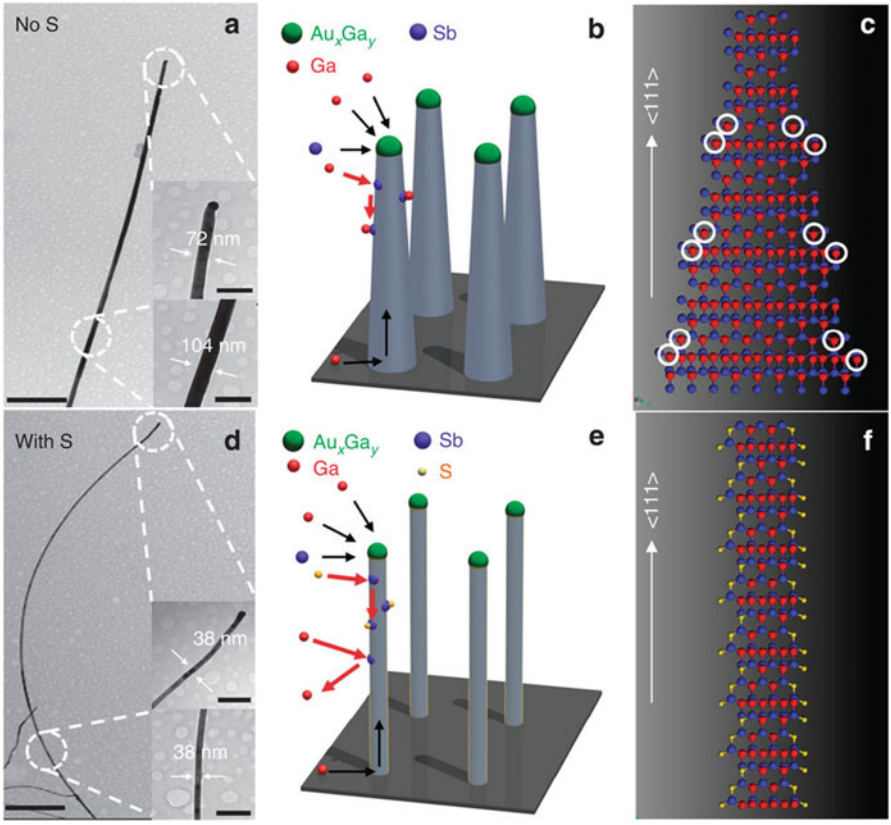

Fig. 3.3 (**a**, **d**) TEM image of GaSb NWs without and with surfactant growth (all scale bars are 200 nm in the inserts). (**b**, **e**) Schematic illustration of the atom movement during NWs growth without and with surfactant. (**c**, **f**) Atomic modeling schematic of resulting NWs without and with sulfur-terminating surface. (Reprinted with the permission from Ref. [14]. Copyright 2014 Nature Publishing Group)

is used, since Al has a lower work function (4.0–4.26 eV), the electrons are donated to the InAs NW. Hence, the *on*-current is enhanced, and the V_{th} is negatively shifted which confirms the versatility of this technique.

In another report, Miao et al. demonstrated similar result (Fig. 3.4a, b), but more importantly, when metal cluster-decorated InAs NW is used to fabricate photodetector, the photoresponsivity of the Au-decorated InAs NW photodetector is 300% higher than the original one (Fig. 3.4c) [45]. This is because the built-in electric field created by the contact to the Au cluster and the InAs NW can suppress the recombination rate of photo-generated electron-hole pairs.

Unfortunately, the study of applying this technique on III–V NW device is still limited. In other material systems, this metal cluster decoration technique has also been used in applications in, e.g., sub-ppm-specific In_2O_3 NW gas sensor due to the

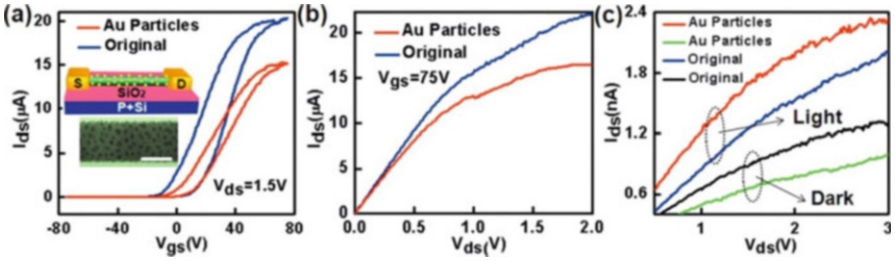

Fig. 3.4 The (**a**) transfer and (**b**) output characteristic of 1 nm Au nanoparticle-decorated InAs NWFET. The scale bar in the insert of (**a**) is 30 nm. (**c**) Photoinduced change in output characteristic of InAs NWFET. (Reprinted with the permission from Ref. [45]. Copyright 2014 American Chemical Society)

selective sensitivity of certain metal to certain gas [46] and plasmon FET for optoelectronic application due to the plasmon resonances of Au nanoparticles and ZnO thin film [44]. The method is expected to be useful for sensor application when coupled with III–V NWs.

3.2.3 Surface Coating

The surface of some III–V NWs (e.g., InAs) is very sensitive to ambient due to the large surface-to-volume ratio and the existence of electron accumulation layer. When molecules are adsorbed onto the surfaces, the conductance of the NW device is changed by the "floating gate" effect which is associated with the change of surface charge and state, gate potential, local work function, band alignment, gate coupling, and/or carrier mobility [47]. Several reports show that InAs NWs are capable of gas sensing [48, 49]. However, exposing the NW device to ambient was also reported to have negative effect on the electrical performance of InAs NW transistor. For example, H_2O molecules can increase the hysteresis and negatively shift the V_{th} of an InAs NWFET (Fig. 3.5) [50].

3.2.3.1 By Thin Dielectric Layer

One simple and straightforward way to prevent the adsorption is to use a thin high-k oxide film to physically isolate the NW surface from the ambient. Han et al. used a 20-nm e-beam-evaporated Al_2O_3 layer to suppress the hysteresis without any significant changes in mobility [9]. On the other hand, 10 nm of atomic layer deposition (ALD)-prepared HfO_2 thin film was deposited on InAs NWFET by Miao et al. [45]. The HfO_2 passivation layer can minimize the hysteresis and improve the mobility by isolating the InAs NWFET from ambient. Also, during the ALD process, the InAs NW surface states are removed by surface reaction [51–53]. As

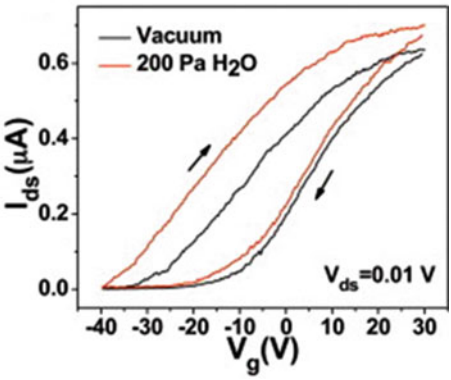

Fig. 3.5 The transfer characteristic of In_2O_3 NWFET measured under vacuum (black line) and in 200 Pa H_2O (red line). (Reprinted from Ref. [50], Copyright 2015, with permission from Elsevier) (Color figure online)

ALD has already been used in semiconductor industry, such technique is totally compatible with in-chip fabrication process.

3.2.3.2 Core-Shell Nanowire

Radial heterostructures, or core-shell structures, are another method to physically isolate the NW surface from surrounding environment. The motivation of developing such structures is to passivate the sidewalls of the core materials. GaAs-AlGaAs NW is one of the most studied core-shell heterostructure, and the GaAs core is passivated. GaAs has higher mobility than silicon, making it an attractive candidate to replace silicon in chip fabrication. Also, the direct bandgap of GaAs makes it an ideal replacement for the indirect bang gap silicon for optoelectronics application due to its effectiveness in light absorption. The issue of GaAs NW is the surface accumulation layer pins the Fermi Level and forms a depletion layer. Hence, the electron mobility is low (usually lower than 1500 $cm^2\ V^{-1}\ s^{-1}$) [54–57]. Also, the surface recombination velocity is extremely high (10^5–10^6 cm/s), and the carrier lifetimes are extremely short (few picoseconds) compared to other III–V materials [54, 56, 58]. To overcome this issue, wider bandgap semiconductor such as AlGaAs is grown on the surface of GaAs. With careful adjustment of the shell thickness, the scattering rate is drastically reduced (Fig. 3.6a) [59]. The electron mobility can also increase as high as 3000 $cm^2\ V^{-1}\ s^{-1}$ which is about 65% of that of typical high-quality undoped bulk GaAs (Fig. 3.6b) [59]. The photoconductivity lifetime is also increased to the nanosecond range, reaching 1.6 ns. Such a core-shell structure can be further developed into a core-multishell structure and utilized as a single NW photodetector which shows impressive peak photoresponsivity of 0.57 A/W [60]. Combined with Si delta (δ)-doping process, the core-shell NWFET shows high low-temperature field-effect mobilities of up to $5 \times 10^3\ cm^2\ V^{-1}\ s^{-1}$ with low subthreshold slopes of 70 mV/dec and on/off ratios of $> 10^4$–10^5 at room temperature [61].

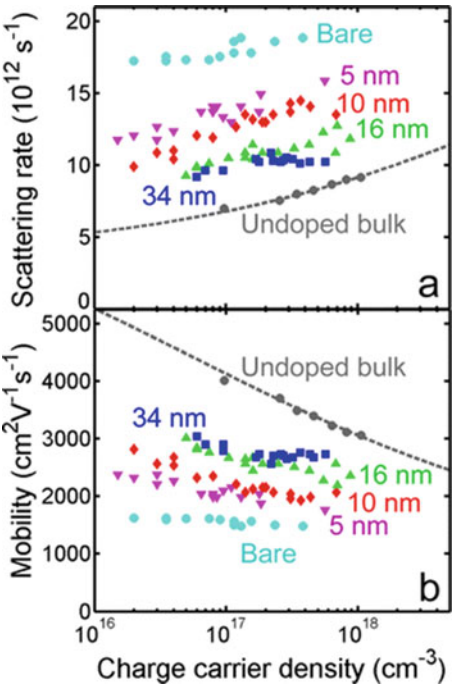

Fig. 3.6 The relation between shell thickness of AlGaAs in GaAs-AlGaAs-GaAs core-shell-cap nanowire to the (**a**) scattering rate and (**b**) room temperature mobility. (Reprinted with the permission from Ref. [59]. Copyright 2014 American Chemical Society)

Another most studied III–V core-shell structure is InAs-InP NW. As repeatedly mentioned in this chapter, the surface states do hamper the electronic properties, and capping it with thin InP layer does efficiently enable surface passivation of the InAs NW and leads to the formation of high-mobility NWFET. The conduction band offset of InP (~0.52 eV) confines the electrons in the type-I quantum well structure. By capping the InAs surface with 2–3 nm InP epitaxial shell, a high field-effect mobility of 11,500 cm^2 V^{-1} s^{-1} can be achieved at room temperature [62]. With 0.5–1 nm InP epitaxial shell, the low-temperature (2 K) field-effect mobility increased by 2–5 times compared to bare InAs NW and some even exceeding 20,000 cm^2 $V^{-1}s^{-1}$ [63].

The two examples given above do show that the core-shell structure improves the overall performance of NWFET or detector drastically, and more core-shell structures are being extensively studied, and we believe that this approach will be important for future applications.

3.3 Contact Engineering

When considering a transistor device, the total resistance is the sum of the resistance of the conduction channel as well as the resistance of the contact area (i.e., contact resistance) in a simplified model

$$R_{\text{total}} = R_{\text{channel}} + 2R_{\text{contact}} \tag{3.2}$$

To fabricate high-performance transistor, the total resistance should be kept as low as possible in order to reduce the power consumption.

The channel resistance of the NW is

$$R_{\text{channel}} = \frac{\rho L}{\pi r^2} \tag{3.3}$$

where ρ, L, and r are the specific resistivity, length, and radius of the NW channel, respectively. Hence, the Eq. (3.2) becomes

$$R_{\text{total}} = \frac{\rho L}{\pi r^2} + 2R_{\text{contact}} \tag{3.4}$$

With size shrinking of the device on a chip, the channel resistance also decreases with the channel length. When the feature size of transistor is pushed to sub-10-nm range, the role of the contact resistance becomes important and requires consideration.

To lower the contact resistance, one has to understand the metal-semiconductor junction. There are three types of junctions, ohmic junction, Schottky junction, and tunnel junction. The type of junction depends on the band alignment. The simplest model to predict is using the equation $\phi_b = \phi_M - \chi$ where ϕ_b is the barrier height, ϕ_M is work function of the contact metal, and χ is semiconductor electron affinity. In general, ohmic contact is formed when the electron affinity of the semiconductor is higher than the work function of the contact metal, i.e., $\chi > \phi_M$, for n-type semiconductor, and $\phi_M > \chi$ for p-type semiconductor. Ohmic contact provides low-resistance contact for electrons to transfer into the transistor and is desirable for device fabrication.

On the other hand, Schottky contact is formed when $\phi_M > \chi$ for n-type semiconductor or $\chi > \phi_M$ for p-type semiconductor. The formation of a large barrier height and a depletion layer increase the contact resistance. Despite the contact having higher resistance, Schottky junction does have applications in PV devices and optical sensors. When the ϕ_b is high and the depletion layer is thin enough, electrons can tunnel through the barrier with considerably low-contact resistance and do have its own unique application. Therefore, studying the formation of contacts is important for device applications.

Theoretically, to efficiently achieve an ohmic contact or a Schottky contact, one can choose contact material with the right work function. However, the quality of the contact area can significantly affect the electrical performance of a device. In general, for silicon the contact quality can be improved by increasing the doping level and the effective contact area and the lowering of the barrier height [64]. For III–V materials, the high density of surface states usually forms a charge accumulation layer on the surface, and the pinning of the position of the Fermi level depends on the material property. For example, the Fermi level of InAs is pinned above the

conduction band minimum, enabling easy realization of ohmic contact [65]. However, such pinning effect may have negative effect on the electrical performance. To achieve high performance, such a charge accumulation layer at the contact region must be passivated before metallization, especially for one-dimension III–V nanostructure, because the high surface-to-volume ratio makes the negative effect more profound.

In the following sections, several schemes on engineering the properties of the contacts are discussed.

3.3.1 Contact Treatment

Since the native oxide is harmful to the contact quality, one straightforward solution is to remove the oxide and stabilize the surface as discussed in the previous surface engineering section. The native oxide can be removed by treating the contact area in inorganic acid such as HF or HCl. However, immediately after the surface layer is removed, the core of the III–V material might be reoxidized when exposed to ambient, and once again a charge accumulation layer is formed. Another method is wet chemical etching with sulfur-containing molecules. For example, utilizing ammonium polysulfide, $(NH_4)_2S_x$, water solution, which is made by adding extra elemental sulfur to the original $(NH_4)_2S_x$ (20%) solution, as an etching agent to remove the native oxide before metallization, is quite effective in lowering the contact resistance. The sulfur atoms form covalent bonds with the surface and provide short-term stability against reoxidation in air and aqueous solution before metal deposition.

For InAs NW, untreated NWs give high-contact resistivity because the contact area is covered by native oxide [66]. Contact treatment with diluted $(NH_4)_2S_x$ has been used to etch the contact area to form ohmic contact before metallization [67]. Using undiluted ammonium polysulfide solution is not practical due to the high etching rate. For bulk materials, some material removal is acceptable due to the large dimension. For NW structure, high etch rate leads to smaller cross-session and hence higher contact resistance. Demonstrated by Suyatin et al., a highly diluted solution (about 2% or less) gives negligible etching effect and high yield of ohmic contact, with a contact resistivity below 10^{-2} Ω cm [67]. The contact resistivity increases after exposing the device in air for 2 weeks and is probably due to the oxidation of the contact area. The resistivity stays stable after storing for 1 month in vacuum. Isolating the device from ambient by, for example, surface coating should help to maintain the contact stability.

The wet etching method can also be used to form a p-n junction on p-type InAs NW [68], since sulfur can be used as n-type dopant on the local surface of p-type III–V material [69]. With sufficiently high doping level, the p-n junction and also a tunnel junction can be utilized as a backward diode, or Esaki diode. Without further treatment, the peak-to-valley current ratio (PVCR) of the device reaches 9.2 and is

the highest reported value for NW-based tunnel diodes to date. The study demonstrates a promising doping technique to engineer the contact property.

Another straightforward solution to deal with the contact interface is to remove the native oxide without allowing the NW to reoxidize, that is, removing the oxide layer in vacuum before metallization. Argon milling before metal deposition has been employed to minimize the contact resistance [70]. The process allows both the oxide removal and the metal deposition in the same chamber without breaking the vacuum. It was found that in situ argon milling process effectively removes the native oxide without reoxidation. The specific contact resistance of the contact interface treated by argon milling is an order of magnitude lower compared to wet etching by $(NH_4)_2S_x$ and three order of magnitude lower compared to untreated interface.

3.3.2 Nickelide Formation

Low-resistance local interconnect becomes a critical issue for industry as the feature size of transistor keeps shrinking. For silicon, the formation and electrical properties of metal silicides has been extensively studied [71]. The benefits of using such a technique are low-contact resistance, good process compatibility with silicon, and formation of good contact with other metals. For III–V materials, a silicide-like metallization process is rarely reported. Nickel is one of the few reported materials that can form stable metallic phase with InAs [72, 73] and InGaAs [74]. The benefit of using a nickelide interconnect is, firstly, low thermal budget. The formation of nickelide starts at about 250–300 °C and remains stable at 300 °C which matches the thermal budget of III–V devices [73, 75]. Secondly, the specific contact resistance, the sheet resistance, and the Schottky barrier height are low when employing such a contact. Lastly, ultrashort channel (i.e., < 60 nm) can be fabricated with ease by the self-aligned S/D formation followed by selective etching of excessive Ni by HCl [73, 76].

The first study of nickelide formation with III–V NW was reported by Cheuh et al. [72]. The formation of the crystalline nickelide is by solid source reaction of Ni thin film with InAs NW at 220–300 °C under 40 torr pressure. The Ni_xInAs is metallic in nature and forms good ohmic contact with InAs NW. The short-channel effect, which leads to higher off current, is reduced for transistor with submicron channel length employing Ni_xInAs NW connect which is in contrast to bulk Ni contact (Fig. 3.7a, b). When fabricated as a back-gated transistor with a buried gate, the ungated InAs segment induces parasitic resistance that will deteriorate the ON current. Using nickelide contact (Fig. 3.7c, d), due to its metallic nature and ohmic contact formation with InAs NW, the contact resistance is reduced. The effectiveness of the nickelide contact to reduce the specific contact resistance can be extended to ultrathin NW (sub-7 nm) and NW with medium doped level [77, 78].

Apart from InAs, Ni can also form nickelide with binary or ternary III–V compounds such as InSb, InP, and GaSb [79]. Pd and Pt are alternative metals that

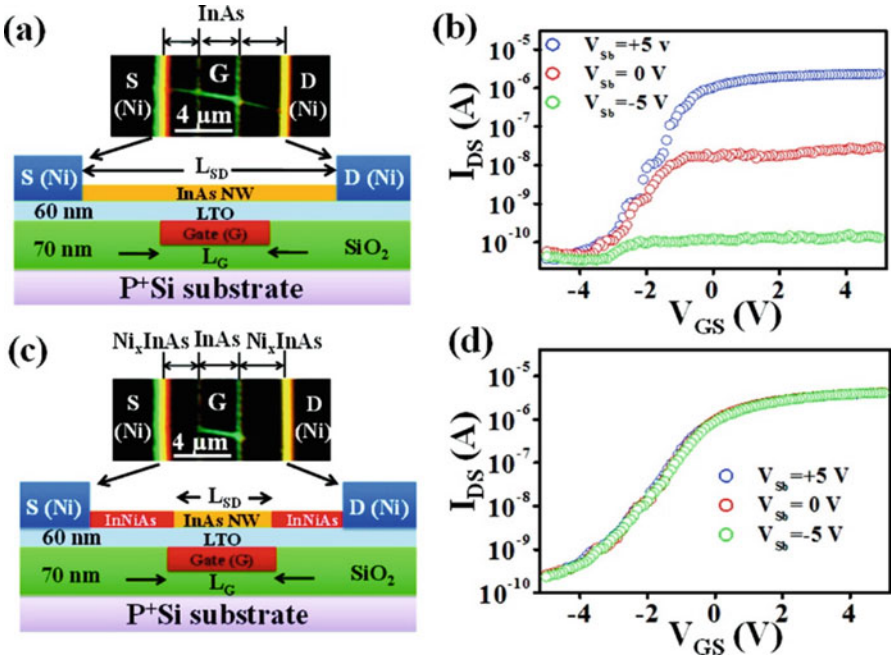

Fig. 3.7 (**a**, **c**) The schematic of InAs buried-gate NWFET before and after Ni diffusion into the channel. (**b**, **d**) The transfer characteristic of the InAs NWFET before and after Ni_xInAs formation. (Reprinted with the permission from Ref. [72]. Copyright 2008 American Chemical Society)

frequently are studied as alloying contact with III–V semiconductors. No matter which contact metal is used, further studies on factors like thermal stability, internal stress distribution, and growth kinetic are still needed.

3.3.3 Catalytic Tip Contact

Nanoscale contact of semiconductor NW and its corresponding metallic catalyst tip used in the growing process is a promising way to engineer and control the contact properties. There were two reports that studied the GaAs NW/metallic catalyst tip contact. Han et al. studied the photovoltaic effect of GaAs NW/AuGa catalytic tip and found out that the Schottky barrier is reduced compared to GaAs NW/AuGa contact (Fig. 3.8) [80]. The abrupt interface between the NW and the catalyst tip minimizes the trap density and reduces the Schottky barrier, hence reduces the Fermi level pinning that usually degrade the PV performance and improves the PV performance.

On the other hand, Suyatin et al. fabricated a low n-type Schottky barrier (~0.35 eV) with GaAs NW/AuIn catalyst tip nanoscale contact which is lower than the normal values from 0.9 eV to 0.52 eV [81]. The author attributed the low

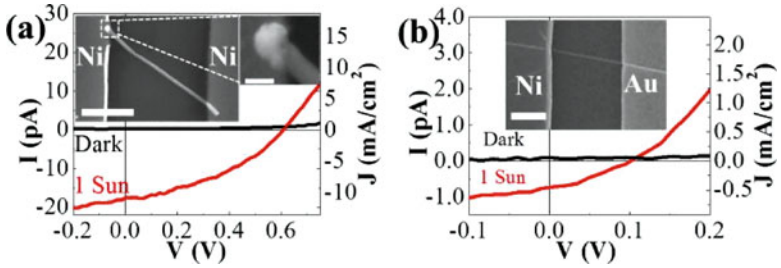

Fig. 3.8 The IV characteristic of dark current and under one sun illumination (AM1.5G, 100 mW/cm^2) of single GaAs NW PV device with (**a**) ~70 nm in diameter with Au-Ga tip (left) and Ni (right) as electrode (the scale bars in insets are 1 μm and 100 nm, respectively) and (**b**) ~60 nm in diameter with Ni (left) and Au (right) as electrode (the scale bar in inset is 1 μm). Both current density (J) is normalized by the light absorption cross-sectional area. (Reprinted with permission from Ref. [80]. Copyright 2012, American Institute of Physics)

Schottky barrier to a reduced pinning state density (10^{17} m^{-2}) and the formation of electric dipole at the interface between the NW and the catalyst particle. The electric dipole is formed by the As atom at the termination of (111) B zinc blende phase and (000-1) wurtzite phase interface and the catalyst particle. The authors suggested that better contact is possible by the careful selection of interfacial atom as well as using an appropriate crystal orientation.

Ohmic contact can also be formed by using such contact scheme. Using STM probe to measure the electrical properties, InAs and InP NWs are found to form ohmic contact with their corresponding Au-In catalyst tips [82]. One should note that most of the work focused on Au-based catalyst tip. III–V NWs can now be grown in various non-gold catalysts [83], and the alloy composition can be tuned by controlling the supersaturation; thus it is possible to control precisely the contact properties. The crystallographic detail of the catalytic tip may also be used to modify the contact properties.

3.4 Crystal Engineering

Considering NW as water pipe with fixed diameter and charge carriers as water, the water flow rate would be determined by the obstacles existed within the water pipe. With more obstacles, water flows slower. Using the same analogy, obstacles in NW mean any crystalline features that increase the resistance of the NW; thus the crystal features can affect significantly the electrical and optical properties of III–V NWs.

First of all, the crystal phases of the NW are usually found to be cubic zinc blende (ZB) or hexagonal wurtzite (WZ) assuming no crystal impurities. They have different crystal structures; hence the electronic properties and the transport properties will be different from each other. These differences have been studied both theoretically and experimentally. For example, for InAs NW the WZ phase has larger bandgap

and larger ON/OFF ratios when fabricated into transistors [84–88]. It is because WZ phase NW in <0001> direction is smoother and has less dangling bond on the surface; hence there are less surface states to degrade the electrical properties.

On the other hand, even with the same crystal phase, the crystal orientation is a factor that affects the transport properties. Energetically, III–V NWs tend to grow in the <111>B direction. Adjusting the growth parameters can control the growth direction of the NW. In a detailed study of the transport properties of InAs NWs reported by Fu et al., parameters such as SS, V_T, ON−OFF ratio, and Φ_{OFF} are all affected by the crystal orientation [88]. The difference is attributed to the surface condition that varies with different growth direction. For example, for zinc blende crystal structure, six equivalent nonpolar (110) surface planes exist along the <111>-oriented NWs, which have the lowest density of dangling bond [37] in the ZB crystal phase compared to other crystal orientations such as <110> and <211> planes.

Polytypism is another factor that might degrade the transport properties. Without careful adjustment of the growth condition, the NW is usually composed of a mixture of ZB and WZ crystal phases, that is, a large amount of twinning and stacking defects locate across the NW that can significantly degrade the electrical performance of a device depending on the material used. Due to the different electronic structures of these phases, discontinuity in the conduction band usually takes place. For InP NWs, the ZB segment acts as an electron-trapping region and forms bound states below the WZ CB edge [89]. The conductivity of the NW depends on the longest ZB segment; when the segment is increased from 3 nm to 10 nm, the Fermi level is shifted by 50 meV and the conductivity is decreased by 1 order of magnitude. In InAs NWs, the phase mixing leads to higher resistivity (up to 2 orders of magnitude) [90] and lower mobility (up to 4 times difference at 4.2 K) [91] compared to single-phase NWs.

Lastly, crystal defects such as elemental precipitates [92] and alloy fluctuations [93] may also act as scattering centers and hamper the electrical performances.

In recent years, controlling the phases of III–V NWs has been studied extensively by different research groups. Due to the advancement in characterization techniques and the tremendous efforts put in, the crystal phase of NW can be controlled down to few monolayer levels. Understanding how parameters such as temperature, III–V ratio, catalyst choice, and diameter affect the NW growth is essential in controlling the crystal phase and hence the electronic properties. In the following sessions, the techniques on how to carry out phase engineering and defects reduction are described.

3.4.1 Catalyst Diameter Control

As mentioned, WZ and ZB phase NWs have different electrical properties; thus controlling the phase is very important for device applications, and the phase purity can be controlled by the catalyst diameter.

In general, the WZ crystal is more favorable in thin (under 20 nm in diameter) NWs [94, 95] due to its lack of energy stability [96]. In a study carried out by Johansson et al. [97], InAs NWs with different diameters are grown by MOVPE, and pure WZ phase with no stacking fault is observed in small-diameter NW. Increasing the diameter leads to the appearance of stacking faults. When the diameter is increased further, the amount of ZB phase is also increased till the ZB phase becomes dominant in the NW.

Thus, controlling the catalyst dimension is the key in obtaining pure-phase WZ NWs. It can be achieved by employing ultrathin metal film as the catalytic layer [96]. Thin metal film leads to small catalyst droplets. Pure-phase MBE-grown InAs and GaAs NWs have been obtained by Shtrikman et al. using 0.5–1 nm Au layer on (111)B GaAs and (011) GaAs substrates [96, 98]. For amorphous substrate such as SiO_2 which is believed to be more cost-effective, pure WZ GaAs NWs can be obtained by using 0.1 nm Au thin film as the catalytic layer, as reported by Han et al. using tube furnace [99]. The obtained NWs are free of defects and are p-type.

Another method to obtain pure-phase WZ is to shrink the catalyst size by a two-step catalyst-annealing procedure [100]. Reported by Pan et al., the use of Ag catalytic layer with one-step catalyst annealing yields large distribution of droplet diameter due to Ostwald ripening [101]. This results in InAs NWs with large distribution in diameters. Although pure-phase WZ InAs NWs can be obtained, it is found that once the diameter exceeds 72 nm, there are NWs with mixed ZB/WZ phase. To overcome Ostwald ripening effect, the Ag catalytic layer is first annealed for 10 h and then annealed at higher temperature before the NW growth. The two-step catalyst annealing procedure results in a layer of smaller and uniform Ag droplets. The resulting NWs are very thin (average diameter ~10 nm) and are pure WZ phase. These NWs have good electrical performance (Fig. 3.9), and when they were fabricated into devices, the transistors operate in enhancement mode which is preferred for device applications.

For practical applications, one would expect pure-phase NWs within certain diameter range are needed. Therefore, it is necessary to fabricate thick WZ or thin ZB NWs. Thick WZ NWs can be fabricated by enhancing the lateral growth through tuning the growth parameter after the NWs are nucleated [96]. On the other hand, NW thinning can be done by reverse-reaction growth proposed by Loitsch et al. [102]; the as-grown NWs are directly annealed after growth, and ZB phase GaAs NWs with diameter of about 7 nm can be grown on silicon substrate using this method.

3.4.2 Growth Temperature

The properties of NWs are sensitive to the growth temperature. Reports show that for III–V NWs, WZ phase tends to yield in high temperature and ZB phase tends to yield in low temperature [103–106]. There are other restrictions on choosing the growth temperature. In high growth temperature, undesirable radial growth takes place and

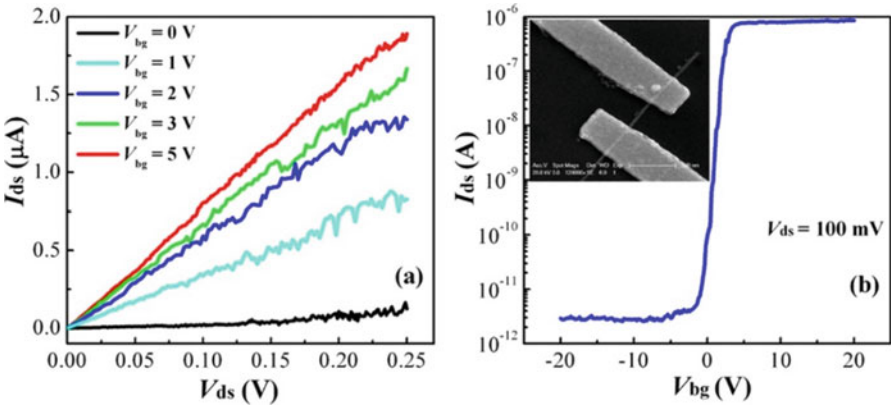

Fig. 3.9 The (**a**) output and (**b**) transfer characteristic of a Ag-catalyzed InAs NW. Inserted is the SEM image of an ultrathin InAs NW with Cr/Au contacts. (Reprinted with the permission from Ref. [100]. Copyright 2014 American Chemical Society)

causes tapered NWs [107, 108] and nonuniformed composition along the NW [109], and crystal crystallographic defects also increase with increasing growth temperature [104]. On the other hand, at low growth temperature, the catalyst tip may not be homogenous, and the NW shape becomes irregular and overcoated [110, 111].

The two-step growth method, in which a nucleation step with temperature higher than the growth temperature is used before growing, can help to obtain long, straight, and defect-free NWs [111, 112]. Under high-temperature nucleation step, the catalyst is expected to be homogenous liquid, and hence no kinked structure can be nucleated. In this way, the NWs grown are regular, and as they are grown in low temperature, the radial growth is limited, and hence no tapering can be observed. Reported by Hou et al., the InGaAs NWFET, fabricated using the two-step method NWs to reduce the kinked morphology and surface coating along the NWs, exhibits impressive electrical performance [111, 113].

There have been two reports on using the two-step growth method to reduce the defect density of GaAs NWs [92, 112]. Joyce et al. used the two-step growth method to limit the radial growth and eliminate the twin defects at the same time [112]. In another report, Han et al. eliminated the crystal defects of GaAs NW by the same technique. Using solid source CVD [27], the transport types of the obtained GaAs NWs switch from n-type to p-type when the diameter of NW decreases compared to the traditional one-step method. The effect is attributed to the acceptor-like states at the oxide interface that deplete the conduction channel near the interface. With thinner NW, this effect dominates and the NW is p-type. For thicker NW, the donor-like crystal defects such as As precipitates [114–116] are generated by insufficient Ga supersaturation in the catalytic tip during growth, neutralizing the depletion of the oxide interface defects and dominating when the NWs get thicker; thus the NW becomes n-type. With the two-step growth, the crystal defects are reduced (shown in Fig. 3.10a, b where both PL and Raman spectra confirm the

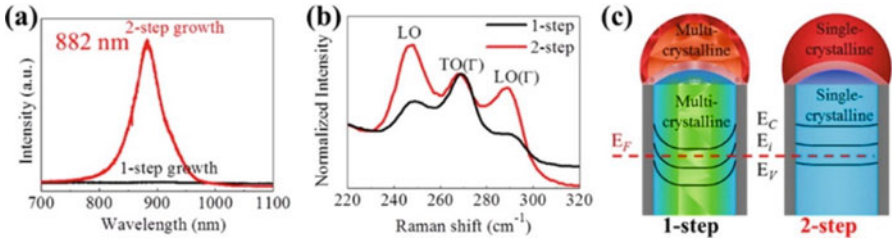

Fig. 3.10 (**a**) Room temperature PL spectra of one-step and two-step growth GaAs NWs. (**b**) Raman spectra of one-step and two-step grown NWs. (**c**) Schematic of cross-sectional view of one-step and two-step growth GaAs NWs and their corresponding crystal quality and equilibrium energy band diagram at the zero gate bias. (Reprinted with the permission from Ref. [92]. Copyright 2013 American Chemical Society)

reduced crystal defects in two-step GaAs NWs) due to the improved crystallinity (Fig. 3.10c), and the larger diameter NWs can remain as p-type.

3.4.3 Source Flow Control

The crystal phase of III–V NW is strongly affected by the source flow. For techniques such as MBE and MOVPE, the flow rate of group III and V elements can be controlled separately; the V/III ratio can be precisely controlled. For MOVPE-grown NWs, pure WZ NWs are yielded at high V/III ratio, and ZB NWs are yielded at low V/III ratio [117, 118], with twins and stacking faults (SFs) appearing during the in-between ratio. For GaAs NWs, the growth behavior is different [119, 120]. WZ NWs are yielded at low V/III ratio, and ZB NWs are yielded at low V/III ratio (coupled with low grow temperature) (Fig. 3.11).

The V/III ratio is also highly coupled with other growth parameters. For example, increasing the V proportion (by increasing the V flow or decreasing the III flow) reduces the supersaturation of the catalyst particle that affects the crystal purity. Temperature is another factor that strongly interrelated with the V/III ratio. Although the underlying mechanism of how these parameters are related is complicated, using phase engineering is seen as a viable alternative, and by tuning the V/III ratio and other growth parameters, ZB-WZ junction can be fabricated down to a few monolayers [84].

3.4.4 Challenges

The above discussions give a general approach on how to engineer the phases of NWs. Factors that affect the crystal phase include substrate direction, catalyst choice [121], and catalyst supersaturation [122]. All these factors are important when

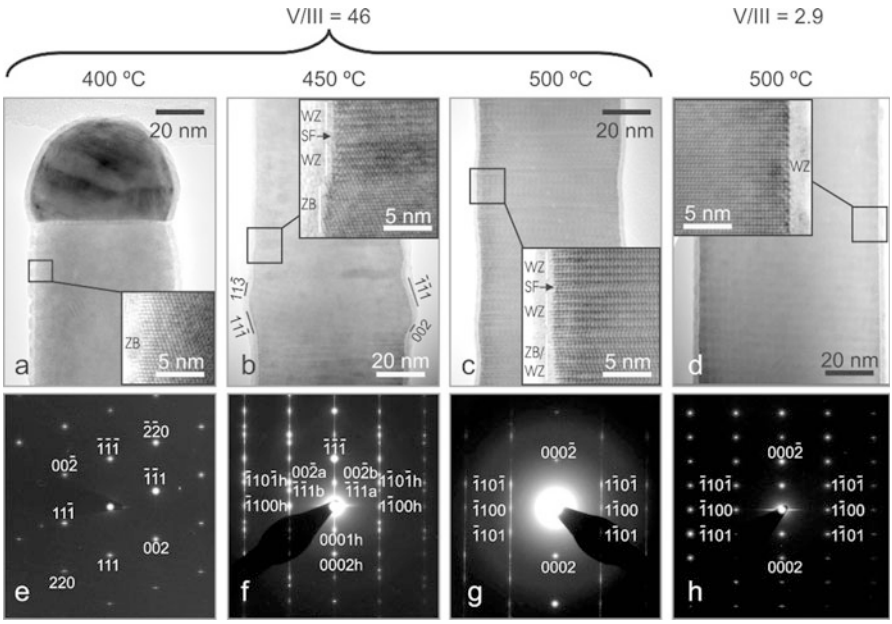

Fig. 3.11 (**a**–**d**) TEM/HRTEM images of GaAs NW under different conditions and (**e**–**h**) their corresponding SAD pattern. (Reprinted with the permission from Ref. [120]. Copyright 2010 American Chemical Society)

designing the desirable NW structure and its electronic properties. The phase control is a complicated process, because tuning one factor would greatly affect the NW property, and to obtain the desirable NW phase, morphology, and electronic properties, two or more factors need to be optimized at the same time. With extensive studies carried out in the last decade, the phase engineering of III–V NW grown on III–V substrate and silicon substrate is well-studied. There are problems that remain to be overcome, such as unwanted tapering [123] and unintentional carbon doping for MOVPE process [124].

3.5 Conclusions

The future of III–V NW is bright and promising. The NW exhibits unique characteristics such as high mobility, direct bandgap, and wide range of composition with bandgaps that match the wavelengths from IR to UV. It can be used to fabricate advanced device structure such as GAA that may be the key to the next generation of low-power and high-performance transistor. It can also be used in various devices such as integrated circuit, photodetector, and biosensor.

Although many device structures and applications have been proposed and demonstrated, commercial III–V NW products are still limited. Further studies and understanding are required, such as the integration cost, how well it can be integrated in existing chip fabrication facilities, and, as the purpose of this chapter, how well and precise their electronic properties can be controlled in a production environment. As mentioned, NW can be obtained by top-down or bottom-up approaches, and the device structure can be vertical-built or horizontal-built. These differences require further analysis to see what the limitations are and which technique is more suitable for commercialization. The push to engineer the crystal, the NW surface, and the contact interface will continue, and further attention and solution are required before commercial product becomes a reality. We believe and hope that the content covered in this chapter contributes to the development of III–V NW in the said direction.

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Chapter 4
Probing Material Interfaces in Nanowire Devices Using Capacitive Measurements

Yu-Chih Tseng

4.1 Introduction

A modern transistor is a system of materials with a broad range of electrical conductivities, ranging from oxides for gate insulator to semiconductors for transistor channel, to metals and their alloys for electrical contact. The electrical properties of each constituent of a device influence only partly the overall function. More often than not, the interface between two materials is equally important. The PN junction is the most fundamental example. It is because of the space charge region at the interface that diodes provide rectification, and that electron-hole pairs generated in solar cells can be separated. Another example is the metal-semiconductor (MS) contact, which provides current rectification because of the Schottky barrier between the metal and the semiconductor. The MS contact can also be ohmic if the substrate is heavily doped. The oxide-semiconductor interface in a MOSFET is yet another important example. Because the current flowing in a MOSFET is located directly under the gate oxide, a good oxide-channel interface is necessary to ensure a satisfactory transistor performance.

Modern transistors utilize many elements in the periodic table to meet advanced performance and reliability benchmarks. Examples include Ge for straining the channel [1], HfO_2 and ZrO_2 for gate dielectric [2, 3], Mo and its associated compounds for the gate electrode [4], C in low-k interlayer dielectrics [5], W in vias [6], Co or Ni in the contacts [7], and As, Sb for low-diffusivity dopants. Many other elements and compounds, such as PtSi [8] and SrTiO [9], are investigated as well. As a result of this material diversification, interface properties are ever more important.

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As a transistor shrinks in size, one-dimensional semiconductor materials become very interesting candidates as a building block for the transistor. These, represented by carbon nanotubes and nanowires of various semiconductor materials, are synthesized using chemical and self-assembly methods and cannot be easily manufactured starting from bulk materials. These nanowires and nanotubes offer new possibilities. In carbon nanotubes, for example, carrier scattering is greatly reduced, leading to high carrier mobility, suitable for high-performance transistors [10]. The mere shape of these nanotubes and nanowires facilitates the fabrication of devices with novel geometry, such as surround-gate transistors with optimal electrostatic control [11].

The performance of these nanotube and nanowire transistors depends, just like their counterpart in bulk, on the engineering of their interfaces and junctions with other materials. Semiconductor carbon nanotubes, for example, usually form Schottky contacts with metals, and such a junction can dictate completely the device's behavior [12]. In Si nanowires, it has been shown that the conditions at the surface can alter the carrier mobility considerably [13]. A similar behavior is observed in other types of nanowire devices.

Unlike bulk materials, there is little systematic study of the interfaces of these bottom-up materials. The primary reason is the smallness of these nanoscale objects, which precludes the usage of common surface characterization techniques such as X-ray photoemission spectroscopy (XPS), capacitance-voltage, deep-level transient spectroscopy (DLTS), admittance spectroscopy, or secondary ion mass spectroscopy (SIMS). Furthermore, these nanoscale objects generally vary greatly in size, and assembling many of them with a long-range order, in a way that unambiguous information can be obtained, is still a challenge.

In this chapter, I provide a summary of investigations into basic junctions in these novel one-dimensional semiconductors using capacitance-voltage measurements, as well as new developments on the important problem of nanoscale semiconductor junctions.

4.2 Diffused Junction of a Semiconductor Nanowire

Semiconductor nanowires have many potential applications, including biochemical sensing, computing, and energy applications. Important material parameters such as the dopant distribution and surface state density are crucial in determining the performance of nanowire transistors in many applications. Here I provide an overview of applying the capacitance-voltage (C-V) method to a single silicon nanowire surround gate field effect transistor to extract the radial dopant distribution. The work in this section demonstrates the application of C-V measurements on a silicon nanowire transistor, fabricated using a vapor-liquid-solid (VLS) method. Finite element modeling (FEM) is used to support the results and to test for limitations in the doping profile resolution. The results are compared with those from planar metal-oxide semiconductor (MOS) structures and with the common assumptions used in modeling the electrostatics of nanowire transistors.

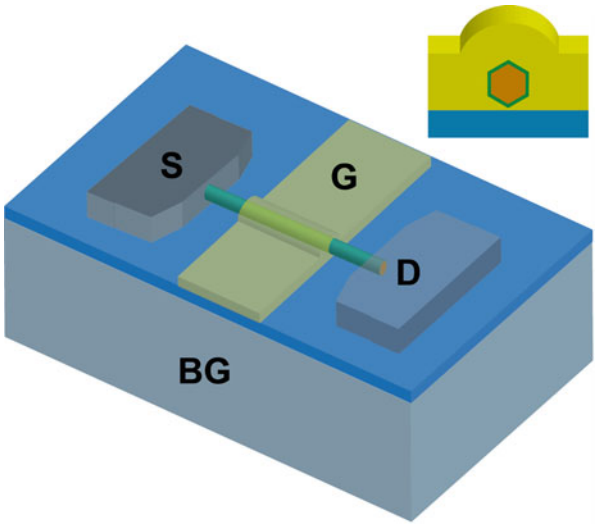

Fig. 4.1 Device test structure for C-V measurement. S/D: source and drain. G: top gate. BG: back gate. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [15], copyright 2009)

4.2.1 Design of Test Structure and Measurement Scheme

The test structure is similar to that proposed by Ilani et al. [14]. Figure 4.1 illustrates the design of the structure. On an SOI wafer, a silicon nanowire bridges two heavily boron-doped silicon contact pads, about 4 μm apart. A top gate stack composed of high-k/metal materials is formed in the middle of the wire. This gate stack, along with the nanowire, forms a MOS capacitor. However, 1 μm of the nanowire from each side of the S/D electrodes is not covered by the top gate and is instead gated by the back gate. The back gate is used to extract the background parasitic capacitances.

To measure the capacitance between the nanowire and the gate, the scheme in Fig. 4.2 is followed. In the first measurement, the back gate is negatively biased to turn on the exposed parts of the NW, and both the gate-nanowire capacitance C_s and the background parasitic capacitances C_p contribute to the measured capacitance. In the second measurement, the back gate is positively biased, and the contribution from C_s is eliminated. Subtracting these two measurements yields only the capacitance from the gate- nanowire capacitance C_s.

4.2.2 Device Fabrication

The fabrication of the test devices is detailed in previously published work, integrating nanowires synthesized by a gold-catalyzed VLS method [13, 17].

The diffused junction in the nanowire is formed by diffusing boron dopants into the nanowire in an environment containing the boron precursor BCl_3. The gate

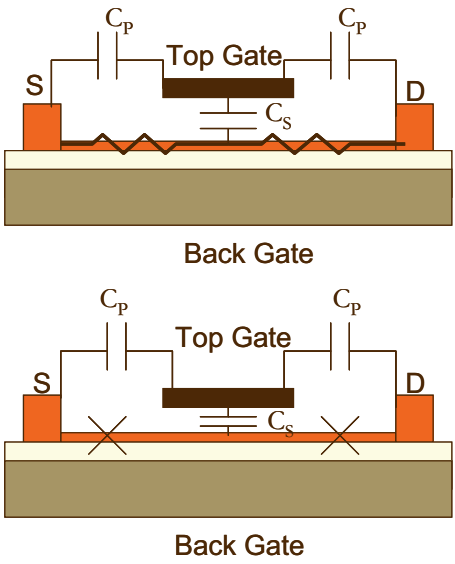

Fig. 4.2 Measurement scheme to extract background capacitance. Top: negatively biased back gate leads to low-resistance contacts to the gate-nanowire capacitor C_s. Bottom: positively biased back gate turns off access to C_s. (Reprinted from Ref. [16])

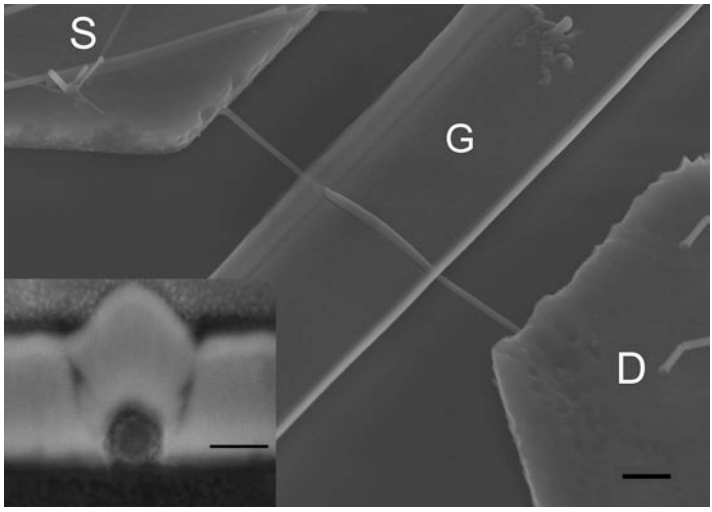

Fig. 4.3 SEM picture of an actual nanowire test device for C-V measurements. The inset is a cross-sectional view of the device taken after focused ion beam (FIB) milling. The scale bars are 1 μm (main panel) and 100 nm (inset). (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [15], copyright 2009)

dielectric was Al_2O_3, deposited by atomic layer deposition (ALD) using alternating pulses of trimethylaluminum and water. The surround-gate metal (Cr in this case) was patterned via photolithography and liftoff. Figure 4.3 shows a completed Si nanowire FET.

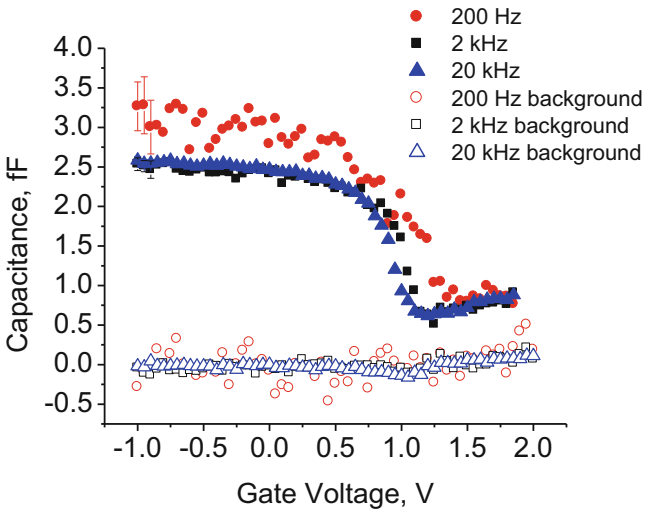

Fig. 4.4 Capacitance-voltage measurements at 77 K and 200 Hz (red), 2 kHz (black), and 20 kHz (blue), with the background shown in the corresponding open symbols. The error bars are shown only for the first 3 data points for clarity. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [15], copyright 2009) (Color figure online)

4.2.3 Capacitance Measurement and Determination of Dopant Density

Following the scheme in Fig. 4.2, the capacitance was measured at 77 K using the Andeen-Hagerling AH2700A with an excitation amplitude of 20 mV, with long averaging times. Figure 4.4 shows the silicon nanowire C-V response at 200 Hz, 2 kHz, and 20 kHz with the back gate set at −20 V. The background capacitance was measured with the back gate at 8 V. Both measurements were repeated at the three frequencies.

The experimental C_{ox} of 2.58 fF, taken from the strong accumulation region of the 20 kHz C-V, is within 7% of the calculated C_{ox} value, using the measured geometrical dimensions ($L = 2.3$ μm, $D = 75$ nm), $\kappa = 7.3$ for Al_2O_3, and $T_{ox} = 15$ nm. If we assume instead that the 15 nm oxide consists of 1 nm native SiO_2 and 14 nm of Al_2O_3 as would be expected according to a previous TEM study [18], then we get only 1% deviation between experimental and simulated C_{ox} values. The agreement suggests that quantum confinement effect is comparatively not important, which is expected for a thick oxide layer. Deducing the roll-off frequency using the measured conductance and capacitance, we see in Fig. 4.5b that the roll-off frequency is well above the measurement frequency for the range of top gate voltages of interest (−1 to +1 V). The measured depletion region in the C-V curve is therefore not an artifact of the access resistance.

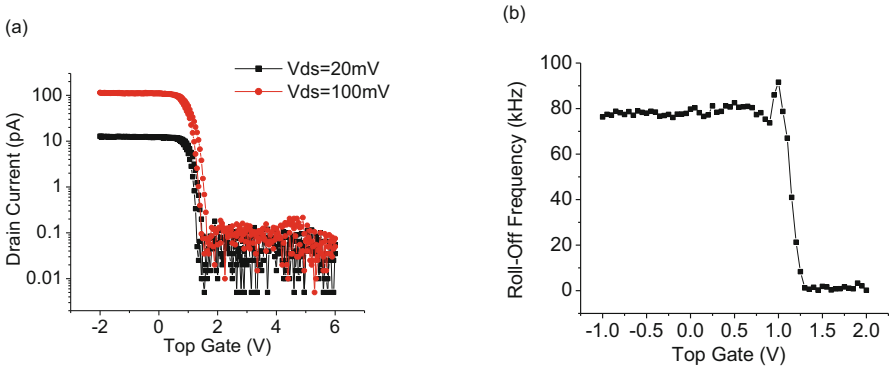

Fig. 4.5 (**a**) Transfer (Id-Vg) characteristics of the test structure. (**b**) The calculated roll-off frequency using Fig. 4.5a and Fig. 4.4. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [15], copyright 2009)

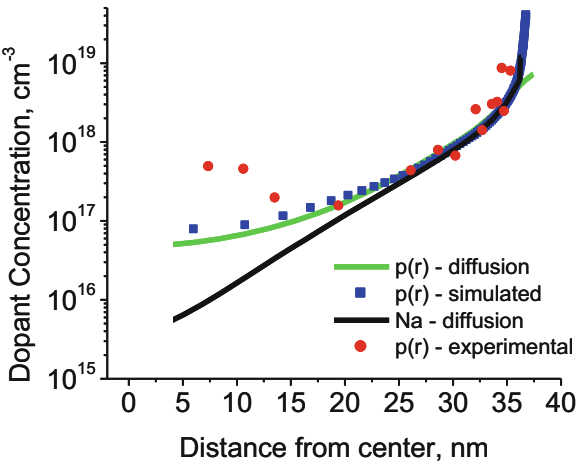

Fig. 4.6 Radial charge and dopant profile extracted using C-V measurement. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [15], copyright 2009)

4.2.4 Dopant Profile

The dopant profile was also extracted using the high-frequency C-V curve, using depletion approximation. The results are compared to the simulation from TSupreme, using the actual device dimensions and process conditions simulator, including the interstitial- and vacancy-assisted diffusion models. In addition, we assume that the dopant concentration at the surface was fixed at the solid solubility ($\sim 10^{19}/cm^3$ at 675 °C). The depletion approximation is also verified using finite element electrostatic simulations (COMSOL Multiphysics), to include both the ionized dopants and the majority carriers. Figure 4.6 shows the agreement between the simulated diffusion profile and the experimental data. In addition, the FEM simulation shows that the profiles of the ionized dopant and the majority carrier

match well, except at low doping levels. This is expected since the characteristic length of Debye screening is fairly long (~6 nm) at these doping levels (<10^{17}/cm^3). The disagreement near the core of the wire is expected according to C-V dopant profile resolution limitations. Due to the lower carrier density in semiconductors (as opposed to metals), charges in semiconductors cause local electric field penetration over some significant distance. In doped semiconductors, this distance is known as the extrinsic Debye screening length (L_d) and depends on dopant density, temperature, and dielectric constant [19].

It has been well established that depth resolution in C-V dopant profiling is limited to about $2L_d$, which at our measurement temperature of 77 K should be about 2 and 13 nm at the surface and core, respectively, due to the different doping levels [20]. Furthermore, because the Fermi level depends on dopant concentration, some majority carriers will redistribute within the nanowire from the high to low dopant density regions. Since C-V actually measures the free carriers and not the dopant atoms, the experimentally extracted majority carrier profile will only match the dopant profile in regions where the carrier redistribution has a minimal impact, typically 10^{17} cm^{-3} or higher [21, 22]. It is important to note that outside of these resolution limits, we can certainly differentiate between a graded profile and a uniform dopant distribution. Using the same FEM 3-D simulations, we can compare the simulated C-V to the experimental C-V curves in order to determine the flat band voltage (V_{fb}) and further validate our dopant profiling and D_{it} extraction techniques.

Figure 4.7 shows the FEM simulated C-V curves calculated from the diffusion and flat profiles (Na = 10^{17}/cm^3) compared to the high-frequency (20 kHz) experimental C-V curve. The simulated curves are shifted horizontally so they overlap one another, for the purpose of comparison. Without this shift, the flat band voltage for the flat profile would be about 0 V. Clearly, our experimental C-V curve does not match that obtained from a flat dopant profile, but it is a good match to the C-V curve obtained from a diffusion profile simulated using TSupreme.

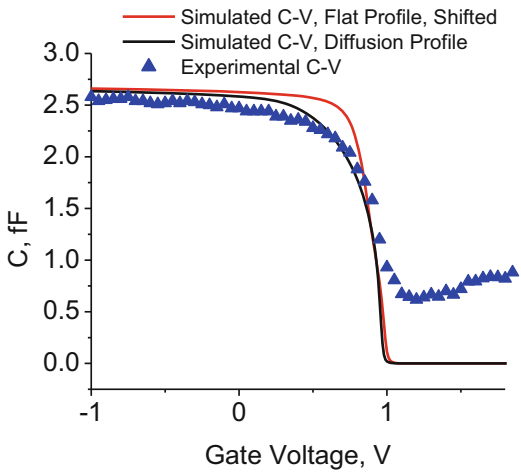

Fig. 4.7 Capacitance-voltage simulations. Experimental high-frequency 20 kHz C-V curve (blue) compared to the finite element modeling (FEM) simulated C-V curves for the boron diffusion profile (black) and the flat profile (red) as shown in Fig. 4.6. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [15], copyright 2009) (Color figure online)

The only major deviation comes at full depletion where the simulation goes essentially to 0 fF, while the experimental curve does not go below 0.5 fF. This extra capacitance in the experiment may come from direct coupling between the surround gate and the nanowire leads; the simulation would not see this since it does not incorporate a back gate and thus allows for the leads to become depleted. Since the simulation did not account for interfacial defects, the minor deviation in slope likely stems from interface states, which are known to cause stretch-out even in high-frequency C-V measurements.

In Fig. 4.7, it was necessary to shift the simulated C-V curve horizontally to match the measurement. In addition to the shift due to the built-in potential between the metal gate and the substrate, a fixed oxide charge density of -4.6×10^{11} cm^{-2} is necessary to match the flat band voltages. This value is similar to previous literature reports for Al_2O_3 deposited using ALD.

4.2.5 Summary

The C-V measurement applied conventionally to planar metal-oxide capacitors was used to characterize a diffused junction in a silicon nanowire synthesized by the VLS method. The radial boron dopant profile was deduced and matched the expected profile from dopant diffusion simulations with a surface concentration near the boron solid solubility of 1×10^{19} cm^{-3}. This is in contrast to a flat dopant profile guessed from measured conductivity, mobility, and threshold voltage in the previous literature on Si NW transistors. These results unambiguously demonstrate that quantitatively understanding and controlling the surface properties and dopant distribution within semiconductor nanowires will be critical to achieve reproducible high-performance devices.

4.3 Surface States of Semiconductor Nanowires Characterized by Capacitance-Voltage Measurements

The interface between the gate dielectric and the channel is very important to the performance of a field-effect transistor (FET). For materials with high carrier mobility such as III–V semiconductors, their utilization as channel material in a FET has been hampered by the unavailability of a gate dielectric with an acceptable interface quality. Transistors based on bottom-up semiconductor materials such as nanowire of Si [18], Ge [23], InAs [24], or carbon nanotubes [10] are also shown to have very large carrier mobility, leading to a current density much superior to devices based on bulk Si. However, most prior estimates of the mobility were based on rather simple calculation of the gate capacitance [25]. In these primitive devices, the channel is often back-gated because that geometry is easy to fabricate

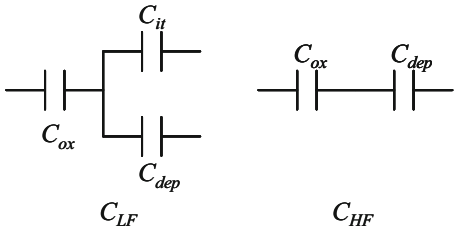

Fig. 4.8 Circuit model of the gate stack capacitances at low and high frequencies

and one can dispense with a gate dielectric that usually negatively impacts on the carrier mobility. As a result, the electrostatic environment is not simple due to the complex geometry of the dielectric medium surrounding the channel.

In this chapter, the C-V technique is used to characterize a Si nanowire and individual InAs nanowires in their usual back-gated configuration, both to extract the oxide capacitance accurately and to characterize the interface quality, in terms of usual parameters such as interface trap density and trap lifetime.

4.3.1 *The Interface State Density of a Si Nanowire with Al_2O_3 Oxide*

There is significant frequency dispersion in the depletion region of the C-V curves shown in Fig. 4.4 of the previous section. The dispersion is typically attributed to the finite lifetime of charge traps by the interface states, which cannot respond quickly enough to high frequencies. We can extract the interface state density (D_{it}) as a function of energy level in the bandgap by comparing the high- and low-frequency capacitance curves. Figure 4.8 shows the approximate circuit models in each case. At frequencies much slower than the trap lifetimes, the contribution from the traps (C_{it}) is measured in addition to the depletion (C_{dep}) and oxide capacitances (C_{ox}), whereas at high frequencies the traps are not seen at all.

Straightforward circuit analysis gives the following expression for D_{it}:

$$D_{\text{it}} = \frac{(C_{\text{LF}} - C_{\text{HF}})}{q\left(1 - \frac{C_{\text{LF}}}{C_{\text{ox}}}\right)\left(1 - \frac{C_{\text{HF}}}{C_{\text{ox}}}\right)2\pi rL} \text{ states/cm}^2\text{ev} \tag{4.1}$$

Applying Eq. 4.1 to the measurements in Fig. 4.4, we can extract D_{it}. This is shown in Fig. 4.9, where the resulting D_{it} varies from 4×10^{11}/eV·cm^2 at mid-gap to 1×10^{13}/eV cm^2 closer to the band edge. The trend matches well with results from on control MOS capacitors fabricated on planar silicon, following the same doping and oxide deposition steps. The mid-gap density is about an order of magnitude above high-quality thermal oxide interfaces but similar to both literature and planar control experiment values for Al_2O_3 on silicon [26–29].

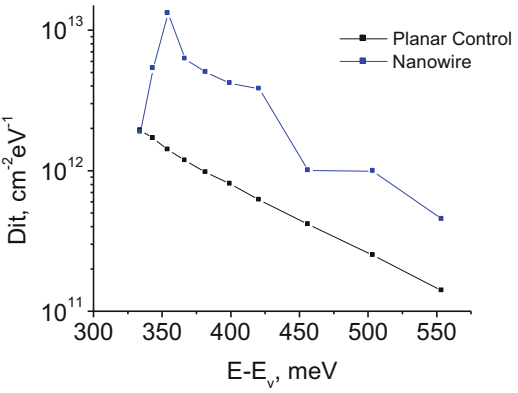

Fig. 4.9 Surface state analysis. Interface state density versus position in the bandgap with respect to the valence band. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [15], copyright 2009)

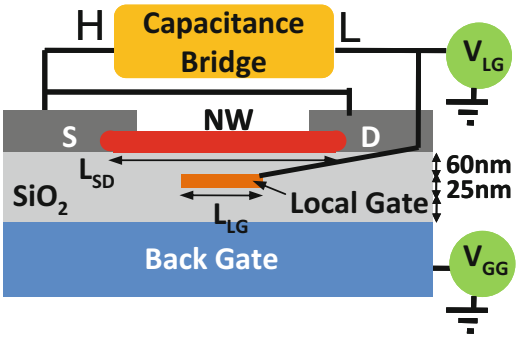

Fig. 4.10 Test structure for C-V measurement of InAs nanowires. The underlapped region can be modulated by the back gate for extracting background capacitance. The capacitance is measured between the local gate and the source/drain. (Reprinted with permission from Ref. [24]. Copyright 2009 American Chemical Society)

The shape of the D_{it} curve and peak position within several hundred meV of the valence band edge is also qualitatively similar to what has been observed in planar silicon junctions. Compared to the planar control, D_{it} is larger, possibly due to faceting of the Si nanowire, seen in the inset of Fig. 4.3.

Note that our results should be taken as the lower limit of the true D_{it}, since AH2700A is limited to operate between 50 Hz and 20 kHz, and it is not possible to access the true high- and low-frequency characteristics. The high-low method is well-known to underestimate the interface state density due to the difficulties in obtaining true high- and low-frequency behavior.

4.3.2 The Native Oxide in InAs nanowires

InAs is a small-bandgap and high-mobility material. To extract mobility in InAs nanowires, we use the test structure illustrated in Fig. 4.10. It is very similar to the structure previously used for measuring Si nanowire, with the exception that both gates are buried, so that no gate dielectric is in contact with the nanowire. Instead, the

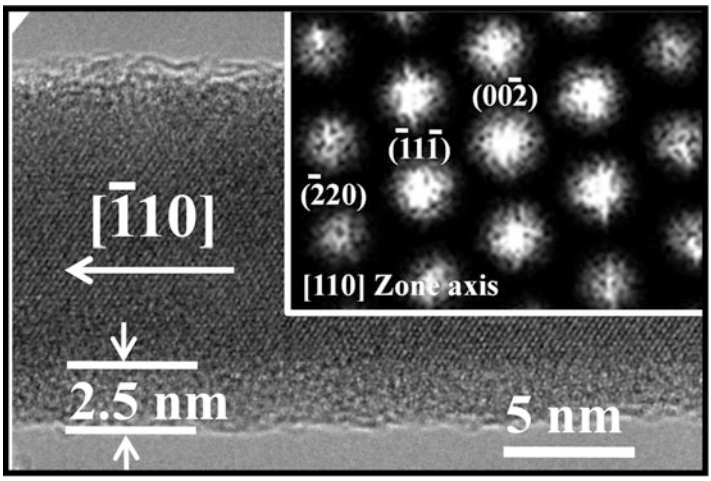

Fig. 4.11 TEM image of an InAs nanowire, showing the crystallinity of the wire as well as the presence of a 2.5 nm native oxide. (Reprinted with permission from Ref. [24]. Copyright 2009 American Chemical Society)

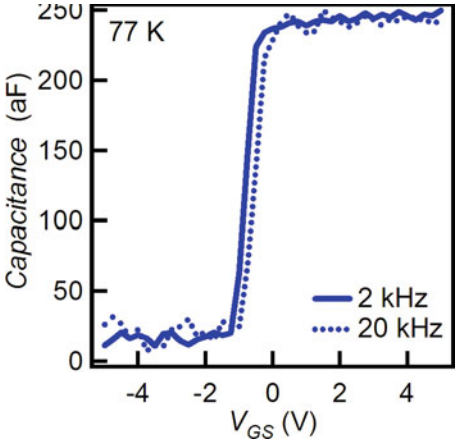

Fig. 4.12 Typical C-V curve at 77 K for an InAs nanowire. (Reprinted with permission from Ref. [24]. Copyright 2009 American Chemical Society)

InAs nanowire is surrounded by its native oxide, about 2.5 nm thick as shown in Fig. 4.11.

Figure 4.12 shows a typical C-V curve measured at 77 K. At this temperature, the surface states are too slow to respond to the applied signal frequency (1–20 kHz). As the temperature is increased, frequency dispersion due to interface traps becomes observable (Fig. 4.13). Above 200 K, the lifetime of the traps is short enough to respond to the highest frequency (20 kHz) of the instrument, and they completely dominate the capacitance measurement, so that the wire cannot be depleted and an accurate measurement of the background cannot be done. Indeed,

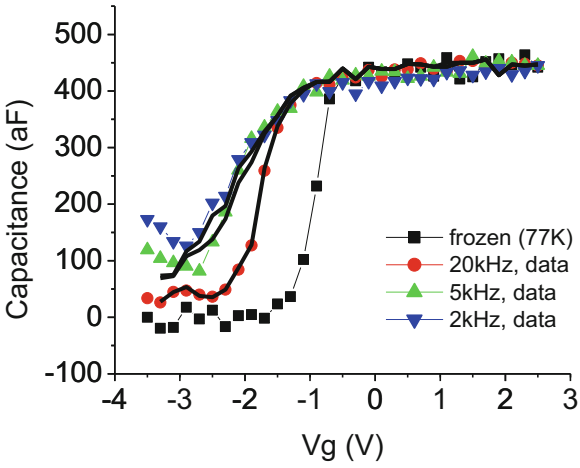

Fig. 4.13 C-V curve of an InAs nanowire measured at 200 K. (Reprinted from Ref. [16])

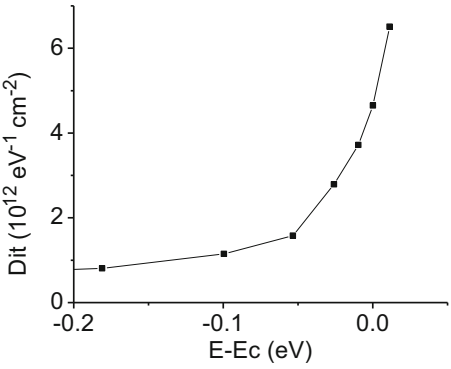

Fig. 4.14 Trap density D_{it} vs position in the bandgap, deduced from single-lifetime fit to the C-V curves in Fig. 4.13. (Reprinted from Ref. [16])

a recent report [30] shows that frequency as high as 20 MHz is necessary at room temperature to freeze out all traps.

A single time-constant model for the trap lifetime successfully reproduces the frequency dispersion effect in Fig. 4.13. Based on this model, a surface trap density D_{it} of ~10^{11} to 10^{12}/eV-cm^2 can be extracted from the C-V curves (Fig. 4.14). The capture cross section σ_p of the trap can also be estimated by using the formula [17]

$$\tau = \frac{1}{v\sigma_p n} \tag{4.2}$$

where τ, v, and n are, respectively, the trap lifetime, thermal velocity, and carrier density. n can be estimated from a Taurus 3-D simulation which shows a remarkably uniform charge density throughout the wire, despite the back-gated geometry (Fig. 4.15). Figure 4.16 shows the trap lifetime deduced from the C-V curves and compared to the expected values calculated from Eq. 4.2. There is a relatively

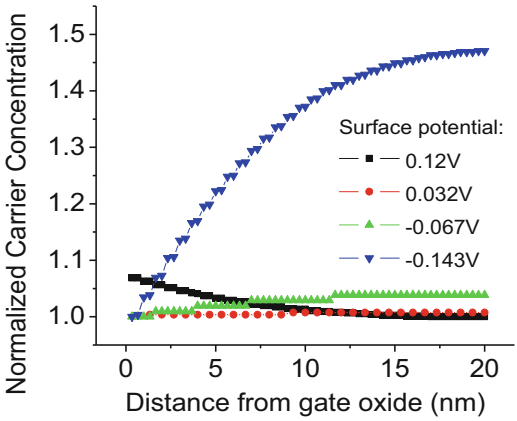

Fig. 4.15 Normalized carrier density vs distance from gate oxide for several surface potentials. The carrier density is normalized to the smallest value along the profile. (Reprinted from Ref. [16])

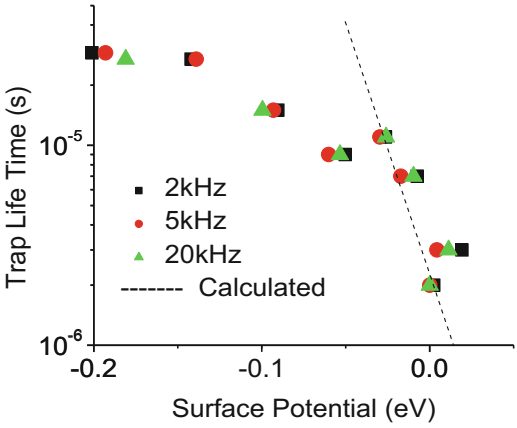

Fig. 4.16 Deduced trap lifetime compared to calculated values from Eq. 4.2. A capture cross section $\sigma_p = 2 \times 10^{-15}$ cm^2 is deduced from this calculation. (Reprinted from Ref. [16])

good agreement for traps near the conduction band, when a capture cross section of 2×10^{-15} cm^2 is used. This value is significantly larger than traps at the Si-SiO_2 interface (~3×10^{-16} cm^2) [30].

A literature search reveals no prior estimate of the capture cross section of surface states of InAs nanowires. For larger surface potential where the lifetime is relatively independent of the surface potential, other processes may be causing the frequency dispersion in the C-V curves.

4.3.3 Capacitance for Mobility Determination

InAs nanowires grown using solid-source CVD have a diameter ranging from 20 nm to 40 nm [24]. The geometric component of the gate oxide capacitance of several back-gated InAs NW transistors is shown in Fig. 4.17. Electrostatic simulation

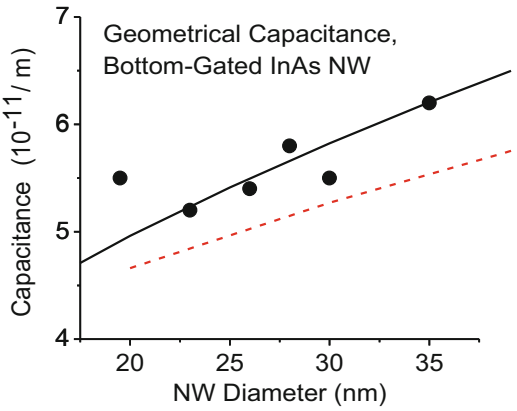

Fig. 4.17 Capacitance per unit length for InAs nanowires in a back-gated geometry. Dashed line: electrostatic simulation. (Reprinted with permission from Ref. [24]. Copyright 2009 American Chemical Society)

reproduces well but underestimates the capacitance slightly, probably due to an error in the oxide thickness measurement. The oxide at the edge of the buried gate can also be much thinner than expected due to nonuniform coverage from the CVD oxide. More importantly, Fig. 4.17 shows that a simple analytical model (Eq. 4.3) fits well only when the nonuniform dielectric medium is taken into account.

$$\frac{C_{ox}}{L} = \frac{2\pi\varepsilon\varepsilon_0}{\cosh^{-1}\left(\frac{T_{ox}+R_{NW}}{R_{NW}}\right)} \tag{4.3}$$

This can be simply done by making the dielectric constant a fitting parameter, which at 1.77 gives a reasonable fit. This reflects the fact that some electric field lines go through air. This result is similar to approximations used for striplines in microwave circuits [31].

With the gate capacitance accurately known, low-field mobility can be confidently extracted and is shown in Fig. 4.18. At sufficiently low temperatures, phonon scattering is suppressed, and there is an overall increase in mobility. The more rapid decrease in mobility at small nanowire radii may be attributed mostly to surface scattering.

4.3.4 Summary and Future Work

Capacitance-Voltage measurements were used to deduce parameters for describing the surface states of a single silicon nanowire and individual InAs nanowires. In addition, it was shown that the geometrical gate-channel capacitance fits well to an analytical estimate, provided that the nonhomogeneous dielectric medium is accounted for. The accurate measurement of the oxide capacitance is necessary

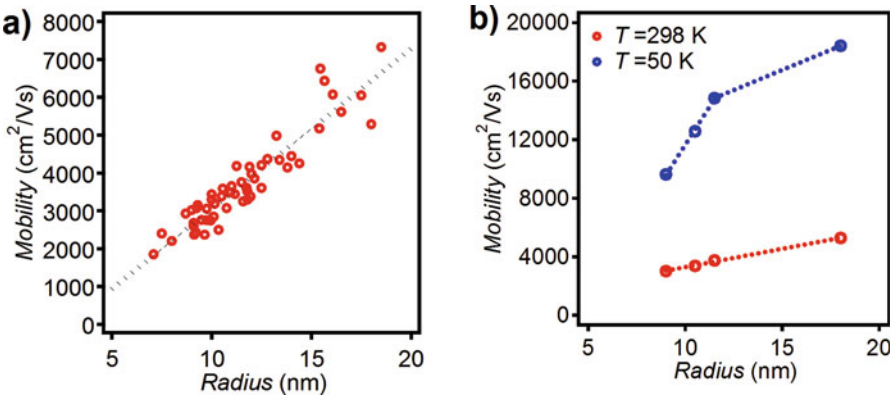

Fig. 4.18 (**a**) Low-field electron mobility vs nanowire radius at room temperature. (**b**) Mobility vs radius at room temperature and 50 K. Phonon scattering dominates at room temperature, masking the effect of surface scattering. (Reprinted with permission from Ref. [24]. Copyright 2009 American Chemical Society)

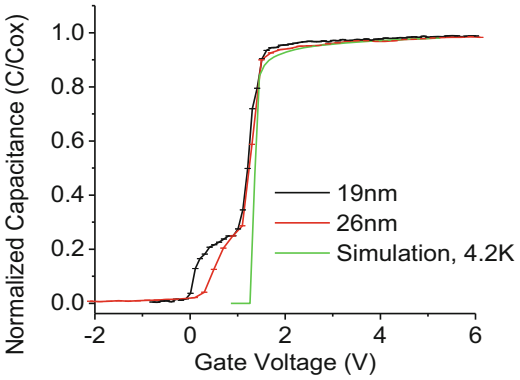

Fig. 4.19 Measured C-V curves of two small-diameter InAs nanowires (with diameters of 19nm and 26nm) at 4 K. Simulation: diameter = 20 nm. (Reprinted from Ref. [16])

to accurately calculate carrier mobility in InAs nanowires. When phonon scattering is suppressed at low temperatures, the dominant mechanism for mobility reduction in very small wires seems to be surface scattering.

There are other properties of an InAs nanowire that can be probed using this technique, one of which is the quantization effect arising from the small diameter. Figure 4.19 shows a much more precise C-V measurement of two small-diameter InAs nanowires at liquid helium temperature and its comparison to simulation. There are small but interesting steplike features near $Vg = 0$ that cannot be reproduced by a straightforward electrostatic simulation employing bulk density of states.

At this temperature, the traps should be completely frozen out as shown in this section. Simulation taking into account sub-bands resulting from one-dimensional confinement can qualitatively reproduce the measurements in Fig. 4.19. However, in

this case, the device geometry, having a planar gate instead of a concentric dielectric layer, significantly complicates a charge density calculation that accounts for both electrostatics and quantum confinement. More careful design and manufacture of test devices in the future will facilitate the comparison of experimental data to theory.

4.4 Capacitance Measurement of Metal-Semiconductor Carbon Nanotube Contacts

The metal-semiconductor (MS) contact in a semiconductor device is very important. For a device based on carbon nanotubes, the MS contact can completely dictate the device behavior. For this reason, knowing the Schottky barrier height (SBH) of a MS contact is very important for understanding and modeling the device behavior. Chen et al. [32] extracted the SBH of a carbon nanotube-metal contact using NEGF-based models. Appenzeller used a simple argument to qualitatively deduce the SBH from the transfer characteristics of a nanotube transistor [33]. Nevertheless, these do not directly measure the SBH of the contact in question. Unlike bulk MS contacts, there is no convenient way of measuring this device parameter, due primarily to the smallness of the contact. Temperature-dependent transport measurement of a Schottky diode structure reveals that many thermally activated processes are present, making a reliable determination of the SBH difficult. Another obvious alternative is the C-V measurement. An instrument designed for low-level capacitance measurement, as the results in this section show, is capable of measuring this important parameter in a straightforward manner.

4.4.1 Test Structure for C-V Measurement and Its Fabrication

As in C-V measurement of a bulk MS contact, it is necessary to fabricate a Schottky diode. Two MS contacts are necessary: the Schottky contact to be measured and a low-resistance ohmic contact to the semiconductor. For all the devices studied, the ohmic contact is made using Pd, and the Schottky contact is made with a variety of metals: Ti, Nb, and Cr.

The test structure is illustrated in Fig. 4.20. Two different metals are used to form the Schottky and ohmic contacts. The gap between the electrodes is about 1 μm. A back gate, separated from the nanotube and S/D contacts by 500 nm, can be used to modulate the conductivity along the bulk of the nanotube. The background parasitic capacitance can be measured by turning off the nanotube. The oxide needs to be thick to prevent excessive loss across the MS contact via tunneling. As shown in

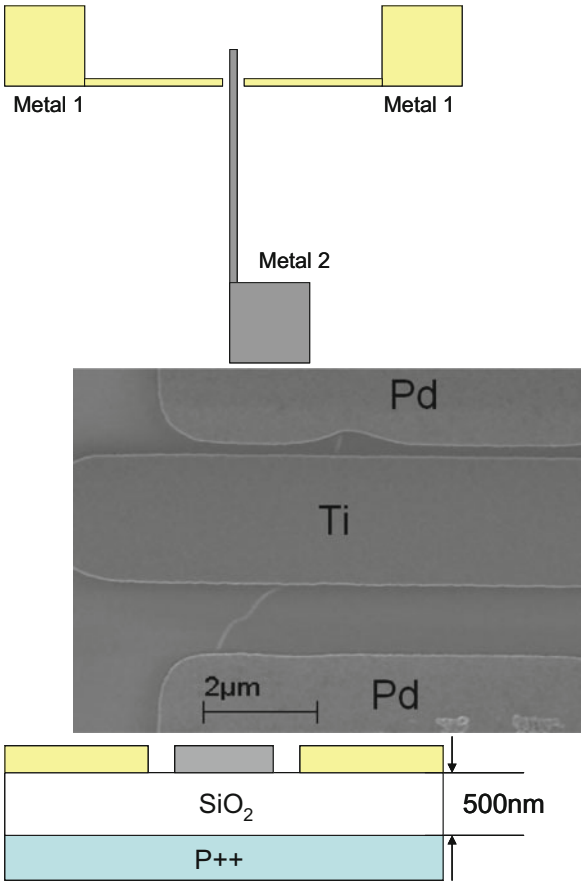

Fig. 4.20 Test structure for C-V measurement. Only one such device is placed on each 5 mm × 5 mm die to reduce background parasitic capacitances. (Reprinted from Ref. [16])

Fig. 4.20, the bonding pads are purposely placed far away (200 μm) from the device, and their area minimized to reduce shunting capacitance to ground.

The current-voltage characteristics of a Schottky diode are shown in Fig. 4.21. As expected, the device is rectifying. Qualitatively, the negative bias applied to the titanium electrode cancels the built-in voltage at the Schottky contact, turning on the diode. The negatively biased back gate electrostatically dopes the tube p-type, allowing conduction of holes in the channel. Reverse leakage starts to develop at large positive V_{ds}, when the energy bands are sufficiently bent to allow band-to-band tunneling from the valence to the conduction band of the nanotube.

4.4.2 Simulation of the C-V Measurements

We estimate the magnitude of the capacitance using a Poisson-Schrödinger solver for 1-D semiconductors [34]. The simulated structure is shown in Fig. 4.22. A

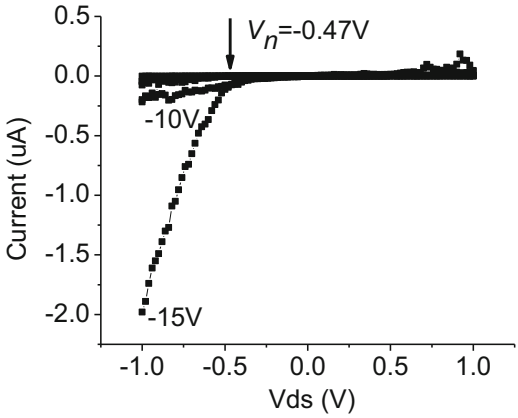

Fig. 4.21 I–V characteristics of a Pd-CNT-Ti Schottky diode, exhibiting rectifying behavior. (Reprinted from Ref. [16])

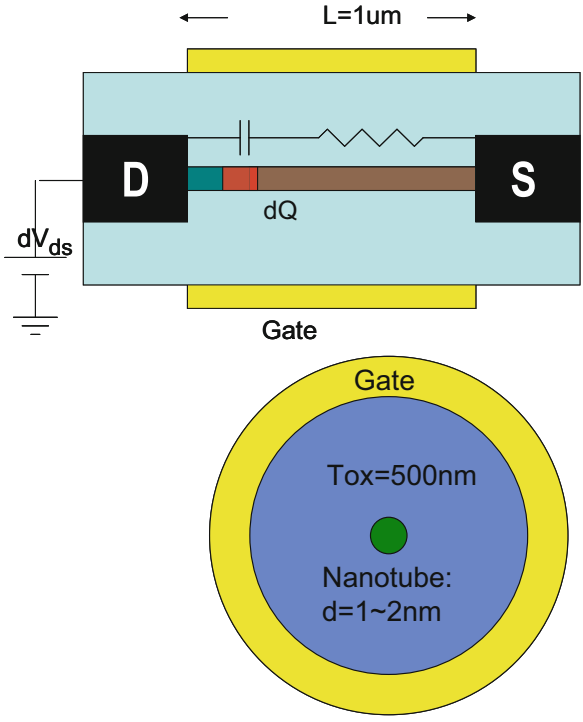

Fig. 4.22 Device structure for simulating the C-V measurement. Top: side view. Bottom: front view. (Reprinted from Ref. [16])

semiconductor CNT is surrounded by a concentric gate and gate dielectric, with the source and drain electrode at each end of the nanotube. The SBH of each contact electrode can be specified independently. To model the Ti-CNT Schottky diode, the source work function is aligned to the conduction band and that of the drain to the middle of the bandgap (Fig. 4.23). The simulation is done for electrons. Since the conduction and valence bands are symmetrical, trivial modifications lead to the same

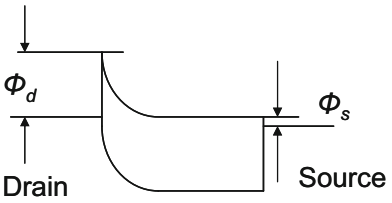

Fig. 4.23 Energy alignment in simulated device. Φ_s = SBH on source side. Φ_d = SBH on drain side. (Reprinted from Ref. [16])

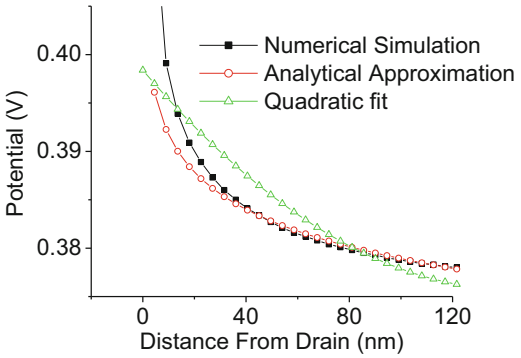

Fig. 4.24 Potential along the length of a nanotube with V_{ds} applied along its length. (Reprinted from Ref. [16])

results for holes. Although the results presented below are those of the concentric geometry, they are also applicable to a device with a planar geometry, provided that an effective dielectric constant (1.8) is utilized.

Two different C-V measurements were simulated. The first is the capacitance across the source and drain versus the voltage V_{ds} across the same two electrodes, with a fixed and non-zero gate voltage. This simulates the actual experiment where the nanotube is gated on, and V_{ds} is swept to see any change in the capacitance. This measurement is very similar to what would be done on bulk, with the exception of an extra gate terminal. The bias applied at the gate terminal can be thought as a way to electrostatically "dope" the nanotube (Fig. 4.24).

Figure 4.26a–b shows the potential and charge profile as V_{ds} is varied. As predicted from early work on electrostatic in objects with one-dimensional electronic DOS, potential applied across the long axis of the tube is poorly screened and falls as $\sim\ln(T_{ox}/x)$ along the nanotube, where T_{ox} is the dielectric thickness between the gate metal and the nanotube. This differs significantly from the textbook case of uniformly doped planar Schottky junction, where the potential falls quadratically with distance.

The simulated C-V_{ds} curves for several nanotube diameters are shown in Fig. 4.25. Obviously, it does not follow the $\sim 1/(V_{ds}\text{-}V_{bi})^{-1/2}$ rule in a planar junction. Rather, it increases very slowly and increases very steeply just before flat band, when the applied bias is about equal to the SBH. This steep increase reflects the occupation of the first sub-band as the potential profile becomes flat, as evidenced in Fig. 4.26a. As the potential profile is biased to flat-band, the quasi-Fermi level moves closer to

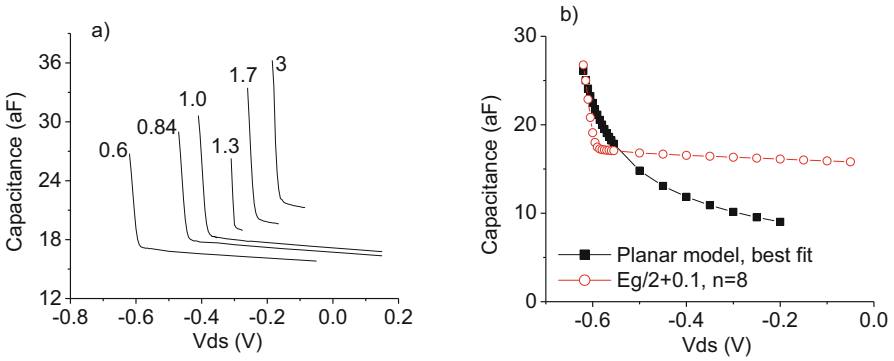

Fig. 4.25 (**a**) Simulated C-V_{ds} curves for Schottky junctions of various CNT diameters (in nm). The SBH is set as Eg/2 + 0.1 (eV). (**b**) Comparison of the simulated C-V_{ds} curve to a planar model $\sim B/(V_{bi}\text{-}V_{ds})^{0.5}$, with fitting parameter B, and $V_{bi} = 0.67$ V, the SBH in the numerical simulation. (Reprinted from Ref. [16])

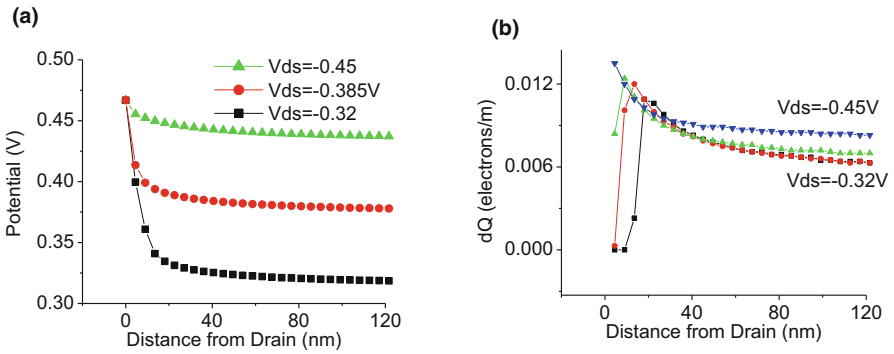

Fig. 4.26 (**a**) Potential profile near the Schottky junction for different applied bias V_{ds} across it. (**b**) Charge density dQ modulated by applied bias dV_{ds} across the source-drain of the Schottky junction. (Reprinted from Ref. [16])

the band edge, leading to a sudden increase in charge. At this condition, the same modulation dV_{ds} changes the amount of charge dQ on the tube more significantly (Fig. 4.26b), more so then a reverse-biased junction. Thus, in measuring the quantity C-V_{ds} and finding where it increases very steeply, one can readily extract the SBH of the junction.

A second useful measurement to simulate is the capacitance across the source and drain versus the gate voltage V_g, at a zero bias between the source and drain electrodes. This measurement extracts the capacitance of the junction relative to the background parasitic capacitance. This parameter represents essentially the electrostatic coupling between the drain contact and the channel, very similar to what would describe DIBL in a MOS compact model. To obtain a numerical value of the capacitance C-V_{gs}, we calculate the change in charge (dQ) on the entire tube as a

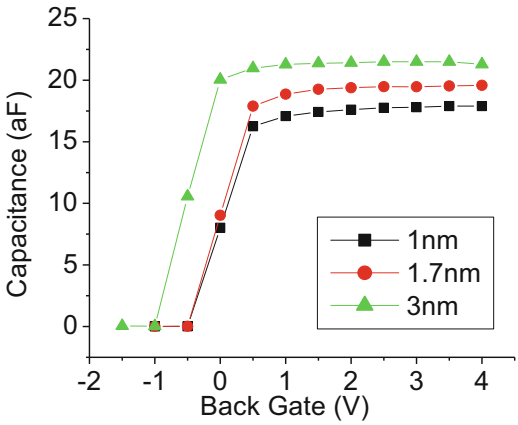

Fig. 4.27 Simulated C-V_g curves for SB diodes for three CNT diameters. (Reprinted from Ref. [16])

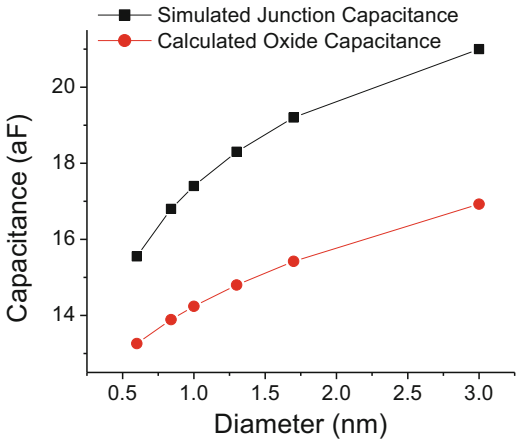

Fig. 4.28 Simulated C-V_g as a function of diameter. (Reprinted from Ref. [16])

function of a small change in the drain voltage (dV_{ds}) and set $C = dQ/dV_{ds}$. This is repeated for a range of gate voltages V_{gs}. Figs. 4.27 and 4.28 show the simulation results and the dependence on nanotube diameter. Qualitatively, this parameter is related to C_{ox} in a very simple way. As a small V_{ds} is applied, the threshold voltage V_t changes due to DIBL, and the amount of charge on the tube changes as well. An equation that describes this would be

$$dQ = C_{ox}\left(V_g - V_t\right) - C_{ox}\left(V_g - V_{t'}\right) = C_{ox}\left(V_t - V_{t'}\right) \tag{4.4}$$

where V_t, V_t, would depend on the applied V_{ds}.

A prior experimental work measured this quantity using a Coulomb blockade experiment at very low temperatures (~30 mK) and showed qualitatively the same behavior [35], though with smaller numerical value (~3 aF). This may be reconciled

with the fact that the nanotube was suspended in air, which reduces the effective dielectric constant between the drain and the channel.

4.4.3 Measurement Results

The measured C-V_g curve of a CNT Schottky diode is shown in Fig. 4.29. The measurements were performed with both the home-built bridge and the AH2700A commercial capacitance bridge. Very little loss is observed using either method. The two curves agree well, except near the threshold V_t. This is due to the larger AC excitation that is needed for the AH2700A to obtain a signal of useful size. Several control experiments were repeated with identical electrode layout, but without a nanotube in between. In all these cases, the capacitance is observed to stay constant to less than 1 aF over the full range of applied gate and source/drain biases.

The change in capacitance with applied gate bias shown in Fig. 4.29a (15aF) matches well with that expected from simulation. Comparison with the I_d-V_g characteristics shows that the abrupt increase in capacitance is due to the bulk of the nanotube becoming conductive, and the capacitance across the junction is measured in addition to the background. A qualitative agreement between simulation and measurement is also observed for the C-V_{ds} measurement shown in Fig. 4.29c. As V_{ds} becomes more negative, beyond a certain threshold, the capacitance increases steeply, until significant loss is encountered, as evidenced by the phase component in the output of the cold bridge. The rapid increase in capacitance occurs at a much smaller voltage than that required for the device to conduct. Figure 4.29e shows the C-V_{ds} curve of another device, with much better agreement between simulation and experiment. The quality of the fit differs from device to device, because many non-idealities, such as surface charges and on-tube defects, are not modeled.

C-V_g measured on 15 devices varies from about 10aF to 25aF. Plotting this change in capacitance versus the SBH extracted by the C-V_{ds} method in Fig. 4.30, a clear relationship arises, where devices having larger C-V_g also have a smaller barrier height. Using our simulator, this relationship reproduced qualitatively and is shown in Fig. 4.30. Essentially, the magnitude of the capacitance reflects simply the diameter of the nanotube, and its dependence with SBH is the result of the unpinned metal-CNT junction. As evidenced in Fig. 4.30, there is a shift when Cr, a metal with higher work function (4.5 eV), is used. Nb and Ti, being of similar work function (4.3 eV vs 4.33 eV), lead to data points that more or less overlap with one another. The size of the shift in the Cr data series (0.1–0.3 eV) is in agreement with the work function difference between Ti (Nb) and Cr, confirming once again the unpinned nature of the metal-CNT contact.

However, the measured capacitances for devices with Cr contacts differ considerably from simulation. It is possible that details of the contact geometry are different for Cr, like the case for Pd. Further modeling is warranted to fully understand the discrepancy.

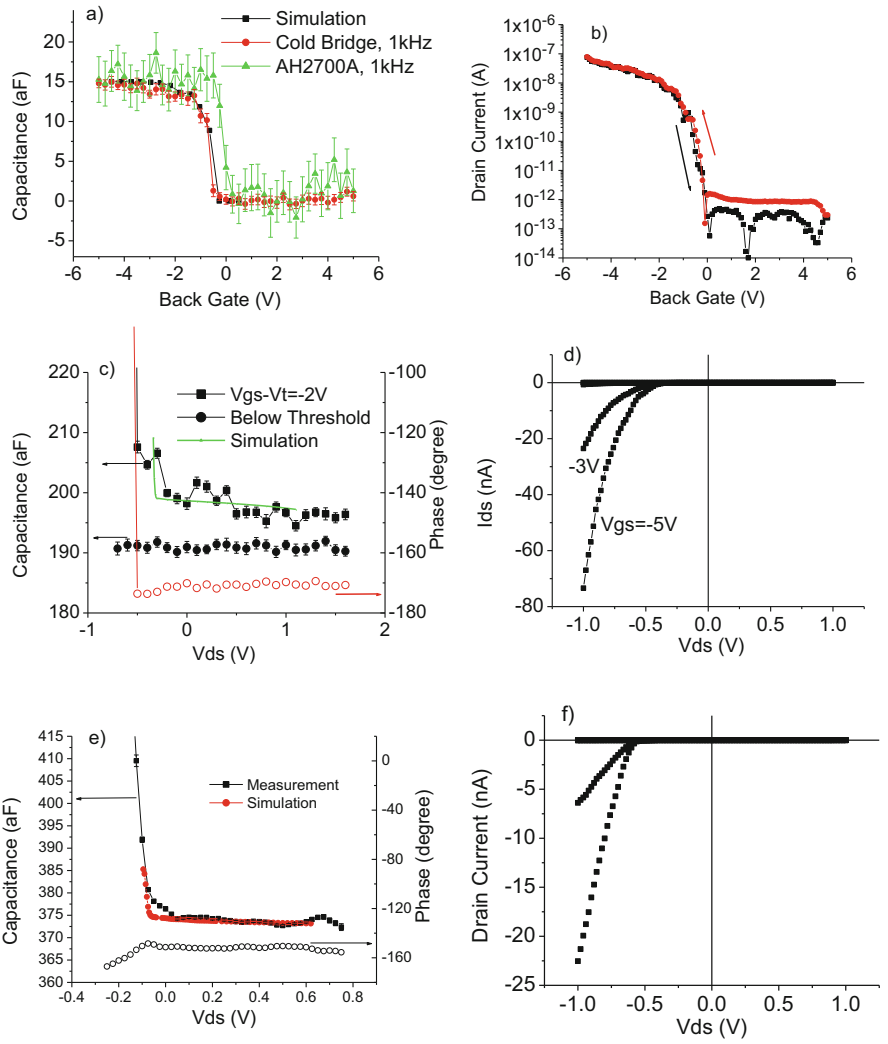

Fig. 4.29 (**a**) Capacitance across a Metal-CNT Schottky contact as a function of back gate voltage V_g, measured using both the cold bridge and a commercial bridge. (**b**) Id-V*g* characteristics of the same device (Vds = −1 V). (**c**) Capacitance as a function of voltage across the Metal-CNT Schottky contact. (**d**) I–V characteristics of the Schottky diode. (Reprinted with permission from Ref. [36]. Copyright 2010, American Institute of Physics)

4.4.4 The Geometry of Metal-CNT Contacts

Leonard predicted [37], using a side-contact geometry, that the SBH for a metal-CNT contact should fall to zero at around 1.5 nm for Pd, instead of 1 nm from ideal Schottky model (Fig. 4.31). The SBH Φ_h is well approximated by Eq. 4.5:

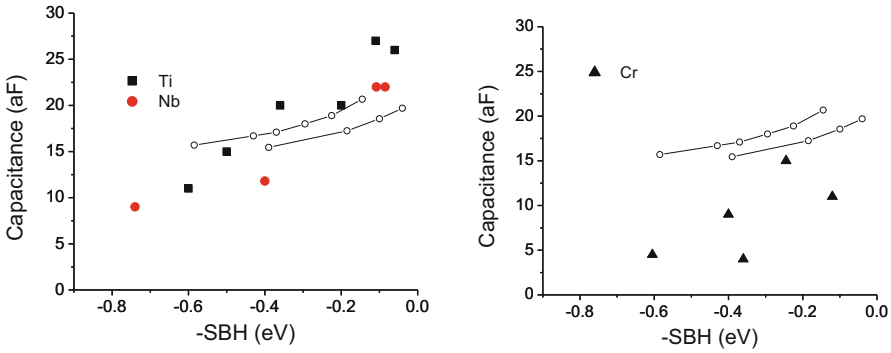

Fig. 4.30 Capacitance C-V_g as a function of measured SBH. Open symbols: simulated results. The horizontal shift comes from varying the work function of the metal contact. (Reprinted with permission from Ref. [36]. Copyright 2010, American Institute of Physics)

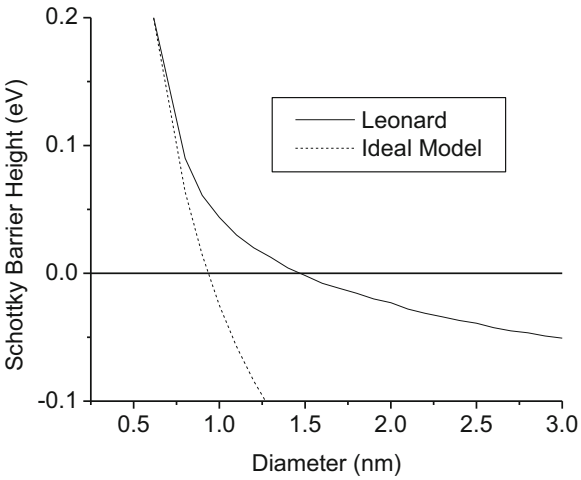

Fig. 4.31 Calculated SBH. Φ_M-$E_M = 0.38$ eV. (Reprinted from Ref. [16])

$$\Phi_h = \frac{kT}{\beta} \ln\left(\frac{\alpha\sqrt{\frac{Eg}{2kT}}}{\ln\left(\alpha\sqrt{\frac{Eg}{2kT}}\right) - \frac{\Phi_{h0}}{kT}}\right) \tag{4.5}$$

with Φ_{h0} given by Eq. 4.6, $\beta = 0.7$ and $\alpha = 4.58 \times 10^{-11}/(R * ln((R + s)/R))$, $R =$ CNT radius, and $s =$ distance between metal and CNT ~3 Å:

$$\Phi_{h0} = \frac{E_g}{2} + E_M - \Phi_M \tag{4.6}$$

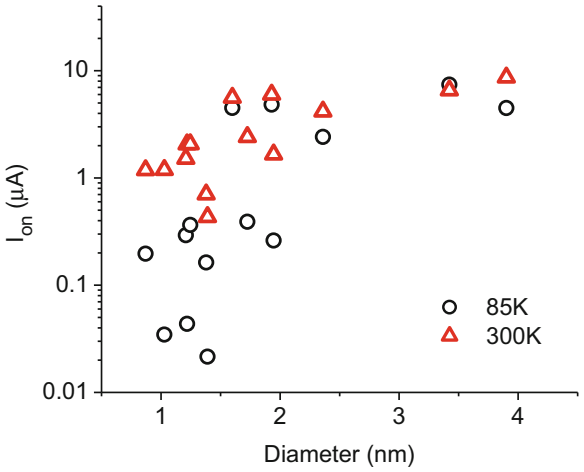

Fig. 4.32 I_{on} vs diameter at two temperatures for 14 back-gated CNT transistors with Pd S/D contacts. A sharp drop in I_{on} at low temperature is observed for all devices with diameters <2 nm. (Reprinted from Ref. [16])

The results are relatively insensitive to *s*. Although there is a possible method for measuring directly the SBH in a metal-CNT contact, as described in the previous section, a temperature-dependent measurement can explicitly show the presence of a significant Schottky barrier. Figure 4.32 shows that on-state current in Pd-contacted CNT transistors drops sharply upon cooling when $d < 1.5$–2 nm, indicating that a Schottky barrier starts to develop at that diameter, in agreement with theoretical prediction [37].

Short of a method to directly measure the SBH, it can only be extracted by fitting the I–V data to a device model [32]. For the large devices analyzed here, a compact model is suitable because of its speed and simplicity. First-principle models based on non-equilibrium green's function (NEGF) [38] would be too expensive computationally because they require specifying the potential energy to atomic scale, much too fine compared to the device dimensions here.

The details of the compact modeling can be found elsewhere [39]. Briefly, it utilizes measured device dimensions (length, oxide thickness, and CNT diameter), assumes a mobility vs length model [39], and iteratively fits to measured data by adjusting these device parameters: SBH, series resistance, and source-channel coupling capacitance C_d. It captures the effect drain on the potential in the bulk of the channel and is similar to DIBL in planar MOSFETs.

Figure 4.33 shows the SBH extracted from 25 CNT transistors with Pd contacts, using compact modeling. Although there is significant scatter, the data agrees with the side-contact model better than predictions from the ideal Schottky model in Eq. 4.6, when the same contact potential Φ_M-E_M is used. Although the ideal model agrees with the data when Φ_M-$E_M = 0.2$ eV, this would imply that the Pd work function is at the lower end of expectations. Recent four-probe measurements concluded that electrical current does flow under the metal contacts [40, 41], over a distance of several tens of nanometers.

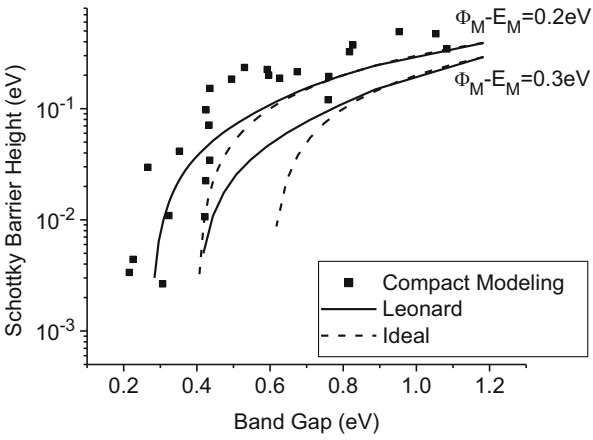

Fig. 4.33 Schottky barrier height extracted using compact modeling compared to Leonard's model and ideal Schottky model. (Reprinted from Ref. [16])

4.5 Summary and Future Work

In summary, we have developed a method to measure very small capacitances across a nanoscale Schottky diode. In our model system of Ti-CNT Schottky barrier, the experimental results match qualitatively with the calculations based on a Poisson-Schrödinger device simulator. We have extracted the Ti-CNT Schottky barrier height that is consistent with transport measurement. Capacitive measurement of the SBH across metal-CNT contacts involving different metals shows once again the unpinned nature of the contact. Nb-CNT contacts are similar to Ti, but Cr is rather different, possibly due to the effective contact area between the metal and the CNT.

The Pd-CNT contact, or any other low-barrier height contacts, is of particular interest. To measure the barrier height in these systems using the C-V method would be very difficult since these junctions are in fact very lossy capacitors. In a recent work from IBM, the series resistance from Pd-CNT contacts was examined by varying the contact length on a very long single CNT. The results there demonstrate that the effective contact length is in the order of a few hundred nanometers, in agreement with the model proposed by Leonard [37]. Thus, for Schottky contact in nanotubes, a careful consideration of the contact geometry is necessary to draw meaningful conclusions.

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Chapter 5
Metal-Semiconductor Compound Contacts to Nanowire Transistors

Renjie Chen and Shadi A. Dayeh

5.1 Introduction

Semiconductor nanowires [1–4] are promising building blocks for next-generation ultrascaled devices for electronic [5–7] and optoelectronic [8–10] applications. An important aspect for the development, maturity, and efficiency of these ultrascaled devices is the detailed understanding of and control over the phase transformation that accompanies the formation of their compound contacts for lithography-free self-aligned gate design [11, 12]. The term "compound" here refers to the formed phases that have fixed stoichiometry between metal and semiconductor elements, to be distinguished from the broader "alloy" term for phases that may include nonstoichiometric or amorphous structure. This distinction is important because the formation of a low resistance, crystalline, and thermally stable compound contact is most preferred for realizing reliable functionality in ultrascaled semiconductor transistors. Usually, the phase of compound contact and its interfacial property with semiconductor nanowire (NW) can largely affect the band alignment and charge injection in NW channels. This demands the detailed studies of the metal-semiconductor solid-state reactions, including the formed compound phases,

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reaction kinetics, and their correlation to the device performances. In this book chapter, we provide a thorough discussion of these three topics.

5.2 Phases of Metal-Semiconductor Compound Contacts

Deep knowledge on the material sciences of metal-semiconductor compound contacts is critical for achieving desired device performance for NW transistors. The development of these high-fidelity contacts should start with an understanding of the phases of the naturally or thermally formed metallic compound contacts at the metal-semiconductor junction. Ideally, a crystalline compound with low-resistivity phase is preferred as contact to a NW transistor. It has also been noticed that atomically abrupt interfaces between metallic contacts and semiconductor can help reduce the surface Fermi-level pinning and control the Schottky barrier height (SBH) [13], which is especially critical for small bandgap semiconductors (e.g., Ge, III–V, etc.) that have small electronegativity difference and a generally low index of interface behavior [14] with high density of surface and metal-induced gap states. Moreover, interfacial correlations between compound contact and semiconductor nanowire channel can further alter the electrical performances by exerted strains. Therefore, a thorough understanding of the phases and interfacial relationships for those compound contacts is needed.

Several precedent reviews [15–19] have extensively discussed the solid-state reactions between various metals and semiconductor NWs. In this chapter, we will not cover all the compound contacts to NWs with different metal-semiconductor combinations, but rather focus on several critical ones of practical importance for devices and provide in-depth discussions on the phase selection rules in low-dimensional NW semiconductor channels. A table (Table 5.3) can be found at end of this section, which summarizes the compound contacts surveyed in this chapter.

5.2.1 Metal Silicide in Si NWs

Metal silicides have long been used as the standard contacts to conventional Si CMOS devices, and the semiconductor manufacturing lines witnessed the transition from $TiSi_2$ to $CoSi_2$ and to NiSi technology due to the considerations of contact resistance and dimensional scaling [20, 21]. NiSi has demonstrated its superior properties to other candidates, such as reduced thermal budget, low resistivity, less Si consumption for ultrathin device layer, and controlled silicide formation by Ni diffusion [22–24]. Therefore, nickelide silicide shows great promise to serve as a standard contact to Si NW transistors and has been most widely studied.

In the nickel silicide reaction on thin film or bulk Si structures, δ-Ni_2Si is the single phase formed at low temperature around 200 °C, transformed to NiSi phase at

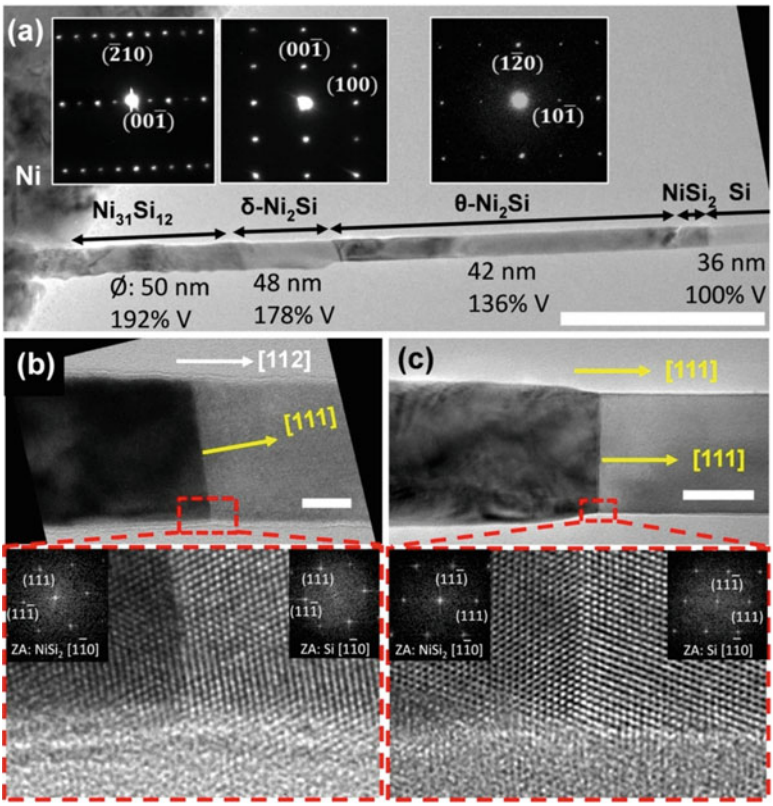

Fig. 5.1 TEM images of nickel silicide formation in a Si NW. (**a**) TEM image showing the phases that coexist during solid-state reaction between Ni pad and Si NW at 425 °C. The inserted diffraction patterns (from left to right) represent $Ni_{31}Si_{12}$, δ-Ni_2Si, and θ-Ni_2Si phases with their zone axes of [010, 120, 212], respectively. Scale bar is 400 nm. (**b**) and (**c**) TEM images with higher magnification at $NiSi_2$ and Si interfaces. Despite the Si NW growth orientations of [112] or [111], the reaction front is on a Si (111) plane. Scale bars are 20 nm and 50 nm, respectively. (Reproduced with permission from Ref. [26]. Copyright 2012 American Chemical Society)

temperatures above 350 °C, and finally converted into $NiSi_2$ phase at above 750 °C [25]. However, in Si NW channels, the phase sequences are dramatically different. As shown in Fig. 5.1a, several phases exist simultaneously upon thermal annealing of Ni pad on top of a Si NW, including $NiSi_2$ as the leading and interfacial phase in direct contact with the pristine Si NW, followed by θ-Ni_2Si, δ-Ni_2Si, and $Ni_{31}Si_{12}$ [26]. This phase sequence is generally observed under a broad range of reaction temperatures, 300~650 °C, with some minor differences (presence or absence) in some of the Ni-rich intermediate phases [27–29]. The leading phase, $NiSi_2$, has the same crystal family as pristine Si with very similar lattice constant, leading to nearly zero volume changes after $NiSi_2$ phase formation. This $NiSi_2$ phase grows on the low-energy Si (111) facets independent of the growth orientation of Si NW

(as shown in Fig. 5.1b, c), and the interfacial correlation is $NiSi_2(111)||Si(111)$ and $NiSi_2[-110]||Si[-110]$ is applicable to the various studied orientations. Near the Ni contact pad, more Ni-rich silicide phases appear, and their crystal structures, lattice constants, and volume expansions are all summarized in Table 5.3. It is worth noting that $NiSi_2$ is the phase that is thermodynamically favored to form at high temperature when Ni reacts with planar thin film or bulk Si and that θ-Ni_2Si is stable above 825 °C according to the Ni/Si phase diagram. In the following part of this section, two questions will be addressed: (1) why are the phase sequences quite different in NWs than in bulk and planar films, and (2) can the phase sequences formed in Si NW be manipulated?

To address these questions and to understand the coexistence of multiple phases (including high-temperature phases, $NiSi_2$ and θ-Ni_2Si) instead of expected NiSi phase at reaction temperatures of 300~650 °C, one need to consider the different thermodynamic treatments in two extremes of relative material abundance of the binary solid-state reactants. As we know, the driving force of silicide reaction is the total reduction of system Gibbs free energy:

$$\Delta G_f = \Delta H_f - T\Delta S_f \tag{5.1}$$

where ΔG_f, ΔH_f, and ΔS_f are the free energy, enthalpy, and entropy of formation, respectively, at a given reaction temperature. Usually, the term $-T\Delta S_f$ is negligible compared to ΔH_f for solid-state reactions at low temperatures, and therefore the system free energy is largely determined by the enthalpy term [30]. In the silicide reaction between Ni and Si bulk or thin film, Si is considered unlimited, and the enthalpy of formation for each silicide reaction is listed in Table 5.1. It can be found that the Ni_2Si has the smallest formation enthalpy (−141 kJ/mol) and therefore the largest driving force to nucleate at a low reaction temperature, while $NiSi_2$ has the largest formation enthalpy (−2 kJ/mol), and hence the $NiSi_2$ phase formation in thin film or bulk reactions is perceived as nucleation controlled, which can only occur at a temperature of above 750 °C. On the contrary, Ni is considered as an excess reservoir in the silicide reaction with NWs, and the enthalpy of formation for each silicide reactions is listed in Table 5.2. It's clear that several phases, including $NiSi_2$, Ni_2Si, and $Ni_{31}Si_{12}$, have small enough enthalpies that allow the formation of multiple phases simultaneously during the silicide reaction. This also indicates that nucleation is no longer the limiting step in determining the leading phase of $NiSi_2$, and kinetic competitive growth models suggest that the faster growth rate will separate the leading phase with the others [31]. At the same time, we should also consider the existence of θ-Ni_2Si phase, which is a high-temperature phase that is stable above 850 °C. In situ X-ray diffraction studies of NiSi substrate reaction show that θ-Ni_2Si is a transient phase, which may appear at low temperatures but is later consumed by δ-Ni_2Si phase with temperature increase [32], which is in agreement with the observations made on the reaction of Ni with Si NWs [26]. Another experiment to test the stability of θ-Ni_2Si phase suggests that high temperature formed θ-Ni_2Si phase transformed into δ-Ni_2Si and ε-Ni_3Si_2 during cooling down

Table 5.1 Enthalpy of formation for each silicide reaction with excess Si reservoir (thin film or bulk reactions)

Reactions	ΔH_f (kJ · mol^{-1})	ΔH_f (kJ · cm^{-3})	Molar volume (cm^3)
$2Ni + Si = Ni_2Si$	−141	−7.08	19.9
$3Ni_2Si + Si = 2Ni_3Si_2$	−15	−0.43	34.4
$Ni_3Si_2 + Si = 3NiSi$	−11	−0.75	14.6
$Ni_2Si + Si = 2NiSi$	−16	−1.09	14.6
$NiSi+Si = NiSi_2$	−2	−0.07	23.6

Values adapted from Ref. [34]

Table 5.2 Enthalpy of formation for each silicide reactions with excess Ni reservoir (NW reactions)

Reactions	ΔH_f (kJ · mol^{-1})	ΔH_f (kJ · cm^{-3})	Molar volume (cm^3)
$2Si + Ni = NiSi_2$	−88	−3.72	23.6
$NiSi_2 + Ni = 2NiSi$	−42	−2.90	14.6
$NiSi+Ni = Ni_2Si$	−55	−2.74	19.9
$Ni_2Si + 3Ni = 2Ni_2Si$	−97	−4.87	19.9
$12Ni_2Si + 7Ni = Ni_{31}Si_{12}$	−1819	−6.39	284.7

Values adapted from Refs. [21, 34]

below 825 °C, while on the other hand, that low temperature (460 °C) formed θ-Ni_2Si phases didn't decompose even during cooling down to room temperature [33]. These observations suggest that, although θ-Ni_2Si is a high-temperature stable phase, it also retains a certain type of stability at low temperatures, likely due to high kinetic barriers for phase transformation.

Many studies were carried out to control the phase formations in Si NW templates [27–29, 35–37]. These studies were driven with the desire to eliminate the Ni-rich silicide phases (e.g., $Ni_{31}Si_{12}$) that generally have higher resistivity which compromises the series resistance in NW transistors. A dielectric shell (SiO_2 [27, 35] or Al_2O_3 [29]) coating can exert a compressive stress to the silicide core and suppress the formation of phases that have high-volume expansion ratios. This is because high compressive stresses squeeze the interstitial sites through which Ni diffuses, increasing the activation barrier of Ni diffusion. As shown in Fig. 5.2a–d, an ALD Al_2O_3 layer with a thickness of 22 nm on a Si nanowire with a diameter of ~50 nm can effectively exclude $Ni_{31}Si_{12}$ phase in the formed nickel silicide sequence. Importantly, the leading silicide phase in direct contact with pristine Si determines the SBH and consequently charge injection/extraction, and therefore a better control of the leading phases could potentially fulfill various device functionalities. Since coexistence of multiple nickel silicide phases in NW is thermodynamically preferred, the leading phase adjustment relies on the kinetic competitions [28, 37]. It has been found that $NiSi_2$ growth rate is limited by interfacial reactions (the kinetic limiting steps will be revisited in Sect. 5.3) and remains constant at a given temperature despite the NW size. On the contrary, θ-Ni_2Si growth is diffusion limited and the

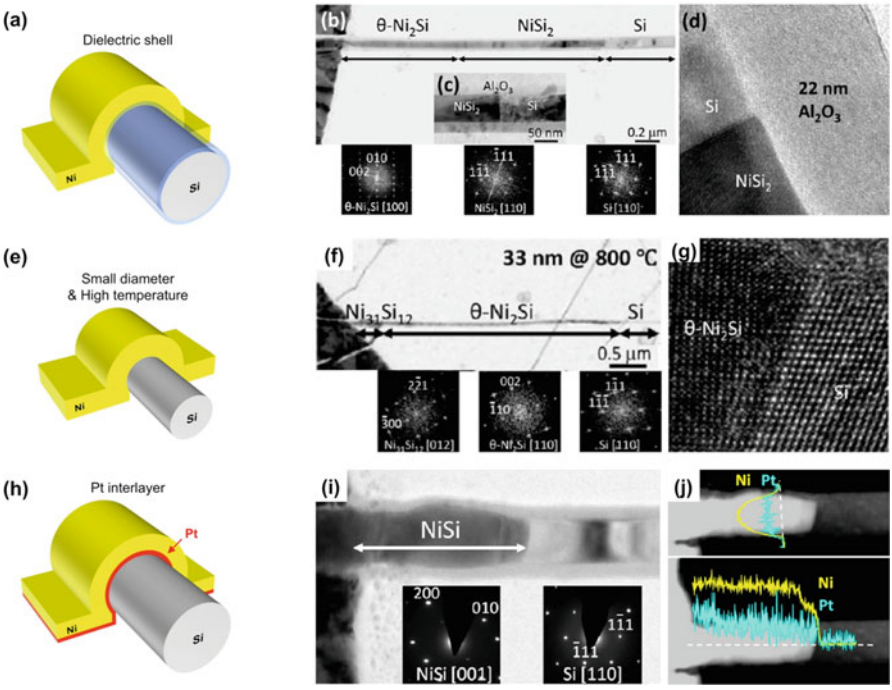

Fig. 5.2 Manipulation of nickel silicide phases in Si NW templates. (**a**) Schematic of reaction between Ni and Si NW with dielectric shell coating. (**b**–**d**) TEM images of nickel silicide growth in a Si NW with a thick (22 nm) Al_2O_3 shell at 800 °C for 30s. The leading phase is $NiSi_2$, and the $Ni_{31}Si_{12}$ phase with highest volume change is suppressed. (e) Schematic of reaction between Ni and Si NW with small diameter at high temperature. (**f**–**g**) TEM images of nickel silicide growth in a thin (33 nm) Si NW at 800 °C for 30s. The leading phase is θ-Ni_2Si in this case. (**h**) Schematic of reaction between Ni and Si NW with a thin Pt interlayer. (**i**–**j**) TEM image and elemental mapping of nickel silicide growth in a ~70 nm Si NW with 5 nm Pt interlayer and a thick Al_2O_3 shell, at 450 °C for 2.5 h. The leading phase and the only phase is NiSi. (TEM images are reproduced with permission from Refs. [28, 29]. Copyright 2012, 2013 American Chemical Society)

diffusion rate can significantly increase in Si NWs with smaller diameter. At a high reaction temperature, where stable θ-Ni_2Si phase is favored, there exists in principle a transition diameter, below which θ-Ni_2Si would be favored over $NiSi_2$ as the leading phase. Chen and et al. [28] derived this critical diameter of 234 nm, by extracting the diffusivity (D) of Ni in θ-Ni_2Si and the reaction constant (k) at $NiSi_2$/Si interface and setting the average growth rates of these two phases to be equal. Figure 5.2e–g demonstrates the feasibility of formation of θ-Ni_2Si as leading phase in a small (33 nm in diameter) Si NW at reaction temperature of 800 °C.

Thus far, the most preferred low-resistivity NiSi phase in bulk NiSi reaction was not yet observed in NiSi NW reaction and was only reported in point contact reaction in Si NWs [38, 39]. In order to manipulate the NiSi phase formation, Chen and et al. [29] inserted a very thin layer of Pt in between Ni pad and Si NW, schematically shown in Fig. 5.2h. Pt has a higher solubility in NiSi phase than that in $NiSi_2$ [40],

because the PtSi and NiSi share the same crystal structure with similar lattice constant and could potentially form solid solution [41]. Therefore, Pt promotes the NiSi phase formation rather than $NiSi_2$, and by combing the constraining dielectric shell (to suppress Ni-rich silicide phases), a single NiSi phase was experimentally observed as shown in Fig. 5.2i, j.

5.2.2 *Metal-Germanide in Ge NWs*

Benefiting from the intrinsically higher hole mobility, Ge NWs hold a great promise in PMOS devices, together with GeSi alloy [42] or Ge/Si core/shell [43] NWs. Similar to the case of Si, Ni is also the promising candidate for contact to p-type Ge, due to the small SBH and the ease of formation of Ni_xGe compounds. By virtue of being a group IV semiconductor, Ge has the same diamond lattice structure as Si, and many similarities exist between metal-germanide reactions and metal-silicide ones. In this section, we will review the different behaviors of metal-germanide phase formation in Ge NWs.

Firstly, no conclusive phase sequences have been observed in Ni reacting with Ge NWs over a broad reaction temperature range, and different Ni germanide phases have been reported at different reaction temperatures. Dellas et al. [44] carried out the solid-state reaction between a Ni pad and a Ge NW at the temperature range of 300~400 °C. The formed polycrystalline Ni_xGe phase (shown in Fig. 5.3a) was found to match Ni_2In prototype structure (hexagonal crystal structure) with the $P6_3/mmc$ space group. They pointed that the stoichiometry of Ni_xGe may deviate from $x = 2$ due to vacancies on one of the Ni sub-lattices [45], leading to similar lattice constants for several germanide phases (Ni_2Ge, Ni_5Ge_3, $Ni_{19}Ge_{12}$, $Ni_{17}Ge_{12}$, and Ni_3Ge_2) [46]. In comparison, their experimentally observed diffraction data was most consistent with Ni_3Ge_2 phase. They also reported that this germanide phase was independent of Ge NW growth orientations, and that further increase of reaction temperatures above 450 °C would lead to a decomposition and discontinuity in germanide segment, the reasons of which were not clear. Tang et al. [47] reported the Ni germanide reaction in <111> Ge NWs at the temperature range of 400~500 °C and observed a single crystalline orthorhombic Ni_2Ge phase (shown in Fig. 5.3b). They found an abrupt interface between Ni_2Ge and Ge NW, and the interfacial correlation was $Ni_2Ge\ (100) \parallel Ge\ (1\bar{1}\bar{1})$ and $Ni_2Ge\ [0\bar{1}1] \parallel Ge\ [01\bar{1}]$. At the reaction temperature of 650 °C, the same group reported cubic Ni_3Ge phase (shown in Fig. 5.3c) with same cubic structure to Ge [18]. Their observations have shown very similar lattice constant between Ni_3Ge and Ge with only ~1.5% lattice mismatch, which was different from the conventional lattice constant for cubic Ni3Ge phase [48, 49], as summarized in Table 5.3. Similar to Si NWs, oxide confinement was also found to suppress the formation of Ni-rich germanide that had large volume expansions. An Al_2O_3 shell coating led to the formation of

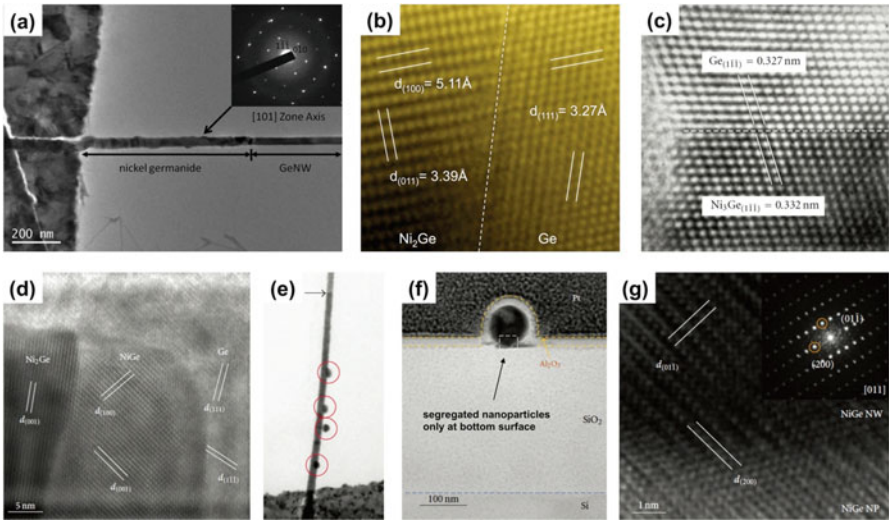

Fig. 5.3 Different Ni_xGe/Ge NW interfaces at different reaction temperatures. (**a**) Ni_3Ge_2 phase formed at 400 °C for 2 min anneal. Reprinted with permission from Ref [44]. Copyright 2010 American Institute of Physics. (**b**) Ni_2Ge phase formed at 500 °C for 60s anneal. (**c**) Ni_3Ge phase formed at 650 °C. (**d**) NiGe phase formation at 450 °C, with Al_2O_3 shell confinement. (**e**) Segregation of Ni_xGe nanoparticles upon thermal anneals. (**f**) Cross-sectional TEM of germanide nanowire coated with Al_2O_3 shell. There are segregated nanoparticles underneath the nanowire, the region that is not covered by Al_2O_3. (**g**) HRTEM image of the germanide phase in (**f**), which is NiGe. ((**b**–**g**) are reproduced with permission from Ref. [18]. Copyright 2011 Jianshi Tang et al.)

orthorhombic NiGe phase (shown in Fig. 5.3d) in adjacent to pristine Ge NW followed by Ni_2Ge phase, at reaction temperature of 450 °C.

Secondly, the nickel germanide reaction is usually accompanied with segregation of Ni_xGe nanoparticles. Tang et al. [18] found that the segregation of Ni_xGe nanoparticles could be caused by two factors, the instable native oxide, GeO_x, and the large lattice mismatch. As shown in Fig. 5.3e, with elongated reaction time Ni_xGe nanoparticles gradually formed at the surface of a germanide segment. When confined by the Al_2O_3 shell, Tang et al. have shown these segregated nanoparticles could be effectively suppressed, as shown in the NW cross section in Fig. 5.3f, except the bottom surface on substrate where the Al_2O_3 shell was not conformal. It's worth noting that the germanide phase here with an Al_2O_3 shell confinement was found to be NiGe as validated in Fig. 5.3g and had a large lattice mismatch of 77.7% with the Ge interface. This large lattice mismatch is another contributor to the formation of segregated nanoparticles at the non-coated surface. One possible way to eliminate the segregation is to introduce a Ni point contact on the Ge NW, benefiting from the smaller Ni flux through the limited contact area [18].

Table 5.3 Summary of several commonly observed phases when metal and semiconductor NWs form compound metallic contacts

Phases	Reaction condition	Crystal structure	Lattice constant			Volume Change	Interfacial plane structure	Refs.
			a (Å)	*b* (Å)	*c* (Å)			
Si NW		Cubic	5.431	–	–	1		
$NiSi_2$	300~650 °C	Cubic	5.406	–	–	0.99	$NiSi_2$ (111) ‖ Si (111)	●[26, 28, 29]
							$NiSi_2$ [−110] ‖ Si [−110]	
NiSi	450 °C	Orthorhombic	5.659	5.233	3.258	1.21	NiSi (−110) ‖ Si (1–11)	●[29]
	Al_2O_3 shell and Pt interlayer						NiSi [001] ‖ Si [110]	
θ-Ni_2Si	800 °C	Hexagonal	3.805	–	4.890	1.54	θ-Ni_2Si [110] ‖ Si [110]	●[28]
	small *radius*							
δ-Ni_2Si	300~650 °C	Orthorhombic	5.004	3.722	7.068	1.65	–	●[26, 70]
$Ni_{31}Si_{12}$	300~650 °C	Hexagonal	6.671	–	12.288	1.99	–	●[26, 71]
PtSi	520 °C	Orthorhombic	5.935	5.596	3.604	1.49	PtSi (101) ‖ Si (111)	●[72]
							PtSi [010] ‖ Si [1–10]	
$CoSi_2$	800 °C	Cubic	5.365	–	–	0.96	$CoSi_2$ (−111) ‖ Si (−111)	●[73]
							$CoSi_2$ [110] ‖ Si [110]	
MnSi	650 °C	Cubic	4.556	–	–	1.18	MnSi(−2–14) ‖ Si(345)	●[74]
							MnSi [1–20] ‖ Si[3–1-1]	
GeNW		Cubic	5.658	–	–	1		
Ni_3Ge_2	300~400 °C	Hexagonal	3.95	–	5.187	1.55	–	●[44]
Ni_2Ge	400~500 °C	Orthorhombic	5.11	3.83	7.26	1.57	Ni_2Ge (100) ‖ Ge (1–1-1)	●[47]
							Ni_2Ge [0–11] ‖ Ge [01–1]	
Ni_3Ge	650 °C	Cubic	?5.75	–	–	?1.05	Ni_3Ge (111) ‖ Ge (111)	●[18]
			3.572			2.01	Ni_3Ge [110] ‖ Ge [110]	□[48, 49]
NiGe	450 °C	Orthorhombic	5.38	3.42	5.81	1.18	NiGe (001) ‖ Ge (1–1-1)	●[75]
	Al_2O_3 shell						NiGe [010] ‖ Ge [01–1]	
Cu_3Ge	310 °C	Orthorhombic	5.28	4.22	4.54	2.23	Cu_3Ge(211) ‖ Ge (1–11)	●[76]
							Cu_3Ge[−102] ‖ Ge [−112]	

(continued)

Table 5.3 (continued)

Phases	Reaction condition	Crystal structure	Lattice constant			Volume Change	Interfacial plane structure	Refs.
			a (Å)	*b* (Å)	*c* (Å)			
Mn_5Ge_3	450 °C	Hexagonal	7.18	–	5.05	1.67	Mn_5Ge_3(0001) ‖ Ge(001)	●[77]
							Mn_5Ge_3[−12–10] ‖ Ge [110]	
$In_xGa_{1-x}As$		Cubic	5.6533 + 0.405x					
Ni_3InAs	220~300 °C	–	–	–	–	–	Ni_3InAs(−1–10) ‖ InAs(−110)	●[55]
							Ni_3InAs[001] ‖ InAs [112]	
Ni_3InAs	High T	Orthorhombic	5.71	6.84	3.75	1.32	Ni_3InAs(001) ‖ InAs(001)	●[58]
	Theoretical						Ni_3InAs [110] ‖ InAs [100]	
$Ni_2In_{0.53}Ga_{0.47}As$	250~350 °C	Hexagonal	3.93	–	5.10	1.34	$Ni_2In_{0.53}Ga_{0.47}As$ (0001) ‖ $In_{0.53}Ga_{0.47}As$ (111)	●[67]
							$Ni_2In_{0.53}Ga_{0.47}As$ [−12–10] ‖ $In_{0.53}Ga_{0.47}As$ [0–11]	□[65, 66, 68]
Ni_2GaAs	200~400 °C	Hexagonal	3.84	–	4.96	1.40	Ni_2GaAs (0001) ‖ GaAs (111)	□[60, 61]
							Ni_2GaAs [11–20] ‖ GaAs [1–10]	
Ni_xGaAs ($x = 2$~3)	200~400 °C	Hexagonal	3.79~3.90		5.01~5.07	1.38~1.48	–	□[62–64]

Note: "●" represents the studies carried out in NW channels, while "□" represents the studies on planar films

5.2.3 Metal and III-V Compound Contacts

Continued progress in increasing transistor density incurs power dissipation constraints in MOSFET scaling [50], which may substantially elevate the packaging and cooling cost and make the chips impractical for most applications. One hasty way to lower the power consumption is to reduce the operation voltage, which would in return compromise the logic gate switching speeds [51]. A possible solution is to introduce a channel material in which the charge carriers travel faster than in conventional Si channels, allowing a lower operation voltage without sacrificing device performances. Therefore, III–V compound semiconductors, especially $In_xGa_{1-x}As$ ($0 \leq x \leq 1$), are regarded as potential replacement candidates due to their high electron mobility [19].

In order to take full advantages of the mobility enhancement, the contact requirements become very stringent for III–V transistors [52]. There are several general considerations for the metal contact to III–V transistors. Since more than two elements are involved in the solid-state reactions between contact metal(s) and III–V compound semiconductors, fundamental studies become more difficult in these multi-compound reactions. Simultaneously, a technical concern arises for the instability of the compound contact to III–V materials under elevated thermal processes [53], and therefore the electronic properties of compound contacts need to be carefully coordinated with the studies of their morphologies and phases. Despite the well-established contact theory in planar III–V channels [53, 54], only few detailed studies have been carried out on compound contacts in III–V nanostructures.

Chueh et al. [55] were the first to demonstrate the fabrication of Ni_xInAs compound contact in vapor-liquid-solid (VLS) grown InAs NWs, by reacting Ni pad with <110>-oriented InAs nanowires at 220~300 °C. The Ni_xInAs/InAs heterojunction showed an atomically abrupt interface, with the epitaxial relationship of $Ni_xInAs(\bar{1}\bar{1}0) \parallel InAs\ (\bar{1}\bar{1}0)$ and Ni_xInAs [001] ‖ InAs [112]. Their EDS analysis gave a Ni:In:As atomic ratio of 58:22:20, suggesting the ternary phase as Ni_3InAs. Limited by the InAs NW growth orientation and the TEM viewing zone axes, details on the crystal structure and lattice constant of Ni_3InAs phase were not reported. In their following studies, a Ni:In:As atomic ratio of 49:25:26 was found in the reaction of Ni with planar InAs [56], and the Ni_2InAs stoichiometry was also found in NW channels [57].

Later, Schusteritsch et al. [58] presented a first-principle calculation for the composition of this Ni_xInAs compound contact. They used ab initio random structure searching (AIRSS) approach to determine the value of x and found that the Ni_3InAs phase has the lowest formation enthalpy among others ($x = 1$~6). For the different possible crystal structures of Ni_3InAs, their calculations showed that an orthorhombic structure with Pmmn space group gave the lowest formation energy, which was not observed in the limited experimental data [59]. The possible reason of the difference between first-principle simulation and experimental observations, as they also pointed out in the paper, can be intuitively concluded from our discussions

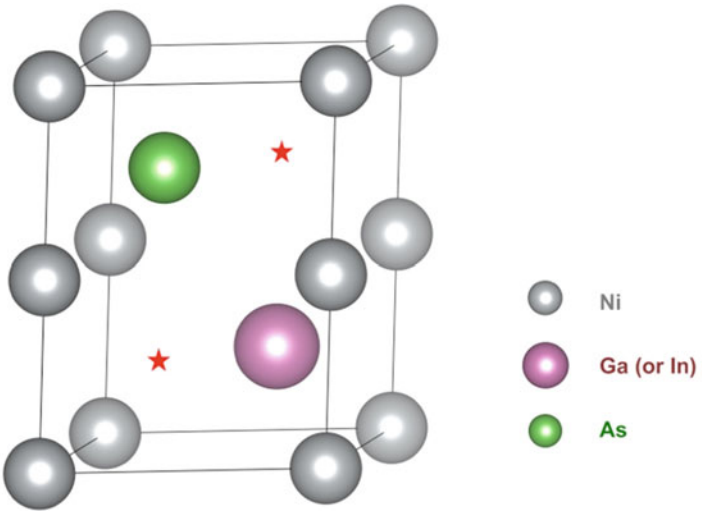

Fig. 5.4 Lattice structure of Ni_xGaAs. In principle, the stoichiometry can have a range of $x = 2$~4. The schematic shows Ni_2GaAs, and extra Ni atoms can occupy one or both of the "★" sites to form Ni_3GaAs or Ni_4GaAs, respectively

in the Si NW Sect. 5.2.1 above, as the phase selection is not only determined by thermodynamics but also by kinetic competition, volume expansion, lattice mismatch, etc.

In fact, the stoichiometry has long been an argument in Ni_xGaAs compound contact to GaAs thin film structures [60–64]. Ni_xGaAs was observed as hexagonal lattice system, adopting NiAs (B8) crystal structure, with the value of x ranging in principle from 2 to 4 and the experimentally observed range to be within 2 to 3. As shown in Fig. 5.4, Ni atoms occupy the corner sites (0, 0, 0) and the edge sites (0, 0, 1/2), forming the hexagonal frame. Ga and As atoms occupy the (1/3, 2/3, 3/4) site and (2/3, 1/3, 1/4) site, respectively. There are still other two empty sites (1/3, 2/3, 1/4) and (2/3, 1/3, 3/4) that Ni can selectively occupy resulting in the possible stoichiometry of x from 2 to 4. Following experimental results presented in [65–68], we will show that stoichiometry of $x = 2$ is the most commonly observed crystalline phase in $In_{0.53}Ga_{0.47}As$, as further squeezing of Ni in between the closely packed atoms becomes impractical.

We investigated the compound contact formation between Ni and $In_{0.53}Ga_{0.47}As$ NWs (the stoichiometry of $In_{0.53}Ga_{0.47}As$ originates from its epitaxial growth nature on InP substrate). These $In_{0.53}Ga_{0.47}As$ NWs are top-down etched from a 50 nm thin film, which has been pristinely transferred on insulator on Si substrate [67, 69]. There are several advantages of doing this: (i) top-down etched and horizontal lying NWs (or Fins) have more flexibility for the selection of size, length, and alignment to certain crystal orientations, and the fabrication approach is CMOS compatible; (ii) functional III–V transistors on Si substrate are always desired from a cost-effective aspect of industrial fabrication; (iii) studying the solid-state reactions

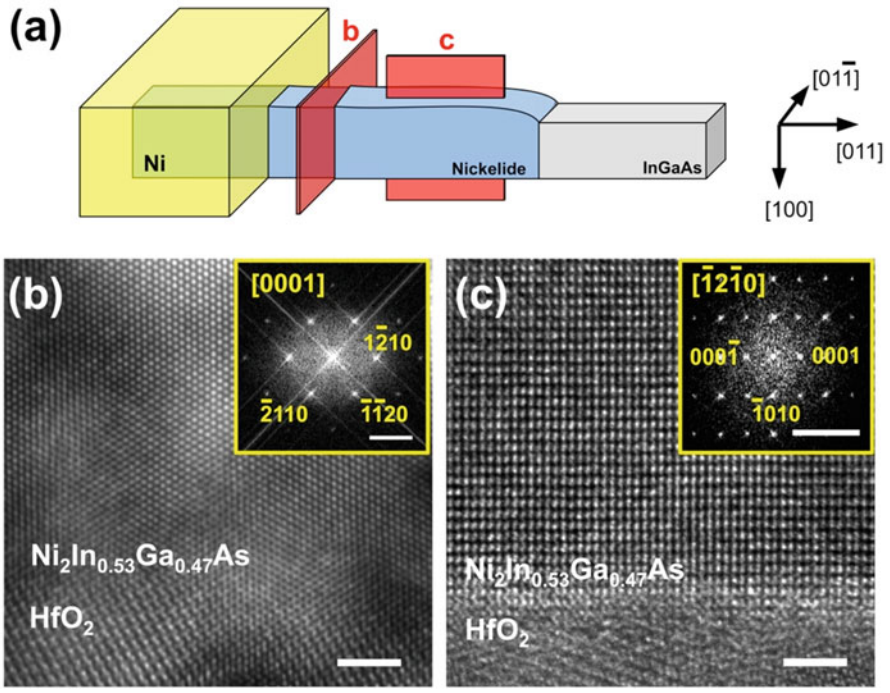

Fig. 5.5 Crystal structure analysis of nickelide phases. (**a**) Schematic illustration of the relative positions of FIB cut lamellas for panels b−c. HRTEM images of nickelide phase with FIB cut lamellas (**c**) along NW orientation and (**b**) perpendicular to the NW orientation. The nickelide phase was identified as $Ni_2In_{0.53}Ga_{0.47}As$ with (0001) plane perpendicular to the NW orientation. Scale bars are 2 nm for all HRTEM images and 5 nm^{-1} for all FFT images. (Reprinted with permission from Ref. [67]. Copyright 2015 American Chemical Society)

between metal and III–V on insulator can eliminate interfering influences and reactions with the III–V growth substrate. Details of the reaction between Ni and an $In_{0.53}Ga_{0.47}As$ [011] NW that has rectangular cross section are schematically shown in Fig. 5.5a. In order to identify the phase of $Ni_xIn_{0.53}Ga_{0.47}As$ (referred to as "nickelide" for simplicity), focused ion beam (FIB) lamellas were prepared in two orientations as indicated by the red planes of Fig. 5.5a. From the corresponding TEM images in Fig. 5.5b, c, we extract the lattice constant of the nickelide structure and identify it as hexagonal $Ni_2In_{0.53}Ga_{0.47}As$ phase through comparison to the known lattice values in the literature [65, 66]. This two-zone detection method eliminates possible errors in extracting the lattice constant associated with single-zone detection and provides an example to identify unknown phases with complicated compositions.

Unlike multiple silicide phases coexisting during the nickel silicide reaction in Si NWs, the nickelide segment in $In_{0.53}Ga_{0.47}As$ NW exhibited a single phase, $Ni_2In_{0.53}Ga_{0.47}As$, as shown in Fig. 5.6. Interestingly, the $Ni_2In_{0.53}Ga_{0.47}As$ crystal undergoes a gradual rotation from the reaction interface toward the Ni reservoir. The

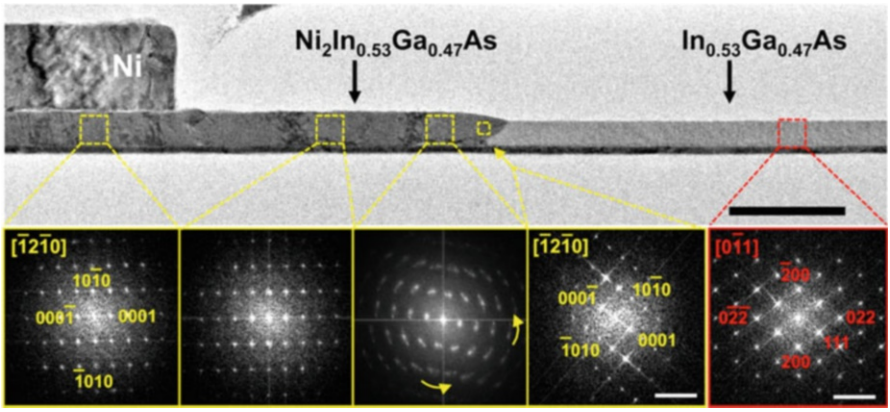

Fig. 5.6 Cross-sectional TEM image of the entire nickelide region. The fast Fourier transform (FFT) patterns were collected from different regions along the NW. The nickelide (0001) plane is well aligned with $In_{0.53}Ga_{0.47}As$ (111) plane at the interface. But away from the interface, there is a gradual rotation of the crystal structure to maintain an equilibrium [0001] nickelide axis parallel to the NW [011] direction. Scale bar is 200 nm for the TEM image and 5 nm^{-1} for all FFT patterns. (Reprinted with permission from Ref. [67]. Copyright 2015 American Chemical Society)

interface at the reaction front is $Ni_2In_{0.53}Ga_{0.47}As$ (0001) ‖ $In_{0.53}Ga_{0.47}As$ (111) with the $Ni_2In_{0.53}Ga_{0.47}As$ [0001] direction pointing 35.3° below the NW axis orientation of [011]. Far away from the interface, the $Ni_2In_{0.53}Ga_{0.47}As$ [0001] direction is parallel to the [011] NW channel orientation. The crystal rotation of $Ni_2In_{0.53}Ga_{0.47}As$ phase happens within about 200 nm near the $Ni_2In_{0.53}Ga_{0.47}As$/$In_{0.53}Ga_{0.47}As$ interface and undergoes a gradual change with defective crystallites (FFT pattern shows continuous arc for each diffraction spot rather than the paired sharp spots for twinned structures). Throughout the whole range of nickelide segment, the zone axes were fixed as $[\bar{1}2\bar{1}0]$, with $Ni_2In_{0.53}Ga_{0.47}As$ $[\bar{1}2\bar{1}0]$ ‖ $In_{0.53}Ga_{0.47}As$ $[0\bar{1}1]$. On the basis of these observations, we speculate that the nickelide phase growth starts with the energy preferred epitaxial planar interface of $Ni_2In_{0.53}Ga_{0.47}As$ (0001) ‖ $In_{0.53}Ga_{0.47}As$ (111), and undergoes a post-growth crystal rotation to form the low-energy $(10\bar{1}0)$ top surface [67].

A closer look at the interfacial structure can be found in the HRTEM image in Fig. 5.7a. Here, we deduce that the nickelide phase growth follows layered steps from the top surface toward the bottom as indicated by the yellow arrows. This saw-tooth interface is believed to relax the strains at the growth interface. To better understand how Ni atoms fill into the lattice of $In_{0.53}Ga_{0.47}As$ and to briefly estimate the strain at the interface, we draw the atomic models for $In_{0.53}Ga_{0.47}As$ and $Ni_2In_{0.53}Ga_{0.47}As$ in Fig. 5.7b with their interfacial planes lying horizontally. In (or Ga) and As atoms have hexagonal arrangement inside the (111) planes, and upon $Ni_2In_{0.53}Ga_{0.47}As$ formation, Ni diffuses in between each In (or Ga) and As layers and breaks the bonds between these particular layers. Inside each layer, atoms remain in the hexagonal arrangement, and the atom-to-atom spacing decreases by

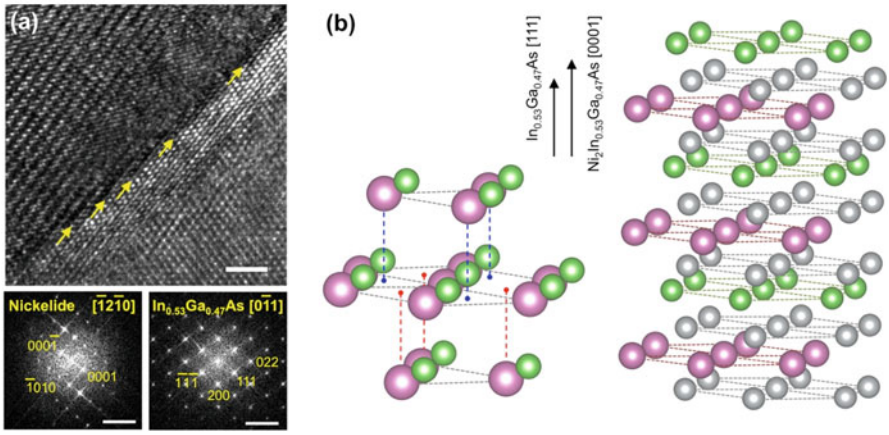

Fig. 5.7 TEM characterization and structural analysis of the $Ni_4In_{0.53}Ga_{0.47}As/In_{0.53}Ga_{0.47}As$ interface. (**a**) HRTEM image at the nickelide (dark contrast) $In_{0.53}Ga_{0.47}As$ (bright contrast) interface. The yellow arrows indicate the layered growth of nickelide on the interfacial plane of $Ni_4In_{0.53}Ga_{0.47}As$ (0001) ‖ $In_{0.53}Ga_{0.47}As$ (111) from top surface toward the bottom interface with HfO_2. (**b**) Atomic models of $In_{0.53}Ga_{0.47}As$ and $Ni_2In_{0.53}Ga_{0.47}As$ aligned along their [0001, 111] directions, respectively. The atomic models clearly indicate the nature of Ni squeezing in between each In (or Ga) and As layers. (Reproduced with permission from Ref. [67]. Copyright 2015 American Chemical Society)

~5.5% (according to their lattice constants summarized in Table 5.3). However, in the direction perpendicular to the interfacial plane, the layer-to-layer spacing of same atom increases by ~50.5%. Therefore, the $In_{0.53}Ga_{0.47}As$ NW at the reaction interface experiences compressive stresses from both inside the interfacial plane due to lattice mismatch and perpendicular to the interfacial plane due to volume expansion in the reacted nickelide phase. The effect of strain on semiconductor energy band-edge structures is discussed in Sect. 5.4 of this chapter. Moreover, one could notice from the atomic models that further formation of $Ni_xIn_{0.53}Ga_{0.47}As$ ($x > 2$) phases needs much higher energy for Ni to squeeze in between the closely packed III or V atoms inside each layer, and therefore a crystalline $Ni_2In_{0.53}Ga_{0.47}As$ phase is observed over the entire reaction temperature of 250~350 °C. Higher reaction temperatures above 400 °C usually lead to deposition of the nickelide phase [63, 64].

5.3 Kinetics of the Solid-State Reaction Between Metal and Semiconductor NWs

The implementation of metal-semiconductor compounds as standard contacts to NW field-effect transistors (FETs) urges understanding and control over the dynamic processes in this metal-semiconductor solid-state reaction beyond the knowledge of phases discussed in Sect. 5.2. On one hand, the kinetics in NW reactions can be quite

different from that in thin film or bulk reactions, where the surface-to-volume ratio is tremendous. Size effects, defects, and stain effects can all play a role – or become dominant effects – in these nanoscale reactions. On the other hand, a well-controlled kinetic process is a prerequisite for realizing tunable channel lengths and ultimately ultrashort channel devices.

Ni is the dominant diffusion species in this silicide reaction, and there are generally two diffusion paths: through the entire NW cross section (volume diffusion) or through the few atomic layers at the surface of the NW (surface diffusion). Appenzeller et al. [78] were the first to discuss the kinetics of the NiSi NW reaction and to deduce the Ni diffusion path during the silicide formation process. They found a strong size effect on the silicide growth rate and plotted the silicide length (L_{silicide}) versus R^{-1} and R^{-2}. Based on their experimental observation that the L_{silicide}~R^{-2} plot passed the origin point, they deduced a Ni volume diffusion dominant kinetics, with the assumption that the amount of diffused Ni (measured by the volume of reacted Ni silicide segment $L_{\text{silicide}} \cdot \pi R^2$) was constant and that the silicide length should approach zero for infinitely large NW ($R^{-2} \approx 0$) under a short reaction time. Later, Katsman et al. [79] argued that the extracted volume diffusion coefficient was much higher than realistic at the low reaction temperature of 280 °C. They replotted Appenzeller's data with L_{silicide}~$R^{-1/2}$ coordination following their own surface diffusion model and fitted the plot with linear approximation. This fitted line didn't pass through zero either, while they extrapolated this intercept as a transition diameter R_0 above which the interfacial diffusion (at silicide/Si interface) started to play a role.

Besides the Ni diffusion paths, there are also other limiting steps for the reaction kinetics. Lu et al. [38] studied the nickel silicide reaction in [111]-oriented Si NWs by point contact with Ni NWs. The silicide phase found in this study was nickel-mono-silicide, NiSi, which exhibited a linear dependence of L_{silicide} with time, t, instead of the conventional $L_{\text{silicide}} \propto t^{1/2}$ dependence for a diffusion-dominant process. The authors ruled out the phase growth on the silicide/Si interface as the rate-limiting step, as their observed epitaxial growth rate was much faster than the diffusion speed. Therefore, they concluded that this point contact reaction was limited by the rate Ni dissolution into Si NW at the contact interface. Dellas et al. [80] investigated the silicide reaction at higher temperatures (400 ~ 500 °C) and found a NW orientation-dependent reaction kinetics. They attribute this effect to the differences in dominant phase formed in different NW growth directions, and [111]-oriented (or [112]-oriented) NW had a linear $L_{\text{silicide}} \propto t$(or hyperbolic $L_{\text{silicide}} \propto t^{1/2}$) kinetics due to the formed $NiSi_2$ phase (or θ-Ni_2Si phase). Chen et al. [28] extended the discussions on kinetics of different silicide phases and demonstrated the first phase selection by kinetic competition for small NWs at a high reaction temperature (800 °C) as discussed in Sect. 5.2.1.

All these debated aspects for the metal-semiconductor compound contact formation starve for a standard model that can quickly determine the rate-limiting steps

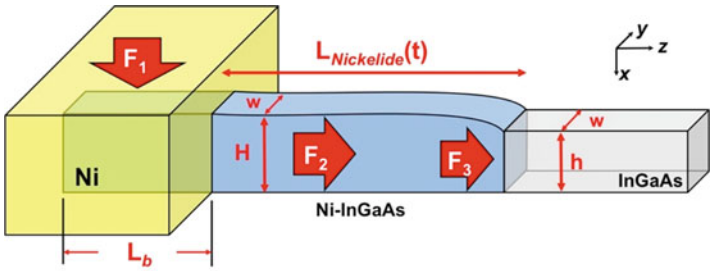

Fig. 5.8 A schematic illustration of the rate-limiting processes involved in nickelide formation in InGaAs NW channel. Due to volume expansion, the height of InGaAs NW increases from h to H after nickelide formation and the width increases from w to W. (Reprinted with permission from Ref. [67]. Copyright 2015 American Chemical Society)

and guide the extrapolation of relevant parameters. In this section, we propose a mono-compound phase model that depicts the kinetic steps involved in the metal-semiconductor reactions and provide a case study of nickelide reaction in InGaAs NWs. To the first order, stoichiometry does not influence the kinetics and is ignored here for simplicity. Then we will introduce the atomic-scale dynamics of the compound phase formation by utilizing in situ TEM technique and conclude with some specific cases when the kinetics may be altered.

5.3.1 Kinetics Modeling: A Case Study of Ni-InGaAs Reaction

This kinetic model extends previous modeling [17, 35, 81] of Ni silicide reaction in Si NWs that have cylindrical shape and focuses on more general cases in top-down etched and horizontally lying NWs that have rectangular cross sections. These top-down processed NWs (or Fin structures) present an ideal platform for studying compound metal contact formation with nanoscale channels at precisely defined widths and crystallographic orientations, in contrast to lesser control over such parameters in devices made on VLS-grown NWs that have been subject to similar studies. At the same time, we account for the volume expansion in the reacted segments, allowing for more accurate interpretation of experimental data.

As shown in Fig. 5.8, the mass transport of Ni atoms during the Ni-InGaAs compound (nickelide) growth involves three steps: (i) Ni dissolution across the Ni/nickelide interface, (ii) Ni diffusion along the formed nickelide segment, and

(iii) Ni-InGaAs reaction at the nickelide/InGaAs interface. The fluxes of Ni atoms in the above three processes can be expressed as:

$$F_1 = k_{\text{dissolve}}\left(C^{\text{eq}}_{\text{Ni/Nickelide}} - C_0\right)\cdot(W+2H)\cdot L_b \tag{5.2}$$

$$F_2 = -D_{\text{Ni}}\frac{C_L - C_0}{L_{\text{Nickelide}}}\cdot X \qquad X = \begin{cases} H\cdot W & \text{Volume Diffusion} \\ 2(H+W)\cdot\delta & \text{Surface Diffusion} \end{cases} \tag{5.3}$$

$$F_3 = k_{\text{growth}}\left(C_L - C^{\text{eq}}_{\text{Nickelide/InGaAs}}\right)\cdot hw \tag{5.4}$$

where k_{dissolve} and k_{growth} are the interfacial reaction rate constants for Ni dissolution into nickelide and for nickelide growth at the reaction front with InGaAs, respectively. At these two interfaces, $C^{\text{eq}}_{\text{Ni/Nickelide}}$ and $C^{\text{eq}}_{\text{Nickelide/InGaAs}}$ denote the equilibrium Ni concentrations. C_0 and C_L are the equilibrium Ni concentrations inside the formed nickelide segment, at zero-length position and at a reacted-length position, $L_{\text{Nickelide}}(t)$. The flux of Ni atoms diffusing along the formed nickelide segment, F_2, depends not only on the diffusion coefficient of Ni species but also on the diffusion cross section X. The diffusion cross section describes the diffusion path of Ni atoms, with $H \cdot W$ for volume (bulk-like) diffusion and $2(H + W) \cdot \delta$ for surface diffusion, where δ is the thickness of high-diffusivity surface layer, taken conventionally to be one atomic layer high.

In steady-state, the fluxes of Ni atoms in the above three processes will reach the same value, $F_1 = F_2 = F_3 = F$, and F can then be derived as:

$$F = \frac{C^{\text{eq}}_{\text{Ni/Nickelide}} - C^{\text{eq}}_{\text{Nickelide/InGaAs}}}{\frac{1}{k_{\text{dissolve}}\cdot(W+2H)\cdot L_b} + \frac{L_{\text{Nickelide}}(t)}{D_{\text{Ni}}\cdot X} + \frac{1}{k_{\text{growth}}\cdot hw}} \tag{5.5}$$

Here, we can find three terms in the denominator, each representing a rate-limiting mechanism. In order to solve this equation, the mass conservation of Ni atoms should be considered as follows:

$$HW\cdot\frac{dL_{\text{Nickelide}}(t)}{dt} = F\cdot\frac{M_{\text{Nickelide}}}{N_A\cdot\rho_{\text{Nickelide}}} \tag{5.6}$$

If we assume a constant, P, such that $P = M_{\text{Nickelide}}\cdot\left(C^{\text{eq}}_{\text{Ni/Nickelide}} - C^{\text{eq}}_{\text{Nickelide/InGaAs}}\right)/(N_A\cdot\rho_{\text{Nickelide}})$, and if we then substitute Eq. (5.6) into (5.5), we will get:

$$\frac{dL_{\text{Nickelide}}(t)}{dt} = \frac{P}{\frac{HW}{k_{\text{dissolve}}\cdot(W+2H)\cdot L_b} + \frac{HW\cdot L_{\text{Nickelide}}(t)}{D_{\text{Ni}}\cdot X} + \frac{HW}{k_{\text{growth}}\cdot hw}} \tag{5.7}$$

To solve this differential equation and to separate the three rate-limiting mechanisms, the terms in the denominator are considered one at a time.

If Ni supply is the rate-limiting step, then:

$$L_{\text{Nickelide}}(t) = k_{\text{dissolve}}\left(\frac{1}{H}+\frac{2}{W}\right)L_b P \cdot t \tag{5.8}$$

If Ni diffusion is the rate-limiting step, and Ni follows surface diffusion path, then:

$$L_{\text{Nickelide}}(t) = \sqrt{4PD_{Ni}\delta \cdot \left(\frac{1}{H}+\frac{1}{W}\right) \cdot t} \tag{5.9}$$

If Ni diffusion is the rate-limiting step, and Ni follows volume diffusion path, then:

$$L_{\text{Nickelide}}(t) = \sqrt{2PD_{Ni} \cdot t} \tag{5.10}$$

If interfacial reaction is the rate-limiting step, then:

$$L_{\text{Nickelide}}(t) = k_{\text{growth}}\frac{hw}{HW}P \cdot t \tag{5.11}$$

The conditions and properties of each rate-limiting step are summarized in Table 5.4. It can be clearly seen that for a diffusion-limited process, including surface diffusion and volume diffusion paths, the nickelide segment lengths have a hyperbolic dependence on time. However, for an interface-related limited process, including Ni dissolution at Ni/nickelide interface and nickelide growth at nickelide/InGaAs interface, the nickelide segment lengths have a linear dependence on time. Among these four rate-limiting steps, the Ni source supply limit and the surface diffusion limit exhibit size dependence on NW dimensions. Even though Eq. (5.11) also involves geometric terms, the solution mainly relies on the expansion ratio in the cross-sectional area, indicating a dependence on the formed nickelide phase.

Table 5.4 Nickelide growth in InGaAs NWs for different rate-limiting steps according to Eqs. (5.8, 5.9, 5.10 and 5.11)

		Size dependence		Time dependence	
Rate-limiting step	Conditions	Yes	No	Linear (t)	Hyperbolic ($t^{1/2}$)
Ni source supply limit	$k_{\text{dissolve}} \ll k_{\text{growth}}, D_{\text{Ni}}$	✓		✓	
Surface diffusion limit	$D_{\text{Ni}} \ll k_{\text{dissolve}}, k_{\text{growth}}$	✓			✓
Volume diffusion limit	$D_{\text{Ni}} \ll k_{\text{dissolve}}, k_{\text{growth}}$		✓		✓
Interfacial reaction limit	$k_{\text{growth}} \ll k_{\text{dissolve}}, D_{\text{Ni}}$		✓	✓	

Please note that this kinetic model considers a single-phase metallic compound formation during the metal-semiconductor reaction, and more complicated modeling with multiple-phase formations can be found elsewhere [82, 83].

From the experimental results of nickelide reaction in InGaAs NWs with different widths, clear size-dependent nickelide segment lengths are observed as shown in Fig. 5.9a, b. Ni diffuses into the InGaAs NW channels from both ends with the nickelide segment exhibiting a lighter contrast, and smaller NW channels have longer nickelide segment for the same annealing time. This indicates that either the Ni source supply limit or the surface diffusion limit is the rate-limiting step here in the nickelide formation in these top-down etched InGaAs NWs. The interface between nickelide and InGaAs is rougher in the <100>-oriented NWs, due to the crystalline correlation at interface as discussed in Sect. 5.2.3. The $L_{\text{Nickelide}} \sim t$ plots in Fig. 5.9c, d show hyperbolic curves with good $t^{1/2}$ fitting, suggesting a surface diffusion-limited process. Therefore, Eq. (5.9) is used to describe this kinetic process, and the data is replotted as $L_{\text{Nickelide}} \sim \sqrt{1/H + 1/W}$ in Fig. 5.9e, f. As the volume expansion is found to mainly cause the height change in these experiments and negligible width change is observed, the w is used here to replace W. For both orientations, linear fits with two slopes agree well with data measured for each annealing time. The different slopes become more eminent as the annealing time is larger than 25 min. The "corner" points (deflection points in linear fits) correspond to NW widths of ~ 100 nm for <110>-oriented NWs and ~ 150 nm for <100>-oriented NWs.

These deflection points indicate certain changes are happening with the increase in NW size. The insets in Fig. 5.9c, d also show an incubation time before measurable nickelide lengths for NW channels were detected, and the incubation time increases as the NW width becomes larger. However, there's no incubation time for the planar films, indicating different kinetic processes between thin film structures and NW channels. Indeed, metal diffusion in thin films is always considered as volume diffusion, while we have demonstrated the surface diffusion dominant behaviors in NW reactions. The incubation time is likely associated with Ni diffusion through the body of the InGaAs NW underneath the Ni pads, where the larger NWs require longer time for Ni to fill the entire NW cross section. At the same time, larger NWs have much smaller surface-to-volume ratio, which may be attributed to some contribution from volume diffusion instead of pure surface diffusion, causing the deflections in the linear fittings in Fig. 5.9e, f.

To further clarify this, the length of nickelide segment is plotted against both the time and geometry factors in Fig. 5.10a, b. Accounting for both geometric and time dependencies, all experimentally measured data for different annealing times and at a single temperature can be linearly fitted (in agreement with Eq. 5.9) validating the surface diffusion dominant kinetic process. The non-zero intercept with the x-axis indicates an average incubation behavior of all NWs with 250 °C thermal treatment, but no average incubation time for higher temperature treatments. However, larger

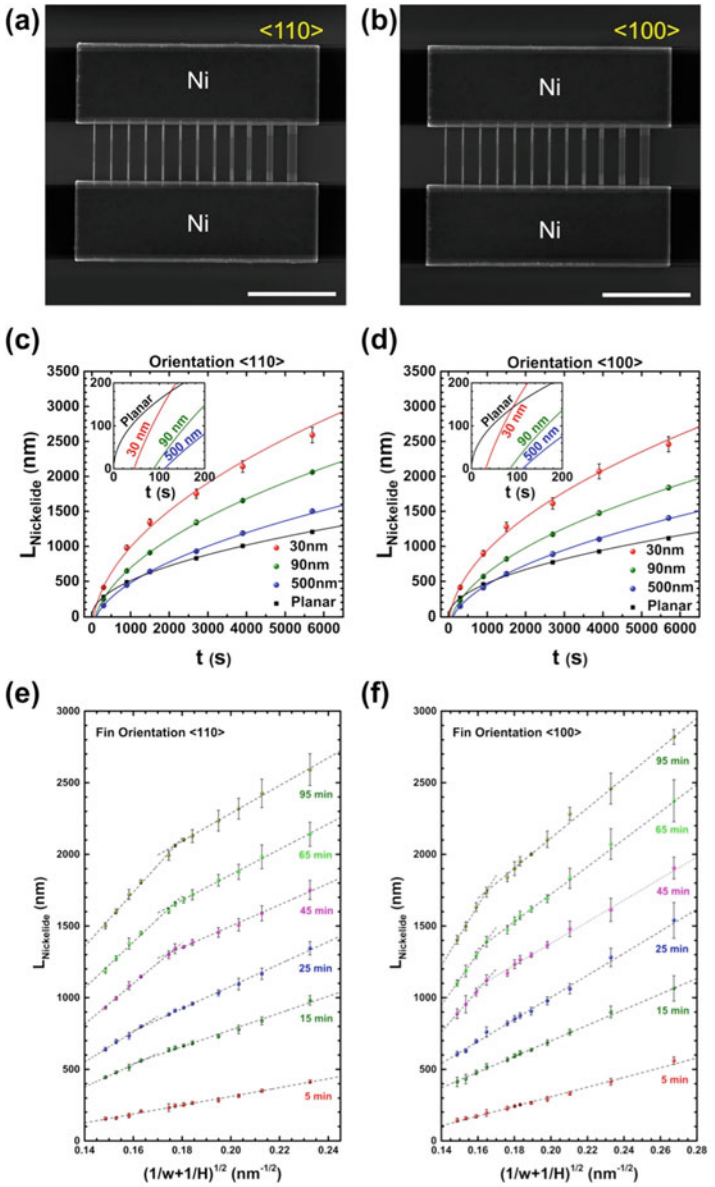

Fig. 5.9 Size, orientation, and time dependence of nickelide formation. (**a** and **b**) SEM images illustrating the size-dependent and orientation-dependent morphologies for nickelide contacts with InGaAs fin channels pre-defined in <110> and < 100> orientations, respectively. Scale bars are 5 μm. (**c** and **d**) The length of nickelide segments versus annealing time at 250 °C for <110> and < 100> fin orientations, respectively. In both orientations, the data were well fitted with a $t^{1/2}$ dependency. (**e** and **f**) The length of nickelide segments versus $\sqrt{1/w + 1/H}$ at 250 °C with two different fin orientations, <110> and < 100>, respectively. (Reproduced with permission from Ref. [67]. Copyright 2015 American Chemical Society)

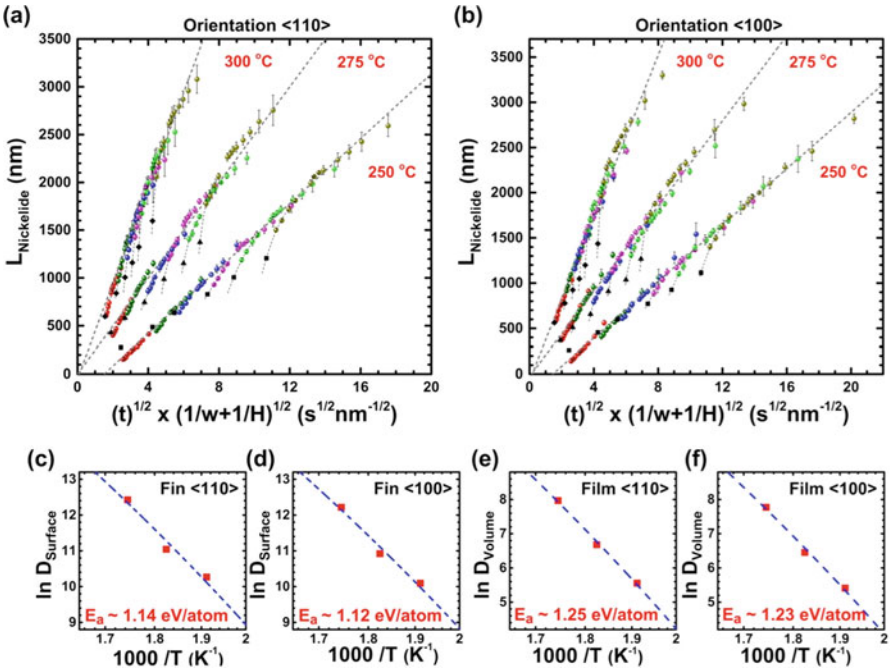

Fig. 5.10 (**a** and **b**) Combined plots of nickelide segment length in relation to annealing time and NW geometrical factors, according to the surface diffusion-limited model, at three different growth temperatures and with NW orientations of <110> and < 100>, respectively. (**c**–**f**) Extracted kinetic parameters for NW channels and planar films in both <110> and < 100> orientations. (Reproduced with permission from Ref. [67]. Copyright 2015 American Chemical Society)

NWs (left-side data points of each data set, color-labeled) fell below the linear trend, indicating a deviation from the surface diffusion-limited kinetic model. Interestingly, these deflected data points gradually extend approaching the black squares, which are the data points obtained from nickelide growth in InGaAs thin films. All those observations suggest that the behaviors of nickelide formation in larger NWs gradually deviate from surface-dominant to a volume-dominant diffusion-limited growth process. Then, the diffusion coefficients can be extracted and plotted according to the Arrhenius relationship, $D \propto e^{-E_a/kT}$, followed by the extrapolation of activation energies of nickelide formation in both NW channels and film structures.

The above analysis provides a general way of investigating the kinetic processes during the metal-semiconductor reactions, and NWs with cylindrical shape can be derived similarly by replacing the geometry factors with those related to the NW diameter, R [17].

5.3.2 Atomic-Scale Dynamics

The dynamic process during metal-semiconductor reaction is reflected by the ledge nucleation and movement at atomic scale. Generally, a ledge or a train of ledges form on the compound contact/semiconductor interface and propagate through the entire cross section of NWs. In situ heating TEM technique provides the platform to observe these ledge (or called step) events with atomic resolutions [84].

In the study of $CoSi_2$ formation in Si NWs, Chou et al. [73] prepared the [111]-oriented Si NWs with point contact of Co NWs and annealed the sample inside TEM chamber at 800 °C with real-time video recordings. They observed repeating events of the nucleation and stepwise growth mode during the epitaxial $CoSi_2$ phase formation, which has the same crystal structure and close lattice constant with pristine Si as seen in Table 5.3. Shown in Fig. 5.11a–d are the HRTEM images near Si/$CoSi_2$ interface, with the step movements labeled on the figures. By recording these repeating nucleation and growth events, they plotted the $CoSi_2$ atomic layers as a function of time in Fig. 5.11e, and several information can be interpreted from this plot. First, the vertical lines in this plot represent the steps of newly formed $CoSi_2$, and the height of each vertical transition is constantly that of one atomic layer of $CoSi_2$ (111) plane, indicating the layer-by-layer growth nature of $CoSi_2$ phase. Second, these vertical lines are not perfectly in parallel with y-axis but are sloped with a certain width that corresponds to the growth time of each $CoSi_2$ atomic layer with the average value of ~0.17 s. Third, the horizontal segment in between vertical lines is the stagnation period before the nucleation of another step, which is called incubation time of nucleating a step. Taking into account the incubation time for nucleating every step, the average growth rate of $CoSi_2$ along the axial direction is 0.0365 nm/s. The radial growth rate (step velocity) is about 135 nm/s, calculated by the average step growth time and NW diameter, which is about 3700 times faster than the axial growth rate. This also indicates that interfacial reaction was not the rate-limiting step in this cobalt silicide growth. Fourth, the stair-step plot in Fig. 5.11e can be treated as the microcosmic view of a conventional $L_{\text{silicide}} \sim t$ relationship (discussed in Sect. 5.3.1), in which a linear dependence was found over a long reaction time. The authors attribute this linear time dependence to a Co source supply limited reaction, which agrees with our judgment in Table 5.4. Moreover, each step of $CoSi_2$ showed a homogeneous nucleation behavior in the center of Si NW atop the $CoSi_2$/Si interface instead of the heterogeneous nucleation at the triple point of oxide shell, Si, and $CoSi_2$. Though homogeneous nucleation was seldom expected in theory, the authors explained the nucleation behavior here that the energy of oxide/silicide interface is higher than that of oxide/Si interface reducing the nucleation frequency at the triple points. They provided further experimental evidence [39] in Fig. 5.12a, b that the steps slowed down as approaching the oxide/Si/$CoSi_2$ triple points due to the high energy barrier. Their in situ TEM study of Ni point-contacted Si NW showed similar homogeneous nucleation of steps, as shown in Fig. 5.12c, d.

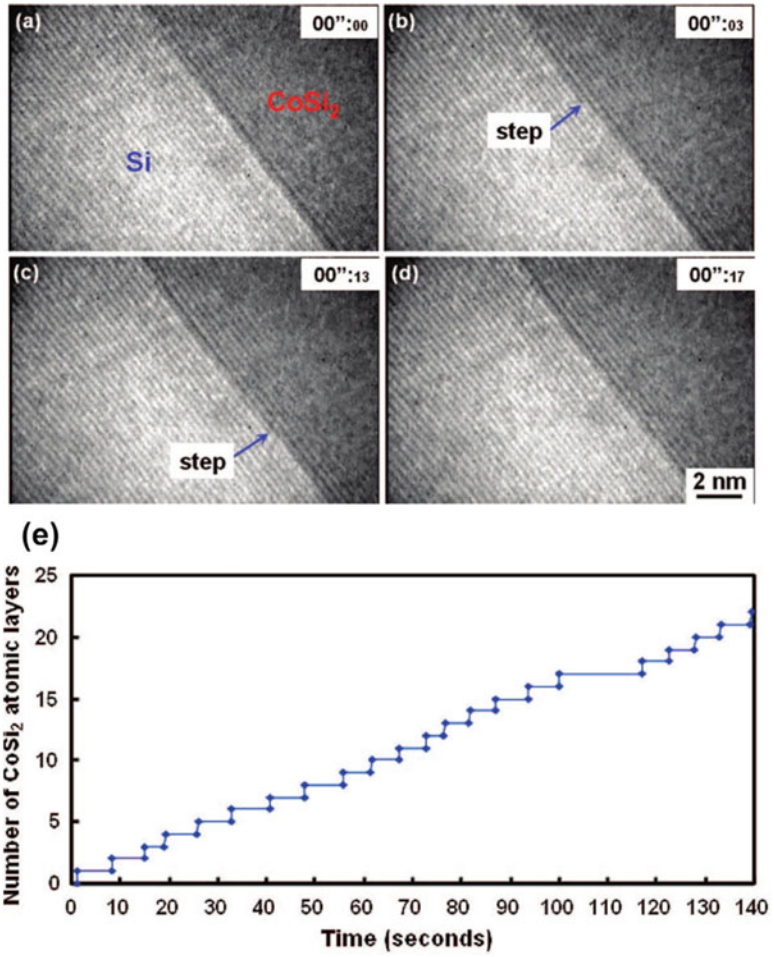

Fig. 5.11 (**a**–**d**) In situ HRTEM image sequences of growing $CoSi_2$/Si epitaxial interfaces within a [111]-oriented Si NW. (**e**) Plot of $CoSi_2$ atomic layers as a function of time to show the nucleation time and growth time of each step. (Reproduced with permission from Ref. [73]. Copyright 2008 American Chemical Society)

5.3.3 Modified Kinetic Process

Through the discussions above on kinetics of the solid-state reactions between metal and pristine semiconductor NWs, we mentioned several factors that potentially dominated the rate-limiting steps, such as NW sizes, surface oxide, reaction temperature, and formed phases. A table (Table 5.5) can be found at the end of this section that summarizes the reaction kinetics and extrapolated rate constants in metal-semiconductor compound formation in NW channels. In the following paragraphs,

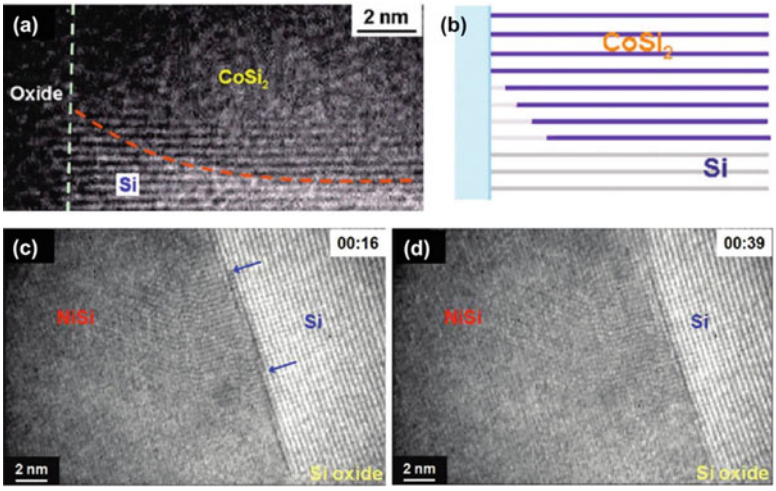

Fig. 5.12 (**a** and **b**) HRTEM image and schematics of the $CoSi_2$/Si epitaxial interfaces at the oxide/Si/$CoSi_2$ triple point. (**c** and **d**) In situ HRTEM image sequences of growing NiSi/Si epitaxial interfaces within a [111]-oriented Si NW. (Reproduced with permission from Ref. [39]. Copyright 2009 American Chemical Society)

we will discuss another important factor that may modify the nucleation and growth behaviors of compound contact in NW channels: defects.

In advanced semiconductor technology nodes, defects are intentionally built into the device to tailor the stress in Si channel. The stress memorization technology [85] is one example that utilizes stacking faults to exert tensile strain in the channel by inducing missing planes in the source/drain regions. In other instances, defects can be unintentionally introduced to the S/D regions during dopant implantation and subsequent activation thermal anneal [86]. Therefore, understanding the interactions between metal-semiconductor reactions and defects becomes important in controlling compound contact formation in defect-engineered nanochannels.

We previously investigated the nickelide silicide nucleation and growth in the presence of defects in Si NWs [87]. The Si NWs are grown at different conditions [88], to intentionally introduce two types of defects: (1) twin boundary (TB) along the axial direction of the NW with a high growth pressure and (2) Si nanoparticles on the NW surface forming the grain boundary (GB) with high growth temperature. It has been found that the $NiSi_2$ prefers the heterogeneous nucleation at the defect sites in order annihilate the high-energy interfaces.

As shown in Fig. 5.13, the $NiSi_2$ phase grows on the Si (111) plane in a layer-by-layer manner, and the growth fronts move asynchronously at two sides of the TB. The steps nucleate at the TB but never propagate across it, because the high energy barrier of forming new $NiSi_2$/$NiSi_2$ TB prevents so. The lagging interface can catch up with the leading interface because the $NiSi_2$/Si corner at TB is a preferable hetero-nucleation site, so on the average asynchronous step height does not grow

Table 5.5 Summary of reaction kinetics when metal and semiconductor NW form compound contacts

Nanowire	Phase	Temperature range	Activation energy (eV/atom)	Rate-limiting step	Rate constant	Refs.
Si [111]	$NiSi_2$	400~550 °C	0.76 ± 0.10	Interfacial reaction	–	[80]
Si [112]	θ-Ni_2Si		1.45 ± 0.07	Surface diffusion		
(50~75 nm)						
Si in SiO_2 shell	$NiSi_2$	300~440 °C	–	Surface diffusion	Without shell	[35]
					D~3.6e^{-12} cm^2/s	
					With shell	
(10~100 nm)					D~9.6e^{-13} cm^2/s	
Si	Ni_xSi	300~440 °C	1.7 ± 0.15	Source supply (I) → diffusion (II)	–	[81]
(25~50 nm)						
Si [111]	$NiSi_2$	300~800 °C	1.79 ± 0.10 (I)	Interfacial reaction (I) → diffusion (II)	k = 1.2e^{-5} cm^2/s (I)	[28]
(20~234 nm)	□-Ni_2Si	800 °C	1.64 ± 0.24 (II)	Diffusion	D = 2.3e^{-10} cm^2/s (II)	
			–		D = 3.65e^{-10} cm^2/s	
Ge [111]	Ni_2Ge	400~500 °C	0.55 ± 0.05	Linear t dependence	–	[18]
InAs [110]	Ni_3InAs	220~280 °C	~ 1.04	Volume diffusion (size independent)	D = 1.13e^{-10} cm^2/s (280 °C)	[55]
(20~40 nm)						
$In_{0.53}Ga_{0.47}As$	$Ni_2In_{0.53}Ga_{0.47}As$	250~300 °C	~1.14 (surf, [110])	surface (small r) → volume (large r) diffusion	D_{110} = 1.33e^{-10} cm^2/s	[67]
[110] and [100]			~1.12 (surf, [100])		D_{100} = 1.08e^{-10} cm^2/s	
(30~500 nm)			~1.25 (vol, [110])		(30 nm, 300 °C)	
			~1.23 (vol, [100])			
GaAs [111]	Au_xGaAs	264~354 °C	0.66~1.60	linear t dependence	–	[89]
(<100 nm)	(no-epi)		(different interface orientation)			

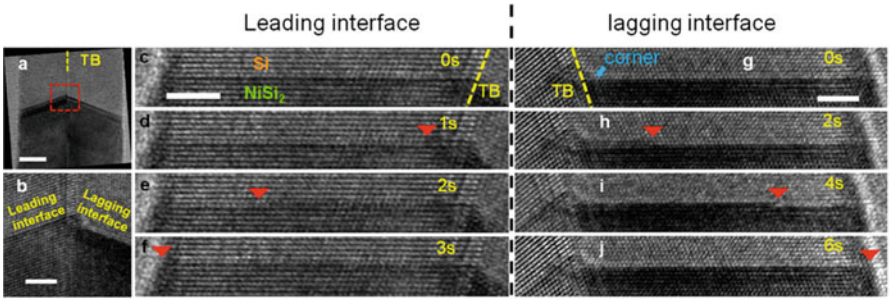

Fig. 5.13 (**a** and **b**) $NiSi_2$ growth in Si NW with a TB. (**c**–**f**) and (**g**–**j**) HRTEM sequences showing the nucleation and propagation of $NiSi_2$ steps at the leading interface and at the lagging interface, respectively. Scale bar is 10 nm for (**a**) and 3 nm for all the rests. (Reprinted with permission from Ref. [87]. Copyright 2013 American Chemical Society)

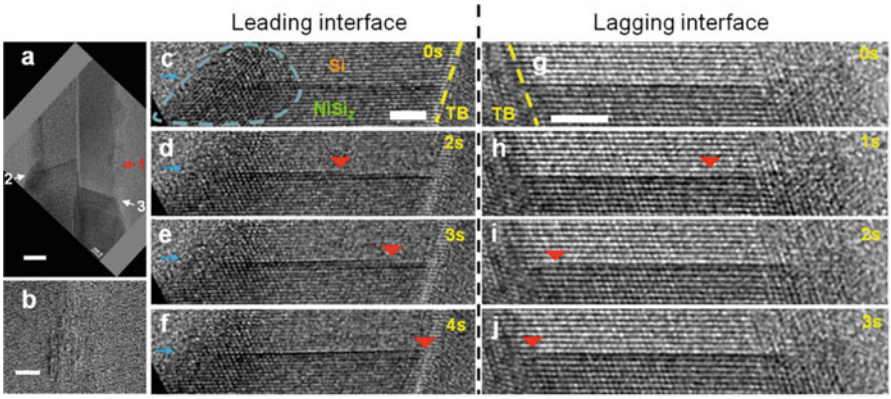

Fig. 5.14 (**a**) $NiSi_2$ growth in Si NW with TB running along its central axis and GBs present at its surface. (**b**) Zoom-in HRTEM image of a cluster of surface grains. (**c**–**f**) and (**g**–**j**) HRTEM sequences showing the nucleation and propagation of $NiSi_2$ steps at the leading interface and at the lagging interface, respectively. Scale bar is 10 nm for (**a**) and 3 nm for all the rests. (Reprinted with permission from Ref. [87]. Copyright 2013 American Chemical Society)

significantly, given that Ni supply is equally available for both halves of the bi-crystal. With the presence of GBs on the NW surface as shown in Fig. 5.14, the heterogeneous nucleation is further facilitated and the steps are found to start from the GB and propagate toward the TB, in both leading and lagging interfaces, indicating that the GB is the more energetically preferred nucleation site.

These observations are related to the effectiveness of nucleation barrier reductions in $NiSi_2$ phase formation, and this reduction can be evaluated at the three

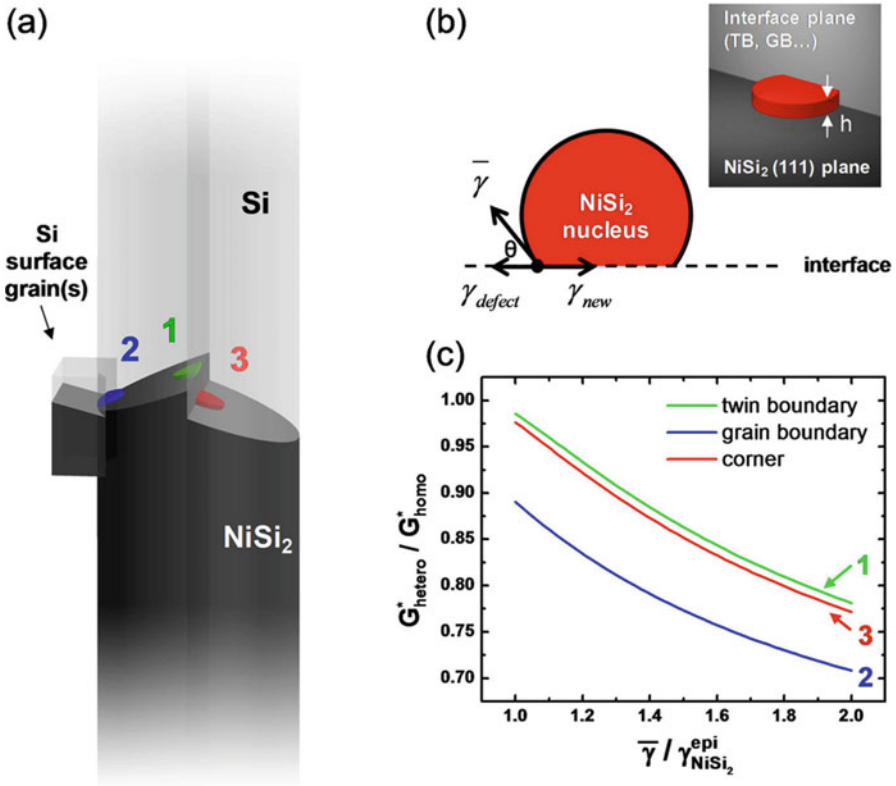

Fig. 5.15 (**a**) Schematic of three different heterogeneous nucleation sites. (**b**) Zoom-in view of the heterogeneous nucleus with disk shape and the correlation between different surface energies and contact angle θ. (**c**) Reduction in the nucleation barrier at different heterogeneous sites. (Reprinted with permission from Ref. [87]. Copyright 2013 American Chemical Society)

possible heterogeneous nucleation sites (illustrated in Fig. 5.15a): (1) TB, (2) "corner," and (3) surface GB, by calculating [87]:

$$\frac{\Delta G^*_{\text{hetero}}}{\Delta G^*_{\text{homo}}} = \frac{(\pi - \theta) + \sin\theta\cos\theta}{\pi} \tag{5.12}$$

where $\Delta G^*_{\text{hetero}}$ and ΔG^*_{homo} are the heterogeneous and homogeneous nucleation barriers, respectively. The contact angle θ is given by Young's equation, $\overline{\gamma}\cos\theta + \gamma_{\text{defect}} = \gamma_{\text{new}}$, in which $\overline{\gamma}$, γ_{defect}, and γ_{new} are the different interfacial energies as shown together with θ in Fig. 5.15b. In the three different nucleation sites, the energies for original defect γ_{defect} and new interface γ_{new} have different values, which are summarized in reference [87]. Using these values, the nucleation barrier reductions can be plotted in Fig. 5.15c, as a function of $\overline{\gamma}$. Therefore, with a reasonable estimation of $\overline{\gamma} = 1.2\gamma^{\text{epi}}_{\text{NiSi}_2}$, the values of $\Delta G^*_{\text{hetero}}/\Delta G^*_{\text{homo}}$ can be

calculated for TB, "corner," and GB as 0.93, 0.90, and 0.83, respectively. This indeed proves that the nucleation is more preferred on GB than "corner" and than TB sites.

5.4 Electrical Properties

Thus far, we discussed the phases of the metal-semiconductor compound contacts and the kinetics during the solid-state reaction processes, but the end goal of these metallurgical studies is to achieve a robust control over the electrical properties of the compound contacts and the resulting NW FET performances. It has been found that the S/D series resistance increasingly becomes the limiting factor for integrating nanostructures into high-performance electronics and the dominant performance degradation component below 10 nm node [90]. Therefore, understanding the electrical properties of the nanoscale electrical contacts, especially compound contacts, is a key step for fulfilling the leap from laboratory to real-world technology [91].

Here we will start by introducing the various applications of most commonly used compound contacts and continue with contact theories to NW channels and reports on the ultrashort channel devices. We summarize the property of compound contacts and the performance of NW FET devices discussed in this section in Table 5.6.

5.4.1 Electrical Applications of Compound Contacts

Nickel silicide and nickel germanide are most commonly used contacts in conventional CMOS technologies and extend their wide applications to NW FET studies. NiSi has low annealing temperature, low resistivity, and superior scaling to linewidths <100 nm [22]. Planar-geometry NiSi-based contact demonstrated a specific contact resistance of $<10^{-8}$ Ωcm^2 [24]. Its low density, smoother interfaces with Si, and less Si assumption add up to a superior contact to ultrathin Si-on-insulator device layer [23]. The planar-geometry NiSi has a Schottky barrier height (SBH) of 0.75 eV to n-Si and 0.39 eV for p-Si at room temperature [14], and the silicide work functions can be further adjusted by varying the doping concentrations in Si before silicide formation [92]. In Si NWs, $NiSi_2$ is the most commonly observed first phase interfacing with pristine Si.[13,15,16] There are usually two types of coherent $NiSi_2$/Si interfaces: type A interface, where $NiSi_2$ has the same orientation with Si, and type B interface, where $NiSi_2$ forms a twin boundary-like interface. It has been found that type A $NiSi_2$/Si interface has an electron SBH (0.64 eV) that is 0.14 eV smaller than that of a type B interface (0.78 eV) [93].

Nickelide compound was also demonstrated to be a superior contact to planar III–V channels, such as $In_xGa_{1-x}As$ (referred in short as InGaAs). First, this Ni-InGaAs compound forms at a low annealing temperature, meeting a good thermal processing

Table 5.6 Summary of the property of compound contacts and the performance of NW FET devices

Phase	T(°C)	Compound contact			Channel			Compound/semiconductor/compound device						Refs.
		ρ (μΩ-cm)	J_{max} (A/cm^2)	SBH (eV)	d (nm)	L (μm)	Gate dielectric	R_C (Ω-cm^2)	$-V_{ds}$ (V)	SS^{-1} (mV/dec)	g_m (μS)	Mobility (cm^2/V/s)	I_{max}/I_{min}	
NiSi	550	10	>10^8	–	30	3	Back: 600 nm SiO_2	–	1	–	0.275	325 (h)	–	[11]
Ni_xSi	470	–	–	–	20	0.67	Back: 300 nm SiO_2	~10^{-6}	1	–	–	– (i)	10^7	[117]
$NiSi_2$	400	–	–	–	32	0.017	Top: 10 nm HfO_2	–	0.01	350	~15	–	~10^3	[26]
NiSi	500 (poly-Si NW)	13 ± 2	1.6 × 10^8	–	–	–	–	–	–	–	–	–	–	[118]
Ni_2Si		25 ± 1	1.2 × 10^8											
$Ni_{31}Si_{12}$		60 ± 2	8 × 10^7											
Ni_2Si	850 (CVT)	21	>10^8	–	–	–	–	–	–	–	–	–	–	[70]
PtSi	520	28.6	>10^8	~0.2	50	2.3	Top: 7 nm HfO_2	–	0.2~1	110~220 (h)	~12	168 (h)	>10^7	[72]
										320(e)				
$ErSi_{2-x}$	450	–	–	~0.3 (n)	8	0.5	BOX	–	1.2	~180	–	–	10^5	[101]
Ni_2Ge	400	88	3.5 × 10^7	~0.2	40	3	Back: 330 nm SiO_2	–	0.1	–	0.013	65.4 (h)	>10^3	[47]
NiGe	450	–	–	0.11	70	0.67	Back: 330 nm SiO_2	–	0.1	2330	0.168	210 (h)	10^5	[75]
							(Al_2O_3 passivation)							
$NiSi_xGe_y$	300	–	–	–	18	0.19	Top: 4 nm HfO_2	–	0.01	100	3	730 (h)	>10^5	[119]

$NiSi_xGe_y$	300	–	–	–	18	0.07	Top: 4 nm HfO_2	–	0.5	~200	78	136 (h)	10^5	[120]
						0.04				~290	91	91 (h)		
Ni_2Ge	300	–	–	–	30	0.4	Top: 10 nm HfO_2	$\sim 10^{-8}$	0.1	260	1.1	50 (h)	10^5	[114]
Ni_2Ge/ $NiSi_y$					20	0.3				140	4	200 (h)	10^6	
Cu_3Ge	310	34	5×10^7	0.218	20~30	0.7	Back: 200 nm SiO_2	–	0.2	–	–	264 (h)	$>10^3$	[76]
Cu_3Ge	250	–	–	0.115	35	0.25	Top: 20 nm SiO_2	–	0.2	830	–	142 (h)	$>10^3$	[121]
				(Ga +)										
Mn_5Ge_3	450	240	–	0.25	50	0.5	Back: 300 nm SiO_2	–	0.1	–	0.25	>170 (h)	10^5	[77]
							(Al_2O_3 passivation)							
Ni_3InAs	250	167	10^8	<0 (*n*)	~30	0.28	Buried: 60 nm LTO	–	0.5	–	–	–	10^5	[55]

ρ here is the resistivity of pure compound phase as NW shape. SBH is the hole Schottky barrier height except for $ErSi_{2-x}$ and III-V NWs. SS^{-1} is the inverse subthreshold slope

budget. It has been reported that nickelide starts to form at around 230 °C, and the formed phase is thermally stable between 350 °C and 450 °C [94]. Unlike the phase transition of nickel silicide at elevated temperatures, Ni-InGaAs suffers a degradation of electrical properties at 450 °C and above, resulting from the decomposition of the quaternary compound to binary compounds. Second, atomic abrupt interfaces were found in between the nickelide contact with III–V NW channels [55, 67], enabling an accurate control of the channel lengths. Third, selective etching of excessive Ni from nickelide contact with concentrated HCl facilitates the self-aligned gate process [95]. Most importantly, the Ni-InGaAs alloy has a low sheet resistance (20–25 Ω/square) [96, 97] and a low electron SBH. Ivana et al. [98] observed the alignment of nickelide contact to near conduction band of $In_{0.53}Ga_{0.47}As$ at interface by using ultraviolet photoelectron spectroscopy, which gave a hole SBH of 0.8 ± 0.1 eV and an ohmic contact to n-$In_{0.53}Ga_{0.47}As$. Mehari et al [99] obtained an electron SBH of 0.2396 ± 0.01 eV for n-$In_{0.53}Ga_{0.47}As$ through temperature-dependent current-voltage characteristics. These different values may originate from different interfacial properties between nickelide contact and InGaAs channel, which requires detailed studies on SBH of nickelide contacts in NW channels. Generally, a good ohmic contact is readily formed between nickelide contact and $In_xGa_{1-x}As$ that has high "In" content ($x > 0.7$), due to the Fermi-level pinning at the contact interface [100]. Currently, electrical studies on nickelide contacts to III–V NWs are still lacking [55].

Besides the Ni-based compound contacts, other metals have also been investigated in the solid-state reaction with semiconductors to form contacts, demonstrating a wide variety of applications. Erbium silicide, $ErSi_{2-x}$, was used to contact with n-type top-down etched Si NW, and a low electron SBH of ~0.3 eV was reported [101]. Platinum silicide, PtSi, that formed in the SiNW has a low hole SBH of ~0.2 eV, with a minimum achieved channel length of 8 nm [72]. At the same time, many compound contacts exhibit good magnetic properties, allowing the study of spin-polarized carriers in semiconductor NWs. Unusual ferromagnetic properties in single-crystalline CoSi NW were observed, significantly different from the diamagnetic properties in CoSi bulk [102]. Single crystal MnSi NW had paramagnetic to ferromagnetic transition temperature of 29.7 K, and the MnSi/p-Si/MnSi NW transistor was employed to study the carrier tunneling via the Schottky barrier and spin-polarized carrier transport in the Si NW [74]. Paramagnetic FeSi NW was transferred into Fe_3Si NW by a diffusion-driven crystal structure transformation method, with the Fe_3Si NW showing high-temperature ferromagnetic properties with $T_c \gg 370$ K [103]. In Ge NW system, there are also analogous ferromagnetic compound contacts, such as Fe_3Ge [104], Ni_3Ge [104], Mn_5Ge_3 [77, 105], etc., to investigate the electrical spin injections and detections in Ge NW transistors.

Moreover, asymmetric metal-semiconductor compound contacts can also be introduced to NW channels to expand their electrical functionalities. One approach is to form two different metal silicide at the opposite ends of the Si NW. Wu et al [106] reported the fabrication of β-Pt_2Si/Si/θ-Ni_2Si, β-Pt_2Si/θ-Ni_2Si, and β-Pt_2Si/

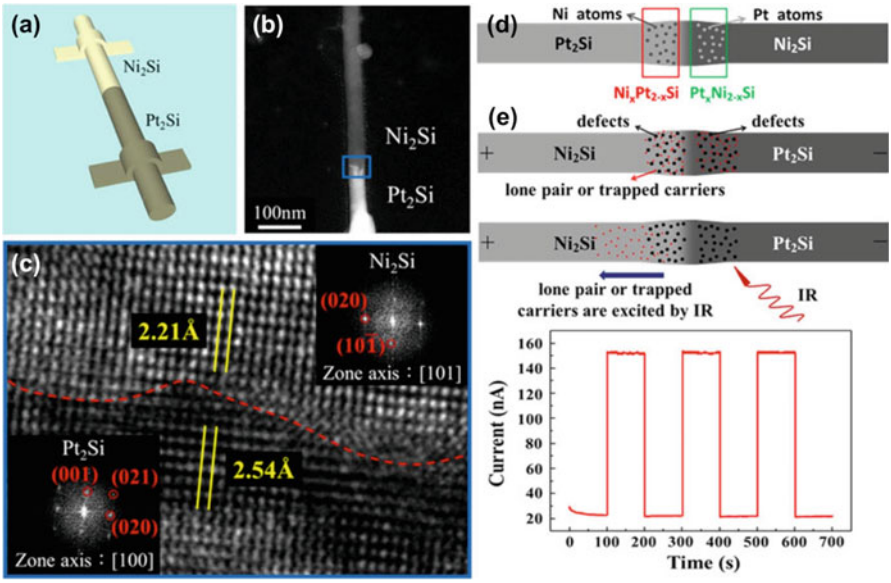

Fig. 5.16 (**a**) Schematic of nickel/platinum dual silicide formation in a Si NW. (**b**) Low magnification and (**c**) high magnification TEM images of the β-Pt_2Si/θ-Ni_2Si interface. (**d**) Schematic of the ternary compound formation at the interface with further interdiffusion. (**e**) Schematics of the infrared light-sensing mechanism and the time-dependent photoresponse with 940 nm infrared light turned on and off repeatedly. (Reprinted with permission from Ref. [106]. Copyright 2016 American Chemical Society)

$Ni_xPt_{2-x}Si/Pt_xNi_{2-x}Si$/θ-$Ni_2Si$ axial heterostructures by depositing Pt and Ni on two sides of the Si NW and consequent annealing at 650 °C for certain controlled times. Shown in Fig. 5.16a–c are the schematics of the dual silicide formation and the TEM images of the merged interface between β-Pt_2Si and θ-Ni_2Si. Further annealing led to the intermixing of binary compounds to ternary compounds at the interface, as shown in Fig. 5.16d. Though Pt_2Si/Ni_2Si NW gave the lowest resistivity of 593.3 μΩ cm, the Pt, Ni, and Si ternary NW heterostructures exhibited an excellent infrared light-sensing property, owing to the excitation of trapped carriers in the defective ternary compound region (shown in Fig. 5.16e).

In another approach, the asymmetric compound contacts can be formed in Si-Ge axial NWs with the same-metal reactions at the opposite ends. This offers a unique opportunity for exploring nanochannel devices with asymmetric contacts to assist charge transport in one desired direction and block it in the opposite direction. An example is shown in Fig. 5.17, in which Ni was used to contact the both ends of a Si-Ge axial NW [107]. In such a device, the difference in barrier heights at either end of the channel can add to the total potential drop in the channel and enhance current

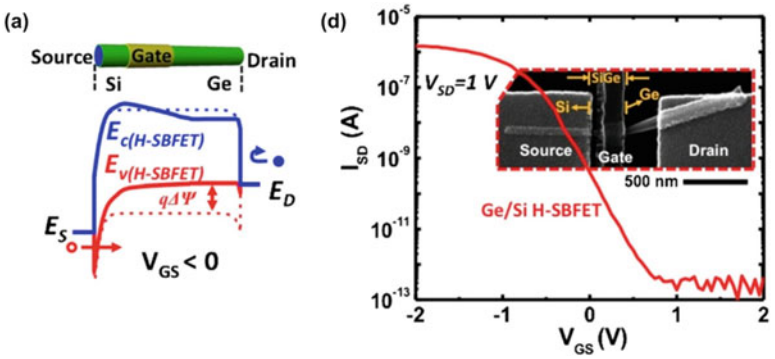

Fig. 5.17 (**a**) Schematic of the Si-Ge asymmetry SBH FET device, and the Silvaco simulated energy band-edge diagrams in on-state. Dashed lines correspond to the situation of a pure Si channel under the same bias conditions. (**b**) Transfer curve of a p^+ Ge–Si NW heterostructure SBFET showing $10^7 I_{on}/I_{off}$ ratio ($V_{SD} = 1$ V). Inset is an SEM image indicates the S/G spacing of ~40 nm, G length of ~200 nm, and G/D spacing ~260 nm. Reproduced with permission from Ref [107]. Copyright 2011 American Institute of Physics

transport in one direction. The potential drop across the valence band edge along the channel with applied S/D voltage can be expressed as:

$$\left|E_{v(S)} - E_{v(D)}\right|/q = V_{SD} + \Delta E_{v(Ge-Si)}/q + \varphi_{Bp(S)} - \varphi_{Bp(D)} \tag{5.13}$$

where V_{SD} is the applied source and drain voltage and $\Delta E_{v(Ge\ -\ Si)}$ is the average valence band offset between Si and Ge with the value ~0.57 eV. $\varphi_{Bp(S)}$ and $\varphi_{Bp(D)}$ are the hole SBH at the source and drain sides, respectively. The built-in potential drop in this asymmetry-contact transistor, $\Delta E_{v(Ge\ -\ Si)}/q + \varphi_{Bp(S)} - \varphi_{Bp(D)}$, can be as large as 0.82 V and can therefore significantly accelerate the hole transport from the Si to the Ge side. This resulted in an excellent I_{SD} modulation with on/off ratio of 10^7 exceeding NW FETs made on pure p^+ Ge or Si segments. This device architecture adds an important ability to accommodate band offsets and built-in electric fields in the conduction or valence bands utilizing asymmetry SBH at S/D of NW FETs. By proper selection of metal-semiconductor barrier heights, the functionalities can be thus be expanded for next-generation semiconductor devices.

5.4.2 Band Alignment and Charge Injection

The charge injection from metal-compound contacts into semiconductors is largely dominated by the band alignment at the contact-semiconductor interface. Due to the different contact geometries and size effects, NW transistors exhibit distinct band alignment and charge injection properties than their bulk counterparts [91]. Here, we will discuss several theoretical studies of the nanoscale contacts.

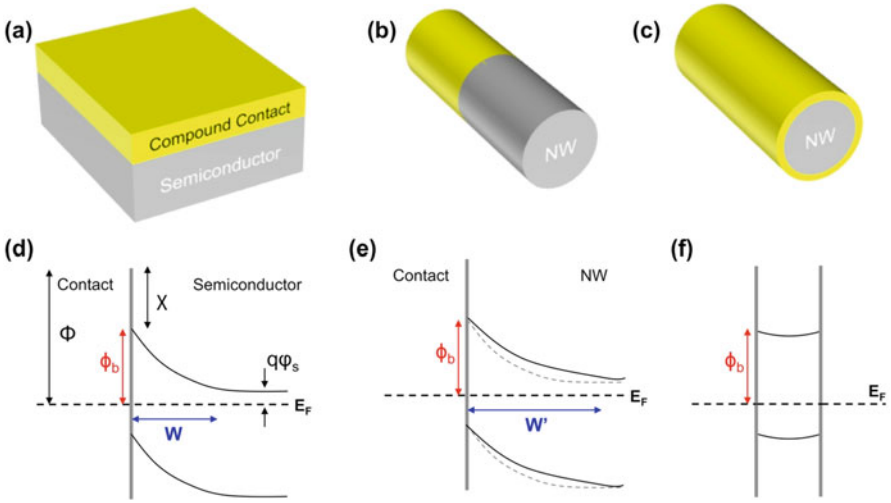

Fig. 5.18 Schematics for the band alignment diagrams for (**a** and **d**) planar-geometry contact, (**b** and **e**) end-bonded contact, and (**c** and **f**) side contact

For planar-geometry contacts (Fig. 5.18a), metal is deposited on the semiconductor surface followed by thermal anneal to form the compound interfacial layer. For nanoscale contacts, there are generally two categories: end-bonded contacts and side contacts [91]. The end-bonded contact (Fig. 5.18b) refers to the case that the metal or metallic contact has an abrupt interface with semiconductor in axial direction of nanochannels, in which atomic bonds form between the contact and the semiconductor. The compound formations in NW channels through metal diffusions as we discussed above all belong to this category. The side contact (Fig. 5.18c) refers to the metal embedded geometry in the NW radial direction. A simple deposition of metals on top of the NW is considered as in this category, in which a weak bond forms in between metal and NW. It has also been found that a metal that reacts with semiconductor at high temperature can readily form a thin layer of metal-semiconductor compound at the surface of NW upon deposition at room temperature, due to the latent heat during the condensation of metal vapor [108]. This also forms a side contact but with strong bonds (atomic bonds) between compound contact and semiconductor.

In the planar-geometry contact [109], the simplest model suggests that the electron SBH is given by:

$$\phi_b = \Phi - \chi \tag{5.14}$$

where Φ is the work function of metal-compound contact and χ is the semiconductor electron affinity as illustrated in Fig. 5.18d. The electrical charge flow across the contact-semiconductor interface equals the contact work function with

semiconductor Fermi-level and causes the conduction and valence band-edge bending near the interface. This band-edge bending is associated with a depletion (or accumulation) region and associated with a width given by:

$$W = \sqrt{\frac{2\varepsilon\phi_b}{nq}} \tag{5.15}$$

where ε is the dielectric constant of semiconductor, n is the dopant density, and q is the electron charge. In the presence of a Schottky barrier, the transport mechanisms are thermionic emission, tunneling through the barrier, and the electron-hole recombination in the depletion region. Usually, the electron-hole recombination current is much smaller than the other two, and the thermally excited tunneling current density can be expressed as [110]:

$$J_t = \frac{A^* T}{k} \int_0^\infty \tau(E) \cdot e^{-(E+q\varphi_s)/kT} dE \times \left[1 - e^{-qV_f/kT}\right] \tag{5.16}$$

where A^* is the Richardson constant, k is the Boltzmann constant, T is the temperature, and E is the conduction band-edge energy. $\tau(E)$ is the tunneling probability for carriers, V_f is the applied forward bias, and $q\varphi_s$ is the potential energy of the charge carriers relative to the Fermi level. And therefore the contact resistivity can be calculated as [111]:

$$\rho_c = \left(\frac{\partial J}{\partial V}\right)^{-1}\Bigg|_{V=0} \tag{5.17}$$

In the end-bonded contact, the depletion width was found to be larger than that in planar contact with same doping density and SBH [112]. This is related to the size-dependent fringing field in between metal contact and semiconductor NW surface. In small NWs, the strong fringing field makes the electric field lines near the contact interface incline to the ambient around the NW, causing a week electric field inside the NW. The reduced electric field screening in the small NWs results in larger depletion width, smaller tunneling current, and consequently larger contact resistivity. Shown in Fig. 5.19 are the simulation results of band-edge diagrams and contact resistivity changes versus NW radius, comparing the end-bonded contacts in NW (NW-3D contact and NW-1D contact) to planar-geometry contact [112]. It can be found that the contact resistivity of NW-1D contact is less vulnerable to change of NW size than that of NW-3D contact, indicating the advantages of forming metal-semiconductor compounds contacts inside the NW channels. In principle, high contact doping can reduce the depletion width and bring down the contact resistivity.

In the side contact, the band realignment due to charge transfer is weak due to the limited available depletion width in the NW cross section. Theoretical studies [113] of the side contact to NW device suggested that the nanoscale dimension of the NWs

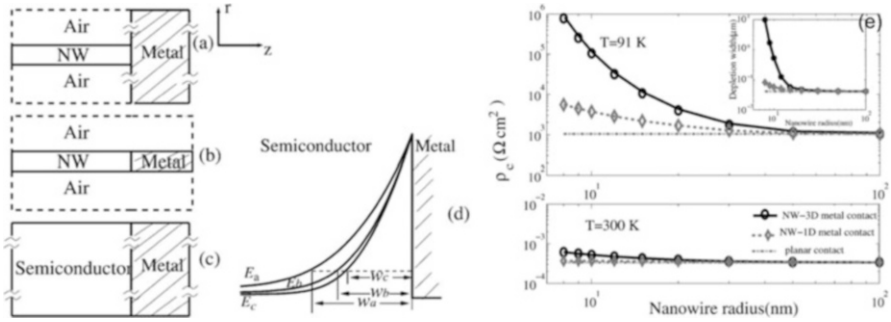

Fig. 5.19 Schematic illustrations of different contact geometries to NWs: (**a**) NW-3D metal contact, (**b**) NW-1D metal contact, and (**c**) planar contact. (**d**) Simulated energy band-edge diagrams for different contact geometries. (**e**) Contact resistivity vs NW radius for different contact geometries at temperatures equal to 91 and 300 K, respectively. (Reproduced with permission from Ref. [112]. Copyright 2008 American Institute of Physics)

prevents the energy band edge from reaching their asymptotic value and instead presents only a weak band bending. Shown in the Fig. 5.20 are the simulated results of band bending and contact resistance for a heavily doped Si NW (1×10^{19} cm^{-3}) with side contact. The results indicate that the conventional strategy of heavily doping the semiconductor to obtain Ohmic contacts breaks down as the NW diameter is reduced. A dramatical increase of contact resistance is expected for small NWs, as shown in Fig. 5.20c. By modeling the density of states using 1D equation in NW structures, the authors found that the quasi-1D system (NWs) requires almost 2 orders of magnitude larger density of pinning states compared with the bulk interface for the same effect of Fermi-level pinning, meaning that NWs are generally free of contact Fermi-level pinning for very small diameters. This in principle applies for end-bonded contacts as well.

In experimental measurements, the contact resistance between the compound contact and the semiconductor is sometimes misinterpreted. This is because the conventional four-probe technique can only contact resistance between metal/compound interface, but not the important compound/semiconductor interface. Transmission line measurement (TLM) is therefore a more preferred method, by patterning multiple metal pads with various spacing on a single NW channel followed by a short thermal annealing to form compound contact. An example is shown in Fig. 5.21 for TLM results on Ge/Si core/shell NWs with patterned Ni pads [114]. The fabrication was conducted on a 50 nm thick SiN_x membrane, so that after thermal annealing, the unreacted semiconductor NW segments can be precisely measured under TEM. As shown in Fig. 5.21, the contact resistance between $NiGe_xSi_y$ and Ge/Si NW is below 10 kΩ, which is significantly smaller than typical resistance values of a NWFET device made on the same type of NWs and operating at maximum transconductance. This suggested that the contact resistance was negligible in these Ge/Si core/shell NWFET performance analysis and mobility extraction.

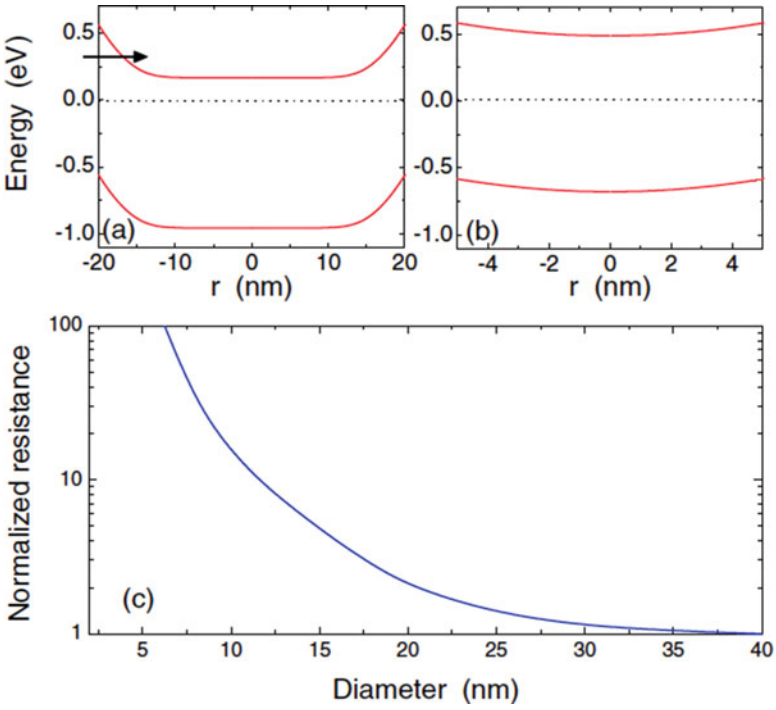

Fig. 5.20 Simulated energy band-edge bending across Si NWs (doping of 1×10^{19} cm^{-3}) with side contact for diameters of (**a**) 40 nm and (**b**) 10 nm. (**c**) The normalized resistance as a function of NW diameter. (Reprinted with permission from Ref. [113]. Copyright 2006 American Physical Society)

5.4.3 Ultrashort Channel Devices

Enhanced NW FET performance is enabled with ever-smaller channel lengths that can provide high on-current drives. The transistor channel length is usually defined by the metal gate width (in a gate-first self-aligned process) or the distance between its S/D electrodes, both of which requires expensive e-beam lithography tools or sophisticated photolithography techniques. The metal-semiconductor compound contact formation provides a lithography-free method to achieve ultrashort channel lengths in NW channels with controlled metal-semiconductor reactions. Figure 5.22 summarizes the prominent researches that demonstrated ultrashort NW channels with two terminal contacts. The most commonly used way was to monitor the metal-semiconductor NW reactions in situ inside a TEM or SEM chamber, and the ultrashort channels have been achieved in Si [72], Ge [76], and Ge/Si core/shell [17] NWs.

Joule heating-assisted nickel silicide reaction is shown in Fig. 5.22d–e, with the channel length monitored by the current measurements across the NW [115]. During

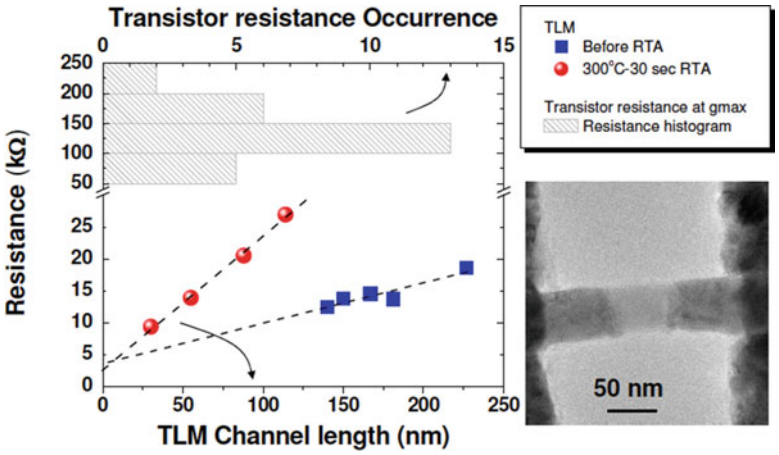

Fig. 5.21 NW resistance as a function of non-reacted semiconductor channel lengths. The contact resistance in Ge/Si core/shell NWs is extracted to be below 10 kΩ, which is much smaller than the typical resistance of the NW FET operating at maximum transconductance (histogram peaks at 100–150 kΩ). (Reprinted with permission from Ref. [114]. Copyright 2014 American Chemical Society)

this process, voltage V_1 and V_2 were applied on the metal strip at one side of the NW, and the joule heat peaked at the strip center and induced the Ni diffusion into the Si NW. The voltage drop across the NW, equaling to $(V_1 + V_2)/2$, introduced a current flow that was recorded to monitor the silicide reaction process. Silicide could also form at the other end of the Si NW by applying V_1 and V_2 on the opposite metal strip. Due to the Schottky barrier between silicide and Si, the recorded current through Si NW was low (dominated by thermionic emission) in long channels and increased slowly as channel length decreased. When the channel length was below 50 nm, the device showed a dramatic current increase due to the carriers effectively tunneling through Schottky barrier. With carefully monitored channel current, an ultrashort channel length of 8 nm was achieved.

It has also been found that the compound contact formation in NW channels can introduce tremendous strain in the semiconductor channel [38, 67]. In the study of $Ni_2In_{0.53}Ga_{0.47}As$ contact formation in $In_{0.53}Ga_{0.47}As$ NW, we observed a quasi-hydrostatic compressive stress exerted on the non-reacted $In_{0.53}Ga_{0.47}As$ channel, as shown in Fig. 5.23a. Inside the interfacial plane, formed $Ni_2In_{0.53}Ga_{0.47}As$ has a smaller lattice contact than that of $In_{0.53}Ga_{0.47}As$, while in the direction perpendicular to the interface, volume expansion in $Ni_2In_{0.53}Ga_{0.47}As$ phase introduced another compressive stress to the channel. The strain gradually vanished far from the interface (>100 nm) but caused a large energy bandgap change of $In_{0.53}Ga_{0.47}As$ at the contact interface (shown in Fig. 5.23b). In ultrashort NW channels, the strain could build up even higher (shown in Fig. 5.22f).[25]

To characterize the performance of the ultrashort channel device, we firstly monitored the NiSi NW reactions in TEM chamber through in situ heating, until

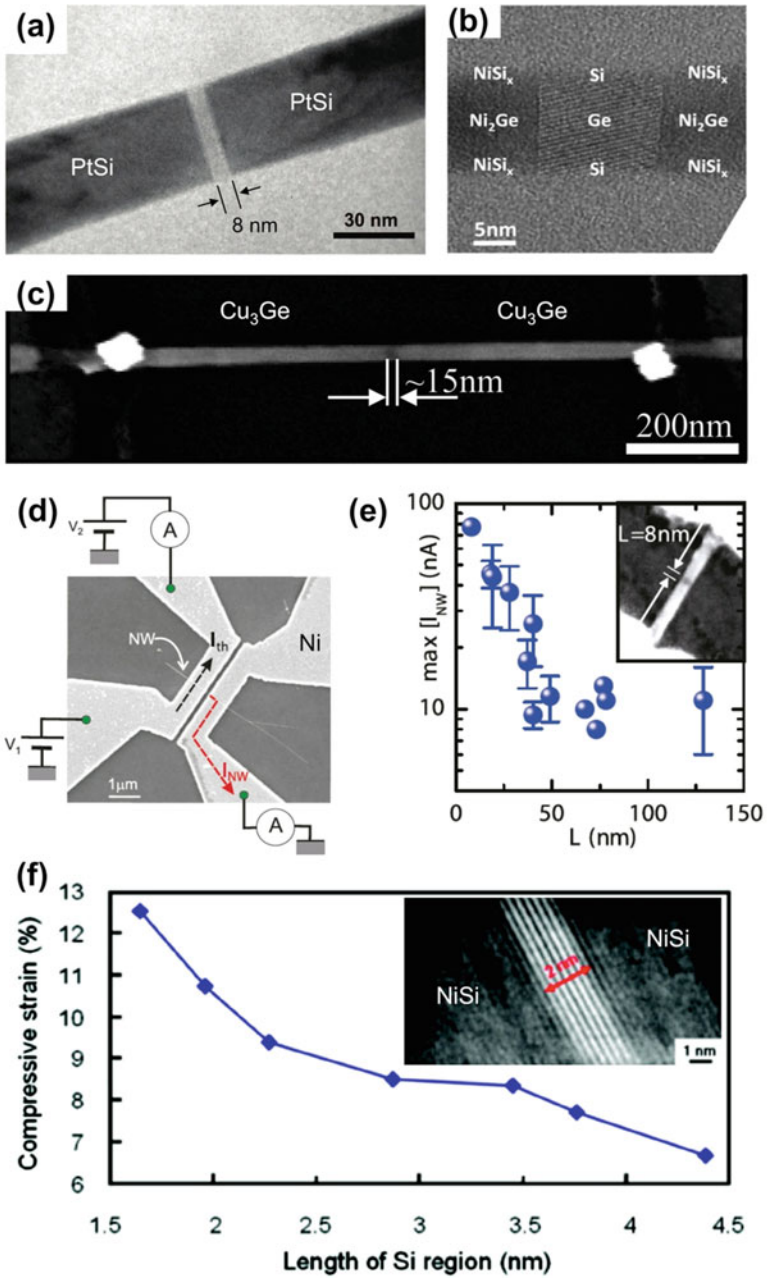

Fig. 5.22 (**a**) PtSi/Si/PtSi NW with Si length of 8 nm. Reprinted with permission from Ref [72]. Copyright 2008 American Chemical Society. (**b**) Ultrashort channel formed in Ge/Si core/shell NW. Reprinted with permission from Ref. [17]. Copyright 2014 IOP Publishing. (**c**) Cu_3Ge/Ge/Cu_3Ge NW with Ge length of 15 nm. Reprinted with permission from Ref [76]. Copyright 2009

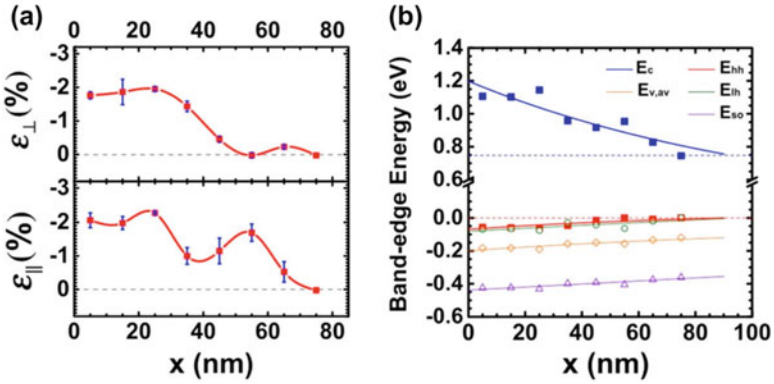

Fig. 5.23 (**a**) Out-of-plane and in-plane strains of $In_{0.53}Ga_{0.47}As$ as a function of distance from the interface with nickelide contact in $In_{0.53}Ga_{0.47}As$ NW channel. (**b**) The calculated band-edge energies as a function of distance along x-axis based on elastic theory that incorporates deformation potentials obtained from local density functional theory [116]. The estimated bandgap of $In_{0.53}Ga_{0.47}As$ near the InGaAs/nickelide interface is ~1.26 eV in this case. (Reproduced with permission from Ref. [67]. Copyright 2015 American Chemical Society)

reaching a channel length of 17 nm. Then, 10 nm HfO_2 was deposited on top as a gate dielectric, followed by the Ti gate deposition. The ultrashort channel device shows higher on-currents than those with longer channel lengths but with higher off-state current too because of the much larger NW diameter compared with the channel length (Fig. 5.24b), which enforced stronger short channel effects. The dependence of maximum transconductance, g_m, versus the channel length, L_G, is shown in Fig. 5.24c, and the performance gain with down-scaled transistor channels starts to saturate below 100 nm. This is because the Ni-silicide/Si SB contact resistance starts to dominate the on-state conduction at short channel lengths. Figure 5.24c inset shows an energy band-edge diagram of a Si NW SB FET in the on-state with a large potential drop across the contact SB and comparatively much smaller effective carrier-driving potential drop along the channel. This suggests that the SB contact engineering is vital to best fulfill the advantages of short channel SB-FETs.

Fig. 5.22 (continued) American Chemical Society. (**d** and **e**) Joule heating-assisted nickel silicide formation in Si NW with ultrashort channel length of 8 nm. Reproduced with permission from Ref [115]. Copyright 2011 American Chemical Society. (**f**) NiSi/Si/Si NW formed by anneal point-contacted Ni to Si NW. The channel strain was measured in those ultrashort channels. (Reproduced with permission from Ref. [38]. Copyright 2007 American Chemical Society)

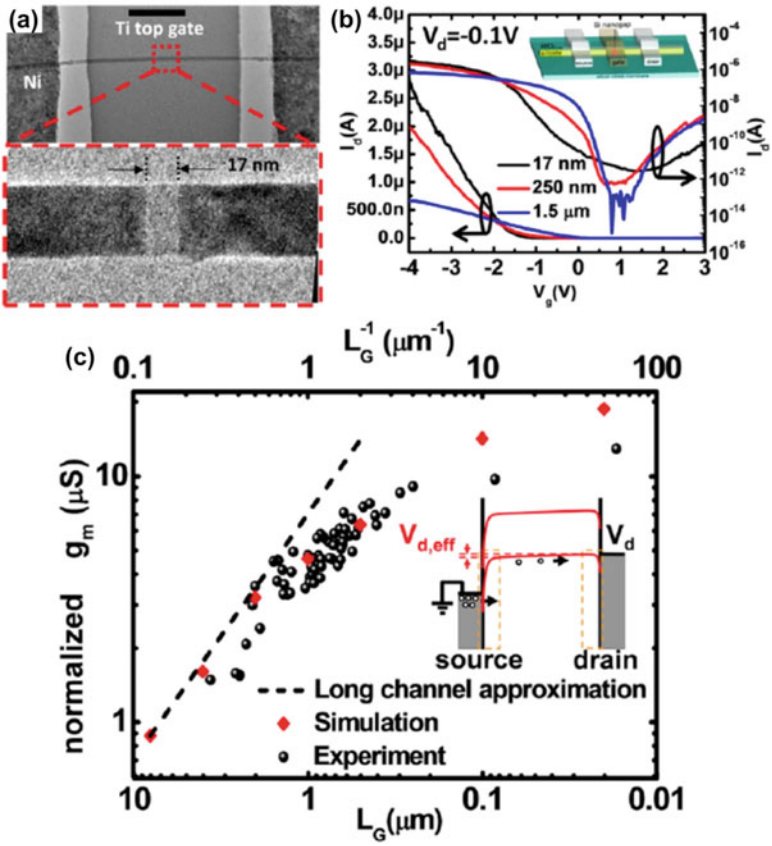

Fig. 5.24 (**a**) TEM image of a Si NW FET device with 17 nm channel length. Scale bar is 1 μm. (**b**) I_d–V_g characteristics of Si NW FETs with different channel lengths at $V_d = -0.1$ V at linear (left y-axis) and log (right y-axis) scales. Inset is a schematic of the ultrashort channel Si NW FET device. (**c**) Channel length-dependent device performance. Inset is the energy band-edge diagram of Si NW SBFET in on-state. (Reproduced with permission from Ref. [26]. Copyright 2012 American Chemical Society)

5.5 Conclusions

In this chapter, we discussed compound contacts to NW transistors that are formed by solid-state reactions between metal and semiconductor NWs. We introduced the observed phases of compound contacts formed in Si, Ge, and III–V NWs and discussed in detail about the multiphase coexistence in Si NW system and the quaternary compound phase analysis in III–V NW system. Then, we discussed the kinetic process during this solid-state reaction and proposed a model to distinguish the rate-limiting steps and to extrapolate the kinetic parameters. We then reviewed the dynamic process of the atomic-scale ledge nucleation and movements, together

with the special case when defects were present. These discussions paved the way for the introduction of electrical properties of NW transistors with these compound contacts. Different applications of these compound contacts were summarized, including tunable SBH electrical contact, spin-polarized carrier injection, infrared light detection, etc. Different contact geometries in NWs were discussed together with their band alignment and charge injection properties. Several reports on ultra-short channel devices were summarized where the channel lengths were controlled by the compound contact reaction. These comprehensive studies demonstrate the promise of compound contacts in nanoscale electronics.

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Chapter 6
Nanowire-Based Transparent Conductive Electrodes

Han-Yi Chen and Meng-Che Tu

6.1 Introduction

Transparent conductive electrodes (TCEs) are important segments in many optoelectronic devices, such as light-emitting diodes (LEDs) [1, 2], liquid crystal displays (LCDs) [3], thin-film transistors (TFTs) [4], touch screens [5–8], smart windows [5, 7], and solar cells [5, 7, 9, 10].

At the end of the 1960s, the industrial demand for transparent conductive oxides (TCOs) started since Sn and In_2O_3 were used in infrared light filters on low-pressure sodium discharge lamps in order to improve the lamp efficiency [11–13]. In_2O_3:Sn (ITO) has been the most efficient and widely used TCO material when the flat-panel display technology was explored since the 1970s [13]. ITO exhibits excellent electrical conductivity (electrical resistivity $\approx 10^{-4}$ Ω cm) and optical transparency (> 80%) which widen its applications in various optoelectronic devices.

Among different kinds of emerging technologies, one-dimensional (1-D) nanostructures such as nanowires, nanorods, and nanotubes provide high potential because of their special properties related to high aspect ratio and good crystallinity [14]. 1-D nanostructures not only provide a direct conduction pathway for enhancing charge collection but also increase the surface area which also improves the charge collection. ITO nanostructures with good performance have been successfully synthesized via physical vapor transportation methods [14–16]. In these ITO nanostructures, ITO nanowires are promising in various applications in nanoscale electronic and optoelectronic devices such as dye-sensitized solar cells (DSSCs) and LEDs [2, 17].

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Although ITO exhibits excellent electrical conductivity and optical transparency, researchers have been looking for the replacement due to the scarcity of indium which leads to increasing costs [18–20]. SnO_2:F (FTO) and ZnO:Al (AZO) have been developed because of their lower cost as compared to ITO [21, 22]. However, those TCOs are brittle and therefore are not compatible in flexible and stretchable electronic devices [23, 24].

Recently, nanostructured transparent conductive materials, including carbon nanotubes (CNTs), graphene, and nanostructured metals (such as metallic nanowires and metal grids), have attracted more attention owing to their promising properties and applications [18, 25–27]. The general requirements for those TCEs are sheet resistance $R_{sh} < 100\ \Omega$/sq and transmittance $T > 90\%$ in the visible range [28]. Lower sheet resistance (below 5 Ω/sq) is even necessary for the applications in large-area display and solid-state lighting [29]. The large contact resistance of tube–tube junctions in CNT networks restricts its practical applications. Metallic nanowire-based percolating networks such as silver nanowires (AgNWs) and copper nanowires (CuNWs) networks exhibit high flexibility, high optical transparency, and high electrical conductivity which are suitable for flexible electronic devices [20]. Owing to high aspect ratio of nanowires, those metallic nanowire-based percolating networks with little amount of raw materials can exhibit optoelectronic performances as good as ITO-based electrodes [14]. The required amount of indium in an ITO electrode is usually much higher than the amount of Ag in an AgNW electrode [3]. Furthermore, metallic nanowire networks can be prepared by solution processes which lead to low cost and enable large area deposition [13]. In addition to the optoelectronic applications mentioned in the beginning, metallic nanowire networks can also be used in transparent heaters [30–32], stretchable radio frequency antennas [33, 34], and transparent electromagnetic shielding [35, 36].

Different types of TCEs with different properties can be used in great diversity of possible applications. Striking a balance between the physical properties (optical, electrical, mechanical), stability (thermal, chemical, electrical, mechanical), processing methods, and costs of TCE materials in order to meet the requirements of certain market is also an important issue [15].This chapter focuses on overviewing different nanowire-based TCE materials and their applications. The synthesis, fabrication, and physical properties of TCO nanowires and metallic nanowire networks are described in Sects. 6.2 and 6.3, respectively. The applications for above TCE nanowires are discussed in Sect. 6.4.

6.2 Synthesis, Fabrication, and Physical Properties of Transparent Conductive Oxides

Transparent conducting oxides (TCOs) are wide-bandgap (≥3 eV) semiconductors which combine low electrical resistivity (10^{-4}–$10^{-3}\ \Omega$ cm), high optical transparency (>80% transmission of visible light), and high mobility ($\mu < 100\ cm^2\ V^{-1}\ s^{-1}$)

[13, 37]. TCOs with high carrier concentrations up to $n < 1.5 \times 10^{21}$ cm^{-3} are *degenerate semiconductors* in which the Fermi level has shifted to the conduction band (n-type TCOs) or valence band (p-type) of the host, resulting in metallic-like electrical conductivity [13, 37]. The electron concentration of n-type TCOs is 50–100 times lower than metals, while the resistivity is 50–500 times higher than bulk metallic conductors such as Au, Ag, Al, and Cu [13, 37].

Tin-doped indium oxide or so-called indium tin oxide (In_2O_3:Sn, ITO), fluorine-doped tin oxide (SnO_2:F, FTO), and aluminum-doped zinc oxide (ZnO:Al, AZO) are the most important TCOs for optoelectronic applications. The charge carriers in ITO, FTO, and AZO are generated by replacing In(III) by Sn(IV), O^{2-} by F^-, or Zn(II) by Al(III), respectively [13, 37].

The conductivity (σ) of material is related to three factors including carrier concentration (N), carrier mobility (μ), and elementary charge (e) and can be expressed as the following equation [13]:

$$\sigma = eN\mu \tag{6.1}$$

The carrier mobility μ is related to the free carrier scattering time, τ, and the carrier effective mass, m^*, as follows:

$$\mu = \frac{e\tau}{m^*} \tag{6.2}$$

The free carrier scattering time in TCEs is highly related to extrinsic factors including dopants, defects, or grain boundaries which are dependent on the preparation procedures. Because of the much smaller effective mass of electron than hole/ion, the mobility of electron is higher than hole/ion. The defects or dopants generate free carriers (electrons or holes) that determine the carrier concentration. The absorption of light by free carriers restricts the carrier concentration. The carrier gas generates a gathered plasma excitation in the electrical field of a light wave [13]. The Drude model gives the plasma frequency as follows which can predict the free charge density of a metal [13, 38]:

$$\omega_p = \sqrt{\frac{Ne^2}{m^* \varepsilon_r \varepsilon_0}} \tag{6.3}$$

where $\varepsilon_r\varepsilon_0$ is the permittivity of the material. The material is nearly transparent for $\omega > \omega_p$, while its absorption coefficient and the reflectivity are high for $\omega < \omega_p$ [39].

6.2.1 N-Type Transparent Conductive Electrodes

6.2.1.1 Indium Tin Oxide Nanowires

Indium tin oxide (ITO) is the most widely used n-type TCO nowadays owing to its excellent conductivity, high reflectivity, and low absorption in the region of visible light. ITO materials have been applied to various fields, including flat-panel displays [15], photovoltaics devices [39], radiation protection [40], and smart windows [41]. The electrical and optical properties of ITO material are influenced by its structure, morphology, and composition. Therefore, the preparation methods of ITO are crucial. The resistivity of commercial ITO is reported to be around 1×10^{-4} Ω cm [42], which is the lowest among commercial available n-type TCOs. The transmission of ITO film could be optimized up to 95% [43] by different synthesis methods.

Several processes have been developed to grow ITO thin film, including chemical vapor deposition (CVD) [44], sputtering [45], evaporation [46], sol-gel process [47], and spray pyrolysis [48]. Each methodology has its own advantages and issues. Generally, sputtering technique is able to produce high quality, high purity, and good uniformity of the thin film. Because of the intensive development of nanotechnology in recent years, the growth of 1-D nanostructures of ITO has been developed owing to its advantages such as high surface area, enhanced active sites, and reduced diffusion distances. Different kinds of synthesis methods to grow ITO nanowires have been utilized and well-studied.

Chiquito et al. [49] reported a synthesis method of 1-D ITO nanowires through vapor–solid (VS) process with carbothermal evaporation at 1150 °C. The diameters of those ITO nanowires were ranged from 4 to 60 nm with the length of several microns. This group utilized microfabricated device to measure the electrical transport properties of individual nanowires as shown in Fig. 6.1. The results showed that decreasing the dimensions of the wires changes them from metallic to a nonmetallic character of the transport owing to quantum effects.

Pho Nguyen et al. [16] synthesized ITO nanowire arrays via a carbothermal reduction followed by a catalyst-mediated heteroepitaxial growth at process temperature of 840 °C. The heteroepitaxial growth process enables complicated ITO cross-networks which are composed of uniform ITO nanowires and leads to highly regular ITO nanowire arrays with high density. Wan [50] reported vertically aligned ITO single-crystalline nanowire arrays in a pulsed laser deposition system by using Au-catalyzed vapor–liquid–solid (VLS) method. The synthesis temperature could be reduced dramatically to 600 °C due to the utilizing of Au catalyst. The diameter and length of Au-catalyzed ITO nanowires are <200 nm and ~2.5 μm, respectively, as shown in Fig. 6.2. The author claimed this 1-D material is promising for vacuum electron emitter application because of their high aspect ratio and small tip radius of curvature. The as-grown ITO nanowires exhibit an increased field emission with a turn-on field of ~2.0 V m^{-1} at a current density of 1 A cm^{-2}. In addition to the

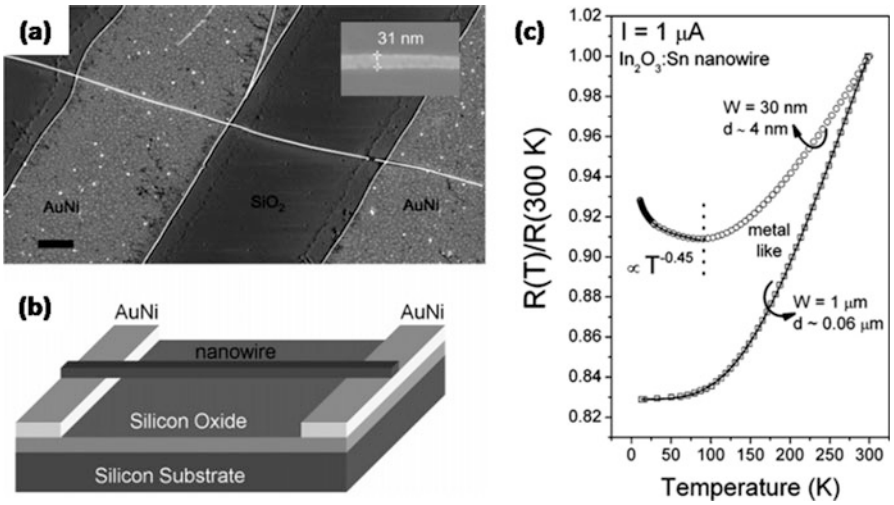

Fig. 6.1 Microfabricated device for measuring individual nanowire is shown in panel (**a**). The scale bar is 1 μm. A 31-nm-thick Sn-doped In_2O_3 nanowire was trapped on the two Au/Ni electrodes of the device (insert). The doping level used was $n = 1.8 \times 10^{20}$ cm^{-3}. (**b**) Sketch of the device. (**c**) Temperature-dependent resistance measurements for two different samples. (Reprinted from Ref. [49], Copyright 2007, with permission from American Chemical Society)

growth of single-crystalline ITO nanowire, the level of tin doping also influences the electrical and optical properties of ITO nanowires.

Gao et al. [14] tuned the amount of tin in ITO nanowires in order to optimize the sheet resistance and transmittance. The results showed a low sheet resistance of 6.4 Ω/sq, and the resistivity of an individual nanowire was 2.4×10^{-4} Ω cm with a carrier concentration up to 2.6×10^{20} cm^{-3}. An optical transmittance around 80% was detected in the visible region.

With regard to the applications, ITO nanowires have been extensively used as electrodes in photovoltaics and energy storage devices. Ednan Joanni et al. [51] reported a dye-sensitized solar cell (DSSC) with ITO nanowire electrode. The ITO nanowires were grown via chemical vapor deposition technique, and the titanium dioxide (TiO_2) nanoparticles were then coated on ITO nanowires by RF sputtering, followed by coating the dye and platinum to assemble the cell. This 3-D architecture reduces the probability of electron-hole recombination by shortening of electronic transport length. Yan et al. [52] reported an energy storage device based on ITO nanowire electrodes as shown in Fig. 6.3. The cyclic voltammetry characterizations revealed that the rate capability of $Co(OH)_2$/ITO nanowire electrodes was better than $Co(OH)_2$/stainless steel electrodes. This unique hierarchical architecture enhances the conductivities of electrode and electrolyte resulting in the improvement of rate capability. Similar 1-D heterostructured ITO nanowires are used as electrodes for lithium-ion batteries (LIBs) [53]. Kim et al. prepared core–shell $SnO_2-In_2O_3$ heterostructured nanowires via one-step CVD method. The formation of this core–shell structure was based on the differences of the reactivity between SnO_2 and

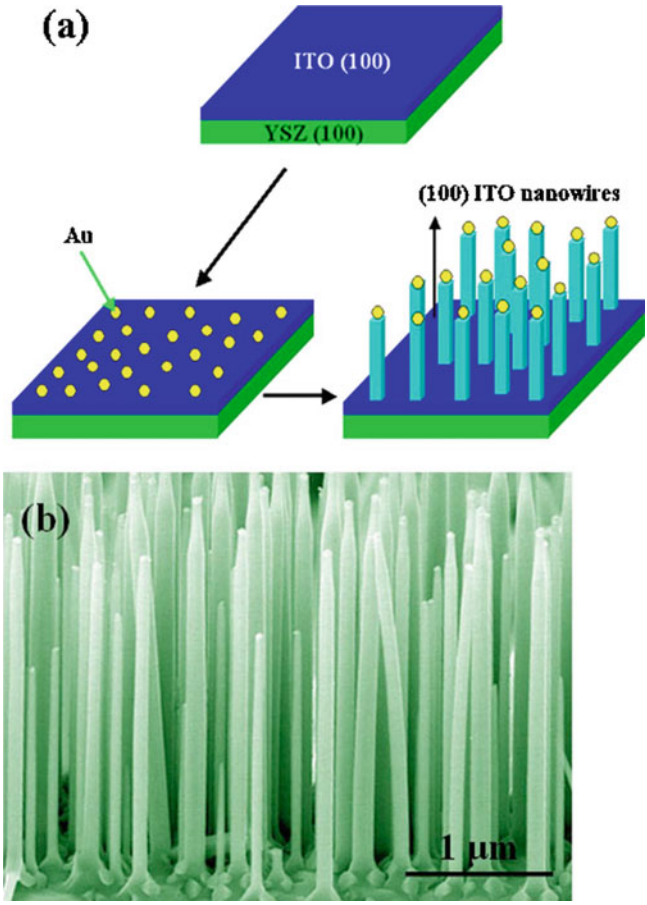

Fig. 6.2 (**a**) Schematic view of processes for vertically aligned ITO nanowire arrays grown on ITO buffer layer/(100) YSZ substrate. (**b**) A side-view SEM image of the vertically aligned ITO nanowire arrays grown on ITO/(100) YSZ substrate. (Reprinted from Ref. [50], Copyright 2006, with permission from AIP Publishing)

In_2O_3. The specific capacity of this core–shell $SnO_2-In_2O_3$ heterostructured nanowire was 60% higher as compared to pure SnO_2 electrode. Park et al. [54] also employed ITO nanowires as electrode for LIBs. These ITO nanowires were synthesized by combination of thermal evaporation process and pulsed laser deposition (PLD). The diameters of the nanowires were around 40 nm with the lengths of several tens of micrometers. This nano-architectured ITO/TiO_2 hybrid electrode exhibits excellent electrochemical performance with high-rate capabilities and superior cycling stability up to 1000 cycles at a current density of 60 C in the range of 1.0–2.2 V.

Molecular beam epitaxy (MBE) is another system that was used to grow ITO nanowires under high vacuum (10^{-8}–10^{-12} Torr). O'Dwyer et al. [2] developed a

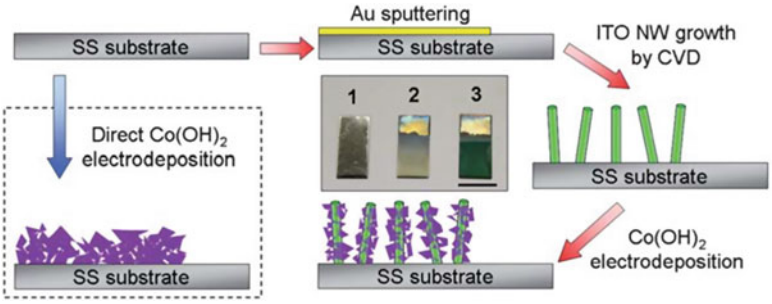

Fig. 6.3 Schematic models showing the fabrication procedures of $Co(OH)_2$ and $Co(OH)_2$/ITO nanowire electrodes for comparative studies. The $Co(OH)_2$/ITO nanowire electrodes were fabricated by combinational CVD and electrodeposition methods. The inset is the digital image of Au/SS (sample 1), ITO NW/SS (sample 2), and final $Co(OH)_2$/ITO nanowire/SS (sample 3). Scale bar: 1 cm. SS: stainless steel. (Reproduced with permission from Ref. [52]. Copyright (2011) Royal Society of Chemistry)

bottom–up growth method for ITO nanowires on silicon substrate via MBE system at 500–600 °C (Fig. 6.4). In and Sn precursors were utilized to grow branched ITO nanowires on silicon and oxidized silicon surfaces under oxygen atmosphere. The diameter and length of ITO nanowires were ranged from 8 to 20 nm and 40 to 500 nm, respectively. The transmittance of those as-grown ITO nanowires was higher than 80% in visible region and more than 90% between wavelength of 1200 and 1600 nm. The resistivity of branched ITO nanowires was reported to be 1.7×10^{-4} Ω cm when the deposition rate is 0.2 nm s^{-1} for In and Sn.

6.2.1.2 Doped Zinc Oxide Nanowires

ITO is the most common used TCO material to date. However, the limit natural abundance of indium leads to high cost and it is not sufficient for high-volume production of optoelectronic devices [55]. Moreover, the superior electrical and optical performances of ITO are decayed when being exposed to a hydrogen plasma atmosphere [56]. Besides, ITO shows low crystalline quality and relatively high sheet resistance (R_s > 50 Ω/sq) on flexible substrates by vacuum deposition [57]. Therefore, developing new materials that are low cost with good electrical and optical properties in order to meet the stringent requirements of optoelectronic devices is highly important.

Zinc oxide (ZnO) has attracted a significant interest as a well-suited TCO material to replace ITO [38, 55, 57]. It has wide direct bandgap of ~3.4 eV, high natural abundance, low toxicity, high thermal stability, good resistance against hydrogen plasma processing damage, lower cost compared with ITO, and competitive electrical and optical properties [38, 55–57]. However, pure ZnO is naturally n-type with poor conductivity. Introducing oxygen vacancies by thermal treatment in a reducing atmosphere or doping with heteroatoms such as Al, Ga, In, B, or Sn can improve the

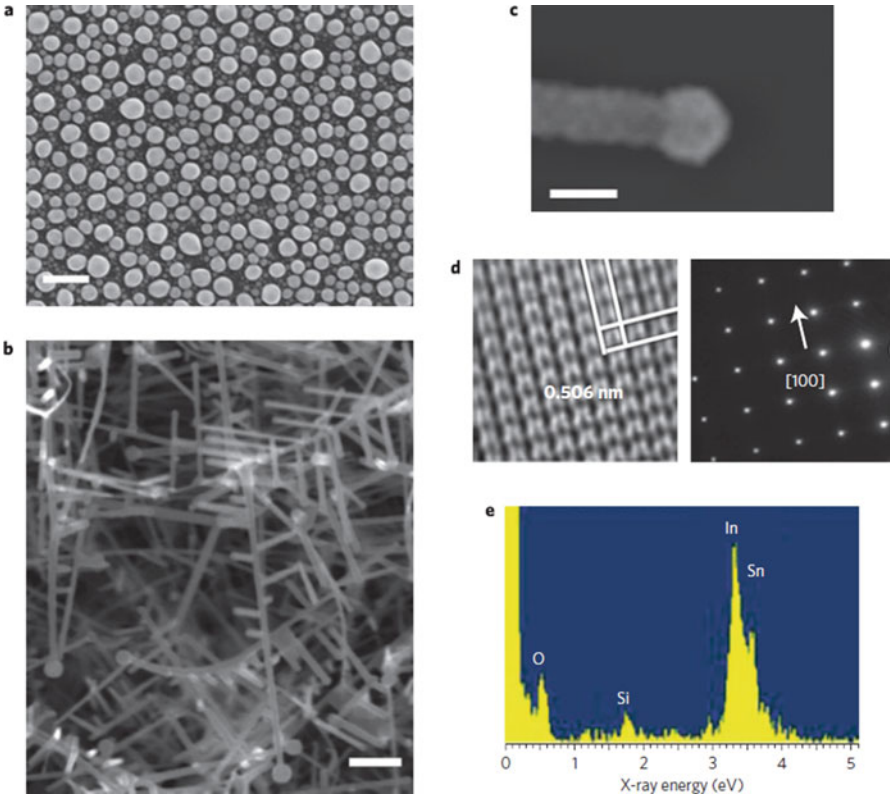

Fig. 6.4 (**a**) Plan-view SEM image of oxidized In–Sn droplet seed crystals under MBE deposition conditions of $T_{sub} = 400$ °C, $T_{In} = 835$ °C, and $T_{Sn} = 1000$ °C and at a rate of 0.1 nm s^{-1}. These seeds nucleate the precipitative growth of the nanowire. Scale bar, 100 nm. (**b**) Cross-sectional SEM image of the interior of the nanowire layer grown at $T_{sub} = 400$ °C at nominal In:Sn (90:10) growth rates of 0.1 nm s^{-1}. Scale bar, 50 nm. (**c**) SEM image of the faceted seed crystal–nanowire interface. (**d**) The higher-magnification HRTEM image and associated selected-area electron diffraction pattern clearly identify the monocrystalline cubic $(In_{1.875}Sn_{0.125})$ O_3 phase with (002) and (020) interplanar spacings of 0.506 nm. (**e**) Large-area EDX spectrum of the nanowire layer showing the In and Sn L-edge lines and O and Si substrate lines. (Reprinted from Ref. [2], Copyright 2009, with permission from Springer Nature)

conductivity of ZnO [38, 56, 58, 59]. Electron mobility of ZnO single crystals at low doping levels is up to ~200 cm^2 V^{-1} s^{-1}, and the value decreases at higher doping levels [59]. Among various doped ZnO TCOs, Al-doped ZnO (AZO) attracts more attention because of its low electrical resistivity (~10^{-4} Ω cm) and optical transparency as well as relatively low cost which is a promising candidate to replace ITO [55, 57, 60–62].

High-quality AZO thin films can be deposited under vacuum or high temperatures. However, AZO prepared by sputtering or CVD has difficulty to obtain uniform thin films due to the high reactivity of Al with residual O_2 [57]. AZO nanowires can

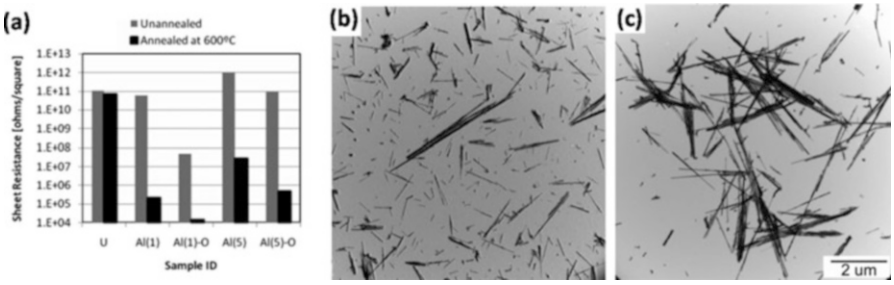

Fig. 6.5 (**a**) Sheet resistance of spin-coated, intrinsic, and Al-doped ZnO NW films (U, intrinsic ZnO; Al(1), 1% Al; Al(1)-O, 1% Al, with oleic acid; Al(5), 5% Al; Al(5)-O, 5% Al, with oleic acid). TEM images of (**b**) Al(1) and (c) Al(1)-O samples. (Reprinted from Ref. [57], Copyright 2010, with permission from John Wiley and Sons)

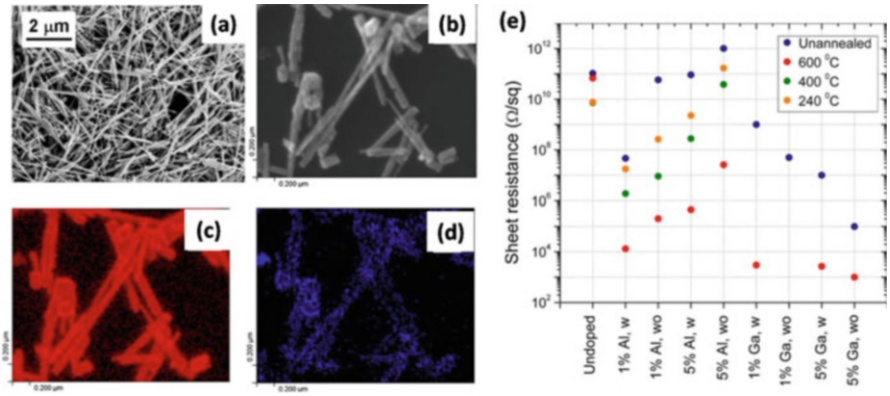

Fig. 6.6 (**a**) SEM micrographs of drop-cast film of ZnO nanowires, 5% Ga, without oleic acid. AES analysis of ZnO nanowires synthesized in Ga solutions: (**b**) SEM micrograph, (**c**) Zn Auger electron map, and (**d**) Ga electron map. (**e**) Sheet resistance of nanowire films formed from different batches and annealing conditions (w, with oleic acid; wo, without oleic acid). (Reproduced with permission from Ref. [63]. Copyright (2008) Springer Nature)

be prepared through solution process, and it is compatible with roll-to-toll processing by dispersing AZO nanowires in a solvent.

Kusinski et al. [57] synthesized intrinsic and Al-doped (1% and 5% nominal atomic concentration of Al) ZnO nanowires by solution process. Those nanowires were prepared by dissolving Zn acetate and Al acetate in trioctylamine at 300 °C. The effect of different doping conditions, a surfactant (oleic acid), and annealing were also investigated. The sheet resistance of spin-coated, intrinsic, and Al-doped ZnO NW films and the TEM images of Al-doped ZnO NWs are shown in Fig. 6.5 [57].

Goris et al. [63] reported a Ga-doped ZnO (GZO) nanowire film which exhibited a sheet resistance of ~10^3 Ω/sq as shown in Fig. 6.6. GZO nanowires were prepared through thermal decomposition of zinc acetate and gallium nitrate in trioctylamine at

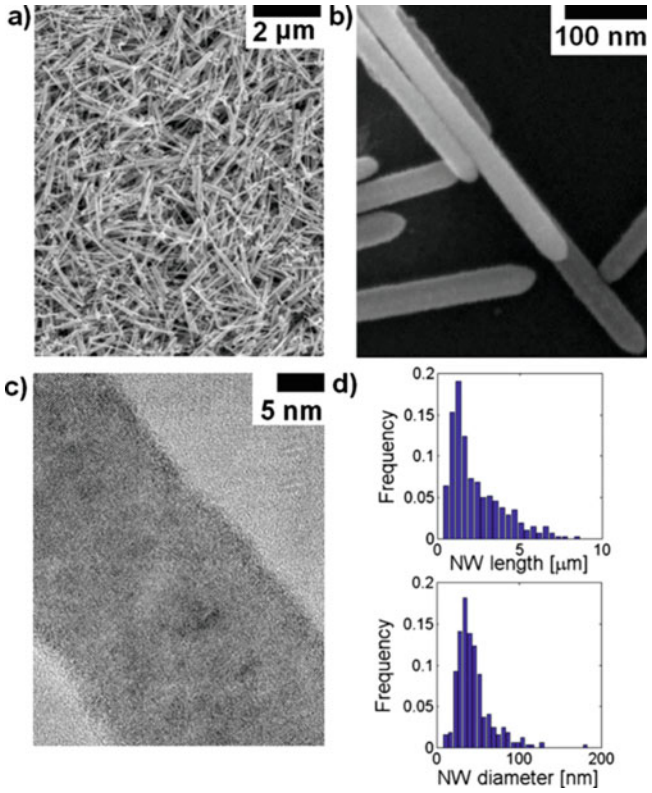

Fig. 6.7 Scanning electron micrographs (**a** and **b**) showing representative samples of the synthesized nanowires. High-resolution electron microscopy (**c**) shows the crystallinity of the solution grown nanowires. The length and diameter statistics for a population of ~350 nanowires are also shown (**d**). (Reprinted from Ref. [38], Copyright 2010, with permission from AIP Publishing LLC)

synthesis temperature of 300 °C. The effects of surfactants (oleic acid) and annealing temperature on the growth of the nanowires were also studied.

Noriega et al. [38] applied a comprehensive set of spectroscopic techniques to investigate the electrical properties of highly Al-doped ZnO nanowires which were synthesized by solution-based low-temperature process (300 °C). The morphology of highly Al-doped ZnO nanowires was measured by SEM and HR-TEM as shown in Fig. 6.7. The as-prepared nanowires have highly crystallinity with diameters and lengths in the 20–80 nm range and few microns, respectively. Carrier mobility and charge density of those AZO nanowires obtained from sensitive optical absorption measurements (applying Drude model) and single-wire field-effect transistor devices (SWFETs) are similar. The mobility of undoped ZnO nanowires is ~28 cm^2/V s and reduces to 14 cm^2/V s with highest Al-doping density as shown in Fig. 6.8. However, the charge carrier density remains approximately constant 10^{20} cm^{-3} without

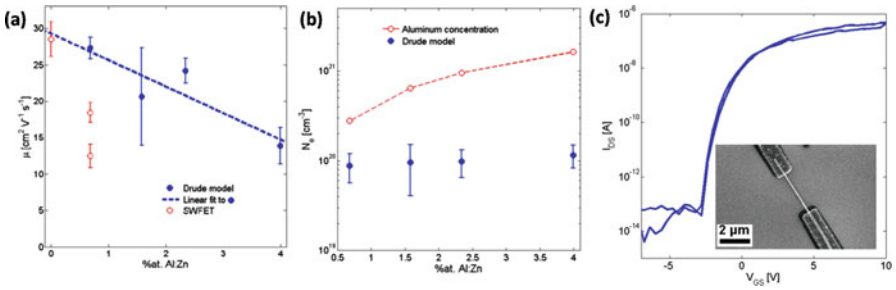

Fig. 6.8 (**a**) Carrier mobility calculated from SWFET measurements (○), as well as values obtained with the Drude model fits (●). (**b**) Concentration of aluminum atoms (○) for various doped ZnO nanowires compared to the free carrier density calculated with the Drude model fits (●). Error bars are ± one standard deviation. (c) Transfer curve of an undoped ZnO nanowire FET with a drain source voltage $V_{DS} = 1$ V (inset, SEM image of the device). The SWFET devices are fabricated from typical AZO nanowires (Fig. 6.7). (Reproduced with permission from Ref. [38]. Copyright (2010) AIP Publishing LLC)

relationship on the Al:Zn ratio. This indicates a limited dopant activation in the ZnO lattice or the appearance of charge-compensating defects. The minimum resistivity of AZO nanowires measured optically was 2.6×10^{-3} Ω cm for wires with 0.68 at % Al.

The vertically aligned AZO nanowire arrays can be synthesized by a seed-assisted wet-chemical method reported by Zang et al. [64]. A cleaned Ti substrate was deposited with a ZnO seed layer using a wet-chemical-annealing method [65] and then was immersed in an autoclave with a solution containing zinc nitrate, aluminum nitrate, and hexamethylene tetramine. The autoclave was heated to 93 °C for 24 h, and the vertically aligned AZO NW arrays were obtained. The morphology of AZO NW arrays was characterized by SEM and TEM as shown in Fig. 6.9, and the average diameter of AZO NW arrays is ~100 nm with the average length ~2 mm. The NW that grows along [0001] direction with a good crystalline nature can be found from the HRTEM image and the select area electron diffraction (SAED) pattern in Fig. 6.9d.

Xu et al. [66] introduced a simple wet-chemical treatment method to in situ fabrication of $ZnFe_2O_4$ onto conductive AZO nanowire arrays for solar-driven water splitting. A hydrothermal growth method was utilized to grow AZO nanowire arrays on FTO substrate at 88 °C, and then the sample was immersed into 0.02 M $FeCl_3$ ethanol solution for 1 min to 7 min. After washing with ethanol and drying at 70 °C, the sample was annealed at 550 °C for 1 h in order to introduce the Fe into $ZnFe_2O_4$ with better crystallinity. The diameters of ~130 nm and lengths of ~7 mm of the as-prepared 0.5% Al-doped ZnO nanowire arrays are observed from SEM images as shown in Fig. 6.10a. Figure 6.10b–d shows the SEM images of AZO NW arrays treated with $FeCl_3$ ethanol solution for 1 min to 7 min. As the treatment time increased, the center of AZO nanowire began to dissolve, leading to a hollow structure on the upper section of each nanowire, and then converts the nanowires into nanotubes.

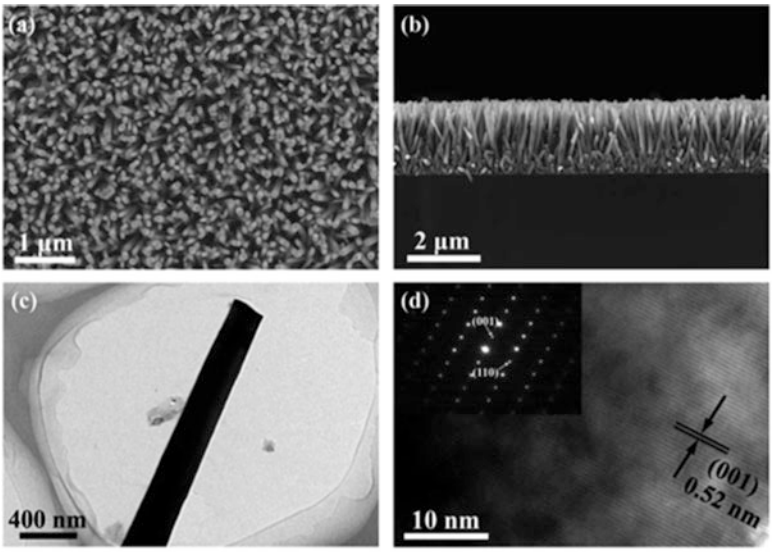

Fig. 6.9 (**a**) SEM image of AZO NW arrays in a top view. (**b**) SEM image of AZO NW arrays in a side view. (**c**) TEM image of one single AZO NW. (**d**) HRTEM and SAED pattern of the tip region of AZO NW. (Reprinted from Ref. [64], Copyright 2014, with permission from Royal Society of Chemistry)

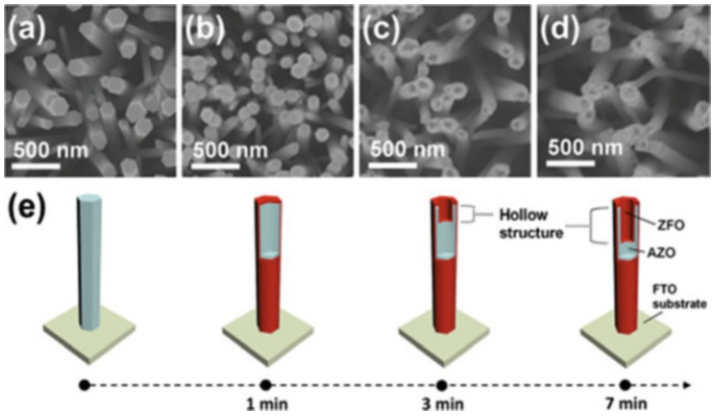

Fig. 6.10 SEM images of (**a**) 0.5% AZO and 0.5% AZO–ZFO with treatment times of (**b**) 1 min, (**c**) 3 min, and (**d**) 7 min. (**e**) The schematic illustration of morphology evolution for the AZO and AZO–ZFO composite photoanodes with different treatment times. (Reprinted from Ref. [66], Copyright 2016, with permission from Royal Society of Chemistry)

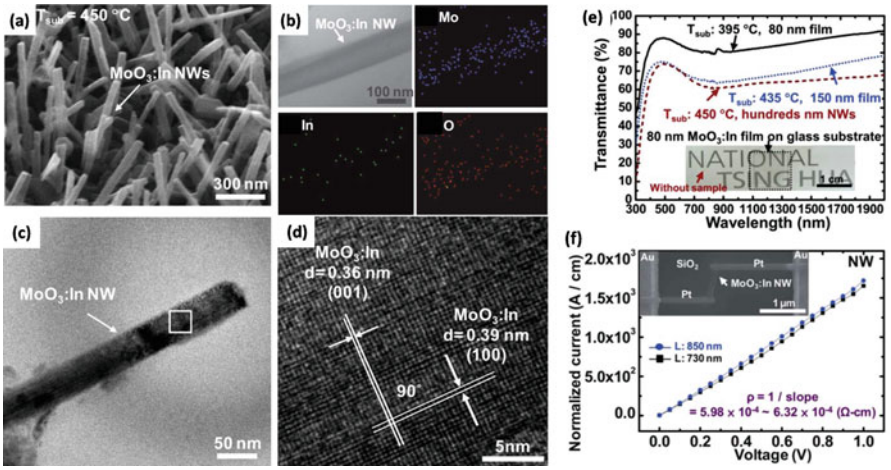

Fig. 6.11 (**a**) The SEM images of MoO_3:In NWs at substrate temperature of 450 °C. (**b**) A bright-field TEM image of an MoO_3:In NW and its elemental mapping of Mo, In, and O. (**c**) A bright-field TEM image of a MoO_3:In NW and (**d**) a high-resolution TEM image taken from the boxed area of (**a**). (**e**) Optical transmittance spectra of MoO_3:In NWs and films on glass substrates. (**f**) Normalized I–V curves of two individual MoO_3:In NWs with the inset showing the typical SEM image of the test pattern for I–V measurements. (Reprinted from Ref. [77], Copyright 2011, with permission from Royal Society of Chemistry)

6.2.2 P-Type TCO Nanowires

After the first p-type TCO, NiO, was announced in 1993 by Sato et al., several potential p-type TCOs have been developed such as $CuAlO_2$, $CuGaO_2$ [67], $CuCrO_2$ [68], $CuYO_2$ [69], Cu_2SrO_2 [70], $CuInO_2$ [71], $(Cu_2S_2)(Sr_3Sc_2O_5)$ [72], $Sr_2Cu_2ZnO_2S_2$ [73], AgInO [74], ZnO [75], and MoO_3:In. Similar with n-type TCOs, the requirements for p-type TCOs are low resistivity, high hole mobility, and high transparency. The resistivity of Mg-doped $CuCrO_2$ films is around 4.5×10^{-3} Ω cm with a transmittance of around 40% at a wavelength of 500 nm. Cu_xS [76] was reported as a transparent p-type semiconductor with a low resistivity around 6.53×10^{-4} Ω cm, while the transmittance of 50-nm-thick films is only 40% at a wavelength of 500 nm.

Chen et al. [77] reported the first p-type TCO nanowires with indium-doped molybdenum (MoO_3:In) oxide. The hole mobility of intrinsic MoO_3 is relatively high as compared to other p-type materials, and it can be used as hole transport layer in organic polymer solar cells. Nevertheless, the conductivity of intrinsic MoO_3 is low. Therefore, the author introduced indium as dopant in MoO_3 in order to enhance its hole concentration and conductivity. The growth of MoO_3:In was conducted based on vapor–solid (VS) mechanism via CVD technique. Both MoO_3:In nanowires and thin films could be obtained at different substrate temperatures as shown in Fig. 6.11. The composition with 45.65 wt % In_2O_3 in MoO_3:In amorphous thin film (80 nm thick) deposited at a substrate temperature of 390 °C exhibits the lowest resistivity (2.5×10

$^{-3}$ Ω cm) and highest hole carrier concentration (2.1×10^{20} cm^{-3}) with moderate hole mobility (11.9 cm^2 V^{-1} s^{-1}). The MoO_3:In single-crystalline nanowires can be obtained at a substrate temperature of 450 °C with a lowest resistivity around 6 x 10^{-4} Ω cm for individual nanowires. In addition to the electrical properties, the optical properties for thin film and nanowires were also measured. The transmittance was ~60% for 270-nm-thick film and ~90% for 50-nm-thick film. MoO_3:In NWs with a length of hundreds of nanometers exhibited a relatively higher transmittance of ~74%. The author also demonstrated its feasibility on flexible substrate (polyimide) for the potential application of flexible electronic.

Another nanostructured p-type TCO, $CuAlO_2$ was synthesized by Liu et al. [78] based on electrospray and electrospinning methods. The electrosprayed film demonstrated 20–50% transmittance in visible region, while the electrospun wire showed a higher transmittance between 50 and 70% in visible region. Nevertheless, current p-type TCOs cannot provide both high transparency and conductivity characteristics like n-type TCOs.

6.3 Synthesis, Fabrication, and Physical Properties of Carbon Nanotube Networks

6.3.1 Transparent Conducting Carbon Nanotube Network Films

Carbon nanotubes (CNT) has been extensively investigated and used in various applications in past decades due to its superior properties including excellent conductivity, high surface area to volume ratio, and good thermal stability. The inherent network architecture comprised from the 1-D nature of CNT with high aspect ratio enables CNT network films to present low electrical resistivity with high optical transmittance in the visible range with film thicknesses below 100 nm [79]. Those properties indicate thin layer CNT as promising TCEs.

Pure single-walled carbon nanotubes (SWCNTs) were utilized to prepare TCEs by a simple filtration process as reported by Wu et al. [80]. The ultrathin SWCNT films can be transferred to various substrates. This filtration process can provide homogeneous films with controllable film thickness. Besides, the size of SWCNT film is restricted only by the diameters of the filtration membranes, which could be few meters long for available membranes. The as-prepared SWCNT film (thickness of 50 nm) exhibited a sheet resistance and a resistivity of 30 Ω/sq and 1.5×10^{-4} Ω. cm, respectively, with a transmittance of ~70% in visible region. In order to overcome the size limitation, Pei et al. [81] prepared a SWCNT film by combining electrophoretic deposition with hot press transferring. This method enables mass production without the limitation of membrane size, controllable thickness by deposition time, and strong adhesion between SWCNT film and flexible substrate.

The sheet resistance of this 54-nm-thick SWCNT film was 20 Ω/sq with an optical transmittance of 81%. In addition to the membrane size limitation of film production, another issue for filtration process was the irregular morphologies and significant roughness, which might result in short circuits and poor reproducibility during device assembling. Tenent et al. [82] utilized an ultrasonic spraying method to prepare uniform SWCNT film with low surface roughness (~3–8 nm) on arbitrarily large substrates. This SWCNT film also exhibited high transparency and low electrical resistivity. Low roughness of SWCNT film led a comparable energy conversion efficiency (3.1%) with ITO film (3.6%) as an electrode for solar cells. The electrical and optical properties could be also enhanced by chemical treatment. Geng et al. [83] presented an enhanced sheet resistance without affecting the optical transmittance by acid treatment. The SWCNT films were treated with several acids, and the sheet resistance of the SWCNT film which was immersed in 12 M HNO_3 for 60 min was significantly decreased by a factor of about 2.5 times with negligible change of transmittance in the visible region. This SWCNT film exhibited a sheet resistance of ~40 Ω/sq with a corresponding transmittance of 70%.

In addition to CNT, another carbon-based material, graphene, was also developed as TCE for various application. Graphene, a two-dimensional monolayer of sp^2-bonded carbon atoms, shows similar or even better physical properties with CNT. Wang et al. [84] fabricated a graphene TCE by reducing graphene oxide. The sheet resistance and optical transmittance of 10-nm-thick graphene TCE were ~1.8 Ω/sq and 50–70% in visible region, respectively. Li et al. [85] proposed an improved transfer process of large-area graphene deposited on Cu foils via CVD technique as shown in Fig. 6.12. An additional polymethyl methacrylate (PMMA) layer was coated on the PMMA/graphene layer which was transferred on the SiO_2/Si substrate. These graphene films with additional PMMA coating in the preparation process provided smooth surface without cracks and exhibited high electrical conductivity and high optical transmittance which enable graphene films a suitable candidate for TCE applications. Figure 6.12e compares the sheet resistances and transmittances at $\lambda = 550$ nm for graphene, SWCNT, and ITO films. The graphene films prepared by the abovementioned improved transferred method showed higher transmittance with comparable sheet resistance as compared to other graphene grown on Ni. Besides, these graphene films on PMMA exhibited even lower sheet resistance than SWCNT films. An even larger-scale production of graphene (>100 meters) as transparent conductive film via roll-to-roll CVD technique was reported by Kobayashi et al. [86]. The sheet resistance of this 100-meter-long graphene transparent conductive film was 150 Ω/sq.

In general, carbon-based materials have been demonstrated as high-potential TCE candidates in aspect of cost-effectiveness, compatibility on flexible substrate, and large-scale production. However, the transmittance and sheet resistivity of carbon-based films should be further improved in order to achieve better electrical and optical properties as same as the commonly used ITO films.

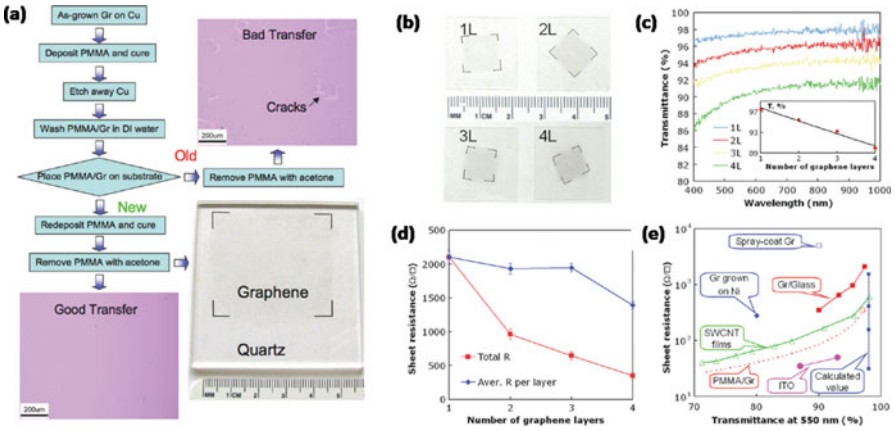

Fig. 6.12 (**a**) Processes for transfer of graphene films ("Gr" = graphene). The top-right and bottom-left insets are the optical micrographs of graphene transferred on SiO_2/Si wafers (285-nm-thick SiO_2 layer) with "bad" and "good" transfer, respectively. The bottom-right is a photograph of a 4.5 × 4.5 cm^2 graphene on quartz substrate. (**b**) Photographs of 1 cm^2 films with one up to four layers of stacked graphene films on cover glass slips. (**c**) Transmittance of n-layer graphene films shown in (**b**). The inset is the relationship between the transmittance, T (%), and $\lambda = 550$ nm as a function of the number of stacked graphene layers, n. (**d**) Sheet resistance of n-layer graphene films as a function of the number of stacked graphene layers, n. (**e**) Comparison of transparent conductive films. (Reprinted from Ref. [85], Copyright 2009, with permission from American Chemical Society)

6.3.2 *Nanomaterial Hybridized Transparent Conducting Nanotube Network Films*

The electrical and optical properties of carbon-based TCEs can be further enhanced by doping nanomaterials. A simple method to decrease the electrical resistivity of SWCNT thin films while maintaining their optical transmittance was introduced by Kong et al. [87]. The electrical conductivity of SWCNT network films was increased two times (up to 2.0×10^5 S m^{-1}) with a transmittance of 80% after combining with Au ions through electroless reduction process. This enhancement was attributed to the doping effect resulting in an electron depletion mechanism. CdSe nanoparticles (diameter = 3.5 nm) assembled on SWCNTs with pyrene assistant were reported by Gruner et al. [88]. The CdSe nanoparticles on the nanohybrid film could generate a photocurrent under visible light and can transfer the charges to SWCNTs. This result demonstrated that CdSe/SWCNT nanohybrid material can be a promising building block for light-harvesting arrays or other applications on optoelectronic devices. An AgNW/CNT nanohybrid composite was reported as a stretchable conductor (>460%) with high transmittance and flexibility by Lee et al. [89]. In this nanohybrid material, good mechanical reliability (>10,000 times) and high optical transparency (80–93%) were attributed to CNTs with a diameter of around 1.2 nm, while low

electrical resistivity (24 ∼ 27 Ω/sq) was attributed to AgNW backbone with a diameter of around 150 nm.

6.4 Synthesis, Fabrication, and Physical Properties of Metallic Nanowire Networks (MNW)

6.4.1 Silver Nanowires

As mentioned in previous section, ITO is the most commonly used TCE in many fields. However, several disadvantages of ITO limit its applications for future optoelectronics. However, high cost of sputtered ITO thin films limits its applications in roll-to-roll processed photovoltaics and large-scale organic light-emitting diodes (LEDs). ITO films are not flexible owing to its brittleness which results in film cracking after bending. The processing temperature of ITO is high which leads to high cost of its production. In order to solve these issues, different materials have been developed to replace ITO. Metallic nanowires are possible candidates as transparent conductive electrode.

Jung-Yong Lee et al. [90] proposed Ag nanowires as potential material to replace the ITO and showed that the transmittance and sheet resistance of subwavelength periodic metal gratings were better than those of ITO by electromagnetic modeling. Silver nitrate was reduced by poly(vinyl pyrrolidone) (PVP) in ethylene glycol in order to prepare Ag nanowires. The diameter of these as-prepared Ag nanowires was around 103 nm with a length of around 8.7 μm as shown in Fig. 6.13. The resulting Ag nanowire solution was dropped on glass substrate for the measurements of optoelectronic properties. The sheet resistance was decreased by annealing at 180 °C due to the removal of the PVP layer. This Ag nanowire electrode exhibited

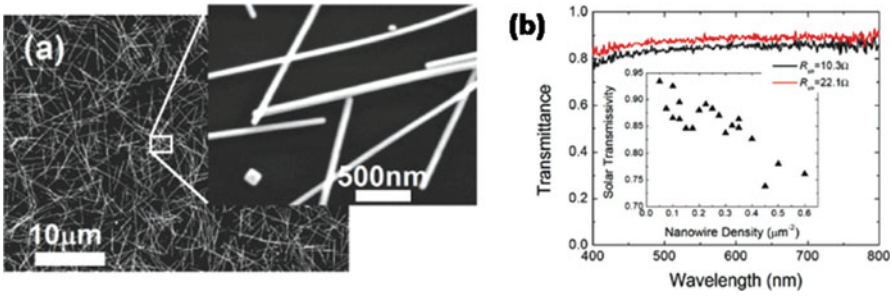

Fig. 6.13 (**a**) SEM images of an Ag nanowire mesh on a silicon substrates. (**b**) Diffuse optical transmittance for two Ag nanowire meshes with $R_{sh} = 10.3$ Ω/sq (black line) and $R_{sh} = 22.1$ Ω/sq (red line). The solar photon flux-weighted transmissivity of these two films is $T_{Solar} = 84.7\%$ and $T_{Solar} = 88.3\%$, respectively. Inset: solar photon flux-weighted transmissivity as a function of Ag nanowire mesh aerial density (triangles). (Reprinted from Ref. [90], Copyright 2008, with permission from American Chemical Society)

a sheet resistance of 16 Ω/sq with a transmittance of 86%. The performance of as-prepared Ag nanowire mesh electrodes is better than that of commonly used metal oxides. Furthermore, these Ag TCEs are prepared totally by solution process with low-temperature annealing process which is compatible with most flexible plastic substrates. These Ag nanowires could be utilized as TCE in organic solar cells and could generate a 19% higher photocurrent than the one with ITO electrode.

Several researches involving Ag nanowires as TCEs using similar synthesis techniques were investigated. Sukanta Daaqqe et al. [91] investigated and optimized the conductivity and transmittance by controlling the thickness and density of Ag nanowire films. The sheet resistance and transmittance were optimized to be 13 Ω/sq and 85% with film thickness of ~107 nm. Besides, the Ag nanowires were deposited on flexible substrate, and more than 2000 bending cycles were tested, and the result showed only <2% of resistance decreased. Bergin et al. [92] discussed the effect of length and diameter of Ag nanowires on the electrical and optical properties. The diameter and length of Ag nanowires could be optimized by varying the reaction temperature owing to the temperature-dependent reducing power of ethylene glycol. The effect of nanowire density and length on the sheet resistance of the Ag nanowire network was investigated in this study by percolation theory relations. The conductivity exponent of Ag nanowire network was determined as 1.33, which is the first experimentally calculated conductivity exponent for a 2-D nanowire network with values similar with the prediction obtained from the theory. In general, the lengths of Ag nanowires are restricted to be smaller than 20 mm. Lee et al. [93] reported a successive multistep growth (SMG) technique for the growth of long Ag nanowires. In the first step of Ag nanowires preparation, copper-additive solution, PVP solution, and $AgNO_3$ solution were added sequentially to ethylene glycol in an oil bath at 151.5 °C. Then the resulting solution was concentrated and preheated up to 95 °C in an oven before injection. This additional process was utilized to decrease the temperature difference between ethylene glycol and Ag nanowires solution, which might lead to inhomogeneous solution mixing. Then the reactants and preheated Ag nanowires were mixed and injected into ethylene glycol. Longer Ag nanowires were obtained by repeating this process 5–7 times, and high optical transmittance could be achieved up to 96% with a sheet resistivity of 9 Ω/sq.

As mentioned above, the Ag nanowire-based TCEs were fabricated by simple drop casting. The major drawback of this method was its high sheet resistance on wire-to-wire junction due to the presence of PVP. High temperature of 200 °C is needed to remove PVP, but this may damage some commonly used flexible substrates, for instance, polyethylene terephthalate (PET) and polycarbonate (PC). Hu et al. [94] synthesized a thinner and longer Ag nanowire in order to reduce the wire-to-wire junction resistance. Hu et al. modified the process by adding KBr reagent and the competition between Br^- and ethylene glycol for Ag^+ resulting in more effective anisotropic growth of the nanowires as shown in Fig. 6.14. With this additive, less junction numbers and lower annealing temperature could be achieved, which could improve the resistivity while keeping the high transmittance. The results showed that the junction resistance was decreased significantly from more than 1 GΩ to 450 Ω.

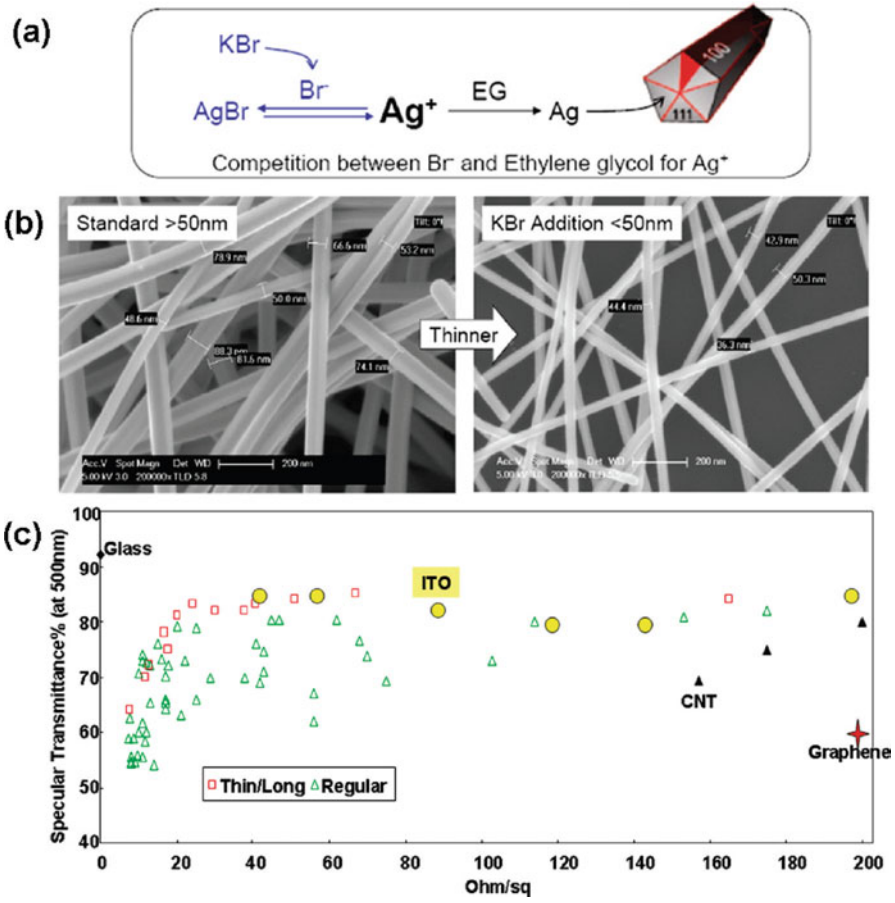

Fig. 6.14 (**a**) Schematic to show that the competition between Br- and ethylene glycol for Ag^+ retards the supply of Ag atoms and results in more effective anisotropic growth of the nanowires. (**b**) SEM confirms that the addition of KBr helps grow longer and thinner wires, from 50–100 nm to 30–50 nm. (**c**) Transmittance at 500 nm and sheet resistances for Ag NW electrodes based on regular NWs and thin/long wires with KBr addition in the NW preparation step. The performance of ITO, CNT, and graphene is shown for comparison. (Reprinted from Ref. [94], Copyright 2010, with permission from American Chemical Society)

Kim et al. [95] reported a Ag nanowire network with a modified synthesis by adding KBr and replacing the AgCl with NaCl seed as shown in Fig. 6.15. The results indicated a significant enhancement of length distributions of the Ag nanowires in the average length from 4.8 (original protocol) to 13.5 μm (modified protocol). After the synthesis of Ag nanowires, the resulting solution was electrostatically sprayed on a PC substrate, and then the substrate was annealed at 120 °C for 8 h in order to remove PVP. This Ag nanowire network showed an optical transmittance of 92.1% at a wavelength of 550 nm and a sheet resistance of 20 Ω/.

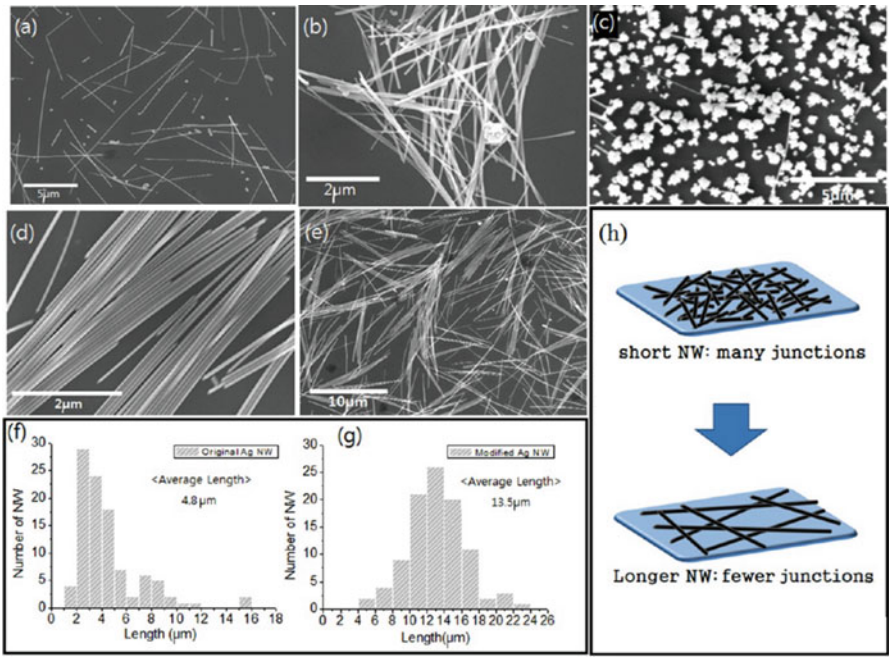

Fig. 6.15 SEM images of the Ag nanowires synthesized using (**a**) the original polyol reduction method, (**b**) with the addition of KBr, (**c**) with the addition of KBr as well as by replacing AgCl with NaCl (titrated), (**d** and **e**) and with the addition of KBr and replacement of AgCl with NaCl (no titration). Ag nanowire distribution as determined from 6000 μm^2 for (**f**) original method, (**g**) with KBr and NaCl (no titration); (**h**) schematic for longer and thinner wires resulting in minimum number of junctions. (Reprinted from Ref. [95], Copyright 2013, with permission from American Chemical Society)

Many studies have been reported to create Ag nanowire TCEs and to reduce the wire-to-wire junctions in order to increase the electric conductivity, such as coating another metal on the Ag networks [90], annealing the Ag nanowire networks at high temperatures [96], and welding the Ag nanowires by providing mechanical stress [97]. These thermal or mechanical assistants require long processing time, and they might be incompatible with some substrates [98]. A monochromatic direct-write pulsed laser technique was reported by Spechler et al. [98] in order to improve the wire-to-wire contact of Ag nanowire networks by optical welding as shown in Fig. 6.16. This Ag nanowire network electrodes exhibited low surface resistances in a range of 3–6 Ω/sq with optical transmittance of 55–70%.

Ag nanowire TCEs demonstrated excellent performance on optical transmittance and sheet resistance. However, their long-term stability still needed to be improved. Polymer additives could improve the long-term stability as reported in literature [99]. Ag nanowires were deposited on transparent cross-linked polymer substrates (polyacrylate) as reported by Yu et al. [100]. Low sheet resistance and high transparency can be achieved by these Ag nanowire/polyacrylate electrodes as compared

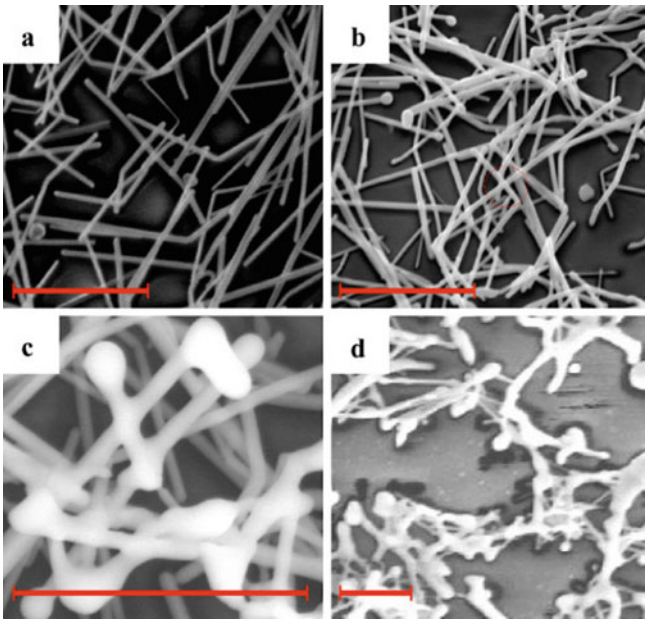

Fig. 6.16 SEM micrographs, all scale bars represent two microns: (**a**) unprocessed nanowires, (**b**) laser processed nanowires showing fusion (circled) and balling of silver at the ends of wires, (**c**) close-up of fused wires, (**d**) overprocessing with the laser leads to degradation of electrodes. (Reprinted from Ref. [98], Copyright 2012, with permission from Springer Nature)

to flexible ITO/PET electrodes. A smooth surface of Ag nanowire/polymer electrodes could be observed with a roughness lower than 5 nm. A 16% compressive strain was applied on this Ag nanowire/polyacrylate electrode, and the change of sheet resistance after bending could be ignored. This demonstrated that Ag nanowire/polyacrylate composite can be applied in polymer light-emitting diodes.

Whitney Gaynor et al. [101] prepared another Ag nanowire/polymer composite transparent electrode. The author claimed that high surface roughness of electrode may reduce the efficiency of organic photovoltaic (OPV) cells. Ag nanowire was drop casted on the glass and then was laminated with poly(4,3-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) by spin coating. The optical transmittance in the range of 350–800 nm and sheet resistance of PEDOT:PSS/Ag nanowire composite on glass were 86% and 12 Ω/sq, respectively. These results are comparable with ITO on glass which has an average transmittance of 90% with a sheet resistance of 20 Ω/sq. The PEDOT:PSS/Ag nanowires were applied in OPV cells. The power conversion efficiency of OPV cells with PEDOT:PSS/Ag nanowire electrode on glass substrate (4.2%) was almost the same as the one with ITO electrode on glass (4.2%) and was much better than the one with Ag nanowire electrode on glass substrate (0.3%). Furthermore, the power conversion efficiency

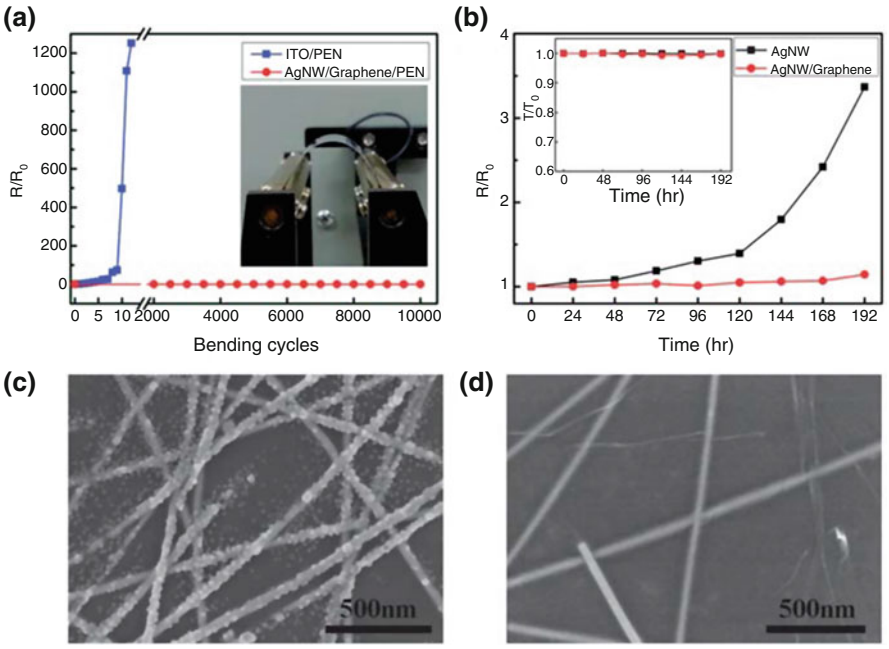

Fig. 6.17 (**a**) The mechanical flexibility test of ITO–PEN and AgNW–graphene–PEN TCEs. (**b**) Sheet resistance change of AgNW and AgNW–graphene hybrid TCEs during the long-term stability test at 70 °C and 70% RH for 8 days. The inset shows the optical transmittance change during the long-term stability test. SEM images of (**c**) AgNW and (**d**) AgNW–graphene hybrid TCEs after the long-term stability test. (Reprinted from Ref. [99], Copyright 2013, with permission from Royal Society of Chemistry)

was 3.8% with PEDOT:PSS/Ag nanowire electrode on plastic substrate, which was better than ITO electrode (plastic substrate, 3.4%). However, high amount of polymer in the Ag nanowire/polymer composite may result in the loss of conductivity.

A Ag nanowire–graphene hybrid TCE was synthesized by dry-transferring a CVD-grown monolayer graphene onto a Ag nanowire TCE as reported by Lee et al. [99]. The Ag nanowire–graphene hybrid TCE exhibited high transmittance up to 92.8% with a sheet resistance of ~34.4 Ω/sq. This hybrid TCE also presented high mechanical stability and flexibility more than 10,000 wrapping cycles without change of sheet resistance. The thermal stability of Ag nanowire and Ag nanowire–graphene hybrid TCE was also tested under high-temperature (70 °C) and high-humidity (70% relative humidity) conditions for 8 days as shown in Fig. 6.17, and the optical transmittances for both TCEs were maintained without change. The sheet resistance of Ag nanowire–graphene hybrid TCE remained unchanged, but the sheet resistance of Ag nanowire TCE increased to around 300% after 8 days. Therefore, this result suggests that the thermal stability of Ag nanowire can be enhanced by combing with graphene layer.

6.4.2 Copper Nanowires

Ag nanowires have demonstrated a great potential as transparent conductive electrodes because their optical transmittance and resistance are comparable with ITO electrodes and the performance of Ag nanowires on flexible substrates is better than ITO film due to the brittleness of ITO film. However, the price of Ag is similar with ITO film ($500 per kg) [102]. Therefore, other low-cost metallic nanowires such as copper were developed as possible transparent conductive electrodes.

The earth abundance of Cu is around 1000 times than In and Ag, and its cost is roughly 100 times cheaper than In and Ag [103]. Furthermore, the bulk resistivity of Cu is in the same order with Ag. Rathmell et al. [102] investigated the growth mechanism of Cu nanowires as well as their optoelectronic properties as transparent conducting films. Gram-scale Cu nanowires were prepared via a solution process which reduced $Cu(NO_3)_2$ by hydrazine in an NaOH solution with ethylenediamine (EDA). The electron diffraction pattern (SAED) indicated that nanowires consisted of a single-crystalline domain. The diameter and the length of Cu nanowires were 90 ± 10 nm and 10 ± 3 μm, respectively. Same with Ag nanowires, the increase of nanowire density leads to lower resistance and transmittance. The transmittance was ~25% lower than ITO film and ~20% lower than Ag nanowire, but 15% higher than CNT film at same sheet resistance, indicating that Cu nanowire TCE is a potential candidate for low-cost devices.

Cu nanowires synthesized from aqueous media might be difficult to be well-dispersed and could also generate plenty of Cu particles that deteriorate the optoelectronic performance significantly [104]. Ultralong single-crystalline Cu nanowires were synthesized in a nonaqueous system which exhibited superior dispersibility as reported by Zhang et al. [104]. Cu nanowires grew self-catalytically in a liquid-crystalline medium which consist of hexadecylamine (HAD) and cetyltriamoninum bromide (CTAB). Copper acetylacetonate was added to HAD/CTAB mixture in order to grow Cu ultralong nanowires with good dispersibility. The Cu nanowires grew spontaneously owing to the presence of a catalytic Pt surface. The length of Cu nanowires was up to a few millimeters with the diameter of around 78 nm. This ultralong Cu nanowire TCE displayed a sheet resistance of around 35 Ω/sq with a transmittance of 85%. However, the stability of Cu nanowires was poor due to the oxidation of Cu nanowires which leads to increased sheet resistance (100 Ω/sq), and it is a critical issue for practical applications. In order to eliminate the influence on the sheet resistance caused by the oxidation of Cu nanowires, passive layers such as AZO/Al_2O_3 were utilized to prevent the oxidation of electrospun Cu nanofibers as shown in Fig. 6.18 [105]. The resistance of AZO-coated Cu nanofibers only increased 10% after oxidizing at 160 °C in dry air and 80 °C in humid air with 80% relative humidity, while Cu nanofibers without AZO coating become insulating. Furthermore, the oxidation and corrosion stability of Cu nanofibers with acidic PEDOT:PSS layer

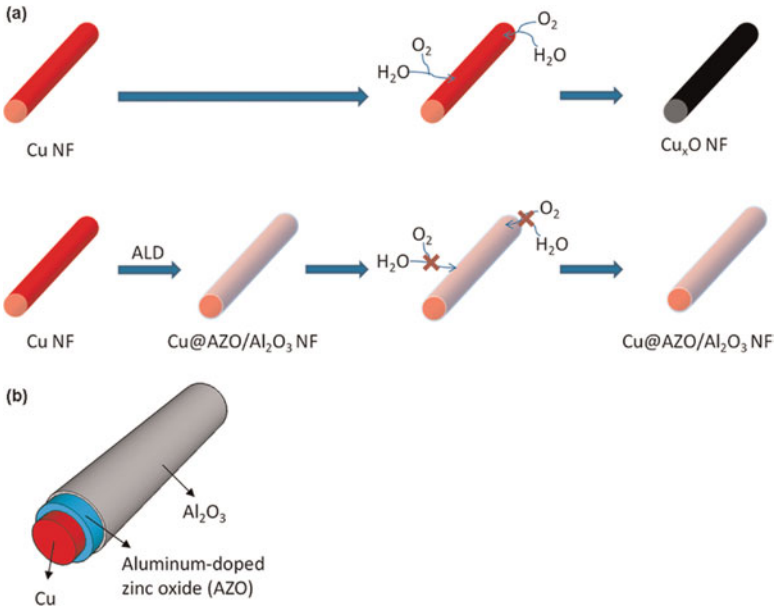

Fig. 6.18 (**a**) Schematic of AZO-coated copper nanofiber preparation and comparison with bare Cu nanofiber in terms of oxidation resistance. Because of the passivation of the AZO/Al_2O_3 layer, the core Cu nanofiber is not subjected to oxidation and therefore can maintain its high conductivity. (**b**) Cartoon (not to scale) of the Cu@AZO/Al_2O_3 nanofiber. (Reprinted from Ref. [105], Copyright 2012, with permission from American Chemical Society)

were improved dramatically after AZO coating with only 18% increase of sheet resistance, whereas bare Cu nanofibers had 6 orders of magnitude increased sheet resistance.

The root cause of the poor stability of Cu wires was reported [106] to be the junction resistance which induces the oxidation process. Kiruthika et al. [107] developed a method of producing copper TCE with seamless junctions. The Cu nanowire network was prepared by electroplating or by electrolessly coating Cu on a disposable template. This Cu TCEs provided high transmittance up to 75% with low sheet resistance of <5 Ω/sq. A higher transmittance of ~90% was obtained with a sheet resistance of 141 Ω/sq. Large-scale Cu nanowire TCEs have also been prepared using the proposed synthesis process. Moreover, the Cu nanowire networks are greatly interconnected in a single plane without wire-to-wire junctions, resulting in excellent stability as regards the oxidation in air, even at high temperature. The resistant increased one order after 31 hours at 130 °C and increased 2% after 4 months at room temperature. The Cu nanowire TCEs deposited on PET substrate also exhibited high flexibility and without significant change in resistance after 1000 bending cycles.

6.5 Applications

6.5.1 Photovoltaics

Transparent conductive films have been frequently reported for the application in photovoltaics (solar cells). ITO nanowires have been extensively used as electrode in photovoltaics or energy storage devices. Joanni et al. [51] fabricated a dye-sensitized solar cell (DSSC) with ITO nanowire electrode. The ITO nanowires were grown via chemical vapor deposition technique, and the titanium dioxide (TiO_2) nanoparticles were then coated on ITO nanowires by RF sputtering. The dye and platinum were coated to assemble the cells. This 3-D architecture can reduce the probability of electron-hole recombination by shortening the length of electronic transport.

ITO electrode has difficulty for flexible device applications due to its brittle nature; thus metallic nanowires have been developed to replace ITO in the applications such as organic photovoltaic devices. Rowell et al. [10] reported an organic solar cell with a P3HT/PCBM active layer and a SWCNT electrode. The scheme and current-voltage curves of this organic solar cell are shown in Fig. 6.19. The short-circuit current (J_{sc}), open circuit (V_{oc}), fill factor (FF), and power conversion efficiency (PCE) were measured and calculated to be 7.8 mA/cm^2, 0.605 V, 52%, and 2.5%, respectively. Although the performance of the organic solar cell with SWCNT electrode was not as good as the one using ITO electrode, the PCE remained unchanged after a series of bending test, indicating the excellent flexibility

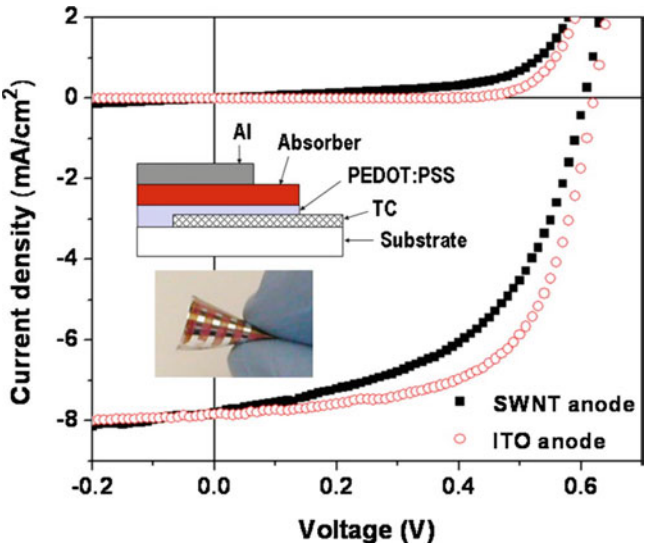

Fig. 6.19 The scheme and current density-voltage characteristics of P3HT/PCBM devices under AM1.5G conditions using ITO on glass (open circles) and flexible SWNTs on PET (solid squares) as the anodes, respectively. (Reprinted from Ref. [10], Copyright 2006, with permission from AIP Publishing LLC)

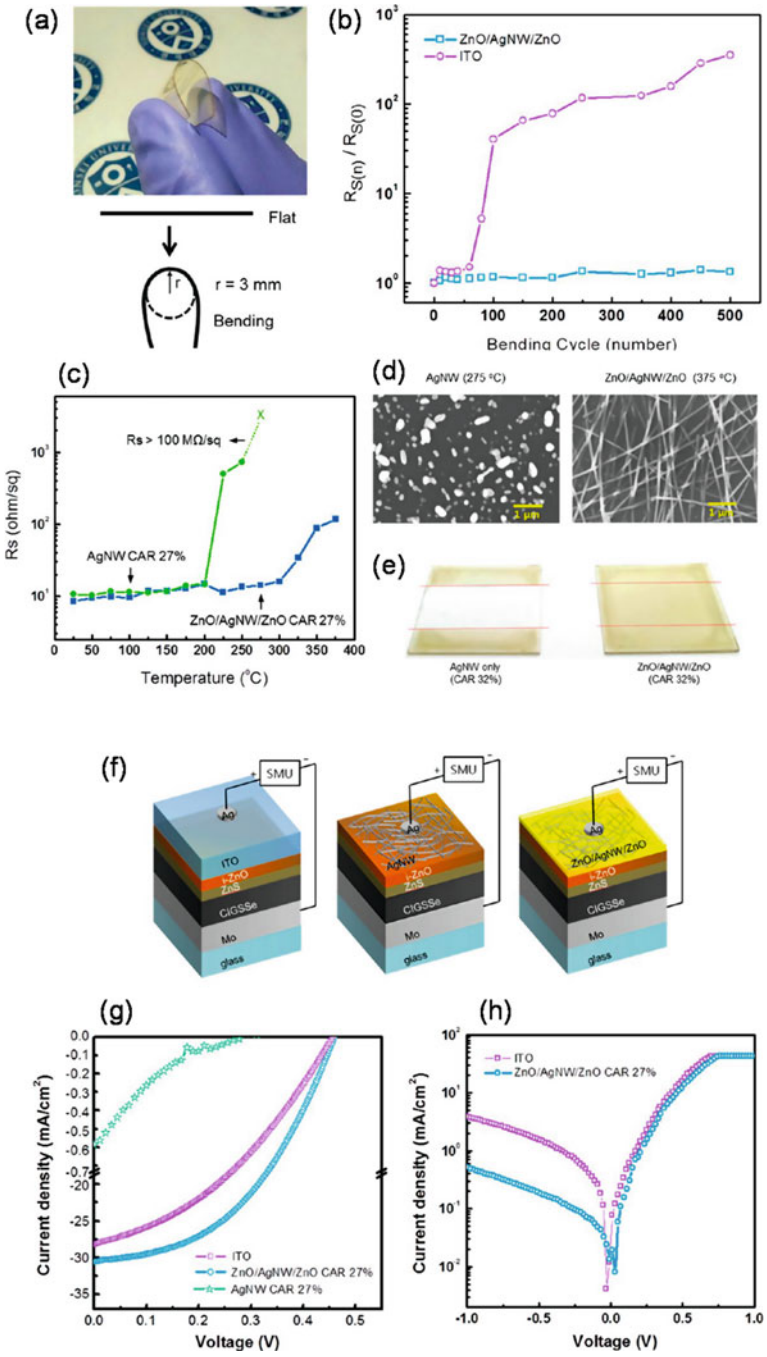

Fig. 6.20 (**a**) Photograph of a flexible and transparent ZnO/Ag nanowire/ZnO composite electrode on a flexible polymer substrate (top) and schematics showing the mechanical bend test conditions (bottom). (**b**) Changes of the normalized resistance during the bend test for the sputtered ITO single

of SWCNT electrode. Another organic solar cell using Cu nanowire as electrode on flexible substrate was reported by Kang et al. [108]. The PCE of the solar cell with Cu electrode was measured to be 2.1%, which is similar with the one with ITO electrode (2.24%). Both solar cells exhibited similar V_{oc} (0.6 V) and FF (62%), while the J_{sc} of the solar cell with Cu electrode was 5.7 mA/cm^2 and the one with ITO electrode was 5.9 mA/cm^2, respectively. This indicates that the lower J_{sc} of the device with Cu electrode might owe to its lower optical transmittance. Yang et al. [109] fabricated a flexible solar cell on PET substrate using Ag nanowire network. The PCE of this flexible solar cell retained 2.3% after ten bending cycles with a large deformation of 120°.

Although Ag nanowires are able to be fabricated on flexible substrates and showed minor effect on PCE after bending cycles, the sheet resistance of Ag nanowire might increase under long-term exposure of harsh environment. In order to enhance the stability of solar cells with Ag nanowire TCE, Kim et al. [110] reported a ZnO/Ag nanowire/ZnO layer structure to overcome this issue. As shown in Fig. 6.20a, b, the mechanical bend test of this ZnO/Ag nanowire/ZnO composite electrode on a flexible polymer substrate is in comparison with ITO electrode. In the bending test, the sheet resistance of ITO film was increased ~2 orders after 100 cycles, while the proposed ZnO/Ag nanowire/ZnO electrode showed negligible changes after ~500 bending cycles. Besides, ZnO/Ag nanowire/ZnO electrode also demonstrated better thermal stability than Ag nanowire electrode as displayed in Fig. 6.20c, d. The sheet resistance of Ag nanowire electrode increased ~100 times after being heated above 200 °C, while less than 10% change in sheet resistance for ZnO/Ag nanowire/ZnO after being heated up to 300 °C. The proposed ZnO/Ag nanowire/ZnO electrode was assembled in a solar cell, and then its device performance was compared with the solar cells which utilized ITO and Ag nanowire TCEs. As shown in Fig. 6.20e, g, Cu(In,Ga)(S,Se)$_2$ (CIGSSe) thin film solar cell using ZnO/Ag nanowire/ZnO electrode with a covered area ratio of 27% exhibited a J_{sc} of 31.0 mA/cm^2, a V_{oc} of 0.458 V, a FF of 45%, and a calculated PCE of 6.37%, which were better than the solar cell with ITO electrode (J_{sc}, 28.5 mA/cm^2; V_{oc}, 0.432 V; FF, 43.2%; PCE, 5.32%) and bare Ag nanowire electrode with a covered area ratio of 27% (J_{sc}, 0.54 mA/cm^2; V_{oc},0.280 V; FF, 15.4%; PCE, 0.029%).

Fig. 6.20 (continued) layer and the ZnO/Ag nanowire/ZnO composite layer on polymer substrates. (**c**) Variations of the resistances of the Ag nanowire single film (covered area ratio = 27%) and the ZnO/Ag nanowire/ZnO composite film (covered area ratio = 27%) on glass substrates as a function of the annealing temperature. (**d**) SEM images and photographs of a Ag nanowires single film and a ZnO/Ag nanowire/ZnO film. (**e**) Photographs of the AgNW single film (left) and ZnO/AgNW/ZnO film (right) on glass substrates after the adhesion test. Scotch tape was firmly attached on the electrode surfaces, followed by rapid detachment. (**f**) Schematic structures of CIGSSe thin film solar cells using different transparent conductors. (**g**) Current density-voltage characteristics for the thin film solar cells based on the various top electrodes. (**h**) Current density-voltage characteristics measured in the dark. (Reprinted from Ref. [110], Copyright 2013, with permission from American Chemical Society)

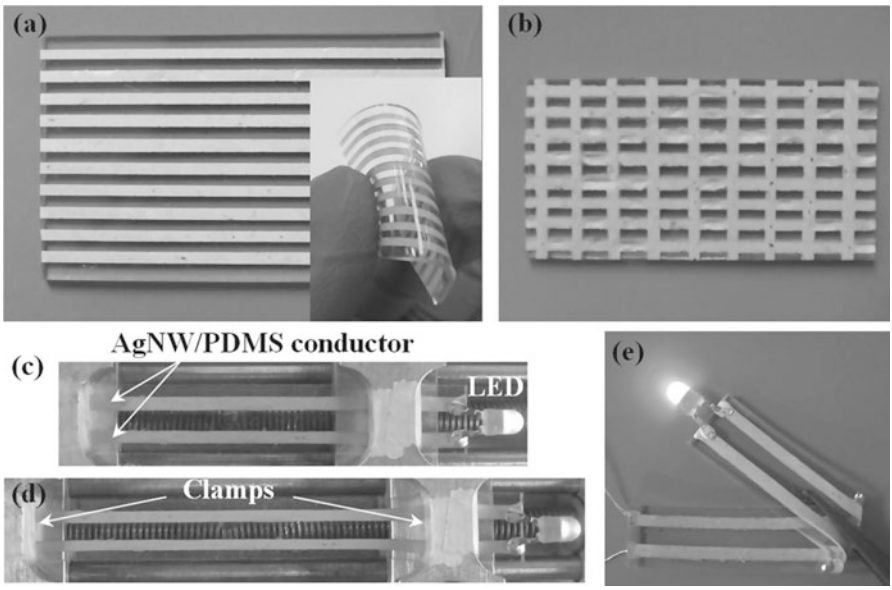

Fig. 6.21 (**a**) Patterned parallel Ag nanowire/PDMS stretchable conductors with linewidth of 800 μ m. The inset shows the conductors deformed by hand. (**b**) Crossed patterns of Ag nanowire/PDMS stretchable conductors. (**c** and **d**) Optical photograph of the LED integrated circuit under tensile strain of 0% and 50%. The two Ag nanowire/PDMS elastic conductors are clamped on a mechanical testing stage. The other ends of the Ag nanowire/PDMS lines were connected to a 1.7 V battery. (**e**) Optical photograph of the LED integrated circuit under folding. (Reprinted from Ref. [111], Copyright 2012, with permission from John Wiley and Sons)

6.5.2 Light-Emitting Devices

O'Dwyer et al. [2] used ITO nanowire as fully transparent (in the region of visible to near-infrared) top contacts for light-emitting devices (LEDs). The forward-bias turn-on voltage of 0.55 V at an injection current of 10 mA was obtained from the LEDs with ITO nanowire contact layer, indicating a significant improvement over LEDs.

Xu et al. [111] utilized Ag nanowire-based stretchable conductors in a stretchable LED circuit and a capacitive strain sensor owing to its flexibility, and the devices fabricated as proof of concept are shown in Fig. 6.21. This Ag nanowire conductor can be bent by hand without significant resistance loss as shown in the inset of Fig. 6.21a, and crossed patterns could also be fabricated as shown in Fig. 6.21b. A simple circuit was designed to lighten a LED with two patterned Ag nanowire/PDMS lines as shown in Fig. 6.21c. After stretching the Ag nanowire/PDMS conductors to a strain of 50% and folded, this LED device kept lightening without the illumination intensity change.

Another highly stretchable polymer LED (PLED) device with Ag nanowire/graphene network as TCE was developed by Liang et al. [112]. The device was

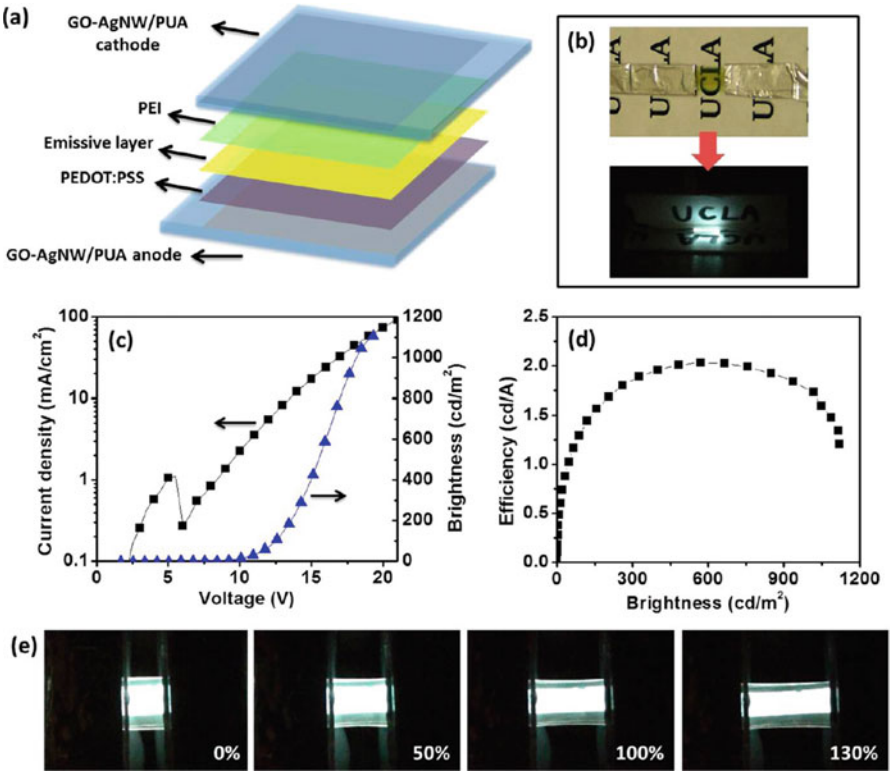

Fig. 6.22 (**a**) Schematic drawing of a fully stretchable PLED using GO-AgNW/PUA composite electrode as both anode and cathode. (**b**) Optical photographs of a semitransparent unlit stretchable PLED (top) and a stretchable PLED operated at 13 V emitting white light from two sides and illuminating two white papers with printed ULCA logo in black (bottom). (**c**) Current density-luminance-driving voltage characteristics and (**d**) current efficiency-brightness characteristics of the PLED device. (**e**) Optical photographs of a PLED (original lighting area, 3 mm x 4 mm) being driven at 14 V and stretched to specified strains. (Reprinted from Ref. [112], Copyright 2014, with permission from American Chemical Society)

composed of a layer of polyethylenimine (PEI), emissive layer, PEDOT:PSS, and two graphene oxide–Ag nanowire/polyurethane acrylate (GO–AgNW/PUA) electrodes as shown in Fig. 6.22. The sheet resistance of the GO–AgNW/PUA electrodes was 14 Ω/sq. The electroluminescence was turned on at around 7 V, and a brightness of 1100 cd/m^2 was obtained at 21 V. At the brightness of 571 cd/m^2, a maximum current efficiency of 2.0 cd/A could be achieved. More surprisingly, after stretching the PLED with a lighting area of 3 $\times$ 4 cm^2 up to 130% linear strain, and driven at 14 V, its emission intensity was kept homogeneous over the whole lighting area as displayed in Fig. 6.22e.

6.5.3 *Smart Windows and Displays*

The requirements of TCEs utilized in smart windows are high optical transmittance, low surface roughness, and strong adhesion between film and substrate. SWCNT films are a suitable TCE candidate for electrochromic devices as reported by Hu et al. [113] as shown in Fig. 6.23. The electrochromic layer, polyaniline (PAN), was electrochemically deposited on a SWCNT film. This SWCNT film which was prepared by a printing method exhibited low roughness (~10 nm) with a sheet resistance of 150 Ω/sq and an optical transmittance of 80% at 550 nm. Figure 6.23a–e showed SWCNT films on PET substrate, and after polyaniline deposition, the color could be tuned by applying different potential to the device. Figure 6.23f revealed that the transmittance of this electrochromic device was voltage dependent, and the transmittance was 50% at 550 nm under −0.2 V and 35% at 500 nm under 0.8 V, which was in agreement with the color change. The highest electrochromic contrast with a transmittance change of $\Delta T = 25\%$ was detected at 625 nm. Those results demonstrated that SWCNT film is a promising candidate for the application of electrochromic windows.

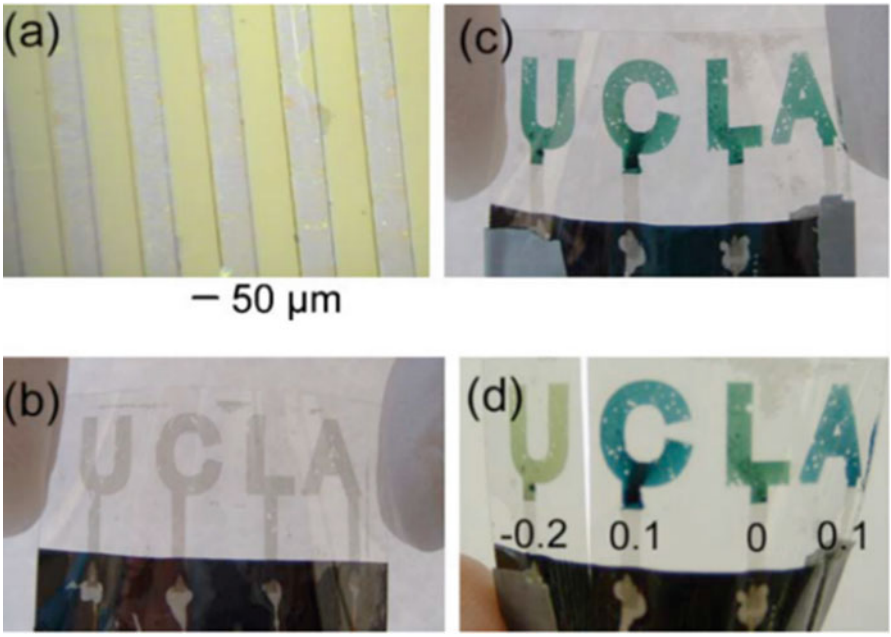

Fig. 6.23 (**a**) Patterned nanotube film lines on PET substrates. (**b**) Patterned SWCNT films on PET, where the horizontal length of each letter is approximately 1 cm. (**c**) The films after a 5 min polyaniline deposition. (**d**) The photo for the top half cell taken immediately after being removed from the device, where each letter is under a different voltage. Films shown in (**c**) and (**d**) were bent to demonstrate the flexibility. (Reprinted from Ref. [113], Copyright 2007, with permission from AIP Publishing LLC)

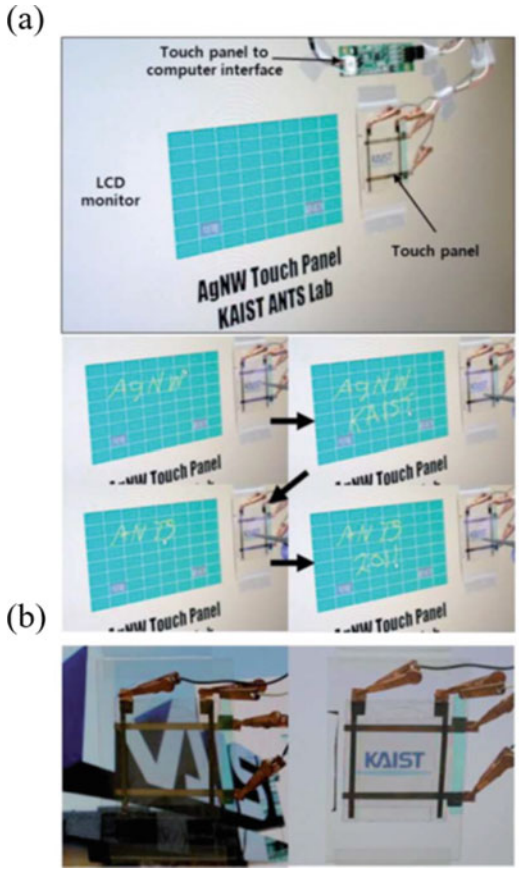

Fig. 6.24 (**a**) Demonstration of applying a very long Ag nanowire transparent conductor for a touch panel. It was connected to a computer with control software. (**b**) Transparency of the touch panel using a Ag nanowire network transparent conductor on the commercial LCD monitor. (Reprinted from Ref. [93], Copyright 2012, with permission from Royal Society of Chemistry)

Lee et al. [93] fabricated a highly transparent touch panel device using very long Ag nanowires with high optical transmittance (up to 96%) and good conductivity (up to 9 Ω/sq) as presented in Fig. 6.24. This touch panel is comprised of a transparent Ag nanowire network electrode and an ITO electrode on a PET substrate with spacers between these two electrodes. The author successfully demonstrated the touch function of the panel with Ag nanowires, and the device showed good transparency on the LCD monitor with good performance as shown in Fig. 6.24b.

6.5.4 Transparent Film Heaters

Transparent heaters are resistance devices which function as surface heating source by injecting an electric current through a transparent conductive film. Important

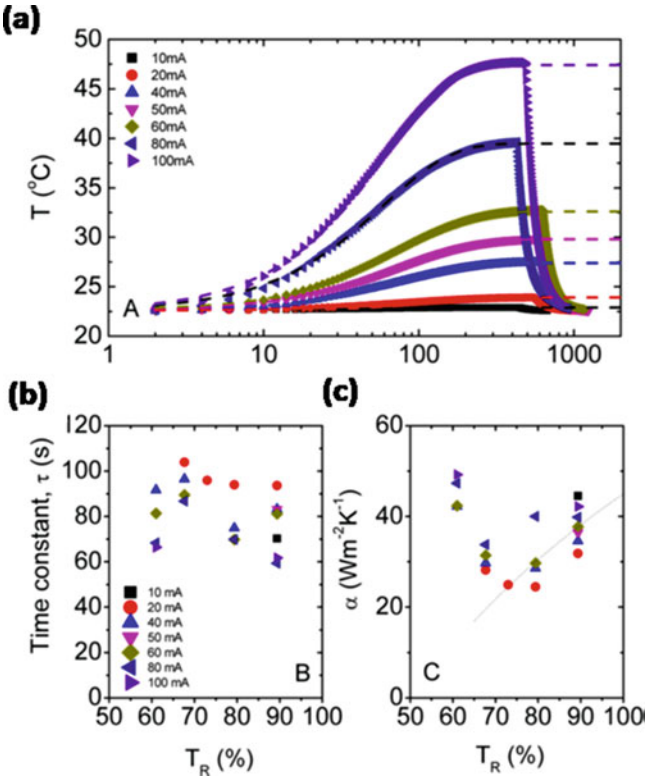

Fig. 6.25 (**a**) Time dependence of temperature rise for an Ag nanowire network (TR = 61%) with a number of different applied currents. (**b**) Time constant τ and (**c**) heat transfer constant, α, for Ag nanowire networks as a function of network transmittance. In each case, data are shown for a range of applied currents. (Reprinted from Ref. [31], Copyright 2014, with permission from American Chemical Society)

parameters for a transparent heater include thermal response time, steady heating temperature, and cycling stability. ITO film is a commercially available transparent heater, which also suffers from high cost and low flexibility. Therefore, other transparent films such as SWCNT and Ag nanowire have been developed owing to their good flexibility. A transparent heater with SWCNT electrode was reported by Yoon et al. [114]. The defroster ability of SWCNT film with 1190 Ω/sq sheet resistance and 91.3% transmittance was tested. A power of 0.12 W was applied on the SWCNT heater for 1 min and showed that almost all the frost on the surface was removed, indicating its potential application in vehicle window defrosters. Sorel et al. [31] prepared a transparent heater with a Ag nanowires network. Figure 6.25 represented a Ag nanowire network with transmittance of 61% at various applied currents. Overall, the temperature increased only with time before ultimately saturating.

6.5.5 *Other Applications*

The usage of transparent conductive nanowires in chemical sensors has been frequently reported because of their good conductivity and high aspect ratio. Wan et al. [115] developed an ethanol sensor with SnO_2 nanowires which were prepared by a second Au-catalyzed VLS growth process. The sensitivity (the ratio of the sensor resistances in air and exposed to the target ethanol vapor) was estimated to be 2.3 for 0.5 ppm ethanol (response time ~4 s) and 50.6 for 100 ppm ethanol (response time 2 s), respectively. Kurowska et al. [116] presented a sensitive and rapid hydrogen peroxide sensor with Ag nanowire array electrode. The results showed linear range for the determination of hydrogen peroxide with the highest sensitivity of 0.0266 μA cm^{-2} μM^{-1} from 0.1 mM to 3.1 mM, and the detection limit was 29.2 μM. The Ag nanowire array sensor possessed high stability that the sensitivity change of this sensor was negligible after storing for 42 days. In addition to chemical sensors, Ag nanowires have been also developed as strain sensors [117]. Mechanical deformations can be detected by strain sensor through the change of electrical resistance or capacitance. The key requirements of strain sensors include high conductivity, high stretchability, and fast response time. Amjadi et al. [117] reported a sandwich-structured Ag nanowire-polydimethylsiloxane (PDMS) nanocomposite strain sensors as shown in Fig. 6.26 where the Ag nanowires were patterned on a polydimethylsiloxane (PDMS) matrix. The stretchability of this Ag nanowire-PDMS strain sensor was 70% which was better than conventional strain sensors, and the response time was about ~200 ms showing a rapid response.

6.6 Summary

ITO is the most commonly used transparent conductive film nowadays; other materials such as metallic nanowire and carbon nanotubes were also developed, attempting to replace ITO. In comparison with ITO, carbon nanotube electrodes are cost-effective and could be fabricated on highly flexible electrode. However, the optical transmittance and sheet resistance of carbon nanotubes need to be further

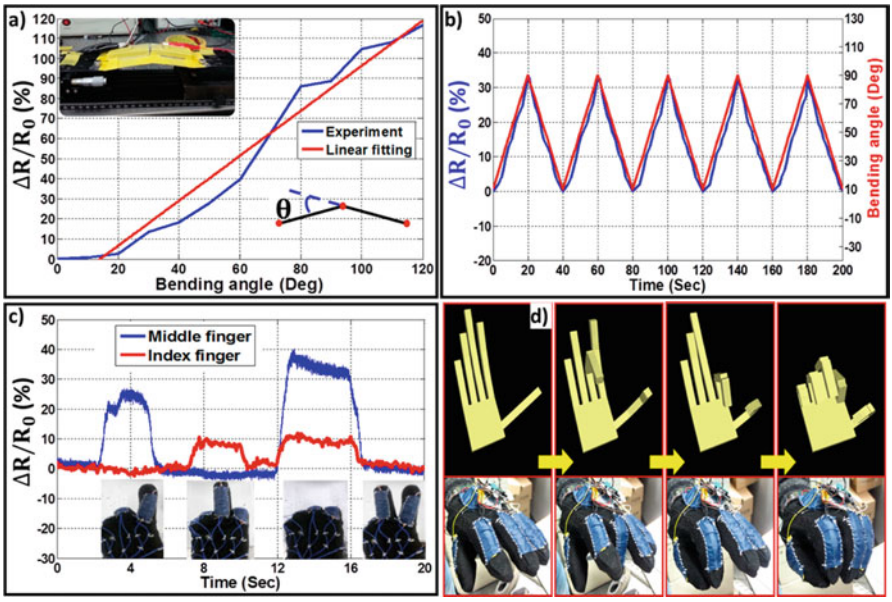

Fig. 6.26 Human motion detection by the sandwich-structured Ag nanowire-PDMS nanocomposite strain sensors: (**a**) response of the sandwich-structured strain sensor to the bending angles from 0° to 120° (inset, photograph of the artificial finger); (**b**) response of the strain sensor under repeated bending/relaxation cycles (10°–90°); (**c**) motion detection of index and middle fingers; (**d**) control of avatar fingers in the virtual environment using wireless smart glove system. (Reprinted from Ref. [117], Copyright 2014, with permission from American Chemical Society)

improved. Metallic nanowires such as Ag nanowires demonstrate a comparable optical transmittance and sheet resistance with ITO. More importantly, Ag nanowire could be fabricated on highly flexible substrates. Nevertheless, the relatively high cost and long-term stability remain issues for Ag nanowires. Cu nanowire is a cost-effective material, but the optical transmittance and sheet resistance are not as good as ITO nor Ag nanowires. The electrical and optical characteristics of nanowire-based transparent conductive electrodes are summarized in Table 6.1.

Table 6.1 The electrical and optical characteristics of nanowire-based transparent conductive electrodes (NW, nanowire)

Material	Synthesis method	Process temperature (°C)	Thickness (nm)	*T* % at visible region	Sheet resistance (Ω/sq.	Potential application	Ref.
ITO NWs	Vapor transport	840		~80	6.4	Interconnects	[14]
ITO NWs	Molecular beam epitaxy	575	380	~90	–	LED	[2]
AZO NWs	Solution-based methods	300	–	–	10^3	–	[63]
SWCNT	–	–	50	70	30	Optical NFET	[80]
SWCNT	CVD	900–1200	54	81	20	Touch screen	[81]
SWCNT	–	–	–	70/80	40/70	Flexible display	[83]
Ag NWs	$AgNO_3$ reduction	200	–	84.7/88.3	10.3/22.1	Solar cells	[90]
Ag NWs	–	–	107	85	13	Electrode	[91]
Ag NWs	Repetitive $AgNO_3$ reduction	95	–	89/96	9/69	LED and touch panel	[93]
Ag NWs	$AgNO_3$ reduction	170	–	60–90	12–110	Flexible electronics	[94]
Ag NWs	$AgNO_3$ reduction	120	–	92.1	20	Flexible electronics	[95]
Ag NWs	–	–	–	55–70	3–6	–	[98]
Ag NWs	$AgNO_3$ reduction	170	–	82/86/91	12/30/100	Polymer LED	[100]
PEDOT:PSS/ Ag	–	180	125	86	12	Organic solar cells	[101]
Ag NW/CNT	Ag NWs: $AgNO_3$ reduction	–	–	85	29 ± 5	Supercapacitor	[89]
	SWCNT: arc-discharge method						
Ag NW/graphene	–	–	–	92–95.3	29.4–57.8	Organic solar cells	[99]

(continued)

Table 6.1 (continued)

Material	Synthesis method	Process temperature (°C)	Thickness (nm)	*T* % at visible region	Sheet resistance (Ω/sq.	Potential application	Ref.
Cu NW	$Cu(NO_3)_2$ reduction	80	–	67	61	Low-cost devices	[102]
Cu NW	$Cu(acac)_2$ reduction	–	–	85	35	Flexible devices	[104]
Cu NW	Electroplating and electroless	RT	–	65–75/95	0.3–3.8/141	Optoelectronics	[106]
MoO_3:In NWs	CVD method	450	–	70	–	All transparent devices	[77]

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Chapter 7
One-Dimensional Nanowire-Based Heterostructures for Gas Sensors

Jun Zhang and Xianghong Liu

7.1 Introduction

Gas sensors with the ability to detect gaseous species in a quantitative and qualitative manner play an important role in various aspects in our daily lives. They can function as a feasible means to monitor air quality, environmental pollution, chemical detection, control of chemical processes, food quality, and medical diagnosis and so forth.

One-dimensional (1D) nanostructures at least one dimension in the range of 1–100 nm (nanowires, nanorods, nanoribbons or nanobelts, nanofibers) have long been considered as promising building blocks for gas sensors [1–7]. The fascinating features of nanowires for gas sensing include high surface-to-volume ratio, sensitive surface, high crystallinity, high carrier mobility, low power consumption and ease for device integration [2, 6, 8, 9]. In 2001 nanowires were initially employed to fabricate gas sensors as proof-of-concept [2, 3]. Afterwards nanowires are drawing fast growing interest in the field of gas sensing with an outcome of over 1200 publications in past 15 years from the Web of Science using the keywords nanowire and gas sensor (Fig. 7.1). It is important to note that among these publications metal oxide nanowires hold a dominant position, while other nanowires including organic polymers, metals, and other semiconductors only register a small part (12.6%). It is not strange that n-type ZnO and SnO_2 nanowires are the most extensively studied materials for gas sensing because the electron mobility in ZnO and SnO_2 is very high (160 and 200 $cm^2\ V^{-1}\ s^{-1}$, respectively) with respect to that of other metal oxides such as In_2O_3, WO_3 and TiO_2 (100, 10 and 0.4 $cm^2\ V^{-1}\ s^{-1}$, respectively)

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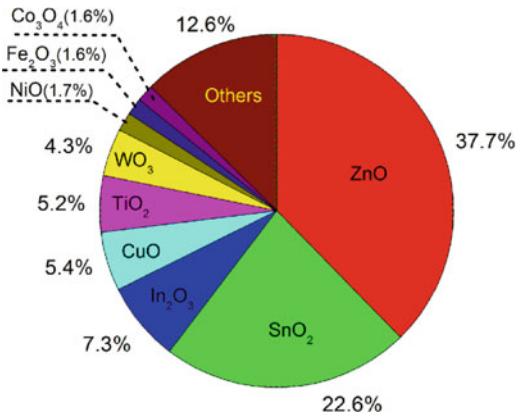

Fig. 7.1 Research on metal oxide nanowires for gas sensors. (From Web of Knowledge, July 2016)

[8]. Although p-type semiconductor metal oxides such as CuO, NiO, Co_3O_4 with low hole mobility only take part of lower than 10% for gas sensing, [10] they can function in high-performance gas sensor by forming heteronanostructures or serving as a catalyst.

1D metal oxide nanostructures were first utilized for gas sensor in 2002, when Comini et al. [11] and Yang et al. [4] demonstrated respectively that single-crystalline SnO_2 nanobelts (nanoribbons) prepared by thermal evaporation were highly sensitive to NO_2. Kolmakov et al. [12] were among the first to show SnO_2 nanowires obtained by using AAO template method exhibited highly sensitive, fast, stable, and reproducible reponses to CO. In 2003, the Zhou group [13] initially reported In_2O_3 nanowires-based field-effect transistor (FET) as a gas sensor to detect NO_2 and NH_3 with significantly improved sensing performance in comparison with the traditional thin-film based sensors. Later in 2004, Wan et al. [14] reported that ZnO nanowire sensors exhibited a very high sensitivity to ethanol and fast response time at 300 °C. Following these early works, research on nanowire sensors has been attracting more and more interest.

In order to improve the sensing properties of nanowires, significant efforts have been directed to sensitize the nanowire surface. By now typical strategies include decorating nanowire surface with secondary-phase nanoparticles, [15–22] forming core-shell structures, [23–26] and elemental doping [27–29]. Among these methods, surface functionalization of 1D nanowire with various nanoparticles (metals, oxides, semiconductors) has attracted considerable interest because of synergistic benefits induced by the coupling and the heterointerface between the host nanowires and guest nanoparticles. Such a nanowire-nanoparticle heterostructure have been shown to greatly improve the "4S" gas sensing parameters, e.g. sensitivity, selectivity, stability, speed (response-recovery time), as well as the operating temperature.

In this chapter, we will specially focus on the progress made in the past 15 years toward using the unique nanowire-nanoparticle heterostructures for achieving superior sensing performance. Since in the field of gas sensing there have been many comprehensive reviews and chapters dealing with synthesis, modification and

application of 1D nanostructure for sensors, [6–9, 30–38] we do not attempt another chapter as such here. The major goal is to identify how one can optimize the above-mentioned gas sensing characteristics through engineering nanowire-nanoparticle heterostructures and contribute to the understanding of function mechanisms for heteronanowire-based gas sensors.

7.2 Advantages of Nanowires for Application in Gas Sensing

As a typical 1D nanostructure, nanowires can offer some essential advantages over nanoparticles for gas sensing [8]. Conventional gas sensing film consists of a large quantity of nanoparticles, which have a risk of grain coarsening induced by the high working temperature. This might cause a decreased stability of the sensor device as the polycrystalline sensitive layer might be sintered due to thermal effects after a long working. This has been proved by Sysoev et al., [39] who carried out a comparative study of the long-term gas sensing performance of single crystal SnO_2 nanowires and SnO_2 nanoparticles (Fig. 7.2a, b). They showed that the device made of nanowires demonstrated excellent sensitivity and long-term stability toward traces of 2-propanol in air. Different from the nanowires, the nanoparticles exhibited a superior initial sensitivity, but the sensitivity deteriorated during the first month of operation and gradually stabilized at the level observed steadily in the nanowires. The enhanced stability of the nanowire sensors is ascribed to the reduced propensity of the nanowires to sinter under real operation conditions with respect to

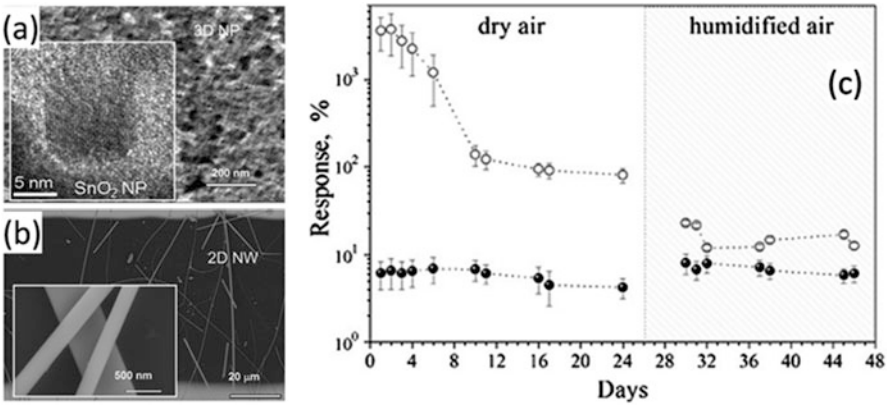

Fig. 7.2 HRTEM and SEM images of (**a**) SnO_2 nanoparticle layer and (**b**) SnO_2 nanowires, (**c**) the change of sensor baseline resistance measured with SnO_2 nanoparticles and SnO_2 nanowires versus time. Open and filled circles correspond to nanoparticles and nanowires. Experiments were initially carried out in dry air and then (since day 26) in humified air. Reproduced from ref. [39], Copyright 2009, with permission of Elsevier

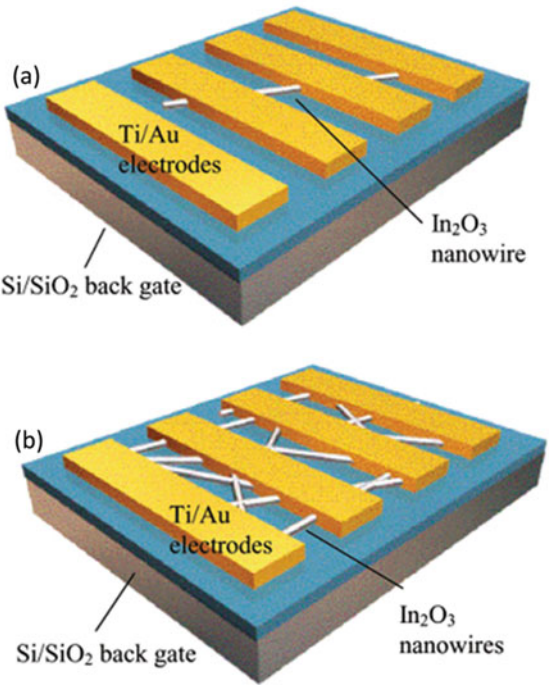

Fig. 7.3 Scheme of gas sensors based on (**a**) a single nanowire transistor and (**b**) multi-nanowires. Reproduced from ref. [40]. Copyright 2004 American Chemical Society

nanoparticles. Long-term working at elevated operating temperature facilitates sintering of nanoparticles, leading to aggregation and encapsulation of nanoparticles into larger agglomerates. This work also reveals that the humidity has very big influence on the sensor stability of nanoparticles, while nanowires possess a relative good resistance to humidity.

Another advantage of nanowires is that they can be directly employed as the sensing element in a single nanowire form (Fig. 7.3a) [40]. In a single nanowire sensor, the nanowire must be carefully positioned on electrodes. Compared to nanowire films (Fig. 7.3b), fabrication of sensor devices based on a single nanowire requires the use of more complex and multiple processes, as well as high fabrication cost.

However, single nanowire sensors afford the opportunity to fully utilize the unique features of 1D nanostructure, e.g., the very thin diameter, large surface-to-volume ratio, and high crystalline quality. Kolmakov et al. [12] demonstrated that for SnO_2 nanowires with a diameter of 60 nm the surface adsorption of molecules could alter the bulk electronic properties of the nanowire, not merely the surface region.

Furthermore, in a single nanowire device, the effects coming from nanowire–nanowire interfaces are avoided, which plays an important role in conventional sensors based on polycrystalline nanoparticle and nanowire films. The absence of such crystallite interfaces ensure the successful realization of a conductivity switch, the bulk conductivity of which is fully determined by the surface sensing behavior.

This offers the base for researchers to study the intrinsic sensing mechanism arising from the surface chemistry occurring on a nanowire.

7.3 Nanowire–Nanoparticle Heterostructures and Gas Sensing Mechanism

Nanowires can function as a sensing element in many sensor configurations [38] such as chemiresistors, Field-effect transistors (FET), optical sensors, surface acoustic wave sensors and quartz crystal microbalance sensors, among which the chemiresistor whose conductance is altered by charge-transfer processes occurring at their surfaces and FET whose properties is controlled by applying an appropriate potential onto its gate are commonly used for investigation of sensing features of nanowires [6, 7].

The fundamental operating principles of gas sensing have been explained in many publications. Briefly electrical conductivity or resistivity of materials is modified by the sensing reactions between ionosorbed oxygen species and gas molecules. The gas sensing reactions induce charge transfer, which alters the conductance or resistance of the materials. The sensing reactions taking place on material surface usually involve mainly three processes, i.e. adsorption, reaction, and desorption. Take n-type metal oxides such as ZnO, SnO_2, and In_2O_3 for example (Fig. 7.4a),

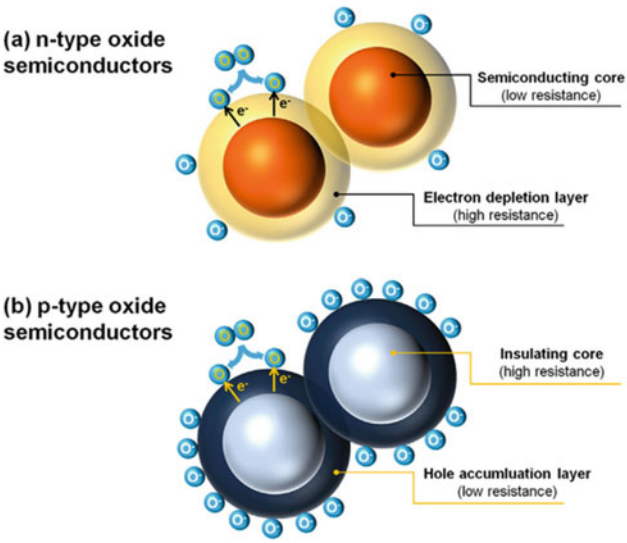

Fig. 7.4 Formation of (**a**) electron depletion layer in n-type and (**b**) hole accumulation layer in p-type oxide semiconductors. Reproduced from ref. [10], Copyright 2014,with permission of Elsevier

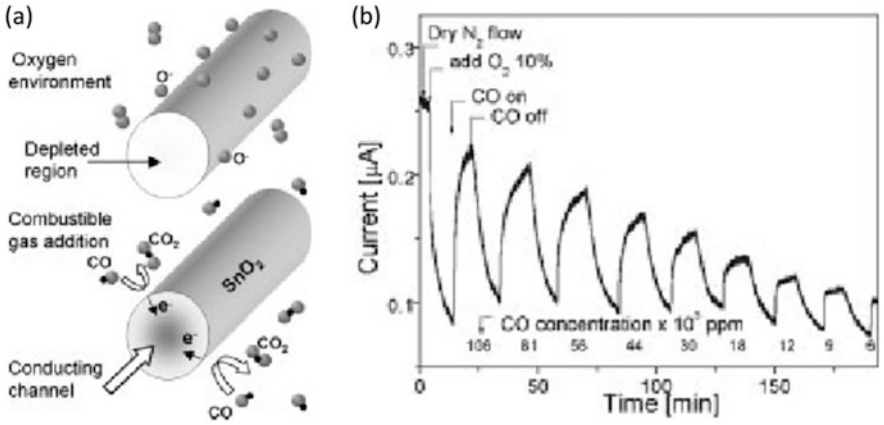

Fig. 7.5 The sensing mechanism of SnO_2 nanowires involves (**a**) a completely depleted and hence nonconductive state under an oxidizing ambient and sharply increased conductance due to electron transfer from surface states back into the nanowires interior when a reducing gas (CO) is admitted. (**b**) The response of the nanowires toward O and CO pulses. The CO concentration in the flowing gas was reduced from pulse to pulse. Reproduced from ref. [12] with permission of Wiley-VCH

oxygen molecules adsorb onto the surface of semiconductors and ionize into chemisorbed oxygen species such as O_2^-, O^-, and O^{2-} by drawing electrons from the surfaces of the semiconductors [41, 42]. In general, it is believed that the chemisorbed oxygen species of O_2^-, O^-, and O^{2-} are dominant at <150 °C, between 150 and 400 °C, and at >400 °C, respectively [42]. This process creates an electron depletion layer and turns the semiconductor into a high resistive state [42]. While for p-type metal oxide semiconductors (Fig. 7.4b), this leads to the formation of hole accumulation layer near the surface. Exposure to reductive gases such as ethanol will result in an increase in the conductivity for n-type semiconductors and a decrease for p-type materials, whereas the effect of oxidative gases is reversed.

1D metal oxide nanowires with a typically high length-to-diameter ratio are regarded as promising candidates for high-performance sensor. Based on the well-known grain size effect [43], sensor sensitivity is critically related to the grain size (D) of nanoparticles when D is comparable to 2 L (L is the thickness of electron depletion layer or space charge layer). When D is larger than 2 L, only the grain boundary is subject to formation of electron depletion layer, meaning that the sensing reactions do not change the sensor resistance very much. From this perspective the diameter of nanowires should have an important effect on gas sensing performances. For example, Kolkamov et al. [12] stated that not only the surface region but also the entire SnO_{2-} nanowire could be depleted of electrons if the diameter is small enough, i.e. comparable to the Debye length (ca. 43 nm for SnO_2 at 500 K). In air rich of oxygen, the SnO_2 nanowires are non-conductive because the nanowire is fully depleted of conduction electrons (Fig. 7.5a). Exposure to

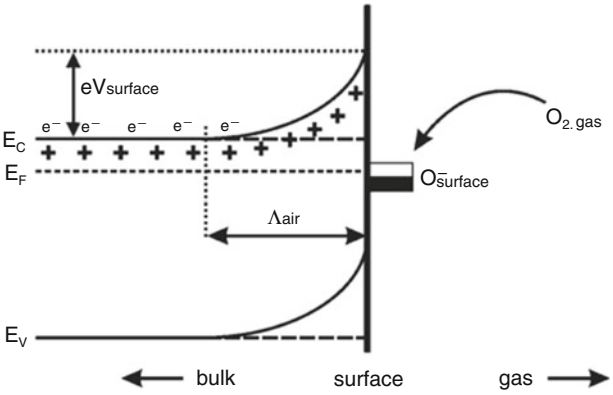

Fig. 7.6 Illustration of band bending in a wide bandgap semiconductor after chemisorption of charged oxygen species on surface sites. E_C, EV, and E_F denote the energy of the conduction band, valence band, and the Fermi level, respectively, while Λ_{air} denotes the thickness of the space-charge layer, and $eV_{surface}$ the potential barrier. The conducting electrons are represented by e^- and + represents the donor sites. Reproduced from ref. [22] with permission of Wiley-VCH

combustible gas such as CO switches the SnO_2 nanowires into conductive state again. Their sensing properties shown in Fig. 7.5b are also consistent with this mechanism.

The adsorption of the charged oxygen species leads to band bending (Fig. 7.6), which generates a surface potential barrier eV_s. The height (eV_s) and depth (w) of the band bending depend on the surface charge concentrations, [22, 44] which is determined by the amount and type of adsorbed oxygen. The conductance of nanowires can be defined as [31, 38, 42].

$$G = n_0 e \mu \pi \frac{(D - 2w)^2}{4L}$$

where n_0 is the concentration of charge carriers, e the electron charge, μ the mobility of the electrons, D and L are the diameter and length of the nanowire channel, w the depth of electron depletion layer which is related to the Debye length of materials. The Debye length is obtained in Schottky approximation [42].

$$w = \lambda \sqrt{\frac{eV_s}{kT}}$$

$$\lambda = \sqrt{\frac{\varepsilon \varepsilon_0 kT}{e^2 n_0}}$$

where V_S is the band bending induced by chemisorption of charged species, ε_0 the absolute dielectric constant, ε the relative dielectric permittivity of the structure, k the

Bolzmann's constant, T the temperature. The change in conductance induced by the surface sensing process can be expressed as

$$\Delta G = \Delta n_s e \mu \pi \frac{(D - 2w)^2}{4L}$$

Therefore the sensor sensitivity (S, in some cases *sensitivity* is also named as *Response* [11]) can be defined as

$$S = \frac{\Delta G}{G} = \frac{\Delta n_s}{n_0}$$

where Δn_s is the change in concentration of charge carriers. The linear dependence of S on Δn_s reveals that a more measurable change in concentration of charge carriers can enhance the sensor sensitivity. Great effort is thus focused on manipulating the Δn_s through surface functionalization of metal oxide nanowires.

Although metal oxide semiconductor holds a dominant position in gas sensing, they suffer from some critical drawbacks such as poor selectivity and high operating temperature. The past 15 years has witnessed significant advance in sensor performance propelled by sensor scientists. Numerous efforts have approved the effectiveness of surface functionalization of nanowires by nanoparticles as a sensitizer or promotor toward optimizing the "4S" sensor parameters, i.e., sensitivity, selectivity, stability, and speed, as well as operating temperature. In the following section we will mainly discuss the unique heteronanowires being composed of nanowires as the host and guest nanoparticles, and their sensing mechanism. Based on the functionalization materials, the guest phase are classified as metal nanoparticles and metal oxide nanoparticles.

7.3.1 Metal Oxide–Metal Heteronanowires

To date, great success has been achieved in employing noble metal nanoparticles as a promotor to sensitize the surface of metal oxide semiconductors for enhanced gas sensing. Metal nanoparticles can be loaded onto metal oxides to give the heterostructures by various physical or chemical techniques [45, 46]. Table 7.1 summarizes some typical gas sensors based on 1D Metal oxide-Metal nanostructures.

From Table 7.1, it is seen noble metals such as Au, Ag, Pd, and Pt have been widely used as a promotor. However the promotion mechanisms are quite different based on the used metals. According to Yamazoe, [43] the "promotion effect" by noble metals can be classified as "chemical sensitization" or "electronic sensitization", depending on whether the noble metals change the work function of the semiconductor or not. The chemical sensitization (Fig. 7.7a) takes place via a

Table 7.1 Properties of gas sensors based on 1D metal oxide-metal nanostructures

Materials	Test gas	Concentration (ppm)	Sensitivity (S)/ Response (R)	Detection limit (ppm)	Temperature (°C)
Pd/ZnO nanowires [21]	H_2S	10	732.1	< 1	265
Pd/ZnO nanowires [47]	Ethanol	500	61.5%	< 5	230
ZnO/Au nanowires [48]	CO	50	60%	< 5	250
ZnO/Pt nanowires [49]	NO_2	0.1	1.08	< 0.1	100
Pd/ZnO nanowire [50]	Acetone	500	153.8	–	300
ZnO/Au nanowires [51]	Ethanol	100	33.6	< 2	380
Au/ZnO nanorods [52]	H_2S	3	475	< 1	25
Au/ZnO nanowires [53]	Benzene	10	6.275	< 1	340
Au/ZnO nanowires [54]	H_2S	1	38	1	25
Au/ZnO nanorods [55]	Ethanol	100	52.5	< 1	310
Au/ZnO nanowires [56]	Ethanol	5	1.33	< 5	325
Ag/ZnO nanowires [57]	Ethanol	10	6	1	280
Au/ZnO nanorods [58]	NO_2	2	16 (S)	500 ppb	150
Pt/ZnO nanowires [59]	Ethanol	50	32.6	250 ppb	265
Pd/ZnO nanorods [60]	CO	1000	4.6	–	300

(continued)

Table 7.1 (continued)

Materials	Test gas	Concentration (ppm)	Sensitivity (S)/ Response (R)	Detection limit (ppm)	Temperature (°C)
Au/ZnO nanorods [61]	CO	200	3.4 (S)	–	150
Pt/SnO_2 nanowires [62]	H_2	100	13	–	150
Pt/SnO_2 nanorods [63]	Ethanol	200	39.5	< 10	300
Pt/SnO_2 nanowires [64]	Toluene	1	40	< 1	300
Pt/SnO_2 nanowires [65]	CO	400	7	1	400
Pd/SnO_2 nanorods [66]	Ethanol	500	5.9	–	300
Pd/SnO_2 nanofibers [67]	Formaldehyde	100	18.8	–	160
Rh/SnO_2 nanofibers [68]	Acetone	50	60.6	< 1	200
Ag/SnO_2 nanowires [69]	NO_2	1	>1000	–	300
Pd/SnO_2 nanorods [70]	H_2	10	2.85	–	350
Au/SnO_2 nanowires [71]	NO_2	60	10	0.1	300
Pd/SnO_2 nanofibers [72]	H_2	1	2.57	20 ppb	160
Pt/In_2O_3 nanofibers [73]	H_2S	600	1490	–	200
Pt/In_2O_3 nanowires [74]	O_2	15	1.04	–	50
Au/In_2O_3 nanowires [75]	CO	5	104	< 0.2	Room temp.

(continued)

Table 7.1 (continued)

Materials	Test gas	Concentration (ppm)	Sensitivity (S)/ Response (R)	Detection limit (ppm)	Temperature (°C)
Au/In_2O_3 nanorods [76]	Acetone	50	40	10 ppb	250
Pd/In_2O_3 nanowires [16]	NO_2	30	8	< 3	300
Au/In_2O_3 nanowires [77]	CO	100	2200	500 ppb	Room temp.
Ag/TiO_2 nanobelts [78]	Ethanol	20	6.659	–	200
Pd/TiO_2 nanobelts	Ethanol	10	7.16	–	200
Pt/TiO_2 nanowires [79]	CO	30	1.18	–	300
Pd/TiO_2 nanowires [80]	H_2	1000	7	–	100
Pd/TiO_2 nanowires [81]	Chloroform	1000	0.65	–	200
Pd/TiO_2 nanorods [82]	H_2	1000	250	–	30
Au/WO_3 nanorods [83]	H_2	50	6.6	–	290
Pt/WO_3 nanorods [84]	Ethanol	200	7.3	< 1	220
Pd/WO_3 nanorods [85]	NH_3	100	5	–	300
Pd/WO_3 nanotubes [86]	H_2	500	17.6	< 10	450
Au/WO_3 nanowires [87]	H_2S	10	80	< 5	291
Ru/WO_3 nanorods [88]	H_2S	10	192	0.2	350

(continued)

Table 7.1 (continued)

Materials	Test gas	Concentration (ppm)	Sensitivity (S)/ Response (R)	Detection limit (ppm)	Temperature (°C)
Pd/WO_3 nanowires [89]	H_2	1000	3	–	300
Au/Fe_2O_3 nanowires [90]	Acetone	1	5.91	< 1	270
Au/Fe_2O_3 nanorods [91]	Butanol	100	9.5	–	320

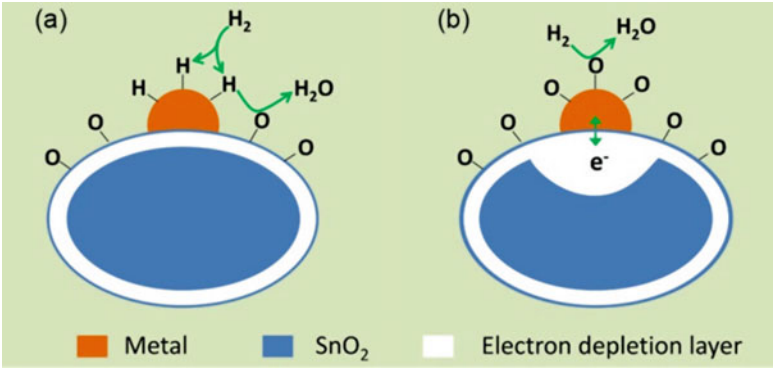

Fig. 7.7 Schematic illustration of (**a**) chemical sensitization and (**b**) electronic sensitization of metal promoters on SnO_2 surface. Reproduced from ref. [93] with permission of Wiley-VCH

spill-over effect, which is well-known in catalytic science. The metal promoter, such as Pt, activates the test gas molecules to facilitate its oxidation on the semiconductor surface. According to Barsan et al., [92] Au also doesn't alter the bulk or surface electronic properties of metal oxide support, hence belonging to the "chemical sensitization" via spill-over effect. In this case the metal promoter does not affect the resistance of the semiconductor and the promoter increases the sensor sensitivity by increasing the reaction rate of the chemical processes. Electronic sensitization (Fig. 7.7b) results from a direct electronic interaction at the interface between the promoter and semiconductor. Specifically, typical promoters (e.g., Ag and Pd) of electronic sensitization are known to form stable oxides (AgO and PdO) in air, and produce an electron-depleted space charge layer on the surface. The electronic sensitization will decrease when the oxide form of metal promoters are reduced to metal by reductive gases.

In another work, Kolmakov et al. [15] have reported that Pd nanoparticles could sensitize the SnO_2 nanowires through spillover effect in addition to electronic

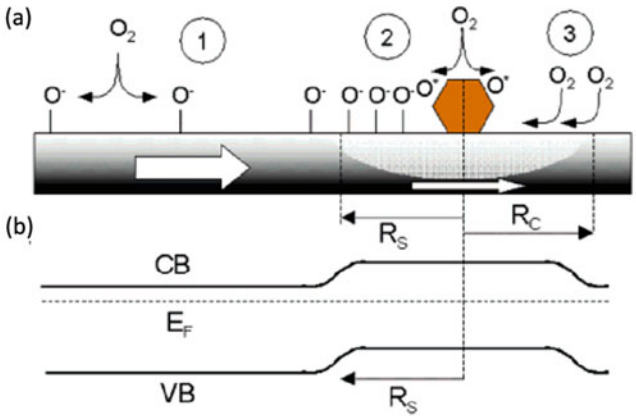

Fig. 7.8 (**a**) Schematic depiction of the three major process taking place at a SnO_2 nanowire/nanobelt surface: (1) ionosorption of oxygen at defect sites of the pristine surface; (2) molecular oxygen dissociation on Pd nanoparticles followed by spillover of the atomic species onto the oxide surface; (3) capture by a Pd nanoparticle of weakly adsorbed molecular oxygen that has diffused along the tin oxide surface to the Pd nanoparticle's vicinity (followed by process 2). R_S is the effective radius of the spillover zone, and R_C is the radius of the collection zone. (**b**) Band diagram of the pristine SnO_2 nanostructure and in the vicinity (and beneath) a Pd nanoparticle. The radius of the depletion region is determined by the radius of the spillover zone. Reproduced from ref. [15] with permission. Copyright 2005, American Chemical Society

sensitization. In contrast to the findings from Barsan et al. [92], they also observed a reduction in conductance of SnO_2 nanowires after loading Au nanoparticles due to formation of baroscopic depletion regions. The decreased conductance is caused by the electron transfer from semiconductor to metal particles induced by nano-Schottky junctions. Figure 7.8 shows both the "chemical sensitization" and "electronic sensitization" of Pd nanoparticles on SnO_2 nanowires. The "electronic mechanism" proposes the formation of depletion zones around the Pd nanoparticles and attributes the improved sensing to the modulation of the nano-Schottky barriers (and hence the width of the conduction channel) due to changes in the oxidation state of the Pd (and therefore its work function) accompanying oxygen adsorption and desorption. Furthermore, the Pd nanoparticles catalytically activate the dissociation of molecular oxygen by spillover effect, "chemical mechanism", whose atomic products then diffuse to the metal oxide support. This process greatly increases both the quantity of oxygen that covering on the SnO_2 surface and the rate at which this dissociation process occurs, resulting in a greater (and faster) degree of electron withdrawal from the SnO_2 (and at a lower temperature) than for the pristine SnO_2 nanowires.

By either chemical sensitization or electronic sensitization, researchers are able to optimize the sensors to selectively detect gas with higher sensitivity and faster response time. In the following parts we will give a detailed overview of the current progress.

7.3.2 *Metal Oxide–Metal Oxide Heteronanowires*

Besides noble metal nanoparticles, various metal oxide nanoparticles also demonstrate great success in improving the sensing features of semiconductors. An appropriate combination of different metal oxide semiconductors to produce heterostructures can lead to enhanced charge transduction and modulated potential barriers at the interface. For heteronanowires constituted by metal oxide nanowires and metal oxide nanoparticles, of central importance is the interface between nanowires and nanoparticles. When two metal oxide semiconductors with different Fermi levels come into contact, the electrons at the higher level will transport across the interface to the lower one until the Fermi energies reach in equilibrium. This leads to a region depleted of charge carriers at the interface. Moreover, a potential energy barrier is generated at the interface due to the band bending which is caused by the difference in original Fermi levels of the materials. Electrons must overcome this barrier in order to cross the interface. Based on the different conductivity type of semiconductors, the coupling of metal oxides can give different heterointerface or heterojunction, e.g. p-n, n-n and p-p. Since n-type metal oxide semiconductors are much more widely used than p-type for gas sensors, [10, 94] within this chapter we mainly focus on the heteronanowires containing n-type metal oxide nanowires as the host.

7.3.2.1 P-N Heteronanowires

P-type metal oxides such as NiO, CuO, Cr_2O_3 and Co_3O_4 are not popularly used for gas sensors due to their low charge carrier mobility and structure instability, [94] however, they can be used as a good promotor in combination with n-type metal oxides to achieve better sensor properties by virtue of p-n heterojunctions. Table 7.2 surveys the gas sensing performances of 1D n-p heterostructures constructed by p-type nanoparticles and n-type nanowires.

The formation of p-n heterojunctions is equivalent to electron–hole recombination in the vicinity of a p–n junctions [103]. Electrons flow from n-type metal oxides to the p-type one and holes flow from p-type metal oxides to the n-type one until the build-up potential prevents such flow. This charge carrier transfer results in a reduction of the hole concentration in the p-type metal oxide and electron concentration in the n-type metal oxide, thus a space charge layer is formed at the heterointerface. Figure 7.9 illustrates the corresponding band structure of heterojunctions in p-Cr_2O_3 nanoparticles/n-SnO_2 nanowires [103]. The width of

Table 7.2 Gas sensing performances of 1D p-n heterostructures

Materials	Test gas	Concentration (ppm)	Sensitivity (S)/Response (R)	Detection limit (ppm)	Temperature (°C)
CuO/WO_3 nanowires [95]	H_2S	100	672.5%	1	300
Co_3O_4/WO_3 nanowires [96]	H_2	2000	6.1	–	200
Co_3O_4/WO_3 nanorods [97]	Acetone	100	5.3	< 6	280
Co_3O_4/ZnO nanorods [17]	NO_2	5	45.4	–	200
NiO/ZnO nanowires [98]	Ethanol	5	29.04	0.05	450
CuO/ZnO nanowires [99]	Ethanol	100	98.8	1	300
CuO/ZnO nanorods [100]	Triethylamine	50	8	< 10	40
CuO/ZnO nanofibers [101]	H_2S	10	18.7	1	230
CuO/SnO_2 nanowires [102]	H_2S	10	15	0.1	300
Cr_2O_3/SnO_2 nanowires [103]	H_2	10	41	–	300
Cr_2O_3/SnO_2 nanowires [19]	Trimethylamine	5	9.87	–	450
NiO/SnO_2 nanowires [104]	H_2S	10	1372	1	300
Cu_2O/SnO_2 nanowires [105]	Benzene	10	12.5	< 5	300
CuO/SnO_2 nanofibers [106]	H_2S	1	23	–	200
CuO/SnO_2 nanofibers [107]	H_2S	10	1.98×10^4	–	300
CuO/In_2O_3 nanowires [108]	H_2S	5	1.16×10^5	1	150

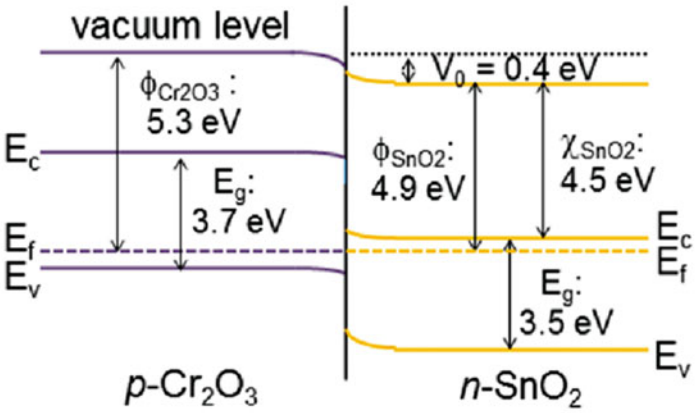

Fig. 7.9 Scheme of the band structure of p-Cr_2O_3/n-SnO_2 heterojunctions. Reproduced from ref. [103] with permission. Copyright 2014, American Chemical Society

the space charge layers (X_n and X_p) induced by the p − n heterojunctions can be calculated using the following equations [46, 103].

$$X_n = \sqrt{\frac{2\varepsilon_n V_0}{q}\left(\frac{N_p}{N_n}\right)\left(\frac{1}{N_n + N_p}\right)}$$

$$X_p = \sqrt{\frac{2\varepsilon_p V_0}{q}\left(\frac{N_n}{N_p}\right)\left(\frac{1}{N_n + N_p}\right)}$$

where ε_n and ε_P, are the static dielectric constant, N_n and N_p carrier concentration of n- and p-type metal oxide semiconductors, respectively, V_0 the contact potential difference between n- and p-type metal oxides.

7.3.2.2 N-N Heteronanowire

Researches have shown that heteronanostructures containing two n-type metal oxides are also quite promising for gas sensing. Table 7.3 lists some typical examples of gas sensors based on n-n heteronanowires.

Unlike the p-n heteronanowires, whose interface at the p–n junction has far few free electrons due to electron-hole recombination, increasing the resistance [45], the interface at an n–n junction simply transfers electrons from the semiconductor with a high Fermi level to the one with a low Fermi level, resulting in a depletion layer in the former and an accumulation layer in the latter. The accumulation layer is further depleted by subsequent oxygen adsorption on the surface, increasing the potential

Table 7.3 Gas sensing performances of 1D n-n heterostructures

Materials	Test gas	Concentration (ppm)	Sensitivity (S)/Response (R)	Detection limit (ppm)	Temperature (°C)
SnO_2/ZnO nanorods [109]	H_2	500	70%	–	400
SnO_2/ZnO nanowires [110]	H_2S	500	1.5	–	250
ZnO/WO_3 nanorods [111]	NO_2	5	281%	–	300
SnO_2/ZnO nanorods [112]	NO_2	500 ppb	13.4	< 200 ppb	Room temp.
ZnO/Fe_2O_3 nanorods [113]	Butanol	100	54.4	–	225
TiO_2/WO_3 nanorods [114]	Acetone	200	7.6	< 10	
ZnO/Fe_2O_3 nanospindles [115]	Ethanol	100	17.8	< 2	280
SnO_2/Fe_2O_3 nanotubes [116]	Ethanol	100	27.45	< 5	200
SnO_2/WO_3 nanowires [117]	H_2	1	137	–	300
Fe_2O_3/In_2O_3 nanowires [118]	Acetone	10	298%	–	200
In_2O_3/SnO_2 nanowires [119]	NO_X	100	8.98	0.1	Room temp.
ZnO/SnO_2 nanotubes [120]	NO_2	5	30.84	0.5	300
In_2O_3/SnO_2 nanofibers [121]	Trimethylamine	10	7.11	< 1	260
La_2O_3/WO_3 nanofibers [122]	Acetone	200	17.8	0.8	350
In_2O_3/WO_3 nanofibers [123]	Acetone	50	12.9	0.4	275
TiO_2/SnO_2 nanofibers [124]	Acetone	100	13.7	< 10	280

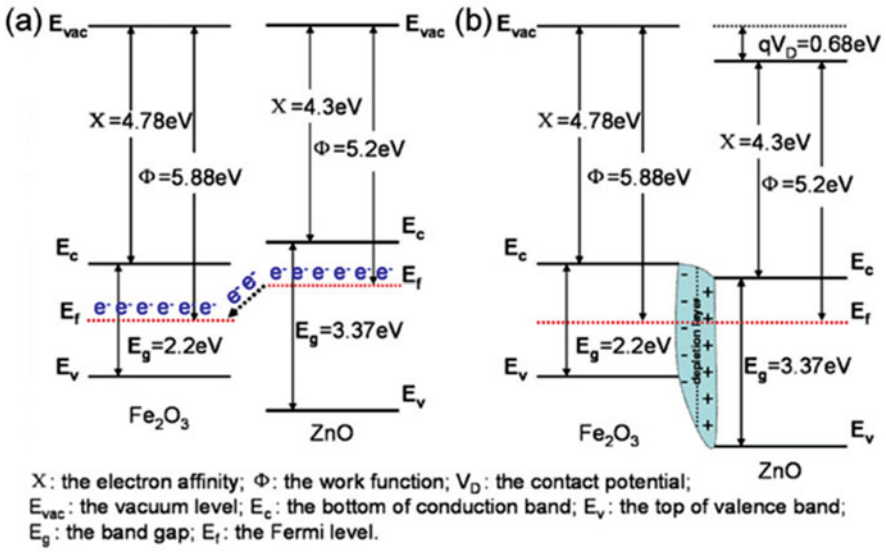

Fig. 7.10 Band structures of (**a**) α-Fe_2O_3 and ZnO and (**b**) α-Fe_2O_3@ZnO heterostructures. Reproduced from ref. [125] with permission of IOP Publishing

energy barrier at the interface. Therefore the sensor response can be enhanced. Fig. 7.10 displays the band structure of a heterostructure based on n-type α-Fe_2O_3 and ZnO [125]. ZnO has a higher Fermi level than α-Fe_2O_3 (Fig. 7.10a), hence the electrons migrate from ZnO to the α-Fe_2O_3 until their Fermi levels equalize, as shown in Fig. 7.10b. The electron transfer leads to the formation of electron depletion layer at the ZnO side. On the surface of ZnO, there is also an electron depletion layer produced by ionized oxygen species. The two conjugated electron depletion layers significantly decrease the carrier concentration in ZnO, making the material highly resistive, and this finally enhances the sensor response.

7.4 Gas Sensing Performances of Heteronanowires

The most important parameters of gas sensor are sensitivity, selectivity, stability and speed (response-recovery rate), namely "4S" and operating temperature. In this section we will overview the advances made in the literature to show how to improve the sensor parameters by using heteronanowires as the sensing layer.

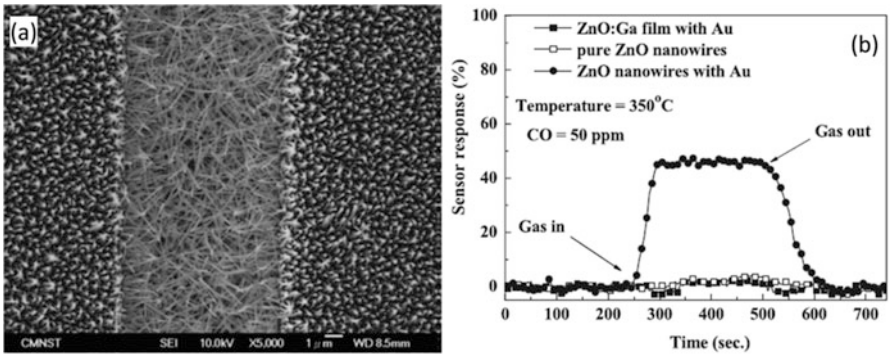

Fig. 7.11 Detector responses of the (**a**) ZnO nanowire-based CO gas sensors; (**b**) responses to 50 ppm CO of different ZnO sensors at 350 °C. Reproduced from ref. [48] with permission of IOP Publishing

7.4.1 Enhanced Sensing Performance of Metal/Metal Oxide Heteronanowires

Numerous works have shown that functionalization of metal oxide nanowires can lead to an enhancement of sensor sensitivity or response. For example, Au-functionalized ZnO nanowires have demonstrated enhanced sensitivity or response to CO, [48] NO_2, [58] H_2S, [52] ethanol, [51, 57] and benzene [53]. In Fig. 7.11, Chang et al. [48] showed that at 350 °C the Au/ZnO nanowires possess a significant higher response to CO than that of pure ZnO nanowire and Au/ZnO film. Other heteronanowires such as Pt/SnO_2 nanowires [64],Pd/ZnO nanorods [60] and Au/In_2O_3 nanowires [75, 77], Pt/TiO_2 nanowires [79] are also reported to enhance the sensor sensitivity or response to CO.

One of the main drawbacks of metal oxide semiconductor sensor materials is the high working temperature, usually between 200 and 400 °C, which is not favorable for obtaining long-term sensor stability. Through metal nanoparticle functionalization, the working temperature of nanowires can be lowered in some cases. For example, Katoch and coworkers [49] reported that the Pt/ZnO nanowires can detect NO_2, CO and benzene at 100 °C with high and fast responses. Lee et al. [75] and Zou et al. [77] show that Au functionalization could result in CO response at room temperature. The FET sensor based on Au/In_2O_3 nanowires [75] is able to detect distinct electrical changes for the CO gas concentration in the range of down to 0.2–5 ppm at room temperature (Fig. 7.12).

For detecting H_2S, Ramgir et al. [54] reported that Au/ZnO nanowires had a much higher response and better selectivity than pure ZnO at room temperature (Fig. 7.13). They also found that the content of Au nanoparticles was crucial to the sensor response. A maximum response is obtained for 1.2 at% Au at room temperature, and this could be attributed to the formation of Au islands ~5 nm size. A remarkable 16-fold increase in the sensor response toward 5 ppm H_2S was obtained by Au

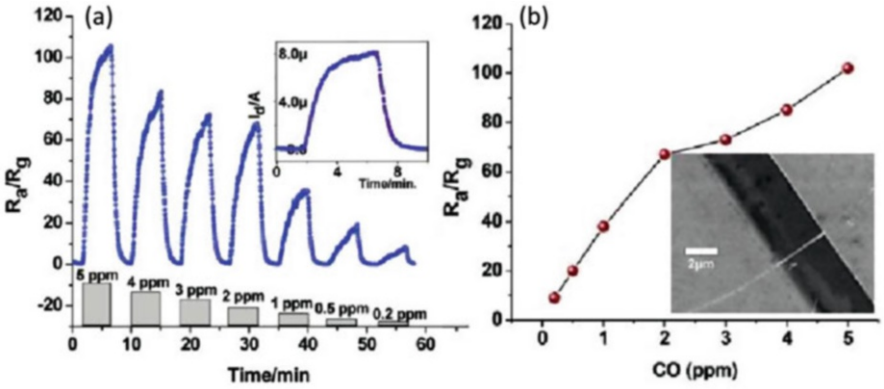

Fig. 7.12 (**a**) Response plot for the Au/In_2O_3 nanowire FET (standard 60 min loading time), when exposed to 5–0.2 ppm CO and inset shows a zoomed view of the I_d-time plot for 5 ppm CO gas, (**b**) sensor response plot for CO gas at room temperature for the same device as shown in the inset. Adapted from ref. [75] with permission. Copyright 2011, American Chemical Society

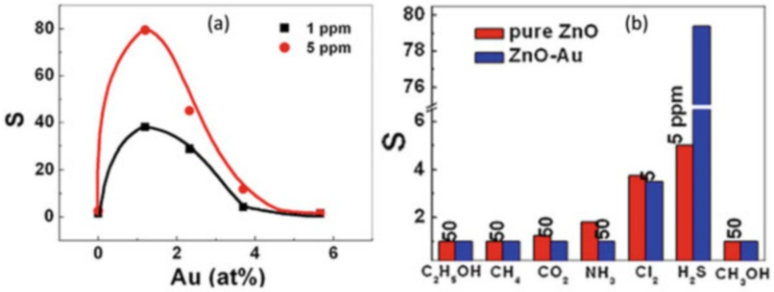

Fig. 7.13 Sensor performance of Au/ZnO nanowires at room temperature, (**a**) sensor response as a function of Au (at%) to H_2S, and (b) selectivity pure and Au (1.2 at%) modified ZnO nanowires samples toward different gases. Reproduced from ref. [54], Copyright 2013, with permission from Elsevier

functionalization. Formation of nano-Schottky type barrier junction at the interface between Au and ZnO has been proposed, and this was correlated with the observance of a higher resistivity and a higher work function (0.2 eV) for Au/ZnO. The enhanced response was thus attributed to the alteration of barrier properties by the adsorption or desorption of adsorbed gas molecules. Decrease in the operating temperature of 1D metal oxide nanostructure-based sensors was also observed in many other material systems such as Pd/SnO_2 nanofibers [72], Pt/In_2O_3 Nanofibers [73], Pt/In_2O_3 nanowires [74], Au/In_2O_3 nanorods [76], and Ag/TiO_2 nanobelts [78], Pd/WO_3 nanowires [126] and Pt/WO_3 nanowires [127].

The selective detection of gas molecules is essential for practical application of gas sensors. Sensors based on semiconductor metal oxides often suffer from a poor discretion among multiple gases. Studies have shown that the sensor selectivity

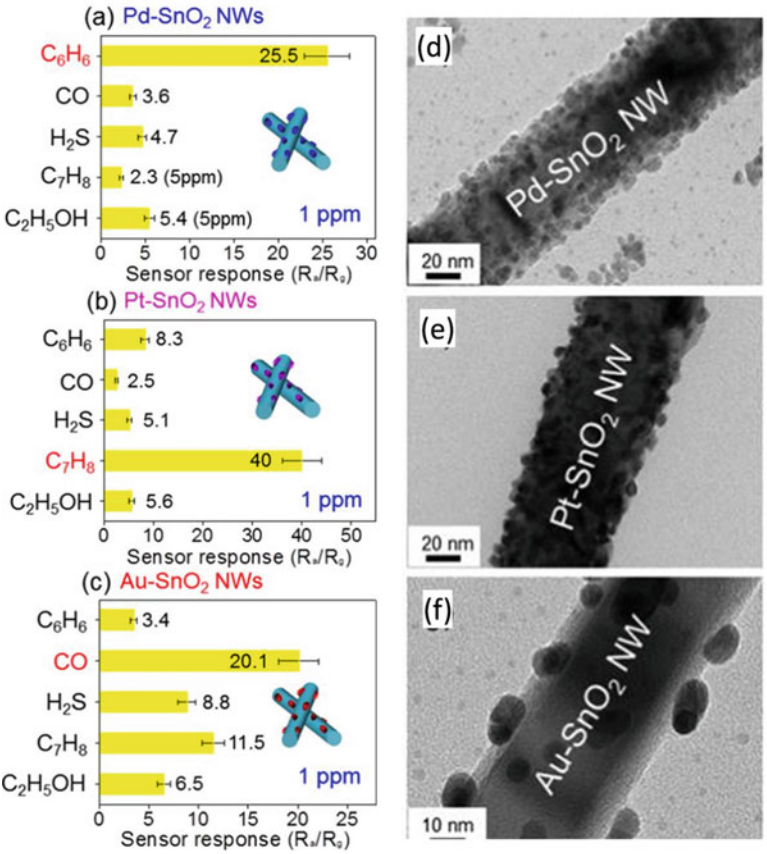

Fig. 7.14 Selective sensing properties of metal-functionalized SnO_2 nanowires: (**a**) Pd, (**b**) Pt, and (**c**) Au; and TEM images: (**d**) Pd/SnO_2, (e) Pt/SnO_2, and (f) Au/SnO_2 nanowires. Reproduced from ref. [64] with permission, Copyright 2016, American Chemical Society

could be optimized by noble metal functionalization towards detecting specific analytes. Kim et al. [64] fabricated a serious of gas sensors based on SnO_2 nanowires functionalized with Pd, Pt and Au nanoparticles using the γ-ray radiolysis technique. Their gas sensing tests (Fig. 7.14) demonstrated that the each noble metal provided exceptional selectivity for a specific gas, i.e., Pd for C_6H_6, Pt for C_7H_8, and Au for CO. They attributed the selective sensing behaviors to the chemical sensitization of noble metals. Briefly, the catalytic oxidation of CO on Au is efficiently improved, the C_6H_6 strongly interacts with Pd, and C_7H_8 tends to bond strongly onto Pt. In another work, Liao and Ho and coworkers [77] designed a gas sensor based on Mg-doped In_2O_3 nanowire FET arrays decorated with Au, Ag, and Pt nanoparticles. This type of gas sensor exhibited a "one key to one lock" selective detection to reducing gases with distinguishable selectivity to CO, C_2H_5OH and H_2, respectively.

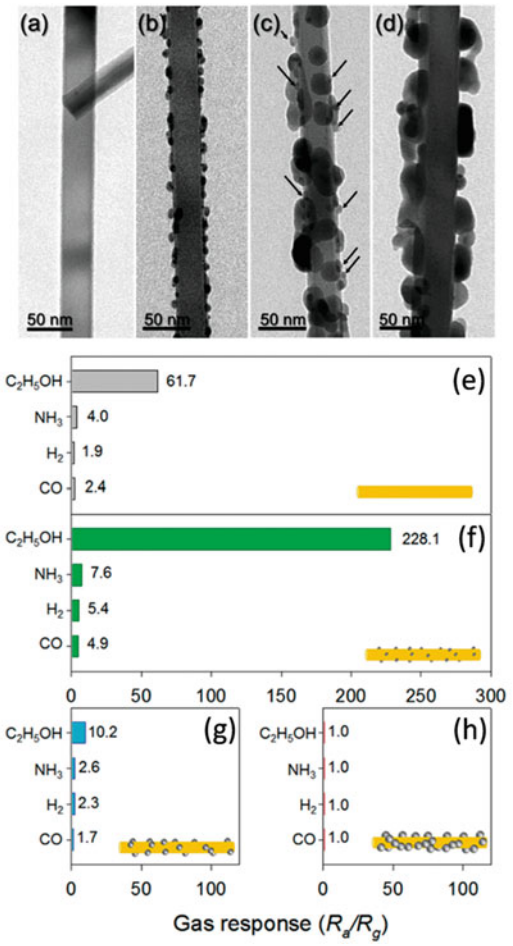

Fig. 7.15 TEM of (**a**) pure SnO_2, (**b**) 5Ag-SnO_2, (**c**) 10Ag-SnO_2, and (**d**) 50Ag-SnO_2 nanowires after heat treatment at 450 °C for 2 h; (e-h) gas responses to 100 ppm various gases at 450 °C. Reproduced from ref. [128] with permission. Copyright 2011, American Chemical Society

For metal nanoparticles functionalization, the loading of metals should be elaborately optimized in order to get the best response. Lee and coworkers [128] studied the effect of the loading of Ag nanoparticles on the detection of ethanol of SnO_2 nanowires. The sensor selectivity to ethanol against NH_3, CO, and H_2 was investigated for three discrete Ag loadings of the SnO_2 nanowires (Fig. 7.15a–d). An optimum Ag loading (Fig. 7.15b, the SnO_2 nanowires were decorated with a high density of 3–8 nm Ag nanoparticles) was observed in terms of both the sensor sensitivity to ethanol and its selectivity for ethanol against the other three gases. In Fig. 7.11f, at the optimum Ag loading, the sensor response to 100 ppm ethanol is 228, significantly higher than that (67) of pure SnO_2 nanowires. It is also seen that higher loading of Ag nanoparticles degraded the sensor response. This might be due to that larger Ag nanoparticles partially or completely connected with each other, as a result, the sensor resistance is not governed by gas sensing properties of SnO_2

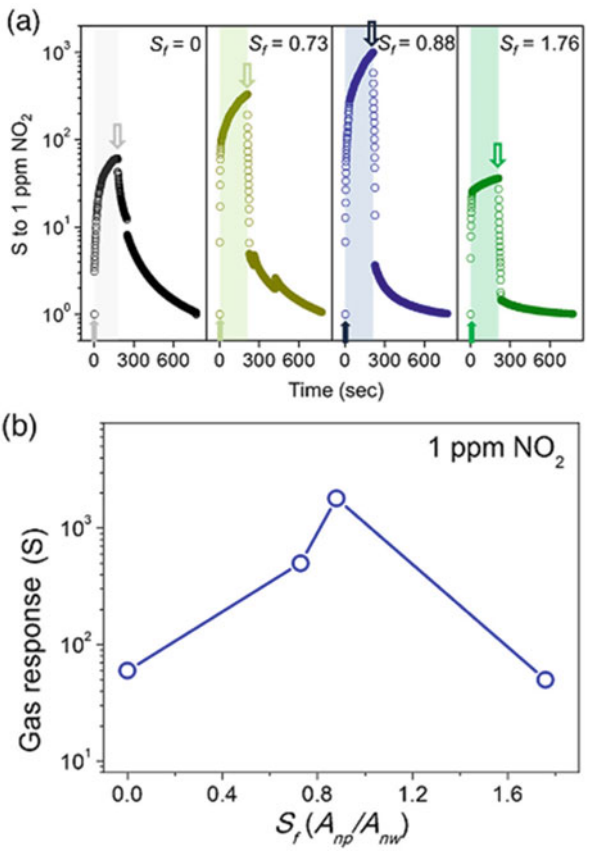

Fig. 7.16 (**a**) Response-recovery curves and (**b**) sensor responses of SnO_2 nanowires functionalized with Ag nanoparticles as a function of S_f. Reproduced from ref. [69], Copyright 2017, with permission from Elsevier

nanowires, but instead it is determined by the insensitive conducting Ag layer. In another work, Kim et al. [69] also studied the NO_2 sensing properties of SnO_2 nanowires as a function of the surface coverage of Ag nanoparticles. The surface coverage (Sf) is defined as the ratio of the average surface area (A_{np}) of Ag NPs to the unit surface area (A_{nw}) of SnO_2 nanowire. As shown in Fig. 7.16, the surface coverage of Ag in the range of 0–1.76 has a large effect on the response to 1 ppm NO_2 of the SnO_2 nanowires. At a S_f of 0.88, the sensor exhibited the highest response, while a further increase of S_f to 1.76 severely deteriorated the response. These works suggest that optimization of S_f or loading of metal is a key parameter in metal nanoparticle–functionalized nanowire sensors.

Response-recovery speed is another important index for gas sensors. The response and recovery times are usually defined as the time for the sensor to reach 90% of the final resistance of the sensor. Metal functionalization of nanowires can also lead to an enhancement of the sensor response-recovery rate. Kim et al. [16] investigated the effect of Pd functionalization on the response-recovery speed of In_2O_3 nanowires for detecting 3 ppm NO_2. In Fig. 7.17, it shows that the response

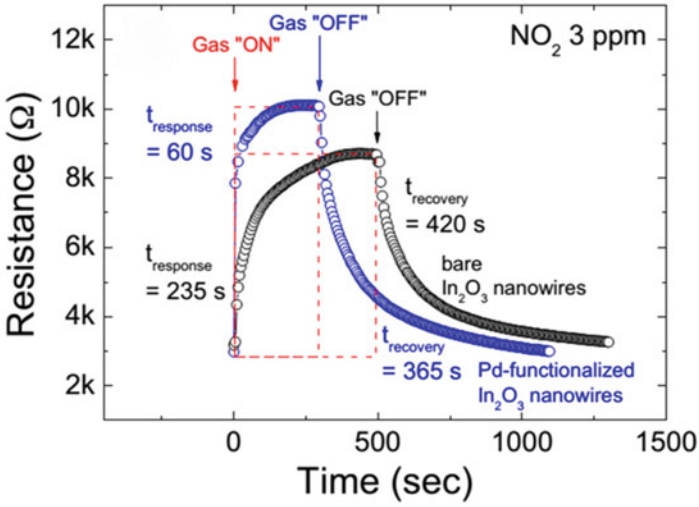

Fig. 7.17 (**a**) Dynamic responses of bare and Pd-functionalized In_2O_3 nanowires for 3 ppm NO_2. Reproduced from ref. [16], Copyright 2011, with permission from Elsevier

time is decreased from 235 S to 60 S due to Pd functionalization, and the recovery time is also greatly shortened.

7.4.2 Enhanced Sensing Performance of P–N Heteronanowires

As shown in Table 7.1, the p-n heteronanowires consist of a variety of material systems, which have demonstrated appealing features in gas sensing. Co_3O_4, NiO, CuO, and Cr_2O_3 are among the most widely used p-type promotors. The unique p-n heterojunction formed at the interface of p-type and n-type semiconductors plays a vital role in gas sensing. By virtue of the p-n heterojunctions, efficient gas sensors for detecting H_2, [96] acetone, [97] trimethylamine, [100] ethanol, [98, 99] CH_4 [110] and NO_2 [17] have been reported. For example, Kim and coworkers [103] examined the Cr_2O_3 nanoparticle-functionalized SnO_2 nanowires for detection of both reducing and oxidizing gases (Fig. 7.18). They found that both pure and functionalized SnO_2 exhibited the highest response to NO_2 at 300 °C in the range of 200–400 °C. The Cr_2O_3/SnO_2 nanowires have a resistance of 5 to 10 times larger than those of the pure SnO_2. This indicates that the electron depletion layer of SnO_2 nanowires is further expanded by the creation of Cr_2O_3/SnO_2 p − n heterojunctions. Notably the Cr_2O_3/SnO_2 nanowires showed greatly improved sensing capabilities to reducing gases (Fig. 7.18c), however, the Cr_2O_3 functionalization was found to deteriorate the oxidizing gas sensing properties of SnO_2 nanowires (Fig. 7.18d).

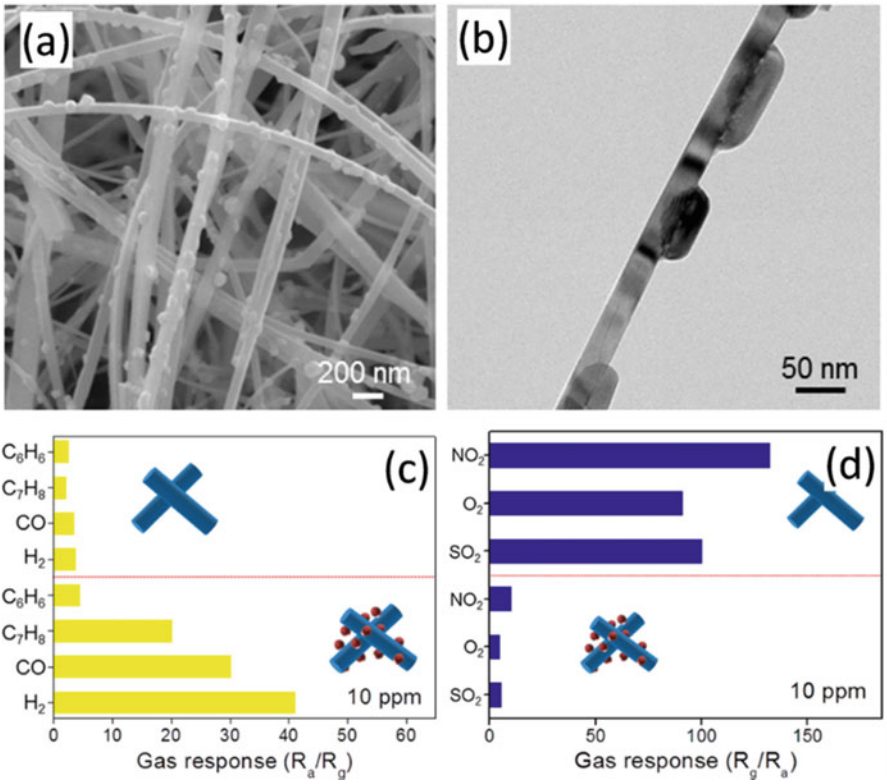

Fig. 7.18 (**a**) SEM and (**b**) TEM images of p-n Cr_2O_3/SnO_2 nanowires, and gas responses to 10 ppm of various gases (**c**) reducing and (**d**) oxidizing gas. Reproduced from ref. [103] with permission. Copyright 2014, American Chemical Society

Hieu and coworkers [104] have applied NiO/SnO_2 nanowires to detect H_2S. The p-n heterojunctions were found to decrease the optimum operating temperature from 350 °C for pure SnO_2 nanowires to 300 °C. Significantly, the NiO/SnO_2 nanowires have a response of 1372 to 10 ppm H_2S, which is 351 higher than that (3.9) of pure SnO_2. Based on the NiO/SnO_2 nanowires, a low concentration of 100 ppb H_2S is also detectable. Such a giant enhancement of H_2S response was attributed to the unique sensing reactions. Upon exposure to H_2S gas at elevated temperatures, the NiO nanoparticles are primarily converted to metallic Ni_3S_2, which is an effective electrical conductor. The formation of metallic Ni_3S_2 can destroy the p-n junction, thus causing a significant decrease in the electrical resistance. A similar mechanism was also widely accepted for CuO-functionalized nanowires for H_2S detection [95, 101, 106, 108], where the formation of metallic CuS greatly altered the sensor resistance during the sensing reactions. Consequently, this mechanism can be used to design H_2S gas sensor materials with a specific selectivity.

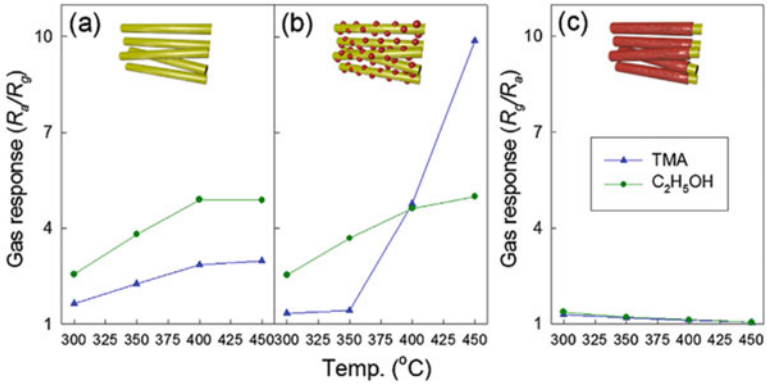

Fig. 7.19 (**a**) Gas responses to 5 ppm C_2H_5OH and 5 ppm trimethylamine at 300–450 °C: (a) pristine SnO_2 nanowires, (**b**) Cr_2O_3-decorated SnO_2 nanowires, and (**c**) core–shell Cr_2O_3/SnO_2 nanowires. Reproduced from ref. [129], Copyright 2014, with permission of Elsevier

Lee and coworkers [129] have shown that Cr_2O_3-decorated SnO_2 nanowires prepared by thermal evaporation were highly sensitive and selective to trimethylamine (Fig. 7.19). The authors found that at temperature of 450 °C the SnO_2 nanowires functionalized with discrete Cr_2O_3 nanoparticles exhibited high response to trimethylamine, when the temperature is below 400 °C, the Cr_2O_3-decorated SnO_2 nanowires are more sensitive to ethanol. They also revealed that if the Cr_2O_3 nanoparticles formed a continuous shell on SnO_2 nanowires, the heteronanowires would lost the discrimination ability to both ethanol and trimethylamine with a negligibly low response. According to the authors, the selective sensing behavior to trimethylamine was attributed, apart from the p-n junction, to the catalytic activity of Cr_2O_3 nanoparticles to promote the selective detection of analyte gas.

7.4.3 Enhanced Sensing Performance of N-N Heteronanowires

In Table 7.3, it shows that the 1D n-n heteronanostructures can be used to detect H_2, NO_2, [112] butanol, [113] acetone, [114] and ethanol [115, 116]. The n-n heterojunctions can lead to enhanced sensor performances based on the chemical or electronic sensitization. For example, Kaneti et al. [113] have demonstrated that ZnO-decorated α-Fe_2O_3 nanorods exhibited excellent sensitivity, selectivity, and stability toward n-butanol gas at a low optimum temperature of 225 °C. Without ZnO functionalization the pure α-Fe_2O_3 nanorods are more sensitive at 250 °C. In particular, the ZnO/α-Fe_2O_3 nanorods has a higher sensitivity compared to pure α-Fe_2O_3 (4 times higher) and ZnO nanorods (2.5 times higher), respectively, as well

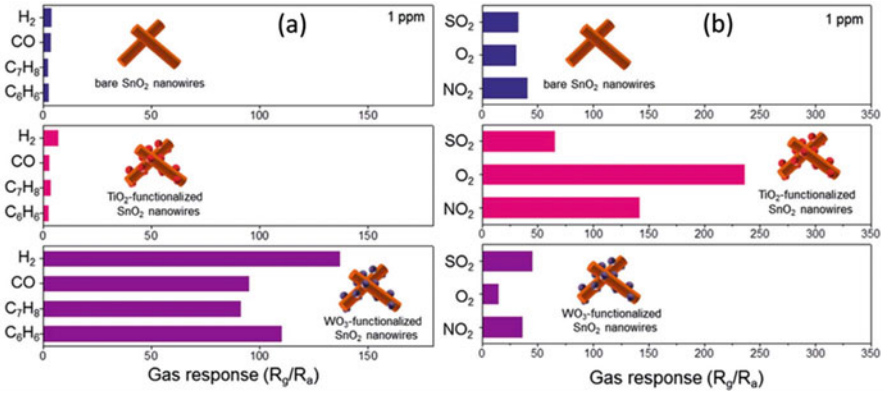

Fig. 7.20 (**a**) gas responses of WO_3/SnO_2 nanowires to 1 ppm various reducing gases and (**b**) gas responses of TiO_2/SnO_2 nanowires to 1 ppm various oxidizing gases (a) 5 ppm trimethylamine at 300 °C. Reproduced from ref. [117] by permission of the Royal Society of Chemistry

as faster response times. In another work from Li et al. [120], it was reported that ZnO nanoparticles improved the response of SnO_2 nanotubes to oxidizing gases, while declined the response to reducing gases. Specifically, the response of ZnO/SnO_2 sensor (1.44) to H_2 was almost nearly one-fifth of the pristine SnO_2 (6.89). While for the oxidizing gas like NO_2, the ZnO/SnO_2 heterojunctions present remarkably enhanced response, being six times higher response (30.84) than that (5.09) of pure SnO_2.

Kuang et al. [110] fabricated a FET gas sensor based on a single SnO_2 nanowire, which was selective to H_2S detection. They showed that at 250 °C the ZnO nanoparticle functionalization could improve the sensor sensitivity to 500 ppm H_2S from 1.26 to 1.50, but in contrast the sensitivity to CO decreased from 1.15 to 1.08, and negligible influence was observed for CH_4.

An acetone sensor with much enhanced response was reported by Lee and coworkers [118]. The good performance was derived from the Fe_2O_3 functionalization of In_2O_3 nanowires. According to the authors the n-n heterojunctions had no effect on the optimum operating temperature, as both pristine and Fe_2O_3 functionalized-In_2O_3 nanowires showed the best response at 200 °C.

Kim et al. [117] recently reported that a selective detection of reducing or oxidizing gases could be realized by functionalizing n-type SnO_2 nanowires with WO_3 or TiO_2 nanoparticles (Fig. 7.20). The key lies in the difference in the work functions of the host nanowires and guest nanoparticles. Specifically, the authors found that the WO_3/SnO_2 nanowires exhibited greatly improved response to reducing gases including H_2, CO, C_7H_8, and C_6H_6. On the other hand, TiO_2 nanoparticles enhanced the oxidizing gas-sensing properties of SnO_2 nanowires. These results are closely associated with the electron flow caused by the work function difference, leading to either compression or expansion of the conduction channel of SnO_2 nanowires along the radial direction. This work intensifies the resistance modulation

of nanowires selectively to either reducing or oxidizing gases, respectively. The approach proposed in this study may contribute significantly to the design of more sensitive nanowire sensors.

7.5 Summary

In this chapter, the utilization of metal oxide nanowires functionalized by metal and metal oxide nanoparticles as the sensing layer for gas sensors has been reviewed. Nanowires with some essential merits such as 1D structure, high crystallinity and tunable diameter are ideal building blocks for gas sensing devices. Due to the large amount of studies published with respect to nanowires and gas sensors, this chapter doesn't attempt to include all the papers to give a complete review. In contrast, a brief overview of gas sensing mechanism and the concept that improve the sensing performances of nanowires, i.e., nanoparticle functionalization, were present. It is concluded that nanoparticle functionalization is an effective method to optimize the sensor performances through either chemical sensitization or electronic sensitization. However challenges are still remaining in this field.

Traditional gas sensing layers are formed by a large quantity of nanoparticles. The nanoparticle units are readily sintered under a long-term working at high temperatures, thus resulting in deteriorated sensor stability. In principle, nanowires offer a better stability compared to the nanoparticle morphology, this should contribute to an improved long-term stability However, it is noted that in most cases, the long-term sensing stability of heteronanowires has not been examined or proved. Thus future efforts are needed to characterize the long-term stability of heteronanowires sensors, especially working in a real operation condition.

Another factor that adds the risk of instability of gas sensors based on heteronanowires is from the nanoparticle promotors. Although the nanoparticle functionalization, as reviewed in this work, could afford significant improvement in sensor sensitivity, the small size of metal nanoparticles makes them unstable. For most metal-functionalized nanowires, a thermal process is usually necessary to stabilize the loading of metal on nanowires. This process is also required to decrease the structural defects in order to enhance the stability of the metal oxides. Thermal treatment or long-term working at a high temperature would lead to a coarsening and aggregation of the metal nanoparticle, thus decreasing the efficiency of chemical sensitization during gas sensing.

The uniform distribution of nanoparticles has a large influence on gas sensing properties of nanowires. The synthetic methods to load nanoparticle are of great importance to guarantee a uniform coverage of nanoparticles with a small size on nanowires. Efforts are still needed to develop more reliable methods.

The understanding of gas sensing mechanism is a central task for sensor scientists. For pristine metal oxides, the basics sensing mechanism has been established and well-understood for decades. However, for a complex system composing of more than two materials, the interactions between each constituents and gas

molecules are also becoming complex. This greatly adds the difficulty for researcher to clarify the gas sensing mechanism. It should be noted that even for the same materials system quite different result can be obtained. As discussed in the context, some works confirm the promotion effect of nanoparticle functionalization in enhancing the sensing performance to reducing gas, but suppressing the sensitivity to oxidizing molecules, while some works obtained an opposite result. Unfortunately, the reasons for such contradictory results are still not clear.

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Chapter 8
Silicon Carbide Nanowires and Electronics

Shanliang Chen, Weijun Li, Xiaoxiao Li, and Weiyou Yang

8.1 Introduction

One-dimensional (1D) nanoscale semiconductors, such as nanowires/rods, nanoneedles, nanotubes, and nanobelts, have attracted a huge amount of attention within the past decade owing to their dimensionality-dependent physical and chemical properties and promising applications in energy conversion, chemical sensing, field emitters, photodetector, etc. [1, 2, 3–6]. Theoretical calculations and experimental investigation indicated that the 1D nanostructures could be superior to those of bulk or thin films [7–10]. Many 1D nanoscale materials have been synthesized and investigated, such as carbon group, oxide group, and sulfide group materials [4, 11, 12]. Among the variety of 1D nanoscale populations, silicon carbide (SiC) nanowires had attracted a lot of interest because they play a crucial role as the building blocks in electronic, optoelectronic applications [13–15].

The manufacture of SiC nanowires with controlled configuration was a significant breakthrough providing a class of nanomaterials [16]. As far back as 1907, Round heralded the technological potential of SiC as an electrical material through his observations of its yellow and blue luminescence which signaled its major technological advantage as a wide bandgap semiconductor [17]. Janzen et al. have discussed the properties of SiC that make it a superior semiconductor to Si for fabricating the device that works under harsh condition of high power, high temperature, and high frequency [18]. These superior properties have since the 1950s attracted scientists' interest to use SiC as a replacement for Si in the microelectronic industry. The difficulty in producing high-quality SiC single crystals from which to cut wafers has hindered its large-scale use in the microelectronics industry. However, researchers have overcome this essential problem in the 2000s, and if this

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development can be carried forward, it could spawn a wide range of improved devices [19].

SiC nanowires with various configurations, such as nanoarrays, core-shell, and some complicated structures, have been synthesized and attracted a lot of research interest due to their shape-induced unique electrical and optical properties [13, 14]. Compared with the bulk and micro-sized SiC structures, SiC nanowires have novel mechanical, electrical, and optical properties as a result of their reduced size [20–22]. Pan et al. reported that SiC nanowires have a very low electron emission threshold and are thus promising for vacuum microelectronics application [23]. Yang et al. confirmed that SiC nanowires can reinforce effectively the strength and toughness of ceramic composites [24]. Thus, up to now, the need to synthesize and understand SiC nanowires is of great importance for use in high-power, high-frequency, and high-temperature nanodevices [25–27].

In this chapter, we will provide a comprehensive review of the state-of-art research activities related to SiC nanowires, including their morphologies and potential electronics applications. We begin with a survey of SiC nanowires with various morphologies and corresponding synthesis methods and experimental parameters. Using various facile techniques, the SiC nanowires had been synthesized under specific growth conditions so far. This will be followed by the main objective of the review which is the prospects of diverse SiC nanowires in various functional devices. The recent progress on the improvement of their properties and finding novel potential electronics applications, such as the latest achievements in using various SiC nanowires as field emitters, supercapacitors, field-effect transistors, photocatalyst, and pressure sensors, will be highlighted.

8.2 Synthesis and Design of SiC Nanowires

Nanowires have stimulated an increasing interest due to their importance in basic scientific research and potential technological applications [2, 28]. The combination of the intrinsic properties of SiC with 1D nanostructure morphology, SiC nanowires offers numerous promising applications [13, 14, 29]. It is generally accepted that SiC nanowires with designed shape and high aspect ratio nature are ideal systems for exploring numerous novel phenomena at the nanoscale and investigating the size and dimensionality dependence of functional properties. They are also expected to play important roles as both interconnects and the key units in fabricating electronic, electrochemical, optoelectronic, and electromechanical devices with nanoscale dimensions [30–33]. Several kinds of conventional SiC nanowires as well as other novel configurations such as hierarchical nanoarchitectures, beaded nanochains, bamboo-like, twinned, bicrystalline, core-shell structures nanowires, high-ordered nanowires arrays, etc. have been reported in the literature, as shown in Fig. 8.1. In this section, we present some typical recently developed processes for the synthesis of SiC nanowires and their structural characterizations.

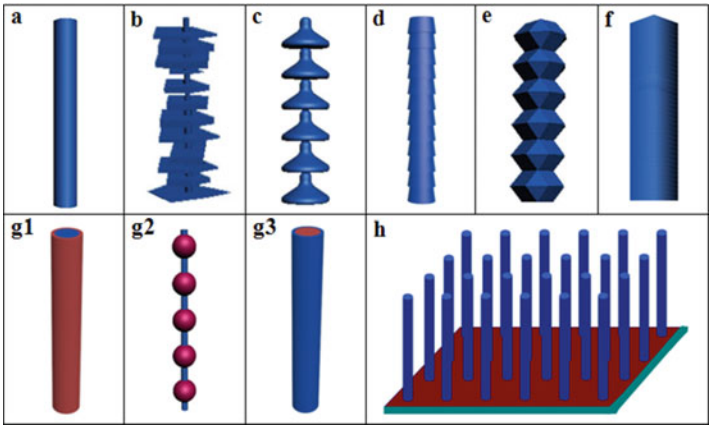

Fig. 8.1 Schematic summary of various morphologies of SiC nanowires reported in the literature. (**a**) Typical nanowires [28], (**b**) hierarchical nanoarchitectures [34], (**c**) beaded nanochains [35], (**d**) bamboo-like [36], (**e**) twinned [37], (**f**) bicrystalline [38], (**g**) core-shell structures (including the (**g1**) SiC-core-based nanocables [39], (**g2**) nanochains [40], and (**g3**) SiC-shell-based nanocables [41]), and (**h**) nanoarrays [42]

In our group, SiC nanowires as well as other typical 1D nanostructures with various morphologies have also been achieved. Most of the SiC nanostructures are fabricated via a vapor-phase route, which can be described as a one-step pyrolysis of polymeric precursor [42–45]. During the cooling stage, a crystal is grown by depositing the SiC seed accumulated directly from a vapor or gaseous state based on the vapor-liquid-solid (VLS) and/or vapor-solid (VS) mechanisms. There are several key parameters such as the material of a precursor, catalysts (including catalyst species, amount, and spatial distribution), temperature, carrier gas (including gas species, composition, and flow rates), bias pressure, evaporation time, cooling rates, and substrates (including substrate types and surface crystal structures) that can be controlled and needed to be selected properly before and during the growth process. In principle, it is possible to construct any desired morphologies, spatial distribution, and doping levels by precisely controlling the mentioned synthesis conditions [46–49]. Figure 8.2 displays the typical morphologies of SiC-related 1D nanostructures, such as nanowires as well as nanorods, nanoneedles, core-shell nanochains, and nanoarrays, which have been synthesized in our laboratory. Keeping in mind several representative works would be discussed in the following sections, herein we won't cover those in detail.

8.2.1 SiC Nanowires Growth in Vapor

Vapor-phase synthesis is probably the most extensively explored approach to fabricate SiC nanowires. There are several key parameters such as the temperature

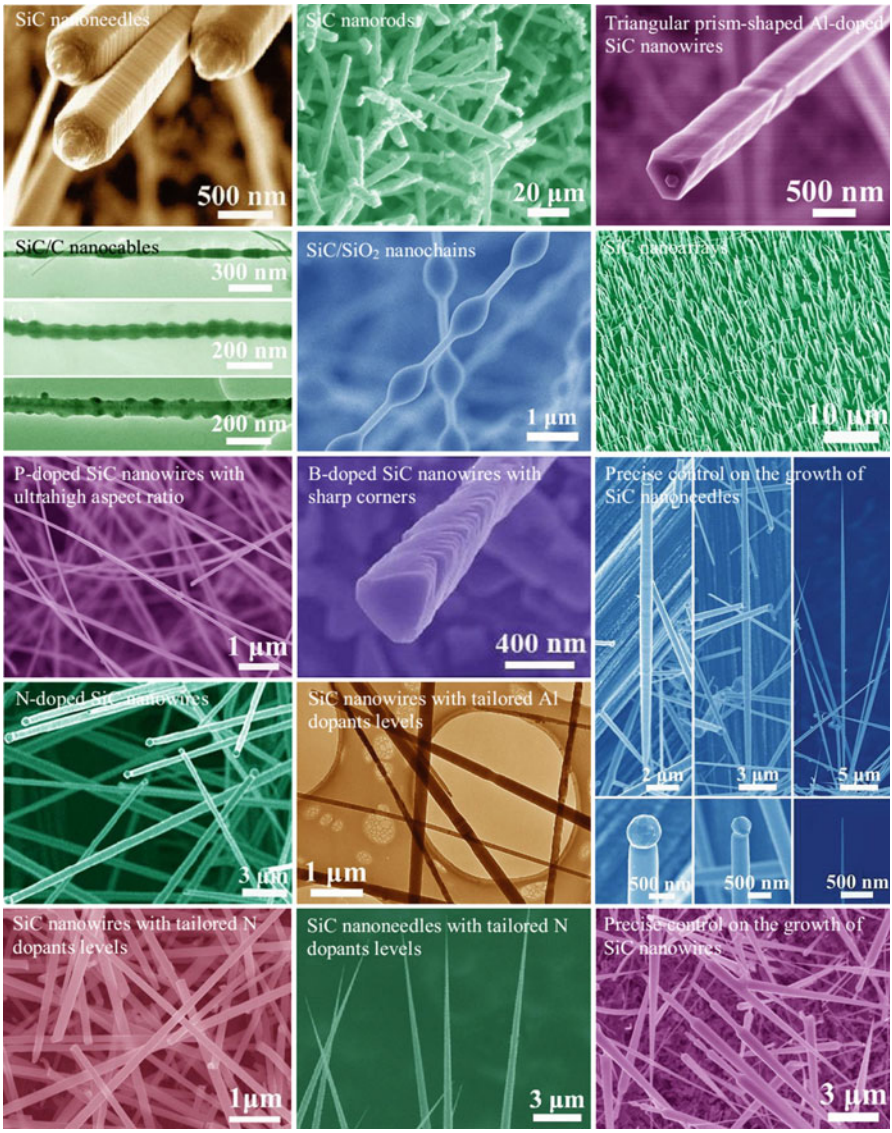

Fig. 8.2 Several typical morphologies of SiC-related 1D nanostructures fabricated in our laboratory

[28, 50, 51], heating rate [48, 52], bias pressure [47, 53], carries gas [46], and substrate type [54] that can be controlled and need to be properly selected before or during the vapor-phase synthesis. Several techniques have been assigned to vapor-phase processes, such as pyrolysis of polymeric precursor, chemical vapor deposition (CVD), carbothermal reduction, and thermal evaporation, which are utilized for

the growth of SiC nanowires, as summarized in Table 8.1. Basically, all these methods are governed by two typical categories: the VLS and VS mechanisms.

8.2.1.1 VLS Growth

For a typical VLS growth route, which was first proposed for the growth of silicon whiskers, metal nanoparticles are exploited as the catalysts to direct the nanowires growth. Such a process involves the formation of catalyst droplets at a high temperature, the adsorption and dissolution of gaseous precursors, and the precipitation of solid nanowires after saturation [73]. Clear evidence for the VLS growth is the existence of metal nanoparticles attached on the tips of the formed nanowires. During this process, the diameters and final shapes of the resulted nanowires can be conveniently controlled by tailoring the size of the catalyst droplets.

Figure 8.3 shows the schematic illustration of SiC nanowires synthesized from a VLS process by pyrolysis of polymeric precursor in our group [52]. The Co alloy droplets were utilized as the catalysts. The growth of SiC nanowires with catalyst nanoparticles attached on the tips or unique clean and sharp tips could be achieved, respectively, by controlling the catalyst droplets though precisely tailoring the cooling rates over the high-temperature pyrolysis process. It should be noted that the sizes of the catalytic droplets are determined by two competition cases, i.e., the dissolvability and vaporization of the catalytic droplet induced by the changes of the temperature. A faster cooling rate suggests a higher supersaturation, leading to a faster reduce in catalytic droplets sizes; and a faster cooling rate implies a lower vaporization induced by the high temperatures, resulting in a slower reduce in catalytic droplets sizes (schematically shown as step V and VI in Fig. 8.3) [52]. The different sizes of the catalytic droplets make the growth of the wire tips with different sharp degrees and final shapes. In addition to the cooling rates, the sizes of the catalytic droplets are also determined by the catalyst's amount and spatial distribution [49], temperatures [28], carrier gas (including gas species, composition, and flow rates) [46], bias pressure [53], and substrate's surface properties [42].

Another typical example for catalytic droplets size determined the morphologies of formed SiC nanowires during the VLS process is the production of SiC nanowires with multistage structures [48, 53]. Wang and co-workers demonstrated a pyrolysis of polymer precursor technique to precisely manipulate and control the morphology of VLS grown SiC nanowires through tailoring the catalyst droplets size by means of varying the pressure of the source species [53]. In this synthetic method, the fabrication of SiC nanowires with varied morphologies could be achieved by altering the pressure via changing Ar pressure during synthesis [53]. For example, as Fig. 8.4 shows, the morphology and diameter of SiC nanowires could be controlled by repeating pressure increasing/decreasing cycles. The spindle-shaped section is formatted during the first pressure cycle. Subsequently, a longer synthesis time is allowed, which leads to an increase of the wire diameter due to the pressure recovery. Finally, at an even longer synthesis time between the second and third pressure drops, a section of nanowires with a constant diameter is obtained (Fig. 8.4c).

Table 8.1 Synthetic routes for SiC nanowires in vapor process

	SiC nanostructures	Synthesis methods	T (°C)	Refs.
Nanowires	C-decorated SiC nanowires	Chemical vapor reaction	1250	[55]
	β-SiC nanowires	Chemical vapor reaction	1250	[56]
	Tapered SiC nanowires	Chemical vapor deposition (CVD)	1500	[57]
	β-SiC nanowires	Carbothermal reduction	1300	[33]
	3*C* and 4*H*-SiC nanowires	CVD process	1150	[58]
	β-SiC nanowires	Chemical vapor reaction	1250	[59]
	β-SiC nanowires	Pyrolysis of polysilazane	1300	[60]
	SiC nanowires	Vapor-solid reaction	1100	[61]
	β-SiC nanowires	Thermal heating process	1250	[62]
	Twinned SiC nanowires	Carbothermal reduction	1300	[63]
	SiC nanowires/ nanorods	Thermal heating process	1700	[21]
	Bamboo-like SiC nanowires	Thermal evaporation	1350	[36]
	Carbon-coated SiC nanowires	Carbothermal reduction	1000–1100	[64]
	BN-coated SiC nanowires	Thermal confined reaction	1400–1600	[65]
	Oriented SiC nanowires	Thermal evaporation	1400	[23]
	SiC nanowires	CVD process	1000	[66]
SiC-related 1D nanostructures fabricated in our laboratory	Au-decorated SiC nanowires	Pyrolysis of polysilazane	1500	[67, 68]
	3*C*-SiC nanowires	Pyrolysis of polysilazane	1500	[48]
	3*C*-SiC mesoporous fabrics	Electrospinning and pyrolysis process	1400	[69]
	β-SiC nanorods	Pyrolysis of polysilazane	1700	[70]
	SiC/SiO_x nanochain heterojunctions	Pyrolysis of polysilazane	1400	[71]
	SiC/C nanocables	CVD process	1300	[72]

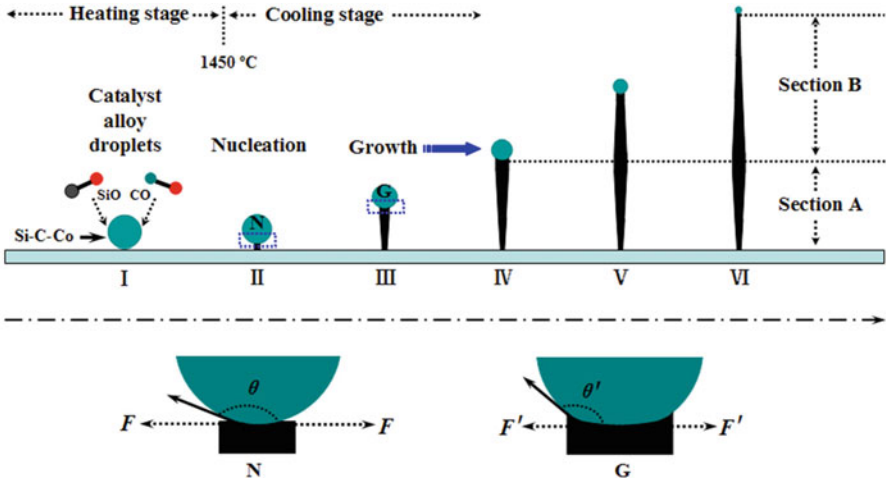

Fig. 8.3 Schematic illustration for the growth of SiC nanowires with tailored morphologies based on the VLS mechanism. (Reproduced from Ref. [52] by permission of the Royal Society of Chemistry)

8.2.1.2 VS Growth

In contrast to the VLS growth, the VS process does not require any metal catalysts for facilitating the nanowire growth. The growth of the nanowires via the VS process is mainly governed by the crystallographic nature of the nanowire material [73]. In such a process, nanowires usually grow along the direction in which the crystal plane has the lowest energy [62, 74, 75].

Wu and co-workers reported the fabrication of 3*C*-SiC nanowires by a catalyst-free vapor deposition method based on VS process using elemental Si and graphite carbon as the starting materials [50]. They confirmed that the morphology of the SiC nanowires can be tuned to cylinder, hexagonal prism, or bamboo shape by simply altering the reaction temperature from 1470, 1550, and 1630 °C, as shown in Fig. 8.5a–c. These nanowires have uniform growth directions along the [111] directions of the cubic SiC phase (Fig. 8.5d). The surface energy minimization combined with growth kinetics is responsible for the formation of the different morphologies of these nanowires [50]. It is well known that the (111) crystal plane of the 3*C*-SiC is the most densely packed plane with the lowest energy, so the nanowires tend to grow along these planes. The final shapes of SiC nanowires produced via the VS mechanisms can also be precisely tuned by varying the preparation parameters, such as substrates [62], source material [34], bias pressure [76], etc.

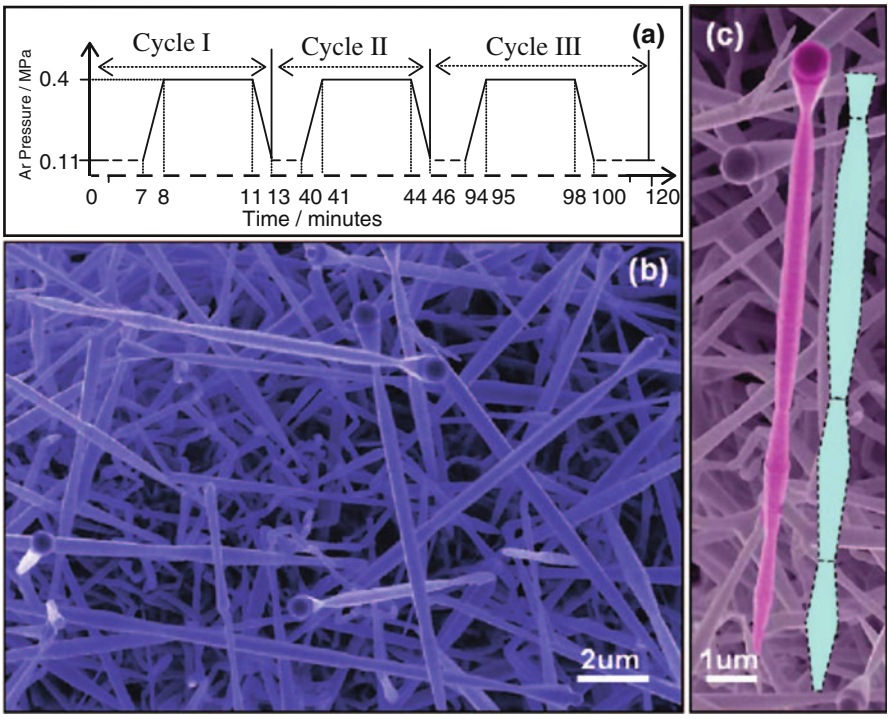

Fig. 8.4 (**a**) Processing schedule showing the pressure change as a function of time. (**b**) SEM image of SiC lathes using the processing described in (**a**). (**c**) High-magnification SEM image of the lathes. (Reprinted with the permission from Ref. [53]. Copyright 2008 American Chemical Society)

8.2.2 SiC Nanowires Growth in Liquid

Conventionally, one of the disadvantages of high-temperature-assisted (above 800 °C) approaches to nanowires synthesis, such as the vapor method mentioned above, is the high cost of fabrication and scaling-up, which, however, exceeds the operation window for most of the organic materials. Therefore, finding low-temperature synthetic routes to SiC nanocrystals is an effective approach to reduce the industrial cost.

8.2.2.1 Solvothermal Method

In the twenty-first century, solvothermal (using non-water as solvents) technology is not just confined to the crystal growth or leaching of metals, but it is going to take a very broad shape covering several interdisciplinary branches of science. It links all the important technologies like geotechnology, biotechnology, nanotechnology, and advanced materials technology [77]. The solvothermal method has been

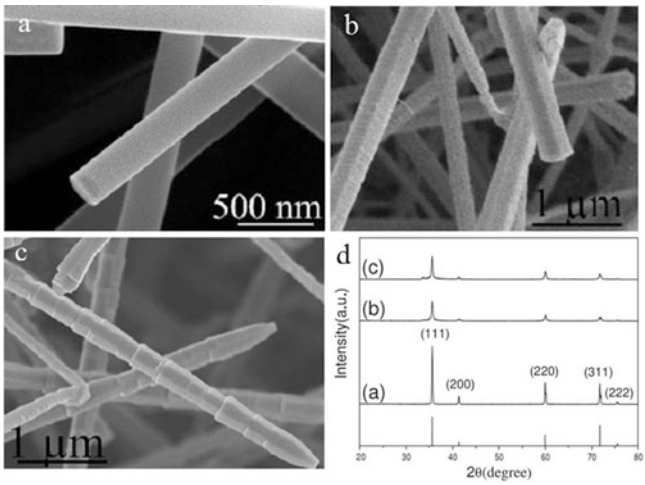

Fig. 8.5 The growth of 3*C*-SiC nanowires with different morphologies based on the VS mechanism ((**a**) nanocylinders, (**b**) nanoprisms, and (**c**) nanobamboos) and their XRD patterns (**d**). (Reprinted with permission from Ref. [50]. Copyright 2008 by the Institute of Physics Publishing. All rights reserved)

demonstrated to be one of the most important technologies for producing 1D nanostructures with well-defined crystalline morphology at low temperature [78]. It is environmentally benign and inexpensive and allows for reduction of free energies for various equilibria.

Recent progress using the solvothermal method has resulted in the creation of SiC nanowires/nanorods in high yields and large scales by using selective catalyst or reactants under low temperature. For example, Qian and co-workers reported the fabrication of β-SiC nanorods through a one-step reaction under pressure at 400 °C [79]. The reaction was carried out in an autoclave by using $SiCl_4$ and CCl_4 as reactants and Na as co-reductant. Then, they achieved β-SiC nanostructures via Mg-catalyzed chemical co-reduction route by using the $SiCl_4$ and 2-ethoxyethanol as the reactants in a stainless steel autoclave under 600 °C [80]. The reagent concentration plays an important role in the formation of SiC nanostructures with desired morphology. The nanorods with near-rectangular cross section translated into the ones with compressed cross section when more amounts of raw materials were added into the reaction system, respectively, as Fig. 8.6a, b shows. Generally, the nanorods are 80 nm wide, 30 nm thick, and 2 μm long. If less reagents are added into the reaction mixture, the final products are needlelike SiC nanostructures with sharp tips (Fig. 8.6c). This experimental phenomenon demonstrated that the shape-controlled synthesis of β-SiC nanostructures could be realized by adjusting the concentrations of the raw materials. More interestingly, in their follow studies, Qian et al. obtained the β-SiC nanowires under 130 °C by solvothermal method through a sulfur-assisted reduction route [81], which was almost the lowest reported temperature for fabricating the SiC nanowires in the solvothermal routes. However,

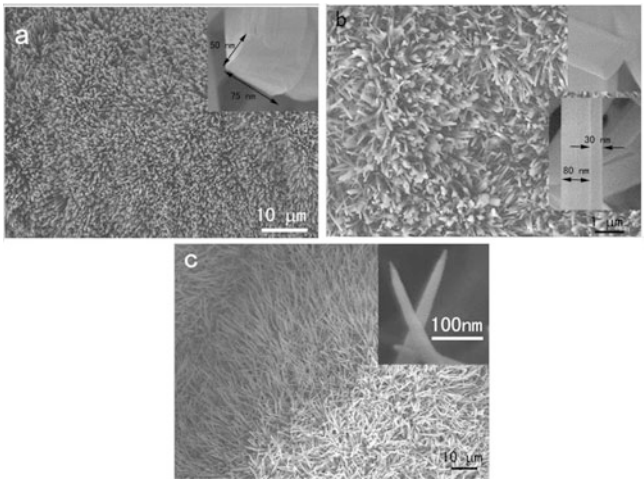

Fig. 8.6 Representative SEM images of the as-synthesized β-SiC samples: (**a**) nanorods with near-rectangular cross sections, (**b**) nanorods with compressed cross section, and (**c**) nanoneedles with sharp tips. (Reprinted with the permission from Ref. [80]. Copyright 2006 American Chemical Society)

the solvothermal process inevitable involved the high pressure, which would also hinder the realization of reliable synthetic SiC.

8.2.2.2 Electrochemical Etching

Electrochemical etching of single-crystal 4*H*/6*H*-SiC wafer had been proved to be another effective route for fabrication of SiC nanostructures. Different from the solvothermal method that required high pressure, the SiC nanostructures could be synthesized though the electrochemical etching route under room temperatures as well as atmospheric pressure [82–84]. The morphologies could be tuned by choosing appropriate condition, such as the etching voltage/current, electrolyte composition, etching time, and anode-cathode distance [85–88]. However, instead of SiC nanowires, most of the as-constructed products based on the electrochemical etching routes are mesoporous, nano-columnar in configuration. For emphasis, the fabrication of highly oriented SiC nanowires arrays would be discussed in detail in the "Aligned SiC Nanowire Arrays" section.

8.2.3 Doping of SiC Nanowires

To utilize semiconductor nanowires as building blocks of functional nanodevices, it is important to synthesize them by having in the end diverse physical properties. This

could be realized via appropriate doping. Recent advances in doped SiC nanowires have shown that their bandgaps and thus their physical properties can be tuned by incorporating the dopant atoms into the SiC nanowires [45, 89–91]. In order to attain the potential offered by SiC, both high-quality *n*- and *p*-type SiC nanowires are indispensable. It should be noted that, compared with liquid routes, the vapor for the growth of doped SiC could be more effective for the controlled growth of SiC nanowires in morphologies and *n*-/*p*-doping [46, 47, 92, 93].

8.2.3.1 *p*-Type Doping

The *p*-type doping of SiC nanowires via formation of substitutional solid solutions might favor a more localized state near the Fermi energy level, which could favor a more facile electron transfer from the Fermi level to the vacuum conduction band [34]. Our group fabricated *p*-type 6*H*-SiC nanowires with tailored Al-doping levels via a vapor route of pyrolysis of polymeric precursors with $FeCl_2$ as the catalyst [43]. The key in this synthetic process of metal Al-doping is the use of aluminum isopropoxide (AIP). The doping concentrations were controlled by tailoring the AIP concentration in the precursors (samples were synthesized by adding 0.2 wt%, 1 wt%, and 5 wt% AIP to precursors, respectively, referred to as PAS02, PAS1, and PAS5). Typical SEM images of Al-doped SiC nanowires that fabricated with different AIP are shown in Fig. 8.7a–d. The nanowires exhibit high-density growth and cylindrical shape with smooth surface. The average diameters are ~150, ~250, and ~300 nm (see Fig. 8.7b–d), and the measured Al concentrations are 0.52, 1.05, and 1.25 at% for the nanowires synthesized from PAS02, PAS1, and PAS5 (see Fig. 8.7d, e), respectively. The photoluminescence peaks of all samples show clear red shifts with increasing Al-doping concentration [43], suggesting that the optical properties of the SiC nanowires can be tailored by Al-doping.

Except for metal-doped SiC nanowires, the non-metal-doped *p*-type SiC nanowires are also much important, which are promising applications in the opto-electronic nanodevices [34, 94–96]. In our laboratory, the B-doped SiC nanowires were first grown via pyrolysis of polymeric route using polyureasilazane ($Si_{0.64}BC_{0.78}N_{1.53}O_{0.25}$) as the precursor material and B source and the high-purity Ar as the carrier gas based on the VLS growth [97]. The length and diameter of B-doped SiC nanowires were typically sized in ~10 μm and 500 nm, respectively. These nanowires possess a slowly tapered root and unique triangular prism-like body with numerous sharp corners around the edges, and their morphology remains similar to that of the undoped nanowires [97].

8.2.3.2 *n*-Type Doping

As compared to the *p*-type SiC nanowires, *n*-type ones are highly required with respect to their unique and excellent properties, and for the fabrication of PN heterojunctions with both *p*- and *n*-type doping, which is extensively used as the

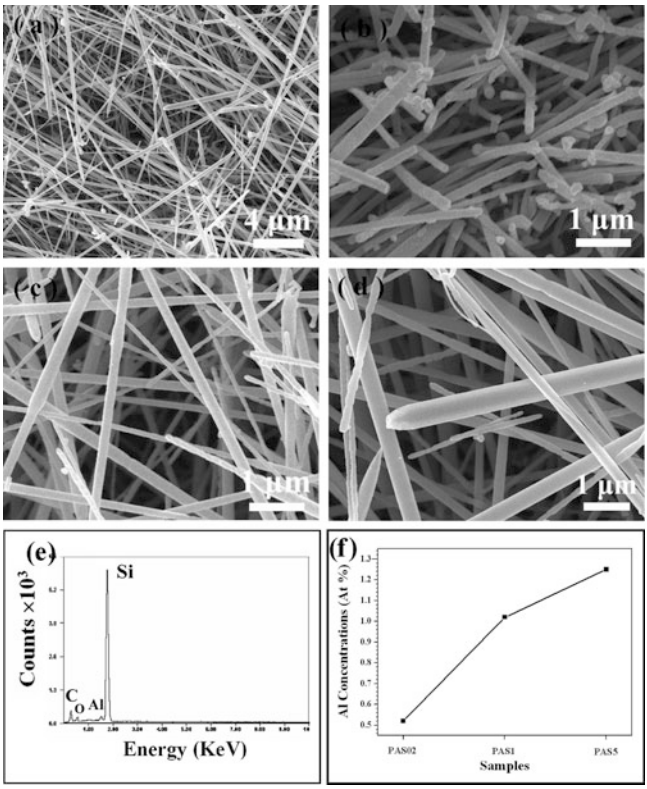

Fig. 8.7 (**a**) Low-magnification SEM image of the SiC nanowires obtained from PAS5. (**b**–**d**) High-magnification SEM images of the SiC nanowires obtained from PAS02, PAS1, and PAS5, respectively. (**e**) A typical EDS spectrum of the nanowires. (**f**) Al concentrations in different nanowires. (Reprinted with the permission from Ref. [43]. Copyright 2008 American Chemical Society)

functional unit in optoelectronic devices. For example, the *n*-type SiC nanowires could contribute more to promote the Fermi level with respect to the conduction, thus leading to a smaller work function and more effective enhancement on the electron emission [45, 92]. Furthermore, the thermoelectric properties of SiC nanowires can be significantly enhanced by N dopants [98].

Our group fabricated the *n*-type 3*C*-SiC nanowires with tailored N-doping levels based on the VLS growth via catalyst-assisted pyrolysis of polymeric precursors [47]. The mixture atmosphere of 5% N_2 and 95% Ar carrier gas was served as N source. The relatively low N_2 partial pressure played a determined role on the introduction of N dopants into the SiC nanowires. The pyrolysis temperatures had a profound effect on the morphologies and doping levels of N, enabling the tunable *n*-type doping of 3*C*-SiC nanowires with various configurations (see Fig. 8.8a1–c3). The N concentrations decreased from 10.14 *at%* to 4.12 *at%* with the increase of the pyrolysis temperatures from 1350 °C to 1450 °C, as Fig. 8.8d, e shows. This could

be attributed to the fact that a higher pyrolysis temperature could result in a lower dissolution of N within the liquid alloy droplets, which, in turn, leads to a lower doping level of N dopants in the final resultant SiC nanowires.

In our next study, the needle-shaped 3*C*-SiC nanowires with tailored N-doping concentrations were synthesized by controlling the N_2/Ar mixture atmosphere and cooling rate [46]. These nanostructures were quasi-aligned arrays, rather straight, and all presented ultra-sharp tips. The N concentrations of nanostructures were 4.39 *at%*, 6.01 *at%*, and 7.58 *at%* when the volume ratio of mixture atmosphere N_2/Ar in the pyrolysis procedure was carefully tailored at 5:95, 10:90, and 15:85 [46]. These works might provide a facile strategy for the growth of *n*-type SiC nanowires. Using the similar process, the P-doped SiC nanowires with ultrahigh aspect ratio have also been fabricated in our group, which exhibit a high yield with uniform spatial distribution of P dopants [45].

Other doped SiC nanowires, such as Fe-doped, Mn-doped, B-doped, N-doped, and P-doped, have been summarized in Table 8.2.

8.2.4 SiC Nanowires with Complex Morphologies

8.2.4.1 Hierarchical SiC Nanowires

Full control of architectures, sizes, morphologies, and patterns within crystals is an important theme in materials science since these parameters are the key elements that determine electrical and optical properties [103]. Hierarchical nanowire architecture is an important process for the fabrication of functional electronics nanodevices [104]. Many techniques have recently been developed to shape nanoscale materials into hierarchical nanoarchitectures, such as hierarchical ZnO nanostructure arrays with sixfold symmetries [105], hierarchical AlN nanoarchitectures [106], ZnS hierarchical nanostructures [107], and so forth.

The hierarchical SiC nanowires architectures have attracted researchers' attention due to their unique applications in nanotechnology. For example, Hou and co-workers fabricated the hierarchical B-doped 3*C*-SiC nanowires with a finned microstructure, and these unique nanoarchitectures make them attractive in application such as photocatalytic hydrogen production [34] and gas sensors [91]. Chen and co-workers achieved the hierarchical SiC nanowires by sol-gel carbothermal reduction method [108, 109]. The hierarchical SiC nanostructures exhibited an enhanced photocatalytic activity by accelerating the photocatalytic degradation of organic dye under visible light irradiation [108].

The hierarchical single-crystalline β-SiC nanoarchitectures have been synthesized using a catalyst-assisted thermochemical process under 1350 °C by Shen and co-workers [110]. The low-magnification SEM images shown in Fig. 8.9a and b display the formation of numerous strings made of platelet structures. Most of the nanoarchitectures are straight; however, some highly bent structures were also observed. The strings are 50–70 nm in diameter and several tens of micrometers in

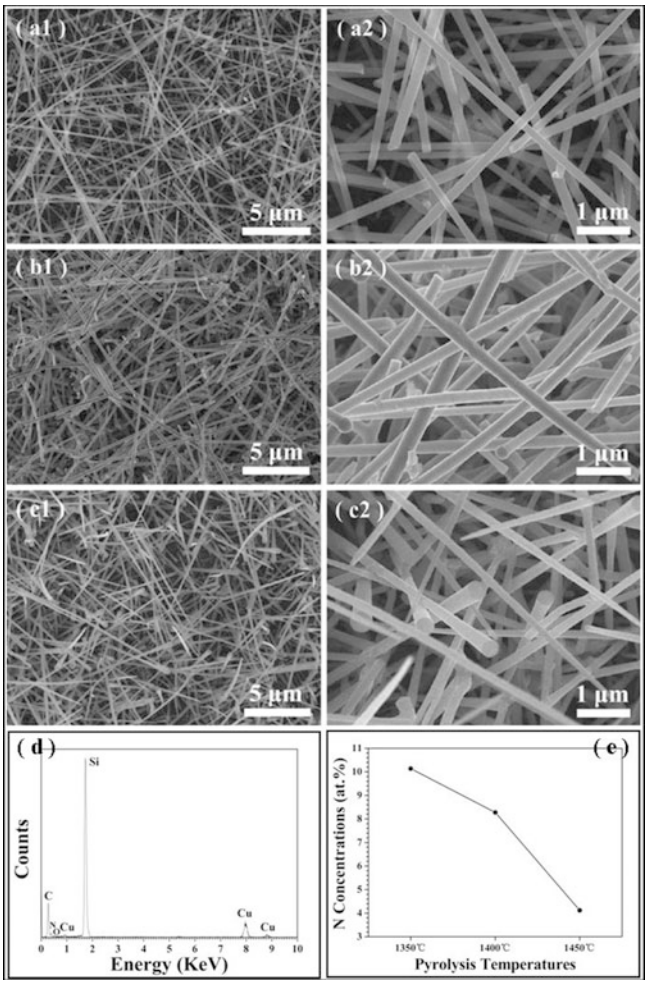

Fig. 8.8 Typical SEM images of SiC nanowires with various N-doping levels synthesized at 1350 °C (**a1**–**a2**), 1400 °C (**b1**–**b2**), and 1450 °C (**c1**–**c2**) under different magnifications. (**d**) A typical EDS spectrum of the SiC nanowires synthesized at 1350. The inset is an enlarged spectrum to show the signal of N dopants. (**e**) The relationship between the concentrations of N dopants and the pyrolysis temperatures. (Reproduced from Ref. [47] by permission of the Royal Society of Chemistry)

length. Closer examination (Fig. 8.9c and d) of the strings indicates that the platelets possess a well-preserved orientation relationship. All platelets grow out of the stems and are parallel to each other. Each platelet has a size ranging from 10 to 150 nm with the thickness of ~5–10 nm. The authors attributed the lack of evenness in the size of the individual platelets to the high reaction temperature and rapid growth [110].

Table 8.2 Representative doped SiC nanowires

	SiC nanowires	Synthesis methods	T (°C)	Refs.
Typical doped SiC nanowires	B-doped 3*C*-SiC nanowires with a finned microstructure	Carbothermal reduction	1500	[34]
	Fe-doped cubic SiC nanowires	Thermal heating process	1400	[89]
	Mn-doped 3*C*-SiC nanowires	Thermal heating process	1400	[99]
	Al-doped β-SiC nanowires	Pyrolysis of polysilazane	1550	[93]
	V-doped SiC nanowires	CVD process	950	[100]
Doped SiC nanowires fabricated in our laboratory	P-doped *3C*-SiC nanowires	Pyrolysis of polysilazane	1450	[45]
	Needle-shaped 3*C*-SiC nanowires with tailored N-doping levels	Pyrolysis of polysilazane	1450	[46]
	B-doped 3*C*-SiC nanowires	Pyrolysis of polysilazane	1550	[97]
	Needle-shaped N-doped SiC nanowires	Pyrolysis of polysilazane	1450	[25]
	N-doped β-SiC nanowires and nanoneedles	Pyrolysis of polysilazane	1450	[52]
	N-doped β-SiC nanowires	Pyrolysis of polysilazane	1500	[44]
	SiC nanowires with tailored N-doping levels	Pyrolysis of polysilazane	1450	[47]
	Al-doped triangular prism-shaped SiC nanowires	Pyrolysis of polysilazane	1450	[101]
	Needle-shaped Al-doped 3*C*-SiC nanowires	Pyrolysis of polysilazane	1400	[102]
	Al-doped 6*H*-SiC nanowires	Pyrolysis of polysilazane	1450	[43]

Based on the reported works, the conventional mechanism for the formation of these hierarchical SiC nanoarchitectures in vapor route could be attributed to a two-step epitaxial growth process, instead of the self-assembly of fused preformed pins or platelets [34, 109–111]. That is, the 1D SiC core stem were first rapid formed own to the high temperature, and then the epitaxial growth of SiC fins or platelets took place during the cooling process.

The typical hierarchical SiC nanowires synthesized in vapor and liquid routes are listed in Table 8.3.

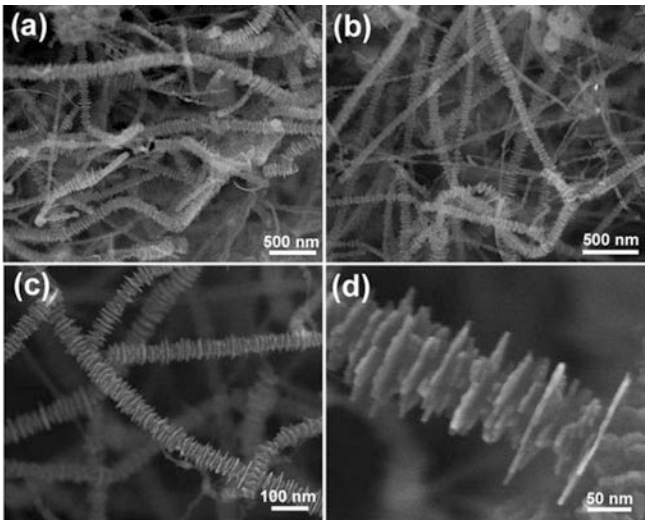

Fig. 8.9 SEM images with different magnifications of a SiC product. Those clearly indicate the hierarchical morphology in which every hierarchical nanoarchitecture is self-assembled revealing numerous thin nanoplatelets parallel to each other and perpendicular to the core stem. (Reprinted with the permission from Ref. [110]. Copyright 2007 American Chemical Society)

8.2.4.2 Beaded SiC Nanochains

Compared with common wire-like nanostructures having uniform profile, the beaded SiC nanochains, also called necklace-like nanowires, with diameter-fluctuating configuration, have been expected to achieve more excellent performance in various fields. For applications of SiC nanowires in composite materials, the strength of the material is strongly influenced by the interfacial strength between the filler and the matrix. Therefore, beaded SiC nanowires may have applications as reinforcing agents because the mechanical interlocking between beads and high specific surface areas can produce stronger interfacial adhesion.

Beaded cubic SiC nanochains are prepared from the carbothermal reduction of a carbonaceous silica xerogel with cetyltrimethylammonium bromide (CTAB) and lanthanum nitrate as additives by Hao and co-workers [35]. Figure 8.10 shows the typical TEM images of the SiC nanochains in a product. The nanochain presents an extremely straight configuration with a length of several microns (Fig. 8.10a), beads with a diameter of 150 nm (Fig. 8.10a), and a thinner stem with a diameter of 50 nm (Fig. 8.10b). The distance between two neighboring beads is 200 nm (Fig. 8.10a), which is almost invariable, and thus can be regarded as the period of the nanochain (L=200 nm). The nanochains have an amorphous SiC thin shell and grow along the [111] direction, as shown in Fig. 8.10c, d, and e, depicting that the concentration of stacking faults is higher in the beads compared with the stems. The authors reported

Table 8.3 Representative hierarchical SiC nanowires

Hierarchical SiC nanowires	Synthesis methods	T (°C)	Refs.
B-doped SiC nanowires with fin-like structure	Carbothermal reduction method	1500	[91]
B-doped SiC nanowires with a finned microstructure	Carbothermal reduction method	1500	[34]
Hierarchical 3*C*-SiC nanowires	Sol-gel carbothermal reduction method	1500	[108]
Hierarchical β-SiC nanodishes	Sol-gel carbothermal reduction method	1550	[109]
Hierarchical 3*C*-SiC nanostructures	Heating a milled Si and SiO_2 powder in the presence of ZnS	1450	[112]
Novel SiC nanoarchitectures	Thermal evaporation and solution strategies	1550	[113]
β-SiC nanowires with fins	CVD process	1350	[111]
Hierarchical SiC with a pagoda architecture	Anisotropic etching of SiC whiskers	RT	[114]

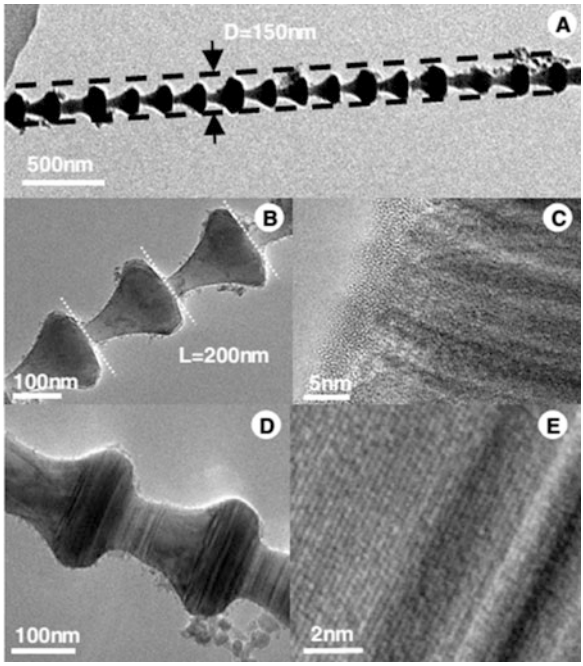

Fig. 8.10 (**a**), (**b**) TEM images of the alternately changed "stem-and-bead" structure of the nanochains. (**c**) Amorphous shell and the growth direction [111] of the nanochains. (**d**) Stacking faults are observed in the beaded nanochains. (**e**) HRTEM image of cubic SiC (left) and stacking faults (right). (Reprinted with permission from Ref. [35]. Copyright 2006 by the Institute of Physics Publishing. All rights reserved)

that the tensile strength increased by 32% for a beaded SiC-nanochain-reinforced epoxy composite [35]. Other typical reported beaded and/or necklace-like SiC nanowires may be found in Table 8.4.

Table 8.4 Representative beaded and/or necklace-like SiC nanowires

Beaded and/or necklace-like SiC nanowires	Synthesis methods	T (°C)	Refs.
Bead-chain-like β-SiC	Nanocarbon-dependent synthesis approach	1450	[115]
β-SiC nanochains	Chemical vapor reaction process by using AAO as the template	1230	[116]
Long β-SiC necklace-like whiskers	Carbothermal reduction of wood flour/silica/phenolic composite	1550	[117]
Necklace-like SiC nanowires	A simple CVD technique without any catalyst	1400	[118]

8.2.4.3 Bamboo-Like SiC Nanowires

Scientists have demonstrated that the peculiar diameter-fluctuation microstructures displayed specific mechanical properties when external force was loaded from the axial direction [9]. Therefore, similar with the beaded SiC nanochains, the bamboo-like SiC nanowires with fluctuated diameter were suitable to employ as the reinforcement owing to the stronger adhesion and interlocking caused by its contoured surface embedded in the matrix [119]. In addition, distinctive properties which stemmed from diameter-fluctuating and sharp-surface SiC nanowires, such as photoluminescence [120], microwave absorption [121], field emission [93], and mechanical properties [122], have also been reported, which were exciting the interest of researchers in the investigation of the peculiar nanostructures.

Single-crystalline bamboo-like β-SiC nanowires were synthesized by thermal evaporation of mixed SiO + C + GaN powders in an Ar atmosphere [36]. The nanowires present mean diameter of ~80–300 nm and lengths of up to several hundred micrometers, as shown in Fig. 8.11a. High-magnification SEM images of Fig. 8.11b–e give a clearer insight into the interesting bamboo-like configuration. In fact, all the bamboo-like SiC nanowires are of hexagonal cross section (Fig. 8.11f and i) with one plate tip (Fig. 8.11h) and one particle-attached tip (Fig. 8.11g). The particle-attached tips confirmed the bamboo-like nanowire growth is governed by the VLS mechanism. Studies found that the stems of bamboo-like nanowires are defect-free, while high-density stacking faults exist in the knot part and induce the periodical growth of larger diameter knots [36]. The authors demonstrated that the bamboo-like nanowires presented enhanced electron emission properties due to their highly faceted hexagonal cross sections and sharp corners [36].

Other bamboo-like SiC nanowires have also been synthesized as listed in Table 8.5.

8.2.4.4 Twinned SiC Nanowires

Twinning, a common crystal defect, is a type of stacking fault which has been regarded as an important microstructural defect in nanoscale materials. Twinning in SiC nanowires by VLS and VS mechanism has also been reported [125]. Wu and

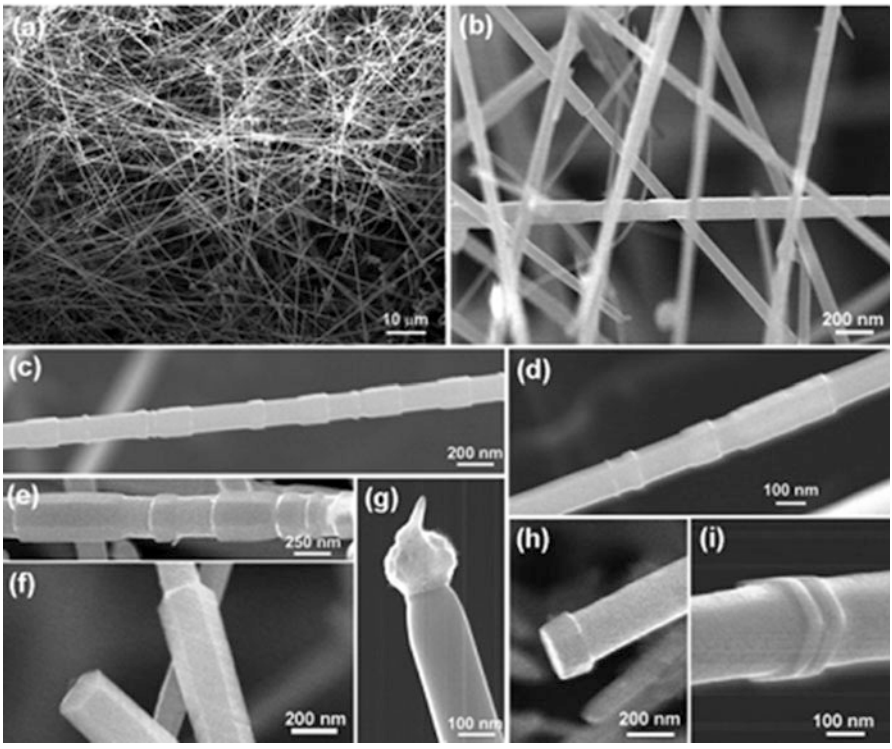

Fig. 8.11 SEM images of the bamboo-like SiC nanowires. (**a**) Low-magnification view, (**b**) high-magnification view. (**c**)–(**i**) High-magnification view, clearly indicating the formations of bamboo-like nanowires with hexagonal cross sections. Parts (**g**) and (**h**) clearly show that the SiC nanowire has one flat tip and one catalyst-attached tip. (Reprinted with permission from Ref. [36]. Copyright 2006 by the Institute of Physics Publishing. All rights reserved)

co-workers have synthesized twinned needle-shaped SiC zigzag nanowires by silicon evaporation on to multiwall carbon nanotubes at 1500 °C for 8 h [37]. Figure 8.12a shows a TEM image of a twinned SiC nanostructure, revealing a flat surface on one side and a zigzag surface on the other side. High-magnification TEM image of the flat end (Fig. 8.12b) and corresponding SAED along the [111] zone axis (Fig. 8.12c) show a serious streak of (202) plane reflections, further indicating the (111) plane stacking is somehow disordered along the length direction of the nanoneedle. The zigzag part shown in Fig. 8.12d and f exhibits a periodically angled profile, the angles are 141°, and the periodicity is about 50 nm. The corresponding SAED pattern (Fig. 8.12e) along the [110] from the zigzag part indexing the diffraction spots gives two symmetrical sets of face-centered cubic lattices, suggesting the zigzag part is composed of (111) twinning structures. By slightly tilting the zigzag nanowire in Fig. 8.12g, the 2D zigzag appearance turns into a 3D periodic microfaceting morphology as shown in Fig. 8.12h.

Table 8.5 Representative bamboo-like SiC nanowires

Bamboo-like SiC nanowires	Synthesis methods	T (°C)	Refs.
Bamboo-like 3*C*-SiC nanowires with fluctuating diameter	A simple chemical vapor reaction approach	1250	[120]
Bamboo-like β-SiC nanowhiskers	Molten-salt synthesis approach	1250	[121]
SiC nanowires with unique bamboo-like morphology	Catalyst-assisted pyrolysis of polysilazane	1550	[93]
Bamboo-like single-crystalline β-SiC nanowires	Catalyst-free carbothermal reduction approach	1500	[123]
Bamboo-like SiC nanowires	A catalyst-free vapor deposition method	1630	[50]
β-SiC nanowires with a bamboo-like structure	Carbothermal reduction of the carbonaceous silicon xerogel	1320	[22]
Bamboo-like SiC nanofibers	Carbothermal reduction of the carbonaceous silicon xerogel	1300	[124]

Strain is believed to be the principal driving force for the formation of the twins observed in SiC [126–128]. Wang et al. reported periodically twinned structures in 3*C*-SiC nanowires by the carbothermal reduction of a carbonaceous silica xerogel prepared from tetraethoxysilane (TEOS) and biphenyl with iron nitrate as an additive and thought the strain played a key role in determining the twinning structures [125]. They also pointed out that periodically twinning structures in 3*C*-SiC nanowires can influence their optical, electronic, mechanical, and chemical properties and in turn their performance [129].

Other twinned SiC nanowires have also been synthesized as listed in Table 8.6.

8.2.4.5 Bicrystalline SiC Nanowires

The bicrystalline SiC nanowires with different growth directions of <001>, <110>, <113>, or <112> have been reported [126, 135, 136]. Wu and co-workers synthesized SiC bi-nanowires (SiC BNWs) with a Y-shaped junction via chemical vapor reaction based on the VLS growth [38]. The SiC BNWs presented different growth directions and are all composed of two individual side branches, as Fig. 8.13 shows. The two branches are of about the same width and share one common axis, making the BNWs symmetrical. When the meeting angles between the two sets of {111} planes of the two nanowires are, respectively, about 109° ± 6°, 121° ± 6°, and 141° ± 6°, the growth directions of BNW can be indexed as the <110>, <113>, and < 112> directions, as shown in Fig. 8.13a, b, and d. Most interesting, for the [113] growth and [110] growth, the two side branches of a BNW contain many stacking faults and nanotwins (Fig. 8.13a and b), whereas for the [112] growth, the formed BNWs can be entirely free of any stacking faults and nanotwins, as shown partly in Fig. 8.13d and e. The formation of SiC NBWs with certain directions is based on the meeting angle and the radii of the two SiC single nanowires with <111> growing directions, and more detailed information can be found in Ref. [38].

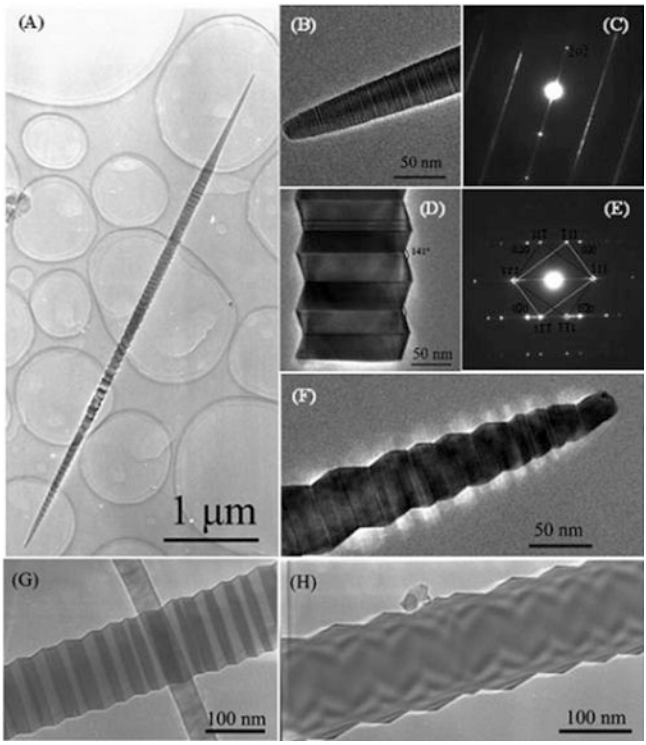

Fig. 8.12 (**a**) TEM image of the needle-shaped SiC nanowire displaying the flat surface of the upper part and the periodic zigzag surface of the lower part. (**b** and **c**) High-magnification TEM image and corresponding SAED pattern of the flat surface. (**d**) High-magnification TEM image of the zigzag surface in the middle of the nanoneedle. (**e**) The electron diffraction pattern along the [011] zone axis of the zigzag part, showing the well-defined (111) twinning relationship. (**f–h**) High-magnification TEM images of the zigzag surface of the nanoneedle. (Reprinted with the permission from Ref. [37]. Copyright 2007 American Chemical Society)

Table 8.6 Representative twinned SiC nanowires

Periodically twinned SiC 1D nanostructures	Synthesis methods	T(°C)	Refs.
Twinned SiC nanowires	A catalyst-free thermal CVD method	1500	[130]
Periodically twinned 6*H*-SiC nanowires with fluctuating stems	CVD process with ferrocene as the catalyst	1500–1600	[131]
Twinned β-SiC nanowires	A simple thermal evaporation method	1550	[132]
Twinned SiC nanowires	A catalyst-free pyrolytic deposition technique	800	[133]
Periodically twinned SiC nanowires	High-temperature thermal evaporation	1500	[134]

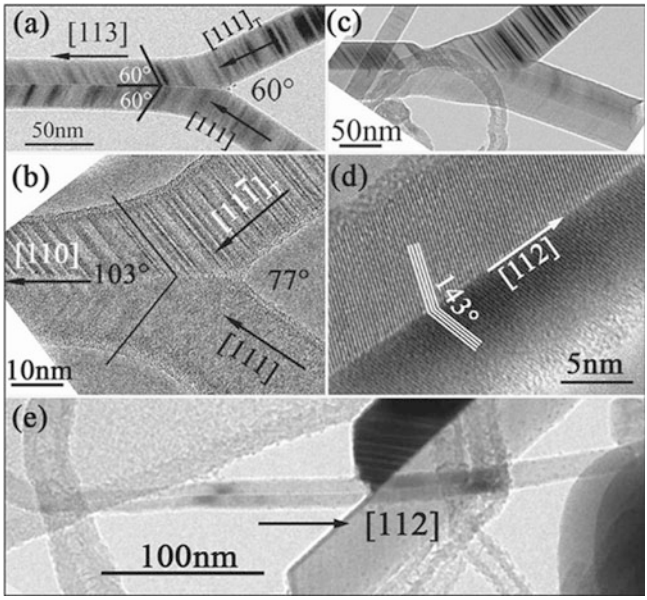

Fig. 8.13 TEM morphology of SiC BNWs with different growth directions. (**a**) The [113] axis, (**b**) the [110] axis, (**c**) a BNW formed from three nanowires, (**d**) and (**e**) the [112] axis. (Reprinted with permission from Ref. [38]. Copyright 2010 by the Institute of Physics Publishing. All rights reserved)

Furthermore, several formation mechanisms for bicrystalline SiC nanowires have also been proposed [126, 135]. For example, 3*C*-SiC bi-nanowires were produced by Seo and co-workers via carbothermal reduction using carbon black powder and silica powder as the starting materials [137]. It was observed that each nanowire consists of one leg and two heads and that the leg, growing along <001> direction and containing two branches, splits into two heads growing in two <111> directions. The authors speculated that the Y-shaped whiskers probably grew from the leg to the heads [137]. Bicrystalline SiC nanowires with uniform BN coating, synthesized by the VLS growth, were reported growing along the <311> axis by Tang et al. [138]. They believed that the bicrystalline nanowires split into two BN-coated SiC nanowires forming the Y-shaped junctions when [111] directions occurred, due to the bending of SiC nanowires. Wu and co-workers synthesized the bicrystalline SiC nanobelts via a reaction of Si and CNTs without catalysts using the evaporation method [136]. The bicrystalline structure is characterized by two parallel parts of SiC crystals with two growth directions, i.e., <121> and < 111>, splitting along the twin boundary that exists at the centerline.

8.2.5 *Coaxial Core-Shell SiC Nanowires*

Extensive efforts have been made to achieve reliable protection of various nanowires with thermally and chemically stable sheathes [139, 140]. An insulating and chemically inert protective shield can allow the inner material to display its natural protective shield and natural properties that are not affected by the environment.

The reported SiC coaxial core-shell nanowires, also called coaxial nanocables, or core-shell heterojunctions, had been extensive studied since last couple decades, and are fundamentally interesting and generation of devices with diverse functions [141–145]. Bechelany et al. presented a simple process for the fabrication of very long SiC-based nanocables with controlled coating thicknesses of 2–10 nm based on the VS growth mechanism [146]. The versatility of this technique is confirmed by the ability to change the chemical composition of the nanocables outer layer from silica to carbon and boron nitride [146]. Our study showed that SiC-C nanocables synthesized by a solid-liquid-solid (SLS) mechanism have a low resistivity of 1.6 Ω at room temperature, which was better compared to bare SiC nanowires of 47 Ω, thus providing a quick pathway for electron transportation [72]. Note that, based on the previous reports, the SiC coaxial core-shell nanostructures could be divided into two important parts, that is, the SiC-core-based core-shell nanowires and SiC-shell-based core-shell nanowires.

8.2.5.1 SiC-Core-Based Core-Shell Nanowires

Generally, the SiC-core-based core-shell nanowires were fabricated by coating a second material with a conformal layer on the surface of SiC core [147–149]. In the fabrication of these kinds of structures, one of the key points is to select a proper material as the outer layer, which can not only stabilize and enhance the optical and electrical properties of the SiC nanowires but also allow chemical surface functionalization to modulate the surface properties for further applications [72, 147]. Therefore, the selected outside coating layers are usually some wide bandgap, low (or negative) electron affinity, chemically stable, or dielectric materials [138, 150, 151].

The SiC/SiO_2 core-shell heterostructures (or SiC/SiO_2 nanocables) were synthesized with catalytic Mn-Si alloy particles by heating Si and SiO_2 powder mixtures (1:1) with a small amount of activated carbon powder under 1600 °C by Liu and co-workers [39]. The SiC/SiO_2 nanocables exhibit uniform diameters, which are in the range of 20–200 nm. A length of the nanocables can be up to tens of micrometers [39]. TEM images of the typical structure of SiC/SiO_2 nanocables are depicted in Fig. 8.14a and b, suggesting that the inner SiC wires with a diameter less than 50 nm are tightly wrapped by the outer uniform, tens of nanometers thick, SiO_2 layers. The inner SiC nanowires show obvious contrast variations of the stacking faults, either

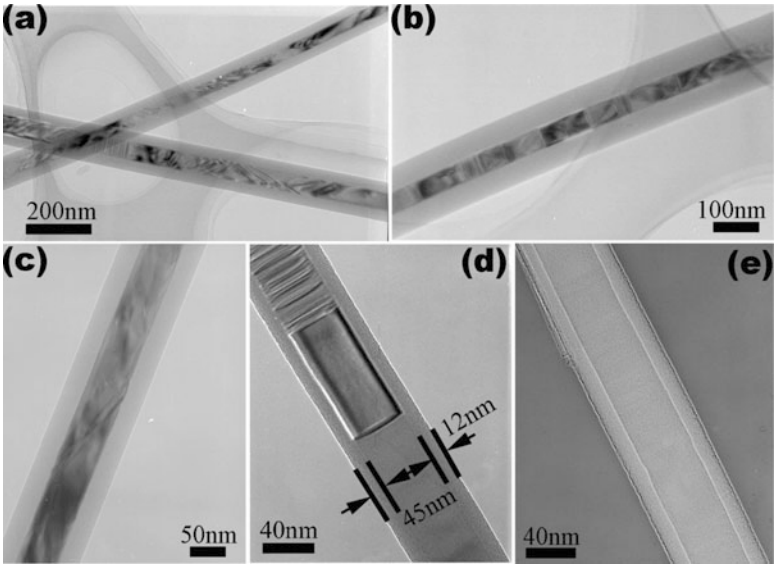

Fig. 8.14 (**a**, **b**) Representative low-magnification TEM images of SiC/SiO_2 core-shell nanowires with uniform diameters and wall thickness of the SiO_2 shells. The contrast difference highlights the stacking faults along the (111) plane. (**c**) Completely and (**d**) partially filled SiC/SiO_2 core-shell heterostructures and (**e**) an empty SiO_2 tubular structure. (Reprinted with the permission from Ref. [39]. Copyright 2008 American Chemical Society)

periodic, along the growth direction, or inclined with respect to it, as seen in Fig. 8.14a–d. An example of the inner SiC wire with some planar defects and a SiO_2 layer with a uniform thickness of ~12 nm is presented in Fig. 8.14d. The majority of SiO_2 nanotubes were completely filled with SiC nanowires to organize dense core-shell heterostructures, but there were also a small number of them only partially filled (Fig. 8.14e) or fully empty (Fig. 8.14e). These SiC/SiO_2 nanocables, together with Mn atoms solely located at the tip-end Mn-Si alloy particles, exhibit room temperature ferromagnetism and are valuable for novel magnetic nanodevices [39].

Respected to the SiC/SiO_x nanocables, achieve the thickness control of SiO_x coating is vitally important for their applications [152, 153]. Li and co-workers introduced a facile and environmentally friendly route to fabricate SiC nanowires with thickness-controlled SiO_2 shells, namely, treatment of SiC/SiO_2 core-shell nanowires in NaOH solution, which favored the core-shell structures with an optimum SiO_2 thickness that holds great promise for potential application [154]. The SiC/SiO_2 nanowires were preliminary fabricated. The authors derived a two-phase reaction kinetic equation to explain the rate of the removal of the SiO_2 shell, in line with the reaction:

$$SiO_2(s) + 2NaOH(aq) = Na_2SiO_3(s) + H_2O(aq) \quad (8.1)$$

The optimum reaction temperature was confirmed to be 70 °C, which could establish an optimum reaction rate of removal of the SiO_2 shell. The thickness of the SiO_2 shell can be controlled by adjusting the reaction time in the NaOH solution, and pure SiC nanowires were also obtained by alkaline cleaning in 1 mol/L NaOH solution for 40 min. The authors also confirmed that the accurate and effective control of the SiO_2 shell thickness plays a fundamental role in determining their photoluminescence properties [154].

Besides the examples discussed above, SiC-core-based nanowires, such as the SiC/SiO_x, SiC/Si, SiC/C, SiC/Al_2O_3, SiC/AlSiC, SiC/BN, and SiC/SnO_2, have also been synthesized, as shown in Table 8.7.

Besides the SiC-core-based nanocables with uniform diameter, the SiC-core-based nanochains, mainly the SiC/SiO_x nanochains, with fluctuated diameters are also one of the most important nanowire heterojunctions with excellent optical and electronic properties [40, 173]. Over the past several years, some progress has been made to prepare and evaluate the properties of SiC-core-based nanochains. Wei and co-workers synthesized SiC/SiO_2 nanochains composed of 3*C*-SiC strings and periodic SiO_2 beads via a microwave method and disclosed that the optical properties of the SiC nanowires could be tailored by the SiO_2 beads [74]. Meng and co-workers obtained SiC/SiO_2 with a chain structured homogeneous nanostructure by anodic aluminum oxide template (AAO)-assisted chemical vapor reaction process and attributed their growth to a speed alternating vapor-solid (SAVS) mechanism [116]. Bechelany et al. reported the high yield growth of SiC/SiO_2 necklace by the dewetting of SiO_2 on the surface of SiC annealed at 1400 °C under a nitrogen flow [174].

Up to now, the SiC/SiO_x nanochains are the most reported SiC-core-based nanochains. The typical mechanism for the formation of SiC/SiO_x nanochains, in line with previous reports, can be attributed to the Rayleigh instability and the poor wettability between SiC and SiO_x, and the SiO_x tends to be broken apart and assembled into spherical nano-droplets to minimize its surface energy and formed into the periodic beads [40, 71, 174].

Based on the reported works, the purity and yield issues are significant challenges for the practical application of SiC-core-based core-shell nanoheterojunctions in functional devices. Recently, the mass production of SiC/SiO_x nanochain heterojunctions via pyrolysis of polyvinylpyrrolidone and polyaluminasilazane precursors was achieved in our laboratory [71], with respect to the following reaction:

$$C(s) + CO_2(g) \rightarrow 2CO(g) \quad (8.2)$$

$$SiO(g) + CO(g) \rightarrow SiC(g) + CO_2(g) \quad (8.3)$$

Figure 8.15a, b are SEM images of the as-synthesized products, showing the purity and yield of the SiC/SiO_2 nanochains in the sample are estimated to be more than 95% and 40%, respectively. TEM images of the typical structure of nanocable

Table 8.7 Representative SiC-core-based core-shell nanowires

SiC-core-based core-shell nanowires	Synthesis methods	T(°C)	Refs.
SnO_2 nanosheets at SiC nanofibers	Hydrothermal method	1500	[155]
Core-shell SiC/SiO_2 nanowires	Chemical vapor reaction process	1400	[156]
SiC/SiO_2 core-shell nanowires	CVD technique	1000–1100	[149]
SiC@Si core-shell nanowires	A two-step CVD method	1051, 500	[144]
Ultra-long SiC/SiO_2 core-shell nanowires	Molten-salt-mediated carbothermal reduction route	1400	[157]
Core-shell SiC@SiO_2 nanowires	Thermal evaporation method	1500	[158]
SiC/SiO_2 nanocables	CVD process	1100	[159]
SiC/SiO_2 core-shell nanowires	CVD process	1020	[160]
SiC/SiO_2 core-shell nanocables	Microwave CVD process	500–1200	[161]
SiC/AlSiC core-shell nanowires	Porous alumina templates assisted plasma-enabled growth process	RT	[148]
SiC/SiO_2 core-shell nanowires	A low-cost carbothermal method	1050–1100	[162]
Al_2O_3-coating SiC nanotubes	Heating evaporation process	1270–1350	[150]
Core-shell SiC/SiO_2 nanowires	Carbothermal reduction method	1100	[143]
SiC/SiO_2 core-shell nanowires	A low-cost carbothermal method	1050–1100	[163]
SiC-C coaxial nanocables	Solvothermal process	~250	[164]
SiC/SiO_2 core-shell nanowires	Thermal decomposition of ethanol	1100	[165]
SiC/SiO_2 nanocables	Thermal CVD process	950	[166]
SiC/SiO_2 core-shell nanocables	Direct heating Si powders and MWCNTs	1450	[167]
SiC/SiO_2 core-shell nanowires	Chemical vapor reaction	1250	[168]
Ultrathin and ultra-long SiC/SiO_2 nanocables	Pyrolysis of poly(dimethyl siloxane)	1050	[169]
SiC/SiO_2 core-shell nanocables	Thermal evaporation method	1400	[170]
β-SiC/SiO_x nanocables	Arc-discharge method	RT	[171]
SiC-BN nanocables	Heating process using Si and In_2O_3 powder as source material	1600	[10]
Uniformly BN-coated SiC nanowires	Thermal evaporation based on the VLS growth mechanism	1400	[138]
Helical crystalline SiC/SiO_2 core-shell nanowires	CVD technique	1100	[172]

are depicted in Fig. 8.15c–e, suggesting that the nanochain is actually structured with a dark SiC core and a light SiO_x shell. The typical thickness of the SiO_x shell is ~210 nm and ~52 nm at the bead and chain areas, respectively. The SiC core has identical diameters (~180 nm) and goes through the beads along its length. The inset

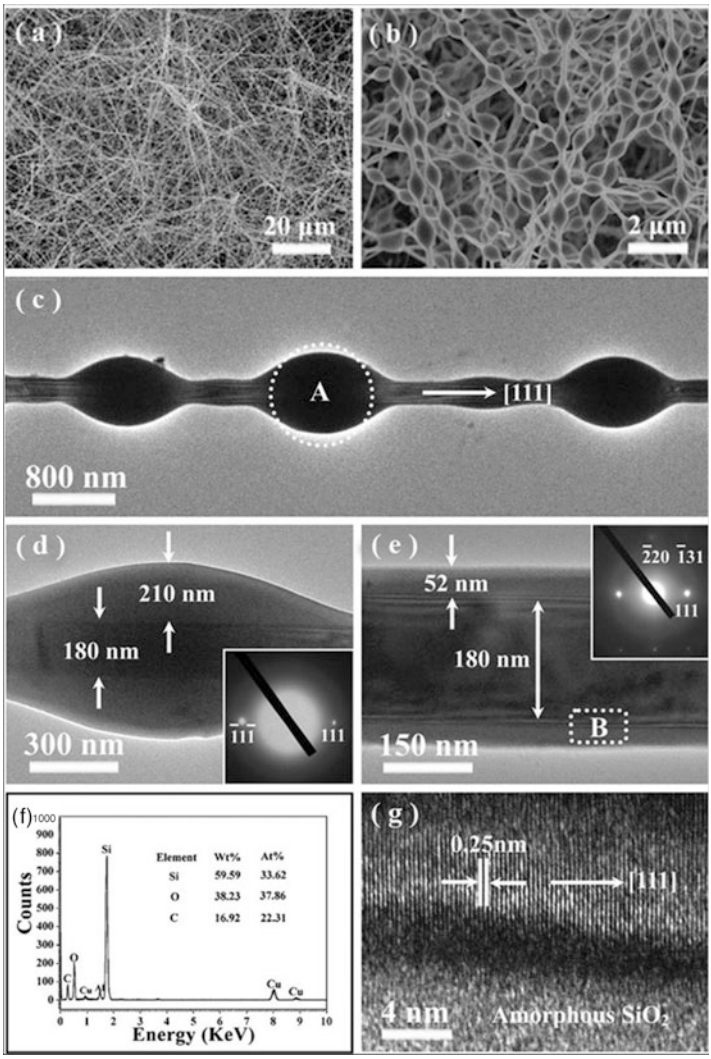

Fig. 8.15 (**a**, **b**) Typical SEM images of the as-synthesized SiC/SiOx nanochain heterojunctions under different magnifications. (**c**) A typical TEM image of a single SiC/SiO_x nanochain under low magnification. Closer observations of the (**d**) and (**e**) string under a high magnification. The insets are their corresponding SAED patterns. (**f**) A representative EDS spectrum of SiC/SiO_x nanochains recorded from the marked area A in (**c**). (**g**) A typical HRTEM image recorded from the marked area B in (**e**). (Reproduced from Ref. [71] by permission of the Royal Society of Chemistry)

SAED patterns of Fig. 8.15d and e implied the amorphous SiO_x shell and single-crystal 3*C*-SiC core of the nanochains. The EDS (Fig. 8.15f) result suggests the nanochains are SiC and SiO_x heterojunctions. Figure 8.15g is an HRTEM image of the marked area of B in Fig. 8.15e, which clearly reveals the lattice-resolved image

Table 8.8 Representative SiC-core-based core-shell nanochains

SiC-core-based core-shell nanochains	Synthesis methods	T(°C)	Refs.
Bead-curtain-shaped SiC@SiO_2 core-shell nanowires	Modified CVD process	1300	[173]
SiC/SiO_2 nanochains	Carbothermal reduction process	1500	[175]
Dumbbell-shaped biomimetic SiC/SiO_2 fibers	Carbothermal reduction method	1500	[176]
WZ-GaN/3*C*-SiC-core-shell heterostructure nanowires	Two-step CVD process	1400	[177]
SiC/SiO_x nanochain heterojunctions	Thermal evaporation method	1500	[40]
SiC/SiO_2 nanochain heterojunctions	Chemical vapor reaction method	1450	[178]
SiC/SiO_2 nanochain heterojunctions	Catalyst-free CVD process	1280	[179]
SiC/SiO_2 chain-like nanostructures	Template/catalyst-free chemical vapor reaction approach	1200–1250	[180]
Nanochains of SiC-CNTs junctions	Thermal evaporation method	1600	[181]

with the interplanar spacing $d = 0.25$ nm, confirming that [111] orientation is the preferred direction for SiC core.

Other typical SiC-core-based nanochains, such as the SiC/SiO_x and SiC/CNTs, with various diameters have also been fabricated as summarized in Table 8.8.

8.2.5.2 SiC-Shell-Based Core-Shell Nanowires

Just in recent years, the novel SiC-shell-based core-shell nanowires have been intensively studied [182, 183]. Incorporation of SiC into other typical nanowire surfaces as a shell is expected to further enhance properties of the core-shell nanowires such as mechanical, chemical resistivity, thermal stability, and other wide range of optical properties [184, 185]. These properties could lead to the applications of SiC-shell-based core-shell nanowires in field emission, nano-field-effect transistors, and sensing [183, 186, 187]. Based on reported works, there are mainly two types of SiC-shell-based core-shell structures: (i) SiC-shell-coated Si nanowires [183, 185, 188] and (ii) SiC-shell-coated CNTs [41, 186, 189].

Recently, Goh et al. proposed a hot-wire chemical vapor deposition approach for fabricating the Si/SiC-core-shell nanowires with various morphologies [184, 185]. These nanowires consisted of crystalline Si and amorphous SiC as core and shell, respectively. The Ni nanoparticles were utilized as metal nano-templates to catalyze the growth of these core-shell nanowires. The core-shell nanowires showed a tapered-like morphology with an average length and diameter of 587 and 51 nm, respectively, at deposition pressure of 0.5 mbar, while the nanowires prepared at 1 mbar shows a significant decrease in length and diameter [185]. Furthermore, they also fabricated the NiSi/SiC-core-shell nanowires through a similar process [182].

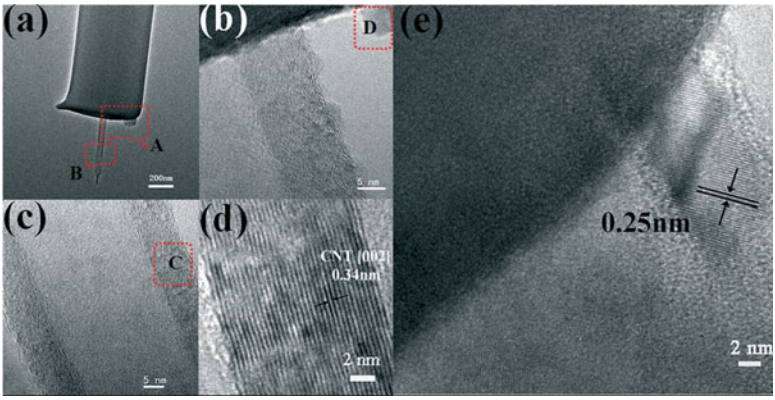

Fig. 8.16 TEM images of SiC-CNT coaxial nanocables on the carbon-coated Cu grid: (**a**) a TEM image of a SiC-CNT nanocable at low magnification. (**b**, **c**) Enlarged TEM images obtained from the top end of the SiC-CNT nanocable recorded from the marked areas A and B in (**a**), respectively. (**d**) An HRTEM image recorded from the area of C in (**c**). (**e**) An HRTEM image recorded from the marked area D in (**b**). (Reproduced from Ref. [41] by permission of the Royal Society of Chemistry)

Furthermore, various synthesis methods have been reported for fabrication of CNTs-SiC-core-shell nanostructures, such as using CNTs as the templates to react with SiO or Si powder [189, 190], and energetic Si-ion irradiated CNTs [186]. Qi and co-workers fabricated the SiC-CNTs coaxial nanocables on a large scale by using a catalyst-assisted carbothermal CVD method [41]. Sol-gel-derived silica xerogels containing commercial MWCNTs template were used as Si and C sources. Based on the skeleton of the CNTs template, the SiC was formed layer by layer via surface diffusion of Si atoms and C atoms on the surface of CNTs with the presence of Co catalyst. As the continuous growth of SiC nanolayers under 1425 °C, SiC-coated CNTs coaxial nanocables can be obtained in line with the reaction:

$$\mathrm{SiO_2(s) + C(s) = SiO(g) + CO(g)} \tag{8.4}$$

$$\mathrm{SiO(g) + 2C(s) = SiC(s) + CO(g)} \tag{8.5}$$

$$\mathrm{SiO(g) + 3CO(g) = SiC(s) + 2CO_2(g)} \tag{8.6}$$

$$\mathrm{CO_2(g) + C(s) = 2CO(g)} \tag{8.7}$$

Figure 8.16 shows TEM images of the as-synthesized SiC-CNTs coaxial nanocables. The surface of the nanocable is smooth and homogeneous (Fig. 8.16a). A clear HRTEM picture of the core-shell structure is given in Fig. 8.16b, which is recorded from the top end of the nanocable. As depicted in Fig. 8.16c, two parallel walls indicate that the inner core is a nanotube. The lattice plane spacing of about 0.34 nm is attributed to the (002) planes of MWCNTs (Fig. 8.16d). According to the HRTEM image (Fig. 8.16e) of the outter layer

Table 8.9 Representative SiC-shell-based core-shell nanostructures

SiC-shell-based core-shell nanostructures	Synthesis methods	T(°C)	Refs.
Si-SiC-core-shell nanowires	Carburization of Si nanowires arrays	≥1000	[187]
NiSi/SiC-core-shell nanowires	Hot-wire CVD process	350	[191]
Si-SiC-core-shell nanowires	Carburization of Si nanowires arrays	≥1000	[183]
Si-SiC-core-shell nanotowers	Hypersonic plasma particle deposition	530–630	[188]
SiC-assisted CNTs heterostructured arrays	Energetic Si-ion irradiation	750	[186]
1D SiC-CNTs composite	Direct solid reaction process	1300–1400	[190]
C-SiC coaxial nanotubes	Direct reaction of CNTs and Si powder	1300	[189]
SiC-shelled ZnS nanoribbons	A two-stage heating process	1150, 1450	[192]

marginal regions recorded from the marked area D in (b), the lattice plane spacing of 0.25 nm corresponds to the SiC(111) crystal plane.

Besides the examples discussed above, other typical SiC-shell-coated Si nanowires, CNTs, and ZnS nanoribbons core-shell nanostructures have also been fabricated as summarized in Table 8.9.

8.2.6 Aligned SiC Nanowire Arrays

Recently, there has been increasing interest in growth of oriented nanostructural systems to construct the nanoarrays because of their numerous potential applications in optoelectronics, sensors, nanogenerators, and electronic circuits [12, 193, 194]. Aligned growth of nanostructures can be achieved with the use of substrates, catalysts, or seeds. Hierarchical assembly of nanowires in a controlled manner is a critical step toward accomplishing these goals. Fabrication of well-aligned SiC nanowires is critically important and highly desired since it is the key step to realize the patterned arrays to be used as the electronic units [23, 195]. Up to now, much effort has been devoted to the synthesis of oriented SiC nanowires, such as the homoepitaxial growth, electrochemical etching, in situ carbonizing, and template-assisted synthesis.

8.2.6.1 Homoepitaxial Growth

The term "epitaxial" is applied to a film grown on top of the crystalline substrate in ordered fashion that atomic arrangement of the film accepts crystallographic structure of the substrate. The deposited film is denoted as epitaxial film or epitaxial layer. Homoepitaxy and heteroepitaxy are two kinds of epitaxy, in which a crystalline film is grown on a substrate or film of the different material and crystalline film grows on a crystalline substrate or film of the same material, respectively [12]. In recent years, homoepitaxial and heteroepitaxial growths have successfully been used in nanotechnology, and indeed they have been confirmed to be one of the best strategies to grow high-quality and highly oriented semiconductor nanostructure arrays [196, 197].

Compared with heteroepitaxy, homoepitaxial growth displays several unique advantages, such as avoiding a lattice and thermal expansion mismatch and a lower-energy barrier existing at the interface between the grown materials and substrate, which is the reason that it has been attracting a great deal of interest. This unique method has also impressively accelerated the fabrication and potential application of SiC nanoarray-based technologies, in particular on various state-of-the-art photonics, electronics, environmental and energy science, etc. [49, 54, 58, 198]. Recently, our group fabricated single-crystalline, well-aligned 3*C*-SiC nanowire arrays epitaxially grown on 6*H*-SiC(0001) substrates with controlled densities and doping by pyrolysis of polymeric precursors using Au films as catalysts [42, 49, 95]. The Au films were synthesized by sputter-coating method. The polymeric precursors were used as precursors to supply Si and C species. After sputtering the substrate surface with the Au films, large-scale homoepitaxial growth of SiC nanowire/nanoneedle arrays was finally realized via a VLS growth process at 1500 °C. Figure 8.17 depicts some representative SEM images of the as-grown SiC arrays on single-crystal SiC substrate in our lab, revealing that most of the nanowires/nanoneedles with a preferred growth orientation of [111] are perpendicular to the substrate surface and have clear tips. The N-doped SiC nanoarrays (Fig. 8.17a1–a3) were achieved by using the N_2/Ar gas mixture (0.1 Mpa, N_2/Ar = 5:95, volume percent) as the carrier gas during pyrolysis procedure [42, 49], while the B-doped SiC nanoarrays (Fig. 8.17b1–b3) were successfully fabricated by pyrolysis precursors of polyborosilazanes under Ar atmosphere [95].

Besides the above examples, homoepitaxial growth of SiC nanowire arrays on different SiC substrate surfaces (such as SiC$(000\bar{1})$, $(10\bar{1}0)$, $(\mathbf{11\bar{2}0})$, and (1230)) has been demonstrated successfully by various methods. Figure 8.19 displays the SEM images of the as-grown SiC nanowire arrays synthesized on the SiC substrates. As Fig. 8.18a and b shows, the SiC nanowires were achieved on SiC(0001) via a simple chemical vapor reaction approach at 1250 °C by using Ni as the catalyst and are orientationally aligned on the top of the SiC substrates [198]. Furthermore, as Fig. 8.18c–h displays, the SiC substrate orientation presented great impact on the growth habits of SiC arrays [54]. The nanowires can grow along the [1102] direction

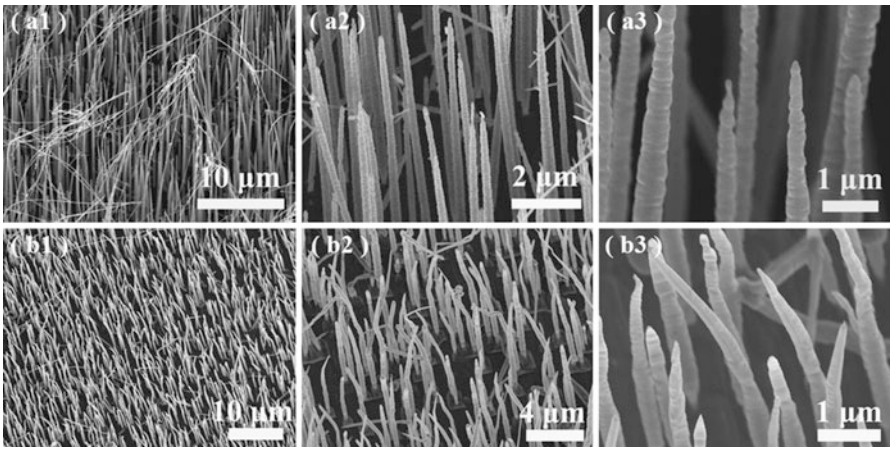

Fig. 8.17 (**a1**–**a3**) Typical SEM images of as-synthesized N-doped SiC nanoarrays under different magnifications. Reprinted with the permission from Ref. [42]. Copyright 2007 American Chemical Society. (**b1–b3**) Typical SEM images of B-doped SiC nanoarrays under different magnifications. (Reproduced from Ref. [95] by permission of the Royal Society of Chemistry)

or its equivalent ones on SiC $(10\bar{1}0)$ substrates, while nanowires grow along the $[10\bar{1}0]$ direction or its equivalent ones on SiC $(10\bar{1}0)$ and $(\mathbf{11\bar{2}0})$ substrates [54]. Systematically investigation of the preferred growth of SiC nanowires can largely improve the quality of SiC nanoarrays, which could favor the SiC arrays with perfect orientation perpendicular to the substrate, and are well aligned in very high coverage density.

8.2.6.2 Electrochemical Etching

As discussed in Sect. 8.2.1.2, electrochemical etching of single-crystal 4*H*/6*H*-SiC wafer had been proven to be an effective route for fabrication of SiC nanostructures, which could favor the fabrication of highly oriented SiC nanostructures under room temperatures (RT) as well as atmospheric pressure [82–84, 199]. The morphologies could be tuned by choosing appropriate condition, such as the etching voltage/current, electrolyte composition, etching time, and anode-cathode distance [85–88]. However, most of the as-constructed products based on the electrochemical etching routes are mesoporous and/or nano-columnar [85, 88]; the fabrication of highly ordered nanowires is still much desired.

Recently, our group achieved large-scale and well-aligned single-crystal 4*H*-SiC nanowires and nanobelts arrays via an electrochemical etching process assisted by introducing the pulsed voltage at RT and under atmospheric pressure [200]. Single-crystalline 4*H*-SiC wafers with N dopants were used as the anode (i.e., the etching

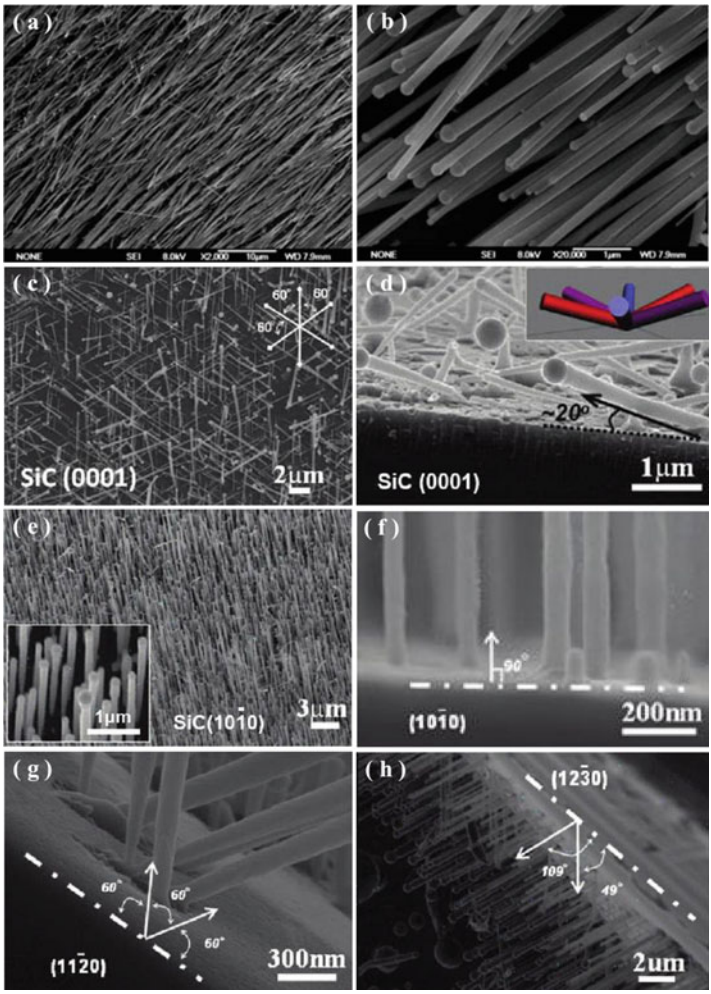

Fig. 8.18 (**a**, **b**) Different magnification SEM images of the SiC nanoarrays synthesized with Ni as catalyst on the 6*H*-SiC(0001) substrate. Reproduced from Ref. [198] by permission of the Royal Society of Chemistry. (**c**–**h**) Typical SEM images of SiC nanowires grown on SiC substrate. (Reprinted with permission from Ref. [54]. Copyright 2010 by the American Chemical Society. (**c**, **d**) SEM images of SiC nanowires grown on SiC $(000\bar{1})$ substrate showing the preferred orientation with six growth directions. (**e**, **f**) SEM images of SiC nanowires grown on SiC $(10\bar{1}0)$ substrate. (**g**, **h**) SEM images of SiC nanowires grown on SiC$(\mathbf{11\bar{2}0})$ and (1230) substrates)

sacrifice substrate). The etching of SiC can be divided into two main steps. One is the generation of SiO_2, and the other is the dissolution of the formed SiO_2, which are expressed as follows:

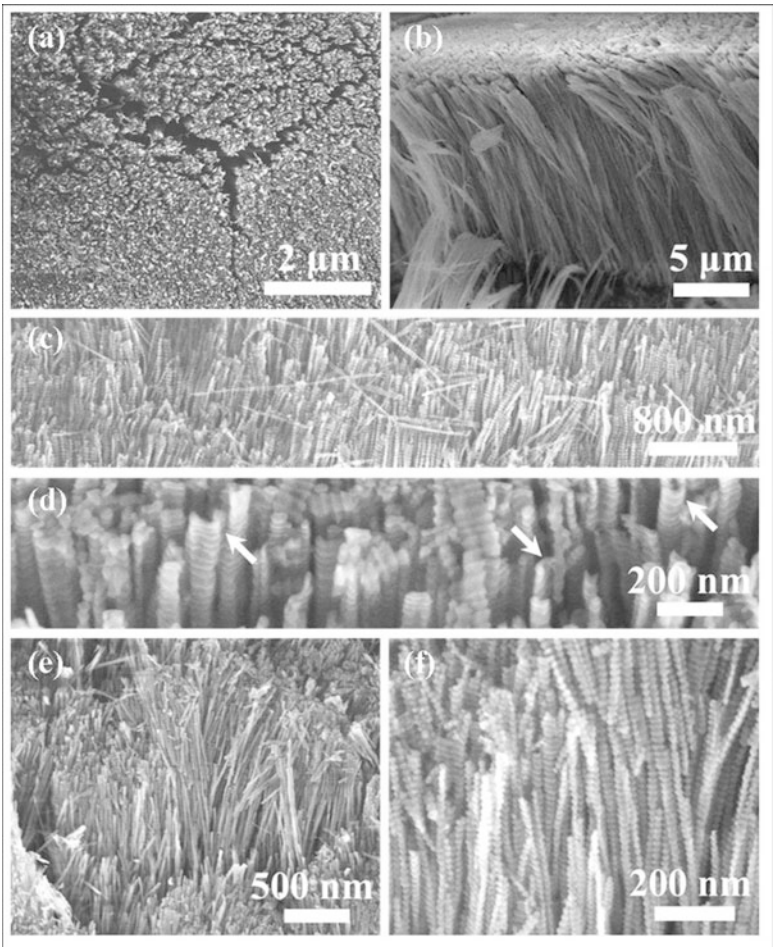

Fig. 8.19 The typical images of SiC arrays. (**a**) The top-view SEM image under low magnification. (**b**) The cross-sectional SEM image under low magnification. (**c** and **d**) The top-view SEM images under high magnifications. (**e** and **f**) The cross-sectional SEM image under high magnifications. (Reproduced from Ref. [200] by permission of the Royal Society of Chemistry)

$$SiC + 2H_2O + 4H^+ + 2O^- \rightarrow SiO_2 + CO_2 \uparrow + 4H^+ \tag{8.8}$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{8.9}$$

The repeated reactions (1) and (2) will make the continuous resolution of SiO_2, resulting in the etching of SiC and the formation of SiC nanoarrays. The obtained nanowires and nanobelts arrays presented gourd-shaped with numerous sharp knots around their surface and highly oriented, as Fig. 8.19 shows, which is an ideal structural configuration for the exploration of emitters. This novel configuration was mainly ascribed to the applied pulsed voltage, which caused the etching reaction,

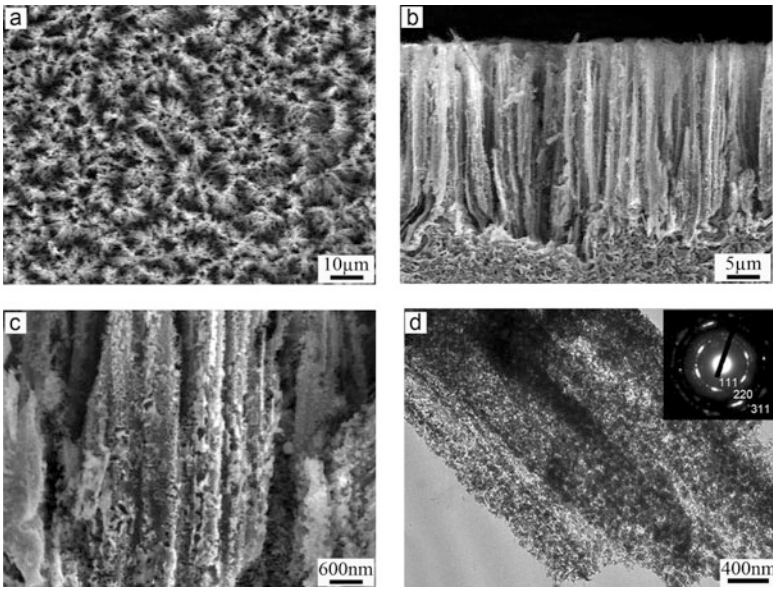

Fig. 8.20 SiC porous nanowire arrays: (**a**) top view and (**b**, **c**) cross-sectional view SEM images in low and high magnification, respectively. (**d**) TEM image and SAED pattern (inset) of SiC porous nanowire arrays. (Reprinted with the permission from Ref. [195]. Copyright 2011 American Chemical Society)

happened periodically, and made the fluctuation of the diameters. The length and morphologies of obtained SiC nanoarrays are strongly dependent on the etching time.

8.2.6.3 Converted from Si Nanowire Arrays by the In Situ Carbonizing Route

From the 1960s, anisotropic Si etch was found to be orientation-dependent in some chemical solutions and then became an important technology in Si semiconductor processing [201]. Up to date, many efforts have been devoted to the exploration of large-scale Si nanowire arrays [202, 203]. Considering the high-ordered and well-aligned configuration of the Si nanowire arrays would logically facilitate the conversion of Si nanoarrays to SiC nanoarrays through the typical in situ carbonizing route.

In 2008, highly oriented SiC porous nanowire arrays on Si substrate have been achieved by Yang and co-workers via in situ carbonizing aligned Si nanowire arrays standing on Si substrate [195]. The aligned Si nanowire arrays were fabricated via a selective chemical etching technique. The resultant SiC nanowire arrays have diameters ranging from tens to hundred nanometers with lengths about 20 μm (see Fig. 8.20a–c), which inherit the diameter and length of the mother Si nanowire

arrays, but have much more roughness and disordered microstructures. The pore sizes of the SiC porous nanowires were randomly distributed from tens to hundreds of nanometers, as Fig. 8.20d shows. The formation of the SiC porous nanowire can be attributed to partial evaporation of Si atoms from Si nanowires and carbonization of remaining Si nanowires at high temperature. First, at the heating temperature of 1350 °C, some of the Si atoms are released from individually separated Si nanowire on Si substrate, leading to Si porous nanowire on Si substrate. Second, in the meantime, the remaining porous Si nanowires react with active carbon species decomposed from C_2H_5OH to form porous SiC [195]. Subsequently, using a similar strategy, Liu and co-workers fabricated well-aligned porous SiC nanowire arrays [204]. The as-prepared SiC nanowires are highly porous, which endows them with a high surface-to-volume ratio, and utilized as photocatalyst for water splitting.

8.2.6.4 Template-Assisted Synthesis

Template-assisted synthesis is an elegant chemical approach for the fabrication of oriented nanostructures, particularly for different solid nanowire arrays. Among these templates, the nanoporous anodic aluminum oxide (AAO) templates have received considerable attention in synthetic nanostructure materials due to their unique structure properties, such as their fully controllable and extremely narrow size distribution in pore diameters, good chemical inertness, physical stability, and ideal cylindrical shape of pores [205]. They also have been used to fabricate SiC nanowire arrays by using a variety of methods [206]. For example, Li and co-workers fabricated large-area highly oriented single-crystalline β-SiC nanowire arrays by chemical vapor reaction approach using an ordered nanoporous AAO template [207]. The synthetic reaction was carried out in a graphite reaction cell using mixture of milled Si and SiO_2 powder and C_3H_6 as the starting materials at 1230 °C. These SiC nanowires have a length of around 8 μm with diameters of about 30–60 nm and are parallel to each other, uniformly distributed, highly oriented, and in agreement with the nanopore diameter of the employed AAO template [207]. The density of SiC nanowires is about 10^9–10^{10} cm^{-2}.

8.3 Electronic Applications of SiC Nanowires

Driven by the thrust of fabricating smaller devices to create integrated circuits with improved performance, SiC nanowires have been exploited as potential building blocks for future nanoelectronics. In this section, we will review some recent typical works on the electronic, electrochemical, optoelectronic, and electromechanical devices built on SiC nanowires.

8.3.1 Field Emission Applications

Over the past decades, field emission behaviors of nanowires have been extensively investigated, due to their importance in both nanoscience and exciting applications such as electron sources in flat-panel displays, electron microscopes, and vacuum microelectronic devices [208–210]. In this section, we begin with the introduction of the field emission phenomena. Then, based on the Fowler-Nordheim (*F-N*) theory, we put forward a comprehensive and up-to-date review on the progress of enhanced field emission properties of SiC nanowires assisted by four important strategies. Finally, we highlighted the latest advances of emerging SiC nanowire-structured flexible field emitters.

8.3.1.1 Field Emission Phenomena

Field emission is a quantum mechanical tunneling phenomenon in which electrons are emitted from the surface of the material through a potential barrier to a vacuum under an applied external electric field [208–210]. This is generally considered as a low-temperature (or cold) process, in the sense that no thermal energy is supplied to energize the electrons. This phenomenon mainly occurs in high electric fields of 0.1–20 V/μm. The current generated by this process is first described by Fowler and Nordheim, called Fowler-Nordheim (*F-N*) theory, based on the metal model in 1928 [211], and thus been widely used to analyze field emission currents from various materials [212–216]. This electron tunneling phenomenon is highly dependent both on the properties of the material and the shape of the particular cathode, and the materials with higher aspect ratios and sharp edges produce higher field emission currents. Figure 8.21a is a schematic illustration of the field emission model. The electron emission occurs from the tip of an emitter due to the local field enhancement effect. The emitter can have different emission currents depending upon the tip geometry such as round tip, blunt tip, and conical tip, as Fig. 8.21b shows.

The emission current density (J) tunneled from an emitter excited by a given electric field (E) is described by the Fowler-Nordheim equation:

$$J = \left(A\beta^2 E^2/\Phi\right)\exp\left[-B\Phi^{3/2}(\beta E)^{-1}\right] \tag{8.10}$$

$$\ln\left(J/E^2\right) = \ln\left(A\beta^2/\Phi\right) - B\Phi^{3/2}/\beta E \tag{8.11}$$

where E is the applied electric field, $A = 1.54\times10^{-6}$ AeV/V^2, $B = 6.83\times10^3$ e/V$^{3/2}$ V/μm[1], and Φ is the work function of the emitter material. β is the field enhancement factor, which is defined by a two-level hierarchy [45, 199]:

(i) The local electric field enhancement (β_L) at the level of the individual emitter, set by the size and shape of the local nanostructure [217], which can be expressed as $\beta_L = h/r$, where h is the height and r is the radius of curvature of

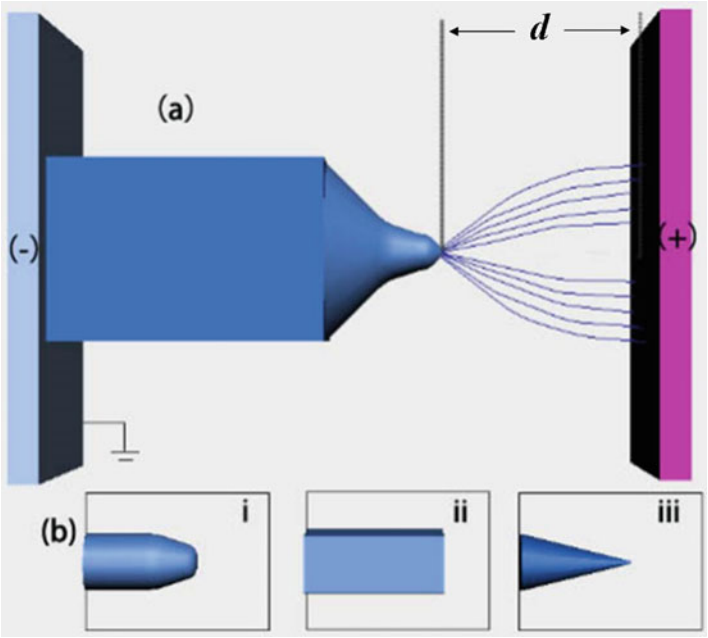

Fig. 8.21 (**a**) Illustration of the field emission model. The emission occurs from the tip of an emitter. (**b**) The emitter can have different emission currents depending upon the tip geometry, such as (*i*) round tip, (*ii*) blunt tip, and (*iii*) conical tip

an emitting center. Thus, emitters with elongated geometry and sharp tips or edges can favor a high β_L value and greatly increase an emission current [218].

(ii) The global electric field enhancement (β_G), set by the larger-scale spatial arrangement of the emitters, which is sensitive to the small variations in the emitters' densities [217, 219], bending states [220], shapes and/or surroundings [221], as well as the change of applied electric fields [222].

FE, as one of the main features of nanostructures, is of great commercial interest in displays and other electronic devices [12, 208]. More impressive, 1D nanostructure-based FE cathode materials are significant in the field of electronics, particularly in flat-panel displays, electron microscopes, and X-ray sources due to their high aspect ratio nature [212, 223, 224]. Numerous 1D nanostructures, including CNTs, oxides, carbides, nitrides, and metals, have been comprehensively studied as candidates for FE applications [208]. Recent progress in the synthesis and assembly of nanowires has resulted in a considerable increase in the current density, lowering of the turn-on voltage, and enhancing the long-term current stability for a variety of nanomaterials [193, 225, 226]. As discussed in previous reviews [208–210], the turn-on field, threshold field, field enhancement factor, FE current density, and its stability are the key parameters of one material FE performance. These properties are strongly dependent on the work function (Φ) of an emitter surface,

Table 8.10 The work function (Φ) of some typical inorganic semiconductors, CNTs, and metal emitters

Emitters	Φ (eV)	Emitters	Φ (eV)	Emitters	Φ (eV)
SiC	4.0	AlN	3.7	Ti	4.33
Si	3.6	GaAs	4.77	Ru	4.7
ZnO	5.3	ZnS	7.0	W	4.5
WO_3	5.7	CdS	4.2	Sn	4.42
SnO_2	4.7	VS_2	4.9	Cu	4.65
CuO	4.5	CNTs	5	Mo	4.37
TiO_2	4.3	Au	5.1	Cd	4.07
GaN	4.1	Ag	4.26	Zn	4.3
BN	6.0	Al	4.28	Hf	3.9

A part of the data reproduced from Ref. [77]

the radius of curvature of the emitter tip, the emission area, the aspect ratio, and arrangement style of the emitters.

According to Eqs. (8.10) and (8.11), the work function (Φ) of an emitter plays a crucial role in the emission current. The Φ is the energy required to remove an electron from the highest filled level in the Fermi distribution of a solid emitter so that it is stationary at a point in a field-free zone just outside the solid, at absolute zero [12]. Table 8.10 lists the work function of typical emitters, including the inorganic semiconductors, CNTs, and metals. It is easy to note that the work function for SiC is lower than most of the other popular field emission materials, such as ZnO, SnO_2, GaN, ZnS, CdS, CNTs, Au, and W [216, 219, 227, 228]. It is clear that at a specific electric field, the SiC can produce a higher electron emission current.

In addition to the low work function, the SiC nanostructures also possessed versatile, excellent properties, such as superior mechanical properties, high thermal conductivity, low thermal expansion coefficient, good thermal shock resistance, as well as excellent chemical stability and electron affinity [20, 29, 208], which facilitated stable emission and long lifetime of SiC emitters under harsh work conditions and favor them utilized as excellent field emitter candidates. Up to date, many works have focused on the FE properties of SiC nanowires. Their turn-on fields (E_{to}; refers to the electric field required to generate a current density of 10 μA/cm^2; if the other values are used, it is separately mentioned) which ranged from room temperature to 500 °C fell usually in just several or even lower than 1 V/μm, showing their excellent FE properties [21, 44, 46, 57, 92, 97, 110, 195, 199, 229, 230].

Motivated by a desire to obtain an ideal field emitter with totally excellent FE performances, four strategies were developed to improve the electron emission from SiC nanowires based on the Fowler-Nordheim (*F-N*) theory: (i) making the nanowires with sharp tips for utilizing the local field enhancement effect [52, 102], (ii) tailoring the bandgap of established nanomaterials via doping strategy [46, 93], (iii) increasing the density of the electron emission sites [55, 67], and (iv) growing the aligned nanowire arrays to limit the shielding effect [42, 49].

8.3.1.2 Enhanced FE Properties by Growing SiC Nanowires with Sharp Tips

From the foregoing discussion in Sect. 8.3.1.1, to improve the FE properties of nanowire emitters, one of the effective strategies is to reduce the tip size of nanostructures, namely, to obtain the needlelike nanowires, which could favor a high electron emission current density due to the strong local electric field at the tips and the unique electron emission direction owing to their geometries of small curvature radius. The synthesis of nanowires with needle-shaped and/or sharp tips is always the center of FE research and FE applications [52, 231–233]. Chen and co-workers offered a comprehensive review on the nanotips [234]. The morphologies and growth techniques of nanoscale tips had been discussed in this review. For FE applications, the authors suggested that some inherent problems existing in the nanowires systems may be automatically overcome by selecting the proper nanotip structure. For example, the field screening in the case of densely packed emitters is much reduced for nanotips because the tips are spaced apart. This spacing also depends on their base diameters [77, 234].

Up to date, several groups have reported on the FE properties of SiC nanowires with needle-shaped and/or tiny tips [52, 92, 235]. Table 8.11 displays a comprehensive and up-to-date summary on the fabrication of SiC nanowires with needle-shaped and sharp tips as well as their FE properties. This is true for these nanowires synthesized by various methods, including the catalyst-assisted pyrolysis of polysilazane, CVD process, and thermal evaporation route. It clearly shows that the typical E_{to} of these nanostructures often fall below 1.8 V/μm, which is lower than most of the other reported typical SiC emitters [21, 44, 199, 230], suggesting their excellent FE performance.

Here, we present the synthesis of novel needle-shaped SiC nanowire emitters with tiny and clean tips via catalyst-assisted pyrolysis of a polyaluminasilazane precursor in our group [102]. The obtained SiC nanowires are needlelike shaped and up to dozens of micrometers in length, and the diameter first increases with the growth process and decreases sharply near the growth end, as verified by a low- and high-magnification SEM images in Fig. 8.22a–c. The formation of this specific structure can be attributed to the size change of the liquid catalytic droplet related to the pyrolysis process, in which the growth of nanostructures is dominant by VLS mechanism [53]. An XRD spectrum taken from the nanowires body is shown in Fig. 8.22d, where all the diffraction peaks can be indexed to 3*C*-SiC without any impurities. The TEM images taken from the tip of nanoneedle are shown and exhibit that the tip is clear without catalyst droplet, and numerous sharp corners around the tip are sized in several to tens of nanometers [102]. These specific structures can greatly enhance the FE behavior because both tiny tips and sharp corners can simultaneously act as efficient electron emitting sites due to the effect of local electric field.

Figure 8.23a shows the corresponding FE current densities, *J*, as a function of applied fields, *E*, for *J*-*E* plots measured under different temperatures in the ranges of

Table 8.11 A comprehensive and up-to-date summary on the fabrication of SiC nanowires with needle-shaped and/or sharp tips as well as their FE properties

SiC nanowires	Synthesis process	FE Properties (E_{to}, E_{thr}[a], β, and current stability)	Refs.
Needle-shaped N-doped SiC nanowires	Catalyst-assisted pyrolysis of polymeric polysilazane	E_{to} = 1.11–1.38 V/μm. The current emission fluctuation is about 8.1%	[46]
N-doped SiC nanoneedles	Catalyst-assisted pyrolysis of polymeric polysilazane	E_{to} decrease from 1.58 to 0.65 V/μm with temperature raised from RT to 500 °C	[236]
Needle-shaped *n*-type 3*C*-SiC nanowires	Catalyst-assisted pyrolysis of polymeric polysilazane	E_{to} decrease from 1.37 to 0.67 V/μm with temperature raised from RT to 400 °C	[25]
SiC nanoneedles with clear and sharp tips	Catalyst-assisted pyrolysis of polymeric polysilazane	E_{to} = 1.15 V/μm	[52]
n-Type 3*C*-SiC nanoneedles	Catalyst-assisted pyrolysis of polysilazane	The E_{to} in the range of 0.5–1.6 V/μm with an average of 1.1 V/μm. $\beta = 6.5 \times 10^3$	[92]
Well-aligned SiC nanoneedle arrays	CVD process without using any templates	E_{to} = 1.3 V/μm, and E_{thr} = 2.2 V/μm. β = 3667	[235]
Al-doped 3*C*-SiC nanowires with clear and tiny tips	Catalyst-assisted pyrolysis of polysilazane	The E_{to} = 0.55–1.54 V/μm with an average of ~1 V/μm β = 2983	[93]
β-SiC nanoneedles	Mg-catalyzed chemical co-reduction	E_{to} = 1.8 V/μm	[80]
Needle-shaped SiC nanowires	Thermal evaporation process and using iron as catalyst	Stable emission with *J* of 30.8 mA/cm^2 at 9.6 V/μm and *J* up to 83 mA/cm^2	[237]

[a] E_{to} and E_{thr} required to generate an emission current density of 10 μA/cm^2 and 1 mA/cm^2, respectively. If other values are used, it will be mentioned separately

RT to 500 °C of obtained needle-shaped SiC emitters. These curves show the same characteristics: (i) all the curves remain horizontal with emission current density of zero at the beginning stage, and (ii) when the applied electric field is beyond a certain value, the current density increased nearly exponentially with the increase of applied electric field [102]. A relatively low E_{to} is extrapolated as 1.30 V/μm, which is lower than most works ever reported on SiC nanostructures [36, 93, 110, 230] and other inorganic semiconductor nanostructures [231, 238–240]. The E_{to} obviously decreased from 1.30 to 0.66 V/μm when increasing the temperature from RT to 500 °C, as shown in Fig. 8.23b. As the *E* is fixed at 1.37 V/μm, the SiC emitters can produce a high emission current density of 2444 μA/cm^2, as depicted in Fig. 8.23b, which is at least three orders of magnitude higher than that at RT (20 μA/cm^2). A high field enhancement factor (β) of 4203 was calculated at RT from a slope of the fitted straight line in Fig. 8.23c. We attributed the low E_{to} and high β to the small radii of curvature and the high aspect ratio of the as-constructed SiC nanoneedles. These data shows that the present SiC emitters are decent field emitters.

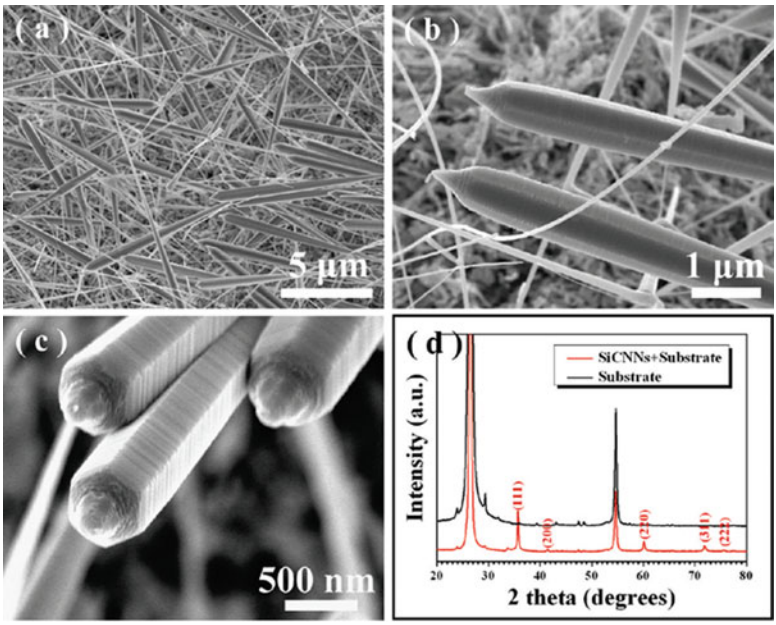

Fig. 8.22 (**a**–**c**) Typical SEM images of as-synthesized SiC emitters under different magnifications. (**d**) Representative XRD patterns recorded from SiC+substrate and substrate. (Reprinted with the permission from Ref. [102]. Copyright 2011 American Chemical Society)

8.3.1.3 Enhanced FE Properties by Doped SiC Nanowires

Besides the morphology control, chemical doping is another important approach to tailor the properties of nanowires, which has been proven effective in the doping of carbon-based materials and other typical semiconductor nanostructures and renders their use for various applications [6, 241, 242]. Usually, there are two means to chemically dope nanostructures: (i) the adsorption of gas, metal, or organic molecules to the nanostructures surface and (ii) substitutional doping, which introduces heteroatoms, such as B, Al, N, and P atoms, into the lattice of nanomaterials. Both of these methods can modulate the band structure as well as the electronic properties of nanomaterials. Wang and co-workers reviewed that after nitrogen doping in the monolayer graphene, the Fermi level shifts above the Dirac point; thus, the bandgap between the conduction band and the valence band will be opened [242]. For graphene nanoribbons, the bandgap is still kept after doping. The bandgap in N-graphene makes it a candidate to be used in semiconductor devices [242]. Hsu and Chang reviewed that various typical enhancements of physical properties have been achieved from doping ZnO 1D nanostructures, such as increased conductivity, increased ferromagnetic properties, increased transparency, or a reduced work function [6].

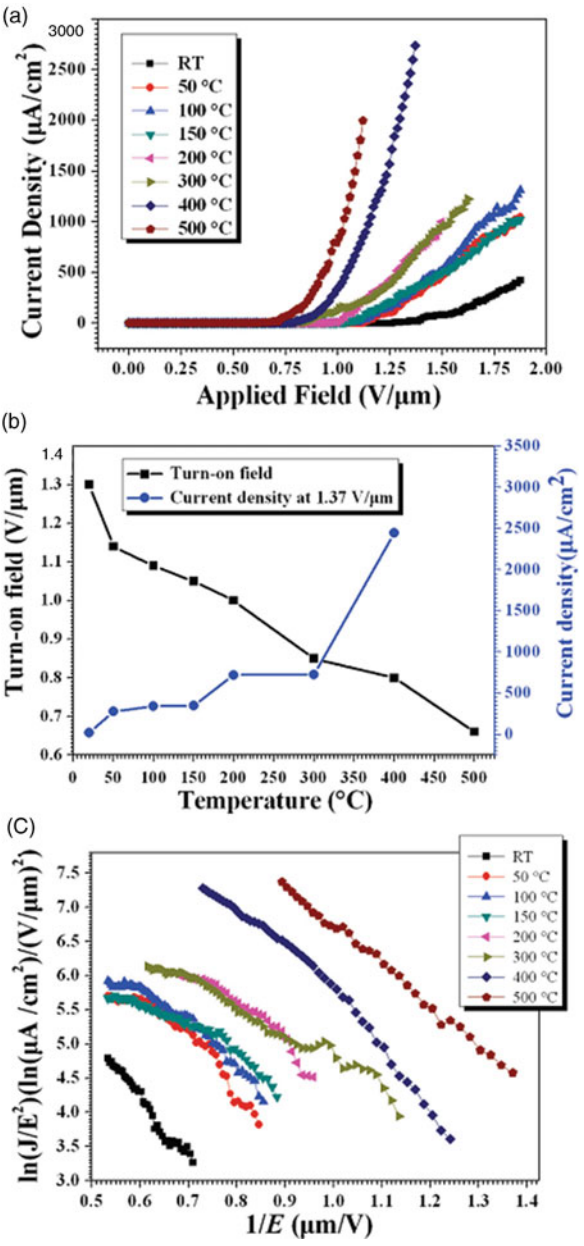

Fig. 8.23 (**a**) *J-E* plots of needle-shaped SiC emitters under different ambient temperatures. (**b**) The variation of turn-on field and emission current density with temperatures for SiC emitters. (**c**) Corresponding *F-N* plots of SiC emitters under different ambient temperatures. (Reprinted with the permission from Ref. [102]. Copyright 2011 American Chemical Society)

With respect to FE applications, it is well known that the work function (Φ) of an emitter plays a crucial role in the electron emission performance [243]. The Φ is the energy required to remove an electron from the highest filled level in the Fermi distribution of a solid emitter so that it is stationary at a point in a field-free zone just

outside the solid, at absolute zero [12]. It is clear that at a specific field, a lower work function material can establish the electron tunneling of the barrier effortless, thus favoring a lower E_{to} and a higher electron emission current [244]. Doping has been proven to be an efficient way to enhance the FE properties of the SiC nanowires, since it can tailor their Φ and/or significantly increase the localized density states around the Fermi energy region [92, 93, 102, 245]. This could facilitate more facile electron excitation from the valence band to the conduction band or the vacuum level through subsequent *F-N* tunneling under the external electric field with low E_{to}, leading to a remarkable enhancement of the FE behaviors of the SiC nanowire emitters. It is well known that the most appropriate dopant materials for the *p*-type doping of SiC nanowires field emitters are found in main group III (i.e., boron (B) [95, 97] and aluminum (Al) [93]) and the *n*-type doping are found in main group V (i.e., nitrogen (N) [44, 46, 92] and phosphorus (P) [245]), respectively.

1. *p*-Type Doping of SiC Nanowire Field Emitters

The *p*-type SiC nanowire field emitters, such as the B- and Al-doped SiC, have been investigated [93, 95, 97]. Zhang and co-workers reported the enhanced field emission properties of quasi-aligned Al-doped SiC nanowires [93]. The as-synthesized nanowires possess a tapered and bamboo-like structure with clear and tiny tips sized in several to tens of nanometers. These *p*-type SiC nanowires presented an extremely low turn-on field of 0.55–1.54 V/μm with average value of ~1 V/μm. The authors attributed the superior FE properties to the significant enhancements of the Al-doping and tapered and bamboo-like unique morphology of SiC nanowires [93].

We fabricated the *p*-type 3*C*-SiC nanowires with B dopants and sharp corners [97]. FE measurements showed that both the B dopants and sharp had a significant influence on their FE properties. As Fig. 8.24a and b shows, the nanowires presented low E_{to} of 1.35 V/μm, and the β is calculated to be ~4895. The excellent FE performances could be attributed to the special *p*-type triangular prism-like nanostructure with B dopants, and the numerous sharp corners on the prism edges, as shown in Fig. 8.24c and d, which could reduce the effective work function and remarkably increase the emission site density. More importantly, the current emission fluctuation with an applied field of 1.88 V/μm at 200 °C could be improved to ~11% from ~22% of the undoped counterparts, suggesting that the high-temperature FE stability of SiC nanowires could be significantly enhanced by the B dopants [97].

Density functional theory (DFT) calculations suggest that *p*-type doping in SiC nanowires could favor a more localized state near the Fermi energy, which facilitates a more facile electron emission from the valence band to conduction band or vacuum level, consequently leading to the remarkable enhancement of the FE properties of the SiC nanowires with low E_{to}, high emission current density, as well as high stability [93, 95, 97].

2. *n*-Type Doping of SiC Nanowire Field Emitters

As compared to the *p*-type doping, the *n*-type doping is approved a more efficient strategy for enhancing the electron field emission of the SiC nanowire emitters

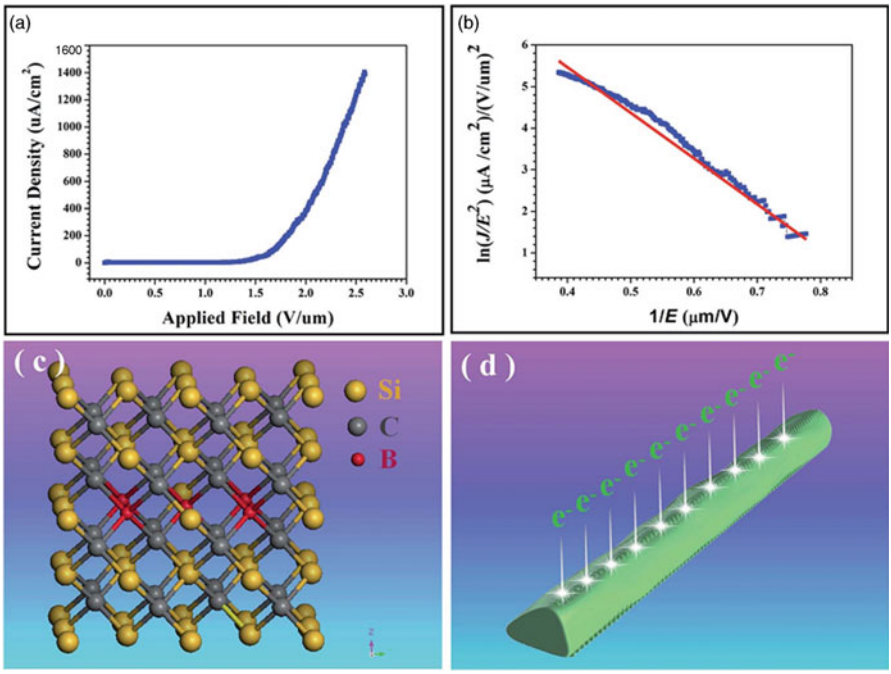

Fig. 8.24 (**a** and **b**) A typical *J-E* curve at RT and the corresponding *F-N* plot of the B-doped SiC wires, respectively. (**c**) Crystal structure of SiC with substitutional solid solutions of B dopants. (**d**) Schematic illustration of the electron emission from the B-doped wires with numerous sharp corners on the edge. (Reproduced from Ref. [97] by permission of the Royal Society of Chemistry)

[25, 92]. Based on the DFT calculations, there are mainly two means for the *n*-type doping to promote the FE behaviors [45]: (i) established more localized state near the Fermi energy, which is similar to the *p*-type doping, (ii) while the *n*-type doping could also facilitate the Fermi energy level significant shift toward the conduction band, thus reducing the Φ. Up to now, various *n*-type SiC field emitters, such as the N-doped [44, 46, 92] and P-doped [45, 245], have been reported. The E_{to} usually lower than 2.7 V/μm, showing their excellent field emission properties.

Directed by *F-N* theory for enhanced field emission behaviors, we fabricated P-doped 3*C*-SiC nanowires field emitters via catalyst-assisted pyrolysis mixed powder of polysilazane and $FePO_4{\cdot}H_2O$ [45]. The SiC emitters were grown into 1D nanostructures with two desired characteristics, namely, with an ultrahigh aspect ratio and incorporated P dopants, which brought profound enhancements to the β and E_{to}. The nanowires exhibit an aspect ratio over 1500 with a uniform spatial distribution of P dopants. The FE measurements exhibit that the E_{to} and β are extrapolated to 0.47, 0.51, and 0.61 V/μm and 11,657, 9642, and 7149, once the anode-to-sample distances (d) are fixed at 700, 800, and 900 μm, respectively, as shown in Fig. 8.25a and b. The ultralow E_{to} and high β was little achieved among the reported studies [45]. A variation of emission current densities of the present

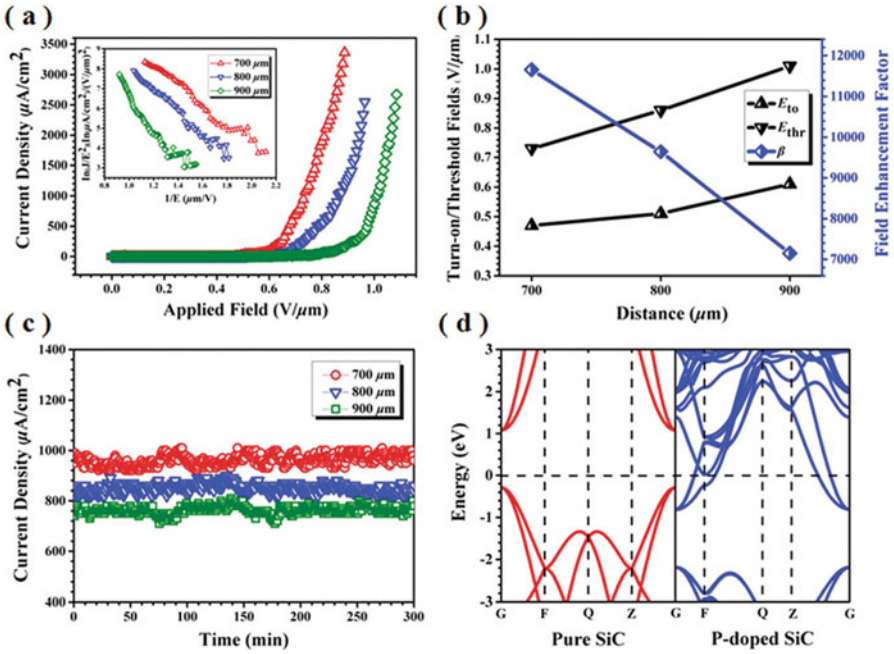

Fig. 8.25 (**a**) Typical *J-E* curves of the P-doped SiC nanowires with different *d*. The inset is the corresponding *F-N* plots. (**b**) The variations of E_{to}, E_{thr}, and β with different *d*. (**c**) The current emission stabilities of the SiC nanowires over 5 h under different *d*. (**d**) The theoretical calculations of the band structures for the intrinsic and P-doped SiC nanowires. (Reproduced from Ref. [45] by permission of the Royal Society of Chemistry)

nanowires under different *d* with 5 h is shown in Fig. 8.25c. There are no any current degradations or notable fluctuations during this period.

The DFT calculations of the electronic band structures disclose that, as compared to that of the intrinsic counterpart, the P dopants favored a more localized state around the Fermi energy level as well as pined the Fermi level moving forward to the conduction band and result in a remarkable reduction of Φ, as Fig. 8.25d shows. Briefly, the P dopants within SiC would increase the effective density of electrons state and reduce the Φ, which consequently facilitate an excellent FE performance of the present P-doped SiC nanowires [45].

8.3.1.4 Enhanced FE Properties by Surface-Decorated SiC Nanowire Emitters with Nanoparticles

Besides grown the emitters with sharp tip and doping route that discussed above, increasing the density of the emission sites is considered as another critically important issue for the enhanced FE performance [246, 247]. Recently, surface decoration of low-dimensional nanostructures with small nanoparticles, for the

purpose of increasing the density of field emission sites, has been studied as one effective method to improve the FE properties [248–250]. Cursory inspection of the *F-N* equation shows that FE current is inversely correlated to the work function. Therefore, the addition of low work function metal or other nanoparticles to the field emitter surface could be also one candidate route to improve the FE properties and indeed has been intensively investigated. Previous reports confirmed that the emitters coated with low work function materials showed much lower E_{to} than that of the pristine counterpart [250, 251]. The reason for the enhanced FE performance of field emitters surface decorated with low work function nanoparticle can be figured out as follows: (i) increasing the density of the electron emission sites, (ii) reducing the work function, and (iii) decreasing the resistance of field emitters.

Recently, it was reported that the surface decoration of the emitters with metal nanoparticles (e.g., Al, Cu, Mn, Ru, Cs, Ag, Ti, and Pt nanoparticles) could be effective to greatly increase the density of the emission sites and reduce the work function of the emitters, thus correspondingly enhancing the FE properties [246, 249, 252–256]. For instance, Gautier et al. proposed that the electric field of the carbon nanotubes for producing a current density of 0.1 μA/cm^2 was decreased from 2.68 to 0.96 V/μm once decorated by Au nanoparticles [248]. By coating MWCNTs arrays with 4 nm Ti nanoparticles, the turn-on field to obtain emission was decreased by 1 V/μm [256]. But the more encouraging point is that the Al nanoparticles-decorated carbon nanotube arrays exhibited exciting excellent FE properties with ultralow E_{to} and E_{thr} of 0.13 and 0.14 V/μm, respectively, which are almost the lowest reported E_{to} and E_{thr} [252].

In addition to the typical metal nanoparticles, the oxide [229], sulfide [254], and rare earth hexaborides [251] are also exploited as the decorated nanoparticles together with the unique combination of their low work function nature, low electron affinity, low volatility at high temperatures, and high chemical resistance.

Recent advances in the design and control of surface decoration of emitters with nanoparticles have opened the door to fabricate the nanoparticles-decorated SiC nanowire emitters. In 2011, Cui and co-workers proposed that the Al_2O_3 nanoparticle-decorated tubular SiC 1D nanostructure shows a remarkable enhanced FE property [229]. Compared with the same density and sized bare tubular SiC, the Al_2O_3 nanoparticle-decorated tubular SiC has an obvious reduction in E_{to} (from 8.8 to 2.4 V/μm) and E_{thr} (from 23.5 to 5.37 V/μm), as Fig. 8.26 shows. This is the first report of FE enhancement of SiC-based nanostructures by virtue of Al_2O_3 nanoparticles decoration. The authors attributed the enhanced FE properties to the small electron affinity of Al_2O_3 nanoparticles, the increased emission sites, and the possible doping of Al into backbone tubular SiC [229].

Generally, a higher density of the emit sites could provide a higher FE current. Nevertheless, on contradictory, once the density of the sites is too high, the field screening effect (also called “shield effect”) would happen to weaken the FE properties [220, 257–259]. Thereby, precise control of decorated nanoparticles density on the SiC nanowire emitters surface is crucially important to push forward their devices application with excellent FE performances. Unfortunately, there are

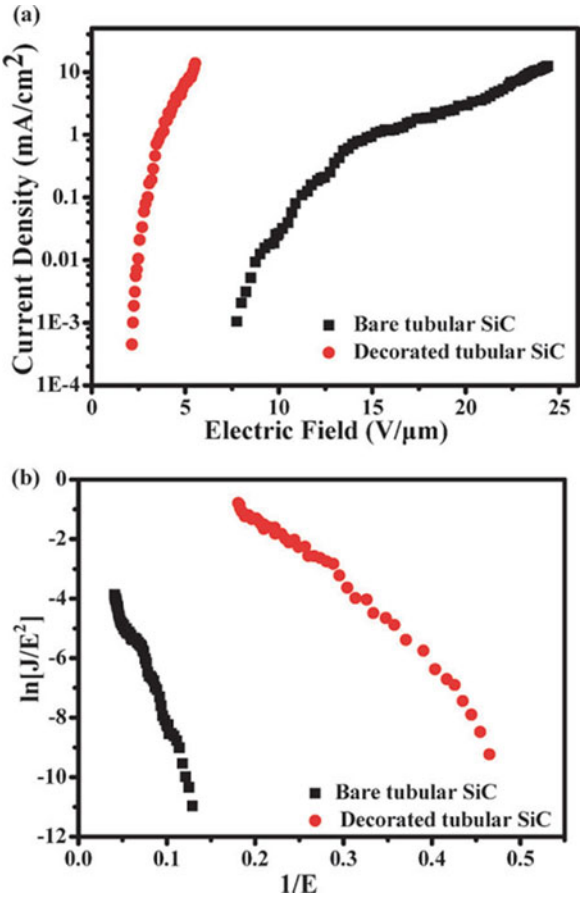

Fig. 8.26 (**a**) *J-E* field emission plot from bare tubular SiC as well as Al_2O_3 nanoparticles-decorated tubular SiC sample. (**b**) The corresponding Fowler-Nordheim plot. (Reproduced from Ref. [229] by permission of the Royal Society of Chemistry)

still little reports that shed light on the control of the densities of the surface-decorated nanoparticles of the SiC nanowire emitters.

Recently, we fabricated the novel Au nanoparticles (AuNPs)-decorated SiC nanowires via the pyrolysis of polymeric, followed by surface decoration with AuNPs by a sputtering process [67]. Then, for increasing the effective electron emission site density with limited field screening effects, we further tailored the AuNPs density by precisely controlling the sputtering times [68]. Samples S0, S5, S15, and S30 refer to the products fabricated with fixed sputtering times of 0, 5, 15, and 30 s, respectively.

The SEM observation confirmed the AuNPs density increased as the ion sputtering time increased [68]. TEM images reveal that once the sputtering time is fixed at 15 s, numerous isolated AuNPs, rather than continuous films, have been homogeneously decorated around the surface of the SiC nanowires with uniform size distribution, resulting in the growth of the nanowires with a rough surface, as depicted in Fig. 8.27a–d. Statistics based on numerous TEM observations (more

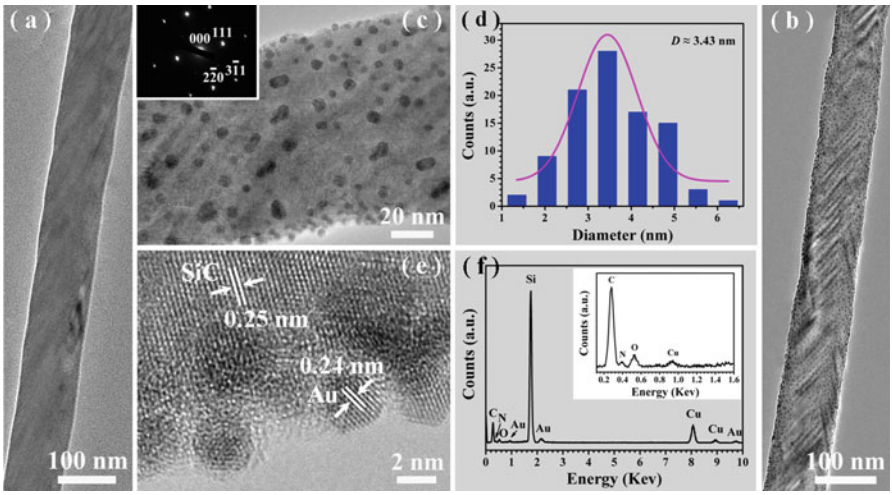

Fig. 8.27 (**a**) and (**b**) Representative TEM images of a single nanowires sample S0 and S15 under low magnifications, respectively. (**c**) Typical TEM image of a single nanowire of S15 under a high magnification. The inset is the corresponding SAED pattern. (**d**) The size distribution of AuNPs on the surface of sample S15. (**e**) Typical HRTEM image of sample S15. (**f**) A representative EDX spectrum of sample S15. (Reprinted with permission from Ref. [68]. Copyright 2016, American Institute of Physics)

than 100 AnNPs) indicate that the AnNPs behave with an average size of ~3.43 nm. The lattice fringe spacing of the AnNPs and SiC nanowires is ~0.24 and ~0.25 nm, as Fig. 8.27e shows, suggesting the cubic Au and SiC were obtained. The detected Au signal (Fig. 8.27f) further confirms the existence of AnNPs decorated around the SiC nanowire surface.

The comparative plots of field emission *J-E* curves and their corresponding E_{to} and E_{thr} as a function of the ion sputtering times for the SiC nanowires with different Au nanoparticles densities are depicted in Fig. 8.28a. The inset in Fig. 8.28a is magnified *J-E* curves for the samples S0 and S5. The *J-E* plots clearly show the profound effect of decorated AuNPs on the electron emission from the SiC nanowires. The measured FE characteristics demonstrated the E_{to} and E_{thr} of the SiC nanowires were tuned to be of 2.06, 1.14, and 3.35 V/μm and 2.59, 1.72, and 4.07 V/μm, respectively, with the increase of the decorated Au nanoparticles densities, as shown in Fig. 8.28b and c. The calculated β based on the *F-N* plots in Fig. 8.28d are ca. 1150, 1193. 6244, and 732 for S0, S5, S15, and S30, respectively. The S15 exhibits the highest β and are nearly 6 times to that of the bare counterparts of S0, which could facilitate the electron emission.

In present work, the E_{to} of sample S30 should be lower than that of S15, due to its higher electron emission sites. However, as mentioned above, sample S15 exhibits the best FE performance, verifying that the FE properties of nanowires are not only determined by the electron emission sites, in regard to the field screening effect [68]. That is, the electron emission from the AnNPs-decorated SiC nanowires is a

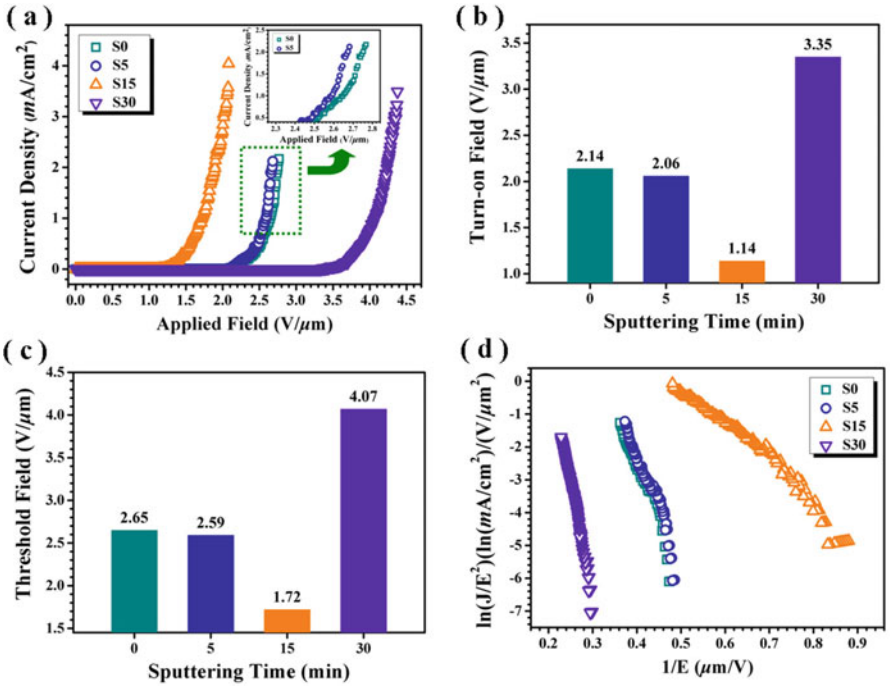

Fig. 8.28 (**a**) *J-E* plots of samples S0, S5, S15, and S30. (**b**, **c**) The variations of E_{to} and E_{thr} with the variations of sputtering times, respectively. (d) The corresponding *F-N* plots. (Reprinted with permission from Ref. [68]. Copyright 2016, American Institute of Physics)

balance between the emission sites and field screening effect. It suggests that a suitable decorated Au nanoparticles density could render the SiC nanowires with totally excellent FE performances by increasing the emission sites and limiting the field screening effects [68].

In addition to the increased emission sites with limited screening effect, the authors also attributed the enhanced FE performance of S15 to the following two reasons [67]: (i) strong local field enhancement effect induced by the small size of the decorated Au nanoparticles and (ii) reduced work function (Φ) of SiC emitters, which is caused by the formed SiC-Au heterojunction.

8.3.1.5 Enhanced FE Properties by Orientation-Ordered SiC Nanowire Arrays

For the highly ordered nanostructure arrays, it not only has an advantage of faster device turn-on time, compactness, and sustainability compared to the conventional bulky technologies, but aligned nanostructures with a high density and orientation can significantly enhance the FE properties of materials [258, 260, 261]. For

example, aligned carbon nanotubes with a high density of emitting tips can greatly enhance the current and uniformity of emission [262]. Wang and co-workers reported enhanced cold field emission of highly oriented ZnO nanowires arrays [219]. It was found that a uniform distribution of nanowires and a clean/flat substrate could further increase the emitting efficiency. And the nanoarrays with various densities presented different E_{to} due to the screening effect. The authors proposed that the fluctuation of E_{to} had been attributed to the screening effect [219].

Well-aligned SiC nanowire emitters were also successfully fabricated since the last decade. In 2000, for the first time, Pan and co-workers reported the preparation of SiC nanowires arrays with the average E_{to} value of 1 V/μm by reaction of SiO_2 and CNTs under 1400 °C [23]. Such low E_{to} has not been reported before for emitters of any type. The authors attributed this emission behavior to the very high density of emitting tips with a small ratio of curvature at the emitting surface [23]. Subsequently, several groups focus on the FE behavior of SiC nanoarrays. Yang and co-workers synthesized the oriented SiC porous nanowire arrays with the E_{to} of 2.3–2.9 V/μm by in situ carbonizing aligned Si nanowire arrays [195]. Kang and co-workers obtained the porous SiC nanoarrays with the E_{to} of 4.4–9.6 V/μm and high emission current of 6 A/cm^2 at 7.5 V/μm assisted by the electrochemical and ion etching route [199].

Although alignment of SiC nanowires has been proven to be one of the facile routes to enhance FE performance, the aspect ratio of the emitters, arrays distribution, and the morphology of individual nanostructures, suitable dopants, etc. should play a different role in various FE performances, including E_{to}, current density at a fixed field, FE stability, and device lifetime [219, 258]. Thus, the issue of balancing FE performances and above-discussed factors seems to be crucial for the emitter optimization. However, scarce works shed light on these important topics.

Recently, orientation-ordered single-crystal needle-shaped SiC nanowire arrays were successfully fabricated using pyrolysis of polyureasilazane process in our group [42, 95]. Different from the preparation of the above-discussed SiC nanoarrays, the synthesis of SiC nanoarrays was conducted on SiC wafer substrate based on a homoepitaxial growth, which is high controllable for fabricating the SiC nanostructure with perfect orientation perpendicular to the substrate, sharp tips, and proper doping. The detailed growth process and SEM observations of obtained N-doped and B-doped SiC nanoneedles arrays were discussed in Sect. 8.2.6.1. The E_{to} (at a current density of 10 μA/cm^2) was measured for the N- and B-doped arrays ensembles to be 1.50–1.95 V/μm [42] and 1.92–2.10 V/μm [95] with the changes of the anode-cathode separation distances from 600 to 900 μm and 500 to 800 μm, respectively. And the E_{to} of two types of nanoarrays decreased from 1.50 to 0.94 V/μm [42] and 1.92 to 0.98 V/μm [95], respectively, with an increase of the temperature from RT to 500 °C. In addition, the current emission could be enhanced significantly from 40.0 to 506.7 μA/cm^2 (at fixed electric field of 1.51 V/μm) [42] and 26.67 to 2846.67 μA/cm^2 (at 2.0 V/μm) [95], respectively, upon increasing the temperature from RT to 400 °C.

Especially, the current emission stabilities of the B-doped SiC nanoarrays at RT and 200 °C are only ~6.5% and 7.8% over the long monitoring time of 8 h,

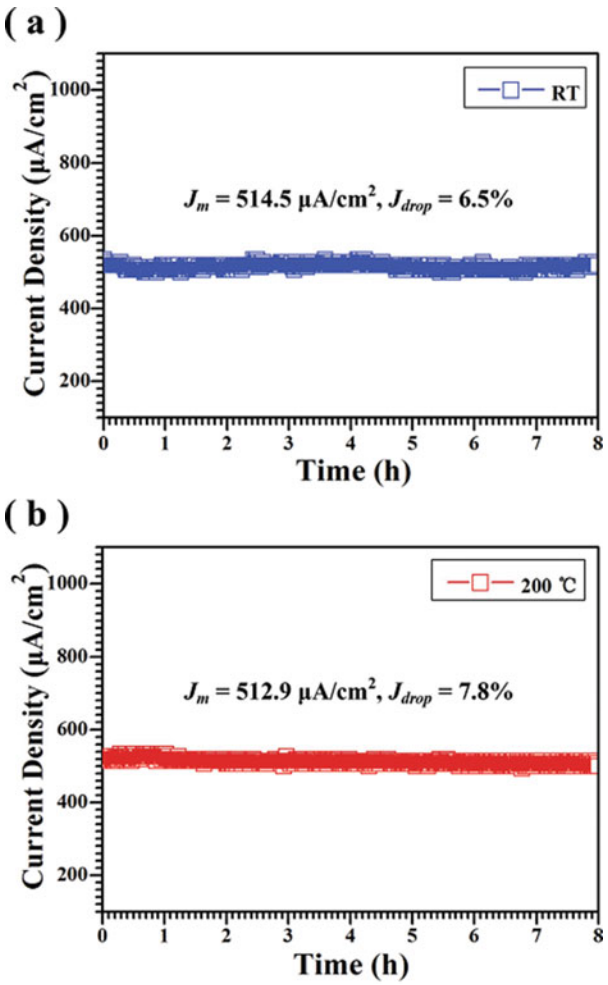

Fig. 8.29 The current emission stabilities of B-doped SiC nanoarrays over 8 h at (**a**) RT and (**b**) 200. (Reproduced from Ref. [49] by permission of the Royal Society of Chemistry)

respectively, as depicted in Fig. 8.29. It is easy to note that the current fluctuations show a slight change (1.3%) between RT and 200 °C. In addition to benefitted from the aligned configuration, such stable FE performance should be also related to the B dopants, which generated more stable B-C atom pairs compared to SiC species in interstitial sites, leading to a higher solubility and better heat dispersion and electrical conductivity [97, 263, 264]. This work might open a door to advance the exploration of robust SiC field emitters with low E_{to} and a high stability, which could be used as robust electron sources able to endure the harsh working conditions of high temperatures [95].

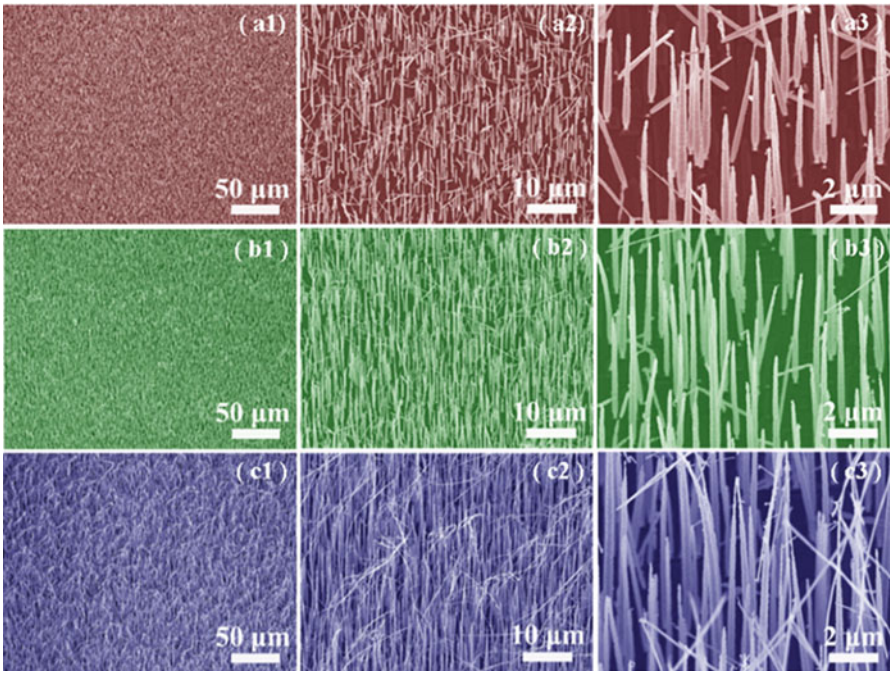

Fig. 8.30 Typical SEM images of the as-synthesized SiC nanoarrays of sample 1 (**a1**–**a3**), sample 2 (**b1**–**b3**), and sample 3 (**c1**–**c3**) under different magnifications, respectively. The colors draw the eyes to the different samples. (Reprinted with permission from Ref. [49]. Copyright 2015, American Institute of Physics)

Screening of the applied electric field on the apex of an emitter by the neighboring emitters comes into effect when interemitter spacing decreases from twice the emitter height, according to recent calculations and discussions [252, 265, 266]. If the density was too low or too high, in an array, the emission was not strong and was inhomogeneous. The former may not have enough emitters, and the latter may be due to the screening effect. Furthermore, to take full advantage of the geometrical field enhancement provided by the high aspect ratio of the SiC emitters [45], it would be ideal to produce SiC nanowire arrays that are very tall with small radius and medium separation.

Considering how to grow highly oriented SiC nanowire emitters with designed densities and shapes, we exploitation of well density controlled of needle-shaped SiC nanowire arrays via an Au-catalyzed pyrolysis of polyureasilazane based on VLS growth process [49]. The key point is a control of the thicknesses of Au catalysts films through sputtering the Au on the SiC wafer substrate with different times. Figure 8.30 shows SEM images of the as-grown needle-shaped SiC nanowire arrays under different magnifications. Samples 1, 2, and 3 refer to the products fabricated with tailored thicknesses of Au catalytic films in 50, 70, and 90 nm,

respectively. Large-scale and high-uniform wire-like SiC nanostructures were grown on the whole SiC wafer substrate, as verified by a low-magnification SEM images in Fig. 8.30a1, b1, and c1. The average densities of samples 1–3 are ca. ~2.9×10^7, 4.0×10^7 and 5.7×10^7 wire/cm^2 (Fig. 8.30a2, b2, and c2) with the increase of the thicknesses of the Au films, respectively. The three types have the unique morphology features with small roots, tapered bodies, and sharp tips, as Fig. 8.30a3, b3, and c3 shows.

For the formation of nanowire-density-dependent SiC nanoarrays, firstly, the Au films would transfer to catalytic drops by agglomeration under high temperatures. They are initially small and closely spaced. Subsequently, they would coarsen driven by surface energy minimization as the reaction progress, which occurs through participation of the residual Au film and the vapor phase. Meanwhile, smaller drops tend to shrink and disappear with their mass being redistributed to larger drops. Finally, this process leads to the average size of drops increase as well as the average drops spacing increase [49]. That is to say, the Au films with various thicknesses would cause the formation of Au catalytic droplets with different sizes and space distributions, which enable the growth of the SiC nanoarrays with various sizes and aspect ratios as well as different densities on the SiC wafer substrate [49].

Figure 8.31a and b shows *J-E* plots and corresponding *F-N* plots of samples 1–3 with the anode-cathode separation distance fixed at 600 μm. The curves own the similar trend, and their relatively smooth and consistent curves indicate that the SiC nanoarray of three samples all exhibit excellent stability. Among these samples, sample 2 exhibits the best FE properties with the lowest E_{to} and E_{thr} (at a current density of 10 μA/cm^2 and 1 mA/cm^2, respectively), as Fig. 8.31c and d shows, suggesting that a suitable emitter density could favor the enhanced electron emission from the SiC nanoarrays with improved emission sites and limited field screening effects. Furthermore, sample 2 exhibits the highest β (3340) corresponding to the best FE performance, as compared to those of sample 1 (3300) and sample 3 (3217). The *J-E* curves and the variations in E_{to} of sample 2 with anode-cathode separation distance fixed at 600–800 μm are depicted in Fig. 8.31e and f. The similar *J-E* curves and E_{to} further verified sample 2, with a suitable nanowire density of 4.0×10^7 wires/cm^2, could effectively limit the screening effect of the electron emission from the present SiC nanoarrays.

8.3.1.6 Enhanced FE Properties of SiC Nanowires with Other Morphologies

Besides shown examples, some others facile routes have also been developed to contribute the enhanced FE properties by several groups. Here, we briefly list some typical works on the FE properties of SiC nanowires so far.

1. SiC Nanowires-Based Core-Shell Structure Field Emitters

Previous research has shown the FE property of nanowires was improved (with the reduction in the turn-on and threshold electric fields) by coating the emitter

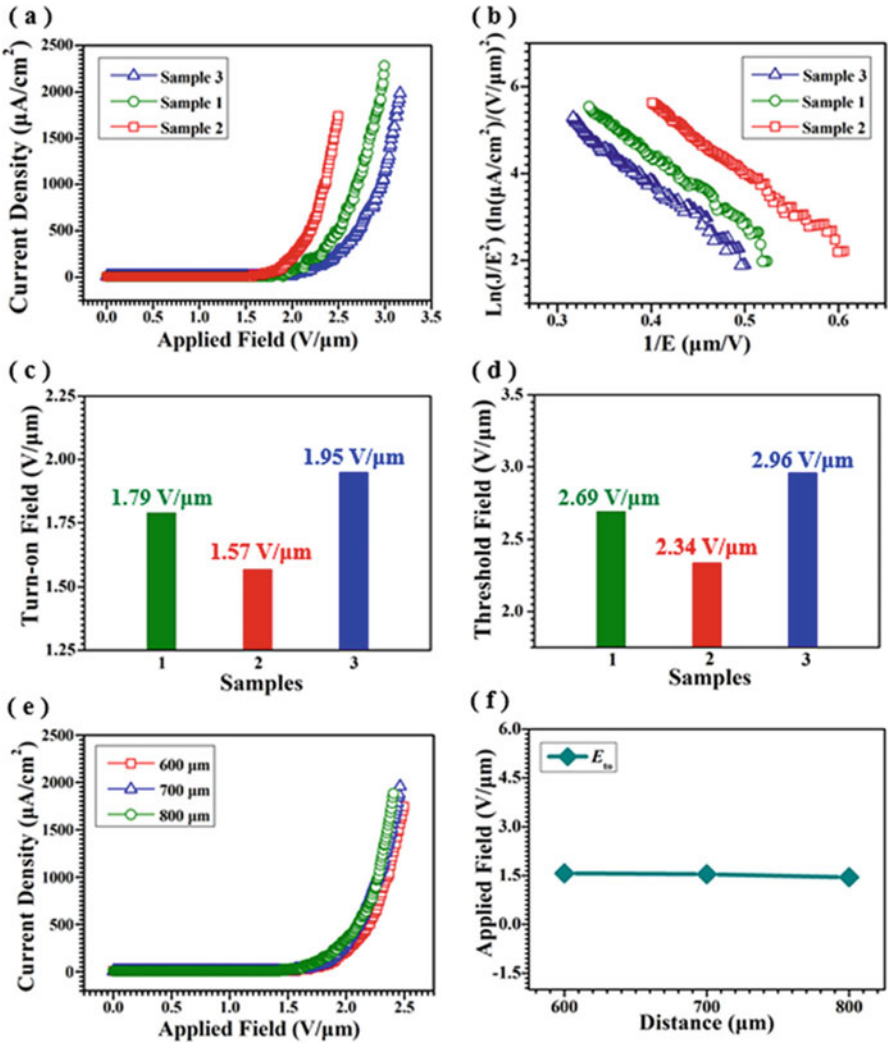

Fig. 8.31 FE properties of the samples 1–3 with different nanowire densities. (**a**) Typical *J-E* curves of samples 1–3 with the anode-cathode separation distance fixed at 600 μm. (**b**) The corresponding *F-N* plots of samples 1–3. (**c** and **d**) The variations of E_{to} and E_{thr} of samples 1–3. (**e**) The *J-E* curves and (**f**) the variations in E_{to} of sample 2 with the anode-cathode separation distances fixed at 600–800 μm. (Reprinted with permission from Ref. [49]. Copyright 2015, American Institute of Physics)

surface with low (or negative) electron affinity, chemically stable, or dielectric layer materials [267–270]. For example, Yi and co-workers reported the enhanced field emission properties of CNTs by coating them with a low electron affinity SiO_2 (0.6–0.8 eV) or MgO (0.85 eV) layer [267].

Based on the conception, recently, it has been reported that SiC nanowire-based core-shell structures, including Al_2O_3/SiC [271], SiO_2/SiC [272, 273], C/SiC [55, 64], BN/SiC [65], and C/SiO_2/SiC [274], show enhanced field emission properties with low E_{to} and E_{thr} compared with corresponding bare SiC nanowires core. Zhang and co-workers presented a chemical vapor reaction route for growing SiC nanowires with the amorphous carbon (a-C) coating [55]. This kind of SiC@a-C coaxial nanocables with rough and sharp surface showed low E_{to} and E_{thr} and high emission current stability. Tang and co-workers reported that the turn-on field of SiC nanowires will be reduced by the BN coating due to their high antioxidation ability [65]. Ryu et al. studied the influence of different thickness of SiO_2 shell on the field emission property of SiC nanowires [272]. The results of FE measurement of SiC/SiO_x nanocables also indicated the low turn-on and threshold electric field [142]. The detailed key performance parameters of these novel SiC nanowire-based core-shell nanostructure field emitters are summarized in Table 8.12.

2. SiC Nanowire Field Emitters with Other Complicated Configurations

For the FE applications, as discussed above, the morphology of field emitters is crucially important for the enhancement of electron emission [59]. Up to now, some other excellent SiC nanowire emitters with complicated configurations have also been developed. For examples, Shen and co-workers synthesized single-crystalline bamboo-like β-SiC nanowires with hexagonal cross sections by thermal evaporation of mixed SiO + C + GaN powders in an Ar atmosphere [36]. Studies found that the SiC nanowires are composed of hexagonal stems decorated with larger diameter knots along their whole length with the [111] growth direction. Field emission measurements suggested a turn-on field of ~10.1 V/μm for this kind of SiC nanowires with rough surfaces, existed stacking faults in the knot parts, and high aspect ratio [36]. Later, they successfully synthesized the hierarchical single-crystalline β-SiC nanoarchitectures using a catalyst-assisted thermochemical process [110]. The central nanowires have diameters of ~10–20 nm, and the branched nanoplatelets have thickness of 5–10 nm, as shown in Fig. 8.10. A turn-on field of about 12 V/μm was detected. Deng and co-workers reported the synthesis of SiC/CNTs heterostructured array field emitters by using energetic Si ion irradiation process [186]. FE study showed that the turn-on and threshold fields were only 0.726 and 1.164 V/μm, respectively, for the silicon ion irradiation dose of 8.6×10^{16} ions/cm^2.

8.3.1.7 FE Properties of Flexible SiC Nanowire Cathodes

1. Fabrication of Flexible FE Cathode

Among the family of field emitters, flexible counterparts are attracting more and more attention due to their wide and unique applications in roll-up field emission displays, electronic textiles, large-area circuits on curved objects, and so on [226, 245, 275–277]. Based on previous reports, two interesting strategies have been developed for the fabrication of flexible field emitters.

Table 8.12 The key performance parameters of SiC nanowire-based core-shell nanostructure field emitters reported in the literature

SiC emitters	Synthesis process	FE properties [a]	Refs.
SiC@a-C coaxial nanocables	Chemical vapor reaction method with the assistance of the Fe-Ni bibasic catalyst	$E_{to} = 0.5$ V/μm, $E_{thr} = 2.1$ V/μm (at 10 mA/cm^2). The fluctuation of the nanocables is less than 5% at 1.8 V/μm over 120 min	[55]
1D hierarchical SiC@SiO_2@C nanostructures	Ni-assisted CVD method	$E_{to} = 0.8$ V/μm, $E_{thr} = 2.6$ V/μm (at 10 mA/cm^2)	[274]
SiC@Al_2O_3 core-shell epitaxial nanowires	Simply heating evaporating Al source and C source on silicon substrate	$E_{thr} = 13.8$ V/μm (at 10 mA/cm^2). The sample shows stable emission property when the current density reaches as high as 16 mA/cm^2	[271]
SiC/SiO_2 core-shell nanowires with different shapes	Reaction between methane and silica using iron as catalyst	$E_{to} = 1.28$–1.56 V/μm. The emission current density of different shaped SiC/SiO_2 nanowires can be up to 0.4–0.72 mA/cm^2 at 2.2 V/μm	[273]
Core-shell SiC/SiO_2 nanowires	Heating NiO-catalyzed Si substrates	$E_{to} = 3.3$ V/μm (10 nm SiO_2-coated SiC) $E_{to} = 4.5$ V/μm (20 nm SiO_2-coated SiC)	[272]
SiO_x/SiC nanocables	Thermal evaporation of C and Si powders by using Fe_3O_4 as catalysts	$E_{to} = 3.2$ V/μm at the vacuum gap of 200 μm $E_{to} = 1.1$ V/μm at the vacuum gap of 1000 μm	[142]
Carbon-coated SiC nanowires	Heating NiO-catalyzed Si substrates	$E_{to} = 4.2$ V/μm The field emitters showed uniform emission image	[64]
SiC nanowires with BN coating	A VLS process using Ni as catalyst, SiO and B_2O_2 gases as the precursors	$E_{to} = 6$ V/μm. The maximum error of currents was less than 5% with number of the repeated measurements	[65]

[a] E_{to} and E_{thr} required to generate an emission current density of 10 μA/cm^2 and 1 mA/cm^2, respectively. If other values are used, it is separately mentioned

The first is the directly grown method (one-stage process), which can be interpreted as the low-dimensional nanostructures were directly fabricated on the flexible substrates. There are two commonly used flexible substrates for the growth of flexible emitters, that is, polymers [278, 279] and carbon fabric [280, 281]. The polymers were the most extensively explored substrate materials approach to fabricate flexible cathode due to their high flexibility and low cost [282, 283]. However, limited by their low melting points, the polymer are not proper for establishing some flexible field emitters that prepared based on conventional CVD, thermal evaporation, or carbothermal reduction routes, because they are can not survive the high temperatures necessary for the growth conditions. As compared to polymers, carbon fabrics can endure very high temperatures with excellent thermal stability and

electrical conductivity. Thus, carbon fabrics have been widely utilized as flexible substrate for the direct growth of low-dimensional nanostructures under high temperatures [239, 247, 284–286].

The second is the novel transfer method, which was a two-stage process [287]. The nanostructure emitters were first grown on a rigid substrate (such as the SiO_2/Si or substrate coated with Ni or Cu films [220, 288]) and then have been exfoliated or etched away from the initial substrate and transferred onto other flexible substrates [289–291]. Compared with the directly grown method, although more complicated, this transfer process is much advantageous for fabrication of flexible cathode due to effectively excluded the limited selection of the flexible substrate. Furthermore, the exfoliated or etched field emitters could also be transferred onto the transparent substrate, which favor the exploration of flexible and transparent field emission cathodes, thus showing great potential for the fields of field emission-based flexible and transparent electronics [226, 292, 293].

Up to date, most of the reported SiC nanowire-based emitters were based on rigid substrates (e.g., graphite, silicon, and SiC wafers), which limited their applications in flexible emitters. As described in Sect. 8.2, the synthesis of SiC nanowires is most executed under high temperatures above 1000 °C, but the polymer substrate cannot endure these high-temperature routes. Excitingly, to the best of our knowledge, several works have achieved the growth of SiC low-dimensional nanostructures on carbon fabric flexible substrate in recent years [46, 57, 92, 236, 245]. These flexible cathodes presented high flexibility and robust, mechanical and electrical stability, as well as low E_{to} and high electron emission stability, which could push forward their practical application as flexible FE nanodevices.

2. FE Properties of SiC Flexible Cathode

In 2012, for the first time, Wu and co-workers fabricated the β-SiC flexible cathode by direct growth of the tapered SiC nanowires on the surface of flexible carbon fabric by a CVD process based on Fe-assisted VLS mechanism [57]. The obtained nanowires had a feature of zigzag faceting over the wire surfaces. The authors attributed such created faceting to a quasiperiodic placement of twinning boundaries along the wire axis, which was explained by surface energy minimization during the growth process. More importantly, the carbon fabric still preserves the flexibility after the reaction at high temperature, and it can even be bended and twisted [57]. Figure 8.32 shows the *J-E* and corresponding *F-N* plot of the SiC flexible cathode. A relatively low turn-on field is extrapolated as 1.2 V/μm at a current density of 10 μA/cm^2 from Fig. 8.32a, while a high field enhancement factor of 3368 is calculated from the slop of *F-N* curve in Fig. 8.32b. This work suggests that directly grown SiC nanowire on the carbon fabric substrate could be an effective strategy to fabricate the SiC flexible cathode. Later, Zhang and co-workers reported the growth of quasi-aligned, single-crystalline N-doped 3*C*-SiC nanoneedles on carbon fabric [92]. The SiC emitters possess a tapered structure with tiny clear tips with sizes of several to tens of nanometers. The cathode is mechanically and electrically robust and can withstand mechanical bending up to 500 times [92]. This flexible cathode showed extremely low turn-on field in the range of

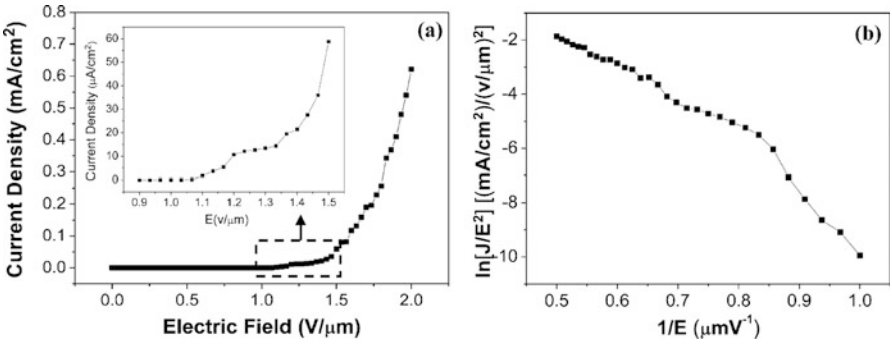

Fig. 8.32 (**a**) Field emission current density versus electric field (*J-E*) curve of tapered SiC nanowires. The inset shows that the turn-on field is ~1.2 V/μm. (**b**) Corresponding Fowler-Nordheim (*F-N*) plot. (Reprinted with the permission from Ref. [57]. Copyright 2011 American Chemical Society)

0.5–1.6 V/μm with an average of 1.1 V/μm and a high field enhancement factor of about 6.5×10^3. The authors suggested that the sharp tips and N-doping are advantageous for the excellent FE of flexible cathode [92].

By checking the pre-existing experiments, we developed a range of novel SiC nanowire flexible cathodes on the carbon fabric substrate with totally high FE performances via the catalyst-assisted pyrolysis of polymeric precursor [25, 44, 46, 236, 245]. The N-doped 3*C*-SiC nanowires were fabricated firstly using the introduced mixture atmosphere of 5% N_2 and 95% Ar carrier gas as the N dopant source [44]. The carbon fabric preserves a high flexibility after the pyrolysis treatment under 1500 °C (Fig. 8.33a, b). The nanowires deposited homogeneously on the fabric substrate (Fig. 8.33c–g) and presented quasi-aligned configuration based on the VLS growth mechanism (Fig. 8.33g–h). With respect to the decreased work function induced by the N dopants, this flexible cathode showed very low turn-on fields of 1.90–2.65 V/μm and threshold fields of 2.53–3.51 V/μm [44].

Aimed to exploration of flexible SiC nanowires with enhanced FE properties by taking advantage of local field enhancement effect, we controlled growth of these N-doped SiC nanowires with clear and sharp tips by tailoring the cooling rates [52]. The turn-on field of obtained sharp nanowires is markedly reduced as compared to those of conventional nanowires, exhibiting the best FE performance with a turn-on field of 1.15 V/μm. The turn-on and threshold fields of N-doped SiC flexible emitters decrease from 1.37 to 0.67 V/μm and 1.87 to 0.96 V/μm with the temperature raised from room temperature (RT) to 400 °C, respectively, and the current emission stabilities under RT and 200 are only 7.7% and 14.1%, respectively [25]. These results suggested stable current emission of the *n*-type SiC nanowires under high-temperature harsh conditions.

Directed by the enhanced FE properties of SiC emitters though doping and needle-shaped growth [25, 44, 52], we further fabricated the needle-shaped 3*C*-SiC nanowires on carbon fabric with tailored N-doping concentrations by simultaneously controlling the N_2/Ar mixture atmosphere as well as cooling rate [46]. These

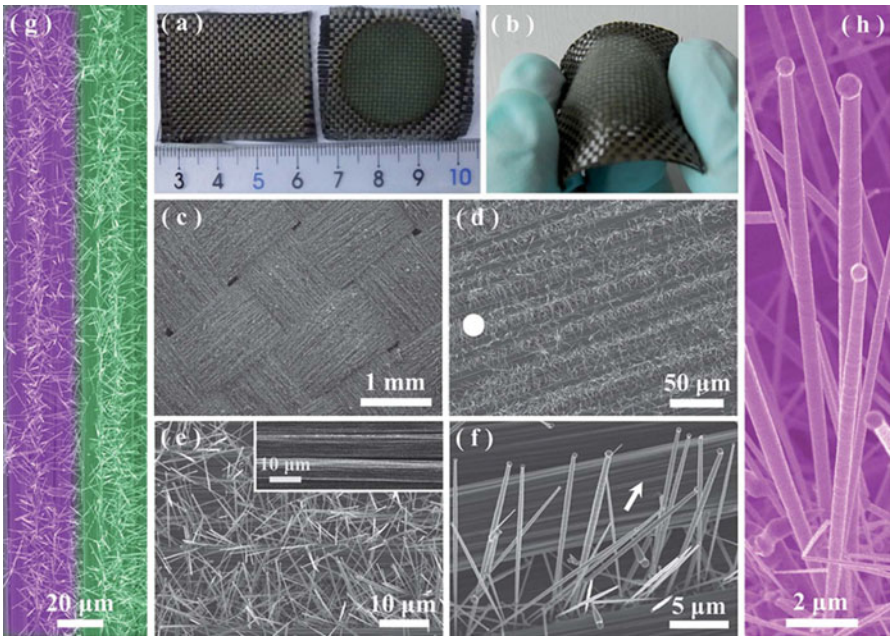

Fig. 8.33 (**a**) A typical digital photo showing the change of the carbon fabric substrates before and after pyrolysis treatment at 1500 °C. (**b**) The curved carbon fabric after pyrolysis. (**c**–**f**) Typical SEM images of the as-synthesized SiC quasi-aligned nanoarrays under different magnifications. (**g**) A representative enlarged image showing the growth of the SiC arrays on the substrate. (**h**) A typical SEM image under high magnification, showing the characteristics of the grown SiC wires. (Reproduced from Ref. [44] by permission of the Royal Society of Chemistry)

nanowires were quasi-aligned arrays, rather straight, and all presented ultra-sharp tips. The N concentrations of nanowires were measured to be 4.39 *at%*, 6.01 *at%*, and 7.58 *at%* when the volume ratio of mixture atmosphere N_2/Ar in the pyrolysis procedure was carefully tailored at 5:95, 10:90, and 15:85 [46]. These flexible emitters can be bended in various states more than 200 times without noticeable structural damage, as Fig. 8.34a shows. From Fig. 8.34b and c, it is easy to note that the E_{to} and E_{thr} of obtained flexible cathode show negligible variations when subjected to repeated bending and various bending states, confirming it to be mechanically and electrically robust. As shown in Fig. 8.34g, both E_{to} and E_{thr} decrease monotonically in the order of concave, flat, and then convex structures (schematic diagram is shown in Fig. 8.34d–f). Compared with their concave and flat counterparts, the slight decrease of E_{to} and E_{thr} in convex geometry is attributed to a weaker screening effect induced by neighboring emitter sites. There is no obvious change in current fluctuations, as Fig. 8.34h shows, suggesting that the stresses of the substrate caused by different bending states do not have any significant effect on emission stability. The present *n*-type SiC nanoneedles could be an excellent candidate for robust field emitters with high flexibility, low E_{to} and E_{thr}, and high stability.

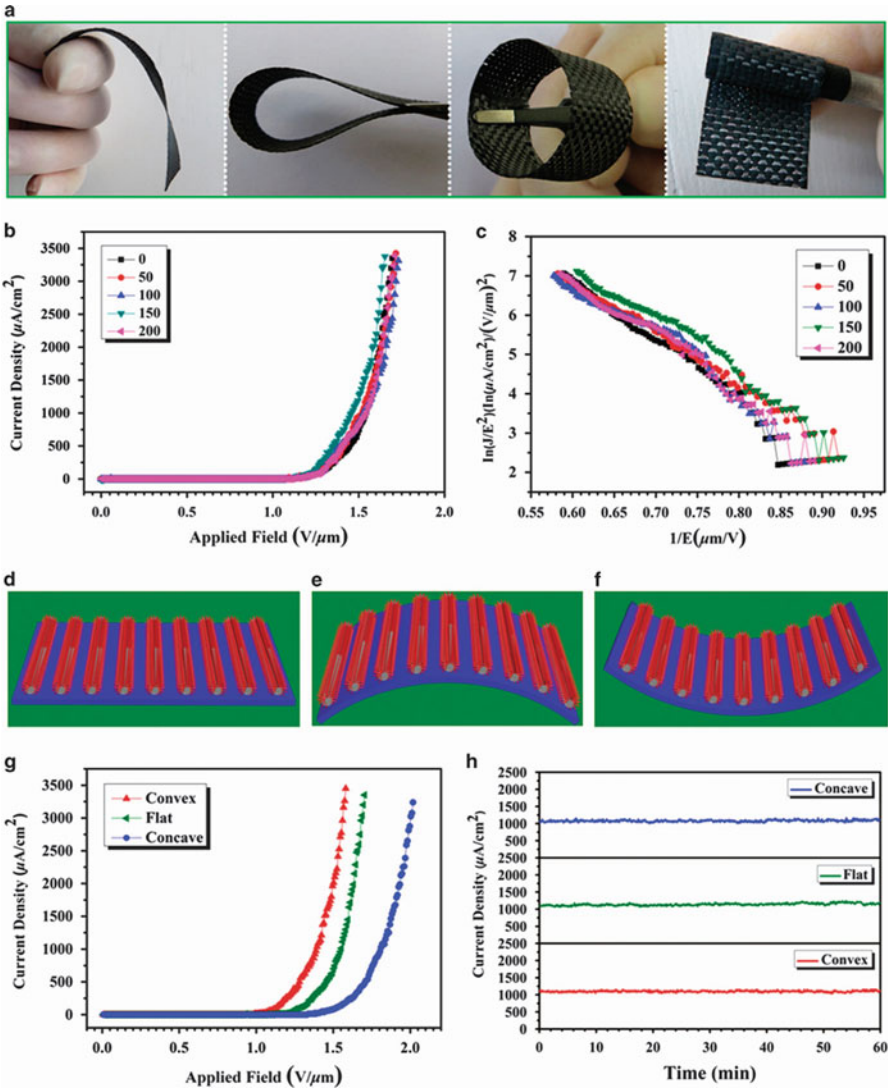

Fig. 8.34 (**a**) Digital photographs showing the high flexibility of needle-shaped SiC nanowires grown on carbon fabric with various bended states. (**b**) *J-E* curves and (**c**) *F-N* plots of flexible cathode after 0, 50, 100, 150, and 200 bending cycles. (**d–f**) Schematic illustrations of flexible cathode in concave, flat, and convex states, respectively. (**g**) *J-E* curves of flexible cathode in concave, flat, and convex states. (**h**) Field emission stability of cathode in concave, flat, and convex states. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [200], copyright 2016)

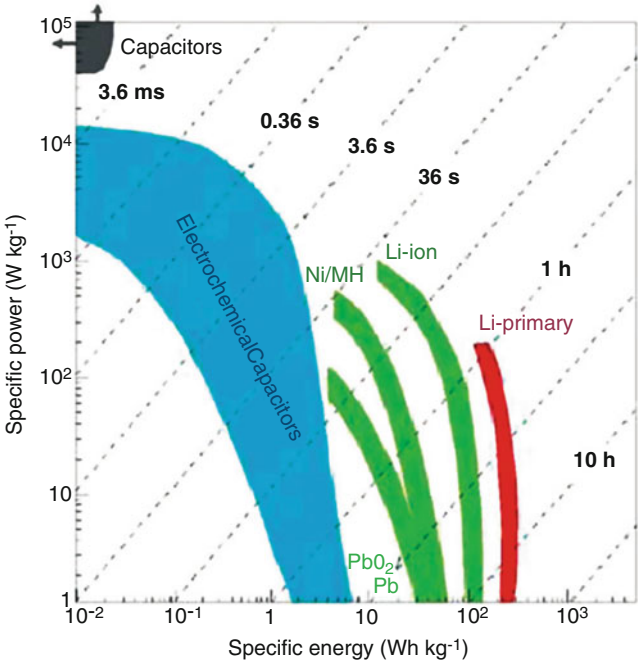

Fig. 8.35 Ragone plot showing the specific power against specific energy for various electrical energy storage systems. (Reprinted by permission from Macmillan Publishers Ltd.: Ref. [294], copyright 2008)

8.3.2 Supercapacitors

Supercapacitors (SCs) are a new type of energy storage device between traditional capacitors and batteries. Due to their high power, excellent reversibility, capability, long cycle life, and low maintenance costs [294], SCs have drawn considerable attention in recent years and can be used independently or coupled with batteries. As illustrated in Fig. 8.35, where various energy conversion and storage devices are compared and presented in the simplified "Ragone plot" [294]. SCs occupy an important position in terms of the specific power densities. SCs typically deliver a power density that is of an order magnitude larger (10 kW/kg) than that of lithium ion batteries. Since SCs store electrical charge only at the electrode surface, rather than the entire electrode, they tend to have higher power densities and lower energy densities compared to batteries [295–297]. The charge-discharge reaction is not limited by ionic conduction into the electrode bulk; therefore, SCs can be run at high rates and provide high specific power. This makes it ideal for many applications, such as electric vehicles, electric tools, digital communication devices, mobile phones, pulse laser technique, and storage of the energy generated by solar cells [295, 297, 298]. According to energy storage mechanism, SCs can be classified into

either of the following two categories: the electrical double-layer capacitors (EDLCs) and pseudocapacitors [299]. The EDLCs store energy by ion electrosorption on porous electrodes, which arising from the charge separation at the electrode/electrolyte interface are usually composed of carbon materials or carbon-based hybrid materials with high-surface areas and suitable pore sizes, whereas faradic supercapacitor materials, such as titanium oxide [300, 301], manganese oxide [302], indium oxide [295], tin oxide [303], and ruthenium oxide [304], not only store energy like an EDLC but also display electrochemical faradic reactions between ions and electrode materials in the suitable potential window.

Aimed to develop SCs performance, especially its specific energy while retaining its basic high specific power, many researchers have focused their efforts on improving the properties of electrode materials [305–307]. Therefore, in order to realize a high-performance supercapacitor electrode, factors that determine the specific capacitance, such as rate capability and cycle stability need to be mentioned here. (1) Surface area: Since charges are stored on the surface of the supercapacitor electrodes, an electrode with a higher surface area leads to an improved specific capacitance. Nanostructuring of electrode materials is a feasible method to considerably improve the surface area of the electrodes [308]. (2) Electronic and ionic conductivity: As specific capacitance and rate capability are considerably dependent on both electronic and ionic conductivities, a high electronic and ionic conductivity will contribute to maintain the rectangular nature of cyclic voltammetry (CV) curve and symmetricity of galvanostatic charging-discharging (GCD) curves.

8.3.2.1 Supercapacitors with SiC Nanowire Electrodes

SiC nanowires, as a promising semiconductor in many areas of futuristic nanoscience and technology, have been widely studied for outstanding electrode material for long-lifetime and high-temperature electrical double-layer capacitors [30, 309, 310]. SiC nanowires supercapacitor electrodes exhibit high surface efficiency, rate capability, and cycle lifetime because of their excellent electrochemical performance, high specific surface area, and compatibility with various electrolytes. Alper et al. reported the supercapacitor electrodes with excellent cycle stability [309], which are made of SiC nanowires grown on flexible carbon fabric. A high areal capacitance of 23 mF/cm^2 is achieved at a scan rate of 50 mV/s under room temperature, and capacitances increase with the rise of the working temperature. Owing to the excellent thermal stability of SiC nanowires and carbon fabric, no observable decrease of capacitance occurs at room temperature (20 °C) after 105 cycles [309]. To date, it is still challenging to provide cost-efficient solution to further improve the energy, power densities, and cyclability of supercapacitors, especially at ultrafast rates and even well-run at arbitrary harsh environments.

Supercapacitors based on N-doped SiC have shown remarkable supercapacitive performance in both aqueous and organic electrolytes with high cyclic stability, energy density, and power density. Chen and co-workers reported the fabrication of quasi-aligned single-crystalline 3*C*-SiC nanowire array with tailored shapes and

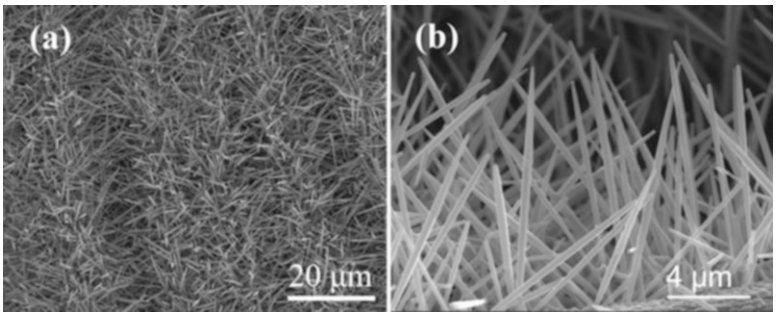

Fig. 8.36 Typical SEM images of obtained *d*-SiCNWs under different magnifications. (Reprinted with the permission from Ref. [90]. Copyright 2015 American Chemical Society)

N-doping [90]. Large-scale SiC nanowires were directly grown on the surface of flexible carbon fabric via a well-controlled co-assisted vapor-liquid-solid (VLS) growth process. As Fig. 8.36 shows, the quasi-aligned growth of N-doped SiC nanowires (*d*-SiCNWs) nanoarrays had diameters ranging from 100 to 300 nm and an average length of 12 μm. The authors found out that the conductivity of SiC nanowire arrays can be substantially enhanced by N-doping, ranging from 7×10^3 to 8.6×10^3 S/m. Figure 8.37a–i shows the electrochemical characterization for electrochemical energy storage at scan rates ranging from 10 to 20,000 mV/s. Even at an ultrafast scan rate of 20,000 *m*V/s, the CV remains nearly rectangular in shape (Fig. 8.37b, c). And this rectangular shape can kept over a wide range at least up to 50,000 mV/s (Fig. 8.37d). The measured areal capacitances are higher with values of 4.8 and 4.7 mF/cm^2, in aqueous and gel electrolytes, respectively. When the scan rate changed from 10 to 1000 mV/s, *d*-SiCNWs electrode retained 77% of its capacitance, exhibiting a higher rate capacitance (Fig. 8.37e). Even at an ultrafast rate of 20,000 mV/s, the *d*-SiCNWs still delivered an areal capacitance of 2.38 mF/cm^2. In marked contrast, undoped one gave such capacitance of only 0.62 mF/cm^2. The excellent performance of *d*-SiCNWs can be explained by the unique macro- and mesoscale-ordered pores of interstitial regions within the array packing structure of *d*-SiCNWs, which helps minimize the pathway for ion diffusion from the electrolyte to the electrode material on the relevant time scale [90]. Meanwhile, N-doping could favor a more localized impurity state near the conduction band edge that greatly improves the quantum capacitance and hence increases the bulk capacitance without sacrificing its high-power capability [90].

8.3.2.2 Supercapacitors with SiC Nanowire Composite Electrodes

The criteria for designing a high-performance supercapacitor electrode is now widely accepted that a directional design/fabrication of the electrode materials [311–314]. Generally, researchers are more likely to tailor electrode materials with desired configuration aim to enhancing ion/electron conductivity, reaction kinetics,

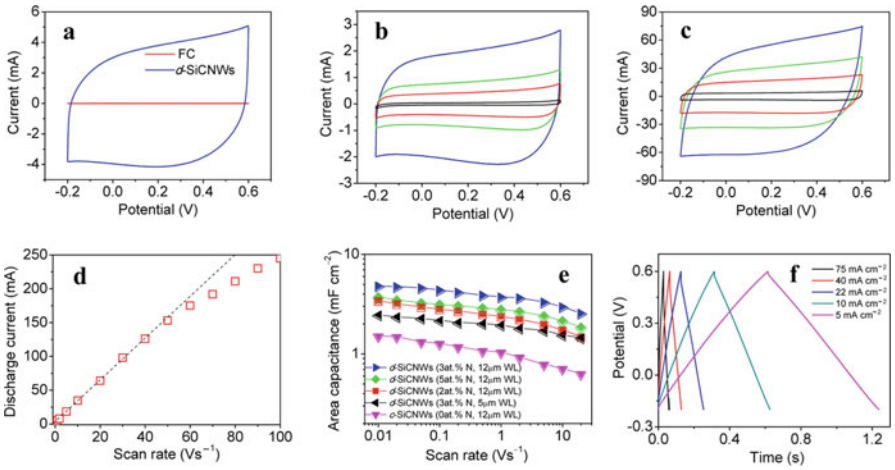

Fig. 8.37 Electrochemical performance of *d*-SiCNW electrodes in aqueous electrolyte. (**a–c**) CV profiles of the carbon fabric and *d*-SiCNW electrodes at a scan rate of 1000 mV/s, and *d*-SiCNW electrodes at scan rates ranging from 10 to 20,000 mV/s ((**b**) 10 (black), 100 (red), 200 (green), 500 mV/s (blue); (**c**) 1000 (black), 5000 (red), 10,000 (green), 20,000 mV/s (blue)). (**d**) A plot of the discharge current as a function of the scan rate (red square line). Linear dependence (dashed line) is observed up to at least 50,000 mV/s. (**e**) Evolution of the specific capacitance of SiC nanowires-based SCs as a function of the scan rate, dopant, and wire length, respectively. (**f**) GCD curves of supercapacitors, operated with current densities ranging from 5 to 75 mA/cm^2. (Reprinted with the permission from Ref. [90]. Copyright 2015 American Chemical Society)

and mechanical stability [315]. But the capacitance of supercapacitors is largely restrained by the limited ion adsorption capability of SiC, resulting in relatively low gravimetric energy density.

A composite material containing backbone material and cost-effective pseudocapacitive material can change this situation, because of its good conductivity and dual energy storage mechanism [316–319]. It is beneficial to the power/energy output due to hierarchical porous system with different pore diameters, high-surface areas, high conductivity network structure, as well as binder-free and additive-free characteristics. Therefore, many works focus on the design of multicomponent electrode materials combining energy storage of electrostatic attraction and faradic reaction, in which active materials such as metal oxides or conducting polymers can enhance the capacitance remarkably. Some researchers have tried to fabricate SiC nanowire-based composite electrode by grown pseudocapacitive materials on the SiC nanowires surface [30, 320]. The SiC served as skeletons, which not only allow electroactive materials distributed uniformly on their surfaces, shorten the diffusion distance for electrolyte ions, and facilitate electron transfer but also act as a buffering phase for the volume changes of electrodes and effectively impede the possible electrode structures corrosion and collapse during continuous charge-discharge process. For instance, the SiC@$Ni(OH)_2$ electrode presented a high specific capacitance of 1724 F/g at a charging/discharging current density of 2 A/g [30]. In

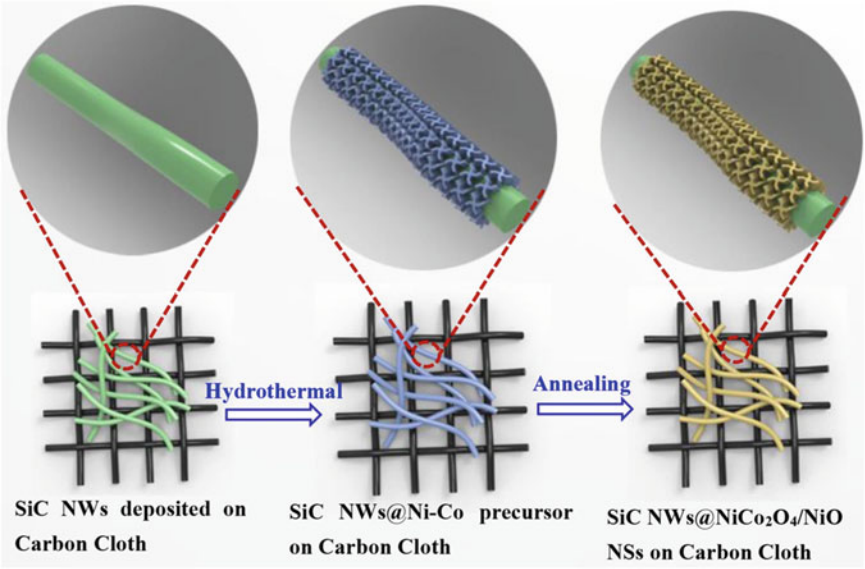

Fig. 8.38 Schematic illustration of the formation of SiC NWs@$NiCo_2O_4$/NiO NSs on CC via hydrothermal reaction and subsequent annealing treatment. (Reprinted with the permission from Ref. [320]. Copyright 2016 American Chemical Society)

addition, the highest energy density of 72.4 Wh/kg and lowest power density of 0.55 kW/kg are achieved, respectively. The electrode still has a specific capacitance of 1412 F/g at an ultrahigh current density of 100 A/g.

Zhao and co-workers successfully employed SiC nanowires (SiC NWs) directly deposited on carbon cloth (CC) as scaffolds [320]. Then the scaffolds were used for the growth of $NiCo_2O_4$/NiO nanosheets (NSs) through combining a hydrothermal reaction and thermal annealing process. Figure 8.38 shows the schematic illustration of SiC NWs@$NiCo_2O_4$/NiO NSs, which displays that the surfaces of SiC NWs are densely covered by the loose, porous, and ultrathin $NiCo_2O_4$/NiO nanosheets. Figure 8.39a illustrates the CV curves, which revealed that the current signal of SiC NWs@$NiCo_2O_4$/NiO NSs composite electrode is much higher than that of the pure $NiCo_2O_4$/NiO NSs and SiC NWs, suggesting that the composite electrode can display larger energy storage capacity. It also reveals a lower resistance and superior rate capability (Fig. 8.39b). The composite electrode has much longer discharging time, as shown in Fig. 8.39c, revealing their specific capacitance is highly improved. On the basis of the GV curves of composite electrode (Fig. 8.39d), the specific capacitances were calculated, as shown in Fig. 8.39e. It still remains 83.2% of the initial capacitance even at 10 mA/cm^2, indicated that it possesses excellent rate capability. In contrast, the specific capacitance of the pure $NiCo_2O_4$/NiO NSs is only 537 F/g at 10 mA/cm^2, corresponding to approximately 49.7% of the capacitance at 1 mA/cm^2. The SiC NWs offer a strong skeleton for $NiCo_2O_4$/NiO NSs and form a

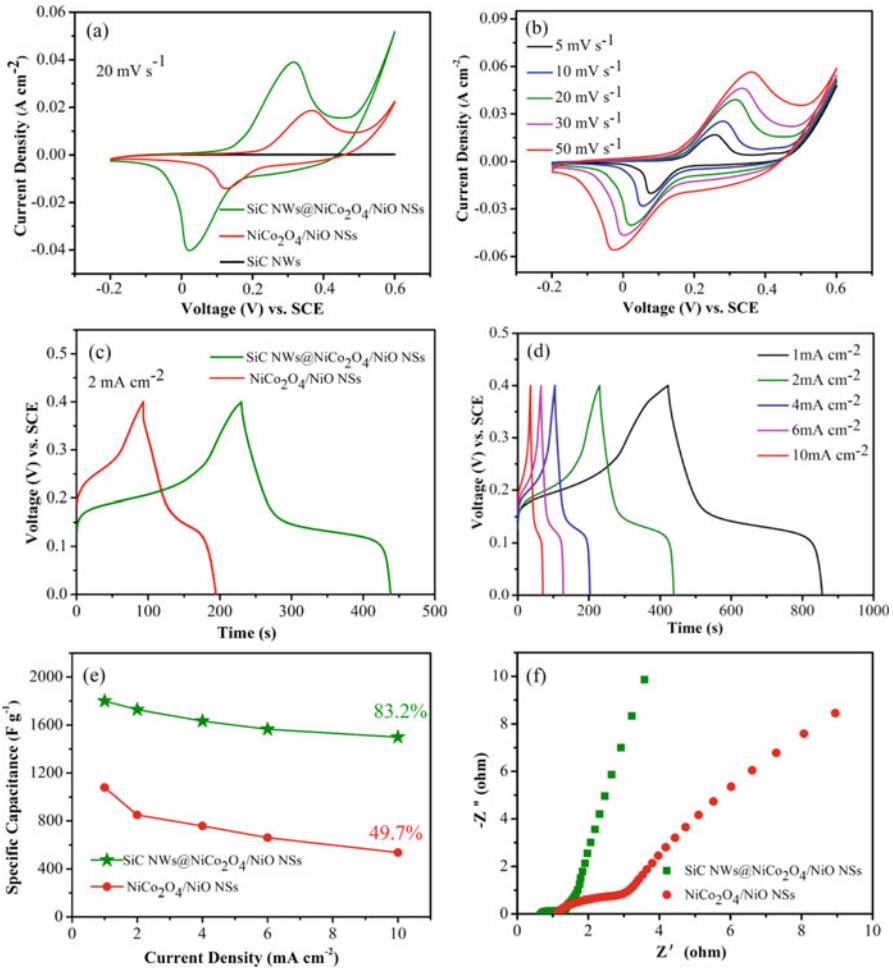

Fig. 8.39 CV curves of (**a**) SiC NWs, $NiCo_2O_4$/NiO NSs, and SiC NWs@$NiCo_2O_4$/NiO NSs on CC at the same scan rate of 20 mV/s and (**b**) SiC NWs@$NiCo_2O_4$/NiO NSs on CC at various scan rates. GV curves of (**c**) $NiCo_2O_4$/NiO NSs and SiC NWs@$NiCo_2O_4$/NiO NSs on CC at 2 mA/cm^2 and (**d**) SiC NWs@$NiCo_2O_4$/NiO NSs on CC at various current densities. (**e**) Comparison of specific capacitance calculated from GV curves as a function of current density and Nyquist plot for the $NiCo_2O_4$/NiO NSs and SiC NWs@$NiCo_2O_4$/NiO NSs on CC, respectively. (Reprinted with the permission from Ref. [320]. Copyright 2016 American Chemical Society)

conductive netty structure, shortening electrolyte ion diffusion pathway and facilitating electron transport (Fig. 8.39f). The ultrathin $NiCo_2O_4$/NiO NSs have high specific surface area and numerous active sites, pledging the expedite ionic intercalate into the electroactive materials for rapid and reversible redox reactions, which results in more efficient charge transportation and large increment for specific capacitance [320]. The SiC NWs are able to avert the erosion and collapse of the

whole electrode structures, highly enhancing their long-term cycling stability. The specific capacitance gradually reduced with an increase in the cycle number, and it is still capable of maintaining 90.9% of the initial capacitance after 2000 cycles, exhibiting a superior stability.

8.3.3 Photocatalysts

Generally, the basic mechanism of a photocatalytic reaction can be ascribed as [34] (i) the generation and separation of charges after the absorption of light, (ii) the transmission of charges, and (iii) the reaction between the photo-generated charge carriers and solution. The charge separation and transfer across interfaces are key aspects in the design of efficient photocatalysts. The efficiency of charge separation is determined by the bandgap and band structure of the semiconductor. Careful construction of structures to maintain the charges being separated and transported efficiently is a common method for the development of photolytic materials with improved characteristics. To achieve this purpose, several strategies, such as surface decoration, doping, structure or morphology modifications, etc., had been developed [321–324].

SiC is an indirect semiconductor with a suitable bandgap (~2.3–3.3 eV) and remarkable chemical stability against hydrolysis. Importantly, these properties are retained when they down to nanoscale. Therefore, SiC nanowires are interesting entities for catalytic activities, where they would require to be exposed to aggressive conditions. The electronic properties and bandgap of SiC nanowires could be easily modified by doping with several elements [47, 97, 245] or surface decoration [67, 150] and thus a promising photocatalyst under visible light irradiation. Therefore, SiC nanowires can play an important role as catalysts in environmental protection through the removal of organic and toxic water pollutants such as dyes and halogenated benzene derivatives in wastewater treatment [325], photocatalytic hydrogen production by split water [34], as well as CO_2 conversion.

8.3.3.1 Photocatalytic Degradation of Pollutants

The possibility of using SiC nanowires for attacking the important global problem of oxidative degradation of organic pollutants from water or other typical gaseous pollutants has been demonstrated [108, 325, 326]. Zhou et al. investigated the photocatalytic activity of the single-crystal 3*C*-SiC/SiO_2 nanowires by measuring the photodegradation rate of acetaldehyde under the UV light irradiation [325]. It exhibited higher photocatalytic activity than the HF-etched, oxide-free SiC nanowires, leading to the efficient decomposition of acetaldehyde with degradation rate reached to 54.99% for 5 h. It is found out that the SiO_2 layer is probably responsible for the enhanced catalytic activity for acetaldehyde because it may serve as a significant source of oxygen for the oxidation of acetaldehyde [325]. 3*C*-SiC

nanowires with hierarchical structure photocatalysts were synthesized via sol-gel carbothermal reduction route by Zhou and co-workers [108]. These hierarchical structures exhibited an enhanced photocatalytic activity that the decolorization rate of methylene blue solution was reached 95% after 5 h under visible light irradiation. The unique hierarchical nanostructures and desired SiO_2 layer were generated in the catalytic process enhancing the catalytic performance by improving light absorption and conversion efficiency, reducing electron-hole recombination, producing surface oxygen vacancies, and improving the hydrophily of nanowires [108].

The studies about photocatalystic degradation of pollutants in early years were conducted under the UV irradiation. What is more important in recent years is that the researchers have been able to adjust the photocatalytic activity of SiC nanostructures using the visible light via constructing composite and surface modification [327–329]. However, to the best of our knowledge, studies to shed light on the utilization of SiC 1D nanostructures for degradation of pollutants under visible light are still scarce [108]. In the future, one should construct novel structures or other complex SiC nanowires which tailored the bandgap that could absorb visible light to enhance the electron transfer and reduce electron-hole recombination; thus, the improved sensitivity and degradation rate can be expected.

8.3.3.2 Photocatalytic Hydrogen Production

Photocatalytic hydrogen production from water splitting with photocatalysts using solar energy has attracted worldwide attention in recent years, since it could potentially provide a clean and renewable resource for the production of hydrogen fuel [330, 331]. The band structure of SiC can well meet the requirements for water splitting. The conduction band edge of SiC is located above the energy corresponding to the H_2O/H_2 redox couple, and its valence band edge is below the redox energy of the O_2/H_2O couple [332].

Actually, the investigation about photocatalytic hydrogen production of SiC nanowires has already been in progress in recent years [204, 322, 323, 333, 334]. Liu and co-worker carbonized Si nanowires arrays with graphite powder under 1250 °C to obtain well-aligned β-SiC nanowire that was utilized as photocatalyst for water splitting under UV irradiation [204]. The SiC nanowires are highly porous, which endows them with large surface areas and greatly enhanced their photocatalytic activities. The photocurrent of SiC nanowires is about 1000 times higher than the dark current, and no decay was observed within 120 min, revealing their high efficiency and good stability to split water under the UV light. In the following research, aiming to utilizing visible light for enhancing the photocatalytic hydrogen production activity, several strategies have been developed, such as ion doping [34], surface modification [33], heterostructure constructuring [334], and noble metal loading [333].

Hao and co-workers synthesized the modified β-SiC nanowires through a combined route of carbothermal reduction and surface acid oxidation treatment [33]. Compared with unmodified SiC, the average H_2 production rate of SiC

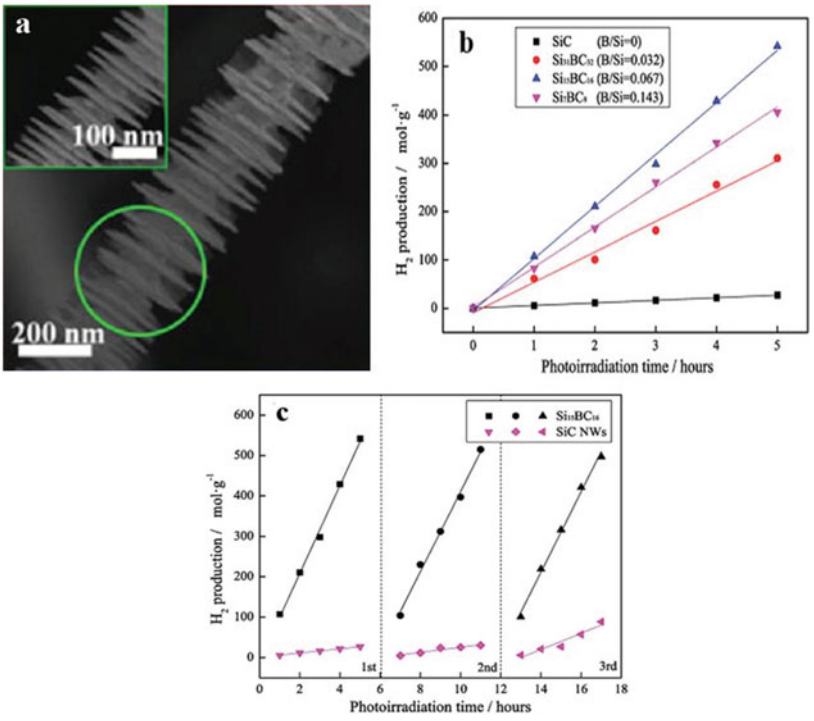

Fig. 8.40 (**a**) Typical SEM image of the as-prepared B-doped 3*C*-SiC. (**b**) Photocatalytic hydrogen evolution performance over B_xSiC. (**c**) Hydrogen production rates of the as-prepared 3*C*-SiC nanowires and B-doped 3*C*-SiC nanowires. (Reproduced from Ref. [34] by permission of the Royal Society of Chemistry)

nanowires could be further enhanced over 76.1% higher by surface modification under visible light, and no noticeable degradation is observed in the repeated runs for 30 h. In addition to the small bandgap and large surface area, the higher H_2 production rate of modified SiC nanowires can be mainly attributed to the increased surface oxygen-contained groups, which can accept more photo-generated holes and reduce electron-hole recombination as well as strengthen the integration between water molecules and the SiC surface [33]. A latter study revealed that Pt nanoparticles-decorated SiC nanowires shows an enhanced photocatalytic activity for water splitting under simulated sunlight irradiation, and its average H_2 evolution rate has been up to 4572 μL/g·h, which is 88% higher than that of bare SiC nanowires [333]. The authors demonstrated that the photo-generated electrons are transferred from SiC to Pt active sites quickly and efficiently to avoid recombination with holes, leading to an enhanced photocatalytic activity.

Furthermore, the B-doped single-crystalline 3*C*-SiC nanowires were synthesized via a carbothermal reduction, and their photocatalytic activities for water splitting under visible light irradiation were also investigated by Yang et al. [34]. As Fig. 8.40a shows, the nanowires possessed novel finned microstructures with fins

about 100–200 nm in diameter and 10–20 nm in thickness. The diameter of inner core stem is about 80 nm on average. After B-doping, the 3*C*-SiC changes into a direct semiconductor, and the bandgap decreases from 2.341 eV to 1.935 eV along with the B/Si molar ratio and increases from 0 to 0.143 [34]. Figure 8.40b depicts the photocatalytic activities of B-doped SiC with different B/Si ratios, which revealed that the B-doping significantly affects the photocatalytic activity. Additionally, the $Si_{15}BC_{16}$ shows an outstanding activity as high as 108.4 μmol/h for H_2 production, which is about 20 times higher than that of 3*C*-SiC nanowires and 2.6 times higher than the highest value purported in the literature for SiC materials. Furthermore, no decrease in catalytic activity was observed in the recycling reactions, as shown in Fig. 8.40c. A combined effect of factors, such as (i) the single-crystalline nature, (ii) small bandgap and easily electron transfer induced by B-doping, and (iii) multiple light reflections and large aqueous suspension contact area due to the finned-like morphology, is attributed to the enhanced photocatalytic hydrogen production [34].

8.3.3.3 Photocatalytic CO_2 Conversion

The continuous rises in the atmospheric CO_2 level and the ever-increasing demand of energy have raised serious concerns about the ensuing effects on the global climate change and future energy supply. Any process that converts the surplus of CO_2 into some high-value compounds fuel will be the most ideal proposition not only to minimize the CO_2 release into atmosphere but also to convert it into a useful product. The photocatalytic conversion of CO_2 into useful fuel, such as CH_4 and CH_3OH, is believed to be one of the best methods to overcome both the environmental problems and energy crisis [335]. SiC also satisfies thermodynamic requirements for CO_2 conversion to hydrocarbon compound in photocatalytic process [336, 337]. For instance, Gondal et al. have reported that CO_2 could be converted into methanol using granular 6*H*-SiC as a photo-reduction catalyst [337].

Unfortunately, there are still no works concerning this state-of-the-art process based on SiC nanowires. Up to now, as discussed in Sect. 8.2, many different SiC nanowires with controlled morphologies, doping, and surface functionalizing treatment have been extensively studied. It is believed that the achieved progress could indeed push forward the photocatalytic conversion of CO_2 application of SiC nanowires.

8.3.4 Field-Effect Transistors

Though field-effect transistors (FETs) based on the thin films are well known for decades, lower sensitivity has limited their widespread applications. Due to the ultrahigh surface-to-volume ratio, nanowires are ideal choices for sensors. Coupling nano-FETs properties and SiC properties, SiC nanowire FETs could be potentially

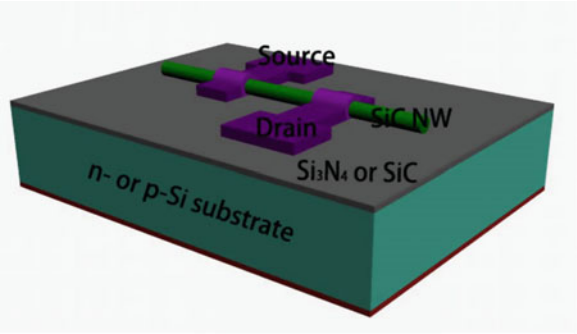

Fig. 8.41 Schematic view of SiC nanowire FET

an excellent candidate for power nanoelectronics and sensors working in harsh or biological environments.

Figure 8.41 shows the typical schematic of the FET configuration based on a single SiC nanowire. For electrical transport measurements of the SiC FET, SiC nanowire was usually prepared on a *n*- or *p*-type Si wafer, pre-patterned by a photolithography process with a Si_3N_4 or SiO_2 layer. The Si wafer served as a back-gate electrode in three-probe structures, and the Si_3N_4 or SiO_2 layer is the gate dielectric layer. In a typical construction process of SiC nanowire-based FETs device, SiC in the solvent is dispersed onto the Si_3N_4 or SiO_2 layer, and then two metal contacts, which refer to the source and drain electrodes, were defined on the ends of the nanowire by either photolithography or electron beam lithography. Based on the measured *I*-*V* characteristic, the contact types could be the ohmic contact and Schottky contact.

8.3.4.1 Electrical Properties of SiC Nanowire-Based FETs

The electrical transport characteristics of various SiC nanowires (such as the 3*C*- and 4*H*-SiC nanowires and Si-SiC-core-shell nanowires) have been studied by several groups through the synthesis and assembly of single nanostructure, field-effect transistor [32, 187, 338–341]. All the results presented similar device performance in terms of transconductance and carrier mobility [342].

Zhou and co-workers obtained the high-quality β-SiC nanowires on carbon fabric by thermal evaporation process under 1450 °C, and FETs were fabricated to investigate the nanowires electrical behavior exhibiting *n*-type conducting behavior [338, 343]. The SiC nanowires presented a diameter of ~6 nm with a length of up to tens of microns. The carrier mobilities of the *n*-type SiC FETs were 6.4 and 15.9 cm^2 /V·s when gate voltage (V_{ds}) is 0.01 and 0.05 V at room temperature, respectively [338, 343]. The author found out that the drain current increased by one order of magnitude under high temperature (80 and 150 °C) than it did at room temperature, revealing that the SiC FET can serve as excellent candidate in fabricating the high-temperature gas sensors proving the possibility of environmental monitoring in the hot and harsh environments [338].

Rogdakis and co-workers investigated the electrical characteristics of the 3*C*-SiC nanowires-based FETs systematically by both the theoretical and experiment routes [340, 342, 344, 345]. Theoretical studies on the FETs operation in ballistic and diffusive regimes by using non-equilibrium Green function formalism and drift-diffusion schemes, respectively, have shown the SiC nanowire FETs have similar performance to the Si-based ones in both transport regimes. Thus, the use of SiC as channel material in nanowire-based FETs will not degrade the electrical characteristics, while it will offer all advantages from the SiC physical properties [340, 344, 345]. The metal contacts of contrasted FETs were also experimentally analyzed [340, 342]. Due to the high carrier concentration along the nanowire, transistors with ohmic-like contacts present a very weak gating effect and could not be switched off even for a very high negative gate voltage (−40 V). In contrast, the Schottky contact acted beneficially for the device performance by suppressing the off current and leading to I_{on}/I_{off} ratio equal to ~10^3 [342]. Therefore, in the case of heavily doped SiC nanowires, the Schottky contact was preferable. On the other hand, if the ohmic contact is used in an FET device, its performance can be improved by reducing doping concentration, which can be realized by modulating the dopant implantation or growth technique.

Beside the most reported SiC nanowire FETs that related to the pure or intrinsically *n*-type unintentionally doped SiC [338, 343], the electrical behaviors of *p*-type SiC nanowire FETs for advanced semiconductor electronic device applications have also been investigated [32, 96]. Chen and co-workers for the first time constructed *p*-type SiC nanowires FETs using an individual Al-doped single-crystalline 3*C*-SiC nanowire [32]. The SiC nanowires have a mean lateral size of 200 nm and a length of up to tens of micrometers, with an aspect ratio of ca. 30, as shown in Fig. 8.42a. Magnified TEM image (Fig. 8.42b) disclosed that the nanowires have an almost uniform diameter throughout their entire length without any tips or any attachments of catalytic droplets. Clear evidence for the incorporation of Al dopants is shown in the EDS spectrum (Fig. 8.42c). Figure 8.42d shows the typical electrical drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) measurements at various gate voltages V_g. The linear and symmetric I_{ds}-V_{ds} curves over the entire V_{ds} range indicated good ohmic contacts of metal stacks to the nanowire. The effective I_{ds} decreases as the V_g increases from −10 to 10 V (the upper inset in Fig. 8.42d) which revealed the majority of carriers in the nanowire are *p*-type. The incorporation of intentional Al dopants can induce additional shallower acceptor states in the SiC band structure while compensating for the native donor states, which was responsible for the transformation of nanowires from intrinsic *n*-type to *p*-type structure [32].

8.3.4.2 Improvement of Source/Drain Ohmic Contact by Ni-Based Contacts

As devices size is scaled down into nanoscale region, the channel resistance of nanowire becomes sufficiently small [346]. Therefore, the source/drain (S/D) contact properties become an important issue and determine the device performance. Many

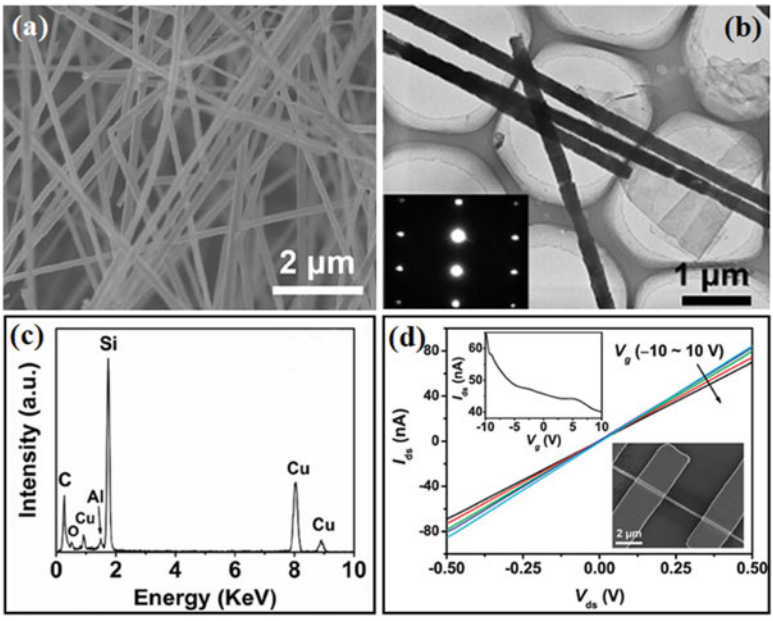

Fig. 8.42 (**a**) Typical SEM image of the obtained SiC nanowires under low magnification. (**b**) Typical TEM images of the SiC nanowires. The inset is the corresponding SAED pattern. (**c**) A representative EDS spectrum of the SiC nanowires. (**d**) I_{ds}-V_{ds} characteristic curves as a function of V_g (−10, −5, 0, 5, and 10 V) for the Al-doped SiC nanowires FET. Upper inset: the I_{ds}-V_g curve of the same device at $V_{ds} = 0.5$ V. Lower inset: a typical FET SEM image of the device. (Reproduced from Ref. [32] by permission of the Royal Society of Chemistry)

efforts have been devoted to tailor the interface between the metal and nanowires for minimizing S/D contact resistance, such as changing the metal species and optimizing the annealing conditions [347, 348].

Studies reported that Ni is the best material for good ohmic contacts to *n*-type SiC substrate because it forms silicide with SiC at elevated temperatures [349]. Jang and co-workers investigated the electrical characterization of two ohmic contacts, which refer to Ni/Au and Ti/Au, to unintentionally doped SiC nanowires using modified transmission line model [350]. The authors found out that deposited Ni/Au ohmic contacts on SiC nanowires had ~40 times lower specific contact resistances of $5.9 \times 10^{-6} \pm 8.8 \times 10^{-6}$ Ω/cm^2 compared to the values of Ti/Au ohmic contacts ($2.6 \times 10^{-4} \pm 3.4 \times 10^{-4}$ Ω/cm^2). A comparison study of the electrical characteristics of top-gated SiC nanowire FET with two different ohmic contacts was conducted. Figure 8.43a shows the SEM image of the FET devices with Ni/Au ohmic contacts for the total resistance measurements. As indicated in Fig. 8.43b, the total resistance with Ni/Au ohmic contacts formed on the source/drain electrodes of SiC nanowire FETs was much lower than that for Ti/Au ohmic contacts. Figure 8.43c shows a histogram that summarizes the total resistances measured on the same size and distance SiC nanowires between the source and drain with two

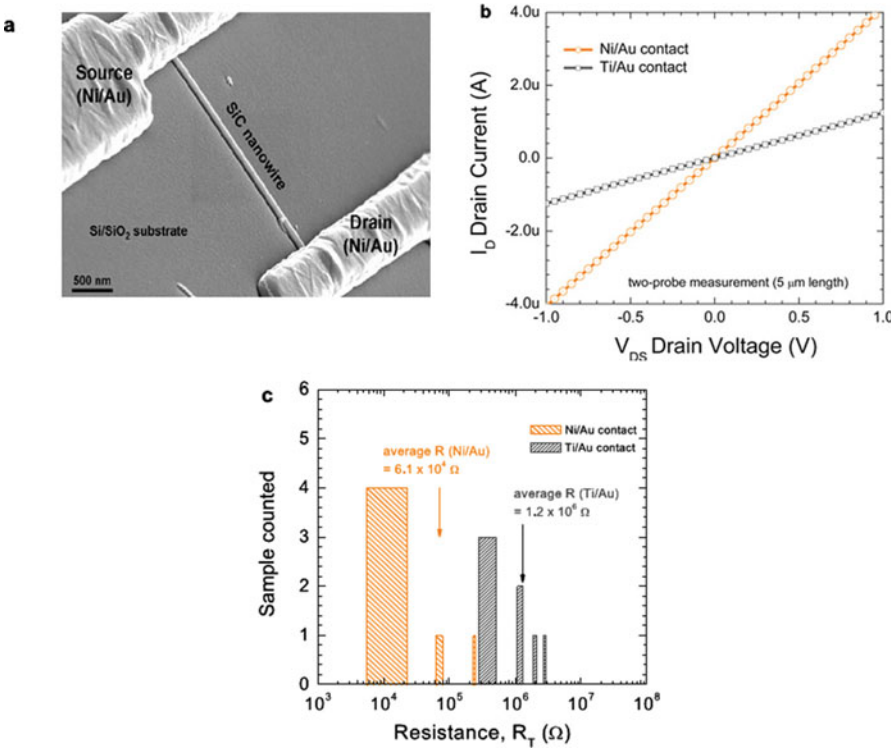

Fig. 8.43 (**a**) The SEM image of a typical SiC nanowire FET. The subsequently evaporated Ni/Au metals were used for the low-resistance source/drain contacts. (**b**) Current-voltage measured between the source and drain contacts with two different ohmic contact metals. (**c**) Histogram of the total resistances measured on the same size and distance SiC nanowires between the source and drain with two different ohmic metals after the annealing process. (Reprinted with permission from Ref. [350]. Copyright 2008 by the Institute of Physics Publishing. All rights reserved)

different ohmic contacts after 700 annealing. These results support the observation that Ni/Au ohmic contacts are clearly better than Ti/Au ohmic contacts on SiC nanowires.

With the similar strategies, Choi and co-workers introduced an annealing optimization study to form the low-contact resistance Ni-silicide phases on the SiC nanowires in the FETs devices [341]. The experimental results show that an annealing temperature of 650 °C leads to the lowest ohmic contact resistance on SiC nanowire FETs. The Ni silicide phase begins to intrude into the SiC nanowire channel after an annealing step at 700 °C for 30 s, and consequently, it forms either a SiC/Ni silicide heterostructure or a fully Ni-silicidized SiC nanowire depending on the channel length. A fully silicidized SiC nanowire exhibits a low channel resistance (740 Ω) and a high current density (1.46 × 107 A/cm^2 at 1.4 V) [341]. The Ni-based silicidation is a key process to guarantee the stability and repeatability of ohmic contact by tailoring the metal-semiconductor interfact [341].

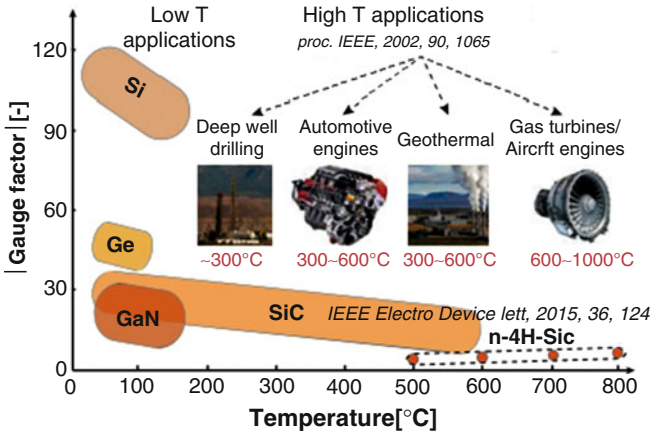

Fig. 8.44 The piezoresistive effect in common semiconductors. © [2015] IEEE. (Reprinted, with permission, from Ref. [362])

8.3.5 Pressure Sensors

The need for smaller, low power consumption and higher performance sensors facilitated various micro-electro-mechanical systems (MEMS) technologies, and piezoresistive sensors have showed great advantage [351, 352]. To date, pressure sensors have been manufactured mainly based on Si crystal, owing to its favorable physical and chemical, worldwide availability, and mature fabrication technologies [353, 354]. With the development of device miniaturization, lightweight, and high performance, it is increasingly important to develop mechanical sensing devices which can withstand hostile conditions such as high temperatures, increased corrosion, high powers, and high frequencies [355, 356]. The energy gap of Si is relatively low (1.12 eV), which limits its piezoresistive applications below 200 °C [357]. Consequently, the piezoresistive effect in materials with a large energy gap (e.g., GaN, SiC) is of interest for mechanical sensors at elevated temperature, as depicted in Fig. 8.44 [358, 359]. Among several large bandgap materials, SiC is recognized as a promising substitute for Si to be serviced under the harsh work conditions. For instance, the SiC pressure sensors were confirmed to be well serviced up to 600 °C [360, 361].

The piezoresistive effect in SiC has been studied for years. However, to the best of our knowledge, there are only a few reports that reviewed the piezoresistive effect of SiC. Barlian et al. [363] reviewed the piezoresistive of semiconductors, in which the piezoresistive effect of 3*C*-SiC was mentioned but not discussed in detail. Werner et al. [358] discussed some preliminary experimental results on the characterization of the piezoresistance in 3*C* and 6*H*-SiC in the 1990s. However, the report on the recent development of SiC piezoresistive sensors, especially the influence of the crystal form, orientation dependence, and doping level, was omitted. Phan et al. [362] reviewed the piezoresistive effect of SiC for MEMS sensors. The review

covers both experimental and theoretical studies and provides important information for MEMS design on the effects of crystal defects, orientation dependence, carrier-concentration dependence, as well as temperature dependence. To date, many efforts have been made in the investigation of the piezoresistive of SiC nanowires since they combine the excellent physical properties and advantages of low-dimension structures [14, 364, 365]. The giant piezoresistance behaviors in Si nanowires, with an exciting gauge factor (GF) of ~5000, exhibit their very promising prospect for the exploration of the novel and efficient pressure sensors [366]. This impressive result raises their hopes, who are researching the piezoresistance effect in SiC nanostructures to obtain a giant piezoresistance behavior for harsh environment applications [367]. But so far, no review has been focused on the piezoresistive effect in SiC nanowires.

Herein we review the research about the piezoresistive effect in SiC nanowires, covering both experimental and theoretical studies. In addition, the current issues and perspectives for further studies and applications of the piezoresistive effect in SiC are also discussed.

8.3.5.1 Piezoresistive Effect in Semiconductors

The piezoresistive effect is defined as the change of electrical resistance under mechanical stress or strain. The electrical resistance (R) of a homogeneous structure is a function of its dimensions and resistivity (ρ):

$$R = \frac{\rho l}{\alpha} \tag{8.12}$$

where l is length and α is the average cross-sectional area. Under the applied strain, the change in resistance is due to both the geometric effect ($1 + 2\upsilon$) and the fractional change in resistivity ($\Delta\rho/\rho$) of the material [368]:

$$\frac{\Delta R}{R} = (1 + 2\upsilon)\varepsilon + \frac{\Delta\rho}{\rho} \tag{8.13}$$

where υ is the Poisson's ratio of the material and ε is the strain in the longitudinal orientation ($\varepsilon = \Delta l/l$).

Gauge factor (GF) is commonly used as the parameter to evaluate and compare the magnitude of the piezoresistive effect in semiconductors:

$$GF = \frac{\Delta R/R}{\varepsilon} = \frac{\Delta\rho/\rho}{\varepsilon} + (1 + 2\upsilon) \tag{8.14}$$

For most metals, the geometric effect is approximately 1.4 to 2.0; the change in resistivity is really small—on the order of 0.3. However, for a semiconductor in certain directions, the applied stress/strain can alter the carrier density and mobility,

which brings about the piezoresistive effect with the change in the resistivity and/or conductivity [363]. $\Delta\rho/\rho$ is 50–100 times larger than the geometric term; thus, the geometric effect $1 + 2\upsilon$ can be ignored. The GF of a strain gauge can be simplified as below:

$$GF = \frac{\Delta R/R}{\varepsilon} = \frac{\Delta\rho/\rho}{\varepsilon} \tag{8.15}$$

The relative change of resistivity can also be presented as a function of the applied stress (σ): $\Delta\rho/\rho = \pi\sigma$ (π is the piezoresistive coefficient of semiconductor). When a uniaxial stress is applied, the stress is connected to the strain via Hooke's law, $\sigma = Y\varepsilon$, where Y is the Young's modulus of semiconductor. Thus, the relationship between the gauge factor and the piezoresistive coefficient is $GF{=}Y\pi$ [363].

Experimental and theoretical studies about the piezoresistive effect in semiconductors could be traced back to 1954, by Smith, who reported the first measurements of the exceptionally large piezoresistive shear coefficient in silicon and germanium [369]. At that time, the existed theories were based on shifts in bandgap energies. For later analyses, include the works of Herring [370], Herring and Vogt [371], and Long [372], taking the model for mobility changes [373] in semiconductors as the basis. Now, the general idea is that the energy band structure of the semiconductors is modified under strain, leading to the mobility and effective mass of the carriers changed, which brings about the piezoresistive effect.

8.3.5.2 The Piezoresistive Effect in SiC Nanowires

1. The Piezoresistive Effect in SiC Nanowires Without Dopants

As shown in Fig. 8.45, a high-quality SiC nanowire with a [111] direction was used to carry out the tensile process and measure the electrical properties by Shao and co-workers [374]. The experiments were performed using a scanning tunneling microscope-transmission electron microscope (STM-TEM) joint instrument. The individual SiC nanowire with a diameter of 150 nm is fixed between an Ag electrode and W tip. Figure 8.45a–h shows a typical tensile process, by controlling the W tip to be far away from the Ag electrode; an uniaxial tension test was performed on the SiC nanowire. The length of the nanowire lengthened from 2600 to 2843 nm, and the corresponding calculated strains are 1.15% to 9.35%, respectively. The nanowire broke at the junction between the wire and Ag electrode followed continuing with the pull, (Fig. 8.45g and h). The authors attributed this to the torsional force. Corresponding to all the *I-V* curves in Fig. 8.45i, the calculated GF of this wire is −6.9, and the piezoresistance coefficient is -1.15×10^{-11} Pa^{-1}. Although this is not an exciting consequence compared with the bulk material [360], the applied strain is really small, and the change of the conductance is large. Shao et al. suggested that the underlying mechanism for the change of conductance was attributed to the strain-induced band structure change. Zeng et al. [375] used a different

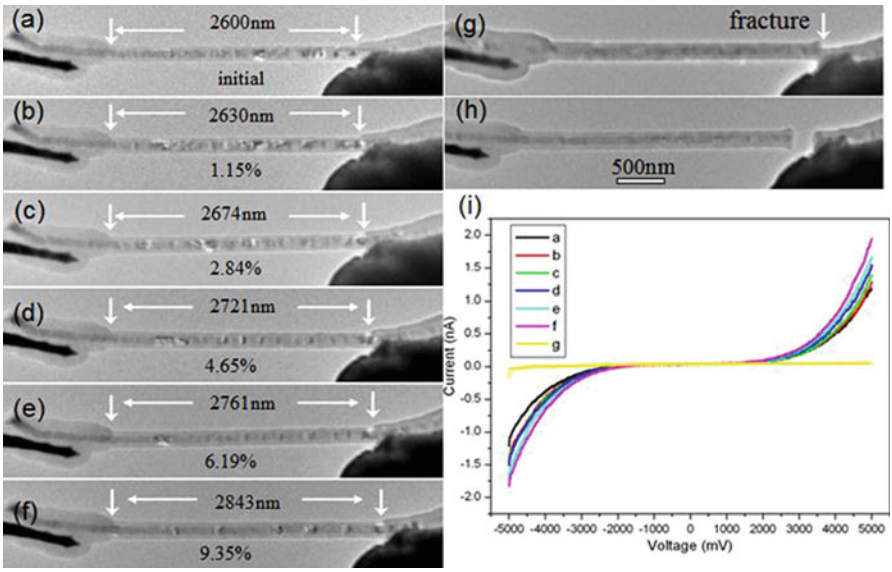

Fig. 8.45 Images of the tensile SiC NWs and the corresponding I-V curves. (**a**)–(**f**) Images of the tensile SiC nanowire, (**g**)–(**h**) images of the fractured nanowire. (**i**) The corresponding *I-V* curves. (Reprinted with permission from Ref. [374]. Copyright 2012, American Institute of Physics)

approach to investigate the piezoresistance effect of 3*C*-SiC nanowires by SEM. The diameter of the wire is about 320 nm. The GF of the wire was determined to be 14.1.

2. The Piezoresistive Effect in Doped SiC Nanowires

Although some researchers have showed a keen interest on the piezoresistance effect in SiC nanowires, unfortunately, the giant piezoresistance effect like Si nanowires was rarely achieved. So far, doping was proved to be an effective strategy for enhancing the piezoresistance effect of SiC [94, 376, 377]. In our group, we simulated the piezoresistance effect in *p*-type 6*H*-SiC nanowires, in which an AFM tip was pressed against a 6*H*-SiC nanowire [376]. The diameters of the wire is 150 nm with 1.05 at% Al dopants. The transverse piezoresistive coefficient $\pi_{[010]}$ of this wire is calculated to be in the range of 51.2 to 159.5 $\times$ 10^{-11} Pa^{-1} under the *F* from 43.8 to 140.2 nN. This is perhaps the largest piezoresistive coefficient reported in SiC material with so small loading forces. However, Young's modulus of 6*H*-SiC nanowires is only ~50 GPa [376]; the corresponding GF can be achieved in range of 25.6 to 79, which cannot be considered as a giant piezoresistive effect. In addition, the strain-induced changes in surface states are the key contributor to the piezoresistive behaviors of present *p*-type 6*H*-SiC nanowires [376].

In the following reports, we investigated the piezoresistive effect of *n*-type 3*C*-SiC nanowires with a similar approach [377]. The nanowires presented a diameter of 230 nm and N-doping level of 8.28 at%. The transverse piezoresistive coefficient $\pi_{[110]}$ is calculated to be in the range of 51.2 to 159.5 $\times$ 10^{-11} Pa^{-1} under the *F* from

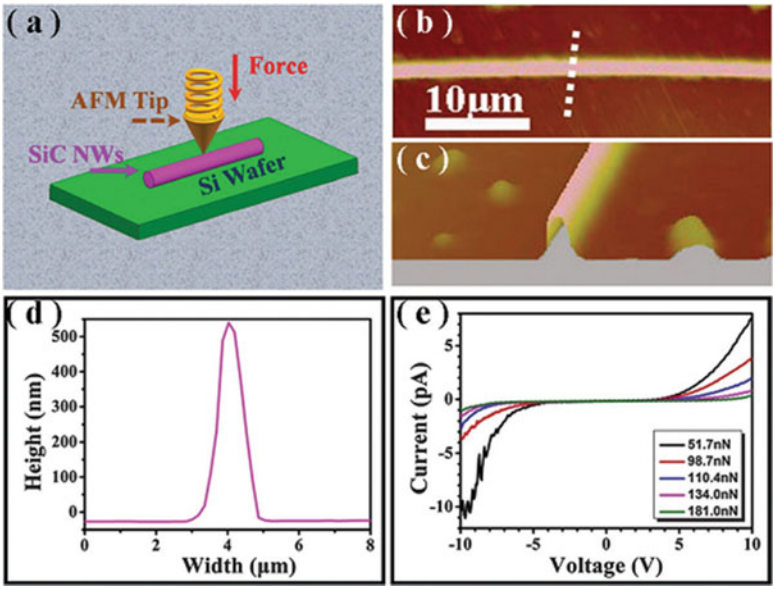

Fig. 8.46 (**a**) Schematic diagram for the measurement of the piezoresistance in SiC nanowire. (**b**–**c**) AFM and topography images of a single nanowire lying on the Si substrate. (**d**) Corresponding height data recorded along the dashed white line marked in (**b**). (**e**) *I-V* curves recorded at different applied compressive forces across the nanowire. (Reproduced from Ref. [94] by permission of the Royal Society of Chemistry)

43.8 to 140.2 nN. The corresponding GF was found to be 4.5 to 46.2. We speculated that the piezoresistance behaviors should be ascribed to the strain-induced change in the surface state and band structure [377]. Once the strain is fixed onto the surface of the wire, the energy surface can be significantly deformed, leading to the change in carrier concentrations and mobility [94, 378–380].

The updated research about the piezoresistance effect in *p*-type 3*C*-SiC nanowires (with B-doping level of 7.18 *at%*) was also conducted in our group [94]. As schematically illustrated in Fig. 8.46a, the transverse piezoresistance characterization of single 3*C*-SiC nanowire was conducted by C-AFM at RT. Figure 8.46b–d suggested the diameter of the wire is ~540 nm. The corresponding measured *I-V* curves with the increase of loading forces ranged from 51.7 to 181.0 nN, as shown in Fig. 8.46e. Different form the previously reported works, the currents of B-doped nanowire exhibit a negative piezoresistance effect. The piezoresistance coefficient $\pi_{[110]}$ of the wire falls in the range of -8.83 to -103.42×10^{-11} Pa^{-1} as the F ranging from 51.7 to 181.0 nN. The calculated GF is as high as -620.5, which is enhanced by more than 10 times compared to the highest ever reported for SiC nanostructures. Besides the strain-induced change in the surface state and the band

structure in SiC nanowire, we suggested the giant negative piezoresistance effect with high GF could be attributed to following two points:

(i) The incorporated B dopants. As compared to our previous work (i.e., 3*C*-SiC nanowires with N dopants [377]), the significant difference is the incorporated B dopants.
(ii) The crystallography of SiC nanowire with a top surface of (110). As compared to other typical crystal orientations (e.g., along the [100] direction, the band warping is negligible), the energy surface in [110] orientation can be significantly warped. This could lead to the profound change of the effective mass and hole occupation in the heavy hole and light hole bands [362, 381].

To date, for full understanding of the piezoresistive effect in SiC nanowires and their applications, various questions still need to be addressed. (i) For single-crystalline 3*C*-SiC nanowires, it is generally considered that the electron transfer and electron shift mechanisms are valid for the estimation/explanation of the piezoresistance in *n*-type 3*C*-SiC nanowires. However, for *p*-type 3*C*-SiC nanowires, due to the complexity of the valance band structure, there are still no reliable reports on theoretical calculations. (ii) Majority reports were focused on the piezoresistance effect of 3*C*-SiC nanowires due to their more attractive MEMS devices. Other typical crystal forms, such as the 6*H*- or 4*H*-SiC nanowires, are scarcely reported. (iii) SiC is an important high-temperature semiconductor, and, for instance, the SiC pressure sensors were confirmed to perform well up to 600 °C [360, 361]. However, the temperature-dependent piezoresistive behaviors of SiC nanowires have not been mentioned. (iv) The orientation plays a crucial role in designing MEMS sensors. For instance, when designing *p*-type single-crystalline 3*C*-SiC film-based mechanical sensors in the (100) plane, the [110] orientation should be selected to achieve maximum sensitivity [380]. However, the experimental results and theoretical studies about orientation-dependent piezoresistive effect of SiC nanowires have not been reported. (v) The influence of defect density and doping concentrations on the piezoresistive effect is still indistinct. (vi) It is well known that the morphology and size of semiconductor have important effects on their physical properties [382]. However, previous works all focused on the SiC nanowires, and other conventional 1D nanostructures, such as nanotubes and nanobelts, have not been involved.

Research on nanowire-based mechanical stimulation into electrical signals has drawn great attention recently [362, 383]. Unfortunately, the piezoresistive properties of SiC nanowires have not yet been fully characterized, whether experimental results or theoretical studies. It should be noted that previous studies all ignore the contribution from the quantum confinement since the diameter of the synthesized nanowires is relatively large (often above 150 nm). Meanwhile, as for competitive advantage in the devices fabrication and performance [76, 384], future research directions may pay more attention to the nanobelts with smaller thickness.

8.4 Conclusions and Outlooks

This chapter has comprehensively reviewed the growth of SiC nanowires with different morphologies and doping levels, associated with their typical electronic applications. To date, the controlled growth of SiC nanowires in morphologies and doping levels has been progressed. Nevertheless, these studies in this field are unsystematic currently. There is a still a grand challenge to realize the generation of SiC nanowires with high quality and quantity through more controllable, predictable, and facile processing. For example, most of the reported works concerning the growth of the SiC nanowires via the vapor route were performed under the temperatures higher than 1000 °C, which are considered as the big obstacle to limit their growth in a controlled manner. The low-temperature solvothermal process exhibits remarkable advantages for the growth of SiC nanowires. However, the high pressures are often required. The electrochemical anodic oxidation, which could execute under RT and atmospheric pressure, may be helpful for the fabrication of SiC nanowires not only in mass production but also in orient growth direction. Furthermore, it is still interesting to make the SiC be precisely doped in concentrations with expected spatial distribution.

Owning to the advantages of the unique geometric configuration and superior physical/chemical properties of the SiC nanowires, a series exciting electronic application have been developed. Examples may include the field emission cathode, supercapacitors, photocatalysts, field-effect transistors, and pressure sensors, suggesting their bright and wide commercial application prospect. These applications, along with the fundamental interest in nanoscience and nanotechnology, will continuously provide compelling motivation for research into techniques for synthesizing nanowires with better controlled configurations and properties.

Regardless of the fact that numerous researches have witnessed the rapid development and substantial achievements in the SiC nanowires and electronics, the following issues are still worth persisting with:

(i) The optimization of the nanodevice performances is the key and ultimate goal to push forward their practical applications. For example, functionalizing the surface of SiC nanowires with oxides or nitride layer is proved to be highly useful for the exploration of the devices. The modified SiC surface by oxidation treatment could establish improved optoelectronic behaviors due to the increased surface oxygen-contained groups. The doping and nanoparticles-decorated SiC surface with proper density would remarkably facilitate the field electron emission. Although some works have shed light on this topic, more and deep research targeting on tuning their conductivities, bandgaps, surface states, and so forth through fully controllable strategies are still highly desired.

(ii) Surprisingly, there is little effort made in SiC nanowires for the exploration of photodetector and photocatalytic CO_2 conversion, despite the interesting physical properties of SiC. The study of photodetector is a field full of opportunities for practical applications, while the photocatalytic conversion of CO_2 is

expected to be a dominant area. Furthermore, in regard to the currently emerging and exciting theme of renewable energy technologies, the investigations on the SiC-nanowire-based energy materials (e.g., the supercapacitors and photocatalyts) are significantly insufficient.

(iii) Another interesting topic in SiC nanowires is the flexible electronic devices. Limited by the growth of SiC nanowires are often performed under high temperatures, the exploration of SiC-nanowire-based flexible units is still a grand challenge. To date, mainly two technologies are worth noting. The first is to make the SiC nanowires grow directly on the flexible carbon fabric substrate, which were recently applied in constructing the flexible field emitters and flexible supercapacitors. The second is described as a two-step process. The SiC nanowires are exfoliated or etched away from the initial substrate and then transferred onto other flexible substrates, which presents some advantage for fabrication of flexible and transparent units, since it can overcome the hindrance for limited selection of flexible substrates.

(iv) Importantly, the performance of the SiC-nanowire-based electronic devices under the harsh work conditions. To date, even much progress has been made on the exploration of SiC-nanowire-based device applications with high performances, scarce reports have shed light on their work ability to be serviced under harsh environments once they fall into micro-/nanoscale dimensions. This is a very important issue waiting to be investigated, which could show the difference and significance of the SiC nanowires with their unique applications capable to be serviced under high-temperature/high-voltage/high-power harsh environments, as compared to the other semiconductors.

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Chapter 9
Nanowire Bioelectronics

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A bioelectronic device transduces a biological signal to or from an electrical signal at the bioelectronic interface. For example, an affinity biosensor employs a surface-immobilized recognition probe such as enzyme, antibody, or single-stranded nucleic acid to selectively capture a target analyte from solution [1, 2]. This biological recognition process is then converted into a measurable electrical signal in the biosensor, which allows for quantitative analysis of the target. Another example of bioelectronics is to record or stimulate bioelectrical activity from an electrogenic cell, such as neuron or cardiomyocyte [3–5]. The translation between the ionic and electronic signals is enabled through either electrochemical reactions at the surface of a metal electrode or capacitive coupling at the interface between a transistor and a cell. Advanced electrophysiological tools are being developed to reveal the functional properties of neurons [6], the processing mechanisms within the central nervous system [7], and the clinical treatment of brain diseases [8, 9].

Over the past decades, bioelectronics has been incorporated into numerous diagnostic and implantable biomedical devices, including point-of-care sensors, cardiac defibrillators, and deep brain stimulators. Recently, whole-genome sequencing has been demonstrated by an integrated complementary metal-oxide-semiconductor (CMOS) microdevice, which opens up new opportunities for personalized genomics owing to the low cost and scalability of modern CMOS technology [10]. Nevertheless, next-generation bioelectronics will need significant

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improvements in sensitivity and miniaturization to meet the requirements in areas such as single-cell analysis and early cancer diagnosis. In addition, implantable devices should be minimally invasive and mechanically compliant with biological tissues for long-term efficacy and biocompatibility. There has been a growing effort to develop flexible bioelectronics to meet the requirements for implant applications. Most current fabrication techniques for bioelectronics, however, do not use materials with optimized sensitivity and biocompatibility.

Advances in nanomaterials offer important opportunities to overcome existing challenges in bioelectronics. In particular, one-dimensional semiconductor nanowires have been broadly explored as building blocks in bioelectronic devices due to their small size, large surface area, and intrinsic readout signals. Controlled synthesis of high-quality semiconductor nanowires has been established through catalytic chemical vapor deposition (CVD). The large surface-to-volume ratio of semiconductor nanowires is beneficial to achieve high sensitivity in the detection of surface processes. A large proportion of the constituent atoms in the nanowires are located at or close to their surface. This characteristic makes the surface atoms play an important role in determining the electronic properties of the nanowires. Moreover, only a small number of analyte molecules, or even a single molecule, are needed to equilibrate the binding sites on the nanowire surface, which allows a significant reduction of the sample volume. In addition, nanowires can interact with cells at a length scale comparable to biological building blocks, such as proteins and nucleic acids. Accordingly, spontaneous internalization of surface-modified nanowires into neurons and cardiomyocytes has been experimentally observed. The cellular penetration of nanowires has been utilized in both nanowire-assisted gene delivery and minimally invasive intracellular recording. Moreover, the use of nanowires and their integration with a polymer substrate lead to greatly enhanced bending flexibility of the bioelectronics, which has allowed their three-dimensional (3D), seamless integration with tissues.

In this book chapter, we will present an overview of recent advances in nanowire bioelectronics. Silicon nanowires (SiNWs) are chosen as representative building blocks in bioelectronics due to their well-established synthesis and surface modification schemes as well as their excellent and tunable electrical properties. These studies were broken down into four groups. Section 9.1 discusses affinity biosensors based on nanowire field-effect transistors (FETs). Section 9.2 describes the transduction of ionic and electric signals at the nanowire and cell interfaces for extracellular electrophysiological recording. Section 9.3 discusses intracellular electrophysiological recording with nanowire transistors through the internalization of nanowires/nanotubes by cells. Section 9.4 will discuss the development of macroporous, flexible nanowire bioelectronics to enable 3D integration with biological systems. We will conclude with future challenges and prospects of nanowire bioelectronics.

9.1 Nanowire Bioelectronics for the Detection of Biological Molecules

Sensitive, selective, and cost-effective detection of biomolecules has been of significant interest in areas such as clinical diagnosis, drug discovery, and environmental testing. An affinity biosensor provides an attractive platform for the rapid, real-time detection of biological molecules due to the direct conversion of biological signals to electric signals. Silicon nanowire field-effect transistors (SiNW FETs) have been widely studied as affinity biosensors for highly sensitive and label-free detection of biomolecules. The surface of the silicon nanowires can be feasibly functionalized with recognition probe molecules, including antibodies and single-stranded nucleic acids. The target antigens or single-stranded nucleic acids are then captured onto the nanowire surface through specific interaction with the recognition probe molecules. The carrier density in the silicon nanowire is changed by the charges or dipoles of the target molecules due to the field effect, which further leads to a quantifiable electrical signal in the nanowire transistor. Affinity biosensors based on SiNW FETs offer the advantages of real-time recognition, simple fabrication and operation, and small sample volume. In addition, silicon nanowires can be well-aligned into highly ordered biosensor arrays, which further enables simultaneous detection of multiple biological targets.

The surface of the silicon nanowires is intrinsically covered with a thin layer of silicon dioxide of a few nanometers. Through the well-known silane chemistry, silicon nanowires can be covalently linked with a variety of functional groups, including carboxylate, amine, and aldehyde groups. For example, Cui et al. modified p-type SiNW FETs with (3-aminopropyl)triethoxysilane to achieve amino-functionalized surface [11]. As the pH of the solution was increased, the surface amino groups underwent deprotonation, which increased the carrier density in the p-type SiNWs. As a result, amino-functionalized SiNWs exhibited pH-dependent conductance that was linear over a large dynamic range.

The functional groups on the silicon nanowires can be further conjugated with a variety of biomolecules. For example, SiNWs were covalently linked with biotin receptors to selectively detect streptavidin molecules down to a concentration of 10 pM [11]. The high sensitivity of the SiNW FETs was attributed to both the large surface-to-volume ratio of the nanowires and the extremely high-affinity/irreversible binding between biotin and streptavidin.

Affinity biosensors based on nanowire transistors can be applied for real-time kinetic analysis of antibody-antigen interactions. For example, Cui et al. monitored the reversible binding between monoclonal antibiotin (m-antibiotin) and biotin receptor on the silicon nanowire surface, which was then used to determine the kinetic characteristics between m-antibiotin and biotin [11]. Duan et al. determined the association and dissociation rate constant of the high mobility group box 1 (HMGB1) protein and DNA pair by using SiNW FETs as affinity biosensors [12].

Controlled assembly of nanowires into high-density transistor arrays has been realized with a variety of approaches, including the Langmuir-Blodgett technique

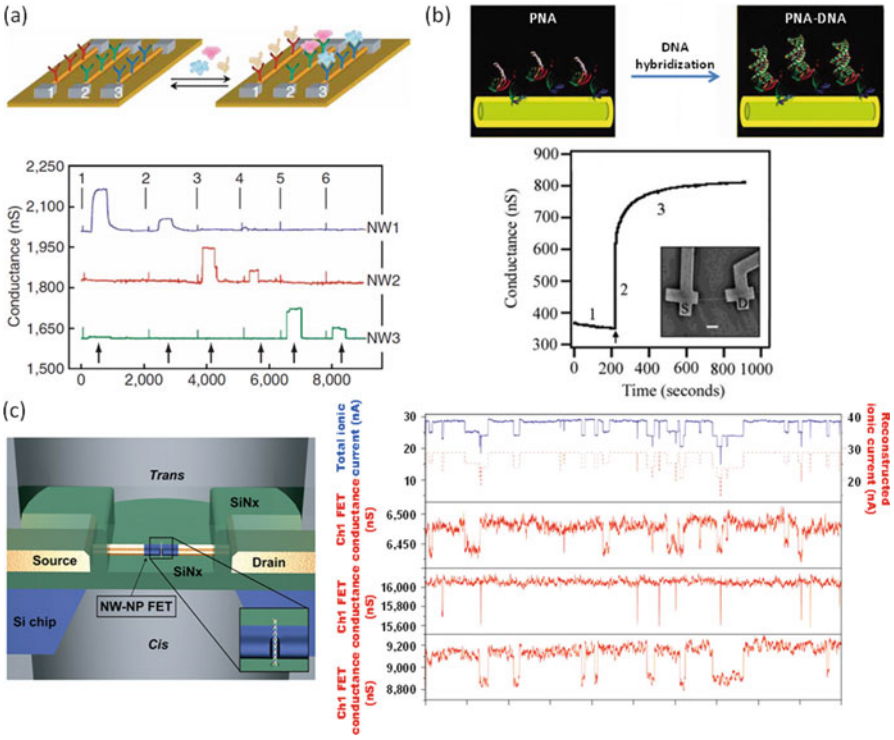

Fig. 9.1 Nanowire bioelectronics for the sensing of biomolecules. (**a**) Schematic (top) and measurement data (bottom) of antibody-modified SiNW FETs for the detection of multiple cancer markers. (Reprinted with permission from Ref. [16]. Copyright 2005, Nature Publishing Group). (**b**) Schematic (top) and measurement data (bottom) of PNA-modified SiNW FETs for the detection of DNA molecules. (Reprinted with permission from Ref. [19]. Copyright 2004, American Chemical Society). (**c**) Schematic of nanowire-nanopore-based DNA analysis platform (top) and the simultaneously recording of ionic current and drain current during the translocation of single DNA molecules. (Reprinted with permission from Ref. [20]. Copyright 2012, Nature Publishing Group)

[13], the blown bubble technique [14], and the nanocombing technique [15]. Zheng et al. applied SiNW transistor arrays for the parallel detection of multiple biomolecules [16]. Distinct nanowires in the array were functionalized with different surface receptors. The SiNW biosensor arrays allowed simultaneous and highly selective and sensitive detection of prostate-specific antigen (PSA), PSA-α1-antichymotrypsin, carcinoembryonic antigen, and mucin-1 (Fig. 9.1a). In addition, the cancer markers were routinely detected at femtomolar concentrations, which was several orders of magnitude better than with that obtained standard enzyme-linked immunosorbent assay (ELISA) technique [17].

SiNW FETs have also been applied for sequence-specific, label-free detection of single-stranded nucleic acids. The surface of the nanowires was immobilized with

single-stranded DNA (ssDNA) or peptide nucleic acid (PNA) receptors [18]. In particular, SiNW biosensors exhibited time-dependent conductance signals upon the hybridization of the complementary ssDNA with the PNA receptor on the nanowire surface (Fig. 9.1b) [19]. Concentration-dependent measurements showed that detection of the ssDNA can be carried out at tens of femtomolar concentrations. In addition, the identification of fully complementary versus mismatched ssDNA has been achieved.

Xie et al. fabricated a nanowire-nanopore FET on a thin SiN_x membrane, which has been applied for the analysis of ssDNA molecules at single-molecular level [20]. A nanometer-sized pore was perforated through the SiNW, and both ends of the nanopore were linked with a chamber filled with saline solution. When a voltage was applied between the chambers, ions passed through the nanopore, which generated a stable open-pore current. When DNA strands were added into the cathode linked chamber, they were driven through the nanopore due to the electrophoresis, which resulted in an ionic current blockage. At the same time, the drain current of the nanowire was changed by the translocating DNA. The ionic current and the transverse drain current of the nanowire were recorded simultaneously [20]. The spikes of the two recorded currents exhibited strong temporal correlation. A key advantage of the nanowire-nanopore DNA analysis is that multiple nanowire-nanopore FET biosensors can be integrated within a single analysis chamber and individually addressed. As shown in Fig. 9.1c, simultaneous recording from three nanowire-nanopore devices has been successfully demonstrated with each FET operating independently.

The rapid and early detection of viruses is essential in determining the onset of viral epidemics and preventing their spread. Patolsky et al. applied SiNW FETs for real-time, highly sensitive detection of single virus particles [21]. Silicon nanowire transistors modified with antibodies for influenza A showed discrete conductance changes characteristic of binding and unbinding of single influenza A virus on the surface of the nanowires. In addition, multiple viruses were selectively detected in parallel by using nanowire biosensors modified with antibodies specific for either influenza or adenovirus. Shen et al. developed SiNW biosensors for the rapid and reliable diagnosis of influenza A viruses at a concentration down to 29 viruses/μL in clinical exhaled breath condensate samples [22]. The nanowire biosensors allowed a rapid detection of influenza A viruses within minutes, which was two orders of magnitude faster compared to the standard method RT-qPCR [23]. In addition, high selectivity of SiNW biosensors was demonstrated using H1N1 viruses, 8-iso-PGF2a, and inert nanoparticles. Furthermore, the diagnosis of dengue, a commonly prevalent arthropod-borne viral infection, has also been successfully demonstrated by the grafting of specifically designed PNA probe molecules onto the surface of SiNW FETs [24].

A variety of other semiconductor nanowires have also been applied as building blocks in affinity biosensors. For example, zinc oxide (ZnO) is a promising semiconducting and piezoelectric material for bioelectronics. Yu et al. used ZnO nanowire transistors functionalized with gold nanoparticle-anti-immunoglobulin G

conjugates (Au NP-anti-IgG) for the specific detection of Immunoglobulin G (IgG) [25]. Under a compressive strain of 0.8%, the piezotronic effect of ZnO nanowire largely enhanced the resolution of the biosensors by lowering the contact barrier of the transistor. As a result, a tenfold increase in sensitivity was achieved for the detection of IgG. In addition, n-type indium oxide (In_2O_3) nanowires with a band gap of 2.8–3.6 eV have been applied for the detection of prostate-specific antigen (PSA), which resulted in a detection limit of 5 ng/mL [26].

The use of semiconductor nanowires in affinity biosensors has taken off rapidly and will surely continue to expand. Nanowire affinity biosensors provide the most straightforward option for the detection of biomolecules with improved resolution, even at the level of individual viruses. The large-scale assembly of nanowire arrays enables parallel, sensitive detection of multiple biological species. Despite the tremendous potential of nanowire affinity biosensors, several challenges should be addressed before they can be actually put into practice. Firstly, a unique challenge to nanowire biosensors is their heterogeneous interface structure, in which the solid-state nanowire transistors are in direct contact with the wet-phase biological targets. The surface chemistry of the semiconductor nanowires, including the coverage and configuration of the receptor and the interaction between the receptor and the target, needs to be characterized to optimize the sensitivity of the biosensors. In addition, nonspecific binding, in which nontarget biomolecules stick to the surface of the nanowire, should be minimized to decrease the background signals and increase the sensitivity of the biosensors. Thus, robust and well-characterized passivation schemes are urgently needed to block nonspecific binding sites on the nanowire surface. Secondly, the stability of the biosensors is a critical feature for their successful practical applications. Silane condensation on oxide surface has been found to be reversible in aqueous solutions. The stability of the silane layer on the nanowire surface is yet to be characterized in physiological solutions and biofluids, including blood serum and urine. In addition, the stability of the solid-state silicon nanowires exposed to physiological solutions needs to be addressed. Thirdly, device-to-device variation in biosensor performance remains a great challenge for chemically synthesized semiconductor nanowires. The device-to-device variation can be attributed to fluctuations in the actual nanowire size and doping level, the existence of the contact barrier, and the distribution of the surface functional groups. Lastly, the performance of nanowire biosensors is fundamentally limited by the Debye screening which determines the distance over which a charge can be sensed in liquid media. To circumvent the Debye screening effect, former work typically operated the nanowire affinity sensors in diluted buffers with long Debye screening length. However, for practical applications, the nanowire biosensors would preferentially work in biofluids with typical Debye screening length of ca. 1 nm. Recent studies showed that polymers, including PEG, can substantially change the dielectric properties and thus increase the effective Debye screening length near the solid surface, which may represent as a promising strategy to circumvent the problem of Debye screening [27].

9.2 Nanowire Bioelectronics for Extracellular Recording

Electrophysiological recording is essential to understand the bioelectrical activities of the body, such as in the brain, heart, and muscles. The lipid bilayer membranes of electrogenic cells, such as neurons and cardiomyocytes, contain a number of ion channel proteins that regulate the transport of selected ions across the cell membranes. During a transient impulse discharge, ions flow across the cell membrane, which leads to both intracellular and extracellular potential spikes. The impulse waves propagate through the heart, resulting in cardiac contraction which propels the blood. In the brain, impulse activities propagate among neural networks to carry out diverse functions of the brain, including learning and memory. The bioelectrical activities in a human brain can be categorized at three different levels: the impulse activities of individual neurons, spatiotemporally coordinated activities of neural networks, and regional neural activities during cognitive and motor tasks. Thus, an ideal bioelectronics platform for electrophysiological recording should provide both high spatial resolution to resolve single neurons and even single neurites and the ability to simultaneously record from large neural networks. In addition, implanted electrodes should be biocompatible for long-term, chronic recording and stimulating of bioelectrical activities of both the brain and heart.

A metal electrode or a transistor positioned near an electrogenic cell can be applied to record the extracellular potential spikes. For example, metal electrode arrays (MEA) have been widely applied for multi-site extracellular recording and stimulation of cardiac or neural activities [28]. However, extracellular signals recorded by MEAs suffer from poor signal-to-noise ratio (SNR). In addition, the spatial resolution of MEAs is limited to tens of micrometers, which is comparable to the cell body but larger than neurites. Reduction of the size of the metal electrodes can increase their spatial resolution. However, the size reduction of the metal electrodes leads to increased impedance, which thus results in increased thermal noise and decreased SNR [29]. As an alternative to metallic microelectrodes, electrolyte-oxide silicon field-effect transistors (EOS-FETs) and their arrays have been developed for multi-site extracellular recording. The extracellular potential spikes can modulate the carrier density in the semiconductor through the electrolyte double-layer capacitance and generate an electric signal in the transistor. Recently, semiconductor nanowire FETs are being actively explored in extracellular recording to substantially improve the spatial resolution.

Patolsky et al. first applied SiNW FETs for the in vitro extracellular recording of single neuron activities in 2004 [30]. As shown in Fig. 9.2a, neonatal rat cortical neurons were cultured on an array consisting of four nanowire transistors. Polylysine patterning was used to guide the growth of neurites across the transistor channels. After 4–8 days of incubation, the dendrites and axon of a single neuron were shown to spread across the four nanowire transistors, forming localized nanowire-neurite junctions of only 0.01–0.02 μm^2. The nanowire transistor array was shown to enable multi-site recording from a single neuron. They further showed that nanowire transistors could work as local input to stimulate the impulse activities of neurons.

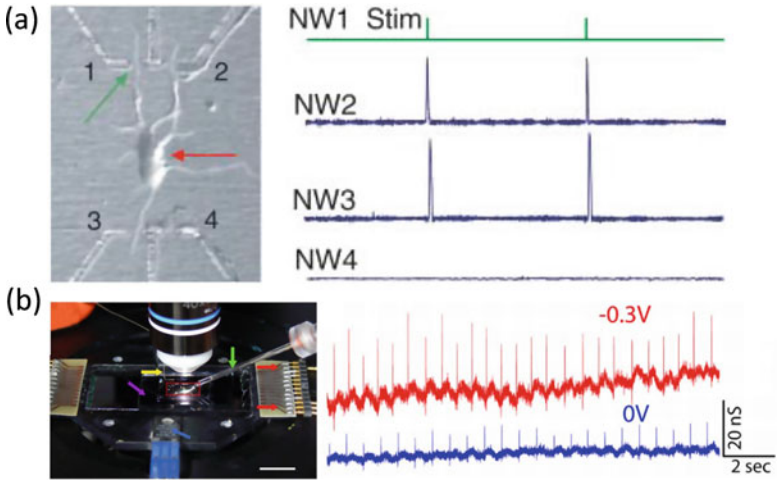

Fig. 9.2 Nanowire bioelectronics for extracellular recording. (**a**) Extracellular recording of neurons. Left: optical image of a cortex neuron and four SiNW FETs arranged at four corners of a rectangle. The FET labeled 1 is used for the stimulus input, and FETs labeled 2 and 3 are connected with two dendrites of the neuron. The FET labeled 4 is not connected with any part of the neuron. Right: in situ current recording of the four FETs shown on the left. (Reprinted with permission from Ref. [30], Copyright 2006, American Association for the Advancement of Science). (**b**) Extracellular recording of cardiac tissues. Left: the photograph of the interfacing between PDMS-supported cardiomyocytes and SiNW FETs. Right: the recording of spontaneously beating cardiomyocytes under different gate voltages. (Reprinted with permission from Ref. [31]. Copyright 2009, National Academy of Sciences)

In addition, an array consisting of 50 individual FETs were further applied to measure the impulse propagation rate along dendrites and axons. The signal propagation rate was determined to be 0.16 m/s for dendrites and 0.43 m/s for axons, respectively.

In 2009, the extracellular recording of cardiomyocyte monolayers was achieved with SiNW FET arrays [31]. Embryonic chicken cardiomyocyte monolayers were cultured on PDMS substrates. A PDMS substrate with the cardiomyocyte monolayer was brought in contact with a device chip integrated with SiNW FET array. The distance between individual nanowires was 300 μm. The impulse propagation in the cardiomyocyte monolayer was recorded by the nanowire transistor array with SNR > 10 (Fig. 9.2b). The impulse propagation rate was determined to be 0.07–0.21 m/s based on a cross-correlation method. In addition, Pui et al. directly cultured cardiomyocyte cells on top-down processed silicon nanowire transistor arrays [32]. Hundreds of aligned long SiNWs were fabricated by deep UV lithography and self-limiting oxidation, which were applied for real-time extracellular recording of cellular bioelectricity.

Nanowire transistors have also been applied to map the functional connectivity of brain slices and the signal propagation in isolated hearts. SiNW FET arrays on transparent substrates were interfaced to acute brain slices of a rat by Qing et al.

[33]. The bioelectrical activities of the brain slices were recorded by the SiNW FET arrays with high temporal and spatial resolution, which revealed the spatially heterogeneous functional connectivity in the olfactory cortex. In addition, the transparent device chips enabled imaging of individual cell bodies and identification of areas of healthy neurons at both upper and lower tissue surfaces. The signal amplitudes of the nanowire transistors were from 0.3 to 3 mV. Compared to conventional MEAs, the active surface of the NWFET devices was only ~0.06 μm^2, and the spacing between individual nanowires was as small as 5 μm, enabling highly localized multi-site measurements of neuronal activities with sub-millisecond temporal resolution.

Timko et al. prepared SiNW FET arrays on flexible and transparent polymeric substrates, which allowed reproducible interfacing with spontaneously beating embryonic chicken hearts in both planar and bent conformations [34]. The conductance change associated with beating could be tuned by device sensitivity, although the voltage-calibrated signals, 4–6 mV, were relatively constant due to the stable transistor-heart interface. In addition, multi-site recording with nanowire transistor arrays yielded signal propagation times across the myocardium with high spatial resolution.

Nanowire bioelectronics is a promising candidate for multi-site extracellular recording with high temporal and spatial resolution. Yet, the SNR of nanowire bioelectronics requires further improvement to resolve subthreshold synaptic potentials generated by single cells. Firstly, the electrical coupling between a neuron or a cardiomyocyte and a nanowire needs to be improved. The low coupling efficacy of ca. 0.1–1% between a cell and a planar substrate implies that only a small fraction of the ionic current can be translated into electronic current of the transistor. Secondly, electrolyte-gated transistors are limited by 1/f noise or flicker noise [35]. The origin of 1/f noise has been attributed to the semiconductor material quality and interface-induced carrier scattering. Recent study has shown that the 1/f noise level of graphene bioelectronics can be greatly suppressed through the suspension of graphene, which effectively enhanced the SNR of the extracellular signals [36].

9.3 Nanowire Bioelectronics for Intracellular Recording

Extracellular recording technique is a powerful tool for long-term recordings of neural or cardiac activities. However, extracellular recordings suffer significantly from low signal amplitude due to the large leakage current along the cleft between the electrode and the cell. On the other hand, intracellular probes can form good electrical coupling with the cell and record the entire electrophysiological repertoire generated by the electrogenic cell. Traditional patch-clamp technique can penetrate the plasma membrane and directly interrogate intracellular potentials of single cells [37]. But patch-clamp technique has been suffering from both mechanical instability and low throughput, which limits its application in long-term recording or studying network activities. Recently, a number of laboratories

began to develop hybrid techniques to merge the benefits of MEAs, including long-term stability and multi-site measurements, with the power of intracellular recording and stimulation. For example, pioneer work by Hai [38] et al. developed a gold mushroom-shaped protruding microelectrode. The gold mushroom-shaped microelectrodes could be engulfed by neurons, which effectively increased the neuron-microelectrode electrical coupling coefficient from approximately 0.1% to approximately 50%. The increased coupling coefficient enabled intracellular recording of both action potentials and synaptic potentials. On the other hand, vertical nanowires of 150 nm in diameter and a few micrometers in height have been integrated on planar electrode arrays by Robinson et al. [39] and Xie et al. [40], respectively. The vertical nanowires were able to access the intracellular cytosol by either spontaneously penetration or electroporation. In addition, multi-site intracellular-like recording of neural networks or cardiomyocyte networks has been demonstrated with the vertical nanowires.

The nanoscale dimensions of SiNW FETs make them potential candidates for intracellular recordings. In addition, complex structural motifs in the silicon nanowires can be rationally designed and added at molecular-scale precision by synthesis. Firstly, the compositions of NWs can be precisely modulated along axial or radial directions during growth. Secondly, kinks can be formed along nanowires by short interruptions of growth. Thirdly, hierarchical branching nanowires can be formed through sequential seeding of the catalysts. These NW motifs can function as point-like probes to enter cells through endocytic pathways and directly access the intracellular cytosol. For example, Tian et al. demonstrated the first transistor-based intracellular recording with a kinked SiNW FET. A kinked nanowire structure was synthesized by introducing a perturbation during synthesis, which was suitable for the noninvasive entrance of the cell [41]. The free arms of the kinked nanowire were heavily doped and linked with flexible electrodes. The phospholipid modified apex of the kink was applied to interface a live cell and record the bioelectrical activities of the cell [42]. The recorded currents were shown to transform from extracellular signals to intracellular signals within 40 seconds, indicating a spontaneous internalization process of the kinked nanotransistor (Fig. 9.3a).

In 2012, Duan et al. developed an intracellular probe by synthesizing an insulating SiO_2 nanotube on top of a SiNW as a "branch" [43]. The free end of the nanotube was modified with phospholipids, which promoted a spontaneous penetration of the nanotube into the cell and form a strong sealing with the cell membrane. A branched SiO_2 nanotube, with inner diameter of $\sim$ 50 nm, was synthetically integrated on top of a SiNW transistor (Fig. 9.3b). After phospholipid bilayer coating, the nanotube was shown to spontaneously penetrate the cell membrane. As a result, the cell cytosol was brought into contact with the transistor by the nanotube. The intracellular potential of the cell modulated the conductance through the SiNW transistor. The inner diameter of the penetrating nanotubes was as small as 3 nm, and the cytosol in the nanotube was estimated to be only 3 aL. Besides, the nanotube branched nanowire transistor could survive for at least five cyclic penetration-retraction processes, with no change in the recorded signal, demonstrating the robustness of the nanoprobe and the nanoprobe-cell interface. Notably, intracellular

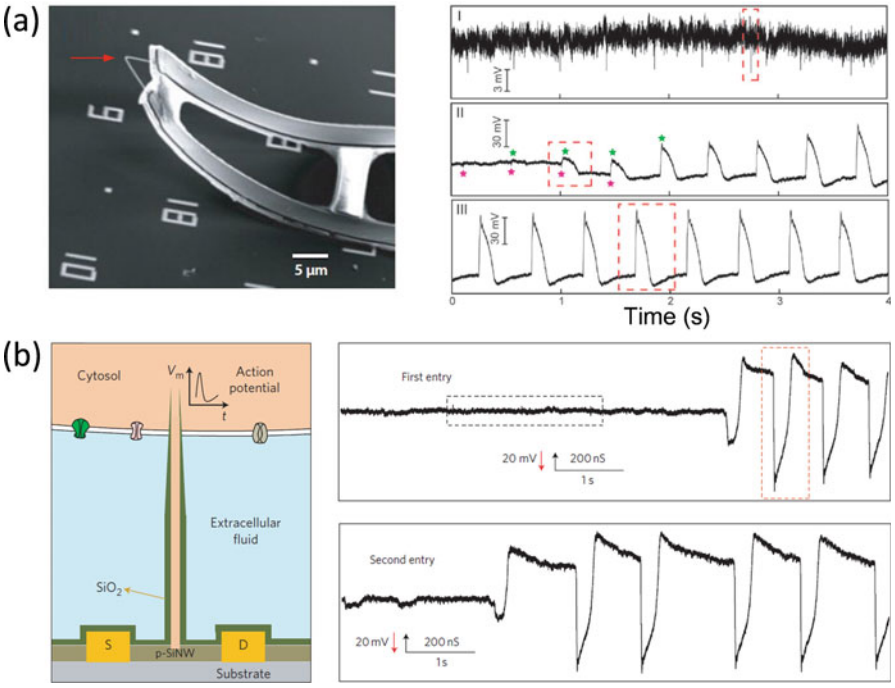

Fig. 9.3 Nanowire bioelectronics for intracellular recording. (**a**) Kinked nanowire for intracellular recording. Left: the SEM image of a kinked nanowire biosensor. Right: electrical recording from beating cardiomyocytes – (I) extracellular recording, (II) transition from extracellular to intracellular recording during the penetration of the probe, and (III) steady-state intracellular recording. (Reprinted with permission from Ref. [42]. Copyright 2010, American Association for the Advancement of Science). (**b**) Nanowire linked nanotube probe for intracellular recording. Left: the schematic of measurement process. Right: the transition from extracellular recording to intracellular recording for the first and second entry into the cell. (Reprinted with permission from Ref. [43]. Copyright 2012, Nature Publishing Group)

signals from a single cardiomyocyte were simultaneously recorded with two branched transistors separated by only ~ 20 μm.

Gao et al. developed an intracellular probe by using a silicon nanotube transistor [44]. Source and drain electrodes were fabricated at one end of a silicon nanotube, and the outer face of the active nanotube between the source and drain electrodes was insulated by dielectric coatings. The other end of the nanotube was modified with phospholipids for spontaneous penetration across the cell membrane and bringing cytosol to the inner tube area of the active nanotube channel. Full-amplitude intracellular action potentials of spontaneously beating cardiomyocytes were recorded by the silicon nanotube transistor.

The spontaneous cellular internalization of nanotransistors provides both effective neuron-electrode coupling and intracellular access. Semiconductor NW building blocks excel among nanomaterials in their capabilities to be rationally designed and synthesized with complex motifs at molecular-scale precision. It is worth noting

that applications of semiconductor NWs in intracellular recording are still in the preliminary stage. The SNR of the nanotransistors is still lower than that of glass micropipettes, which requires further reduction of the intrinsic 1/f noise of the nanotransistors. In addition, the long-term in vivo stability of the nanotransistors remains to be investigated before their full capabilities can be determined.

9.4 Nanowires for 3D Interfacing with Biological Systems

Commonly used MEAs are made of stiff materials, such as platinum, with elastic moduli from 10 to 100 GPa, which significantly exceeds those of neural tissues in the range of kPa to MPa. The drastic mechanical mismatch between implanted electrodes and tissues results in relative micromotion of electrodes within tissues. Micromotion causes inflammatory response of the neural tissues, which results in the formation of glial scars that insulate the electrodes from bioelectrical signals, which eventually leads to electrode failure in long-term, chronic studies [45]. Recent progress in bioelectronics has been driven by advances in flexible electronics. For example, Rogers et al. demonstrated ultrathin polyimide-supported MEAs with an open mesh design by using dissolvable silk films as supports [46]. As the thickness of the polyimide-supported MEAs was reduced to 2.5 μm, the electronics established a highly conformal contact with animal cerebral cortex.

In 2012, Tian et al. integrated nanowire transistors in 3D macroporous polymer scaffolds, the NanoES, for culture of cells [47]. Embryonic rat hippocampal neurons were cultured on the NanoES merged with Matrigel. After 2 weeks, dendrites extended into the porous structure of the NanoES scaffold. In addition, cardiomyocyte cells could also be seamlessly merged with the nanowire transistors in the macroporous scaffolds, which further allowed 3D monitoring of the signals from the cardiomyocytes by nanoelectronics (Fig. 9.4a). The characteristics of the spikes approach those of extracellular recordings, indicating a high level of signal fidelity [47]. In addition, the frequency of spikes doubled with the addition of noradrenaline, a promoter for cardiac contraction. The results above validate the potential of the NanoES based scaffold for the investigation of pharmaceutical effects of biological systems. In the same report, NanoES immersed synthetic vessel was fabricated to monitor the pH change of the fluids passing by. Since the pH change of the blood is a strong indication of many physical disorders, such as inflammation and cancer, the synthetic vessels could play an important part in the monitoring of physical conditions in patients.

Recently, Liu et al. fabricated a freestanding mesh electronics which can be injected into a rat's brain with a syringe (Fig. 9.4b) [48]. The thickness of the mesh electronics was only 0.8 micrometer. As a result, the mesh electronics could be folded to less than 1/30 of its original volume in the syringe and then fully extended after released to the cavities of the brain. The mesh electronics could interface compatibly with rat hippocampal neurons and monitor the internal mechanical strains in real time. The flexible and sensitive electronics could also be

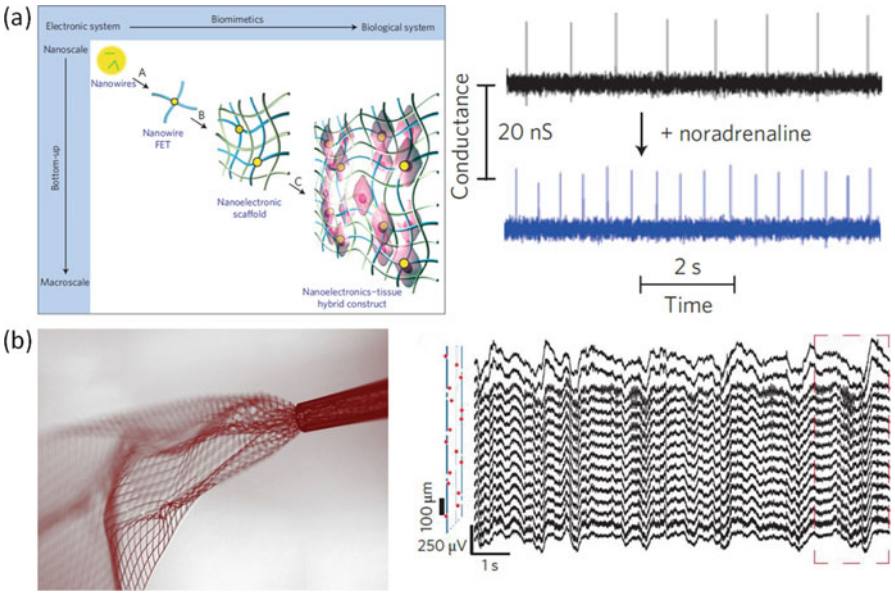

Fig. 9.4 3D interfacing of bioelectronics and tissues. (**a**) The merging of nanoelectronic scaffold and cardiac tissues. Left: the schematic of the merging process. Right: the electrical recording before (top) and after (bottom) the addition of noradrenaline to the cardiac tissue. (Reprinted with permission from Ref. [47]. Copyright 2012, Nature Publishing Group). (**b**) Syringe-injectable electronics. Left: the photograph of the injectable nanomesh. Right: 16-channel recording within a mouse brain by the injected nanoelectronics. (Reprinted with permission from Ref. [48]. Copyright 2015, Nature Publishing Group)

utilized for both signal recording and actuation [49]. Compared with rigid implanted electronics, the flexible mesh induced far less immunological response of the brain with minimal astrocyte proliferation. The capability of chronic brain mapping renders the injectable nanoelectronics a very promising tool in brain science.

Significant achievements have been made for the 3D electrical interfacing with biological tissues. However, the nature of the 3D electronics-tissue interfaces remains to elucidated. Besides, future studies could integrate other functional components, including chemical and optical inputs, with nanowire bioelectronics to enrich their functionalities.

9.5 Conclusion and Prospects

Semiconductor nanowires have been shown to be a versatile tool for interfacing biology at different levels. Biological elements as small as ions and molecules and as large as the whole organs can be analyzed or interrogated with NW electronics. The high surface-to-volume ratio of nanowire electronics ensures high sensitivity in biosensing. Besides, nanowires can be easily integrated into flexible electronics

which allow chronically stable recording of biological signals. The development of 3D electronic-tissue interfacing facilitates not only sensitive monitoring but also efficient manipulation of biological activities. It will be especially important for future studies to translate these laboratory works into clinical applications, such as point-of-care biosensors and neural prosthesis. Finally, the development of integrated and multifunctional nanowire bioelectronics will be of great importance for both fundamental and clinical neuroscience.

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Chapter 10
Nanowires for Triboelectric Nanogenerators

Ying-Chih Lai

10.1 Introduction of Triboelectric Nanogenerators

Currently, the personal portable electronics are powered by traditional batteries. However, as the electronic elements and power consumption increase, the power source has become an issue because it is impractical to frequently recharge or replace the batteries. Especially, for implanted and biomedical electronic systems, to replace the power sources is unrealistic. Moreover, list of the shortcomings of the conventional power sources includes not only the limited capacity but also environmental pollution and possible explosion and health hazards. Besides, the heavy and rigid boxy batteries hinder the further development of flexible and wearable electronics and biomedical electronics. On the other way, most of the existing sensing technologies need to be pre-supported and pre-offered electrical or optical signals to sense environmental information, which inevitably requires foreign power sources. With the increased number and density of sensing networks, the sensors that can be of low-power consumption or even self-powered will be desired for future electronic modules [1–7].

TENG was first invented by Zhong Lin Wang's group in 2012 [8]. A more and deep study and discussion about TENGs can be found in another reference book [1]. Such devices utilize the conjunction of the triboelectrification and electrostatic induction to convert ubiquitous mechanical energy into electricity. The devices can act as efficient and sustainable energy converters and providers from harvesting

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environment low-frequency mechanical energy, such as wind, wave, river flow, rain drop, human body motions, and so forth [2–6, 9]. The collected energy can be converted to electric energy sources for continuously powering electronic devices and even systems [10]. Triboelectric effect is a contact-induced electrification in which a material turns into electrically charged after it is physically contacted with another different kind of materials. It is a natural phenomenon, and, probably, most of the people have been experiencing the triboelectric phenomena in our daily life. However, the mechanisms and availability of triboelectrification were seldom to be explored [11, 12].

When two materials are contacted with each other through friction, the two materials can become electrically charged, which is triboelectrification effect. And, the sign of the charges that are carried on the materials depends on its relative electronegativity in comparison to the contact materials [13]. The effect is generally believed from the fact that when two materials are contacted, charges between some parts of two materials' surfaces transfer from one material to the other due to the tendency to form chemical bonds between two materials, i.e., adherence forces. When the two contacted materials are separated, some of the bonded atoms on the material's surface have an inclination to keep the extra electrons, and some have a tendency to offer electrons. This fact results the triboelectric charges on the two materials' surfaces. As the two surfaces are separated by mechanical forces, the contact-induced electrostatic charges can generate a potential difference.

The work principle of a typical triboelectric nanogenerator can be illustrated in Fig. 10.1 [14]. The typical device is constructed by two dissimilar dielectric materials, i.e., Kapton and polymethyl methacrylate (PMMA) (Fig. 10.1a-I). The two dielectric materials are faced to each other. And, metals that act as electrodes were deposited on the other surfaces of the two dielectric films. The external circuit was connected through the two electrodes. When the two dielectric films are physically contacted by external mechanical forces, surface charges can transfer and create oppositely triboelectric charges on the two contacted surfaces due to the triboelectric effect, as depicted in Fig. 10.1a-II [11, 15, 16]. According to the triboelectric series [17], in a list regarding ranking materials based on their tendency to receive or offer charges, negative electrons from the surface of PMMA have the tendency to transfer onto the surface of Kapton, which results in net negative charges on the Kapton surface and net positive charges on the PMMA surface, respectively. The transferred triboelectric charges are able to keep on the dielectric surfaces for a long-time retention owing to the insulating property of the polymers [18]. At this contact stage, the amounts of transferred negative and positive charges are generated at the same time. And, both contact-induced charges are confined on each material's surface; as a result, there is no electric potential difference between the two electrodes. When the two dielectric materials are detached by some mechanical motion, the opposite triboelectric charges on the two materials' surfaces can be separated apart, and then a potential difference can be formed between the two electrodes under the open-circuit condition, as shown in Fig. 10.1a-III, IV. The open-circuit voltage generated by the TENG increases to the maximum value until the two dielectric materials are fully separated to the original position, as described in

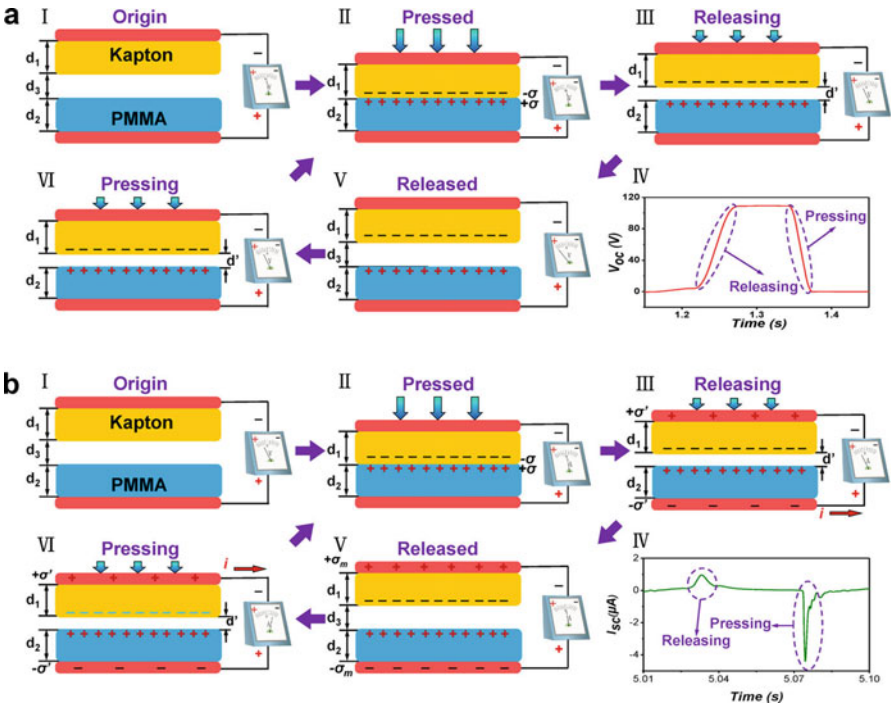

Fig. 10.1 Working principle of the triboelectric generator. (**a**) Open-circuit condition. (**b**) Short-circuit condition. (Reprinted with permission from American Chemical Society [14])

Fig. 10.1a-IV, V. When there is some external motion that can make the two dielectric materials getting close again, the generated potential difference decreases. As a result, the generated open-circuit voltage declines from the maximum value to original level when two dielectric materials are fully touched again, as illustrated in Fig. 10.1a-VI.

When the external circuit connected to the two electrodes is shorted, the transferred charges on the two dielectric materials can induce opposite charges on the electrodes to balance the charges on the dielectric materials, as described in Fig. 10.1b-I. Initially, at the beginning contact stage, the electric charges on the dielectric materials can transfer to each other, as depicted in Fig. 10.1b-II. As the dielectric film is separated, the generated potential difference can drive electrons from the electrode of Kapton to the electrode of PMMA to balance the triboelectric charges on the Kapton and PMMA surfaces (Fig. 10.1b-III). This separation process can lead to an instantaneous positive current, as shown in Fig. 10.1b-IV. As the two dielectric films are separated to its original position, the triboelectric charges on the dielectric films are balanced by the induced charges on the electrodes (Fig. 10.1b-V). When some mechanical motion makes the dielectric materials get close again, the induced electrons on the electrode of PMMA can be driven to flow back to the electrode of Kapton because the transferred charges tend to be balanced and

neutralized by the charges on surfaces of Kapton and PMMA, as described in Fig. 10.1b-VI. This pressing process can cause an instantaneous opposite current, as shown in Fig. 10.1b-IV. All induced charges on the electrodes of Kapton and PMMA are neutralized once the two dielectric materials are fully contacted again, as shown in Fig. 10.1b-II.

The above demonstration is a typical example about a TENG device that harvests mechanical energy and converts it to electric energy. There are four basic modes of TENGs including vertical contact-separation [8], lateral sliding [19], single electrode [20], and freestanding triboelectric-layer mode [21]. Each mode has different advantages in different applications. Materials for triboelectric effect include almost all materials ranging from metals, polymers, skins, cottons, woods, and so on, which means that the materials used for designing TENGs can be huge and diverse.

10.2 Nanowire-Based Flexible TENGs

Nanowires used for designing TENGs enable to promote the abilities and functions of TENGs. Several results have been explored for using conducting nanowires to design the electrodes of TENGs [22–28]. It is worth to note that TENGs possess unique advantages in collecting mechanical energy at low-frequency (<5–10 Hz) regime [29]. In nature, most motions are at low-frequency regime, such as wind blow, water wave, human motions, and so forth. In order to broaden the usages of TENGs in various kinds of situations, it is necessary to design TENGs that are able to deform, stretch, and adapt their shapes for applying on various objects or motion bodies to harvest various kinds of mechanical energy. The human body is soft, irregular, and movable; therefore, designing flexible, deformable, and durable TENGs is especially important for wearable and biomedical uses to harvest energy from human motions, such as walking, tapping, breathing, joint motions, muscle motions, and so on [27, 30, 31].

A variety of materials, including conducting polymers, carbon nanotubes, buckled and serpentine-structured metals, and liquid metals, have been explored as electrical components for the devices that can be soft, flexible, bendable, stretchable, and even deformable. However, conducting polymers and metal thin films suffered from plastic deformations after repeatedly applying strain [30]. Also, the stretchabilities based on conducting polymers and metal thin films are inadequate, which may hinder the TENGs in wearable and conformal uses. And, liquid metals suffer from the issue of high cost and metal-liquid leakiness. By contrast, percolating networks of one-dimensional conducting nanowires have been shown as promising candidates for stretchable electronics by adapting strain via sliding and buckling of the nanowires [32].

Among various conducting nanowires [33], silver nanowires (AgNWs) are one of the common materials acting as stretchable electrodes due to their excellent conductivity, flexibility, stretchability, and low-cost manufacturability advantages. Based on the inherent stretchability and high conductivity, a mechanically durable and super-stretchable electric eel skin-like TENG was realized through the composite of AgNWs and elastic polymers [27]. The electric eel skin-like TENG simultaneously possesses soft feature and the capability to produce electricity while being touched, as depicted in Fig. 10.2a. The intrinsic stretchable components of AgNWs and elastic polymers endow the skin-like TENG excellent mechanical durability and resilience. The schematic diagram of fabricating the stretchable TENG is shown in Fig. 10.2b. Percolating AgNWs acted as the stretchable conducting electrode. And, the networks of percolating AgNWs were sandwiched between elastic silicones. Figure 10.2c shows a cross-sectional scanning electron microscopy (SEM) image of the embedded AgNWs. The components of percolating AgNWs matrix and silicone enable the TENG to fairly endure different mechanical forces and deformations, including twisting, folding, and stretching, as demonstrated in Fig. 10.2d.

The working mechanism of such TENG is illustrated in Fig. 10.2e. Due to the skin and elastic silicone that possess different electron negativities, the electrons on the surface of the skin can transfer to the surface of silicone when the skin touches the elastic polymer. And, after the skin leaves the surface of silicone, the negative electrons on the surface of silicone can induce positive charges in the embedded AgNWs; as a result, free electrons in the embedded AgNW matrix can be driven to flow to the external circuits and provide an output current and voltage signal to the connected element. When the skin touches the polymer again, the induced positive charges in the embedded AgNWs reduce, and the electrons from the reference electrode flow back to the embedded AgNWs; as a result, a reversed electrical output signal can be generated. Repeatedly touching the silicone can generate alternating current to the external load.

Figure 10.2f shows the generated output open-circuit voltage of the skin-like TENG. The generated open-circuit voltage of the skin-like TENG can reach to ~70 V with a contact area about 1.5 × 1.5 cm^2. And, ~100 $\mu C/m^2$ of transferred charges can be reached by simply touching the device (Fig. 10.2g). As a result, ~6 mA/m^2 of short-circuit current can be obtained at a contact frequency of 4 Hz, as shown in Fig. 10.2h. The produced power from the skin-like TENG is shown in Fig. 10.2i. When the load resistance is about 200 MΩ, the maximum output power of 0.5 W/m^2 could be achieved by the skin-like TENG. The resulted device is robust that can endure numerous operations as shown in Fig. 10.2j, which the output current showed no obvious degradation after 3600 times operation. Figure 10.2k demonstrated that the device can directly light up ten LEDs by simply touching.

The intrinsic stretchability of the AgNWs enables the energy harvesting device to tolerate various extreme forces and deformation. Figure 10.3a shows the image that

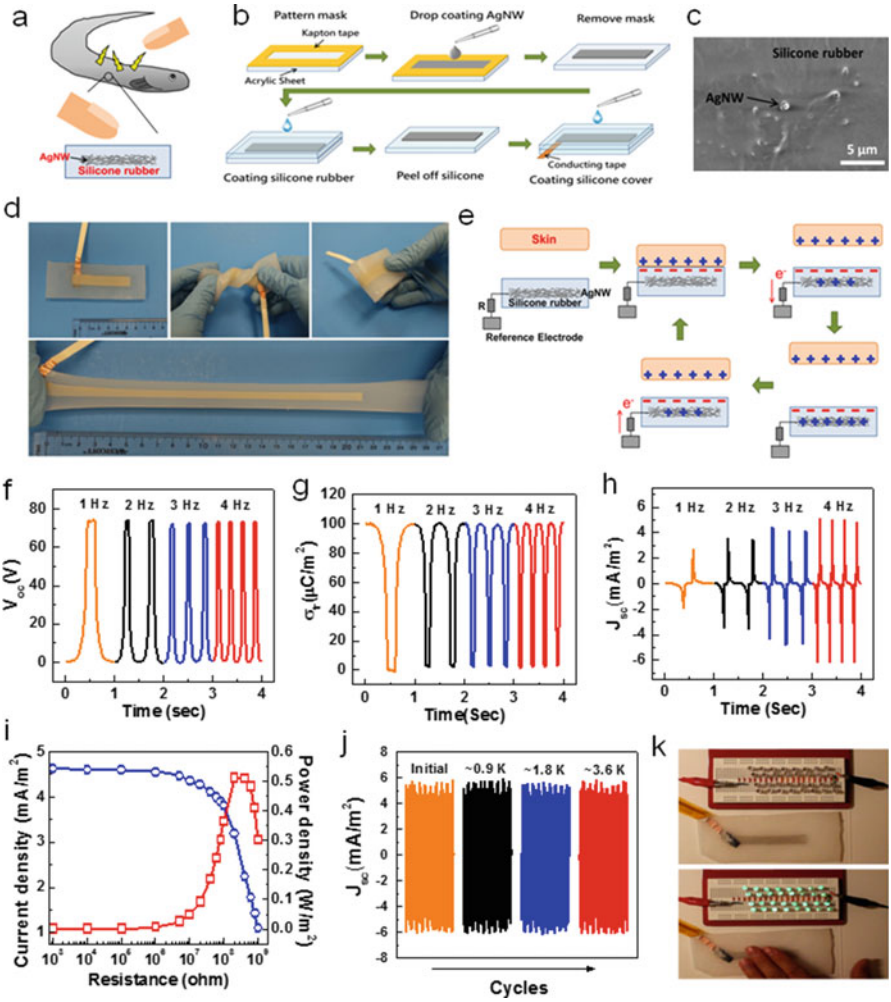

Fig. 10.2 Skin-like super-stretchable and durable triboelectric nanogenerator. (**a**) Concept of an electric eel skin-inspired TENG. (**b**) Schematic diagram of fabrication processes. (**c**) Side view of SEM image of the device. (**d**) Images of TENG with demonstrations of different deformations including twist, fold, and stretch. (**e**) Schematic illustration of mechanism for generating electricity. (**f**) Open-circuit voltage, (**g**) transferred charge density, and (**h**) short-circuit current density of the nanogenerator. (**i**) Relationship between instantaneous power density and the external resistance. (**j**) Short-circuit current density after continuous operation for 900, 1800, and 3600 cycles. (**k**) Image showing that 32 LEDs were lit up when the device was touched. (Reproduced with permission from Wiley [27])

the TENG can scavenge energy from touch and power up a series of LEDs when it was stretched in its long-axis direction. Figure 10.3a (right) shows the produced output current under different levels of strain. The results clearly show the fact that the output generated current increases as the strained length increases. This may be attributed to the fact that the thickness of the silicone became thinner after the device was stretched [27]. Such results are similar as the device under stretching in the short-axis direction, as shown in Fig. 10.3b. Both results show that the device can retain its capability to harvest energy from skin touch even extending the device to a strain of 300%. Moreover, the performance can be recovered when the applied stretching force was released. The device can be also operated even under multiple twists and folds, as shown in Fig. 10.3c and 10.3d, respectively. The results can clearly indicate the fact that the conducting nanowires enable the excellent mechanical durability and flexibility of the energy harvesters. Not only that, the device can retain its function to harvest touch energy even experiencing severe tearing damages. As shown in Fig. 10.3e, the device that was cut four times in half through the conducting network can still retain its stretchability and capability to collect touch energy and power up the LEDs.

Furthermore, the excellent stretchable skin-like TENG can be biaxially stretched, as demonstrated in Fig. 10.4a. Due to the super soft and extreme stretchability of the TENG, the device can be easily conformal on the surface of various desired objects to collect environment energy. As shown in Fig. 10.4b, the TENG fabricated by the AgNWs was multiply stretched, twisted, and folded to wrap a small sphere, and the device can well keep its capability to generate electricity. Figure 10.4c shows a ball attached with the flexible TENG. The shape of skin-like TENG can be adaptive on the ball and produce electricity from human touch. Furthermore, Fig. 10.4d shows that the flexible TENG can be extremely expanded and wrapped on the cap of a tube with no rupture, which exhibits the toughness and softness of the nanowire-fabricated skin-like TENG. The softness and flexibility of the TENG enable it to easily fit on irregular and movable human body uses. Figure 10.4e demonstrates that the TENG wrapped on a human wrist to harvest the touch energy and sustainably drive a commercial smart watch by connecting a power management circuit. From the above demonstrations, it can be clearly observed the softness, flexibility, stretchability, and durability of the TENG that was fabricated by using conducting nanowires.

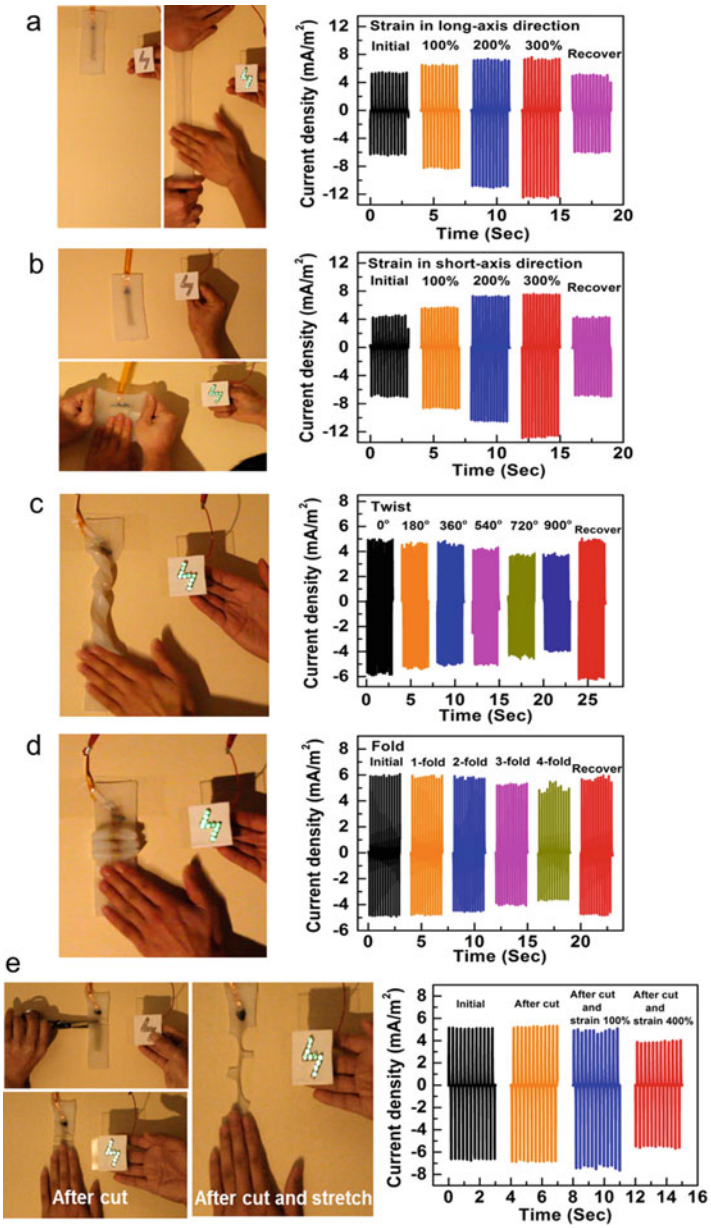

Fig. 10.3 Performance of the TENG under different deformations and even being damaged. (**a**) Left: Image showing that the device can function well and drive a load when it is extremely stretched in long-axial direction. Right: Short-circuit current density at various strain levels in long-axial direction. (**b**) Left: Image showing that the device drove a load when it was stretched in short-axial direction. Right: Short-circuit current density at various strain levels in short-axial direction. (**c**) Left: Image demonstrating that the device drove a load when it was multiply twisted. Right:

10.3 Nanowire-Based Self-Powered Electronic Skins

Besides acting as energy harvesters, because of the energy harvested from skin touch, the TENGs can also use as self-powered tactile devices. As shown in Fig. 10.5a, the AgNWs were deposited as 3 × 3 array and embedded in elastic polymer. The 3 × 3 array acts as a self-powered tactile sensing system that can produce electricity from converting skin touch energy to light up a LED and visibly indicate the touching position without the need of data acquisition circuits and external power supply. Each sensing pixel connected to one LED can map the touching position and respond via intuitively visible LED signals. The self-powered tactile sensing system can adapt its shape to wrap on a human body, as shown in Fig. 10.5b. When the unit of TENG was touched by the skin, the corresponding LED was lit up to identify the touched position, acting like a self-powered electronic skin. And, Fig. 10.5c shows the system attached on a ball. Similar as the results on human arm, the LED lit up to point the position touched by a finger. The presented sensing system based on AgNWs is highly conformal to various substrates with different shapes. And, the deformable tactile sensing system is all self-sufficient without the need of foreign batteries.

10.4 Summary

In summary, a highly deformable and durable skin-like TENG that was fabricated based on conducting nanowires has demonstrated its capability to scavenge energy and act as self-powered tactile sensing systems. The intrinsic flexibility and stretchability of conducting nanowires enable the energy-harvesting devices to collect energy and generate electricity regardless of its physical presentation, including extremely stretching over 300% strain, omnidirectionally stretching, as well as multiple folding and twisting. Furthermore, even if the flexible TENG undergone several tearing damages, it can still retain its functionality and stretchability to scavenge environment touching energy. Due to the attributes of flexibility, stretchability, and deformability, the energy-harvesting devices can be applied on various objects with regular or irregular surfaces, such as human arm, ball, and the cap of tube to collect energy from human touches. The excellent deformability and durability can greatly broaden the applications of the energy devices for scavenging energy. Such devices can be used not only as wearable and flexible power generators

Fig. 10.3 (continued) Short-circuit current density at different-level twists. (**d**) Left: Image showing that the device drove a load when it was multiply folded. Right: Short-circuit current density at different-times folds. (**e**) Left: Image showing that the device can drive a load and retain its stretchability after experiencing severe tear damages. Right: Short-circuit current density after being cut and stretched. (Reproduced with permission from Wiley [27])

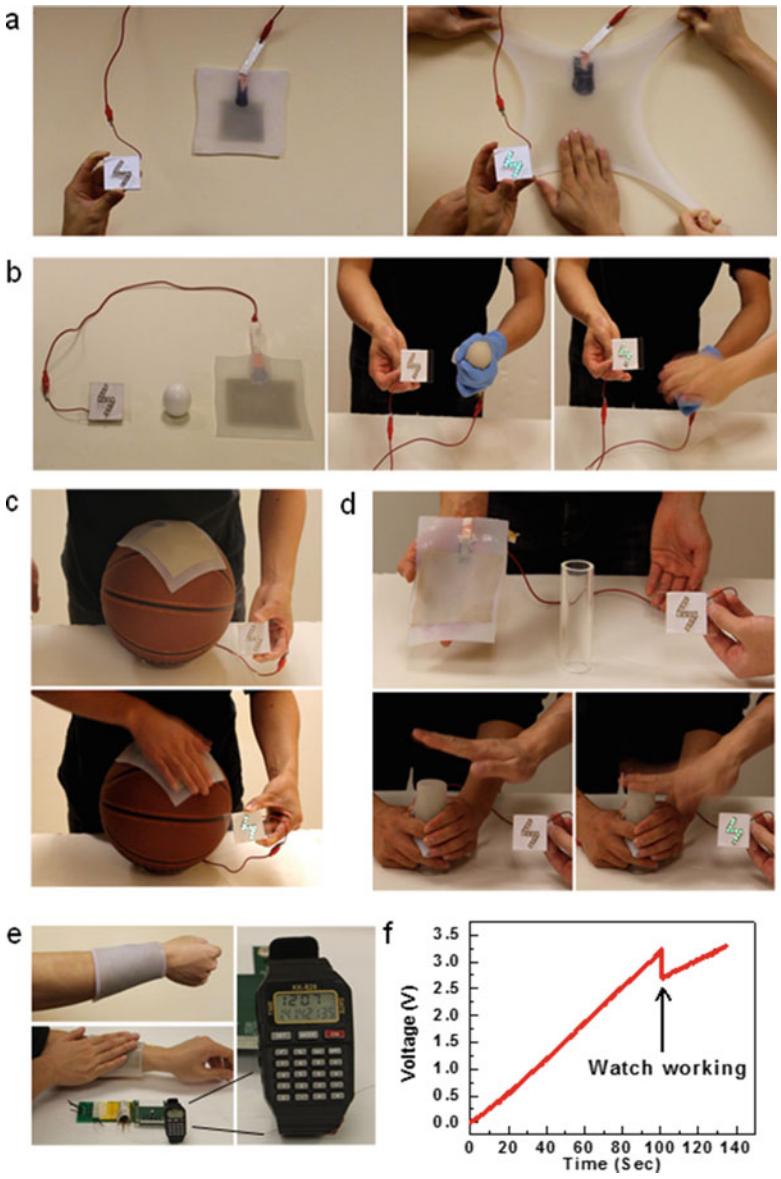

Fig. 10.4 Demonstration of the capability of producing electricity under biaxially stretching and on various nonplanar objects. (**a**) Image showing that the TENG drove a load when it was extremely biaxially stretched. (**b**) Image showing that the TENG drove a load when it fully wrapped a small sphere with a radius of 2 cm. (**c**) Image showing that the TENG drove a load when it conformally attached on a ball. (**d**) Image showing that the device drove a load when it wrapped the cap of a tube. (**e**) Image showing that the TENG worn on the forearm continuously powered a smart watch by hand tapping. (**f**) Charging curve of the capacitor connected with a power management and smart watch by hand tapping. (Reproduced with permission from Wiley [27])

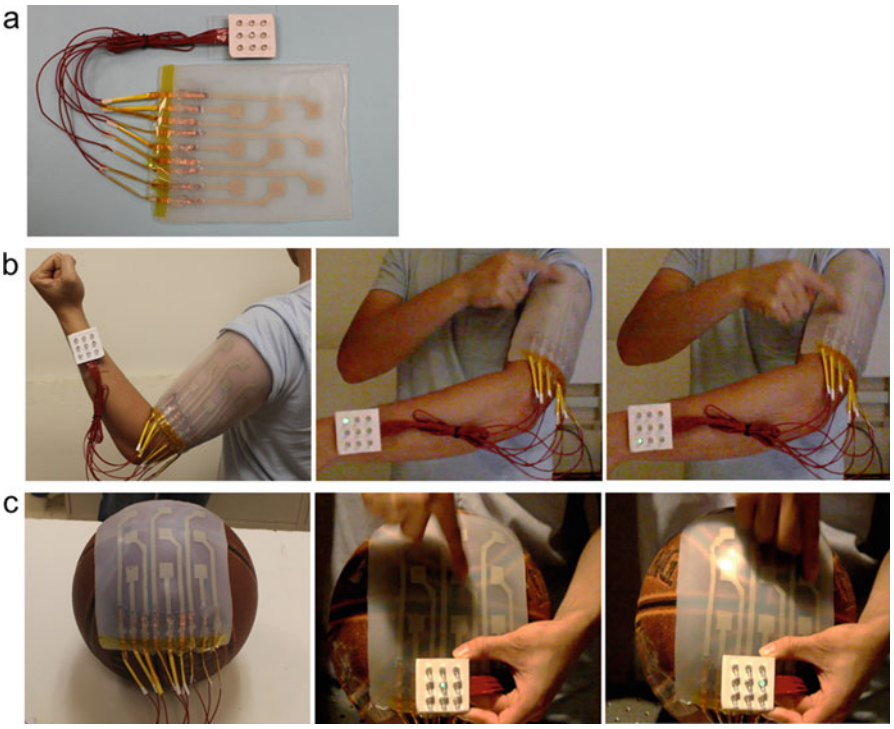

Fig. 10.5 Image of the self-powered and highly conformable tactile sensing system. (**a)** Image of the stretchable self-powered tactile sensing system. There is one-to-one relationship between the LEDs and the TENG units. (**b)** Image demonstrating that the self-powered tactile sensing system conformally contacted on the human arm and the LED lit up corresponded to the e-skin unit that was being touched. (**c)** Image demonstrating that the self-powered tactile sensing system conformally contacted on a ball and the LED lit up located to the unit that is being touched. (Reproduced with permission from Wiley [27])

but also for designing shape-adaptive self-powered tactile sensing system, such as electronic skins. The results illustrate that the conducting nanowires can utilize the stretchable and deformable triboelectric nanogenerators for the uses in the human body and various extremely mechanical conditions.

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Chapter 11
Nanowire-Based Lasers

Wenna Du, Jie Chen, Qing Zhang, and Xinfeng Liu

11.1 Introduction

In 1916, Albert Einstein predicted the existence of stimulated emission in theory, thus providing the underpinnings of lasing action [1]. By expanding the maser techniques to the infrared and optical region, Schawlow and Townes laid the solid foundation [2] for Theodore Maiman to demonstrate the first working laser successfully using a ruby gain material [3]. Till now, lasers have become ubiquitous in science and technology as well as in everyday life. They are vital for signal processing, communication, optical sensing, quantum optics, and metrology and are widely used for biological imaging, local surgery, metal welding, consumer electronics, and so on. From the time of its inception to the present day, there has been intense interest simultaneously in the miniaturization of the laser.

Thereafter, the success and widespread application of semiconductor lasers are mainly because they are much smaller and far cheaper and consume less power than any other kind of laser. One of the dominating areas of research among semiconductor lasers is the semiconductor nanowire laser: a quasi-one-dimensional semiconductor that simultaneously acts as an optical gain medium and optical cavity that, in some cases, possesses the intrinsic capability to lase [4–6]. These properties, along with the ability to tune the lasing wavelength and its possibility for electrical integration, make the semiconductor nanowire laser a promising candidate for use

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in the next generation of optoelectronic devices. They consist of submicron-sized "wires" typically formed from metal oxides, II–VI or III–V semiconductor alloys. Owing to the large difference in refractive index between the semiconductor and the embedding medium (usually free space or a low–refractive index dielectric material), the nanowire acts as both the optical gain medium and the optical cavity, thereby allowing lasing despite the limited volume of gain material. The first working of nanowire laser was observed [7] from ZnO nanowires grown from the "bottom up" on sapphire substrates coated with gold by simply heating a mixture of ZnO and graphite in an argon atmosphere [8]. The bottom-up growth method, which requires fewer post-processing steps than conventional diode lasers, can produce nearly defect-free, single-crystal heterostructures on virtually any kind of substrate, thus tremendously increasing the spatial design parameters. The natural anisotropy and the associated facets of the wurtzite structure of ZnO resulted in the formation of the nanowire optical cavity. Low-threshold operation is expected, owing to the small size of the active region of the semiconductor nanowire laser.

In this chapter, we introduce the concept of the nanowire laser and describe the basic mechanisms of lasing in semiconductor nanowires and most effective materials for nanowire lasers. Then, the wavelength controlling methods in semiconductor nanowire laser are discussed in detail. Improving the performance of the nanowire lasers furthermore, several new nanowire laser cavity structures, especially surface plasmon polariton lasers, are also described. Finally, we review some exciting new reports of electrically pumped nanowire lasers with the potential for integrated optoelectronic applications.

11.2 Nanowire Lasing Mechanisms

The three indispensable elements for nanowire lasers are pump source, gain medium, and optical cavity. The pump can be offered by a light source or a current source, the former of which is more often used for its easier realization while few researches has successfully realized nanowire lasers via electrically pumping. The other two indispensable elements can be satisfied by the nanowire itself due to nanowires' inherent advantages such as big difference of refractive index with its environment, ultrasmooth surface, easily fabricated flat end facet, and high gain merits.

Usually, a single semiconductor nanowire with relatively high refractive index compared with environment is a natural FP cavity and consequently highlighted one key prerequisite for laser cavity design: the sub-wavelength optical confinement of the nanowire geometry. The main component is the FP cavity consisting of a gain medium between two opposite end faces. In the case of nanowires, the gain medium fills the entire cavity, and the opposite end-face reflections are from either parallel- or perpendicular-to-the-nanowire axis (see Fig. 11.1).

Besides, for a nanowire with radius close to or bigger than the semiconductor bandgap wavelength, a WGM cavity can be easily established within the cross-sectional plane of the nanowire. For example, Wiersig [10] reported WGM in

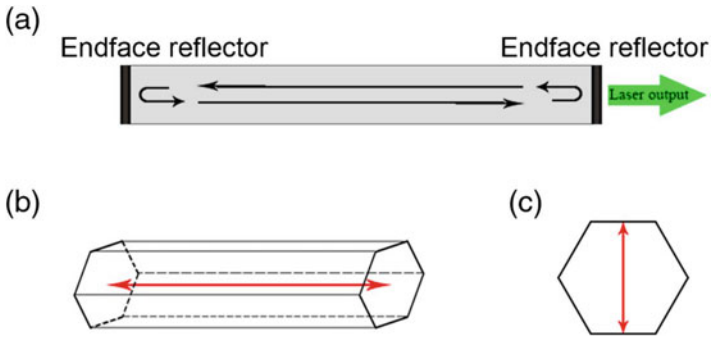

Fig. 11.1 Semiconductor nanowire FP cavity. (**a**) Schematic of an FP cavity laser. (**b**) FP cavity formed by the nanowire's end faces. (**c**) FP cavity formed by the hexagon's end faces parallel to the wire axis. (Reprinted with permission from Ref. [9] Copyright 2006 by the American Chemical Society)

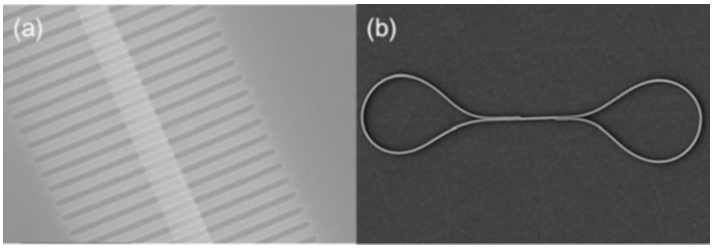

Fig. 11.2 **(a)** Hybrid nanowire–photonic–crystal cavity. (Reprinted with permission from Ref. [11] Copyright 2006 by the American Chemical Society). **(b)** Nanowire loop mirror cavity. (Reprinted with permission from Ref. [12] Copyright 2011 by the American Chemical Society)

hexagonal dielectric cavities. Besides the abovementioned cavities, other geometries of optical cavities have also been fabricated, such as ring cavity, hybrid nanowire–photonic–crystal cavities, or nanowire loop mirror cavities (see Fig. 11.2).

11.2.1 Waveguiding Mechanism

By resolving Maxwell's equations using a similar formalism to an infinite circular waveguide, Ma and Maslov [5, 13] discussed the ability of the nanowire geometry to sustain multiple guided modes, depending on its diameter. Calculating the dispersion curves of the first guided modes (HE_{11}, TE_{01},TM_{01}) yields an estimate of the efficiency of light confinement in such sub-wavelength waveguides as shown in Fig. 11.3. Indeed, these dispersion curves reveal two interesting regimes. The first regime takes place below the cutoff diameter of the first transverse mode (TE_{01} mode), where only the fundamental HE_{11} mode is confined inside the nanowire,

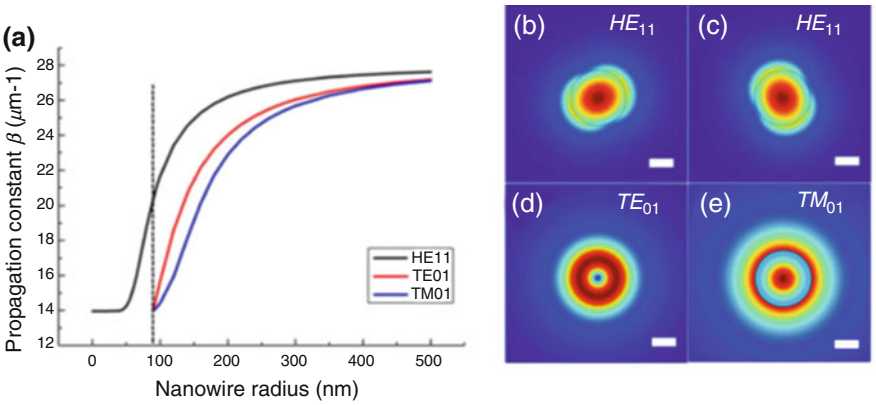

Fig. 11.3 (**a**) Numerical solutions of propagation constant (β) of the HE_{11}, TE_{01}, and TE_{01} modes in an air-clad ZnO nanowire at 450 nm wavelength. Dashed line indicates the single-mode condition for the ZnO nanowire. (**b**)–(**d**) Electric field of the HE_{11}, TE_{01}, and TE_{01} modes in an air-clad ZnO nanowire at 450 nm wavelength with 240 nm diameter. Scale bar, 100 nm. (Reprinted with permission from Ref. [5] Copyright 2013 by the Optical Society of America)

enabling the waveguide to have a single mode along the transverse axis. However, this mode's effective index is not maximized, meaning that the electric field extends considerably outside the nanowire and hence generates significant propagation loss. The second regime occurs above the cutoff frequency of the TE_{01} mode; at higher diameters, several guided modes are strongly confined inside the nanowire, with an effective index asymptotically approaching the semiconductor index, thus reducing the propagation losses of fundamental modes throughout the cavity. However, the presence of several guided modes increases the risk of the device operating in a multimode regime. Moreover, the various electric field distributions of confined modes that overlap with the gain medium will affect the device performance and favor mode competition via gain discrimination.

A simple method to achieve single-mode operation is the reduction of the resonator length, which can be realized by directly cutting the semiconductor nanowire. By this way, the free spectral range will increase to be larger enough to surpass the width of the gain profile and only one longitude mode left in the range finally. In 2012, Li realized a stable, single-mode output as shown in Fig. 11.4a–c, with ~0.12 nm linewidth and > 18 dB side-mode suppression ratio from a 135 nm wide, 4.7 mm long GaN nanowire, which is fabricated by a top-down technique [14]. Numerical simulations indicate that single-mode lasing arises from strong mode competition and narrow gain bandwidth. However, cutting the nanowire to several micrometers will lead to a relatively high threshold for the reduction of gain material and severe loss caused by end-face reflectivity effect [15]. For stable and single-mode lasers with lower lasing threshold and cavity losses, other methods are therefore preferable. One possible route in theory is to fabricate internal mode selection structure, e.g., distributed-Bragg-reflector (DBR) mirrors at the ends of

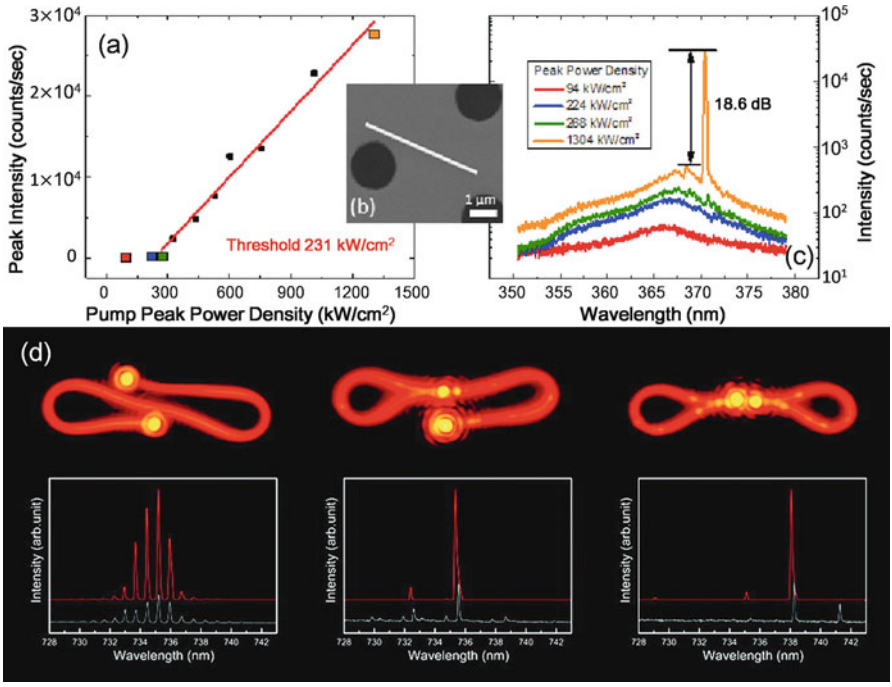

Fig. 11.4 (**a**) Nanowire laser intensity versus pump laser intensity, for nanowires with lengths of 4.7 μm. (**b**) Scanning electron micrographs of the GaN nanowire lasers. (**c**) Photoluminescence spectra from the nanowire lasers under uniform excitation for pump intensities as indicated in the figures. (Reprinted with permission from Ref. [14] Copyright 2012 by the Optical Society of America); (**d**) PL microscope images of lasing cavities and lasing spectra of single-nanowire structures without loop mirror, with one loop mirror, and with double loop mirrors. (Reprinted with permission from Ref. [12] Copyright 2011 by the American Chemical Society)

the nanowires for mode selection [16]. But it is very difficult to fabricate experimentally. Being inspired by the technique adopted on macroscopic lasing devices [17–19], in 2011, Xiao et al. [12] first induced the Vernier effect in the CdSe nanowire laser for fabrication of tunable single-mode nanowire lasers by folding the nanowire to form loop mirrors (see Fig. 11.4d). The Vernier effect will function when two or more cavities coupled together. The output modes must satisfy the oscillation conditions for all the cavities, and thus the number of modes will be greatly decreased. This effect is very attractive for the easiness to couple nanowire cavities and allowing sufficient gain.

It is noted that the waveguiding mechanism sets the nanowire diameter toward that of a single-nanowire laser. Despite the large refractive index difference between the nanowire's core and the surrounding medium (typically air), which favors strong confinement of the electric field, the diameter range for strong confinement of single or multiple guided modes has a minimum value and is scaled by the refractive index

and emission wavelength of the semiconductor. For instance, efficient waveguiding can be achieved for a 100-nm-diameter GaN nanowire emission and a minimum ~165-nm-diameter GaAs nanowire emission at 870 nm [20].

Another key figure of merit for nanowire lasers is the confinement factor Γ of the resonant modes, as a large Γ will favor a low threshold. Γ characterizes the overlap of the lasing mode with the gain medium, which for a nanowire depends strongly on its size and shape as well as on the electric field distribution of the resonant mode. For instance, a large confinement factor ($\Gamma > 0.9$) could be achieved in a single-GaN nanowire cavity with a sufficiently large triangular cross section (cross-sectional size of 300 nm) for the TE01 mode [21]. Robert et al. also presented that producing a large confinement factor is only meaningful when the polarization of the electromagnetic guided mode matches the polarization of the dipole transition of the semiconductor nanowire [22].

As we know, stimulated emission in semiconductors occurs when the Bernard–Duraffourg condition is achieved [23]. The optical susceptibility depends on the joint density of states as well as Fermi-level occupancy probabilities, in quasi-thermal equilibrium. This quasi-thermal equilibrium is necessary for obtaining stimulated emission via strong non-equilibrium carrier densities of electrons and holes. We recall that the density of states depends on the geometry of the structure, which is constant for 2D materials and inversely proportional to the square root of the energy in the case of one-dimensional (1D) nanowires [24]. This leads to Van Hove singularities, where resonant character of the absorption line makes the achievement of strong coupling possible even without formation of a bound state of an electron and a hole. If anything, this should support lasing in 1D nanowires where contrary to the case of conventional exciton polaritons, formation of 1D Van Hove polaritons can be realized in any system with a singularity in the density of states [25]. Under strong pumping condition, the exciton population can be very high, giving rise to the multiexciton interaction processes, such as stimulated emission, Auger recombination, and biexciton recombination. The processes decrease emission lifetime but complete with each other. As Fig. 11.5 shows, as pumping intensity is higher than 28.0 μJ/cm^2, exciton population inversion is reached, leading to amplified spontaneous emission and further lasing processes [26].

11.2.2 Gain and Losses

Amplification in a nanowire Fabry–Pérot cavity relies on the optical feedback from light reflected from the two crystalline end facets of the nanowire and propagated back through the gain medium. Lasing is achieved when the round-trip gain exceeds the round-trip losses [27]:

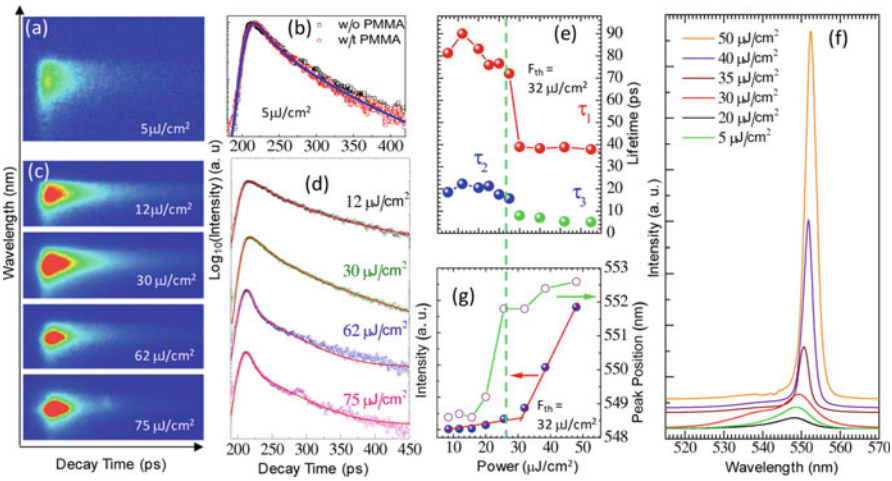

Fig. 11.5 Power-dependent time-resolved PL spectroscopy of single ZnTe nanobelt. Streak camera image (**a**) and time-resolved PL spectra (**b**) of an individual ZnTe nanobelt. Power-dependent streak camera images (**c**) and the corresponding time-resolved PL spectra (**d**) of ZnTe nanobelt. (**e**) The PL lifetimes extracted as a function of power fluence. The green dashed line indicates the threshold of amplified spontaneous emission. (**f**) Power-dependent PL spectra of ZnTe nanobelt. (**g**) Intensity and peak position of PL emission as a function of pumping fluence extracted from (**f**) showing the amplified spontaneous emission. (Reprinted with permission from Ref. [26] Copyright 2012 by the American Chemical Society)

$$\Gamma g > \alpha_{\mathrm{m}} + \alpha_{\mathrm{p}} = \frac{1}{2L} \ln\left(\frac{1}{\mathrm{R}_1 \mathrm{R}_2}\right) + \alpha_{\mathrm{p}} \tag{11.1}$$

where Γ is the confinement factor, i.e., the fraction of the mode intensity confined within the nanowire; g is the material gain; α_{m} is the mirror loss; α_{p} is the propagation loss by absorption or scattering, etc.; L is the cavity length; and R_1 and R_2 are the effective reflection coefficients for each end facet, which are nominally equal. As a result, increasing the gain efficiency or suppressing the round-trip loss may achieve lower threshold.

It has been suggested theoretically that the confinement factors for nanowire lasers are very large in comparison to those for heterostructure lasers and can even exceed unity [13]. The property of large confinement factors has been related to the strongly waveguiding nature of the nanowire, in which the actual length of wave propagation may exceed the axial length of the nanowire [28]. A larger-than-unity confinement factor suggests that modal gain (i.e., amplification specific to a given mode), in addition to material gain, may have a role in allowing a nanowire laser to reach the lasing threshold. In practice, this may aid nanowire lasers in achieving lasing, which would not be possible for different cavity geometry.

One way to increase gain efficiency is decreasing the temperature to dozens of kelvins to induce excitonic recombination [29, 30]. This kind of recombination, to

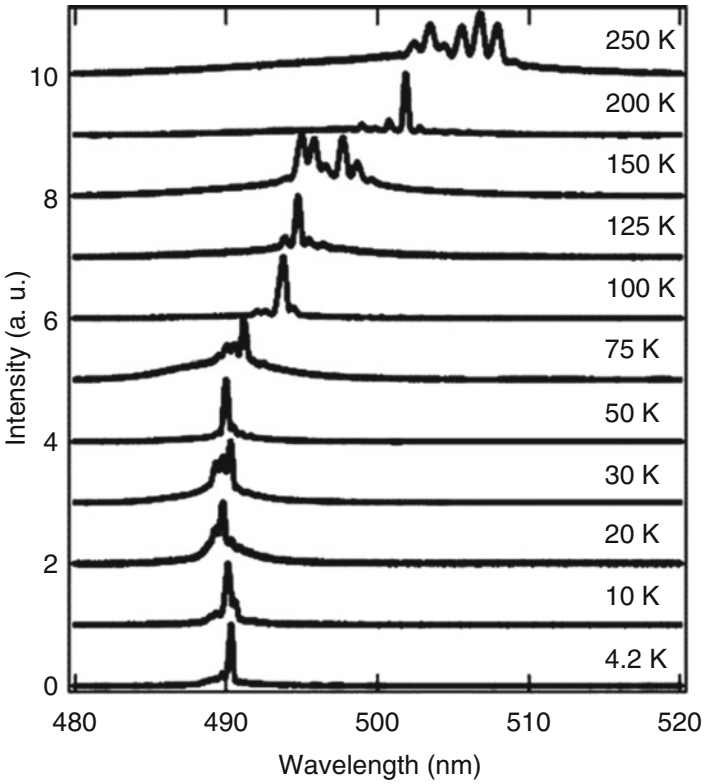

Fig. 11.6 Temperature-dependent spectra recorded from a single CdS nanowire above the threshold for lasing. The temperature values are given next to each spectrum. The excitation power ranges from 0.24 μJ/cm^2 at 4.2 K to 3.3 μJ/cm^2 at 250 K. (Reprinted with permission from Ref. [26] Copyright 2005 by the American Chemical Society)

some extent, can avoid collision between electrons or holes with the lattice and thus more energy can be transferred to photons. In 2005, Agarwal investigated temperature-dependent PL/laser from the single cadmium sulfide (CdS) nanowire cavities [31]. As Fig. 11.6 shows, an exciton−exciton interaction was critical to lasing up to 75 K, while an exciton−phonon process dominates at higher temperatures. Below 75 K, a laser peak at 490.5 nm caused by exciton–exciton scattering was achieved, with a low threshold only at 240 nJ/cm^2.

To assess the losses due to photonic behaviors in the nanowire, we must consider the size of the whole nanowire cavity in the FP regime. First, the growth mechanism causes the nanowire to either lie on a substrate (horizontal geometry) or stand vertically for surface emission (vertical geometry). The interaction with the substrate in both cases induces severe optical losses, which considerably degrade the Q factor

and/or the absolute reflection coefficient at the nanowire–substrate interface. For vertical geometry, optical feedback can be reinforced for sufficiently large nanowire diameters with the appearance of high-order whispering gallerylike cavity modes, allowing stimulated emission for III–V (InGaAs) nanopillar on silicon [32]. A proposed alternative design is to insert a thin metallic layer between the substrate and the nanowire to increase the confinement factor Γ; this part will be detailed later.

Given the gain efficiency and pump technique, suppressing optical loss α, i.e., improving the cavity quality, can naturally decrease threshold for lasers. Compared with their bulk counterparts, the reflecting loss at semiconductor nanowires' end face is more severe because of strong end-face diffraction. Consequently, the Q factor, which is often used to evaluate the quality of cavity, is limited to below 1000 [27, 34–37]. To reach the laser threshold, the relatively low Q factor (< 100) of the nanowire cavities requires the material gain to compensate for the cavity losses. Similarly, we must also mention that the inherent longitudinal multimode regime of the FP resonator, owing to the combination of cavity length and the rather broad linewidth of the nanowire emission profile at room temperature, is also detrimental to achieving efficient gain in nanowire lasers. One method to improve the Q factor is to manipulate the nanowire into ring geometry. Another method is to combine the nanowires with high-quality passive cavity, for example, embedding semiconductor nanowires into photonic crystal or hybridizing them with resonator. In 2006, Barrelet et al. combines chemically synthesized freestanding CdS nanowire emitter with lithographically defined 1D photonic crystal and racetrack micro-resonator structure [11] (see Fig. 11.7a, b). In his fabrication, localized emission and amplified spontaneous emission (ASE) at 4 K were successfully observed. Furthermore, Zhang in 2008 simulated a nano-cavity with ultrahigh Q factor via embedding a semiconductor nanowire in 1D photonic crystal [33] as shown in Fig. 11.7c–e. By defining 1D photonic crystal at the nanowire ends and engineering the microcavity pattern, the reflection on its end face could be improved by 20-folds, and a Q factor up to 3×10^5 was designed.

As the study of single-nanowire lasers matures, it becomes increasingly important to rigorously model the nanowire laser. Modeling helps define the lasing threshold, which can be thought of as the amount of excitation necessary to turn the laser "on." Specifically, modeling the transition from amplified spontaneous emission (ASE) to lasing oscillation enables a closer examination of the threshold behavior. When the spontaneous emission factor is large, as in the case of micro- and nanolasers, the definition of the lasing threshold becomes not consistent [39]. This lasing threshold is generally determined from a power plot describing the relationship between the input excitation and the output emission. For a nanoscale laser, the lasing threshold is less distinguished because the fraction of spontaneous emission coupled into a lasing mode becomes quite large. Rate equation analysis to model this relationship helps to define the lasing threshold of nanowire lasers. The coupled rate equations to describe the carrier density and photon density for a single mode in a semiconductor cavity can be defined as [38]

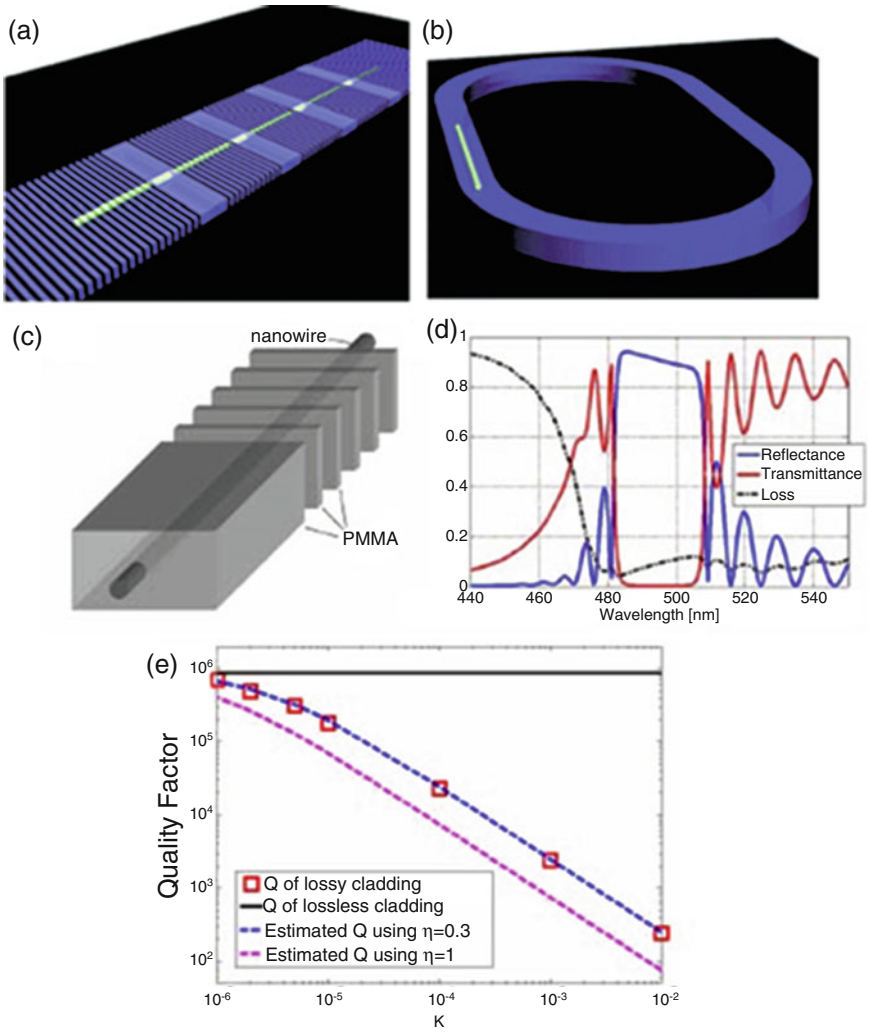

Fig. 11.7 Nanowire photonic crystal (**a**) and micro-resonator (**b**) (Reprinted with permission from Ref. [11] Copyright 2006 by the American Chemical Society). (**c**) Schematic of a semiconductor nanowire with 1D photonic crystal defined at its end. (**d**) Transmittance and reflectance spectra for nanowire with photonic crystal consisting of 30 PMMA/air pairs. (**e**) Quality factor (red square) as a function of imaginary part of refractive index (κ). The Q value with lossless cladding is indicated in black line. The dash lines represent estimation of Q using $\eta = 0.3$ (blue) and 1 (magenta), respectively. (Reprinted with permission from Ref. [33] Copyright 2008 by the Optical Society of America) (Color figure online)

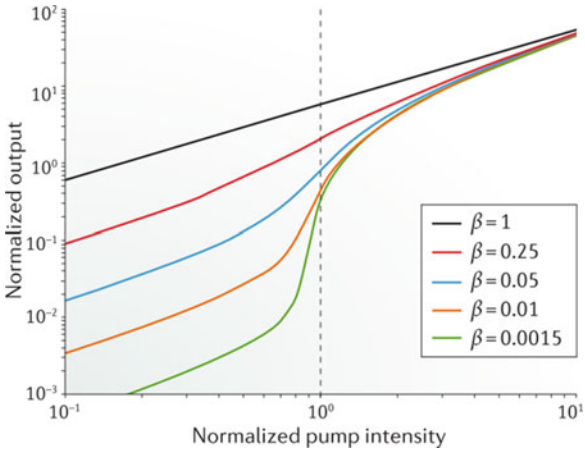

Fig. 11.8 Calculated power plot of a hypothetical GaN laser with different values of β. (Reprinted with permission from Ref. [38] Copyright 2016 by the Macmillan Publishers Limited)

$$\frac{dN}{dt} = \eta P - \frac{N}{\tau_r} - \frac{N}{\tau_{nr}} - \Gamma v_g \alpha (N - N_0) S \tag{11.2}$$

$$\frac{dS}{dt} = \beta \frac{N}{\tau_r} + \Gamma v_g \alpha (N - N_0) S - \frac{1}{\tau_s} S \tag{11.3}$$

where N is the carrier density; S is the photon density; P is the pump intensity; η is the pumping efficiency; τ_r and τ_{nr} are the spontaneous emission and non-radiative lifetime, respectively; τ_s is the photon lifetime; β is the spontaneous emission factor; N_0 is the transparency carrier density; α is the differential gain; Γ is the confinement factor; and ν_g is the group velocity. The gain is approximated in the linear regime by Eq. 11.4:

$$g = \alpha (N - N_0) \tag{11.4}$$

By solving for these coupled rate equations under steady-state conditions, the photon density can be plotted as a function of pump intensity (see Fig. 11.8). The value of β is the fraction of spontaneous emission coupled into the laser mode of interest. A high β-value is crucial for applications, because it improves the nanowire laser emission efficiency and is also necessary for nanowire lasers with high modulation frequency [40]. By fitting the experimental power plot to a calculated plot, the lasing threshold can be more quantitatively defined. Quantum-optical (quantum-mechanical active medium and radiation field) theory of nanoscale lasers suggested that, even without a distinct threshold in the input versus output plot, it may be possible to determine a finite threshold.

To summarize, even though a nanowire laser appears to be an ideal nanosized laser, in practice, it is not as efficient as desired in current technology. Defects, surface states, multimode lasing, poor end-facet reflectivities, mode overlapping, and mode competition are many aspects that still must be addressed for improved device

efficiency. Much work remains to be done to unlock the full potential of semiconductor nanowire lasers.

11.3 Materials for Nanowire Lasers

Since the first demonstration of the bottom-up synthesis of semiconductor nanowires with high optical quality, it made possible to prepare new semiconductor materials suitable for nanowire lasers. This is particularly important for traditional semiconductors, such as ZnO and CdS. The use of relatively simple tube furnaces to grow nanowires of high crystalline quality is attractive for the initial exploration of new materials. The development of nanowire lasers made from GaN also represents the first extension of the single-nanowire laser to new material systems beyond ZnO [37]. One year later, the first example of lasing from a core–shell heterostructure that consisted of a GaN core with an epitaxial shell of $Al_{0.75}Ga_{0.25}N$ was demonstrated [41]. Since these early studies, the library of nanowire laser materials has expanded enormously with emission wavelengths ranging from 370 to 2200 nm, resulting in nanolasers that emit in the ultraviolet (UV), visible, and near-infrared regions. This wide range in emission wavelengths can be seen in demonstrations for II–VI and III–V semiconductors and metal oxides, such as ZnO (REFS [7, 37, 42]), CdS (Ref. [11, 26, 31]), CdSe (Ref. [12, 43]), CdSSe (Ref. [44]), ZnS (Ref. [45]), GaN (REFS [14, 20, 21, 38, 46, 47]), InGaN (Ref. [48]), GaAs (Ref. [20, 49]), InGaAs (Ref. [32]), AlGaAs (Ref. [50]), GaSb (Ref. [51]), and InP (REFS [52, 53]). Stimulated emission due to two- and three-photon absorption with a high threshold of 100 mJ/cm^2 was reported in ZnO nanowires [42]. Zhang et al. further studied lasing performance of ZnO nanowires and demonstrated a lower threshold of 160 μJ/cm^2 from two-photon absorption of ZnO nanowires pumped with a femtosecond pulse excitation at 700 nm [54]. Following these pioneering works, II–VI compounds became the focus of investigation, and Lieber's group at Harvard University first studied the lasing properties of CdS nanowires and the effect of temperature on the lasing threshold [55]. Stimulated emission in III–V compound nanowires was first reported in GaSb with lasing emission around telecommunication wavelengths (1570 nm) [51]. Chin et al. from the NASA Ames Research Center were the first to demonstrate low-temperature lasing emission of a III–V nanowire in the near-infrared range, with $I_{th} = 50$ μJ/cm^2 (see Fig. 11.9).

Recently, methyl ammonium lead halide perovskites were identified as a promising gain material for application in various optoelectronic systems [56–60]. These inorganic–organic hybrid materials exhibit high absorption cross sections, efficient photoluminescence, long diffusion lengths, and low trap-state densities [56]. Initial reports of ASE in hybrid perovskite thin films indicated that methyl ammonium lead iodide ($MAPbI_3$) has high material gain with a low ASE threshold [58]. Recently, lasing in a perovskite nanowire cavity was reported for the first time, with the crucial breakthrough being the synthesis of nanowires with high optical quality and suitable dimensions [61]. Although they exhibit excellent

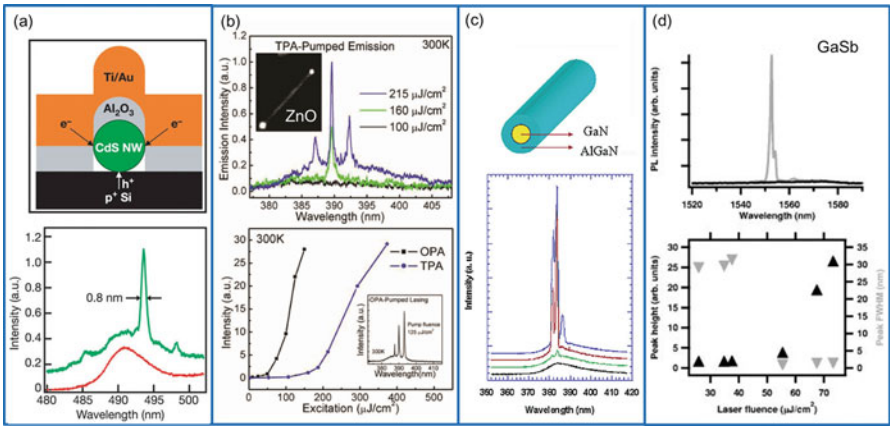

Fig. 11.9 (**a**) Schematic showing the cross section of the device structure. Emission spectra from a CdS nanowire device with injection currents of 200 μA (red) and 280 μA (green) recorded at 8 K. (Reprinted with permission from Ref. [55] Copyright 2003 by the Macmillan Publishers Limited). (**b**) Two-photon pumped emission spectra for difference excitation fluence and integrated emission intensity from ZnO nanowires pumped by single-photon and two-photon processes versus excitation fluence. The inset shows the one-photon pumped lasing spectrum of ZnO nanowires. (Reprinted with permission from Ref. [54] Copyright 2009 by the Optical Society of America). (**c**) Schematic of the GaN/AlGaN core−sheath nanostructures, PL, and lasing spectra of individual nanowires excited by different power densities. (Reprinted with permission from Ref. [41] Copyright 2003 by the American Chemical Society). (**d**) GaSb nanowire NIR lasing and peak PL height at the lasing line wavelength of 1553 nm (black, up triangles) and PL width (gray, down triangles) vs laser fluence. (Reprinted with permission from Ref. [51] Copyright 2006 by the American Institute of Physics) (Color figure online)

performance, hybrid perovskite nanowires are well known for their intrinsic instability [62, 63]. Alternatively, the organic cation can be abandoned altogether, because cation replacement with cesium has opened up a new route to highly luminescent, stable materials [64]. The all-inorganic perovskite nanowires were found to be ultrastable under lasing conditions, continuing to lase even after 10^9 excitation cycles [65]. Mild growth conditions, excellent performance, and constantly increasing stability make perovskite-based nanowire lasers a promising material for the future.

11.4 Wavelength Tunability in Nanowire Lasers

For future nanolaser applications such as optical communication, environmental monitoring, and spectroscopy analysis, two key features must be considered: broadband emission and wavelength tunability. Different methods have been used to achieve tunability. Discrete color tunability can be achieved by using different gain materials, with the ultimate goal of achieving continuous wavelength tunability

to tailor emission to a specific application. Another approach to tune the wavelength is by modifying the dielectric environment of the cavity via the excitation intensity [37], cavity length [66], substrate properties [67], or cavity design [12, 68]. A simple route is changing the geometry of nanowire cavity depending on the FP cavity theory. As a kind of FP lasers, the wavelength of nanowire lasers must satisfy the stand-wave condition, that is, $m\lambda = 2$ nL, where n is the refractive index, L is the length, and m is an integer. Therefore, wavelength tuning can be realized by modulating the optical length nL. Some physical mechanisms including absorption-emission-absorption process and Burstein–Moss effect have been utilized to tailor wavelength on a single nanowire with fixed composition. Li et al. achieved wide tuning of non-doped CdSe nanowire emission by shifting the pump spot position along the nanowire or by gradually cutting the NW shorter [66]. This tuned the lasing wavelength from 706 to 746 nm upon self-absorption of higher-energy photons by the nanowire and subsequent reemission of lower-energy photons, causing the emission wavelength to redshift. This method was also realized in CdS nanowires, where the lasing modes themselves could be similarly tailored [69].They demonstrated an optical self-feedback mechanism based on the intrinsic self-absorption of the gain media to achieve low loss, room-temperature nanowire lasing with a mode selectivity over 30 nm. The CdS nanowire lasing wavelength was continuously tunable from 489 to 520 nm as the length of the nanowires increased from 4 to 25 um, as shown in Fig. 11.10. However, this strategy can only be applied for a limited wavelength range and can be impractical to implement in some cases.

Here, we focus our discussion on tuning the composition of the gain medium for controlling the emission wavelength. Synthesizing ternary or quaternary alloy nanowires with different stoichiometry ratios have been proved effectively to achieve nanowires with different bandgaps. The first is based on spatially graded alloy composition through careful control of the temperature gradient along the growth substrate. Compositional tunability in CdS_xSe_{1-x} nanowires on the same chip was demonstrated in 2005 [44]. These nanowire arrays exhibited chip position-dependent emission ranging from 498 to 692 nm depending on the composition (see Fig. 11.11a). In the same year, Liu et al. demonstrated a wavelength-controlled nanowire laser with $Zn_xCd_{1-x}S$ single-crystal nanoribbons [70]. The lasing emission of 485–515 nm and 340–390 nm was realized by combining laser ablation with thermal evaporation. These results suggest that $Zn_xCd_{1-x}S$ nanoribbon lasers of preselected "tunable" wavelengths between 340 and 515 nm may be achievable by tailoring the composition x. In addition, a composition gradient in the source material was also exploited to grow $In_xGa_{1-x}N$ alloy nanowires [71]. Multi-quantum-well core/shell nanowires were reported based on epitaxially growing highly uniform $(InGaN/GaN)_n$ outside triangular GaN nanowire cores [48]. PL spectra from nanowires with different In compositions have peak at different wavelengths. When the pump intensity reaches threshold, lasing operation occurs, and a redshift happens to the lasing wavelength with an increase in composition (Fig. 11.11c). The demonstrations of alloy composition control through a temperature gradient [44] and elemental gradient [70] enabled the growth of $Zn_xCd_xS_ySe_{1-y}$

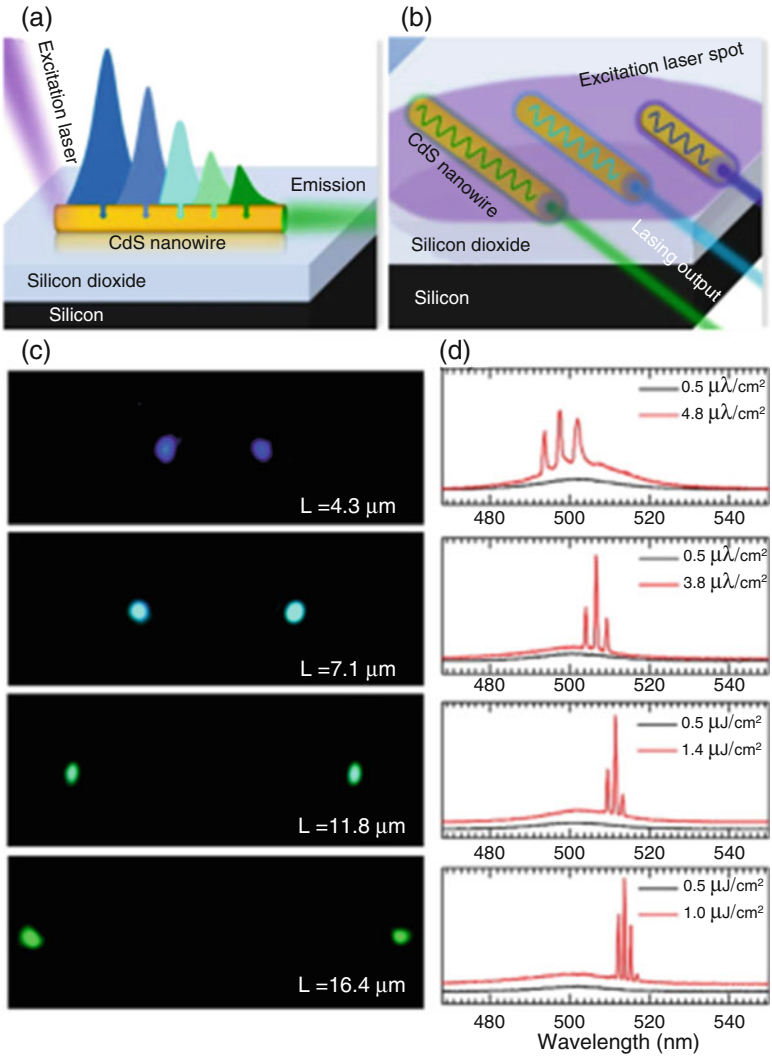

Fig. 11.10 (**a**, **b**) Schematics the length-dependent lasing mode selections for CdS nanowires. When excited with laser pulses at one end (left end), the exciton–polaritons propagate inside the NWs and undergo scattering by the surface defects/phonons and subsequently self-absorption at the Urbach tail. Various output lasing colors are observed at the end facets of CdS NWs. (**c**, **d**) Optical images of four individual CdS NWs with different lengths undergoing lasing and the corresponding emission spectra. (Reprinted with permission from Ref. [69] Copyright 2013 by the American Chemical Society)

in its full composition range from ZnS to CdSe on a single substrate with emission spanning the full visible spectrum [72].

In addition, tuning the composition of the nanowires by changing the ratio of the halide salts in the growth sources enabled lasing across the visible and near-infrared

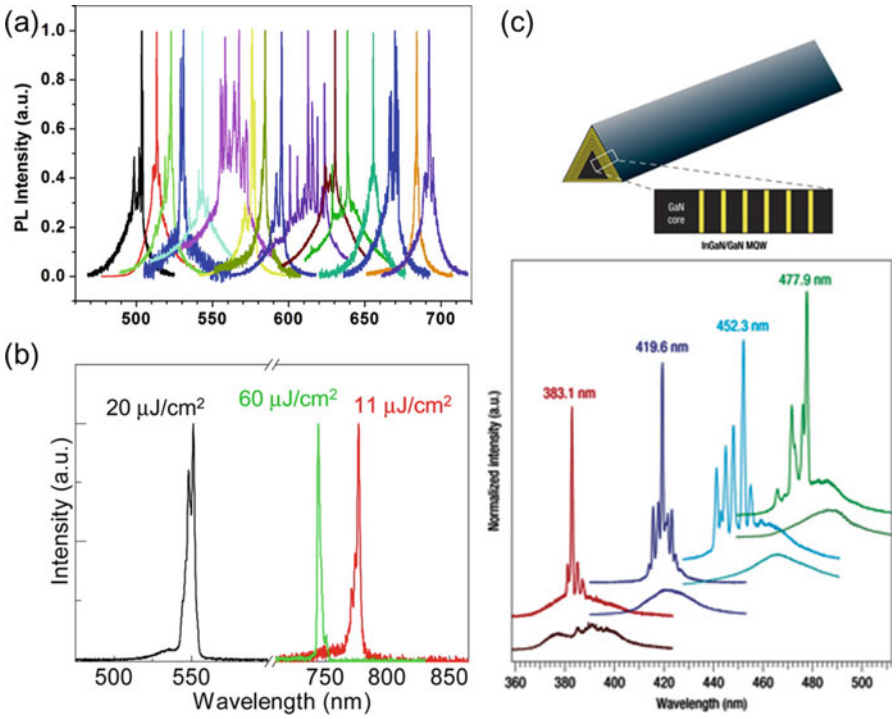

Fig. 11.11 (**a**) CdS_xSe_{1-x} nanowires micro-PL collected at various locations along the substrate maintained at 77 K under high optical pumping condition showing lasing or multimode lasing. (Reprinted with permission from Ref. [44] Copyright 2009 by the American Chemical Society). (**b**) Lasing spectra of ($CH_3NH_3PbI_xCl_{3-x}$) and ($CH_3NH_3PbBr_3$). (Reprinted with permission from Ref. [58] Copyright 2015 by the American Chemical Society). (**c**) Schematic diagram of an InGaN/GaN MQW structure and normalized photoluminescence spectra collected from four representative 26MQW nanowire structures with increasing In composition pumped at different pumping powers. (Reprinted with permission from Ref. [48] Copyright 2008 by the Macmillan Publishers Limited)

spectrum [58, 61]. Xing and Liu et al. have realized room-temperature visible and near-infrared solid-state perovskite nanowire lasers. The lasing wavelength can be tuned from 777 to 744 nm ($CH_3NH_3PbI_xCl_{3-x}$) and then 551 nm ($CH_3NH_3PbBr_3$). Through precisely tuning the component ratio between Br and Cl (I) in $CH_3NH_3PbBr_xCl_{3-x}$ or $CH_3NH_3PbI_xBr_{3-x}$, fine-tuning of the lasing wavelength can be fulfilled (Fig. 11.11b).

11.5 New Nanowire Laser Cavity Structures

The physical manipulation of flexible nanowires provides a method for generating cavities of arbitrary geometry with improved performance. One example is the ring-resonator nanowire laser with higher Q factor. Ring resonators are typically formed by bending a pre-existing nanowire into a continuous loop. If the overlapping nanowire sections are sufficiently coupled to allow for recirculation of light around the loop, optical feedback is increased in the system, thereby lowering the lasing threshold. The first example of a nanowire ring resonator was made from GaN in 2006, which was manipulated into a loop with the two ends side by side [68]. Cavity modes were observed in the spontaneous emission and lasing spectra, indicating the formation of a circular resonator. The Q factor increased to 1300 approximately an order of magnitude larger than what is predicted for freestanding wires. Later, Ma et al. fabricated a pigtailed nanoribbon ring laser constructed with a 600 nm wide and 330 nm thick CdS nanoribbon [73] in 2010 (see Fig. 11.12). When the ring was pumped by a supercontinuum source, multi-longitudinal mode laser emission was observed around 523.5 nm with full widths at half maximum of 0.27 nm, corresponding to a Q factor of about 1900.

Alternative cavity geometries have also been explored to improve nanowire laser performance. Single-mode lasing is highly desirable for applications in sensing, optical communications, spectroscopy, and interferometry. One alternative strategy relies on the formation of a cleaved-coupled cavity [46]. By cleaving a nanowire at a determined point, all but a single lasing mode may be suppressed by modulating the loss at the air gap. Successful device fabrication relies on calculations of both the gap position and the size of each cavity to modulate the lasing threshold of all the longitudinal modes. This process was recently shown for a GaN nanowire that was cleaved using focused ion-beam milling. Another strategy to achieve single-mode lasing relies on the use of "loop mirrors," in which the nanowire is bent into a loop, resulting in both high effective reflectivity and a shortened cavity path length [12]. By bending a CdSe nanowire to include zero, one or two loop mirrors, a threefold decrease in the lasing threshold and near single-mode lasing were observed. Emission occurred at 738 nm with a linewidth of only 0.12 nm and a threshold of 34.4 μJ/cm^2.

In 2008, Yang Q et al. coupled several ZnO nanowires with a silica microfiber knot cavity just by attaching them together through the Van der Waals force [74]. This hybrid structure combines advantages of high gain of nanowires and high-quality factor of microfiber knot cavities. By pumping the nanowires with a 355 nm wavelength laser pulses, Q factor up to 10^4 and a threshold lower than 0.2 mJ/pulse were successfully achieved. This design offers convenient and efficient approach to both pumping and collection of the nanowire lasers and has shown big potential for optical integration in the future. By substituting the microfiber knot to a high-Q silica microdisk cavity, the threshold can be further decreased [75].

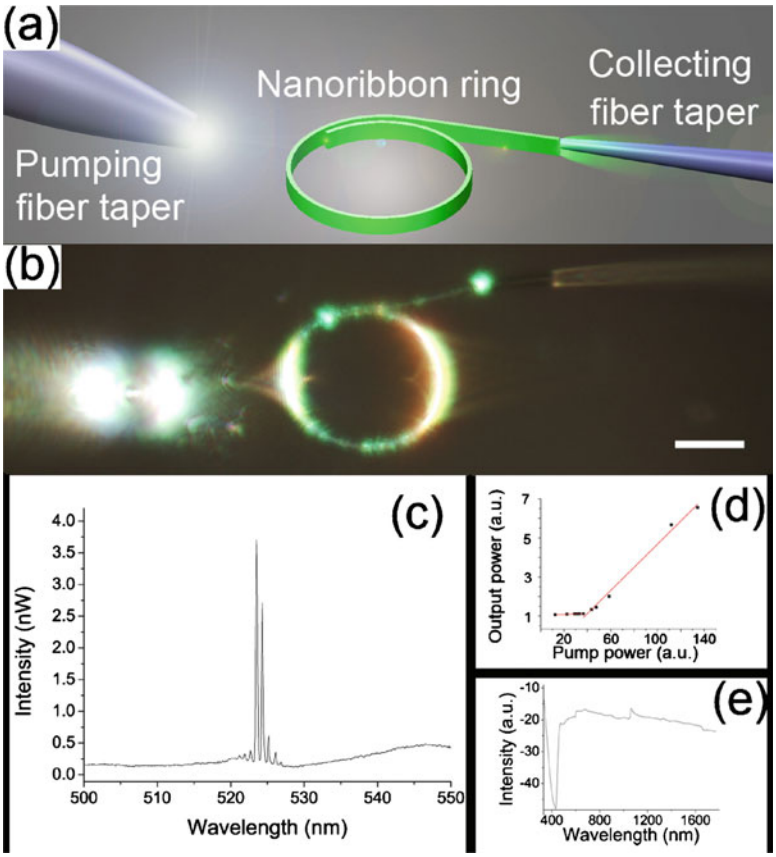

Fig. 11.12 Pigtailed CdS nanoribbon ring laser. (**a**) Schematic of the structure of the nanoribbon ring laser system. (**b**) Optical micrographs of a 20 μm diameter CdS nanoribbon ring under pumping; scale bar, 10 μm. (**c**) Collected lasing spectra of the nanoribbon ring. (**d**) Integrated emission power versus pump energy of the nanoribbon ring laser. (**e**) Spectrum of the pumping light from the supercontinuum source. (Reprinted with permission from Ref. [73] Copyright 2010 by the AIP Publishing LLC)

Meantime, by combining the bandgap engineering and cavity parameters, Liu et al. [76] demonstrated lasing emission between red and green colors separated by 107 nm in wavelength simultaneously in a single bandgap-graded CdS_xSe_{1-x} nanowire (see Fig. 11.13). By looping the wide-gap end of the alloy nanowire through nanoscale manipulation, two relatively isolated cavities were formed, providing lasing oscillations at two different wavelengths. The total output color can be continuously tuned by changing the relative pumping powers of the two cavities.

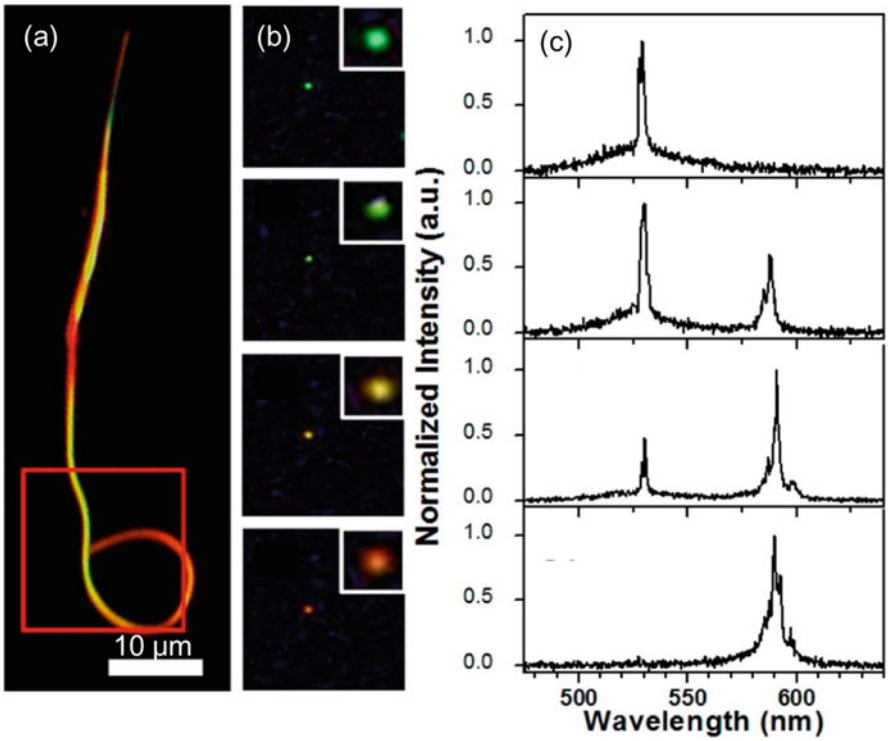

Fig. 11.13 Color control of a looped CdS_xSe_{1-x} wire dual-color laser. (**a**) Dark-field image of the looped nanowire. (**b**) Real-color images of the lasing under different pumping for the two cavities taken from the red box in (**a**). (**c**) Normalized lasing spectra under different controlled pumping intensities. (Reprinted with permission from Ref. [76] Copyright 2013 by the American Chemical Society) (Color figure online)

11.6 Surface Plasmon Polariton Lasers

The miniaturization of semiconductor nanowire lasers is limited by the diffraction limit, which is approximately half of the optical wavelength in the medium. In general, reducing the diameter of the nanowire leads to poor optical confinement and small modal gain, which make photonic lasing impossible. However, nanowires can be used as platforms for creating a new type of laser based on surface plasmon polaritons (SPPs) [77, 78]. SPP waves, which are the collective oscillations of conduction electrons on the surface of a metal, lead to enhanced electromagnetic fields confined at sub-wavelength nanoscale, which allows the laser cavity to store and guide optical energy far below the optical diffraction limit. The strategy of applying a silver coating to a nanowire laser to harness SPPs for lasing and to reduce the overall size of the laser structure was first studied theoretically [79] in 2007. This study suggested the existence of wavelength regions in which the nanowire optical

gain could exceed the metal loss—the process of optical energy absorption and dissipation via electron scattering and thermalization in a metal—to achieve an overall positive gain.

Early theoretical work predicted that a dielectric–metal hybrid structure could be a successful platform for lasing [80]. This was followed by the first report of SPP nanowire lasing in a horizontal CdS nanowire on a silver substrate, separated by a nanoscale film of MgF_2 that provides control over optical confinement, insulates the wire from the metal, and provides a transverse hybrid cavity [81]. Through optical pumping, characteristic signatures of lasing were observed that indicated that the plasmonic nanowires were operating in Fabry–Pérot geometry.

Meantime, combining semiconductor nanowire with metal structures to generate SPP can be a possible route to increase the confinement factor Γ by leading to larger overlap between the mode and the gain material. SPP may also increase the lasers' tolerance to low cavity quality. Noticeably, for the practical realization of low-threshold lasing operation based on SPP, ohmic loss accompanying with it should be effectively suppressed. In 2008, a creative approach hybridizing dielectric waveguiding with plasmonics has been proposed [80]. In 2012, Yu et al. demonstrated a semiconductor nanowire laser with ultralow threshold which can be reached by CW pump at low temperature [82]. The semiconductor nanowire used in his design is a GaN nanorod partially filled with InGaN as gain medium and separated by a 5 nm silicon dioxide (SiO_2) spacer from an atomically smooth epitaxial silver film to avoid unnecessary SPP scattering. The SPPs excited in noble metal structure adjacent to gain media have dramatically reduced the optical mode volume and thus improve the overlap between mode and gain medium. Laser action has been achieved even under CW pump (405 nm). By locating triangular GaN nanowire on Al film with a spacer layer of SiO_2, Zhang et al. [83] demonstrated the first strong room-temperature UV (~370 nm) plasmonic laser with an extremely low threshold (~3.5 MW/cm^{-2}). In the plasmonic devices, the ohmic losses and scattering/radiation losses are efficiently suppressed through reducing the surface roughness of the metal and SiO_2; meanwhile, the gain compensation is greatly enhanced because of the flat metal–insulator–semiconductor interface.

Furthermore, SPs have proved their capability to manipulate the nanowire cavity mode and further the lasing wavelength. As shown in Fig. 11.14a, Zhang et al. demonstrated that an Ag NP in the vicinity of a CdS nanowire can simultaneously modulate the effective cavity length, equivalent phase shift, and the Q factor of the cavity modes [84]. Ag NP acts as a reflective and half-reflective nanomirror when it is located at the end and at the side of the CdS nanowire cavity, respectively. When the CdS nanowire is sitting on Au film with insulator SiO_2 thin layer as spacer, the Burstein–Moss effect inside the CdS nanowires can be enhanced by the extremely confined electric field in the nanometer-thick insulator layer. The hybrid semiconductor–insulator–metal structures are well-known to support the low-loss SPP. The enhanced Burstein–Moss effect leads to a larger blueshift of the output photonic lasing wavelength of the CdS nanowires. The enhancement factor increases with the decrease of the SiO_2 thickness as a result of the increase of localized electric field and exciton–plasmon interaction strength. Through varying the thickness of

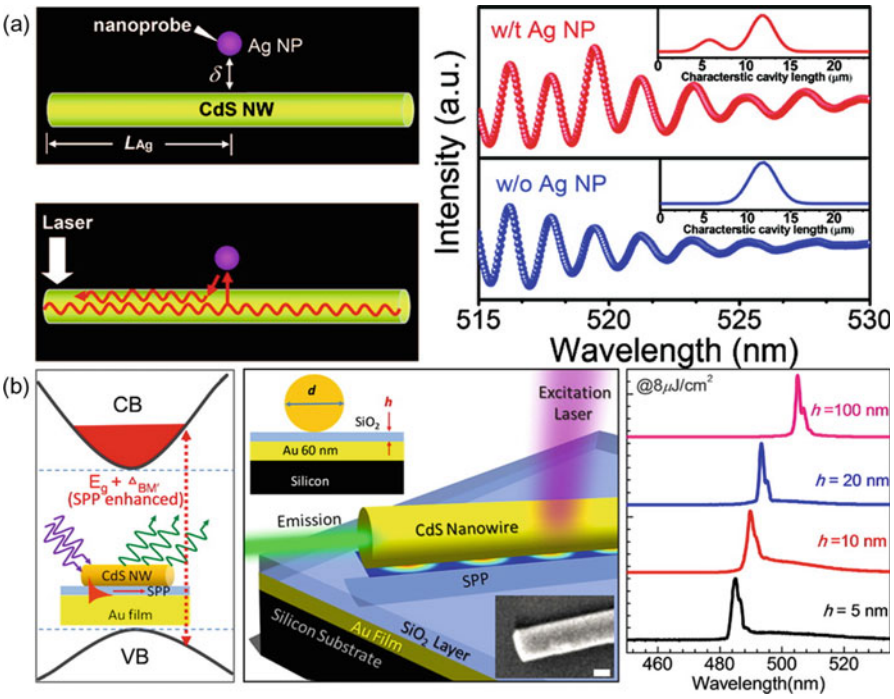

Fig. 11.14 Localized surface plasmon and surface plasmon polariton-modulated cavity modes of CdS nanowire cavity. (**a**) Schematic illustration of the CdS NW–Ag NP hybrid microcavity fabricated with a nanoprobe and modulations of PL Fabry–Pérot oscillation in the CdS NW by an Ag NP located nearby the side surface of the NW and normalized PL spectra at the right end of the NW in the presence or absence of Ag NP when a focused 488 nm laser is illuminated at the middle part of the NW. (Reprinted with permission from Ref. [84] Copyright 2011 by the American Chemical Society). (**b**) The enhanced Burstein–Moss effect and the observation of strong Purcell effect with the presence of the localized electric. The lasing peaks of four devices are blueshift as a consequence. (Reprinted with permission from Ref. [67] Copyright 2013 by the American Chemical Society)

SiO_2 from 100 to 5 nm, the lasing wavelength was tuned from 504 to 483 nm. Tunability of ~30 nm was obtained [67] (see Fig. 11.14b).

11.7 Electrical Excitation of Nanowire Lasers

The nanowire lasers discussed thus far are excited optically by another laser that is orders of magnitude larger. Optical excitation is unsuitable for most of the intended nanowire laser applications, especially in the area of on-chip integrated photonics. The ultimate goal for semiconductor nanowire lasing hinges on achieving reliable lasing through the electrical injection of electrons and holes into a dielectric–metal

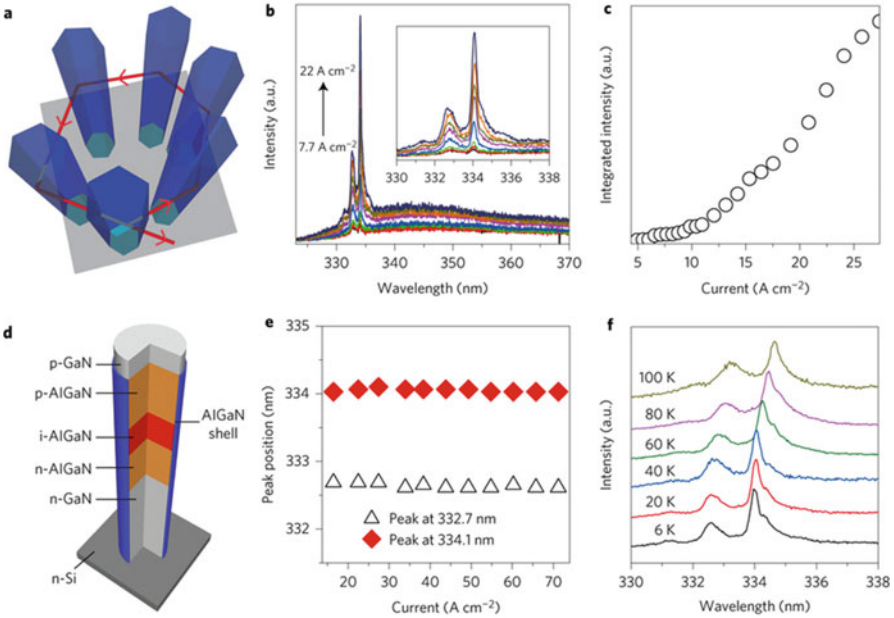

Fig. 11.15 (**a**, **d**) Schematic diagram illustrating the formation of a closed-loop path inside AlGaN nanowire arrays and AlGaN nanowire double heterostructures. (**b**) Emission spectra measured at 6 K under different current densities. (**c**) Integrated intensity of the lasing peak at 334.1 nm as a function of injection current density. (**e**) Plot of peak position versus current density. (**f**) EL spectra measured at different operation temperatures. (Reprinted with permission from Ref. [87] Copyright 2015 by the Nature Publishing Group)

composite nanowire structure. Similar to plasmonic lasers, metal loss has been identified as the primary loss mechanism in electrically pumped cavities [85]. Overcoming this has been a high priority and has been pursued through several different approaches.

Lithographic, top-down techniques are currently the most viable approach for producing electrically driven nanowire lasers. In the first report of electrically pumped nanowire lasing around 509 nm, a horizontal CdS nanowire on a Si (p^{2+}) substrate was coated with an insulating layer of Al_2O_3 followed by a Ti–Au injection layer [55]. Almost a decade passed before promising device architecture arose, the semiconductor core–metal shell [79] structure, which was realized using a top-down fabrication process [86].

Another strategy for electrical pumping relies on nanowire arrays grown directly on conducting substrates followed by post-synthetic introduction of the second contact. Highly stable, electrically pumped random lasing in AlGaN nanowire arrays has recently been reported [87]. As shown in Fig. 11.15, by using the Anderson localization of light in AlGaN–GaN heterostructures, random lasing in the UV spectral region was achieved in a lithography-free nanowire array. Successful continuous-wave operation was observed from 6 to 100 K, with a lasing threshold

of 12 A cm^{-2} and an operational stability at over six times the threshold current. Emission wavelength tunability across the entire ultraviolet AII (UV-AII) band (~320–340 nm) was also observed for various regions depending on the nature of the gain cavity.

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